# AMC3302 高精度、±50mV 入力、強化絶縁型アンプ DC/DC コンバータ内蔵

## 1 特長

- 3.3V または 5V 単一電源、DC/DC コンバータ内蔵
- シャント抵抗による電流測定用に最適化された ±50mV の入力電圧範囲
- 固定ゲイン:41
- 小さな DC 誤差:
  - オフセット電圧:±50µV (最大値)
  - オフセット・ドリフト:±0.5µV/°C (最大値)
  - ゲイン誤差:±0.2% (最大値)
  - ゲインの温度特性:±35ppm/°C (最大値)
  - 非線形性:±0.03% (最大値)
- 高 CMTI:95 kV/µs (最小値)
- システム・レベル診断機能
- CISPR-11 および CISPR-25 EMI 規格に準拠
- 安全関連の認証:
  - DIN VDE V 0884-11 に準拠した強化絶縁耐圧:6000$V_{PK}$
  - UL 1577 に準拠した絶縁耐圧:4250$V_{RMS}$ (1 分間)
- 拡張産業用温度範囲全体にわたって仕様を完全に規定:–40°C～+125°C

## 2 アプリケーション

- 次の用途における絶縁型電流センシング:
  - 保護リレー
  - モーター・ドライブ
  - 電源
  - 太陽光発電インバータ

## 3 概要

AMC3302 は、シャントによる電流測定に最適化された高精度絶縁型アンプです。完全に統合された絶縁型 DC/DC コンバータのおかげで、本デバイスの低電圧側から電力を供給する単一電源動作が可能であるため、スペースに制約があるアプリケーション向けのユニークなソリューションとして活用できます。その容量性強化絶縁バリアは、VDE V 0884-11 および UL1577 により認証済みであり、最大 1.2k$V_{RMS}$ の使用電圧に対応しています。

この絶縁バリアは、各種の同相電圧レベルで動作するシステム領域を分離し、危険な電圧と損傷から低電圧側を保護します。

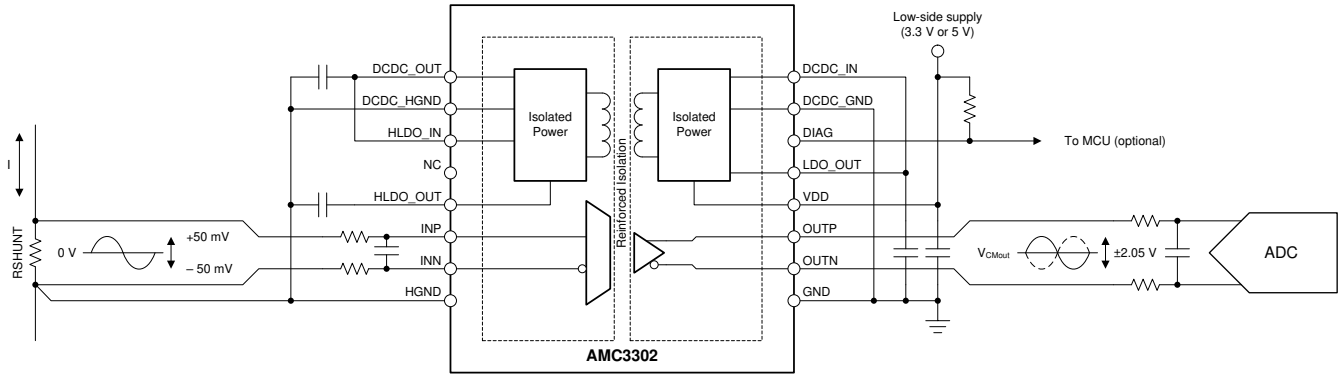
AMC3302 の入力は、低インピーダンスのシャント抵抗またはその他の信号レベルが小さい低インピーダンス電圧源と直接接続できるように最適化されています。優れた DC 精度と小さい温度ドリフトにより、拡張産業用温度範囲 (–40°C～+125°C) にわたる高精度電流測定に対応できます。

AMC3302 の内蔵 DC/DC コンバータ・フォルト検出および診断出力ピンを使用すると、システム・レベルの設計と診断を簡素化できます。

**製品情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| AMC3302 | SOIC (16) | 10.30mm × 7.50mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**代表的なアプリケーション**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision A (February 2021) to Revision B (July 2021)** — **Page**

- Changed LDO_OUT pin description in *Pin Functions* table to include that no external load is allowed on the LDO_OUT pin ... 3
- Changed overvoltage category for rated mains voltage ≤ 600 V from I-IV to I-III and for rated mains voltage ≤1000 V from I-III to I-II ... 6
- Changed $C_{IO}$ from ~3.5 pF to ~4.5 pF ... 6
- Changed output bandwidth (BW) minimum value from 300 kHz to 290 kHz ... 8
- Changed CMTI limits from 85 kV/µs (min), 135 kV/µs (typ) to 95 kV/µs (min), 155 kV/µs (typ) ... 8
- Added discussion of high-side and low-side LDO to *What to Do and What Not to Do* section ... 26
- Added information on reducing radiated emission to *Power Supply Recommendations* section, changed *Recommended External Components* table ... 27
- Added ferrite beads to *Recommended Layout of the AMC3302* figure ... 29

**Changes from Revision * (August 2020) to Revision A (February 2021)** — **Page**

- ドキュメントのステータスを事前情報から量産データに変更 ... 1
- Added $VDD_{UV}$ and $VDD_{POR}$ specifications ... 8


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# 5 Pin Configuration and Functions

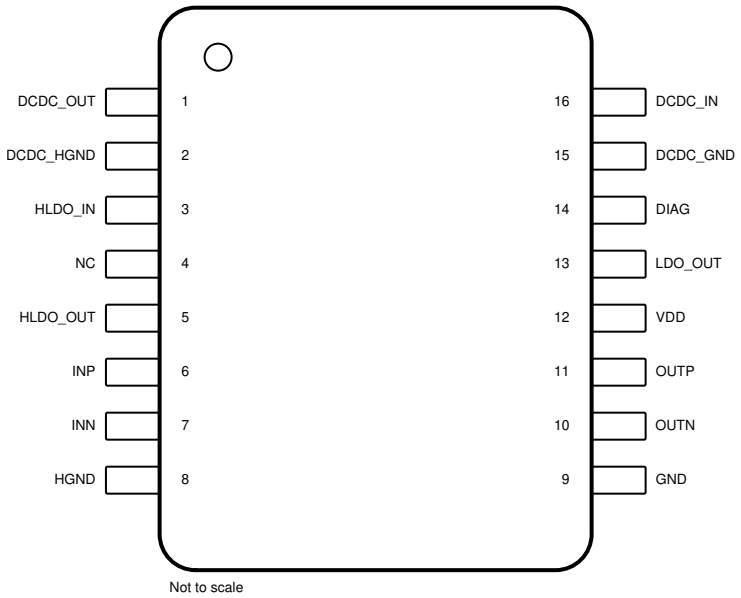


**図 5-1. DWE Package, 16-Pin SOIC, Top View**

**表 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DCDC_OUT | Power | High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin.(1) |
| 2 | DCDC_HGND | High-side power ground | High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin. |
| 3 | HLDO_IN | Power | Input of the high-side LDO; connect this pin to the DCDC_OUT pin(1) |
| 4 | NC | — | No internal connection; connect this pin to HGND or leave this pin unconnected. |
| 5 | HLDO_OUT | Power | Output of the high-side LDO.(1) |
| 6 | INP | Analog input | Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2) |
| 7 | INN | Analog input | Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2) |
| 8 | HGND | High-side signal ground | High-side analog ground; connect this pin to the DCDC_HGND pin. |
| 9 | GND | Low-side signal ground | Low-side analog ground; connect this pin to the DCDC_GND pin. |
| 10 | OUTN | Analog output | Inverting analog output. |
| 11 | OUTP | Analog output | Noninverting analog output. |
| 12 | VDD | Low-side power | Low-side power supply.(1) |
| 13 | LDO_OUT | Power | Output of the low-side LDO; connect this pin to the DCDC_IN pin. The output of the LDO must not be loaded by external circuitry.(1) |
| 14 | DIAG | Digital output | Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used. |
| 15 | DCDC_GND | Low-side power ground | Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin. |
| 16 | DCDC_IN | Power | Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin.(1) |

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

see (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power-supply voltage | VDD to GND | –0.3 | 6.5 | V |
| Analog input voltage | INP, INN | HGND – 6 | $V_{HLDO_OUT}$ + 0.5 | V |
| Analog output voltage | OUTP, OUTN | GND – 0.5 | VDD + 0.5 | V |
| Digital output voltage | DIAG | GND – 0.5 | 6.5 | V |
| Input current | Continuous, any pin except power-supply pins | –10 | 10 | mA |
| Temperature | Junction, $T_J$ | | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged device model (CDM), per JESD22-C101 (2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| VDD | Low-side power supply | VDD to GND | 3 | 3.3 | 5.5 | V |
| **ANALOG INPUT** | | | | | | |
| $V_{Clipping}$ | Differential input voltage before clipping output | $V_{IN} = V_{INP} – V_{INN}$ | | ±64 | | mV |
| $V_{FSR}$ | Specified linear differential full-scale voltage | $V_{IN} = V_{INP} – V_{INN}$ | –50 | | 50 | mV |
| | Absolute common-mode input voltage (1) | $(V_{INP} + V_{INN}) / 2$ to HGND | –2 | | $V_{HLDO_OUT}$ | V |
| $V_{CM}$ | Operating common-mode input voltage | $(V_{INP} + V_{INN}) / 2$ to HGND | –0.032 | | 1 | V |
| **TEMPERATURE RANGE** | | | | | | |
| $T_A$ | Specified ambient temperature | | –40 | | 125 | °C |

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage $V_{CM}$ for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | AMC3302 DWE (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 31 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44 | °C/W |
| $Y_{JT}$ | Junction-to-top characterization parameter | 16.7 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 42.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation | VDD = 5.5 V | | | 231 | mW |
| | | VDD = 3.6 V | | | 151 | |

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## 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance (1) | Shortest pin-to-pin distance through air | ≥ 8 | mm |
| CPG | External creepage (1) | Shortest pin-to-pin distance across the package surface | ≥ 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance - capacitive signal isolation) | ≥ 21 | µm |
| | | Minimum internal gap (internal clearance - transformer power isolation) | ≥ 120 | |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥ 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I-III | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-II | |
| **DIN VDE V 0884-11 (VDE V 0884-11): 2017-01**(2) | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | At AC voltage (bipolar) | 1700 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum-rated isolation working voltage | At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test | 1200 | $V_{RMS}$ |
| | | At DC voltage | 1700 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification test) | 6000 | $V_{PK}$ |
| | | $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test) | 7200 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification) | 6250 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m$ = 10 s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m$ = 10 s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini}$ = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m$ = 1 s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.5 $V_{PP}$ at 1 MHz | ~4.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output(5) | $V_{IO}$ = 500 V at $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V at 100°C ≤ $T_A$ ≤ 125°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO}$ = 4250 $V_{RMS}$ or 6000 $V_{DC}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test) | 4250 | $V_{RMS}$ |

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.


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## 6.7 Safety-Related Certifications

| VDE | UL |
|---|---|
| Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01,<br>DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and<br>DIN EN 60065 (VDE 0860): 2005-11 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Reinforced insulation | Single protection |
| Certificate number: 40040142 | File number: E181974 |

## 6.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V,<br>$T_J$ = 150°C, $T_A$ = 25°C | | | 309 | mA |
| | | $R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V,<br>$T_J$ = 150°C, $T_A$ = 25°C | | | 472 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 73.5°C/W, $T_J$ = 150°C,<br>$T_A$ = 25°C | | | 1700 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of $I_S$ and $P_S$. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where $VDD_{max}$ is the maximum low-side voltage.

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## 6.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A$ = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and the external components listed in the *Typical Application* section; typical specifications are at $T_A$ = 25°C, and VDD = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| $R_{IN}$ | Single-ended input resistance | INN = HGND | | 4.75 | | kΩ |
| $R_{IND}$ | Differential input resistance | | | 4.9 | | |
| $I_{IB}$ | Input bias current | INP = INN = HGND; $I_{IB}$ = ($I_{IBP}$ + $I_{IBN}$) / 2 | –48.5 | –36 | –28.5 | µA |
| $I_{IO}$ | Input offset current | $I_{IO}$ = $I_{IBP}$ – $I_{IBN}$; INP = INN = HGND | | ±10 | | nA |
| $C_{IN}$ | Single-ended input capacitance | INN = HGND, $f_{IN}$ = 275 kHz | | 4 | | pF |
| $C_{IND}$ | Differential input capacitance | $f_{IN}$ = 275 kHz | | 2 | | pF |
| **ANALOG OUTPUT** | | | | | | |
| | Nominal gain | | | 41 | | V/V |
| $V_{CMout}$ | Common-mode output voltage | | 1.39 | 1.44 | 1.49 | V |
| $V_{CLIPout}$ | Clipping differential output voltage | $V_{OUT}$ = ($V_{OUTP}$ – $V_{OUTN}$); \|$V_{IN}$\| = \|$V_{INP}$ – $V_{INN}$\| > $V_{Clipping}$ | –2.52 | ±2.49 | 2.52 | V |
| $V_{Failsafe}$ | Failsafe differential output voltage | $V_{OUT}$ = ($V_{OUTP}$ – $V_{OUTN}$); $V_{DCDC_OUT}$ ≤ $V_{DCDCUV}$, or $V_{HLDO_OUT}$ ≤ $V_{HLDOUV}$ | –2.63 | –2.57 | –2.53 | V |
| BW | Output bandwidth | | 290 | 340 | | kHz |
| $R_{OUT}$ | Output resistance | On OUTP or OUTN | | 0.2 | | Ω |
| | Output short-circuit current | On OUTP or OUTN, sourcing or sinking, INP = INN = HGND, outputs shorted to either GND or VDD | | 14 | | mA |
| CMTI | Common-mode transient immunity | \|HGND – GND\| = 2 kV | 95 | 155 | | kV/µs |
| **ACCURACY** | | | | | | |
| $V_{OS}$ | Input offset voltage(1) (2) | $T_A$ = 25°C, INP = INN = HGND | –50 | ±15 | 50 | µV |
| $TCV_{OS}$ | Input offset drift (1) (2) (4) | | –0.5 | ±0.1 | 0.5 | uV/°C |
| $E_G$ | Gain error(1) | $T_A$ = 25°C | –0.2% | ±0.04% | 0.2% | |
| $TCE_G$ | Gain error drift(1) (5) | | –35 | ±10 | 35 | ppm/°C |
| | Nonlinearity (1) | | –0.03% | ±0.002% | 0.03% | |
| SNR | Signal-to-noise ratio | $V_{IN}$ = 0.1 $V_{PP}$, $f_{IN}$ = 1 kHz, BW = 10 kHz, 10 kHz filter | 77 | 81 | | dB |
| | | $V_{IN}$ = 0.1 $V_{PP}$, $f_{IN}$ = 10 kHz, BW = 100 kHz, 1 MHz filter | | 70 | | |
| THD | Total harmonic distortion(3) | $V_{IN}$ = 0.1 Vpp, $f_{IN}$ = 10 kHz, BW = 100 kHz | | –85 | | dB |
| | Output noise | INP = INN = HGND, $f_{IN}$ = 0 Hz, BW = 100 kHz | | 340 | | $\mu V_{RMS}$ |
| CMRR | Common-mode rejection ratio | $f_{IN}$ = 0 Hz, $V_{CM\ min}$ ≤ $V_{CM}$ ≤$V_{CM\ max}$ | | –101 | | dB |
| | | $f_{IN}$ = 10 kHz, $V_{CM\ min}$ ≤ $V_{CM}$ ≤$V_{CM\ max}$ | | –101 | | |
| PSRR | Power-supply rejection ratio | VDD from 3.0 V to 5.5 V, at dc, input referred | | –120 | | dB |
| | | INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred | | –108 | | |


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## 6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A$ = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and the external components listed in the *Typical Application* section; typical specifications are at $T_A$ = 25°C, and VDD = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| IDD | Low-side supply current | no external load on HLDO | | 27.5 | 40 | mA |
| | | 1 mA external load on HLDO | | 29.5 | 42 | |
| $VDD_{UV}$ | VDD analog undervoltage detection threshold | VDD rising | | | 2.9 | V |
| | | VDD falling | | | 2.8 | |
| $VDD_{POR}$ | VDD digital reset threshold | VDD rising | | | 2.5 | V |
| | | VDD falling | | | 2.4 | |
| $V_{DCDC_OUT}$ | DCDC output voltage | DCDC_OUT to HGND | 3.1 | 3.5 | 4.65 | V |
| $V_{DCDCUV}$ | DCDC output undervoltage detection threshold voltage | DCDC output falling | 2.1 | 2.25 | | V |
| $V_{HLDO_OUT}$ | High-side LDO output voltage | HLDO to HGND, up to 1 mA external load | 3 | 3.2 | 3.4 | V |
| $V_{HLDOUV}$ | High-side LDO output undervoltage detection threshold voltage | HLDO output falling | 2.4 | 2.6 | | V |
| $I_H$ | High-side supply current for auxiliary circuitry | Load connected from HLDO_OUT to HGND, non-switching | | | 1 | mA |
| $t_{AS}$ | Analog settling time | VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling | | 0.9 | 1.4 | ms |

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25℃)} \times TempRange) \times 10^6$

## 6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Output signal rise time | | | 1.3 | | µs |
| $t_f$ | Output signal fall time | | | 1.3 | | µs |
| | $V_{INx}$ to $V_{OUTx}$ signal delay (50% – 10%) | Unfiltered output | | 1.2 | 1.5 | µs |
| | $V_{INx}$ to $V_{OUTx}$ signal delay (50% – 50%) | Unfiltered output | | 1.6 | 2.1 | µs |
| | $V_{INx}$ to $V_{OUTx}$ signal delay (50% – 90%) | Unfiltered output | | 2.3 | 3 | µs |

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## 6.11 Timing Diagram

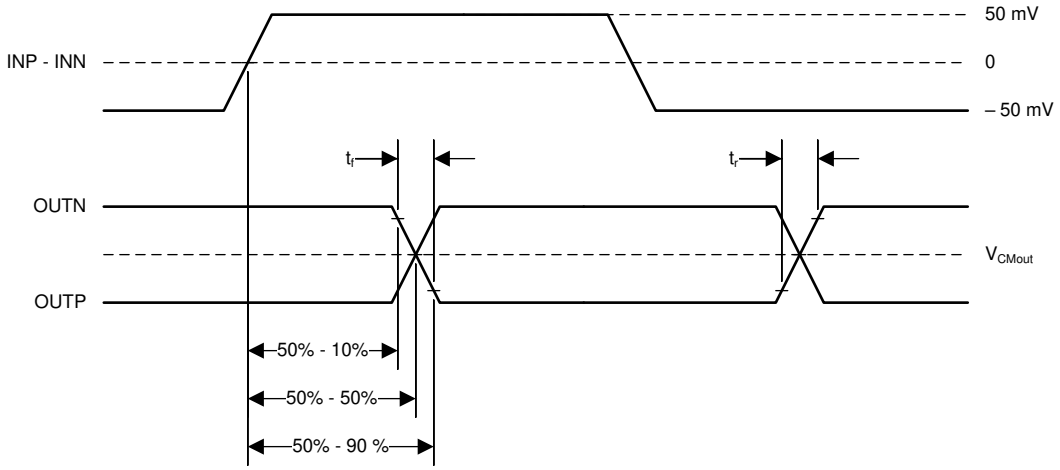


**図 6-1. Rise, Fall, and Delay Time Waveforms**


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## 6.12 Insulation Characteristics Curves

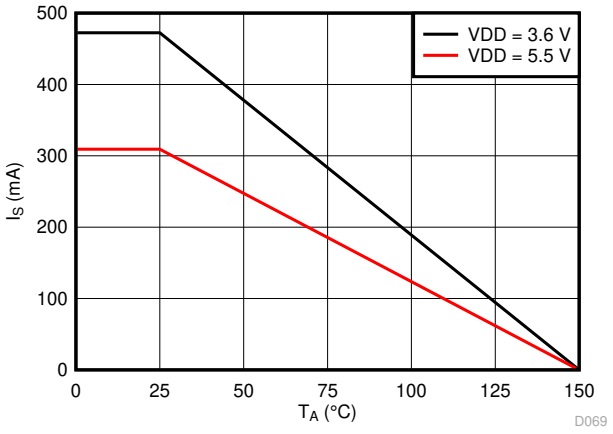



**図 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE**

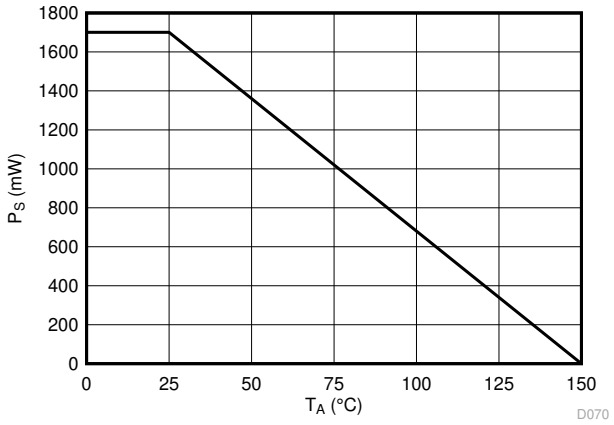
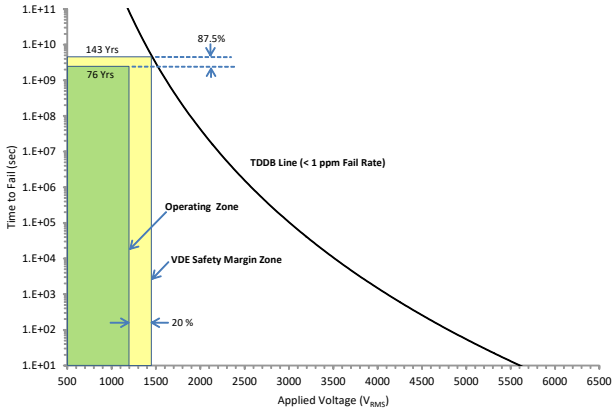



**図 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE**




$T_A$ up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1200 $V_{RMS}$, operating lifetime = 76 years

**図 6-4. Reinforced Isolation Capacitor Lifetime Projection**

## 6.13 Typical Characteristics

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)

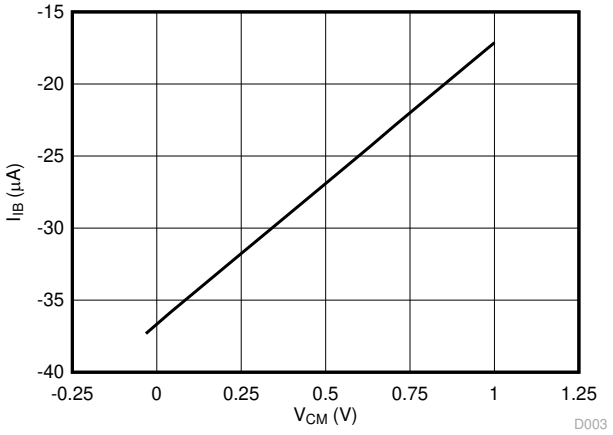



図 6-5. Input Bias Current vs Common-Mode Input Voltage

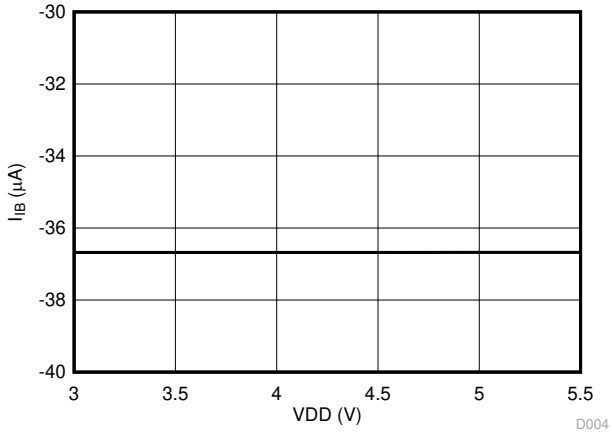



図 6-6. Input Bias Current vs Supply Voltage

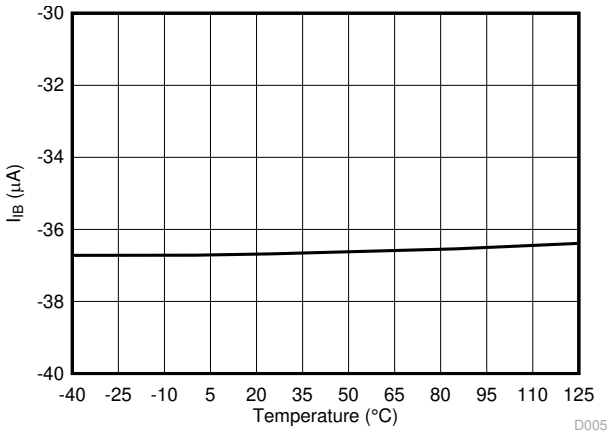



図 6-7. Input Bias Current vs Temperature

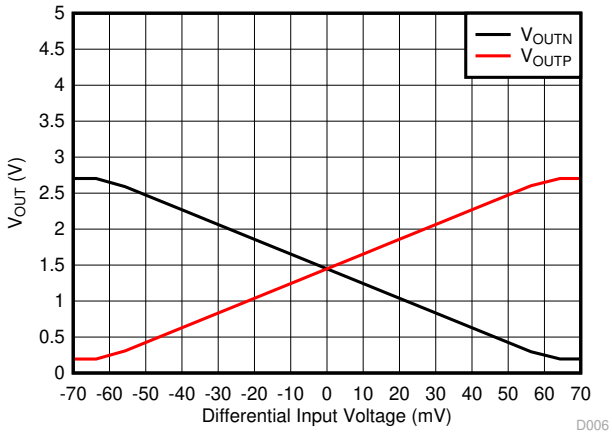



図 6-8. Output Voltage vs Input Voltage

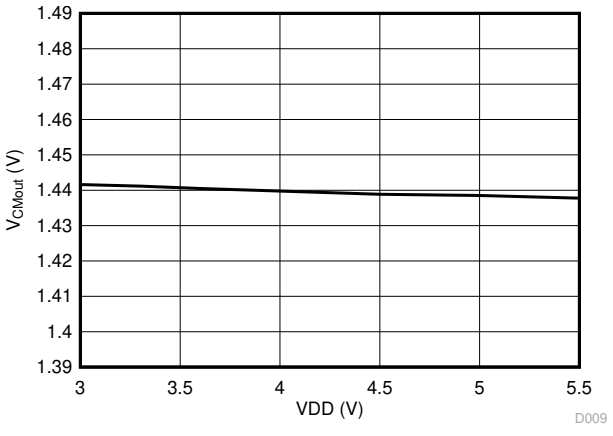



図 6-9. Output Common-Mode Voltage vs Supply Voltage

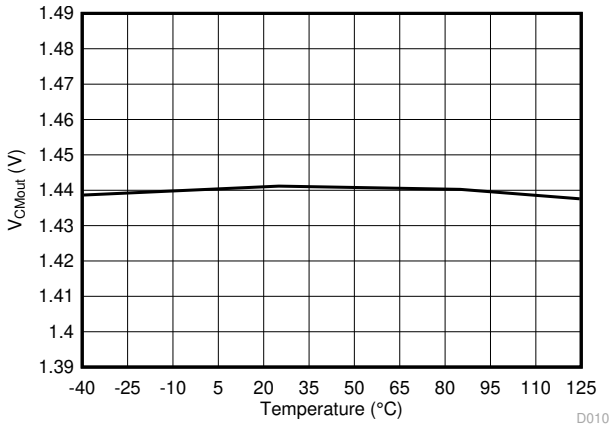



図 6-10. Output Common-Mode Voltage vs Temperature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## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)

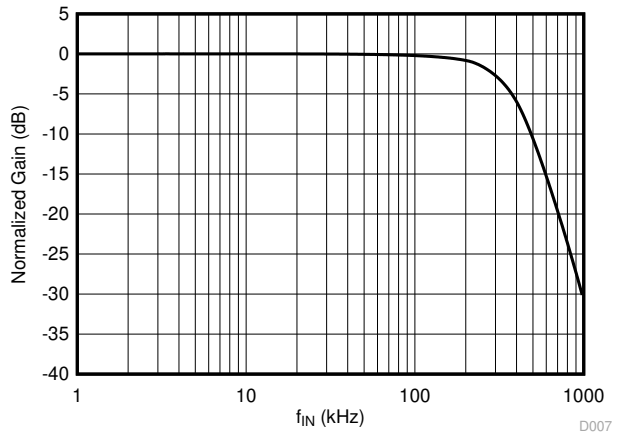


図 6-11. Normalized Gain vs Input Frequency

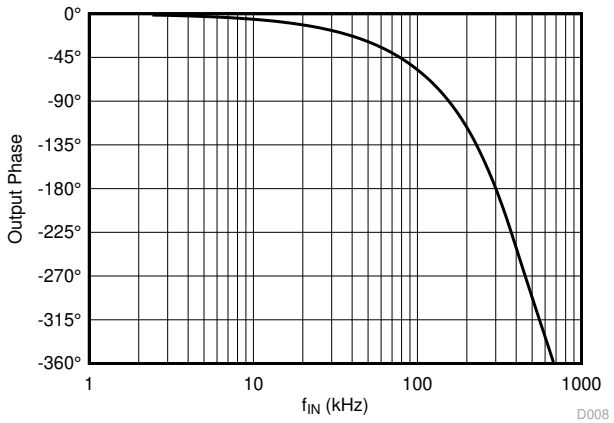


図 6-12. Output Phase vs Input Frequency

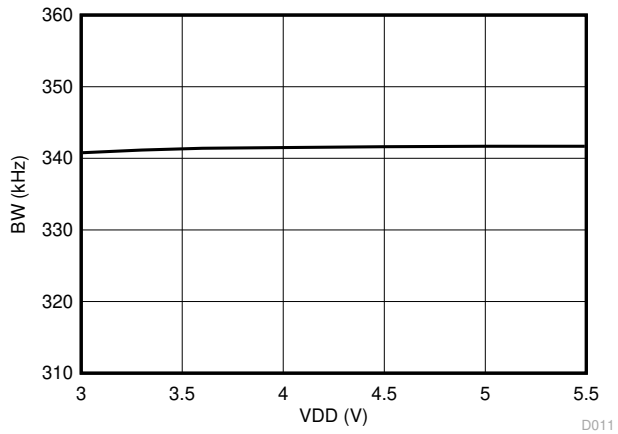


図 6-13. Output Bandwidth vs Supply Voltage

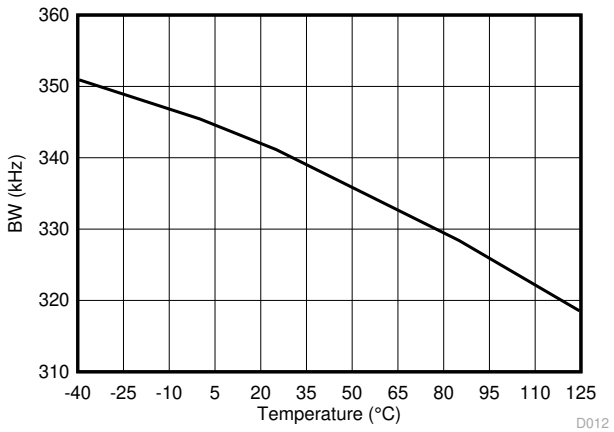


図 6-14. Output Bandwidth vs Temperature

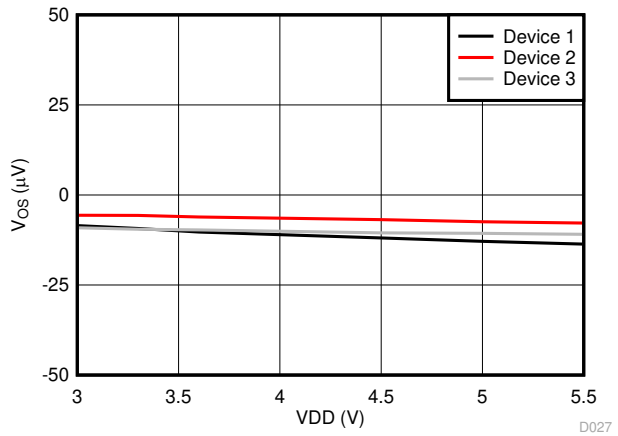


図 6-15. Input Offset Voltage vs Supply Voltage

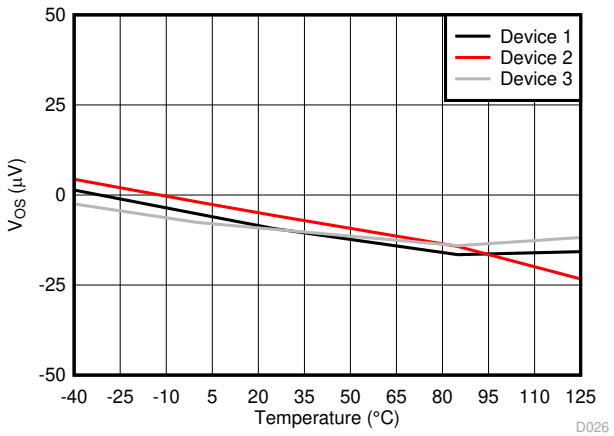


図 6-16. Input Offset Voltage vs Temperature

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## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)

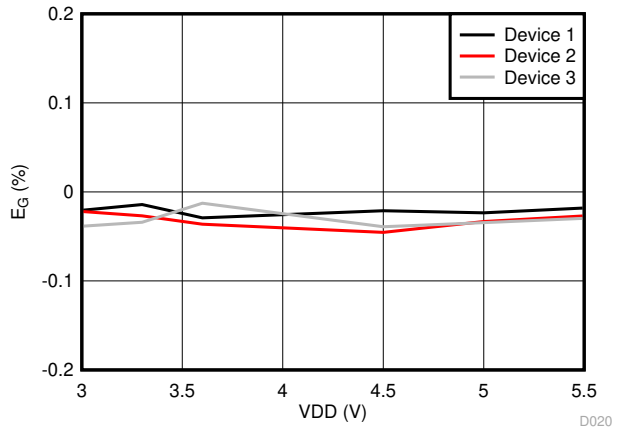



図 6-17. Gain Error vs Supply Voltage

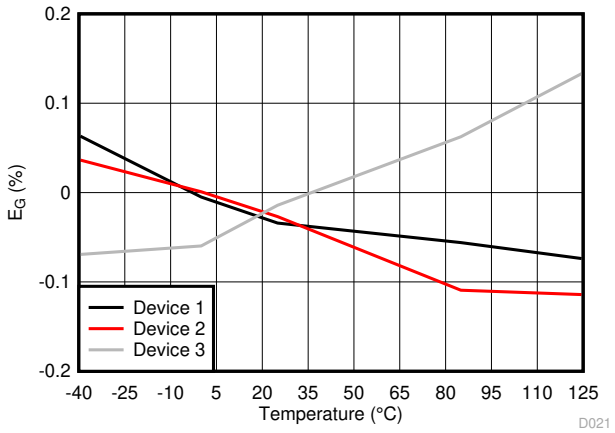



図 6-18. Gain Error vs Temperature

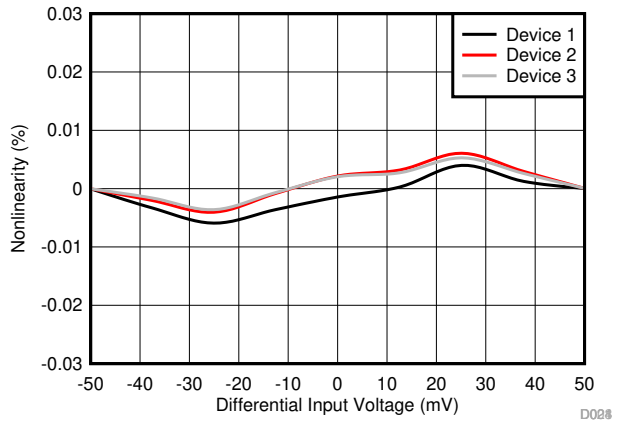



図 6-19. Nonlinearity vs Input Voltage

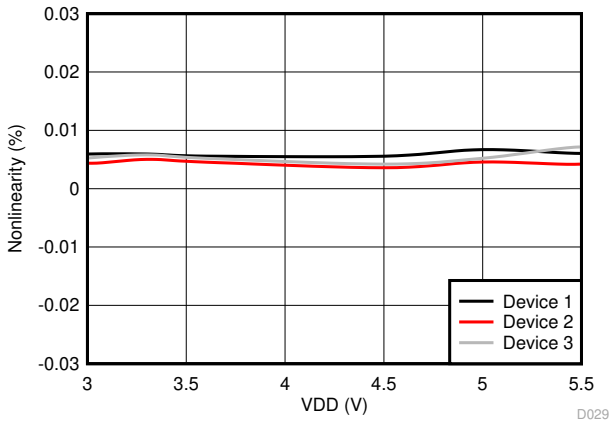



図 6-20. Nonlinearity vs Supply Voltage

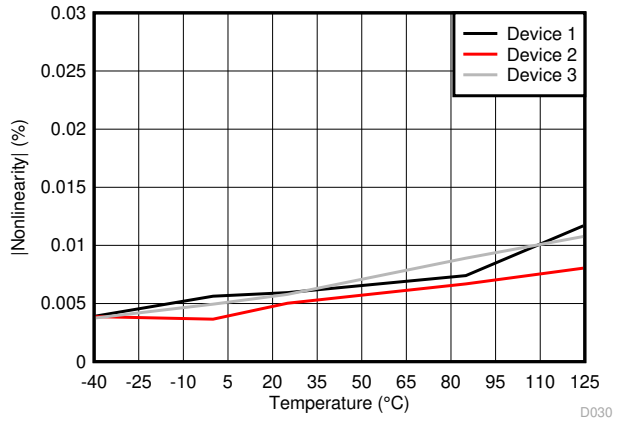
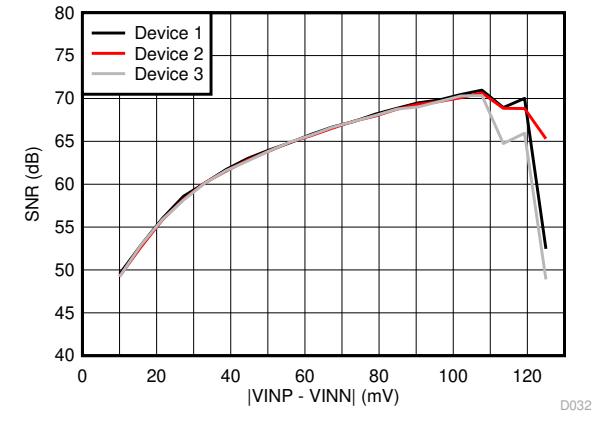



図 6-21. Nonlinearity vs Temperature




$V_{IN}$ = 0.1 $V_{pp}$, $f_{IN}$ = 10 kHz

図 6-22. Signal-to-Noise Ratio vs Input Voltage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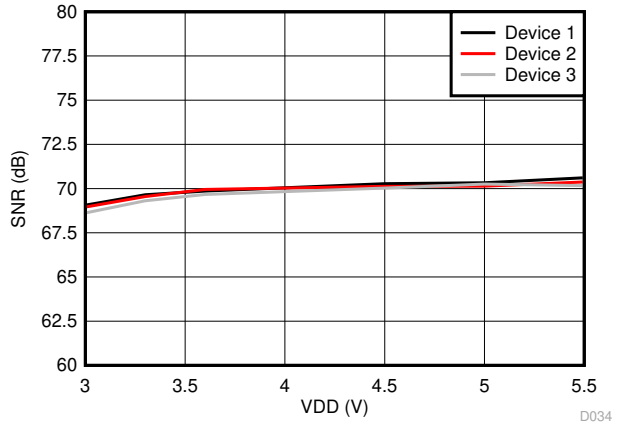
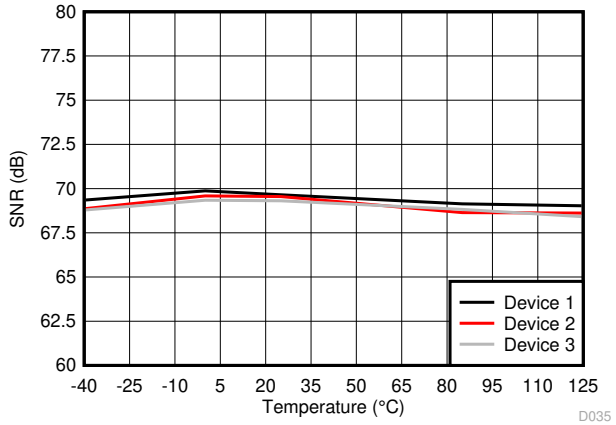
## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)




$V_{IN}$ = 0.1 $V_{pp}$, $f_{IN}$ = 10 kHz

**図 6-23. Signal-to-Noise Ratio vs Supply Voltage**




$V_{IN}$ = 0.1 $V_{pp}$, $f_{IN}$ = 10 kHz

**図 6-24. Signal-to-Noise Ratio vs Temperature**

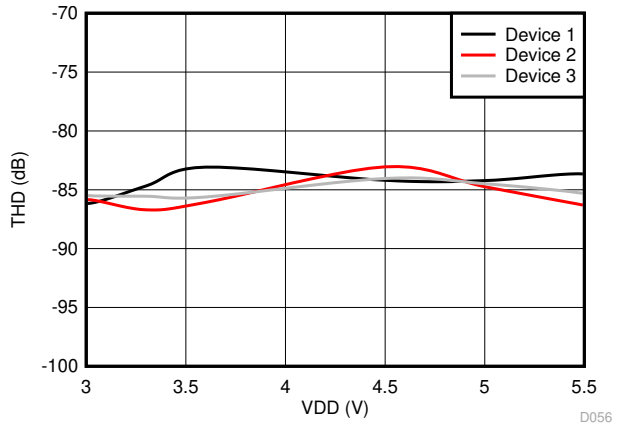



**図 6-25. Total Harmonic Distortion vs Supply Voltage**

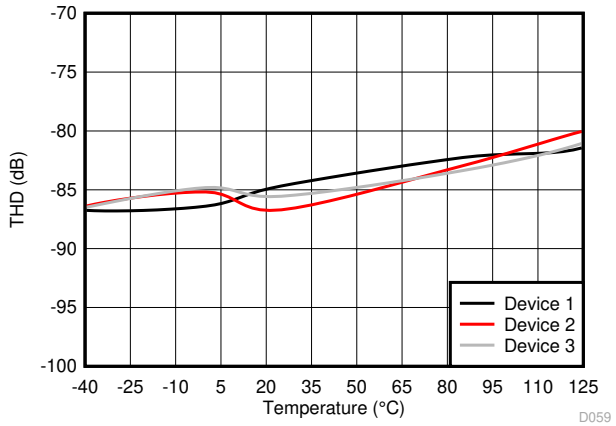



**図 6-26. Total Harmonic Distortion vs Temperature**

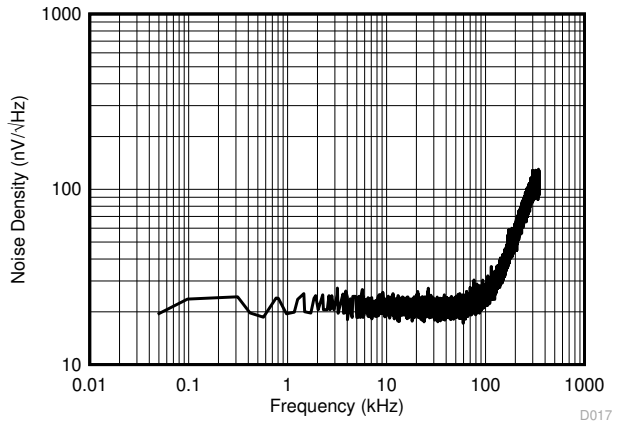



**図 6-27. Input-Referred Noise Density vs Frequency**

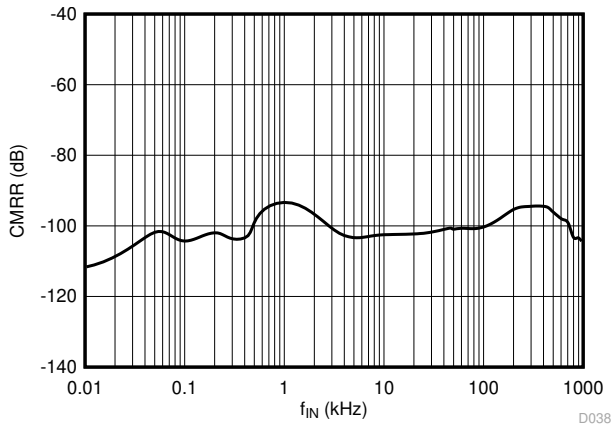



**図 6-28. Common-Mode Rejection Ratio vs Input Frequency**

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## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)

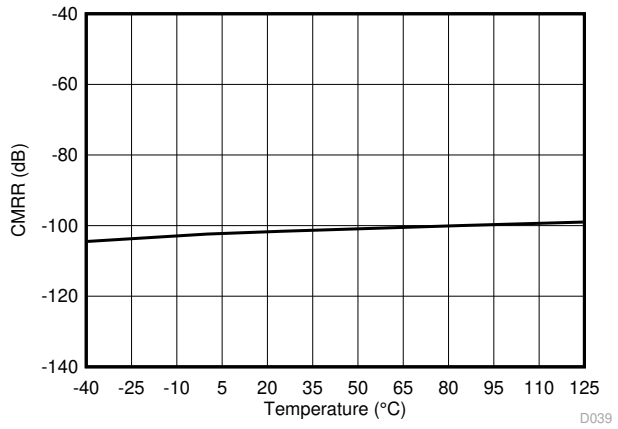


図 6-29. Common-Mode Rejection Ratio vs Temperature

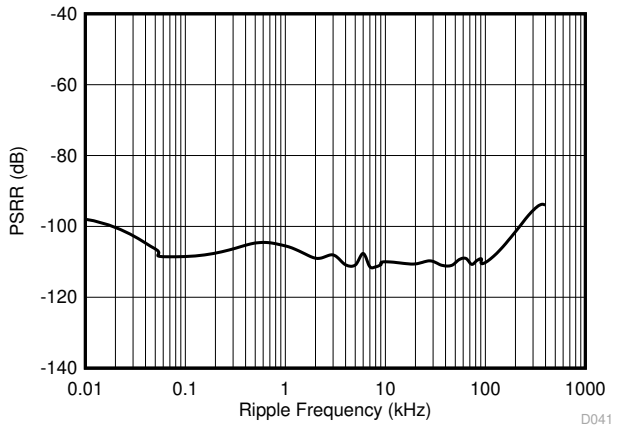


図 6-30. Power-Supply Rejection Ratio vs Ripple Frequency

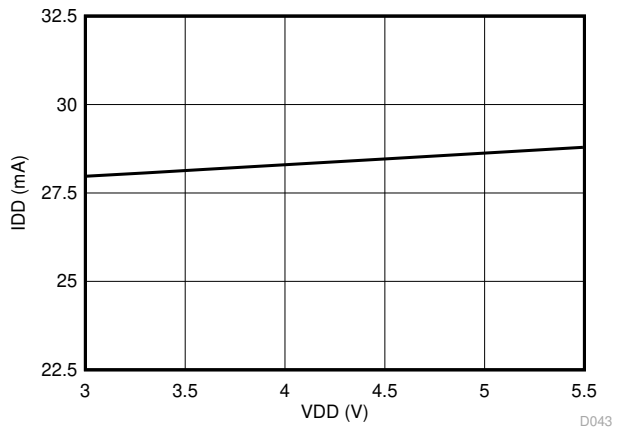


図 6-31. Supply Current vs Supply Voltage

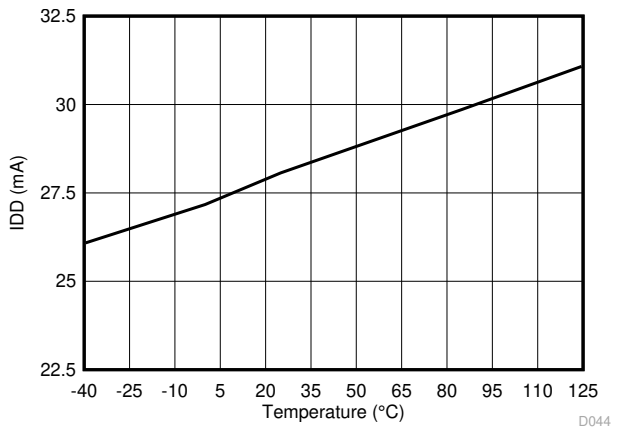


図 6-32. Supply Current vs Temperature

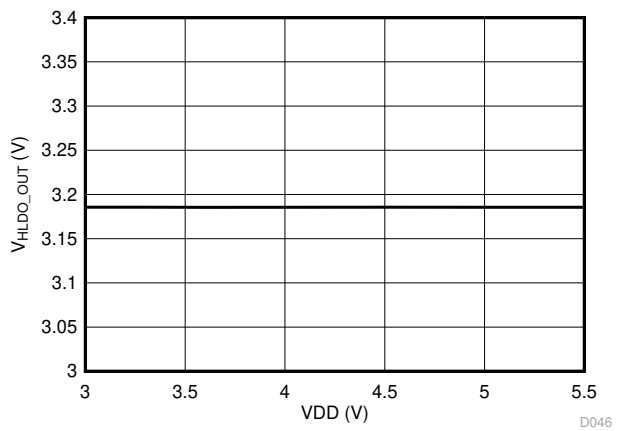


図 6-33. High-Side LDO Line Regulation

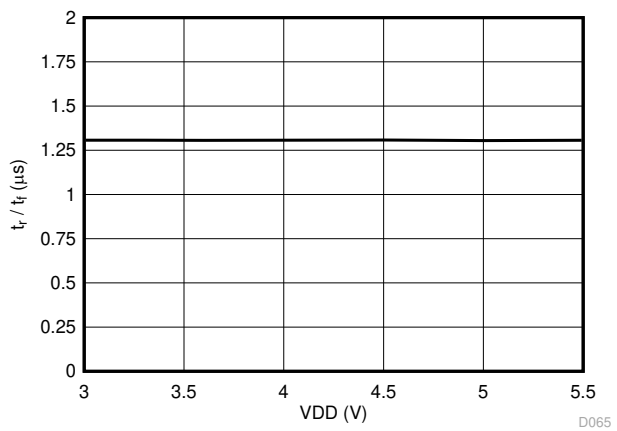


図 6-34. Output Rise and Fall time vs Supply Voltage


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## 6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND = 0 V, and $f_{IN}$ = 10 kHz (unless otherwise noted)

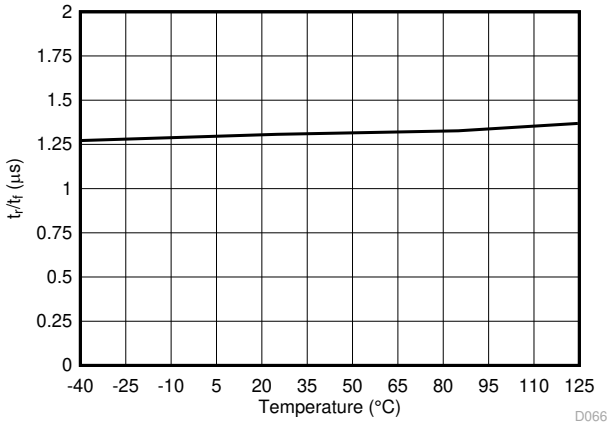



図 6-35. Output Rise and Fall Time vs Temperature

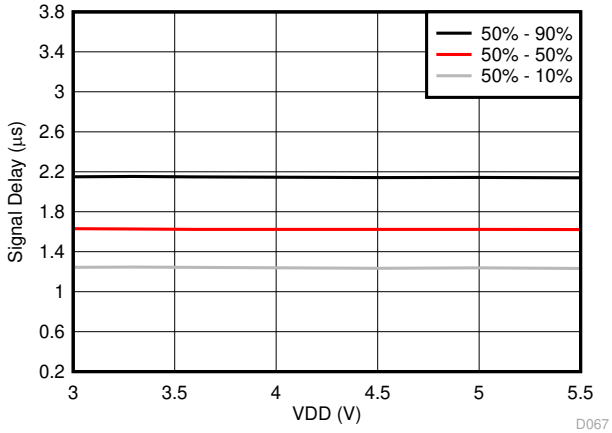



図 6-36. $V_{IN}$ to $V_{OUT}$ Signal Delay vs Supply Voltage

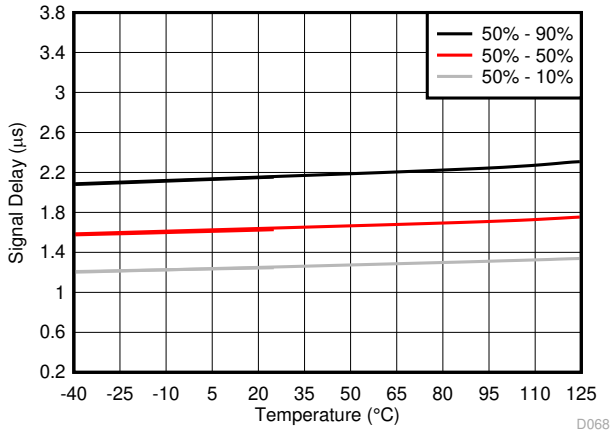



図 6-37. $V_{IN}$ to $V_{OUT}$ Signal Delay vs Temperature

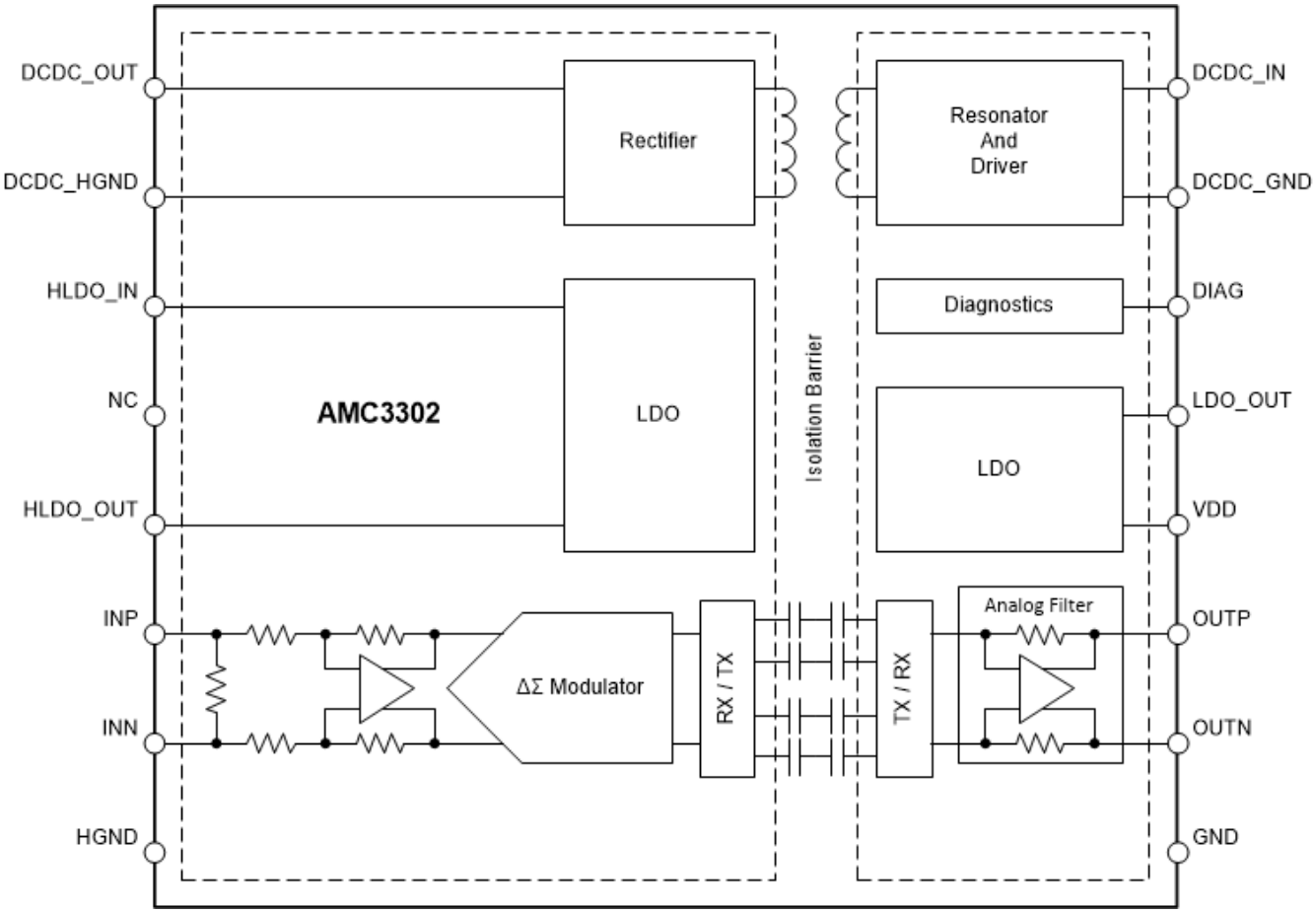
# 7 Detailed Description

## 7.1 Overview

The AMC3302 is a fully differential, precision, isolated amplifier with an integrated DC/DC converter that can supply the device from a single 3.3-V or 5-V voltage supply on the low-side. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the highside from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The signal path is isolated by a double capacitive silicon dioxide ($SiO_2$) insuation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Analog Input

The differential amplifier input stage of the AMC3302 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of $R_{IND}$. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Data Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltages $V_{INP}$ or $V_{INN}$ exceed the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value, because the device input electrostatic discharge (ESD) diodes turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within linear full-scale range ($V_{FSR}$) and within the common-mode input voltage range ($V_{CM}$) as specified in the *Recommended Operating Conditions* table.

### 7.3.2 Data Isolation Channel Signal Transmission

The AMC3302 uses an on-off keying (OOK) modulation scheme, as shown in 図 7-1, to transmit the modulator output bitstream across the capacitive $SiO_2$-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3302 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC3302 transmission (TX) channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

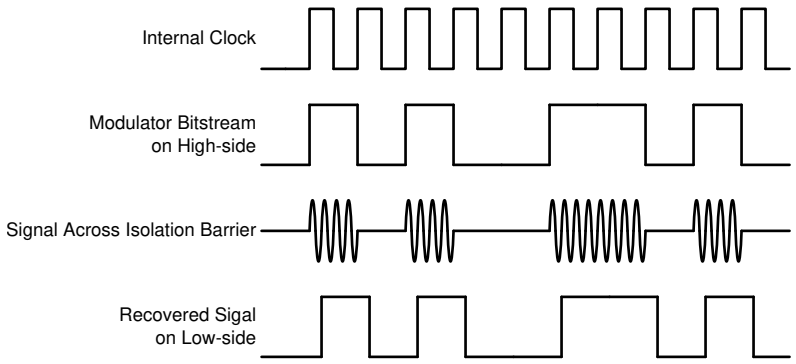


**図 7-1. OOK-Based Modulation Scheme**

### 7.3.3 Analog Output

The AMC3302 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ($V_{INP} – V_{INN}$) in the range from –50 mV to 50 mV, the device provides a linear response with a nominal gain of 41. For example, for a differential input voltage of 50 mV, the differential output voltage ($V_{OUTP} – V_{OUTN}$) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage $V_{CMout}$, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 50 mV but less than 64 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 図 7-2, if the differential input voltage exceeds the $V_{Clipping}$ value.

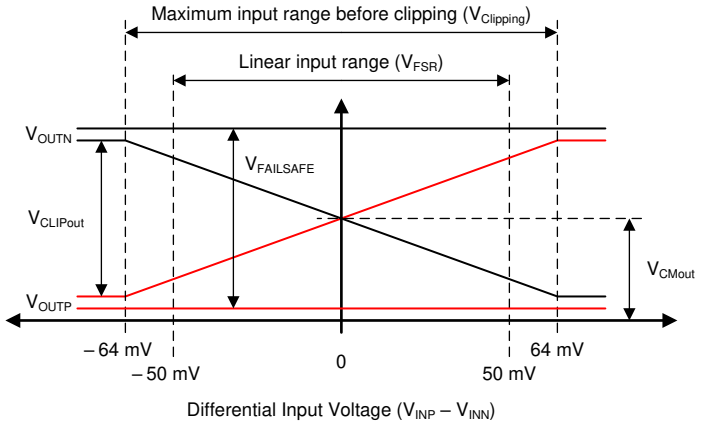


**図 7-2. Output Behavior of the AMC3302**

The AMC3302 provides a failsafe output that simplifies diagnostics on system level. 図 7-2 shows the failsafe mode, in which the AMC3302 outputs a negative differential output voltage that does not occur under normal operating conditions. The failsafe output is active in two cases:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side)
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out)

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the failsafe detection on the system level.

### 7.3.4 Isolated DC/DC Converter

The AMC3302 offers a fully integrated isolated DC/DC converter that includes following components illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side side to stabilize the supply voltage VDD that drives the low-side of the converter. This circuit does not output a constant voltage and is not intended for driving any external load.
- Low-side full-bridge inverter and drivers.
- Laminate-based, air-core transformer for high immunity to magnetic fields.
- High-side full-bridge rectifier.
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path.

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the ΔΣ modulator to minimize the interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3302 and can source up to $I_H$ of additional DC current for an optional auxiliary circuit such as an active filter, preamplifier, or comparator. $I_H$ is specified in the *Electrical Characteristics* table as a DC, non-switching current.


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### 7.3.5 Diagnostic Output

As shown in 図 7-3, the open-drain DIAG pin can be monitored to confirm the device is operational and the output voltage is valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. During normal operation, the DIAG pin is in high-impedance (Hi-Z) state and is pulled high through an external pullup resistor. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side). In this case, the amplifier outputs are driven to the $V_{FAILSAFE}$ value, see 図 7-2.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. The amplifier outputs are driven to $V_{FAILSAFE}$ value, see 図 7-2.

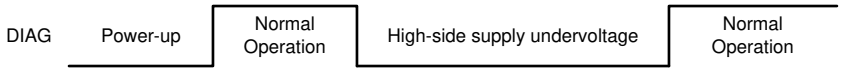


**図 7-3. DIAG Output Under Different Operating Conditions**

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pullup resistor or leave open if not used.

## 7.4 Device Functional Modes

The AMC3302 is operational when the power supply VDD is applied, as specified in the *Recommended Operating Conditions* table.

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC3302 a high-performance solution for industrial applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

## 8.2 Typical Application

The AMC3302 is ideally suited for shunt-based, current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC3302 integrates an isolated power supply for the high-voltage side and therefore makes the device particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

図 8-1 shows a simplified schematic of the AMC3302 in a solar inverter where the phase current is measured on the grid-side of an LCL filter. Although the system offers a supply for the high-side gate driver, there is a large common-mode voltage between the gate driver supply ground reference and the shunt resistor on the other side of the LCL filter. Therefore, the gate driver supply is not suitable for powering the high-side of an isolated amplifier that measures the voltage across the shunt. The integrated isolated power supply of the AMC3302 solves that problem and enables current sensing at locations that is optimal for the system.

図 8-1 also shows the AMC3330 being used for sensing the AC output voltage.

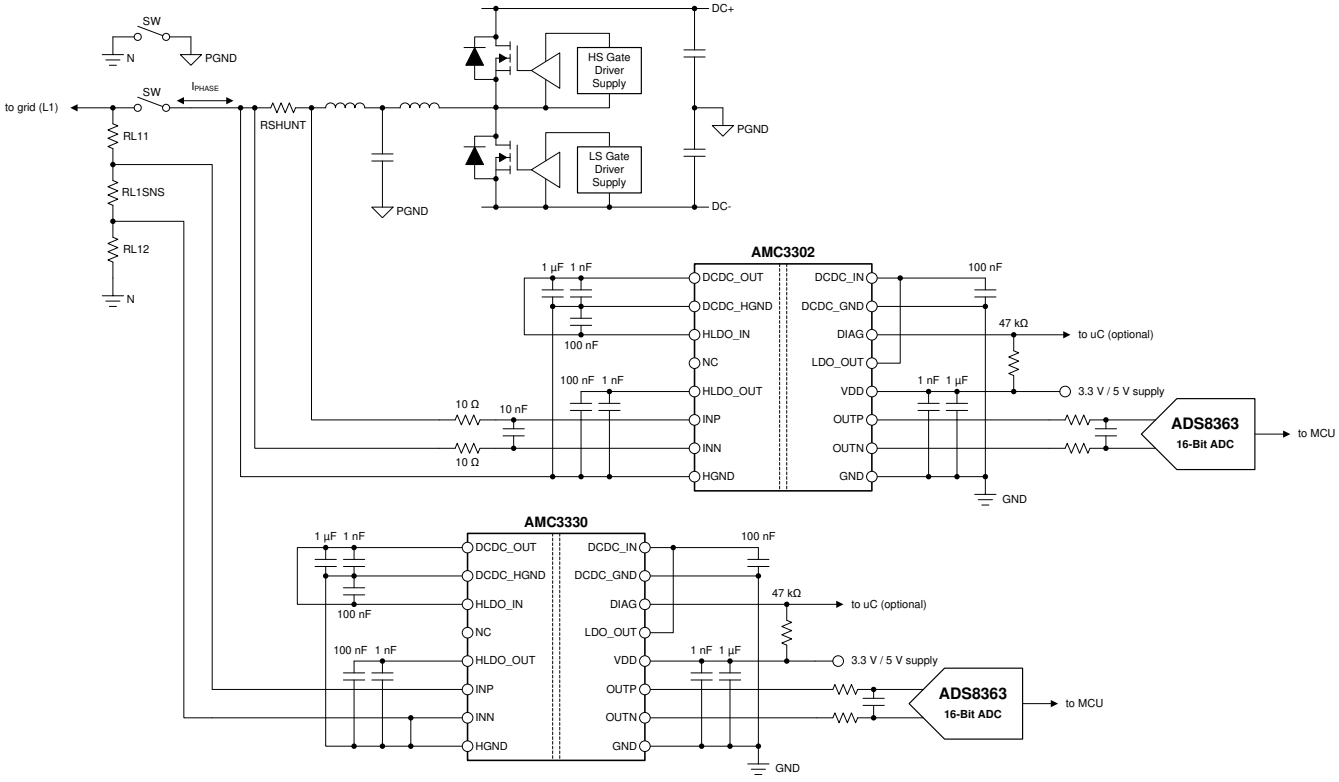


**図 8-1. The AMC3302 in a Solar Inverter Application**


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### 8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

**表 8-1. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| Supply voltage | 3.3 V or 5 V |
| Voltage drop across the shunt for a linear response ($V_{SHUNT}$) | ±50 mV (maximum) |

### 8.2.2 Detailed Design Procedure

The AMC3302 requires a single 3.3-V or 5-V supply on its low side. The high-side supply is internally generated by an integrated DC/DC converter, as explained in the *Isolated DC/DC Converter* section.

The ground reference (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the AMC3302. If a four-pin shunt is used, the inputs of the device are connected to the inner leads and HGND is connected to one of the outer leads. To minimize offset and improve accuracy, set the ground connection to a separate trace that connects directly to the shunt resistor rather than shorting HGND to INN directly at the input to the device. See the *Layout* section for more details.

#### *8.2.2.1 Shunt Resistor Sizing*

Use Ohm's Law to calculate the voltage drop across the shunt resistor ($V_{SHUNT}$) for the desired measured current: $V_{SHUNT} = I \times RSHUNT$.

Consider the following two restrictions to choose the proper value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

#### *8.2.2.2 Input Filter Design*

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications the structure shown in 図 8-2 achieves excellent performance.

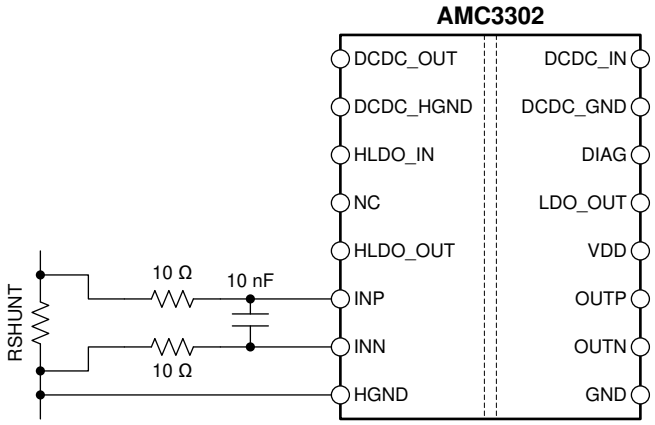


**図 8-2. Differential Input Filter**

#### 8.2.2.3 Differential to Single-Ended Output Conversion

図 8-3 shows an example of a TLV6001-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals ($V_{OUTP}$ – $V_{OUTN}$) + $V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

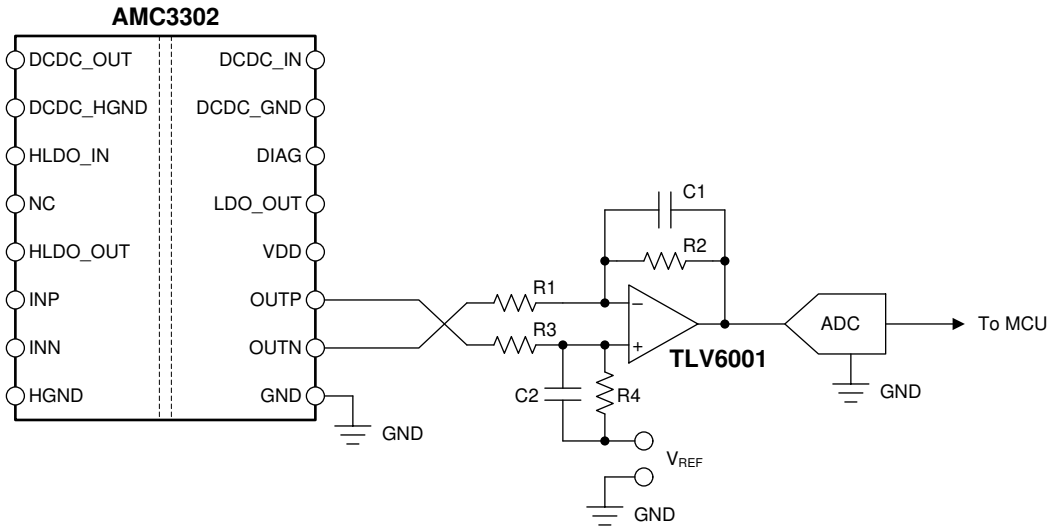


**図 8-3. Connecting the AMC3302 Output to a Single-Ended Input ADC**

For more information on the general procedure to design the filtering and driving stages of successive-approximation-register (SAR) ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide, available for download at www.ti.com.

### 8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. 図 8-4 shows the typical fullscale step response of the AMC3302.


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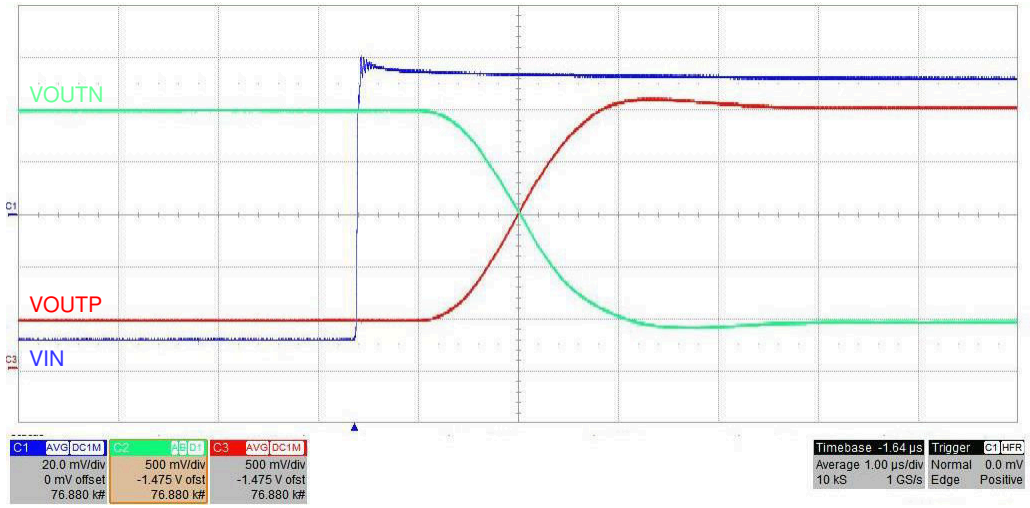


**図 8-4. Step Response of the AMC3302**

## 8.3 What to Do and What Not to Do

Do not leave the analog inputs INP and INN of the AMC3302 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage, leaving the output of the device undetermined.

Connect the negative input (INN) to the high-side ground (HGND), either by a hard short or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

The high-side LDO can source a limited amount of current ($I_H$) to power external circuitry. Take care not to overload the high-side LDO.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the LDO_OUT pin.


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## 9 Power Supply Recommendations

The AMC3302 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V or 5 V. TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in 図 9-1) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3302, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to INN directly at the device input. The high-side DC/DC ground terminal (DCDC_HGND) is shorted to HGND directly at the device pins.

As shown in 図 9-1, TI recommends placing ferrite beads in the INP, INN, and HGND signal lines for best EMI performance. For more information on reducing radiated emissions and guidelines for component selection, see the *Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI* application note available for download at www.ti.com

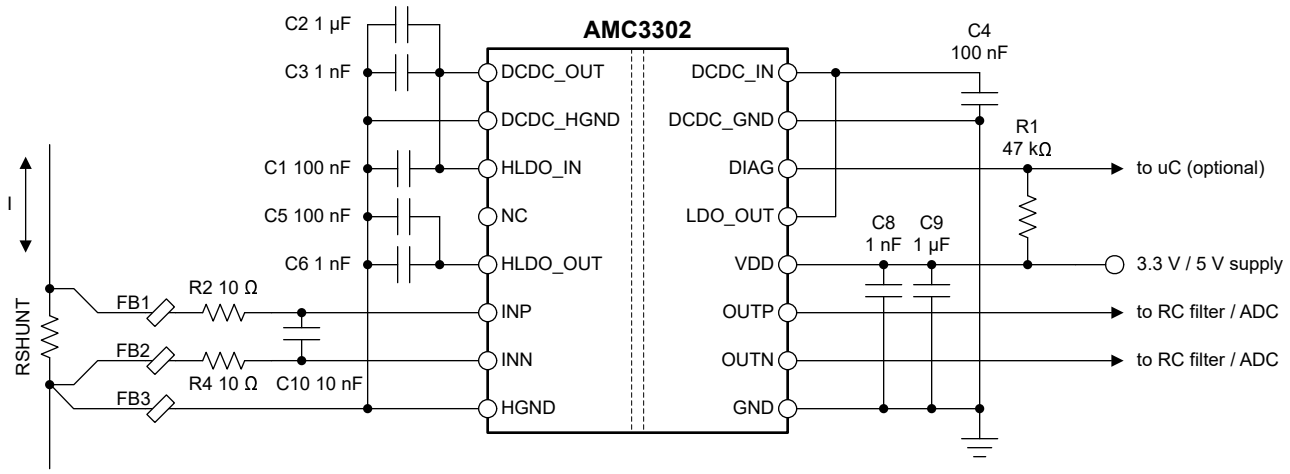


**図 9-1. Decoupling the AMC3302**

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

表 9-1 lists components suitable for use with the AMC3302. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3302.

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**表 9-1. Recommended External Components**

| DESCRIPTION | | PART NUMBER | MANUFACTURER | SIZE (EIA, L x W) |
|---|---|---|---|---|
| **VDD** | | | | |
| C8 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A(1) | AVX | 1206, 3.2 mm x 1.6 mm |
| | | C0603C102K5RACTU | Kemet | 0603, 1.6 mm x 0.8 mm |
| C9 | 1 µF ± 10%, X7R, 25 V | 12063C105KAT2A(1) | AVX | 1206, 3.2 mm x 1.6 mm |
| | | CGA3E1X7R1E105K080AC | TDK | 0603, 1.6 mm x 0.8 mm |
| **DC/DC CONVERTER** | | | | |
| C4 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C3 | 1 nF ± 10%, X7R, 50 V | C0603C102K5RACTU | Kemet | 0603, 1.6 mm x 0.8 mm |
| C2 | 1 µF ± 10%, X7R, 25 V | CGA3E1X7R1E105K080AC | TDK | 0603, 1.6 mm x 0.8 mm |
| **HLDO** | | | | |
| C1 | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C5 | 100 nF ± 5%, NP0, 50 V | C3216NP01H104J160AA(1) | TDK | 1206, 3.2 mm x 1.6 mm |
| | 100 nF ± 10%, X7R, 50 V | C0603C104K5RACAUTO | Kemet | 0603, 1.6 mm x 0.8 mm |
| C6 | 1 nF ± 10%, X7R, 50 V | 12065C102KAT2A(1) | AVX | 1206, 3.2 mm x 1.6 mm |
| | | C0603C102K5RACTU | Kemet | 0603, 1.6 mm x 0.8 mm |
| **FERRITE BEADS** | | | | |
| FB1, FB2, FB3 | Ferrite bead(2) | 74269244182 | Wurth Elektronik | 0402, 1.0 mm x 0.5 mm |
| | | BLM15HD182SH1 | Murata | 0402, 1.0 mm x 0.5 mm |
| | | BKH1005LM182-T | Taiyo Yuden | 0402, 1.0 mm x 0.5 mm |

(1) Component used for parametric validation.
(2) No ferrite beads used for parametric validation.


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# 10 Layout

## 10.1 Layout Guidelines

図 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC3302 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3302 and keep the layout of both connections symmetrical.

To avoid errors in the measurement caused by the input bias currents of the AMC3302, connect the high-side ground pin (HGND) to the IIN-side of the shunt resistor. Use a separate trace in the layout to make this connection to maintain equal currents in the IIN and INP traces.

## 10.2 Layout Example

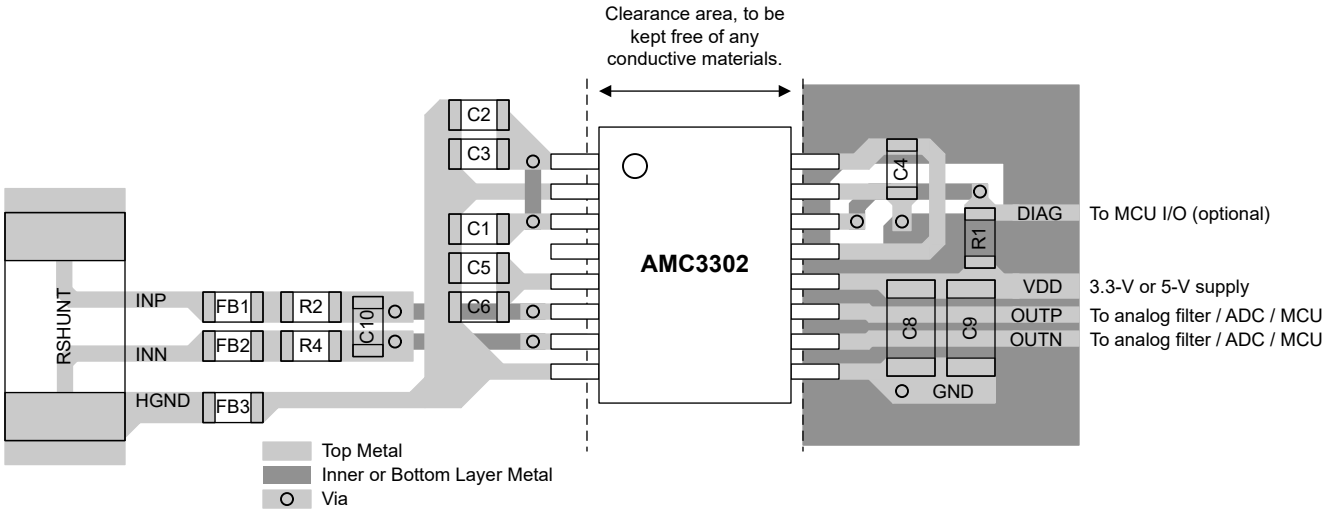


**図 10-1. Recommended Layout of the AMC3302**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *AMC3330 Precision, ±1-V Input, Reinforced Isolated Amplifier* data sheet
- Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool
- Texas Instruments, *Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI* application note

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 サポート・リソース

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## 11.4 Trademarks

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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AMC3302DWE | Active | Production | SOIC (DWE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWE.A | Active | Production | SOIC (DWE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWE.B | Active | Production | SOIC (DWE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWEG4.A | Active | Production | SOIC (DWE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWEG4.B | Active | Production | SOIC (DWE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWER | Active | Production | SOIC (DWE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWER.A | Active | Production | SOIC (DWE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |
| AMC3302DWER.B | Active | Production | SOIC (DWE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC3302 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AMC3302 :**

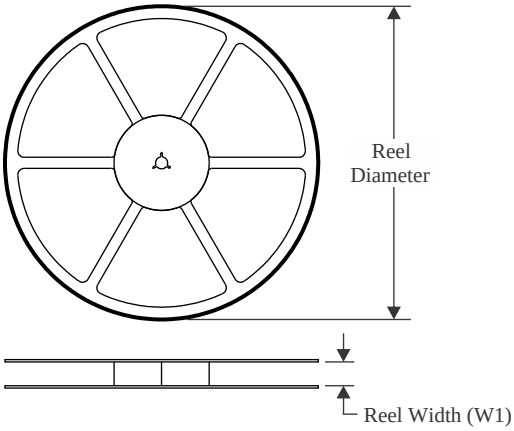
- Automotive : AMC3302-Q1

NOTE: Qualified Version Definitions:

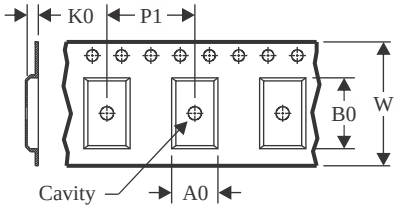
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

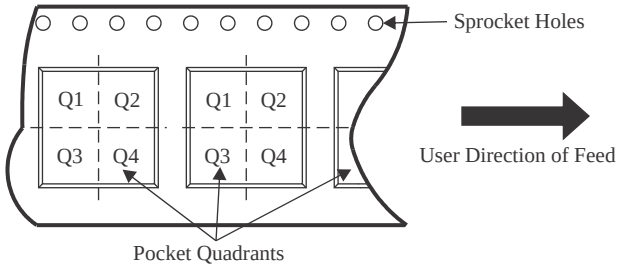



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

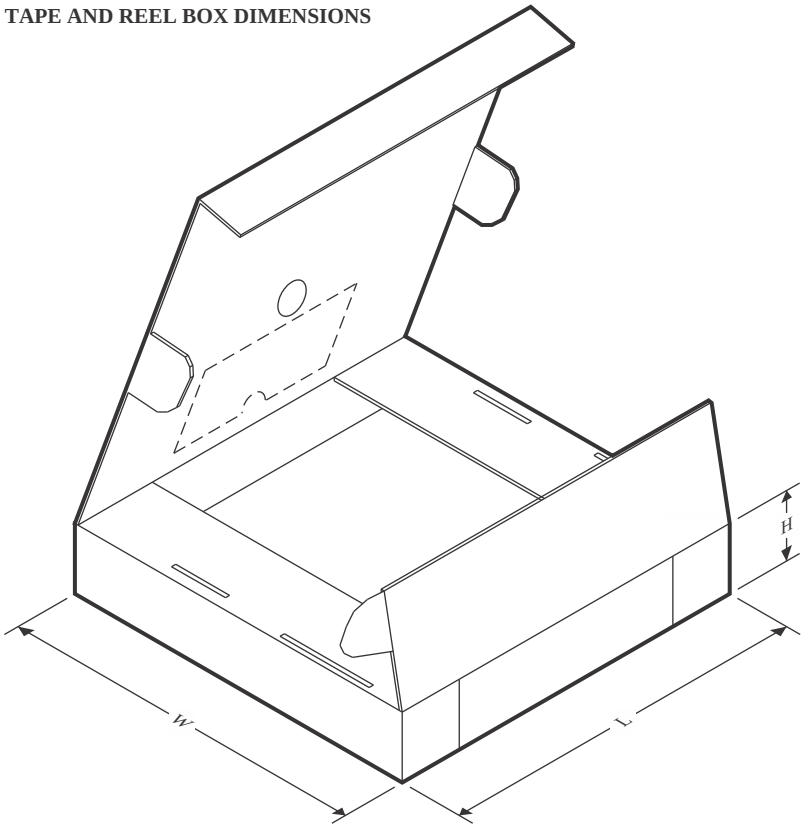
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC3302DWER | SOIC | DWE | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

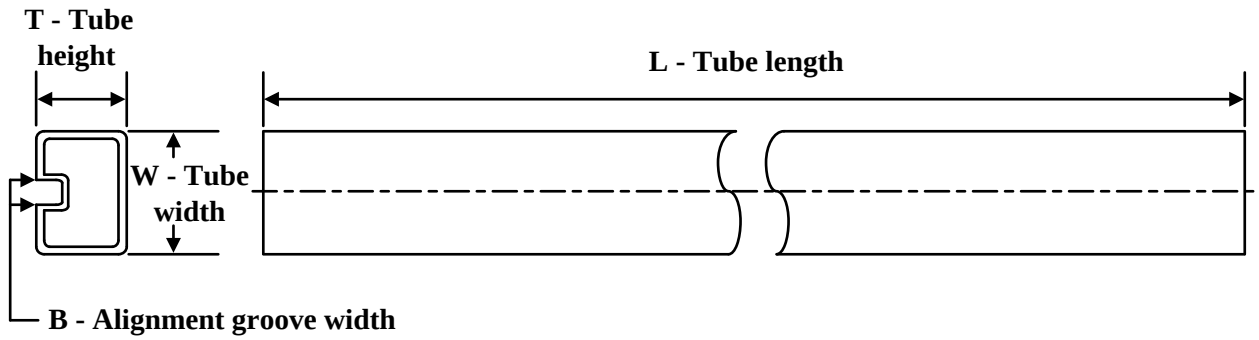
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

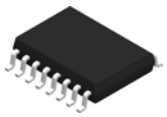
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| AMC3302DWER | SOIC | DWE | 16 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| AMC3302DWE | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| AMC3302DWE.A | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| AMC3302DWE.B | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| AMC3302DWEG4.A | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| AMC3302DWEG4.B | DWE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

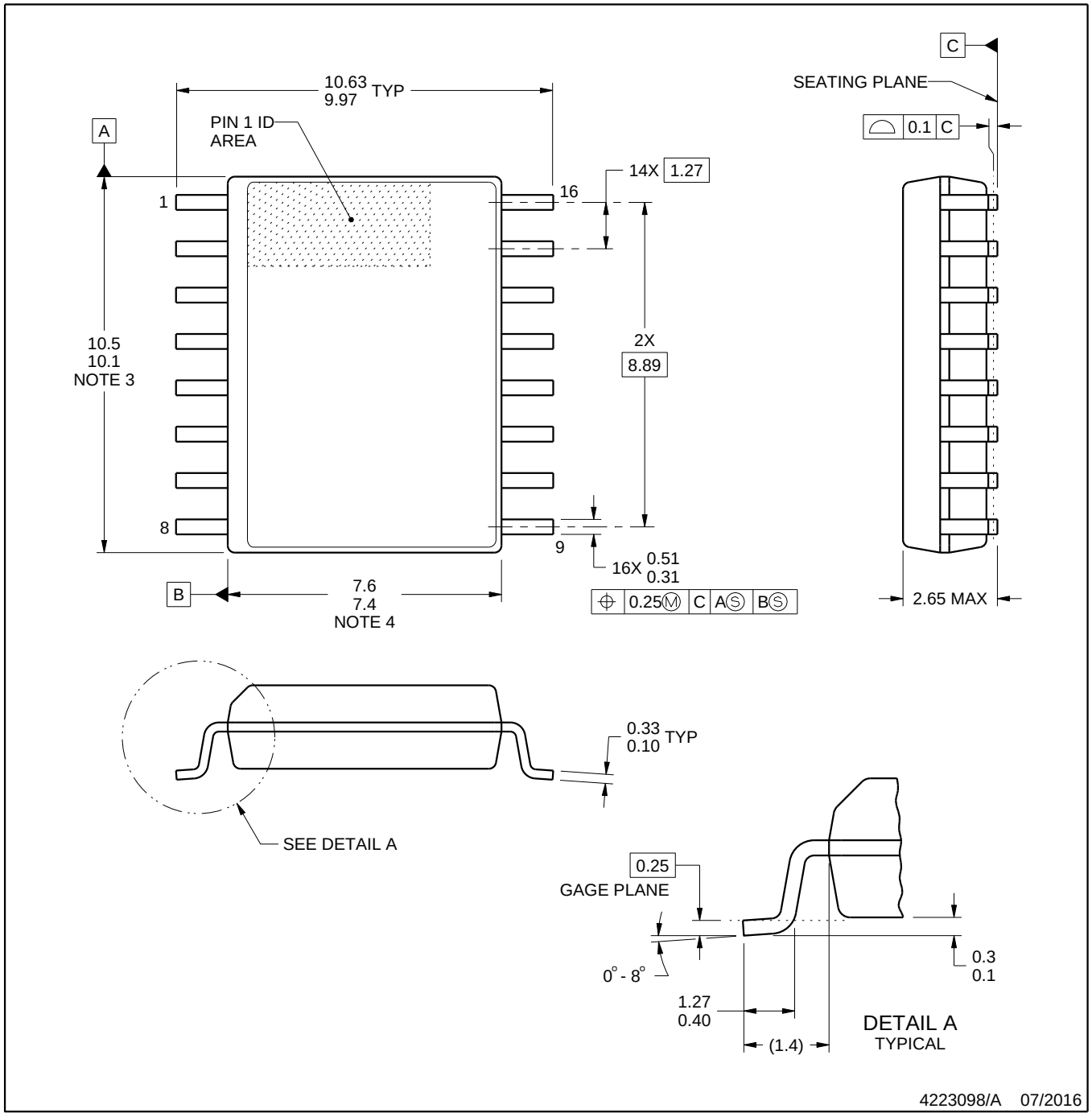


# PACKAGE OUTLINE

## DWE0016A

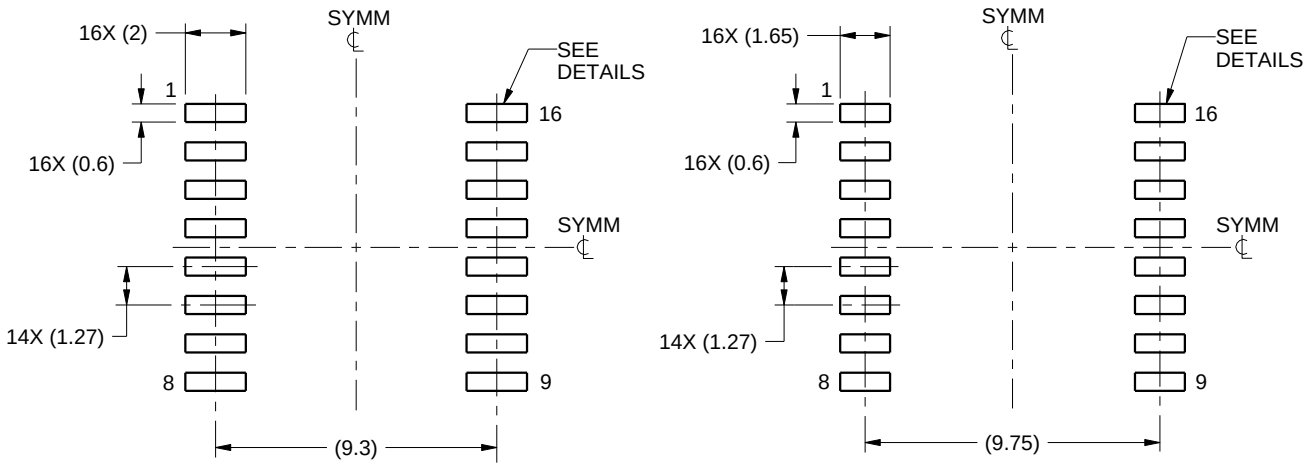
## SOIC - 2.65 mm max height

SOIC




NOTES:

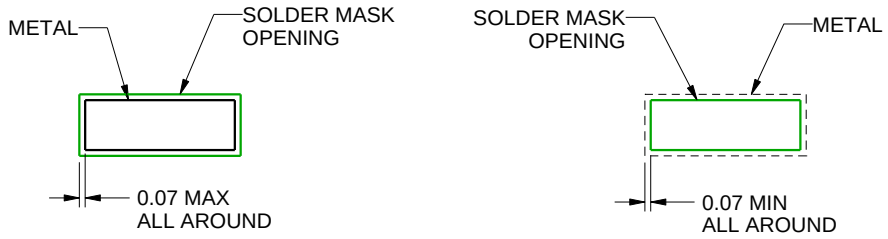
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

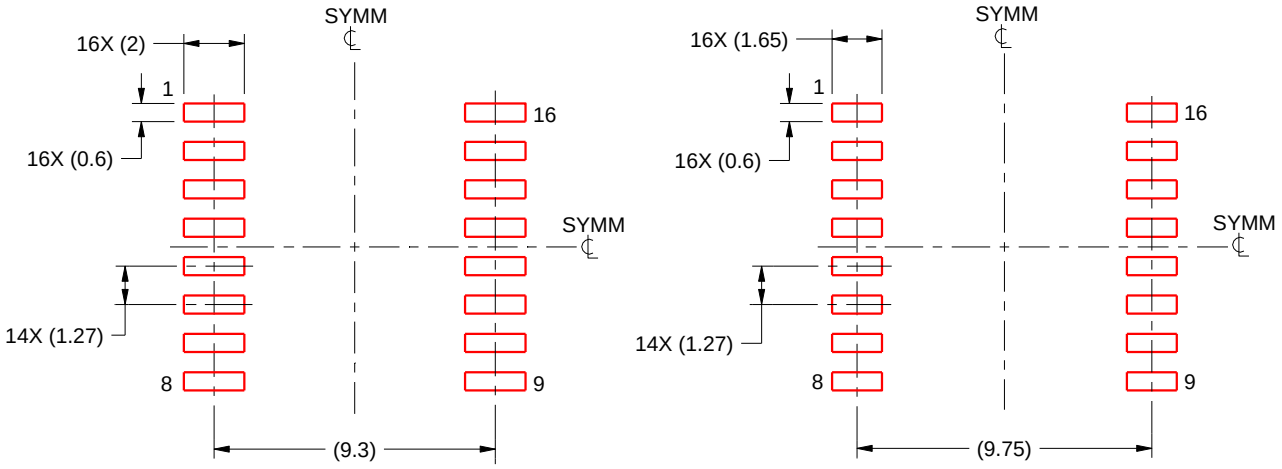
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DWE0016A

## SOIC - 2.65 mm max height

SOIC




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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