BQ25606 スタンドアロン 1 セル 3.0A 降圧バッテリ チャージャ

1 特長

- 高効率 1.5MHz 同期整流スイッチ・モード降圧チャージャ
  - 5V 入力から 2A で 92% の充電効率
  - USB 電圧入力 (5V) 用に最適化
- USB On-The-Go (OTG) をサポート
  - 最大 1.2A を出力可能な昇圧コンバータ
  - 1A 出力で 92% の昇圧効率
  - 正確な定電流 (CC) 制限
  - 最大 500µF の容量性負荷に対するソフトスタート
  - 出力短絡保護
- 1 つの入力で USB 入力および高電圧アダプタに対応
  - 3.9V～13.5V の入力電圧範囲に対応、入力電圧の絶対最大定格 22V
  - 最高 4.6V の入力電圧制限による最大電力トラッキング (VINDPM)
  - バッテリ電圧に自動的に追従する VINDPM スレッショルド
  - USB SDP、DCP および非標準アダプタの自動検出
- 19.5mΩ のバッテリ放電 MOSFET による高いバッテリ放電効率
- ナロー VDC (NVDC) 電力パス管理
  - バッテリ未接続または深放電状態でも即時オン
  - バッテリ補助モードで理想ダイオード動作
- すべての MOSFET、電流センシング、ループ補償を含む高度な統合
- システム電圧スタンバイ状態で 58µA の低いバッテリ・リーク電流
- 高精度
  - ±0.5% の充電電圧レギュレーション
  - 1.2A および 1.8A で ±6% の充電電流レギュレーション
  - 0.5A、1.2A、1.8A で ±5% の入力電流レギュレーション
- 安全関連の認証:
  - IEC 62368-1 CB 認証

2 アプリケーション

- EPOS、携帯用スピーカー
- 携帯電話アクセサリ
- 医療用機器

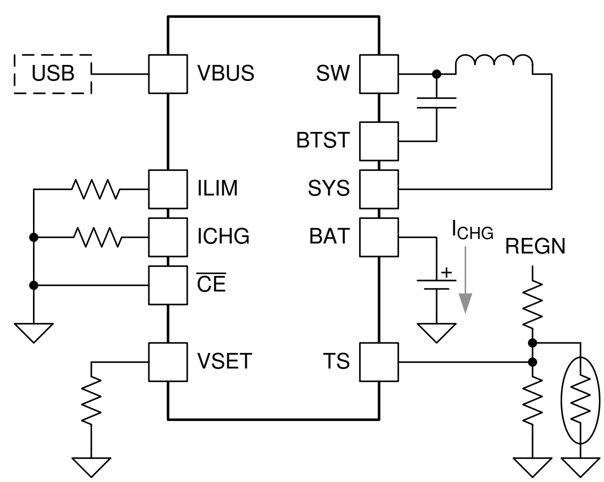
3 概要

BQ25606 は、シングル・セル・リチウムイオンおよびリチウムポリマー・バッテリ向けの、高度に統合されたスタンドアロン 3.0A スイッチ・モード・バッテリ充電管理およびシステム・パワー・パス管理デバイスです。このソリューションは、入力逆電流ブロック FET (RBFET、Q1)、ハイサイド・スイッチング FET (HSFET、Q2)、ローサイド・スイッチング FET (LSFET、Q3)、およびシステムとバッテリの間のバッテリ FET (BATFET、Q4) を高度に統合しています。パワー・パスのインピーダンスが低いため、スイッチ・モードの動作効率が最適化され、バッテリ充電時間の短縮と、放電フェーズにおけるバッテリ駆動時間の延長を実現できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
BQ25606	VQFN (24)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (November 2019) to Revision C (September 2021) — **Page**

- IEC 62368-1 CB 対応を追加 1
- データシート全体にわたって WEBENCH を削除 1
- セクション 5 の 3 番目の段落から「ゼロまで」を削除 4
- Added セクション 6 5
- Added セクション 9.3.4.1 20
- Added セクション 9.3.4.2 20
- Added セクション 9.3.4.3 20
- Added sentence to third paragraph in セクション 9.3.5.4 21
- Changed "fault" to "the timer" in last paragraph of セクション 9.3.5.6 23
- Added セクション 9.3.6 23
- Added セクション 9.3.6.1 23
- Added セクション 9.3.6.2 23
- Added 表 10-1 26
- Changed > to ≤ in last paragraph in セクション 10.2.2.3 27

Changes from Revision A (August 2017) to Revision B (November 2019) — **Page**

- 「アプリケーション」セクションを変更 1

Changes from Revision * (May 2017) to Revision A (August 2017) — **Page**

- データシートのタイトルを変更 1
- セクション 1 から 200ns 高速ターンオフを削除 1
- 「アプリケーション概略回路図」を変更 1
- Changed ACDRV pin references to "NC" in セクション 7 section 6
- Deleted ACDRV pin references from Pin Functions table 6
- Changed VAC pin description in Pin Functions table 6
- Deleted ACDRV pin references from セクション 8.1 table 8
- Added セクション 8.2 table 8
- Deleted VAC debounce time from *Timing Requirements* table 13

- Changed セクション 9.2 17
- Changed Power Up from Input Source section........ 18
- Deleted Power Up OVPFET section........ 18
- Deleted OVPFET Startup Control timing illustration 18
- Added subsection explaining D+/D– detection 18
- Changed Input Overvoltage (ACOV) section........ 24
- Changed BQ25606 Application Diagram schematic........ 26

5 概要 (続き)

BQ25606 は、広範なスタンドアロン充電器および携帯デバイス向けに、高い入力電圧をサポートし、高速充電を行います。入力電圧 / 電流レギュレーションにより、バッテリに最大限の充電電力を供給できます。また、ハイサイド・ゲート・ドライブ用のブートストラップ・ダイオードを内蔵し、システム設計の簡素化を実現しています。

このデバイスは、標準の USB ホスト・ポート、USB 充電ポート、USB 対応高電圧アダプタなど、幅広い入力ソースをサポートしています。また、内蔵された USB インターフェイスによって、デフォルトの入力電流制限を設定しています。入力電流および電圧レギュレーションにより、USB 2.0 および USB 3.0 の電力仕様に準拠しています。内蔵の USB インターフェイスによって入力アダプタが未知であると識別された場合、デバイスの入力電流制限は、ILIM ピンの設定抵抗値により決定されます。また、このデバイスは USB On-the-Go (OTG) の動作電力定格仕様にも適合しており、VBUS 上で最大 1.2 A までの定電流制限付きで 5.15V を供給します。

パワー・パス管理により、システムはバッテリ電圧より少し高く、かつ、最低システム電圧の 3.5V より低下しないようにレギュレートされます。この機能により、システムはバッテリが完全に消耗したとき、または取り除かれたときでも動作を継続できます。入力電流制限または電圧制限に達すると、パワー・パス管理により、充電電流が自動的に低下します。システム負荷が引き続き増大すると、パワー・パスは、システムの電力要件が満たされるまでバッテリを放電します。この補助モードにより入力ソースの過負荷を防止します。

このデバイスはソフトウェア制御なしに、充電サイクルを開始、終了できます。バッテリ電圧を感知し、プレコンディショニング、定電流、定電圧という 3 つのフェーズを移行してバッテリを充電します。充電サイクルの終了時、充電電流があらかじめ設定された制限値を下回り、バッテリ電圧が再充電スレッショルドを上回ると、チャージャは自動的に処理を終了します。十分に充電されたバッテリが再充電スレッショルドを下回ると、チャージャは自動的に次の充電サイクルを開始します。

このチャージャは、バッテリの負温度係数サーミスタ監視、充電安全タイマ、過電圧および過電流保護など、バッテリ充電とシステム運用のための多様な安全機能を備えています。サーマル・レギュレーションにより、接合部温度が 110℃を超えると充電電流が低減されます。STAT 出力により、充電状態とフォルト状態がレポートされます。その他の安全機能として、充電および昇圧モードでのバッテリ温度センシング、サーマル・レギュレーションおよびサーマル・シャットダウン、入力 UVLO および過電圧保護があります。

このデバイスは、24 ピン、4mm × 4mm の QFN パッケージで供給されます。

6 Device Comparison Table

	BQ25606	BQ25616	BQ25616J
Quiescent battery current (BAT,SYS,SW)	58 µA	9.5 µA	9.5 µA
VBUS OVP reaction-time	200 ns	130 ns	130 ns
Input voltage regulation accuracy	±3%	±2%	±2%
TS profile	JEITA	Hot/Cold	JEITA
Charge safety timer accuracy	10 hr	20 hr	20 hr
Charge voltage limit	4.2 V/4.35 V/4.4 V	4.1 V/4.2 V/4.35 V	4.1 V/4.2 V/4.35 V
Battery voltage regulation	±0.5%	±0.4%	±0.4%
ACDRV	No	Yes	Yes

7 Pin Configuration and Functions

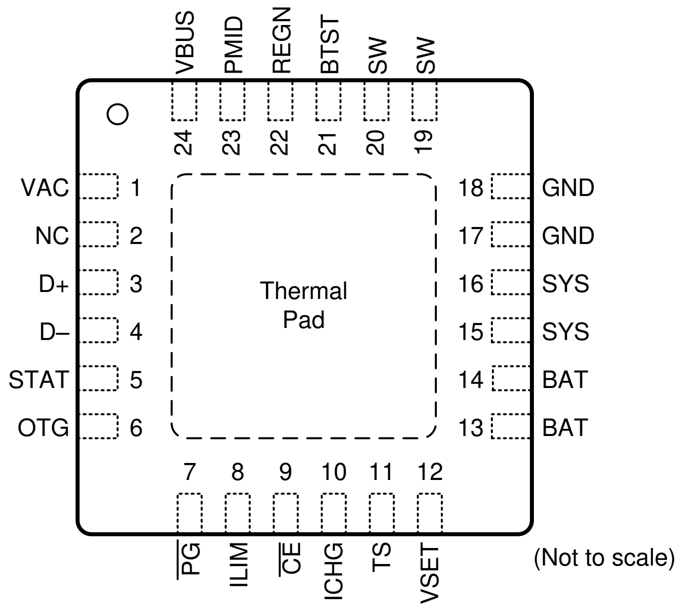


図 7-1. BQ25606 RGE Package 24-Pin VQFN Top View

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	2		No connection. This pin must be floating.
BAT	13 14	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10-µF capacitor closely to the BAT pin.
BTST	21	P	PWM high side driver positive supply. internally, the BTST is connected to the cathode of the boost-strap diode. Connect a 0.047-µF bootstrap capacitor from SW to BTST.
$\overline{\text{CE}}$	9	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
D+	3	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
D–	4	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
GND	17 18	P	Power ground and signal ground.
ICHG	10	AI	I_{CHG} pin sets the charge current limit. A resistor is connected from I_{CHG} pin to ground to set charge current limit as $I_{CHG} = K_{ICHG}/R_{ICHG}$. The acceptable range for charge current is 300 mA to 3000 mA.
ILIM	8	AI	ILIM sets the input current limit. A resistor is connected from ILIM pin to ground to set the input current limit as IINDPM = K_{ILIM}/R_{ILIM}. The acceptable range for ILIM current is 500 mA to 3200 mA. The resistor based input current limit is effective only when the input adapter is detected as unknown. Otherwise, the input current limit is determined by D+/D– detection outcome.
OTG	6	DI	Boost mode enable pin. When this pin is pulled HIGH, OTG is enabled. OTG cannot be floating.
$\overline{\text{PG}}$	7	DO	Open drain active low power good indicator. Connect to the pull up rail through a 10-kΩ resistor. LOW indicates a good input if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and input current limit is above 30 mA.
PMID	23	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 10-µF ceramic capacitor between PMID and GND.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC.

表 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
STAT	5	DO	Open-drain interrupt output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): Blink at 1 Hz.
SW	19 20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect a 0.047-μF bootstrap capacitor from SW to BTST.
SYS	15 16	P	Converter output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect a 20-μF capacitor close to the SYS pin.
TS	11	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend 103AT-2 thermistor.
VAC	1	AI	Input voltage sensing. This pin must be shorted to the VBUS pin.
VBUS	24	P	Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor from VBUS to GND and place it as close as possible to the IC.
VSET	12	AI	VSET pin sets default battery charge voltage in the BQ25606. Program battery regulation voltage with a resistor pull-down from VSET to GND. R_{PD} > 50 kΩ (float pin) = 4.208 V R_{PD} < 500 Ω (short to GND) = 4.352 V 5 kΩ < R_{PD} < 25 kΩ = 4.400 V
Thermal Pad		P	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VAC	–2	22	V
Voltage Range (with respect to GND)	VBUS (converter not switching)[(2)]	–2	22	V
Voltage Range (with respect to GND)	BTST, PMID (converter not switching)[(2)]	–0.3	22	V
Voltage Range (with respect to GND)	SW	–2	16	V
Voltage Range (with respect to GND)	BTST to SW	–0.3	7	V
Voltage Range (with respect to GND)	D+, D–	–0.3	7	V
Voltage Range (with respect to GND)	REGN, TS, $\overline{CE}$, $\overline{PG}$, BAT, SYS (converter not switching)	–0.3	7	V
Output Sink Current	STAT		6	mA
Voltage Range (with respect to GND)	VSET, ILIM, ICHG, OTG	–0.3	7	V
Voltage Range (with respect to GND)	PGND to GND (QFN package only)	–0.3	0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) VBUS is specified up to 22 V for a maximum of one hour at room temperature

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{BUS}	Input voltage	3.9		13.5 [(1)]	V
I_{in}	Input current (VBUS)			3.25	A
I_{SYSOP}	Output current (SW)			3.0	A
V_{BATOP}	Battery voltage			4.4	V
I_{BATOP}	Fast charging current			3.0	A
I_{BATOP}	Discharging current (continuous)			6	A

8.3 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

8.4 Thermal Information

THERMAL METRIC [(1)]		BQ25606 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

8.5 Electrical Characteristics

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.5 V, $V_{BUS} < V_{AC-UVLOZ}$, leakage between BAT and VBUS, T_J< 85°C			5	µA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4.5 V, No VBUS, T_J < 85°C		58	85	µA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, $V_{VBUS} > V_{VBAT}$, converter not switching		1.5	3	mA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} > VUVLO, $V_{VBUS} > V_{VBAT}$, converter switching, VBAT = 3.8V, ISYS = 0A		3		mA
I_{BOOST}	Battery discharge current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} = 0 A, converter switching		3		mA
VBUS, VAC AND BAT PIN POWER UP						
V_{BUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13.5	V
$V_{VAC\_PRESENT}$	REGN turn-on threshold	V_{VAC} rising	3.36	3.65	3.97	V
$V_{VAC\_PRESENT\_HYS}$		V_{VAC} falling		300		mV
V_{SLEEP}	Sleep mode falling threshold	(V_{VAC}–V_{VBAT}), $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC falling	37	76	126	mV
V_{SLEEPZ}	Sleep mode rising threshold	(V_{VAC}–V_{VBAT}), $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC rising	130	220	350	mV
$V_{VAC\_OV\_RISE}$	VAC Overvoltage rising threshold	VAC rising	13.5	14.28	14.91	V
$V_{VAC\_OV\_HYS}$	VAC Overvoltage hysteresis	VAC falling		520		mV
$V_{BAT\_DPL\_FALL}$	Battery depletion falling threshold (Q4 turn-off threshold)	V_{BAT} falling	2.15		2.6	V
$V_{BAT\_DPL\_RISE}$	Battery Depletion rising threshold (Q4 turn-on threshold)	V_{BAT} rising	2.35		2.82	V
$V_{BAT\_DPL\_HYST}$	Battery Depletion rising hysteresis	V_{BAT} rising		180		mV

8.5 Electrical Characteristics (continued)

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	V_{BUS} falling	3.65	3.8	3.93	V
V_{BUSMIN_HYST}	Bad adapter detection hysteresis			200		mV
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		30		mA
POWER PATH						
V_{SYS_MIN}	System regulation voltage	$V_{VBAT} < V_{SYS\_MIN = 3.5V}$, charge enabled or disabled	3.5	3.68		V
V_{SYS}	System regulation voltage	I_{SYS} = 0 A, $V_{VBAT} > V_{SYSMIN}$, charge disabled		V_{BAT} + 50 mV		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ T_A ≤ 125°C		45		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW - Q2	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		62		mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		70		mΩ
V_{FWD}	BATFET forward voltage in supplement mode			30		mV
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C		19.5	24	mΩ
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = –40 - 125°C		19.5	30	mΩ
BATTERY CHARGER						
V_{BATREG}	Charge voltage	R_{VSET} > 50 kΩ, –40 ≤ T_J ≤ 85°C	4.187	4.208	4.229	V
		R_{VSET} < 500 Ω, –40 ≤ T_J ≤ 85°C	4.330	4.352	4.374	V
		R_{VSET} = 10 kΩ, –40 ≤ T_J ≤ 85°C	4.378	4.4	4.422	V
V_{BATREG_ACC}	Charge voltage setting accuracy	V_{BAT} = 4.208 V or V_{BAT} = 4.352 V, –40 ≤ T_J ≤ 85°C	–0.5%		0.5%	
$I_{CHG\_REG\_RANGE}$	Charge current regulation range		0		3000	mA
I_{CHG_REG}	Charge current regulation	R_{ICHG} = 1100 Ω, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	516	615	715	mA
$I_{CHG\_REG\_ACC}$	Charge current regulation accuracy	R_{ICHG} = 1100 Ω, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	-16%		16%	
I_{CHG_REG}	Charge current regulation	R_{ICHG} = 562 Ω, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	1.14	1.218	1.28	A
I_{CHG_REG}	Charge current regulation accuracy	R_{ICHG} = 562 Ω, V_{BAT} = 3.1 V or V_{BAT} = 3.8 V	-6%		6%	
I_{CHG_REG}	Charge current regulation	R_{ICHG} = 372 Ω, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	1.715	1.813	1.89	A
$I_{CHG\_REG\_ACC}$	Charge current regulation accuracy	R_{ICHG} = 372 Ω, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	-5%		5%	
K_{ICHG}	Charge current regulation setting ratio	R_{ICHG} = 372 Ω, 562 Ω V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	639	677	715	A×Ω
K_{ICHG_ACC}	Charge current regulation setting ratio accuracy	R_{ICHG} = 372Ω, 562 Ω V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	-6%		6%	
$V_{BATLOWV\_FALL}$	Battery LOWV falling threshold	Fast charge to precharge	2.67	2.8	2.87	V
$V_{BATLOWV\_RISE}$	Battery LOWV rising threshold	Pre-charge to fast charge	3.0	3.1	3.24	V
I_{PRECHG}	Precharge current regulation	R_{ICHG} = 1100 Ω, V_{VBAT} = 2.6 V, I_{PRECHG} = 5% of I_{CHG} = 615mA	21		38	mA

8.5 Electrical Characteristics (continued)

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PRECHG_ACC}	Precharge current regulation accuracy	Percentage of I_{CHG},R_{ICHG} = 1100 Ω, V_{VBAT} = 2.6 V, I_{CHG} = 615mA	3.4%		6.2%	
I_{PRECHG}	Precharge current regulation	R_{ICHG} = 562 Ω, V_{VBAT} = 2.6 V, I_{PRECHG} = 5% of I_{CHG} = 1.218A	48		67	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy	Percentage of I_{CHG},R_{ICHG} = 562 Ω, V1330 = 2.6 V, I_{CHG} = 1.218A	3.9%		5.5%	
I_{PRECHG}	Precharge current regulation	R_{ICHG} = 372 Ω, V_{VBAT} = 2.6 V, I_{PRECHG} = 5% of I_{CHG} = 1.813A	76		97	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy	Percentage of I_{CHG},R_{ICHG} = 372 Ω, V_{VBAT} = 2.6 V, I_{CHG} = 1.813A	4.1%		5.4%	
I_{TERM}	Termination current regulation	R_{ICHG} = 562 Ω, V_{VBAT} = 4.35V,$_{CHG}$ = 1.218A	26		100	mA
I_{TERM_ACC}	Termination current regulation accuracy	Percentage of I_{CHG}, R_{ICHG} = 562 Ω, V_{VBAT} = 4.35 V, I_{CHG} = 1.218 A	2.1%		8.3%	
I_{TERM}	Termination current regulation	R_{ICHG} = 372 Ω, V_{VBAT} = 4.35 V, I_{CHG} = 1.813 A	56	100	126	mA
I_{TERM_ACC}	Termination current regulation accuracy	Percentage of I_{CHG}, R_{ICHG} = 372 Ω, V_{VBAT} = 4.35 V, I_{CHG} = 1.813 A	3.0%		7.0%	
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.85	2	2.15	V
V_{SHORTZ}	Battery short voltage	V_{VBAT} rising	2.05	2.25	2.35	V
I_{SHORT}	Battery short current	$V_{VBAT} < V_{SHORTZ}$	70	90	110	mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling	87	121	156	mV
$I_{SYSLOAD}$	System discharge load current	V_{SYS} = 4.2 V		30		mA
INPUT VOLTAGE AND CURRENT REGULATION						
V_{DPM_VBAT}	Input voltage regulation limit	V_{VBAT} < 4.1 V (V_{VBAT}= 3.6 V)	4.171	4.3	4.429	V
$V_{DPM\_VBAT\_ACC}$	Input voltage regulation accuracy	V_{VBAT} < 4.1 V (V_{VBAT} = 3.6 V)	–3%		3%	
I_{INDPM}	USB input current regulation limit	V_{VBUS} = 5 V, USB500 charge port detected by DPDM , –40 ≤ T_J ≤ 85°C	448		500	mA
I_{INDPM}	Input current regulation limit	R_{ILIM} = 910 Ω, unknown adaptor detected by DPDM , –40 ≤ T_J ≤ 85°C	505	526	550	mA
I_{INDPM}	Input current regulation limit accuracy	R_{ILIM} = 374 Ω, unknown adaptor detected by DPDM , –40 ≤ T_J ≤ 85°C	1220	1276	1330	mA
I_{INDPM}	Input current regulation limit	R_{ILIM} = 265 Ω, unknown adaptor detected by DPDM , –40 ≤ T_J ≤ 85°C	1.73	1.8	1.871	A
I_{INDPM_ACC}	Input current regulation limit accuracy	R_{ILIM} = 265 Ω, 374 Ω, 910 Ω, unknown adaptor detected by DPDM , –40 ≤ T_J ≤ 85°C	–5%		5%	
K_{ILIM}	Input current setting ratio, $I_{LIM} = K_{ILIM} / R_{ILIM}$	R_{ILIM} = 910 Ω, 374 Ω, 265 Ω, unknown adaptor detected by DPDM, –40 ≤ T_J ≤ 85°C	459	478	500	A×Ω
K_{ILIM_ACC}	Input current setting ratio, $I_{LIM} = K_{ILIM} / R_{ILIM}$	R_{ILIM} = 910 Ω, 374 Ω, 265 Ω, unknown adaptor detected by DPDM, –40 ≤ T_J ≤ 85°C	–5%		5%	
I_{IN_START}	Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION						

8.5 Electrical Characteristics (continued)

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATOVP_RISE}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}	103%	104%	105%	
V_{BATOVP_FALL}	Battery overvoltage threshold	V_{BAT} falling, as percentage of V_{BAT_REG}	101%	102%	103%	
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold			110		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis			30		°C
JEITA THERMISTOR COMPARATOR (BUCK MODE)						
V_{T1}	T1 (0°C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{REGN}	72.4%	73.3%	74.2%	
V_{T1}	Falling	As Percentage to V_{REGN}	69%	71.5%	74%	
V_{T2}	T2 (10°C) threshold, Charge back to I_{CHG}/2 and 4.2 V below this temperature	As percentage of V_{REGN}	67.2%	68%	69%	
V_{T2}	Falling	As Percentage to V_{REGN}	66%	66.8%	67.7%	
V_{T3}	T3 (45°C) threshold, charge back to ICHG and 4.05V above this temperature.	Charger suspends charge. As Percentage to V_{REGN}	43.8%	44.7%	45.8%	
V_{T3}	Falling	As Percentage to V_{REGN}	45.1%	45.7%	46.2%	
V_{T5}	T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to V_{REGN}	33.7%	34.2%	35.1%	
V_{T5}	Falling	As Percentage to V_{REGN}	34.5%	35.3%	36.2%	
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)						
V_{BCOLD}	Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to V_{REGN} (Approx. –20°C w/ 103AT), –20°C ≤ T_J ≤ 125°C	79.5%	80%	80.5%	
V_{BCOLD}	Falling	–20°C ≤ T_J ≤ 125°C	78.5%	79%	79.5%	
V_{BHOT}	Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to V_{REGN} (Approx. 60°C w/ 103AT), –20°C ≤ T_J ≤ 125°C	30.2%	31.2%	32.2%	
V_{BHOT}	Rising	–20°C ≤ T_J ≤ 125°C	33.8%	34.4%	34.9%	
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{HSFET_OCP}	HSFET cycle-by-cycle over-current threshold		5.2		8.0	A
I_{BATFET_OCP}	System over load threshold		6.0			A
PWM						
f_{SW}	PWM switching frequency	Oscillator frequency, buck mode	1320	1500	1680	kHz
		Oscillator frequency, boost mode	1170	1412	1500	kHz
D_{MAX}	Maximum PWM duty cycle[(1)]			97%		
BOOST MODE OPERATION						
V_{OTG_REG}	Boost mode regulation voltage	V_{VBAT} = 3.8 V, $I_{(PMID)}$ = 0 A	4.972	5.126	5.280	V
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	V_{VBAT} = 3.8 V, $I_{(PMID)}$ = 0 A	-3		3	%
$V_{BATLOWV\_OTG}$	Battery voltage exiting boost mode	V_{VBAT} falling	2.6	2.8	2.9	V
	Battery voltage entering boost mode	V_{VBAT} rising	2.9	3.0	3.15	V
I_{OTG}	OTG mode output current limit		1.2	1.4	1.6	A
V_{OTG_OVP}	OTG overvoltage threshold	Rising threshold	5.55	5.8	6.15	V
REGN LDO						

8.5 Electrical Characteristics (continued)

$V_{VAC\_PRESENT}$ < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

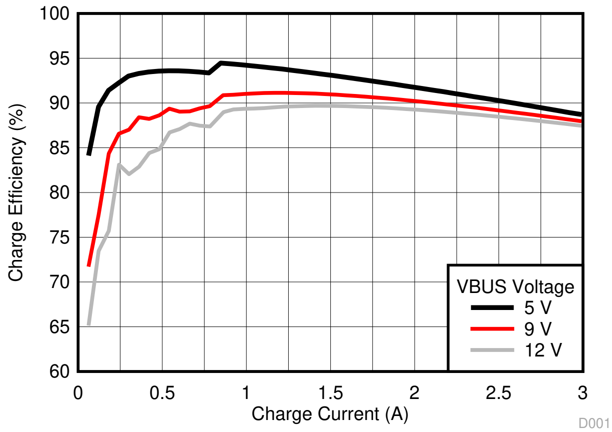
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9 V, I_{REGN} = 40 mA	5.6	6	6.65	V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.6	4.7	4.9	V
LOGIC I/O PIN CHARACTERISTICS ($\overline{CE}$, PSEL, SCL, SDA, $\overline{INT}$)						
V_{ILO}	Input low threshold $\overline{CE}$				0.4	V
V_{IH}	Input high threshold $\overline{CE}$		1.3			V
I_{BIAS}	High-level leakage current $\overline{CE}$	Pull up rail 1.8 V			1	µA
V_{ILO}	Input low threshold OTG				0.4	V
V_{IH}	Input high threshold OTG		1.3			V
I_{BIAS}	High-level leakage current OTG	Pull up rail 1.8 V			1	µA
LOGIC I/O PIN CHARACTERISTICS ($\overline{PG}$, STAT)						
V_{OL}	Low-level output voltage				0.4	V
D+/D– DETECTION						
V_{D+_1P2}	D+ Threshold for Non-standard adapter (combined V1P2_VTH_LO and V1P2_VTH_HI)		1.05		1.35	V
I_{D+_LKG}	Leakage current into D+	HiZ	-1		1	µA
$V_{D–\_600MVSRC}$	Voltage source (600 mV)		500	600	700	mV
$I_{D–\_100UAISNK}$	D– current sink (100 µA)	$V_{D–}$ = 500 mV,	50	100	150	µA
$R_{D–\_19K}$	D– resistor to ground (19 kΩ)	$V_{D–}$ = 500 mV,	14.25		24.8	kΩ
$V_{D–\_0P325}$	D– comparator threshold for primary detection	D– pin Rising	250		400	mV
$V_{D–\_2P8}$	D– Threshold for non-standard adapter (combined V2P8_VTH_LO and V2P8_VTH_HI)		2.55		2.85	V
$V_{D–\_2P0}$	D– Comparator threshold for non-standard adapter (For non-standard – same as BQ2589x)		1.85		2.15	V
$V_{D–\_1P2}$	D– Threshold for non-standard adapter (combined V1P2_VTH_LO and V1P2_VTH_HI)		1.05		1.35	V
$I_{D–\_LKG}$	Leakage current into D–	HiZ	-1		1	µA

(1) Specified by design. Not production tested.

8.6 Timing Requirements

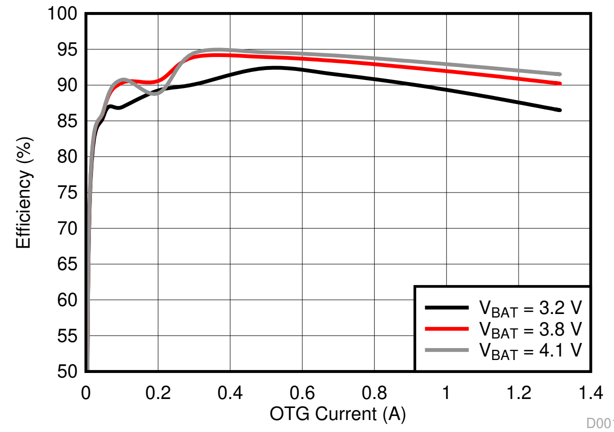
PARAMETER			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{ACOV}	VBUS OVP reaction time	VAC rising above ACOV threshold to turn off Q2		200		ns
t_{BADSRC}	Bad adapter detection duration			30		ms
t_{TERM_DGL}	Deglitch time for charge termination			250		ms
t_{RECHG_DGL}	Deglitch time for recharge			250		ms
$t_{SYSOVLD\_DGL}$	System over-current deglitch time to turn off Q4			100		µs
t_{BATOVP}	Battery overvoltage deglitch time to disable charge			1		µs
t_{SAFETY}	Typical Charge Safety Timer Range		8	10	12	hr

8.7 Typical Characteristics



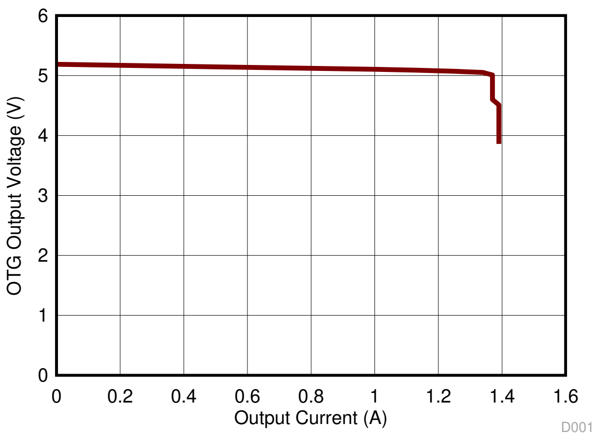
f_{SW} = 1.5 MHz   Inductor DCR = 18 mΩ
V_{BAT} = 3.8 V

図 8-1. Charge Efficiency vs. Charge Current



V_{OTG} = 5.15 V   inductor DCR = 18 mΩ

図 8-2. Efficiency vs. OTG Current



0 A ≤ I_{OTG} ≤1.37 A V_{OTG} = 5.15 V
V_{VBAT} = 3.8 V

図 8-3. OTG Output Voltage vs. Output Current

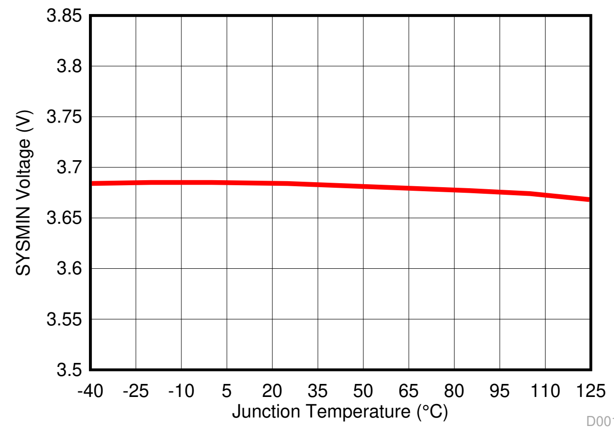


図 8-4. SYSMIN Voltage vs. Junction Temperature

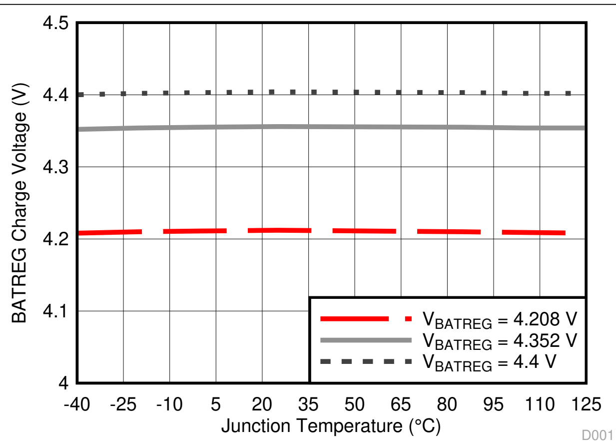
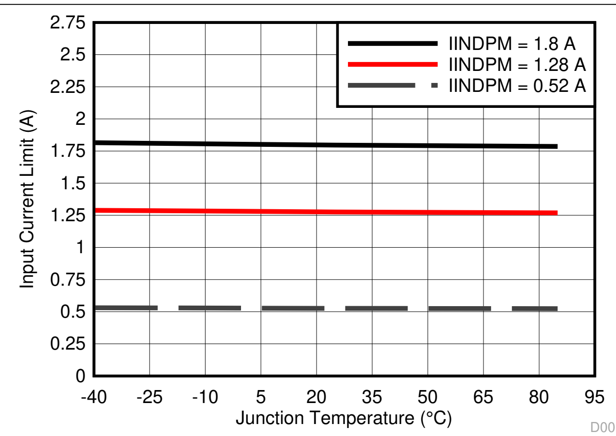


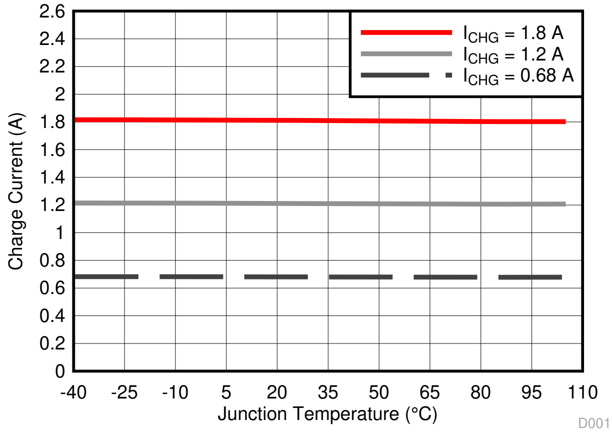
図 8-5. BATREG Charge Voltage vs. Junction Temperature



V_{VBUS} = 5 V

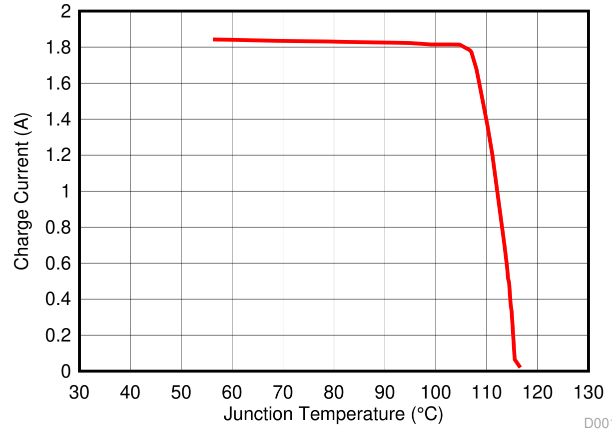
図 8-6. Input Current Limit vs. Junction Temperature

8.7 Typical Characteristics (continued)



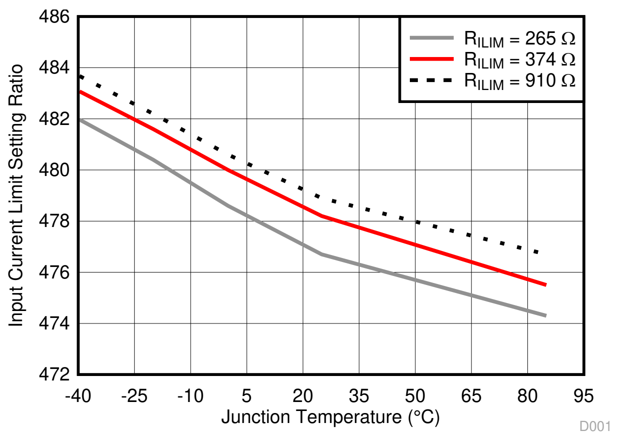
V_{VBUS} = 5 V V_{BAT} = 3.8 V

図 8-7. Charge Current vs. Junction Temperature



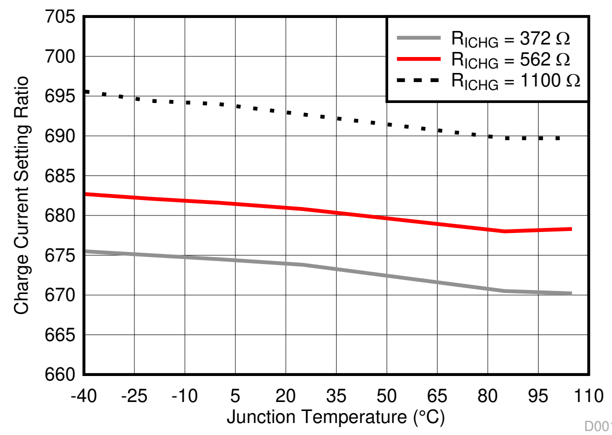
V_{VBUS} = 5V V_{BAT} = 3.8V

図 8-8. Charge Current vs. Junction Temperature Under Thermal Regulation



V_{VBUS} = 5 V V_{BAT} = 3.8 V

図 8-9. Input Current Limit Setting Ratio vs. Junction Temperature



V_{VBUS} = 5 V V_{BAT} = 3.8 V

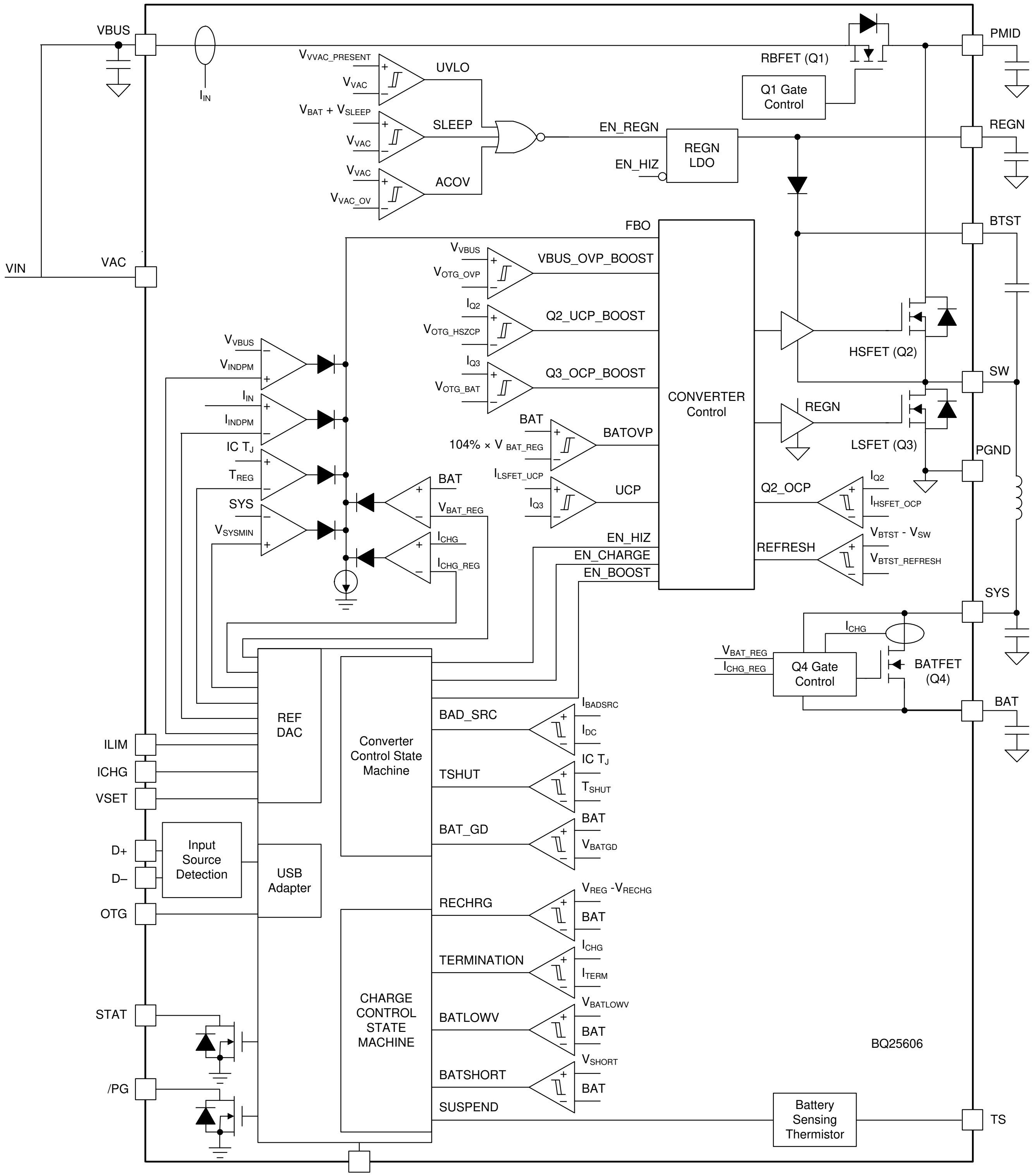
図 8-10. Charge Current Setting Ratio vs. Junction Temperature

9 Detailed Description

9.1 Overview

The BQ25606 is a highly integrated 3.0-A switch-mode battery charger for single cell Li-ion and Li-polymer batteries. It includes an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (Supplement Mode). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately until the input source plugs in again.

9.3.2 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power-up sequence from input source is as listed:

1. Power up REGN LDO
2. Poor source qualification
3. Input source type detection is based on D+/D– to set input current limit (IINDPM) .
4. Input voltage limit threshold setting (VINDPM threshold)
5. Converter power up

9.3.2.1 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- V_{VAC} above $V_{VAC\_PRESENT}$
- V_{VAC} above $V_{BAT} + V_{SLEEPZ}$ in buck mode or VBUS below $V_{BAT} + V_{SLEEP}$ in boost mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than IVBUS_HIZ from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

9.3.2.2 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VAC voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

9.3.2.3 Input Source Type Detection

After the REGN LDO is powered, the device runs input source detection through D+/D– lines. The BQ25606 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/ DCP) and nonstandard adapter through USB D+/D– lines. The BQ25606 sets input current limit through D+/D- detection and ILIM pins.

9.3.2.3.1 D+/D– Detection Sets Input Current Limit in BQ25606

The BQ25606 contains a D+/D– based input source detection to set the input current limit at VBUS plug-in. The D+/D– detection includes standard USB BC1.2 and nonstandard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the nonstandard adapter detection is applied to set the input current limit. The nonstandard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is set at 2.4 A. If an adapter is detected as unknown, the input current limit is set at 500 mA by ILIM pin.

表 9-1. Nonstandard Adapter Detection

NONSTANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within V_{D+_2p8}	V_{D-} within V_{D-_2p0}	2.1
Divider 2	V_{D+} within V_{D+_1p2}	V_{D-} within V_{D-_1p2}	2
Divider 3	V_{D+} within V_{D+_2p0}	V_{D-} within V_{D-_2p8}	1
Divider 4	V_{D+} within V_{D+_2p8}	V_{D-} within V_{D-_2p8}	2.4

表 9-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)
USB SDP (USB500)	500 mA
USB DCP	2.4 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Divider 2	2 A
Unknown 5-V adapter	Set by ILIM pin

9.3.2.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device VINDPM is set at 4.3 V. The device supports dynamic VINDPM tracking which tracks the battery voltage. The device VINDPM tracks battery voltage with 200 mV offset such that when VBAT + 200 mV is greater than 4.3 V, the VINDPM value is automatically adjusted to VBAT + 200 mV.

9.3.2.5 Converter Power Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to 200 mA . After the system rises above 2.2 V, the device limits input current to the value set by ILIM pin.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled.

9.3.3 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. BAT above V_{OTG_BAT}
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH)
4. Voltage at TS (thermistor) pin as a percentage of V_{REGN} is within acceptable range ($V_{BHOT} < V_{TS} < V_{BCOLD}$)
5. After 30-ms delay from boost mode enable

During boost mode, the VBUS output is 5.15 V and the output current can reach up to 1.2 A. The boost output is maintained when BAT is above V_{OTG_BAT} threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot.

9.3.4 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

9.3.4.1 Narrow VDC Architecture

When the battery is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of the BATFET.

When battery charging is disabled and above the minimum system voltage setting or charging is terminated, the system is always regulated at typically 50 mV above the battery voltage.

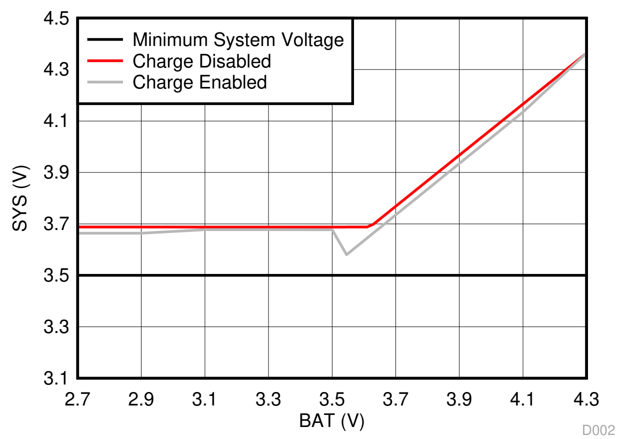


図 9-1. System Voltage vs Battery Voltage

9.3.4.2 Dynamic Power Management

To meet maximum current limit in the USB specification and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit or the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

9.3.4.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. shows the V-I curve of the BATFET gate regulation operation. The BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

9.3.5 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

9.3.5.1 Autonomous Charging Cycle

With battery charging enabled ($\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle. The device default charging parameters are listed in 表 9-3.

表 9-3. Charging Parameter Default Setting

DEFAULT MODE	BQ25606
Charging voltage	VSET controlled
Charging current	I_{CHG} controlled
Precharge current	5% of ICHG
Termination current	5% of ICHG
Temperature profile	JEITA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled ($\overline{CE}$ is low)
- No thermistor fault on TS
- No safety timer fault

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold, the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (blinking).

9.3.5.2 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

9.3.5.3 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

9.3.5.4 JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), the charge current is reduced to 20% of programmed fast charge current. At warm temperature (T3-T5), the charge voltage is reduced to 4.1 V. Charge termination is disabled for cool and warm conditions.

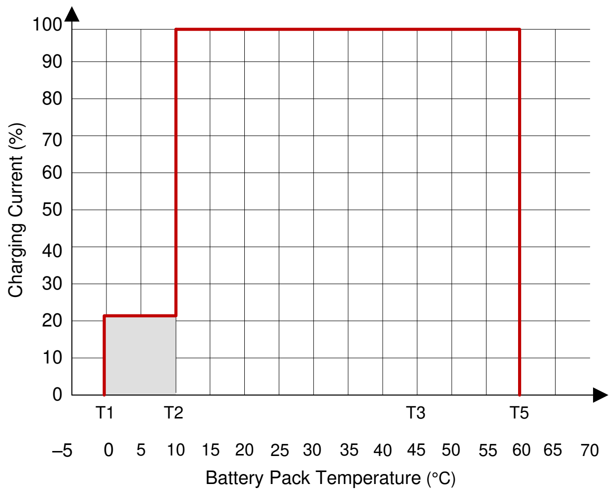


図 9-2. JEITA Profile: Charging Current

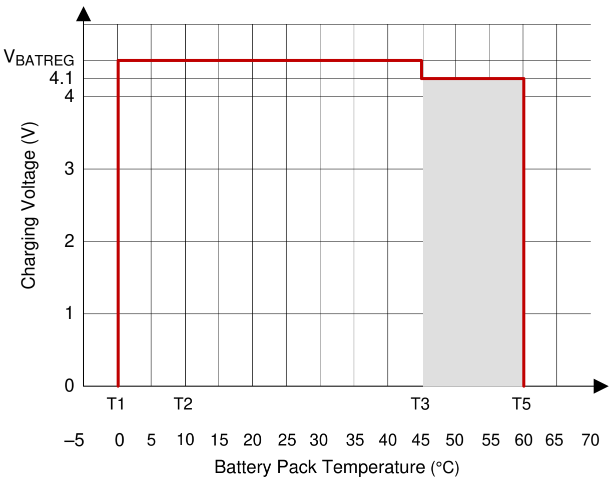


図 9-3. JEITA Profile: Charging Voltage

式 1 through 式 2 describe updates to the resistor bias network.

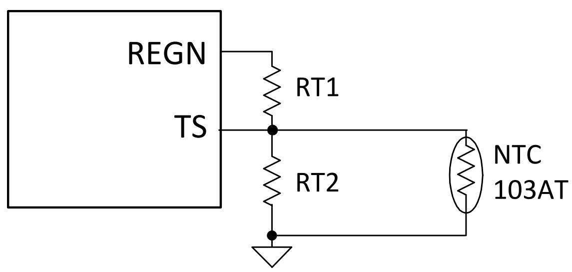


図 9-4. TS Pin Resistor Network

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- RTH_{COLD} = 27.28 kΩ
- RTH_{HOT} = 3.02 kΩ
- RT1 = 5.23 kΩ
- RT2 = 30.9 kΩ

9.3.5.5 Boost Mode Thermistor Monitor during Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLD} to V_{BHOT} thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended.

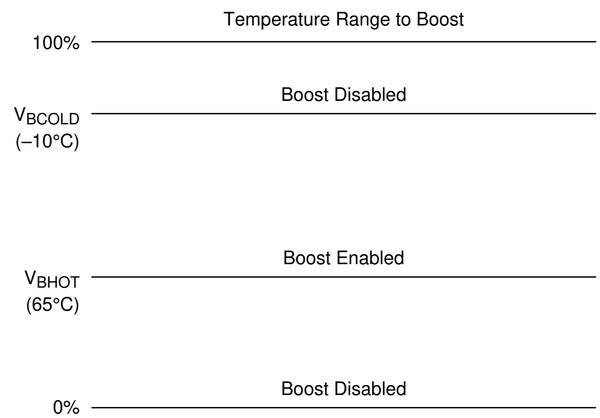


図 9-5. TS Pin Thermistor Sense Threshold in Boost Mode

9.3.5.6 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is two hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation throughout the whole charging cycle, the safety timer will expire in 20 hours.

During the fault, timer is suspended. Once the fault goes away, the timer resumes. If user stops the current charging cycle, and start again, timer gets reset.

9.3.6 Status Outputs ($\overline{PG}$, STAT)

9.3.6.1 Power Good Indicator ($\overline{PG}$ Pin)

The $\overline{PG}$ pin goes LOW to indicate a good input source when:

- V_{BUS} above V_{VBUS_UVLO}
- V_{BUS} above battery (not in sleep)
- V_{BUS} below V_{ACOV} threshold
- V_{BUS} above V_{POOSRC} (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed セクション 9.3.2.3

9.3.6.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

表 9-4. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging termination (top off timer may be running)	HIGH
Sleep mode, charge disable, boost mode	HIGH
Charge suspend (input overvoltage, TS fault, safety timer fault or system overvoltage)	Blinking at 1 Hz

9.3.7 Protections

9.3.7.1 Input Current Limit

The device's ILIM pin is to program maximum input current when D+/D- detection identifies an unknown adaptor plugged in. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

9.3.7.2 Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

9.3.7.2.1 Voltage and Current Monitoring in Buck Mode

9.3.7.2.1.1 Input Overvoltage (ACOV)

If VAC exceeds V_{VAC_OV}, HSFET stops switching immediately.

9.3.7.2.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulate at V_{SYS_MIN}. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30-mA discharge current ($I_{SYSLOAD}$) to bring down the system voltage.

9.3.7.3 Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

9.3.7.3.1 VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

9.3.7.3.2 VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The boost build in accurate constant current regulation to allow OTG to adapt to various types of load. If a short circuit is detected on VBUS, boost turns off and retries 7 times. If retries are not successful, OTG is disabled.

9.3.7.3.3 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG_OVP, the device stop switching.

9.3.7.4 Thermal Regulation and Thermal Shutdown

9.3.7.4.1 Thermal Protection in Buck Mode

The BQ25606 monitors the internal junction temperature T_J to avoid overheat of the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate.

9.3.7.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT} (160°C), the boost mode is disabled and BATFET is turned off. When IC junction temperature is below T_{SHUT}(160°C) - T_{SHUT_HYS} (30°C), the BATFET is enabled automatically to allow system to restore.

9.3.7.5 Battery Protection

9.3.7.5.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging.

9.3.7.5.2 Battery Overdischarge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from overdischarge. To recover from overdischarge latch-off, an input source plug-in is required at VBUS. The battery is charged with I_{SHORT} (typically 100 mA) current when the $V_{BAT} < V_{SHORT}$, or precharge current as set by 5% of ICHG when the battery voltage is between V_{SHORTZ} and V_{BAT_LOWV}.

9.3.7.5.3 System Overcurrent Protection

When the system is shorted or significantly overloaded ($I_{BAT} > I_{BATOP}$) and the current exceeds BATFET overcurrent limit, the BATFET latches off. The BATFET latch can be reset with VBUS plug-in.

10 Application and Implementation

Note

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10.1 Application Information

A typical application consists of the device configured as a stand-alone power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of Smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

10.2 Typical Application

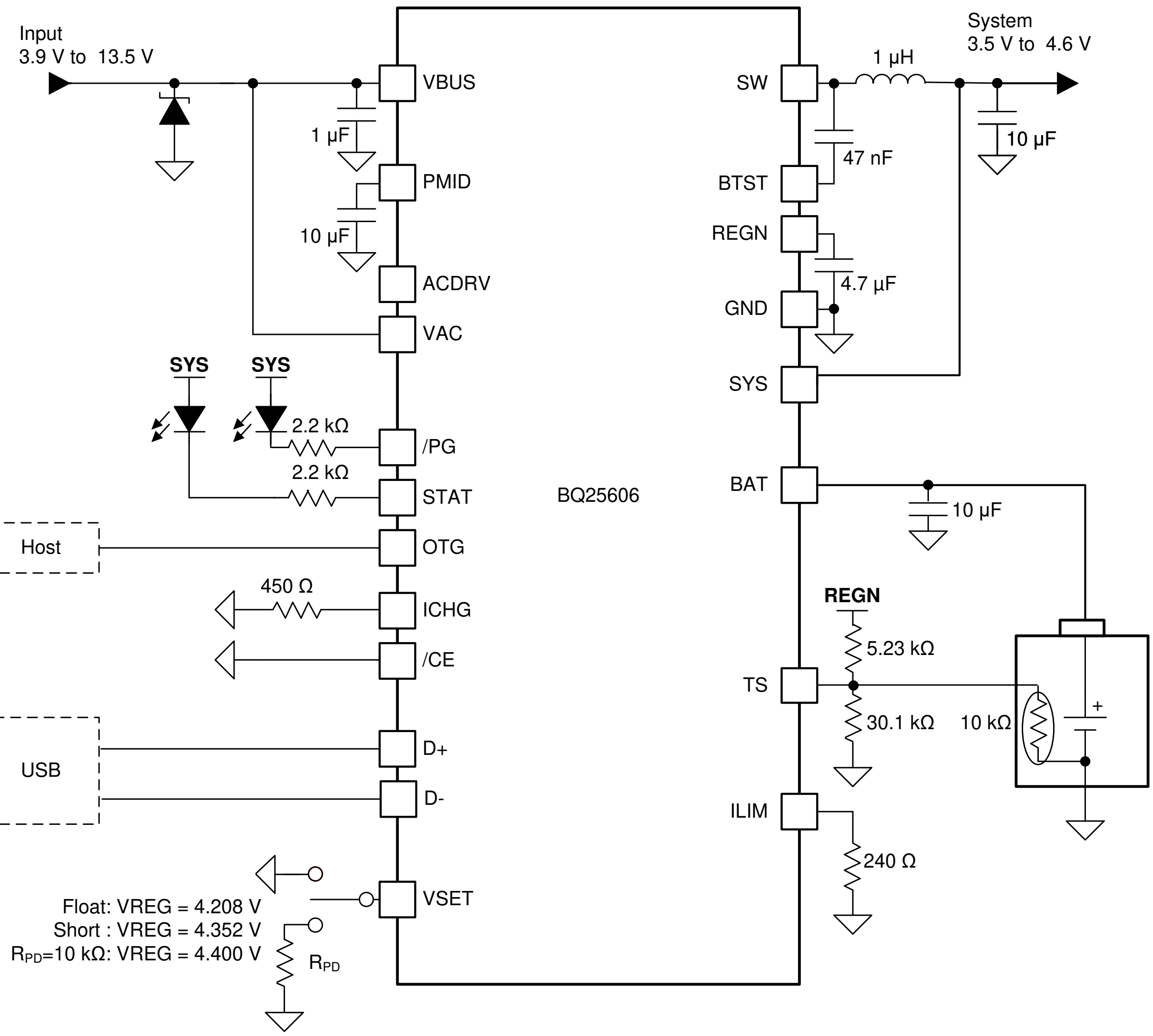


図 10-1. BQ25606 Application Diagram

10.2.1 Design Requirements

表 10-1. Design Parameters

PARAMETER	VALUE
V_{BUS} voltage range	4 V to 13.5 V
Input current limit (D+/D– detection)	2.4 A
Fast charge current limit (ICHG pin)	ICHG pin
Minimum system voltage	3.5 V
Battery regulation voltage (VSET pin)	4.2 V

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{4}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{5}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using 式 6.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{6}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25 V or higher capacitor is preferred for 15-V input voltage. Capacitance of 22 µF is suggested for typical of 3-A charging current.

10.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. 式 7 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

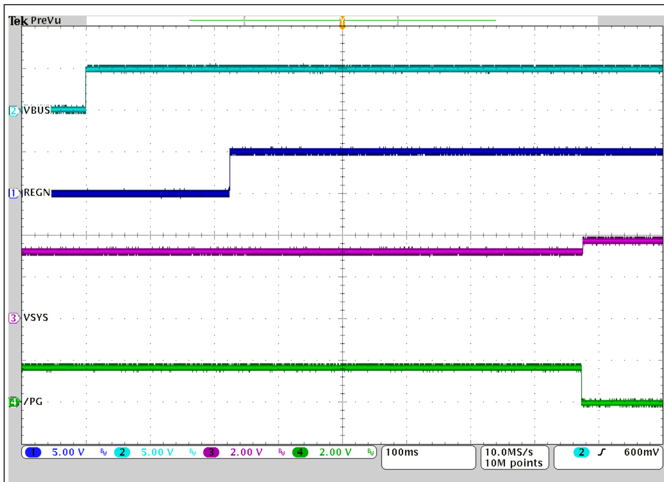
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{8}$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

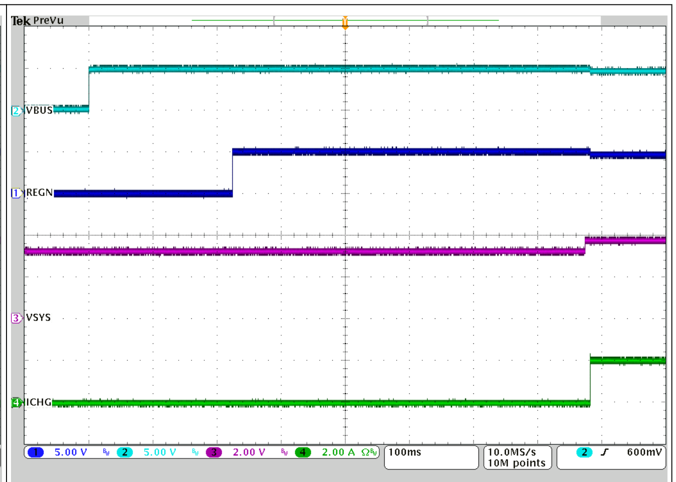
The charger device has internal loop compensation optimized for ≤20-µF ceramic output capacitance. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

10.2.3 Application Curves



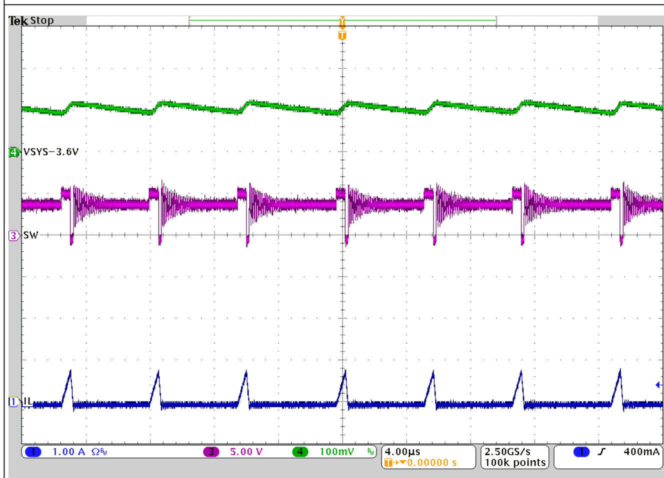
V_{VBUS} = 5 V V_{VBAT} = 3.2 V

図 10-2. Power Up with Charge Disabled



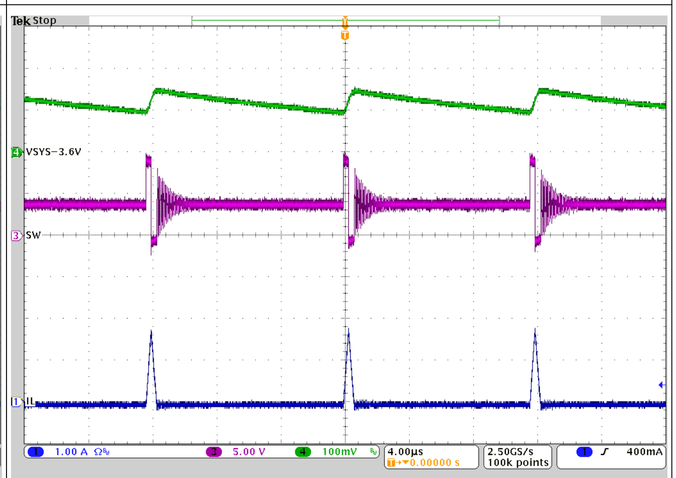
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

図 10-3. Power Up with Charge Enabled



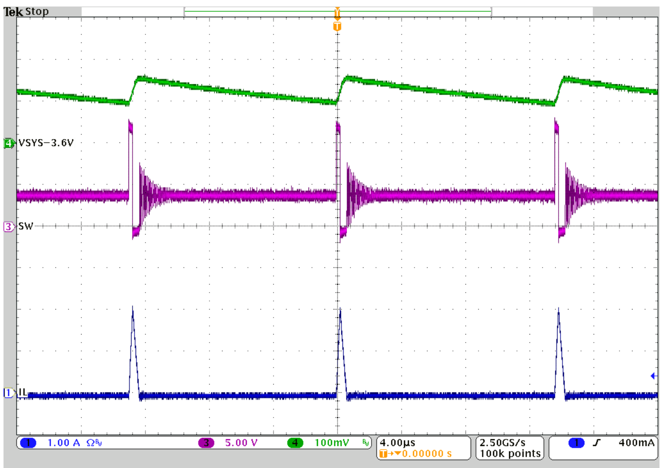
V_{VBUS} = 5 V
I_{SYS} = 50 mA Charge Disabled

図 10-4. PFM Switching in Buck Mode



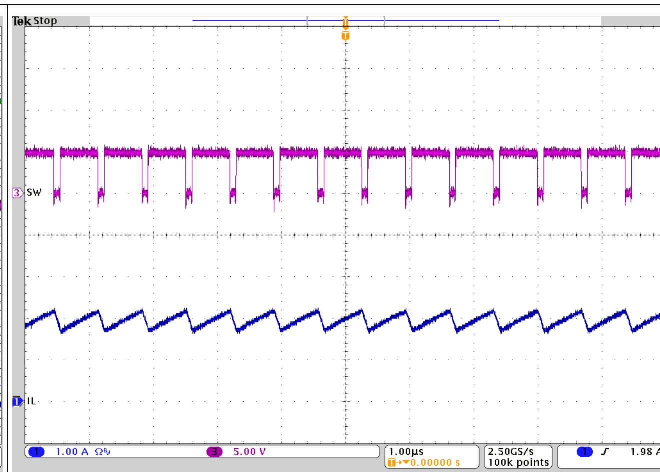
V_{VBUS} = 9 V
I_{SYS} = 50 mA Charge Disabled

図 10-5. PFM Switching in Buck Mode



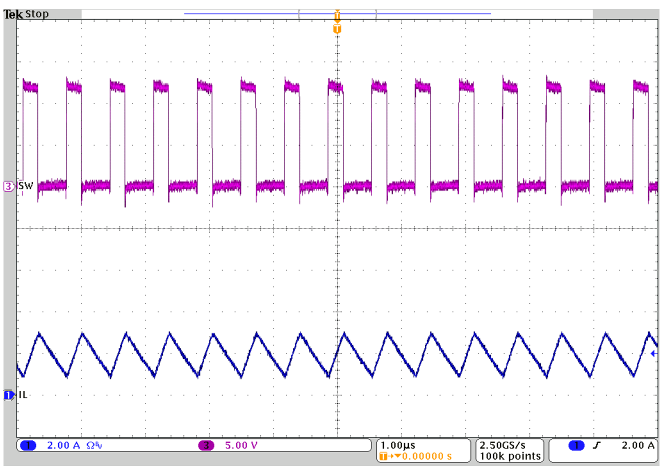
V_{VBUS} = 12 V
I_{SYS} = 50 mA Charge Disabled

図 10-6. PFM Switching in Buck Mode



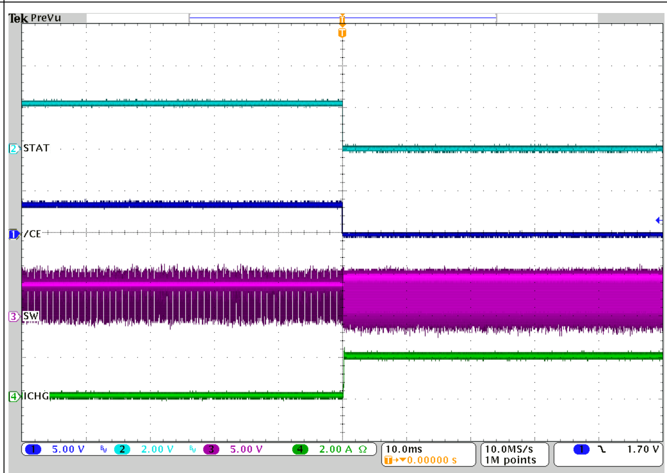
V_{VBUS} = 5 V V_{VBAT} = 3.8 V
I_{CHG} = 2 A

図 10-7. PWM Switching in Buck Mode



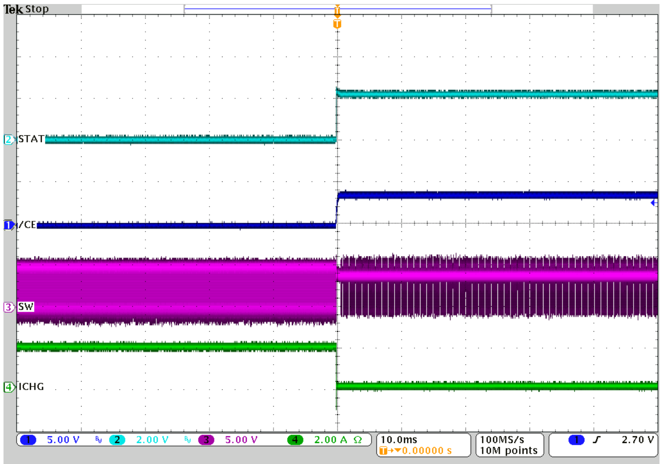
V_{VBUS} = 12 V V_{VBAT} = 3.8 V
I_{CHG} = 2 A

図 10-8. PWM Switching in Buck mode



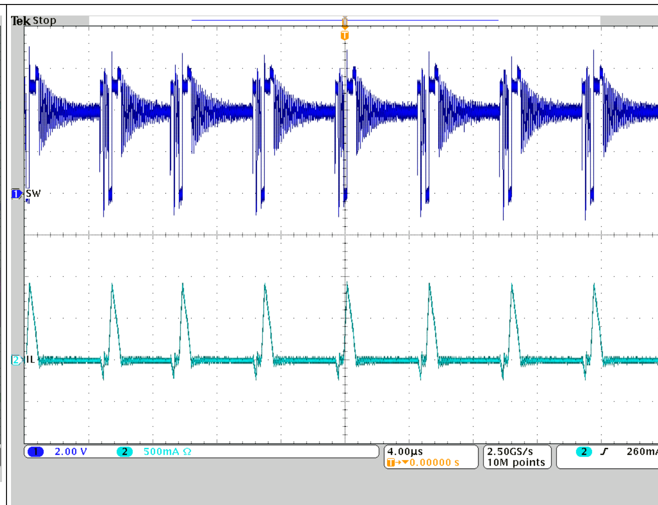
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

図 10-9. Charge Enable



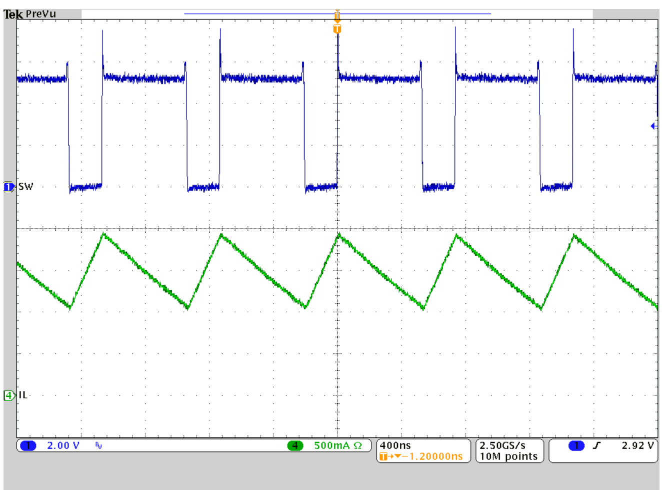
V_{VBUS} = 5 V
I_{CHG} = 2 A
V_{VBAT} = 3.2 V

図 10-10. Charge Disable



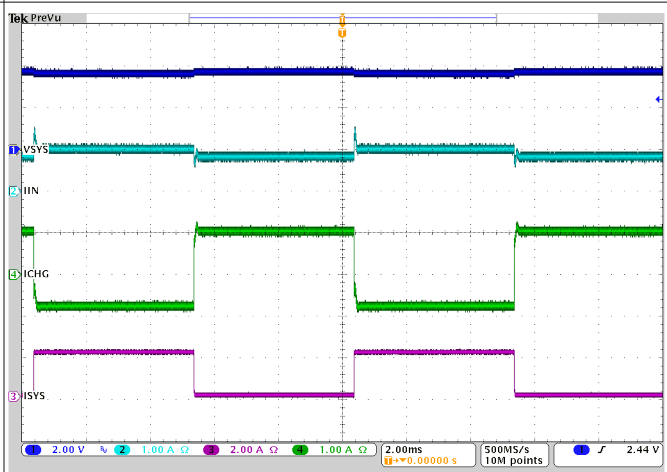
V_{VBAT} = 4 V
I_{LOAD}= 50 mA
PFM Enabled

図 10-11. OTG Switching



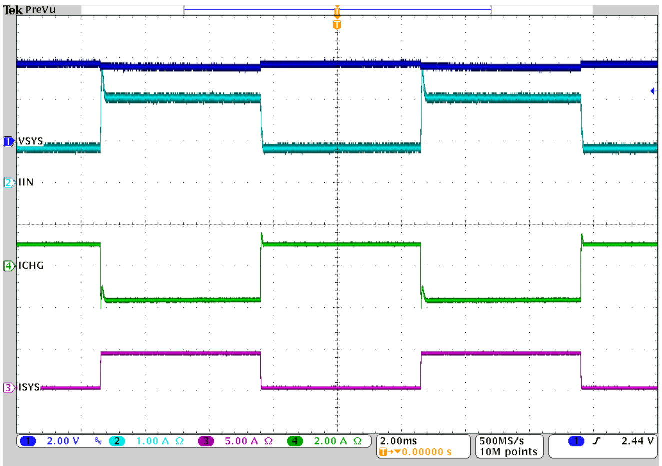
V_{VBAT} = 4 V
I_{LOAD}= 1 A
PFM Enabled

図 10-12. OTG Switching



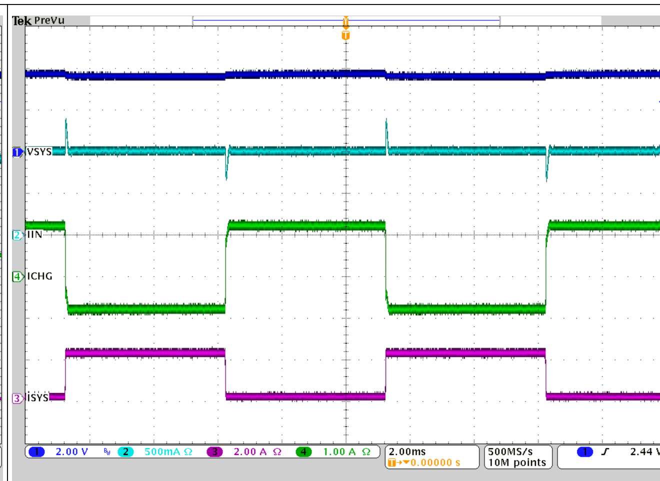
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 1 A

図 10-13. System Load Transient



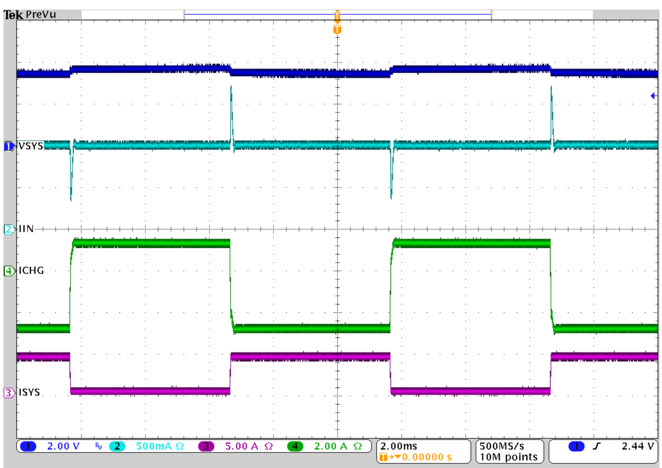
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 1 A

図 10-14. System Load Transient



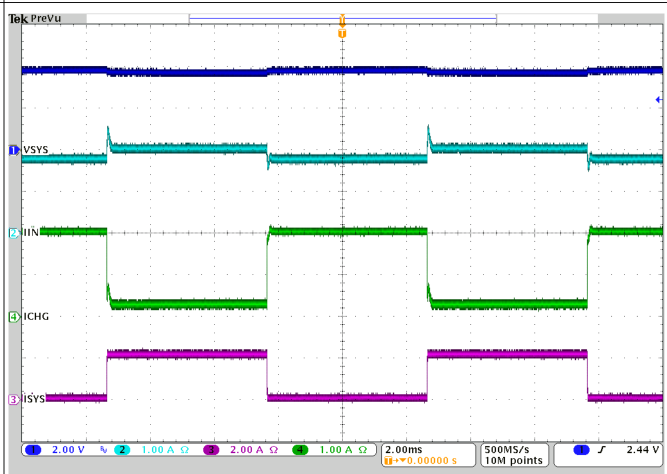
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

図 10-15. System Load Transient



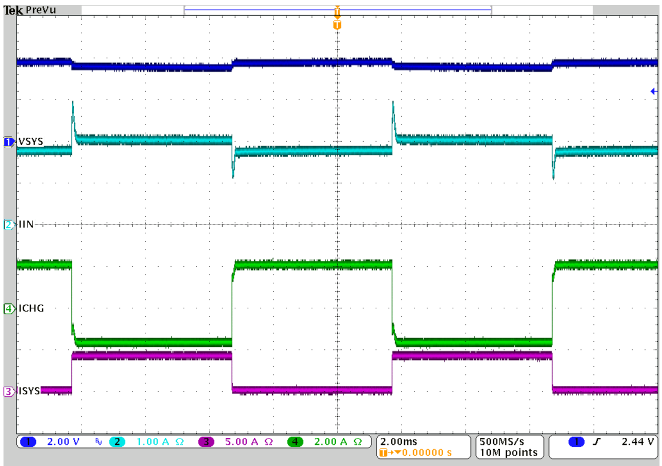
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

図 10-16. System Load Transient



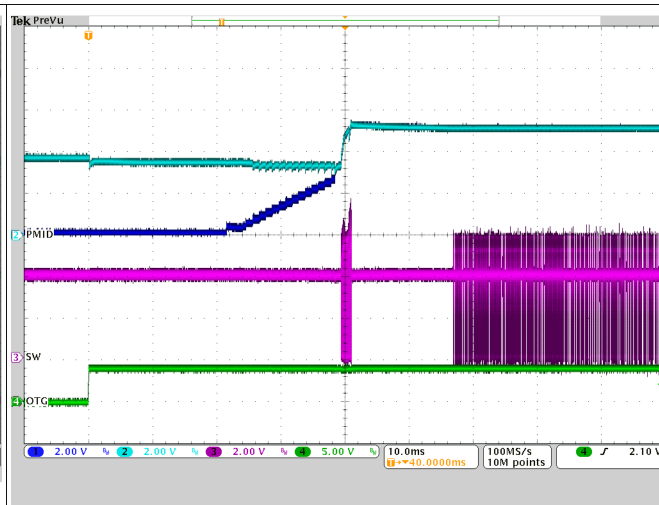
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 2 A

図 10-17. System Load Transient



V_{VBUS} = 5 V
I_{INDPM} = 2 A
I_{SYS} from 0 A to 4 A
I_{CHG} = 2 A
V_{BAT} = 3.7 V

図 10-18. System Load Transient



V_{BAT} = 3.8 V
C_{LOAD} = 470 µF

図 10-19. OTG Start Up

11 Power Supply Recommendations

In order to provide an output voltage on SYS, the BQ25606 device requires a power supply between 3.9-V and 13.5-V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 図 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

Refer to the *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide* for the recommended component placement with trace and via locations. For the VQFN information, refer to the *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

12.2 Layout Example

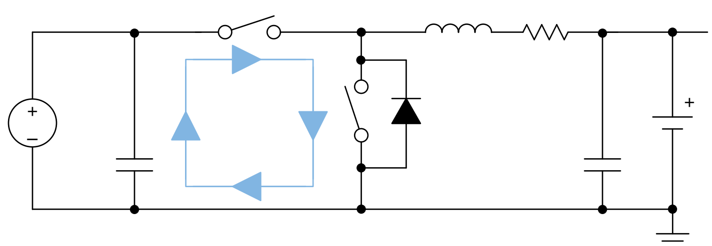


図 12-1. High Frequency Current Path

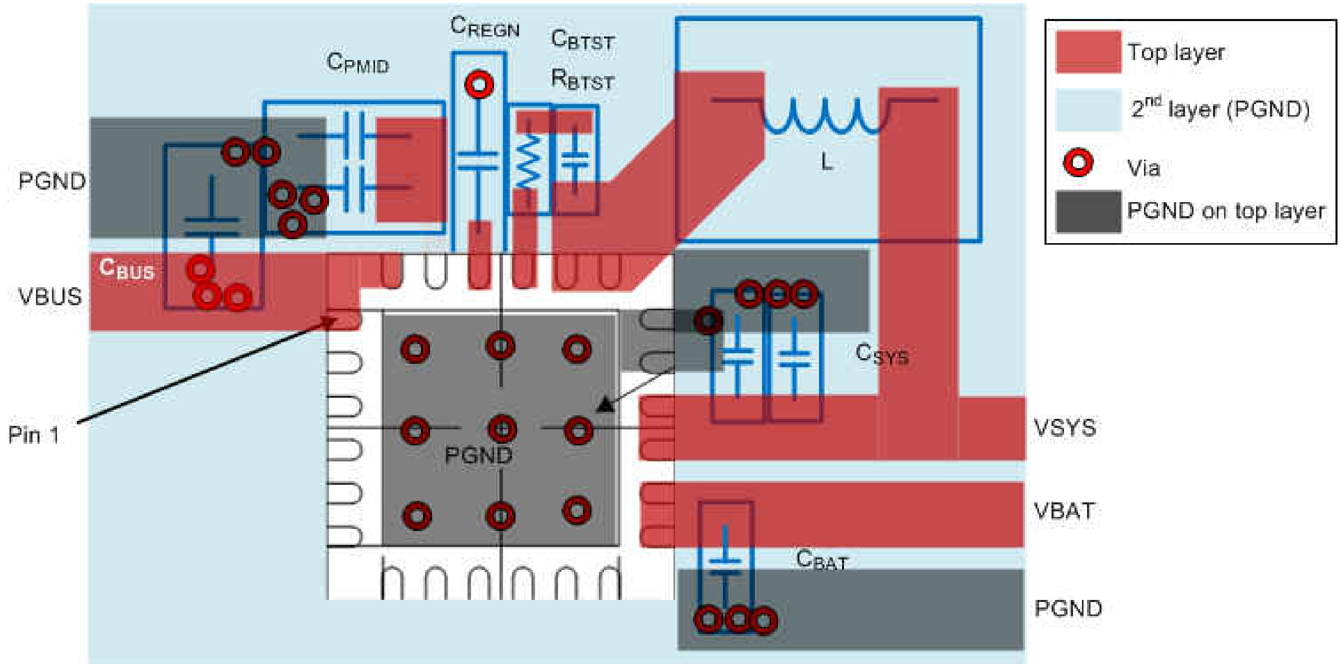


図 12-2. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.3 サポート・リソース

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13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25606RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25606
BQ25606RGER.Z	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25606
BQ25606RGERG4.Z	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25606
BQ25606RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25606
BQ25606RGET.Z	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25606

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

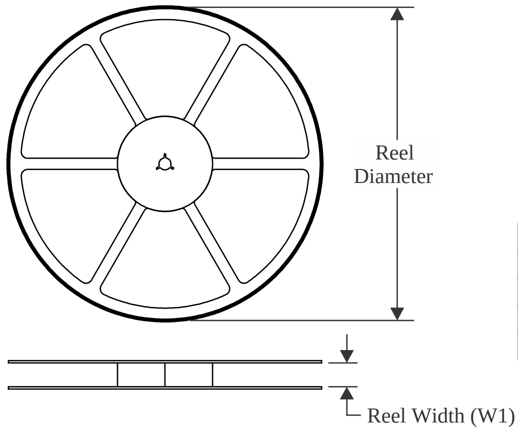
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

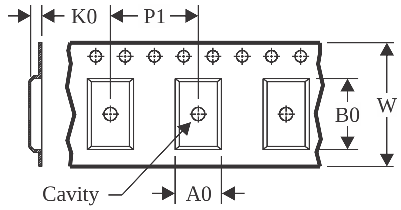
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

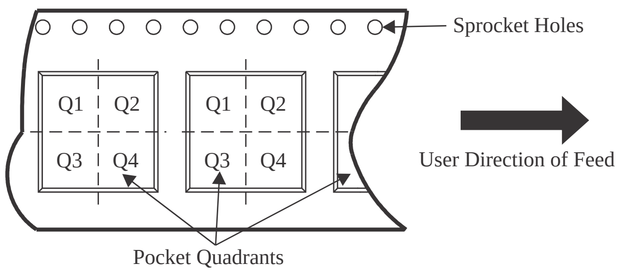


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

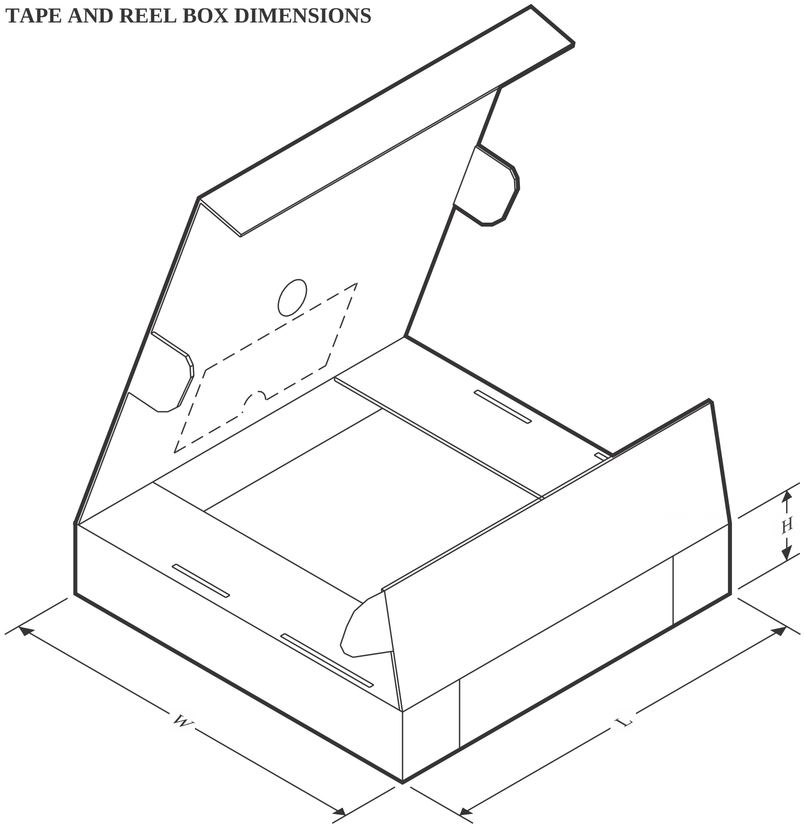
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

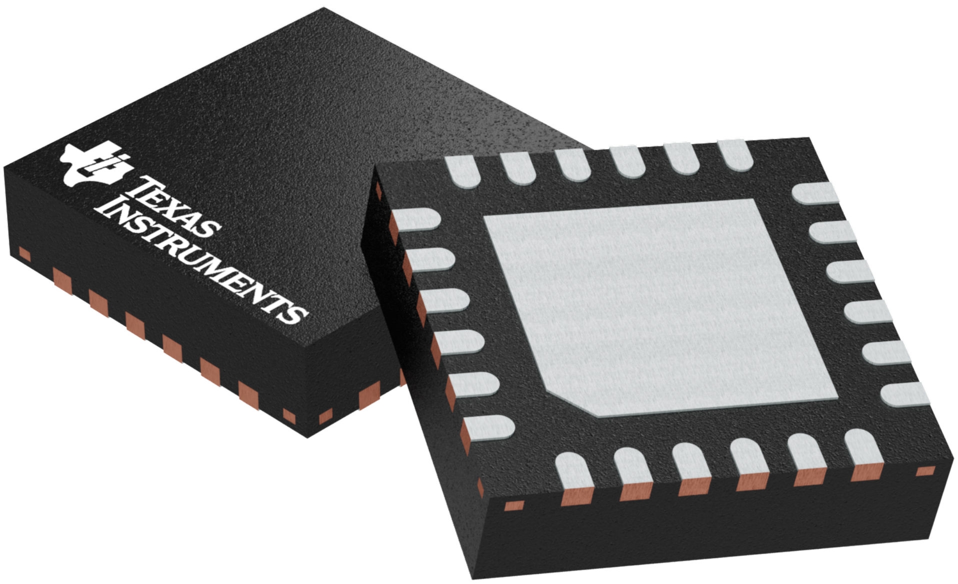
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25606RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25606RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



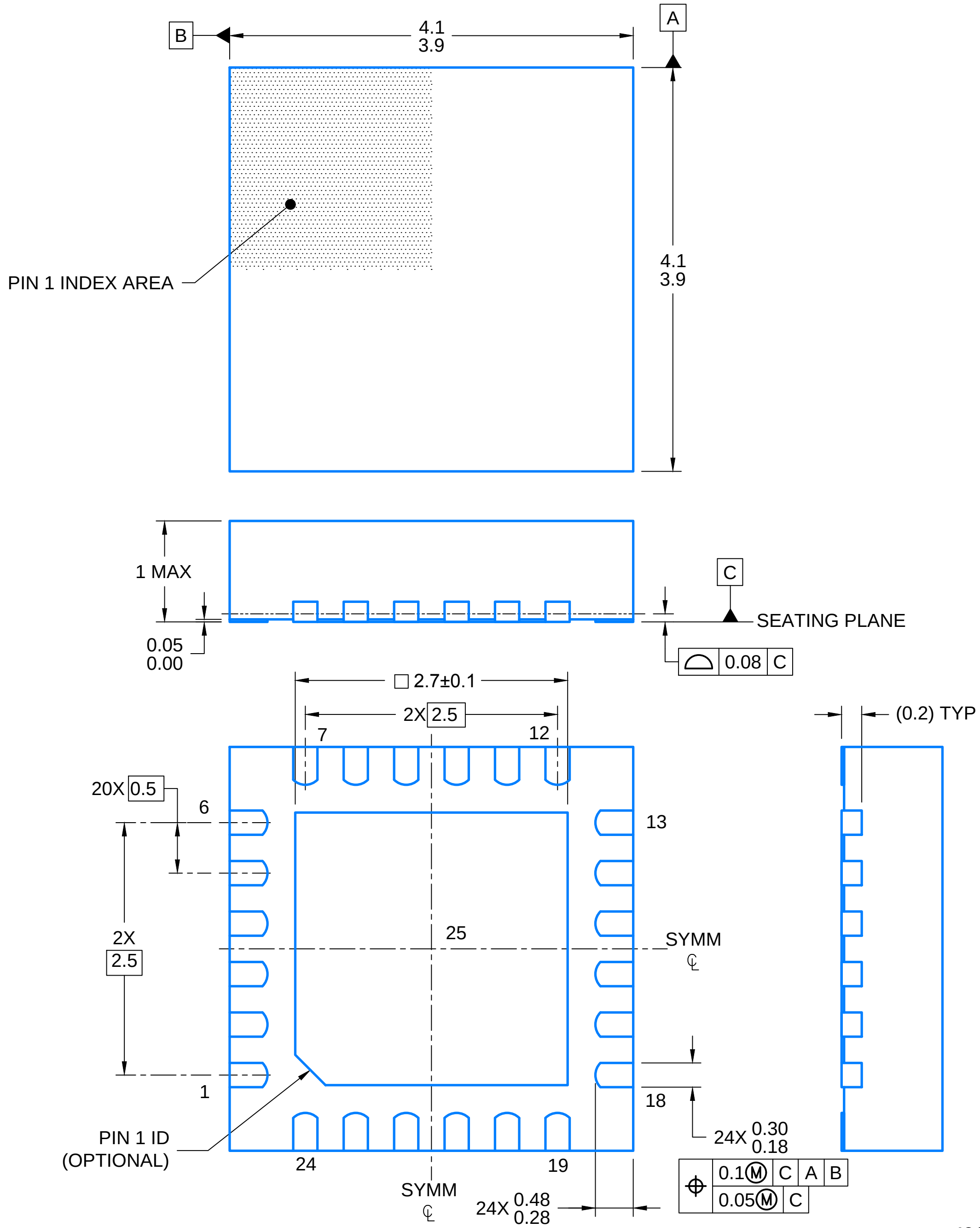
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25606RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ25606RGET	VQFN	RGE	24	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



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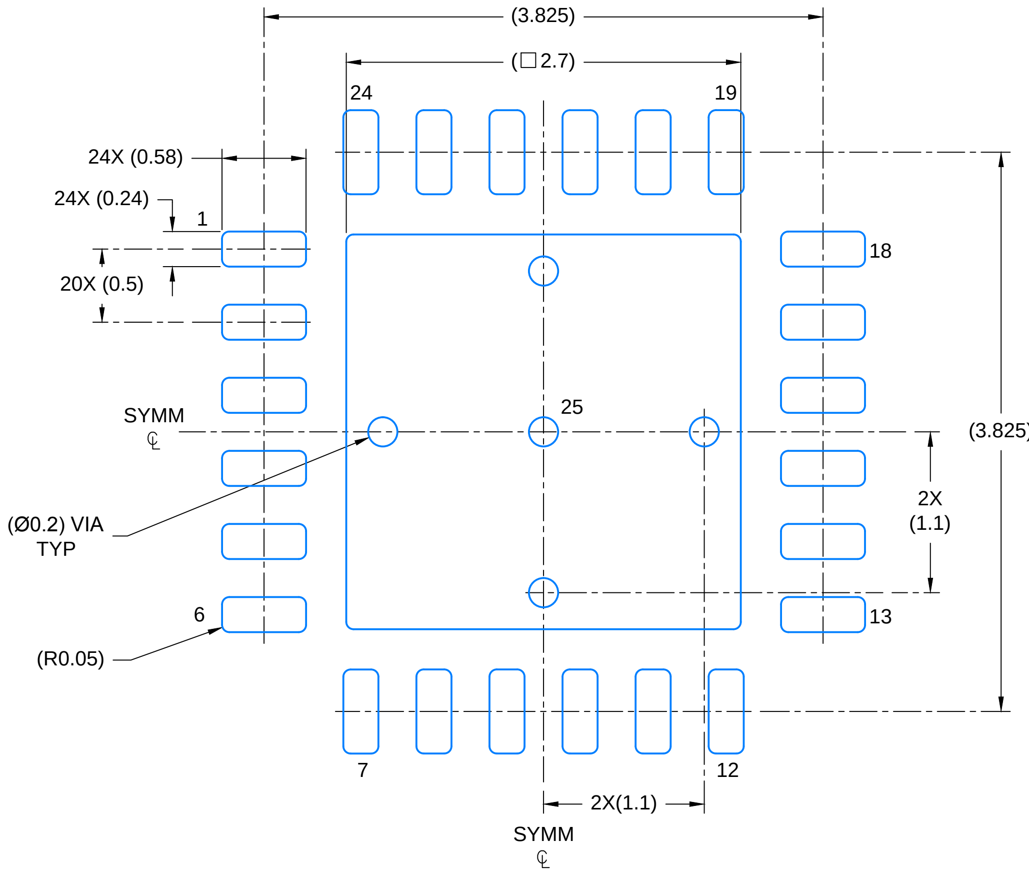
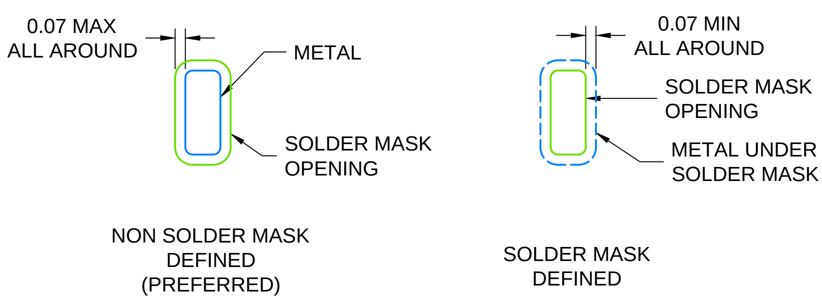
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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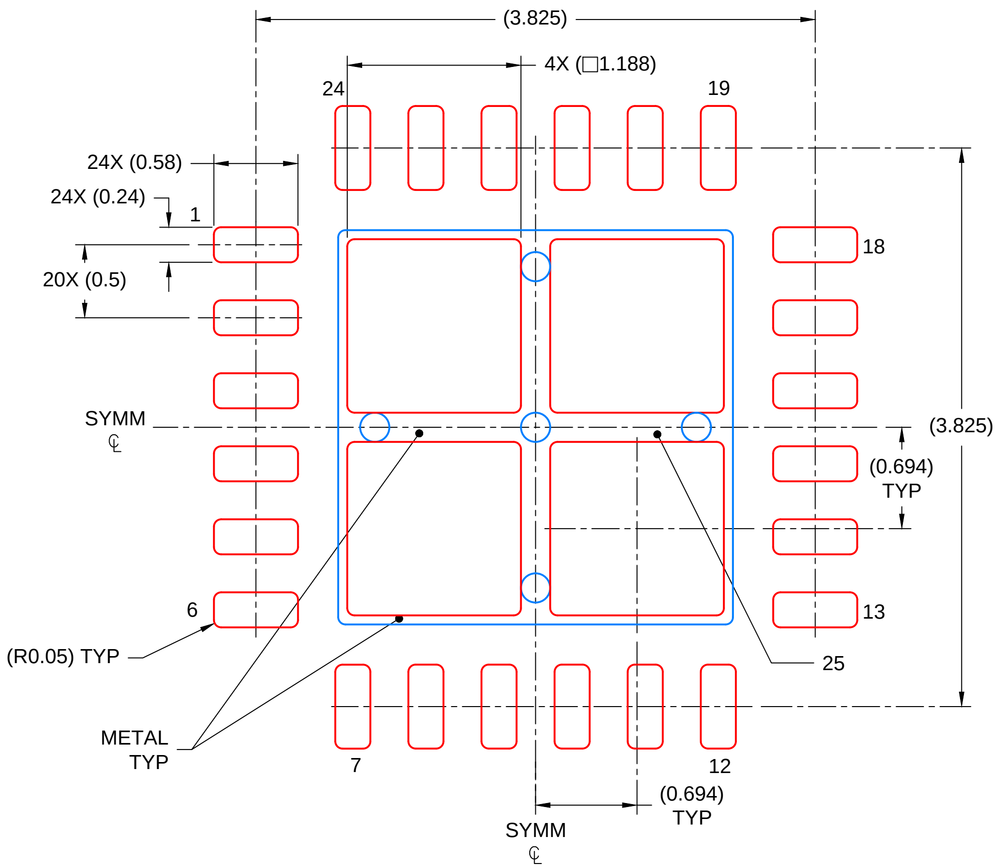
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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