# ISO7041-Q1 車載用、超低消費電力 4 チャネル・デジタル・アイソレータ

## 1 特長

- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能 ISO7041-Q1
- VDA320 絶縁要件に適合
- 超低消費電力
  - チャネルあたり 3.5μA の静止電流 (3.3V)
  - 100kbps 時にチャネルあたり 15μA (3.3V)
  - 1Mbps 時にチャネルあたり 116μA (3.3V)
- 堅牢な絶縁バリア
  - 推定寿命:100 年超
  - 定格絶縁電圧:3000$V_{RMS}$
  - CMTI:±100kV/μs (標準値)
- 広い電源電圧範囲:3.0V～5.5V
- 広い温度範囲:–40℃～+125℃
- 小型の 16-QSOP パッケージ (16-DBQ)
- 信号速度:最大 4Mbps
- デフォルト出力 HIGH (ISO7041-Q1) と LOW (ISO7041F-Q1) のオプション
- 堅牢な電磁両立性 (EMC)
  - システム・レベルの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 超低エミッション
- 安全関連認証 (予定):
  - DIN V VDE 0884-11:2017-01
  - UL 1577 部品認定プログラム
  - IEC 60950-1、IEC 62368-1、IEC 61010-1、IEC60601-1 および GB 4943.1-2011 認証

## 2 アプリケーション

- ハイブリッド、電気自動車、およびパワートレイン・システム (EV/HEV)
  - バッテリ管理システム (BMS)
  - オンボード・チャージャ
  - トラクション・インバータ
  - DC/DC コンバータ
  - インバータおよびモータ制御

## 3 説明

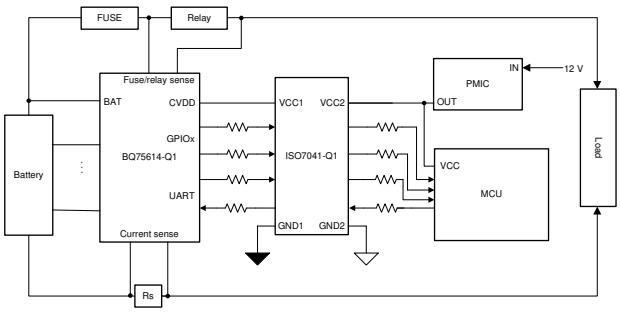
ISO7041-Q1 デバイスは超低消費電力のマルチチャネル・デジタル・アイソレータで、CMOS または LVCMOS デジタル I/O を絶縁できます。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 ($SiO_2$) 絶縁バリアによって分離されています。革新的なエッジ・ベースのアーキテクチャとオン/オフ変調方式の組み合わせにより、超低消費電力でありながら、UL1577 に準拠した 3000$V_{RMS}$ の定格絶縁電圧を実現しています。チャネルごとの動的な消費電流は 120μA/Mbps 未満、チャネルごとの静的な消費電流は 3.3V 時に 3.5μA であるため、ISO7041-Q1 は電力と熱の両方において制約のあるシステム設計でも使用できます。

最小 3.0V、最大 5.5V で動作し、絶縁バリアの両側の電源電圧が異なる場合も完全に機能します。4 チャネルのアイソレータは 16-QSOP パッケージで供給されます (順方向チャネルが 3 つ、逆方向チャネルが 1 つ)。このデバイスには、デフォルト出力が HIGH と LOW のオプションがあります。入力電力または信号が消失した場合のデフォルト出力は、接尾辞 F の付かない ISO7041-Q1 デバイスでは high、接尾辞 F が付いた ISO7041F-Q1 デバイスでは low です。 詳細については、「デバイスの機能モード」を参照してください。

**デバイス情報**

| 部品番号(1) | パッケージ | 本体サイズ (公称) |
|---|---|---|
| ISO7041-Q1 | QSOP (16) | 4.90mm × 3.90mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**アプリケーション概略回路図**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# Table of Contents

**1 特長**.....1
**2 アプリケーション**.....1
**3 説明**.....1
**4 Revision History**.....2
**5 Pin Configuration and Functions**.....3
**6 Specifications**.....4
6.1 絶対最大定格.....4
6.2 ESD Ratings.....4
6.3 Recommended Operating Conditions.....5
6.4 Thermal Information.....6
6.5 Power Ratings.....6
Insulation Specifications.....7
6.6 Safety-Related Certifications.....8
6.7 Safety Limiting Values.....8
6.8 Electrical Characteristics 5V Supply.....9
6.9 Supply Current Characteristics 5V Supply.....9
6.10 Electrical Characteristics 3.3V Supply.....11
6.11 Supply Current Characteristics 3.3V Supply.....11
6.12 Switching Characteristics.....12
6.13 Insulation Characteristics Curves.....12
6.14 Typical Characteristics.....13
**7 Parameter Measurement Information**.....14
**8 Detailed Description**.....15
8.1 Overview.....15
8.2 Functional Block Diagram.....15
8.3 Feature Description.....15
8.4 Device Functional Modes.....17
**9 Application and Implementation**.....19
9.1 Application Information.....19
9.2 Typical Application.....20
**10 Power Supply Recommendations**.....24
**11 Layout**.....25
11.1 Layout Guidelines.....25
11.2 Layout Example.....25
**12 Device and Documentation Support**.....26
12.1 Documentation Support.....26
12.2 Receiving Notification of Documentation Updates.....26
12.3 サポート・リソース.....26
12.4 Trademarks.....26
12.5 Electrostatic Discharge Caution.....26
12.6 Glossary.....26
**13 Mechanical, Packaging, and Orderable Information**.....26

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---|---|---|
| June 2022 | * | Initial Release |


Copyright © 2022 Texas Instruments Incorporated

## Device Comparison Table

表 5-1. Device Features

| PART NUMBER | CHANNEL DIRECTION | MAXIMUM DATA RATE | DEFAULT OUTPUT | PACKAGE | RATED ISOLATION |
|---|---|---|---|---|---|
| ISO7041-Q1 | 3 Forward, 1 Reverse | 4 Mbps | High | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7041-Q1 with F suffix | 3 Forward, 1 Reverse | 4 Mbps | Low | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |

## 5 Pin Configuration and Functions

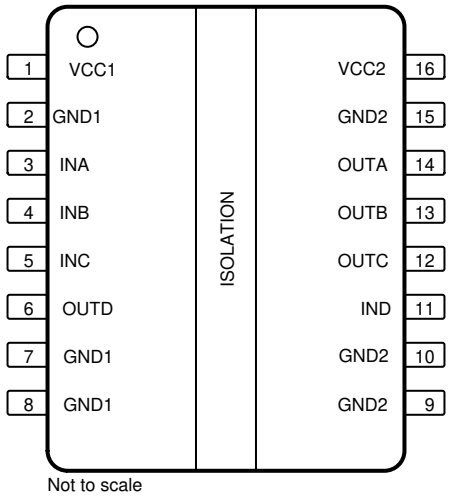



図 5-1. ISO7041-Q1 DBQ Package 16-Pin QSOP Top View

表 5-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND1 | 2 | — | Ground connection for $V_{CC1}$ |
| | 7 | | |
| | 8 | | |
| GND2 | 9 | — | Ground connection for $V_{CC2}$ |
| | 10 | | |
| | 15 | | |
| INA | 3 | I | Input, channel A. 300-Ω series resistor recommended |
| INB | 4 | I | Input, channel B. 300-Ω series resistor recommended |
| INC | 5 | I | Input, channel C. 300-Ω series resistor recommended |
| IND | 11 | I | Input, channel D. 300-Ω series resistor recommended |
| OUTA | 14 | O | Output, channel A. 300-Ω series resistor recommended |
| OUTB | 13 | O | Output, channel B. 300-Ω series resistor recommended |
| OUTC | 12 | O | Output, channel C. 300-Ω series resistor recommended |
| OUTD | 6 | O | Output, channel D. 300-Ω series resistor recommended |
| $V_{CC1}$ | 1 | — | Power supply, side 1 |
| $V_{CC2}$ | 16 | — | Power supply, side 2 |

Copyright © 2022 Texas Instruments Incorporated

# 6 Specifications

## 6.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り)(1) (2) (3)

| | | 最小値 | 最大 | 単位 |
|---|---|---|---|---|
| 電源電圧 | $V_{CC1}$ から GND1 | -0.5 | 6 | V |
| | $V_{CC2}$ から GND2 | -0.5 | 6 | |
| 入力/出力電圧 | INx から GNDx | -0.5 | $V_{CCX}$ + 0.5 | V |
| | OUTx から GNDx | -0.5 | $V_{CCX}$ + 0.5 | |
| | ENx から GNDx | -0.5 | $V_{CCX}$ + 0.5 | |
| 入力電流 | 入力チャネル、Ii | -15 | 15 | mA |
| 出力電流 | Io | -15 | 15 | mA |
| 温度 | 動作時の接合部温度、$T_J$ | | 150 | ℃ |
| | 保管温度、$T_{stg}$ | -65 | 150 | ℃ |

(1) 絶対最大定格を上回るストレスが加わった場合、デバイスに永続的な損傷が発生する可能性があります。これはストレスの定格のみについて示してあり、このデータシートの「推奨動作条件」に示された値を超える状態で本製品が正常に動作することを暗黙的に示すものではありません。絶対最大定格の状態に長時間置くと、本製品の信頼性に影響を与えることがあります。
(2) 差動 I/O バス電圧を除くすべての電圧値は、ローカル・グランド・ピン (GND1 または GND2) を基準としており、ピーク電圧値です。
(3) 最大電圧は 6V 以下である必要があります。

## 6.2 ESD Ratings

(1) (2)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±5000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |
| | | Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4) | ±8000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.


Copyright © 2022 Texas Instruments Incorporated

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$ (1) | Supply Voltage Side 1 | | 3.0 | | 5.5 | V |
| $V_{CC2}$ (1) | Supply Voltage Side 2 | | 3.0 | | 5.5 | V |
| $V_{IH}$ | High level Input voltage | | 0.7 x $V_{CCI}$ | | $V_{CCI}$ | V |
| $V_{IL}$ | Low level Input voltage | | 0 | | 0.3 x $V_{CCI}$ | V |
| $I_{OH}$ | High level output current | $V_{CCO}$ (2) = 5 V | -4 | | | mA |
| | | $V_{CCO}$ = 3.3 V | -2 | | | mA |
| $I_{OL}$ | Low level output current | $V_{CCO}$ = 5 V | | | 4 | mA |
| | | $V_{CCO}$ = 3.3 V | | | 2 | mA |
| DR | Data Rate | | 0 | | 4 | Mbps |
| $T_A$ | Ambient temperature | | -40 | | 125 | °C |

(1) $V_{CC1}$ and $V_{CC2}$ can be set independent of one another
(2) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$

Copyright © 2022 Texas Instruments Incorporated

## 6.4 Thermal Information

| THERMAL METRIC(1) | | ISO7041-Q1 DBQ (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 87.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 33.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 1-MHz 50% duty cycle square wave | | | 7.82 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 4.46 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 3.36 | mW |


Copyright © 2022 Texas Instruments Incorporated

## Insulation Specifications

| PARAMETER | | TEST CONDITIONS | SPECIFICATIONS | UNIT |
|---|---|---|---|---|
| | | | QSOP-16 | |
| **IEC 60664-1** | | | | |
| CLR | External clearance(1) | Side 1 to side 2 distance through air | >3.7 | mm |
| CPG | External Creepage(1) | Side 1 to side 2 distance across package surface | >3.7 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | 17 | µm |
| CTI | Comparative tracking index | IEC 60112; UL 746A | >600 | V |
| | Material Group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300 $V_{RMS}$ | I-III | |
| **DIN V VDE V 0884-11:2017-01(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 566 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; See TBD | 400 | $V_{RMS}$ |
| | | DC voltage | 566 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST}$ = $V_{IOTM}$ , t = 60 s (qualification); $V_{TEST}$ = 1.2 × $V_{IOTM}$, t = 1 s (100% production) | 4242 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST}$ = 1.6 × $V_{IOSM}$ = 6400 $V_{PK}$ (qualification) | 4000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a: After I/O safety test subgroup 2/3, $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)}$ = 1.2 × $V_{IORM}$ , $t_m$ = 10 s | ≤ 5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)}$ = 1.6 × $V_{IORM}$ , $t_m$ = 10 s | ≤ 5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)}$ = 1.875 × $V_{IORM}$ , $t_m$ = 1 s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 × sin (2 πft), f = 1 MHz | ~1.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output(5) | $V_{IO}$ = 500 V, $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 150°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 55/125/21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST}$ = $V_{ISO}$ , t = 60 s (qualification); $V_{TEST}$ = 1.2 × $V_{ISO}$ , t = 1 s (100% production) | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

Copyright © 2022 Texas Instruments Incorporated

## 6.6 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN VDE V 0884-11:2017- 01 | Certified according to IEC 60950-1 and IEC 62368-1 | Certified according to UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 | Certified according to EN 61010-1:2010/A1:2019, EN 60950- 1:2006/ A2:2013 and EN 62368-1:2014 |
| Maximum transient isolation voltage, 4242 $V_{PK}$; Maximum repetitive peak isolation voltage, 566 $V_{PK}$; Maximum surge isolation voltage, 4000 $V_{PK}$ | 3000 $V_{RMS}$ insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014 370 $V_{RMS}$ (DBQ-16) maximum working voltage (pollution degree 2, material group I) | Single protection, 3000 $V_{RMS}$ | Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 400 $V_{RMS}$ maximum working voltage | EN 61010- 1:2010/ A1:2019, 300 $V_{RMS}$ basic isolation EN 60950- 1:2006/ A2:2013 and EN 62368-1:2014, 400 $V_{RMS}$ basic isolation |
| Certification Planned | Certification Planned | Certification Planned | Certification Planned | Certification Planned |

## 6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **16-QSOP PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 87°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 261 | mA |
| | | $R_{\theta JA}$ = 87°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 399 | mA |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 87°C/W, $T_J$ = 150°C, $T_A$ = 25°C | | | 1435 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.


Copyright © 2022 Texas Instruments Incorporated

## 6.8 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -4 mA | $V_{CCO}$ - 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -1 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V | 50 | 100 | | kV/us |
| $C_i$ | Input Capacitance (2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 1 MHz, $V_{CC}$ = 5 V | | 2 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 6.9 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7041-Q1** | | | | | | |
| Supply current - DC signal | Refresh disable | $I_{CC1}$ | | 6.2 | 14.3 | µA |
| | | $I_{CC2}$ | | 10.1 | 18.5 | µA |
| | Refresh enable<br>$V_I$ = $V_{CCI}$ (1) (ISO7041-Q1);<br>$V_I$ = 0 V (ISO7041-Q1 with F suffix) | $I_{CC1}$ | | 8.2 | 16.7 | µA |
| | | $I_{CC2}$ | | 10.8 | 18.5 | µA |
| | Refresh enable<br>$V_I$ = 0 V (ISO7041-Q1);<br>$V_I$ = $V_{CCI}$ (ISO7041-Q1 with F suffix) | $I_{CC1}$ | | 9.5 | 19.9 | µA |
| | | $I_{CC2}$ | | 11.3 | 19.5 | µA |
| Supply current - AC signal | Refresh disable<br>10 kbps, No Load | $I_{CC1}$ | | 6.7 | 19.7 | µA |
| | | $I_{CC2}$ | | 11.8 | 20.6 | µA |
| | Refresh disable<br>100 kbps, No Load | $I_{CC1}$ | | 37.1 | 57.4 | µA |
| | | $I_{CC2}$ | | 25.8 | 37.7 | µA |
| | Refresh disable<br>1 Mbps, No Load | $I_{CC1}$ | | 340.5 | 436.1 | µA |
| | | $I_{CC2}$ | | 167.0 | 211.1 | µA |
| | Refresh enable<br>10 kbps, No Load | $I_{CC1}$ | | 10.6 | 20.8 | µA |
| | | $I_{CC2}$ | | 11.9 | 20.4 | µA |
| | Refresh enable<br>100 kbps, No Load | $I_{CC1}$ | | 37.1 | 57.4 | µA |
| | | $I_{CC2}$ | | 25.8 | 37.7 | µA |
| | Refresh enable<br>1 Mbps, No Load | $I_{CC1}$ | | 338.3 | 436.1 | µA |
| | | $I_{CC2}$ | | 166.0 | 211.1 | µA |
| Total Supply Current Per Channel, Refresh Disabled | DC Signal | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 4.1 | 7.4 | µA |
| | 10 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 5.9 | 10.7 | µA |
| | 100 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 17.4 | 23.4 | µA |
| | 1 Mbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 137.0 | 164.5 | µA |

Copyright © 2022 Texas Instruments Incorporated

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Total Supply Current Per Channel, Refresh Enabled | $V_I$ = $V_{CCI}$ (ISO7041-Q1); $V_I$ = 0 V (ISO7041-Q1 with F suffix) | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 4.8 | 8.5 | µA |
| | $V_I$ = 0 V (ISO7041-Q1); $V_I$ = $V_{CCI}$ (ISO7041-Q1 with F suffix) | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 5.3 | 9.6 | µA |
| | 10 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 5.7 | 10.4 | µA |
| | 100 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 16.4 | 22.3 | µA |
| | 1 Mbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 125.9 | 154.0 | µA |

(1) $V_{CCI}$ = Input-side $V_{CC}$


Copyright © 2022 Texas Instruments Incorporated

## 6.10 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -2mA | $V_{CCO}$ - 0.3 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2mA | | | 0.3 | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -1 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V | 50 | 100 | | kV/us |
| $C_i$ | Input Capacitance(2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 1 MHz, $V_{CC}$ = 3.6 V | | 2 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 6.11 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7041-Q1** | | | | | | |
| Supply current - DC signal | Refresh disable | $I_{CC1}$ | | 5.1 | 8.8 | µA |
| | | $I_{CC2}$ | | 8.9 | 14.0 | µA |
| | Refresh enable<br>$V_I$ = $V_{CCI}$ (1) (ISO7041-Q1);<br>$V_I$ = 0 V (ISO7041-Q1 with F suffix) | $I_{CC1}$ | | 6.8 | 12.2 | µA |
| | | $I_{CC2}$ | | 9.6 | 14.0 | µA |
| | Refresh enable<br>$V_I$ = 0 V (ISO7041-Q1);<br>$V_I$ = $V_{CCI}$ (ISO7041-Q1 with F suffix) | $I_{CC1}$ | | 8.1 | 14.8 | µA |
| | | $I_{CC2}$ | | 10.0 | 15.6 | µA |
| Supply current - AC signal | Refresh disable<br>10 kbps, No Load | $I_{CC1}$ | | 7.9 | 13.7 | µA |
| | | $I_{CC2}$ | | 10.4 | 15.9 | µA |
| | Refresh disable<br>100 kbps, No Load | $I_{CC1}$ | | 35.9 | 48.3 | µA |
| | | $I_{CC2}$ | | 22.7 | 31.4 | µA |
| | Refresh disable<br>1 Mbps, No Load | $I_{CC1}$ | | 316.4 | 395.7 | µA |
| | | $I_{CC2}$ | | 147.2 | 188.2 | µA |
| | Refresh enable<br>10 kbps, No Load | $I_{CC1}$ | | 9.8 | 16.4 | µA |
| | | $I_{CC2}$ | | 10.5 | 16.2 | µA |
| | Refresh enable<br>100 kbps, No Load | $I_{CC1}$ | | 35.9 | 48.3 | µA |
| | | $I_{CC2}$ | | 22.7 | 31.4 | µA |
| | Refresh enable<br>1 Mbps, No Load | $I_{CC1}$ | | 315.3 | 395.7 | µA |
| | | $I_{CC2}$ | | 146.2 | 188.2 | µA |
| Total Supply Current Per Channel, Refresh Disabled | DC Signal | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 3.5 | 5.7 | µA |
| | 10 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 5.2 | 8.2 | µA |
| | 100 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 14.8 | 19.2 | µA |
| | 1 Mbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 115.7 | 138.7 | µA |

Copyright © 2022 Texas Instruments Incorporated

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Total Supply Current Per Channel, Refresh Enabled | $V_I$ = $V_{CCI}$ (ISO7041-Q1); $V_I$ = 0 V (ISO7041-Q1 with F suffix) | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 4.2 | 6.8 | µA |
| | $V_I$ = 0 V (ISO7041-Q1); $V_I$ = $V_{CCI}$ (ISO7041-Q1 with F suffix) | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 4.6 | 7.7 | µA |
| | 10 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 5.2 | 8.2 | µA |
| | 100 kbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 14.8 | 19.2 | µA |
| | 1 Mbps, No Load | $I_{CC1(ch)}$ + $I_{CC2(ch)}$ | | 115.7 | 138.7 | µA |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 6.12 Switching Characteristics

$V_{CC1}$, $V_{CC2}$ = 3.0 V to 5.5 V (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See 図 7-1 | | 148 | 165 | ns |
| $t_{P(dft)}$ | Propagation delay drift | | | 15 | | ps/°C |
| $t_{UI}$ | Minimum pulse width | See 図 7-1 | 250 | | | ns |
| PWD | Pulse width distortion | | | | 10 | ns |
| $t_{sk(o)}$ | Channel to channel output skew time | Same-direction channels | | | 10 | ns |
| | | Opposite-direction channels | | | 10 | ns |
| $t_{sk(p-p)}$ | Part to part skew time | | | | 70 | ns |
| $t_r$ | Output signal rise time | See 図 7-1 | | | 16 | ns |
| $t_f$ | Output signal fall time | See 図 7-1 | | | 16 | ns |
| $t_{DO}$ | Default output delay time from input power loss | See 図 7-2 | | 400 | 750 | us |
| $t_{PU}$ | Time from UVLO to valid output data | | 1 | | 5 | ms |
| $F_R$ | Refresh rate | | 5 | 10 | | kbps |

## 6.13 Insulation Characteristics Curves

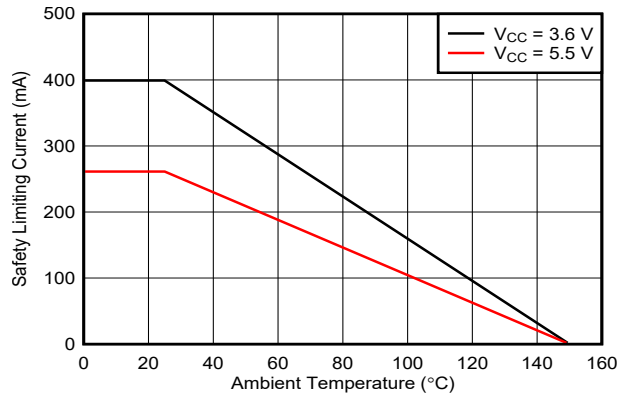



**図 6-1. Thermal Derating Curve for Limiting Current per VDE**

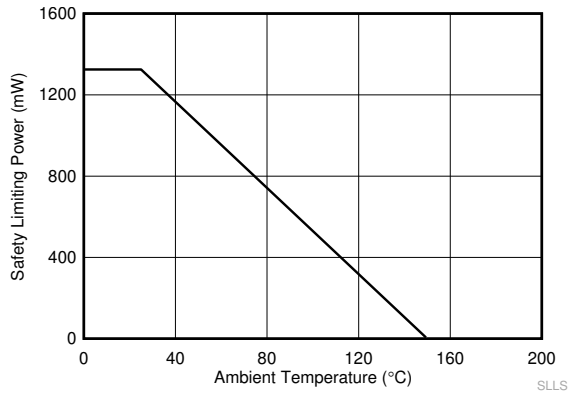
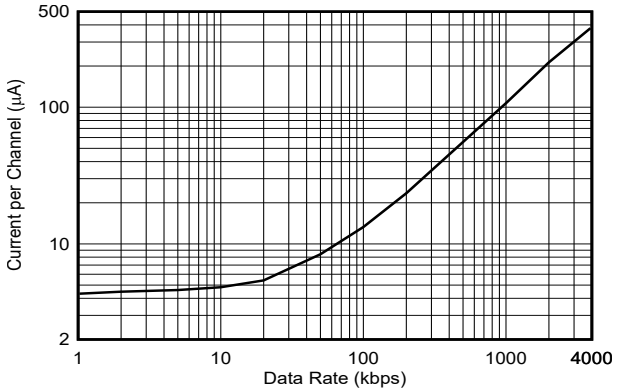



**図 6-2. Thermal Derating Curve for Limiting Power per VDE**

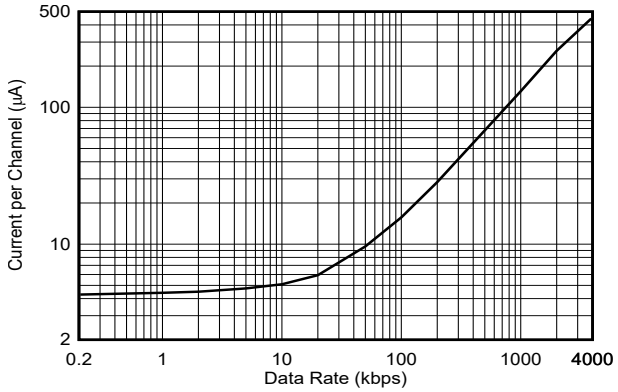

Copyright © 2022 Texas Instruments Incorporated

## 6.14 Typical Characteristics



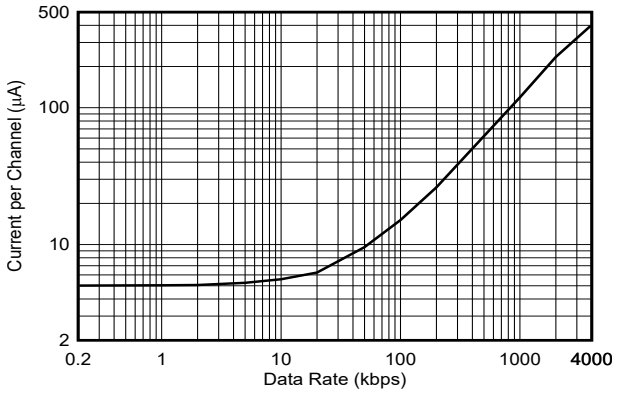

$T_A$ = 25°C $C_L$ = 0 pF

**図 6-3. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With No Load)**



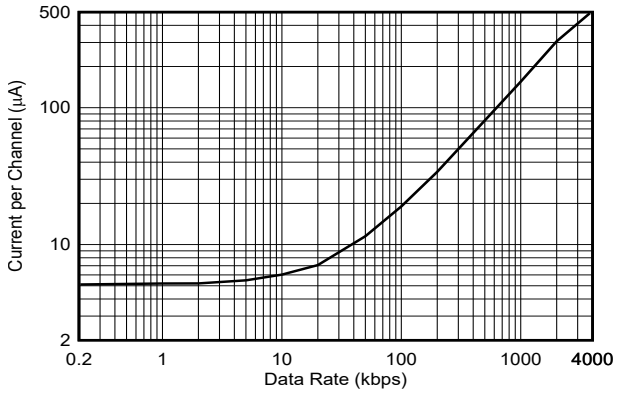

$T_A$ = 25°C $C_L$ = 15 pF

**図 6-4. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)**




$T_A$ = 25°C $C_L$ = 0 pF

**図 6-5. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With No Load)**

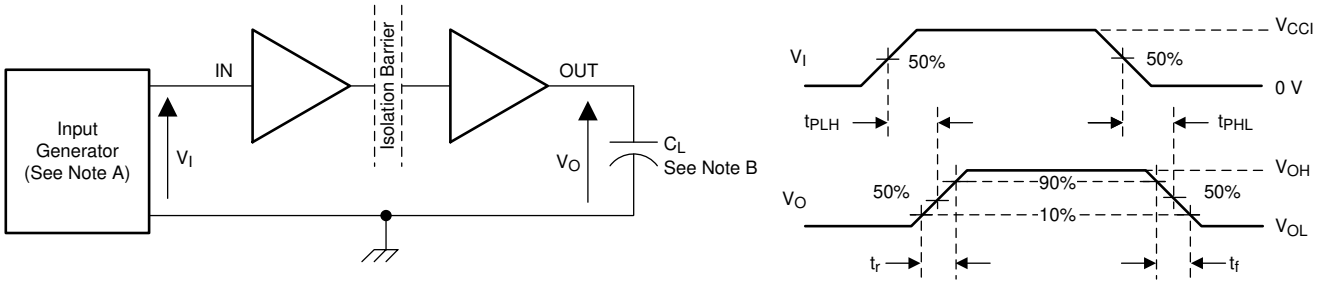



$T_A$ = 25°C $C_L$ = 15 pF

**図 6-6. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With 15-pF Load)**

Copyright © 2022 Texas Instruments Incorporated

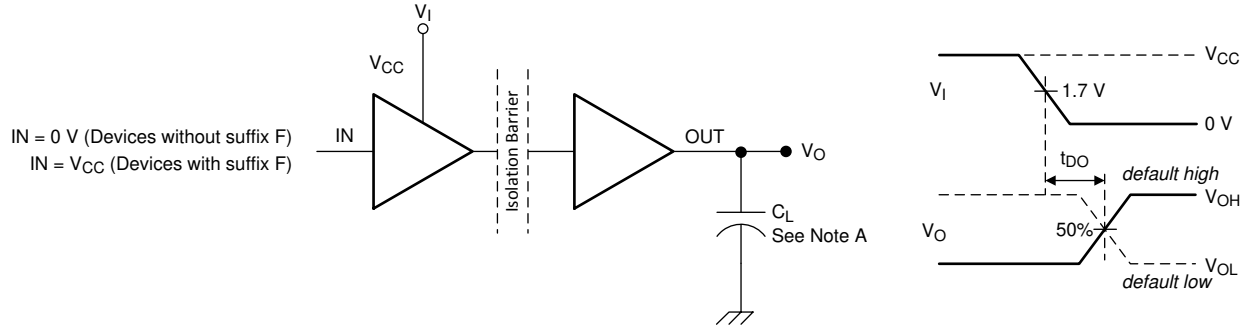
# 7 Parameter Measurement Information




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3ns, $Z_O$ = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

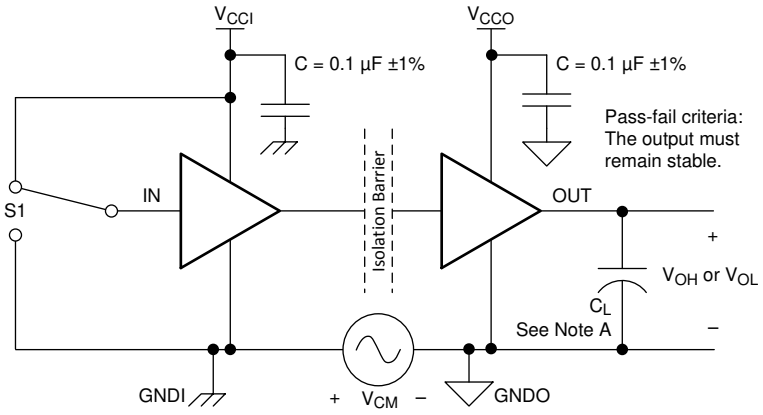
**図 7-1. Switching Characteristics Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

**図 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**図 7-3. Common-Mode Transient Immunity Test Circuit**


Copyright © 2022 Texas Instruments Incorporated

# 8 Detailed Description

## 8.1 Overview

The ISO7041-Q1 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Conceptual Block Diagram of a Digital Capacitive Isolator, shows a functional block diagram of a typical channel.

## 8.2 Functional Block Diagram

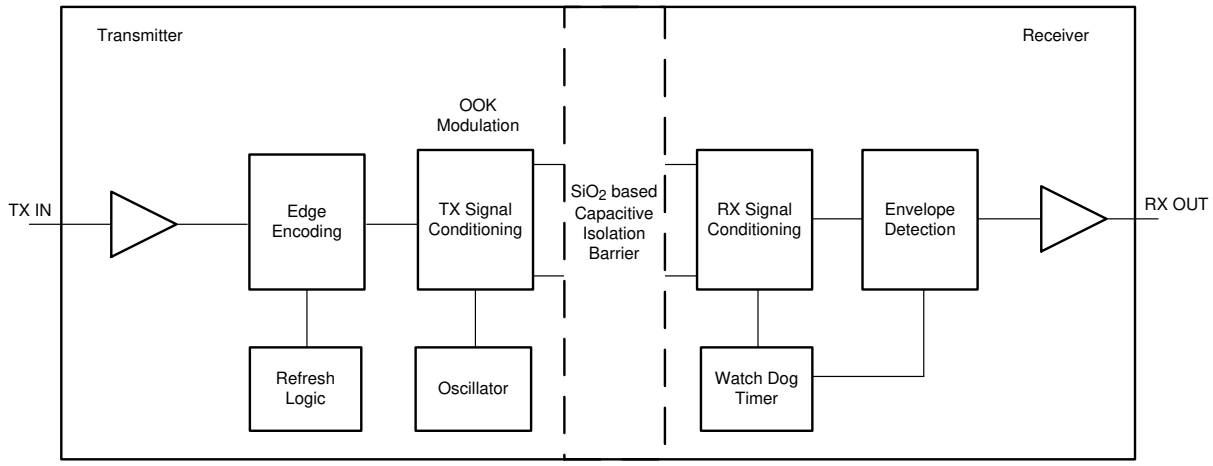



**図 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

## 8.3 Feature Description

### 8.3.1 Refresh

The ISO7041 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. The built in refresh function consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 µs. This ensures that the input and output state of the isolator always match.

### 8.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.

Copyright © 2022 Texas Instruments Incorporated

- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.


Copyright © 2022 Texas Instruments Incorporated

## 8.4 Device Functional Modes

表 8-1 shows the functional modes for the device.

**表 8-1. Function Table**

| $V_{CCI}$ (1) | $V_{CCO}$ | INPUT (INx) | REFRESH ENABLE (ENx) | OUTPUT (OUTx) | COMMENTS |
|---|---|---|---|---|---|
| PU | PU | H | L | H | Normal Operation:<br>A channel output assumes the logic state of its input. |
| | | L | L | L | |
| | | X | H | Undetermined | The device needs an input signal transition to validate the output tracks the input state. Without a signal edge transition, the output will be in an undetermined state. |
| PD | PU | X | L | Default | When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| | | | H | Undetermined | When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the previous state of the output before $V_{CCI}$ powered down. |
| X | PD | X | L | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined.(2)<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. |
| | | | H | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined.(2)<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the selected default option. |
| X | X | X | Open | Undetermined | When ENx is unconnected or open, the device output will be in an undetermined and unknown state. ENx must be connected high or low for the device to behave correctly. |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$; PU = Powered up ($V_{CC}$ ≥ 1.54 V); PD = Powered down ($V_{CC}$ ≤ 1.54); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance.

(2) A strongly driven input signal can weakly power the floating $V_{CC}$ through an internal protection diode and cause undetermined output.

Copyright © 2022 Texas Instruments Incorporated

### 8.4.1 Device I/O Schematics

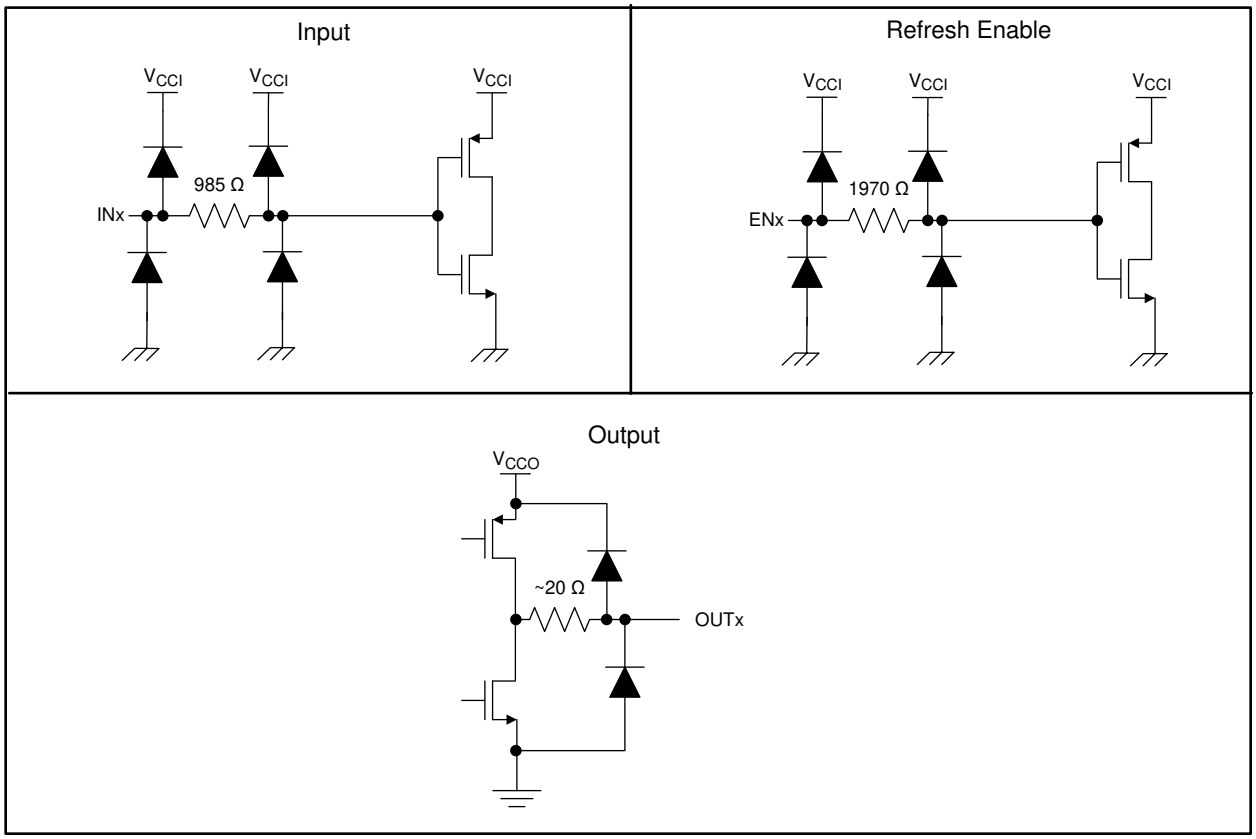



**図 8-2. Device I/O Schematics**


Copyright © 2022 Texas Instruments Incorporated

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO7041-Q1 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 3.0 V to 5.5 V for both supplies, $V_{CC1}$ and $V_{CC2}$, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See *Isolated power and data interface for low-power applications reference design* TI Design for detailed information on designing the ISO70xx in low-power applications.

### 9.1.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see 図 9-1 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

図 9-2 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

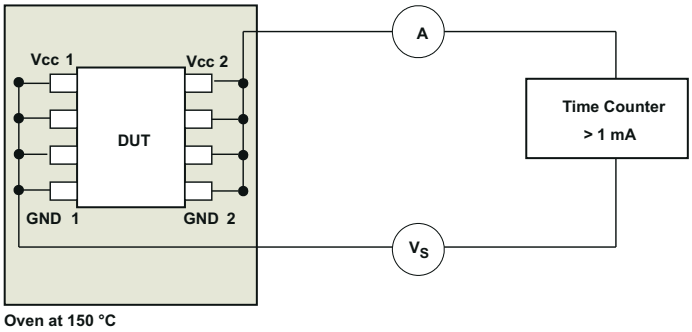



**図 9-1. Test Setup for Insulation Lifetime Measurement**

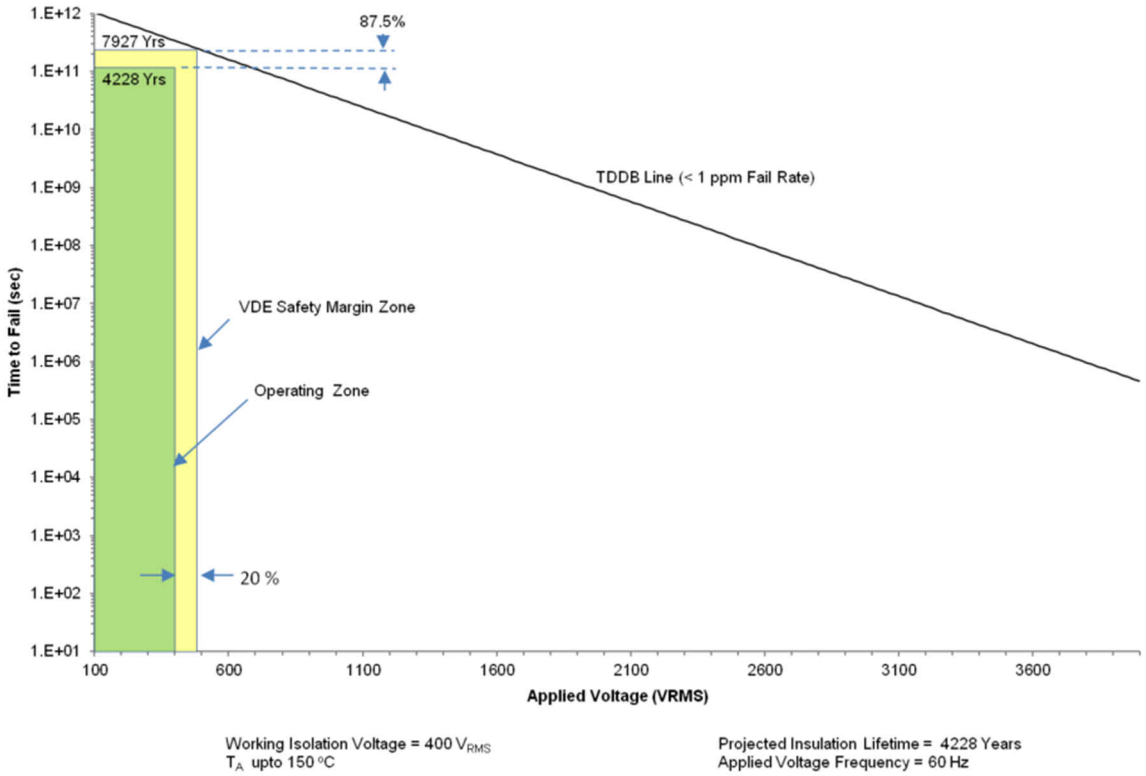



**図 9-2. Insulation Lifetime Projection Data**

## 9.2 Typical Application

Isolated UART for an Automotive Battery Management System shows the isolated UART and GPIO (NFAULT) interface.


Copyright © 2022 Texas Instruments Incorporated

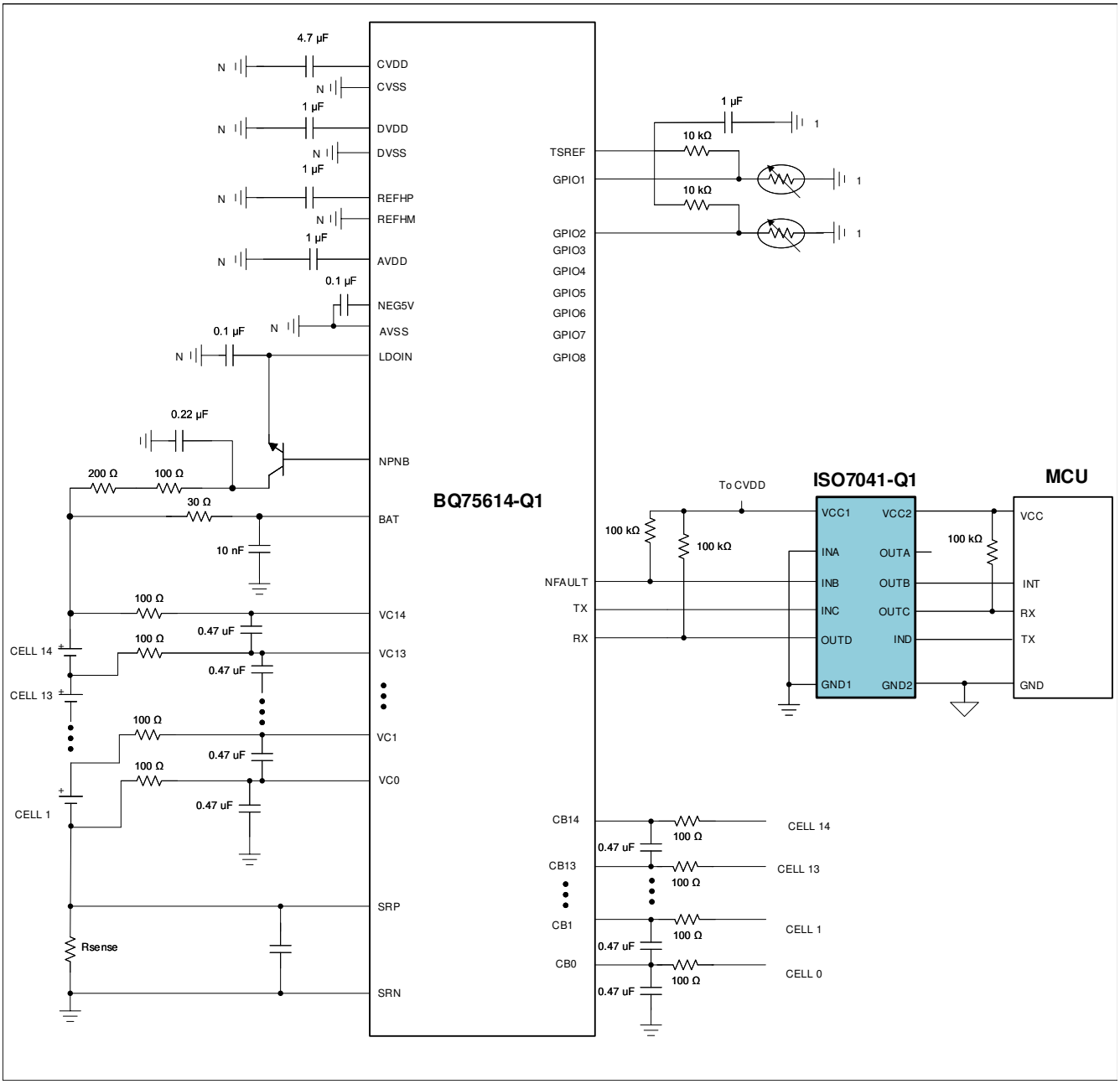



**図 9-3. Isolated UART for an Automotive Battery Management System**

### 9.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 9-1.

**表 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$ | 3.0 V to 5.5 V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1 µF |

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

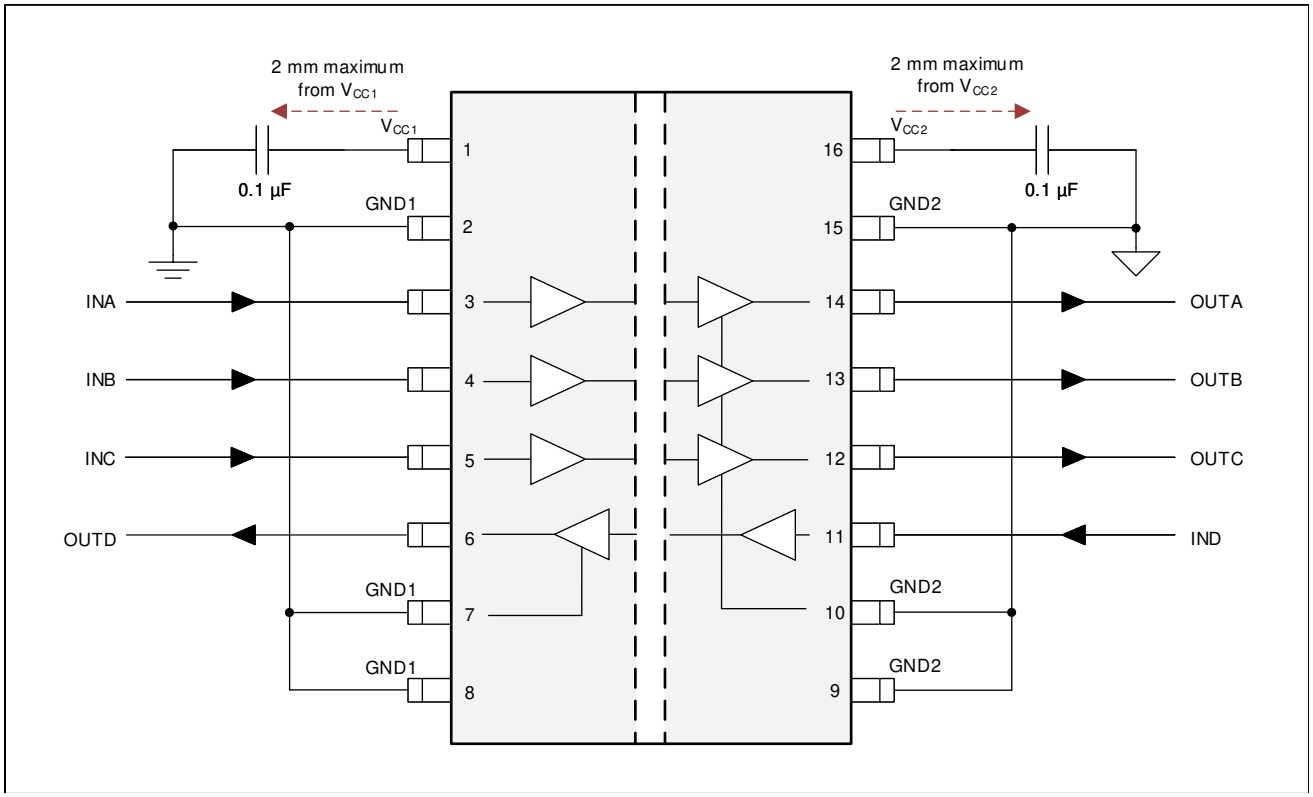



**図 9-4. Typical ISO7041-Q1 Circuit Hook-up**


Copyright © 2022 Texas Instruments Incorporated

### 9.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 4 Mbps.

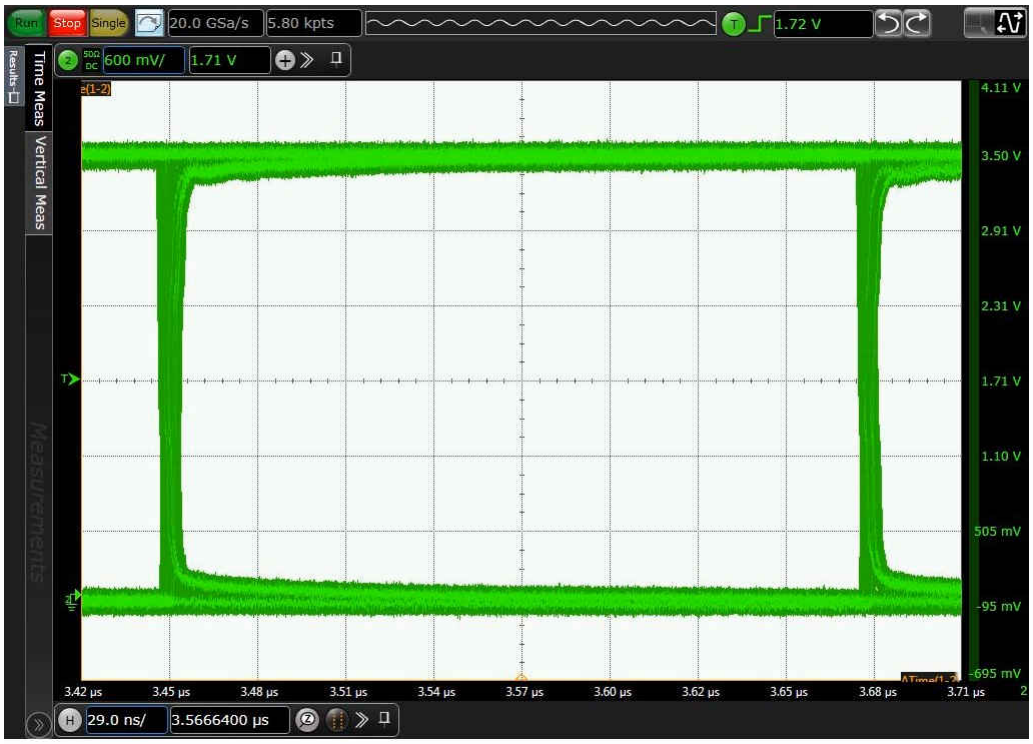



**図 9-5. Eye Diagram at 4 Mbps PRBS $2^{16}$ – 1, 3.3 V and 25°C**

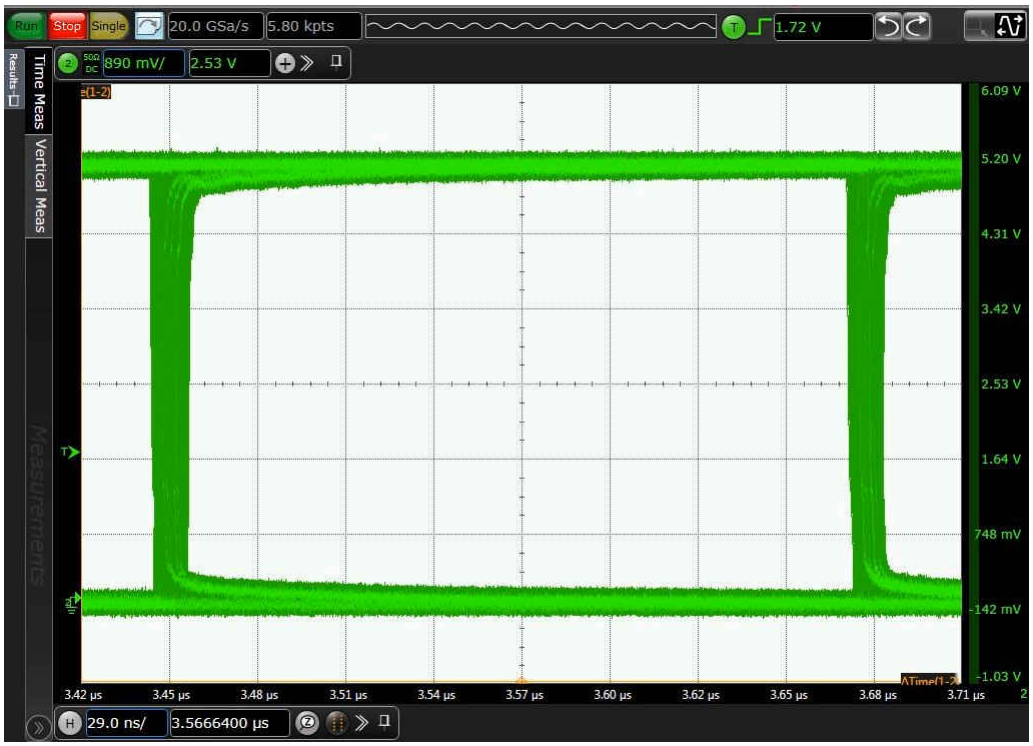



**図 9-6. Eye Diagram at 4 Mbps PRBS $2^{16}$ – 1, 5 V and 25°C**

Copyright © 2022 Texas Instruments Incorporated

## 10 Power Supply Recommendations

Put a 0.1-µF bypass capacitor at the input and output supply pins ($V_{CC1}$ and $V_{CC2}$) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.


Copyright © 2022 Texas Instruments Incorporated

# 11 Layout

## 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations,.

### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 11.2 Layout Example

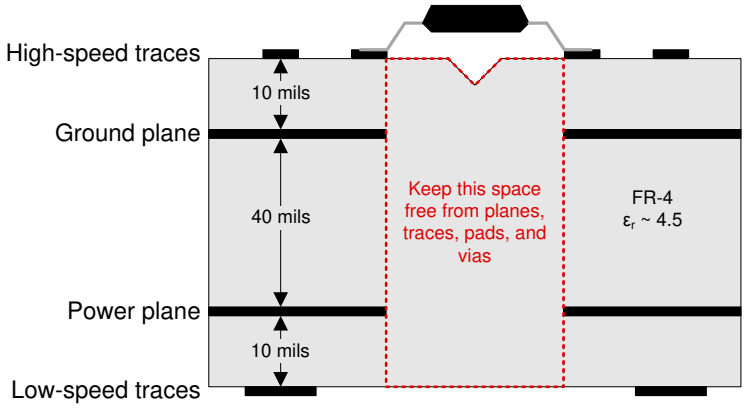



**図 11-1. Recommended Layer Stack**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments,*BQ75614-Q1, 14-S automotive precision battery monitor, balancer and integrated protector with ASIL-D compliance*
- Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications* TI Design
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated power and data interface for low-power applications reference design* TI Design

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2022 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ISO7041FQDBQRQ1 | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7041F |
| ISO7041FQDBQRQ1.B | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7041F |
| ISO7041QDBQRQ1 | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7041 |
| ISO7041QDBQRQ1.B | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7041 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

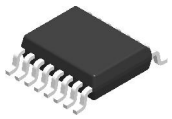
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7041-Q1 :**

- Catalog : ISO7041

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

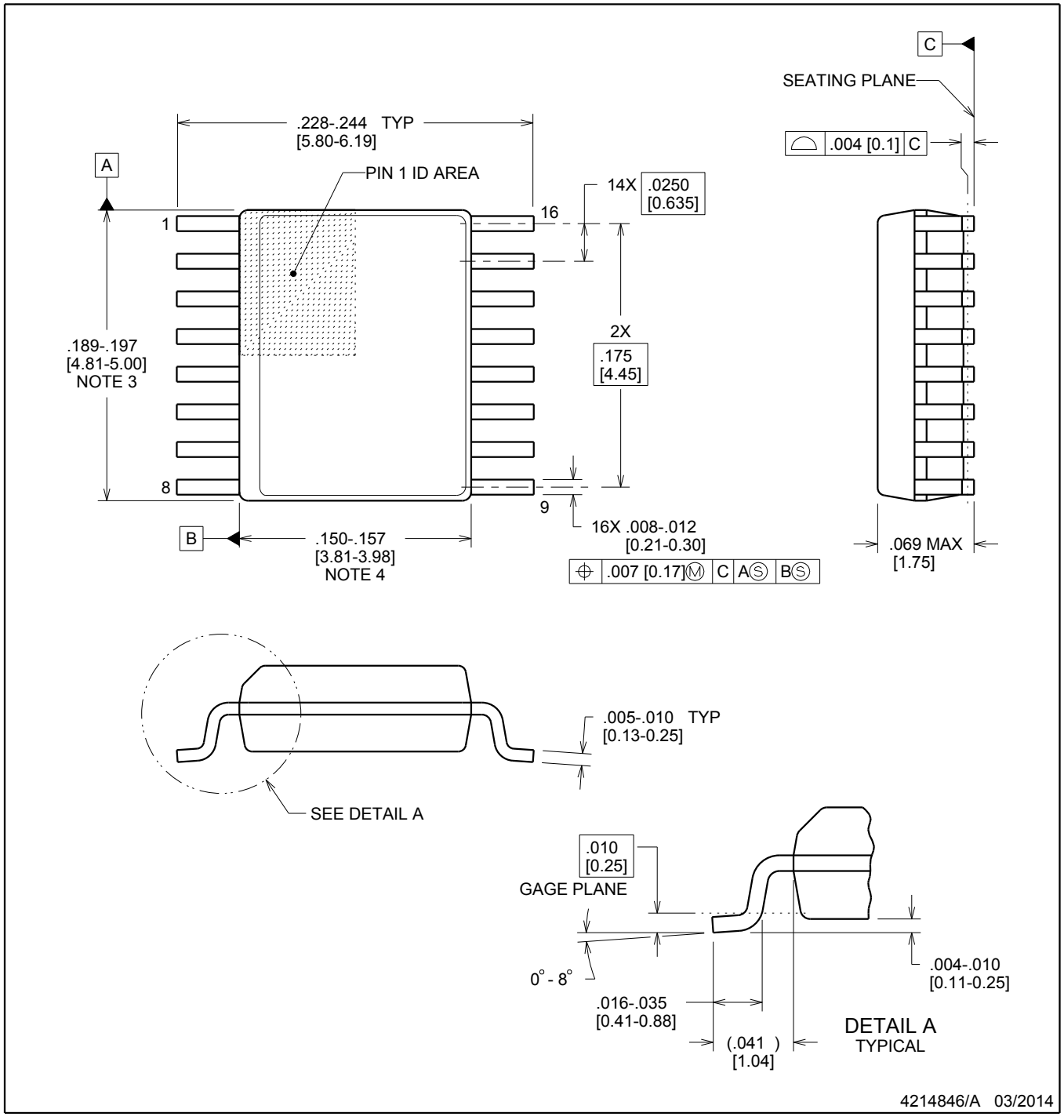


# PACKAGE OUTLINE

## DBQ0016A

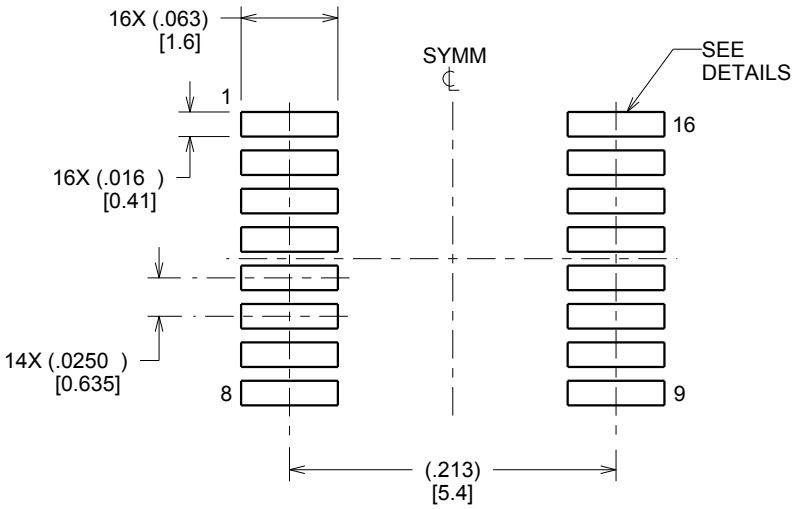
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

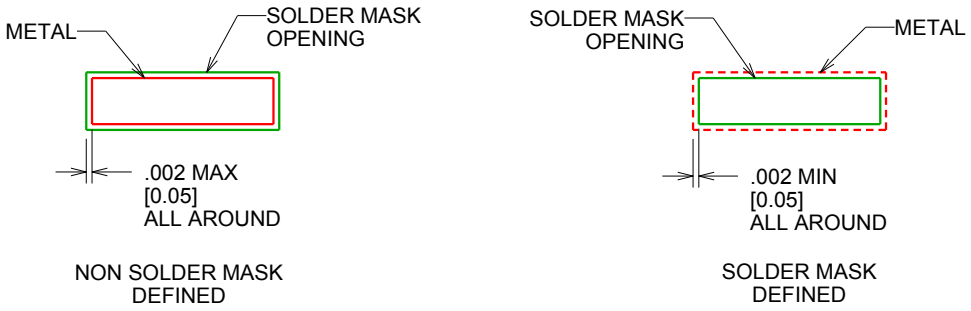



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

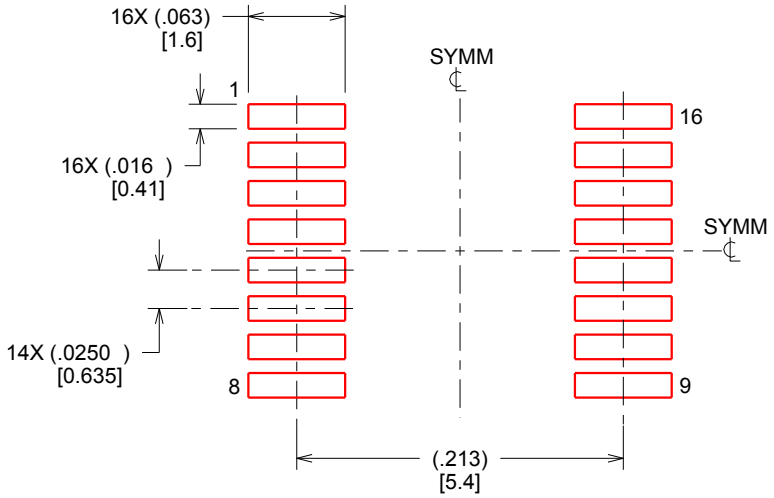
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated