# LM34926 Integrated Secondary-Side Bias Regulator for Isolated DC-DC Converters

## 1 Features

- Wide 7.5-V to 100-V Input Range
- Integrated 300-mA High-Side and Low-Side Switches
- No Schottky Required
- Constant On-Time Control
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Nearly Constant Operating Frequency
- Intelligent Peak Current Limit
- Adjustable Output Voltage From 1.225 V
- Precision 2% Feedback Reference
- Frequency Adjustable to 1 MHz
- Adjustable Undervoltage Lockout (UVLO)
- Remote Shutdown
- Thermal Shutdown
- Packages:
  - WSON-8
  - SO PowerPAD™-8 Packages
- Create a Custom Design Using the LM34926 With the WEBENCH® Power Designer

## 2 Applications

- Isolated Telecom Bias Supply
- Isolated Automotive and Industrial Electronics

## 3 Description

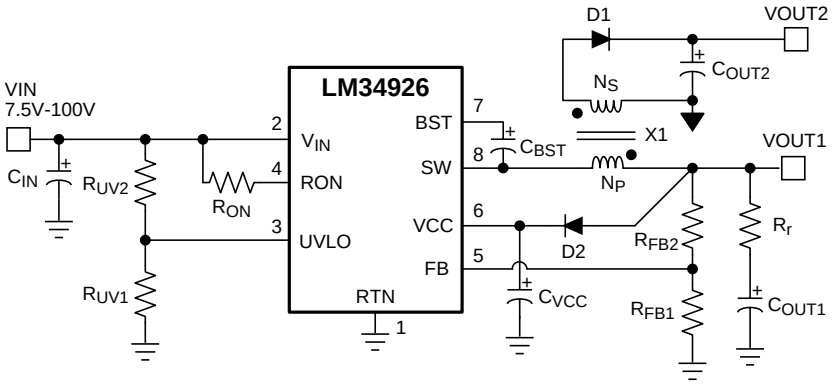
The LM34926 regulator features all of the functions needed to implement a low-cost, efficient, isolated bias regulator. This high-voltage regulator contains two 100-V N-channel MOSFET switches — a high-side buck switch and a low-side synchronous switch. The constant on-time (COT) control scheme employed in the LM34926 requires no loop compensation and provides excellent transient response. The regulator operates with an on-time control that is inversely proportional to the input voltage. This feature allows the operating frequency to remain relatively constant. An intelligent peak current limit is implemented with integrated sense circuit. Other features include a programmable input undervoltage comparator to inhibit operation during low-voltage conditions. Protection features include thermal shutdown and $V_{CC}$ Undervoltage Lockout (UVLO). The LM34926 device is offered in WSON-8 and SO PowerPAD-8 plastic packages.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM34926 | HSOP (8) | 4.89 mm × 3.90 mm |
| | WSON (8) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Revision History

**Changes from Revision E (December 2014) to Revision F** **Page**

- Added WEBENCH links to the data sheet ... 1
- Deleted lead temperature from the *Absolute Maximum Ratings* table ... 5
- Changed $T_{ON}$ *vs* $V_{IN}$ *and* $R_{ON}$ in *Typical Characteristics* ... 7
- Changed 14 V to 13 V in $V_{CC}$ *Regulator* section ... 11
- Added *Receiving Notification of Documentation Updates* section ... 22

**Changes from Revision D (December 2013) to Revision E** **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Switching Characteristics* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- CMS Request No.: C1411181 ... 1
- Changed *Thermal Information* table ... 5
- Changed *Control Overview* section ... 10
- Changed *Soft-Start Circuit*, *Isolated Fly-Buck Converter* graphics. ... 14
- Deleted *Lowest Part Count Isolated Application Schematic* ... 20

**Changes from Revision C (December 2013) to Revision D** **Page**

- Added Thermal Parameters ... 5


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**Changes from Revision B (March 2013) to Revision C** **Page**

- Changed formatting to the TI standard ..... 1
- Changed minimum operating input voltage from 9 V to 7.5 V in *Features*, *Typical Application*, *Pin Descriptions*, *Recommended Operating Ratings* ..... 1
- Added Absolute Maximum Junction Temperature ..... 5

**Changes from Revision A (March 2013) to Revision B** **Page**

- Added SW to RTN (100 ns transient) in *Absolute Maximum Ratings* ..... 5

**Changes from Original (March 2013) to Revision A** **Page**

- Changed layout of National Data Sheet to the TI standards ..... 21

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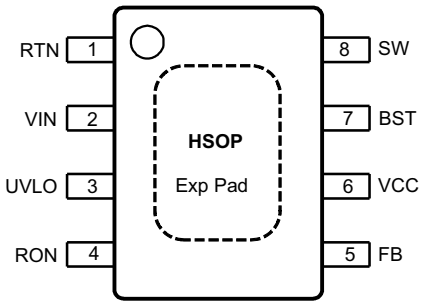
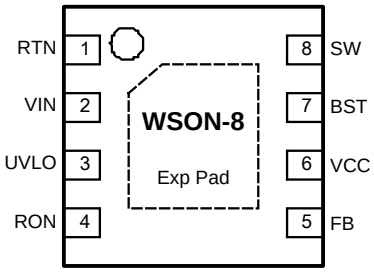
# 5 Pin Configuration and Functions

**DDA Package**
**8-Pin HSOP**
**Top View**




**NGU Package**
**8-Pin WSON**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION | APPLICATION INFORMATION |
|---|---|---|---|---|
| NO. | NAME | | | |
| 1 | RTN | – | Ground | Ground connection of the integrated circuit. |
| 2 | VIN | I | Input Voltage | Operating input range is 7.5 V to 100 V. |
| 3 | UVLO | I | Input Pin of Undervoltage Comparator | Resistor divider from $V_{IN}$ to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When UVLO pin is pulled below 0.66 V externally, the parts goes in shutdown mode. |
| 4 | RON | I | On-Time Control | A resistor between this pin and $V_{IN}$ sets the switch on-time as a function of $V_{IN}$. Minimum recommended on-time is 100 ns at max input voltage. |
| 5 | FB | I | Feedback | This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V. |
| 6 | VCC | O | Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V. | The internal $V_{CC}$ regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0-µF decoupling capacitor is recommended. |
| 7 | BST | I | Bootstrap Capacitor | An external capacitor is required between the BST and SW pins (0.01-µF ceramic). The BST pin capacitor is charged by the $V_{CC}$ regulator through an internal diode when the SW pin is low. |
| 8 | SW | O | Switching Node | Power switching node. Connect to the output inductor and bootstrap capacitor. |
| – | EP | – | Exposed Pad | Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance. |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# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$, UVLO to RTN | –0.3 | 100 | V |
| SW to RTN | –1.5 | $V_{IN}$ + 0.3 | V |
| SW to RTN (100-ns transient) | –5 | $V_{IN}$ + 0.3 | V |
| BST to VCC | | 100 | V |
| BST to SW | | 13 | V |
| RON to RTN | –0.3 | 100 | V |
| VCC to RTN | –0.3 | 13 | V |
| FB to RTN | –0.3 | 5 | V |
| Maximum junction temperature(3) | | 150 | °C |
| Storage temperature, $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The RTN pin is the GND reference electrically connected to the substrate.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Ratings

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$ voltage | 7.5 | 100 | V |
| Operating junction temperature(1) | –40 | 125 | °C |

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

## 6.4 Thermal Information

| THERMAL METRICS(1) | | LM34926 | | UNIT |
|---|---|---|---|---|
| | | NGU (WSON) | DDA (SO PowerPAD) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 41.3 | 41.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.2 | 2.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characteristic parameter | 19.2 | 24.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 19.1 | 30.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 34.7 | 37.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characteristic parameter | 0.3 | 6.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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## 6.5 Electrical Characteristics

Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. $V_{IN}$ = 48 V unless stated otherwise. See(1).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **$V_{CC}$ SUPPLY** | | | | | | |
| $V_{CC}$ Reg | $V_{CC}$ Regulator Output | $V_{IN}$ = 48 V, $I_{CC}$ = 20 mA | 6.25 | 7.6 | 8.55 | V |
| | $V_{CC}$ Current Limit | $V_{IN}$ = 48 V(2) | 26 | | | mA |
| | $V_{CC}$ UVLO Threshold ($V_{CC}$ increasing) | | 4.15 | 4.5 | 4.9 | V |
| | $V_{CC}$ UVLO Hysteresis | | | 300 | | mV |
| | $V_{CC}$ Drop Out Voltage | $V_{IN}$ = 8 V, $I_{CC}$ = 20 mA | | 2.3 | | V |
| | $I_{IN}$ Operating Current | Nonswitching, FB = 3 V | | 1.75 | | mA |
| | $I_{IN}$ Shutdown Current | UVLO = 0 V | | 50 | 225 | µA |
| **UNDERVOLTAGE SENSING FUNCTION** | | | | | | |
| | UV Threshold | UV Rising | 1.19 | 1.225 | 1.26 | V |
| | UV Hysteresis Input Current | UV = 2.5 V | –10 | –20 | -29 | µA |
| | Remote Shutdown Threshold | Voltage at UVLO Falling | 0.32 | 0.66 | | V |
| | Remote Shutdown Hysteresis | | | 110 | | mV |
| **REGULATION AND OVERVOLTAGE COMPARATORS** | | | | | | |
| | FB Regulation Level | Internal Reference Trip Point for Switch ON | 1.2 | 1.225 | 1.25 | V |
| | FB Overvoltage Threshold | Trip Point for Switch OFF | | 1.62 | | V |
| | FB Bias Current | | | 60 | | nA |
| **SWITCH CHARACTERISTICS** | | | | | | |
| | Buck Switch $R_{DS(ON)}$ | $I_{TEST}$ = 200 mA, BST-SW = 7 V | | 0.8 | 1.8 | Ω |
| | Synchronous $R_{DS(ON)}$ | $I_{TEST}$ = 200 mA | | 0.45 | 1 | Ω |
| | Gate Drive UVLO | $V_{BST}$ – $V_{SW}$ Rising | 2.4 | 3 | 3.6 | V |
| | Gate Drive UVLO Hysteresis | | | 260 | | mV |
| **CURRENT LIMIT** | | | | | | |
| | Current Limit Threshold | | 390 | 575 | 750 | mA |
| | Current Limit Response Time | Time to Switch Off | | 150 | | ns |
| | OFF-Time Generator (Test 1) | FB = 0.1 V, $V_{IN}$ = 48 V | | 12 | | µs |
| | OFF-Time Generator (Test 2) | FB = 1.0 V, $V_{IN}$ = 48 V | | 2.5 | | µs |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{sd}$ | Thermal Shutdown Temperature | | | 165 | | °C |
| | Thermal Shutdown Hysteresis | | | 20 | | °C |

(1) All limits are specified by design. All electrical characteristics having room temperature limits are tested during production at $T_A$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) $V_{CC}$ provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

## 6.6 Switching Characteristics

Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. $V_{IN}$ = 48 V unless otherwise stated.

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **ON-TIME GENERATOR** | | | | | |
| $T_{ON}$ Test 1 | $V_{IN}$ = 32 V, $R_{ON}$ = 100 kΩ | 270 | 350 | 460 | ns |
| $T_{ON}$ Test 2 | $V_{IN}$ = 48 V, $R_{ON}$ = 100 kΩ | 188 | 250 | 336 | ns |
| $T_{ON}$ Test 3 | $V_{IN}$ = 75 V, $R_{ON}$ = 250 kΩ | 250 | 370 | 500 | ns |
| $T_{ON}$ Test 4 | $V_{IN}$ = 10 V, $R_{ON}$ = 250 kΩ | 1880 | 3200 | 4425 | ns |
| **MINIMUM OFF-TIME** | | | | | |
| Minimum Off-Timer | FB = 0 V | | 144 | | ns |


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## 6.7 Typical Characteristics

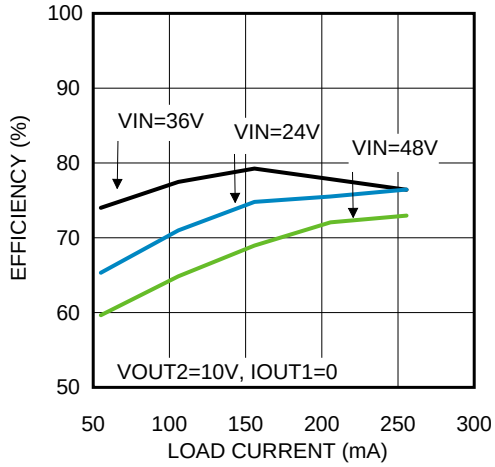


**Figure 1. Efficiency at 750 kHz, $V_{OUT1}$ = 10 V**

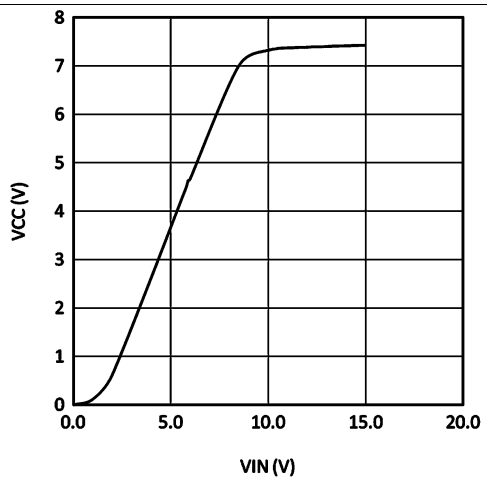


**Figure 2. $V_{CC}$ vs $V_{IN}$**

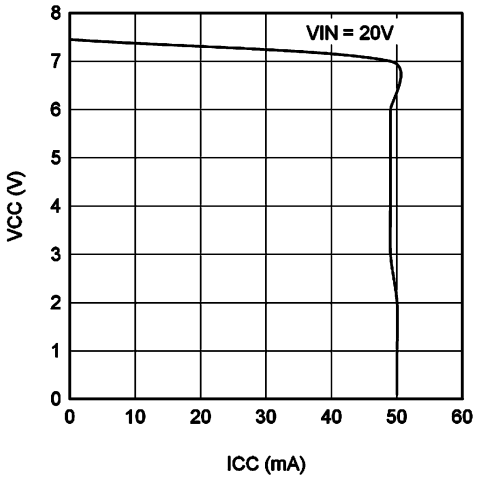


**Figure 3. $V_{CC}$ vs $I_{CC}$**

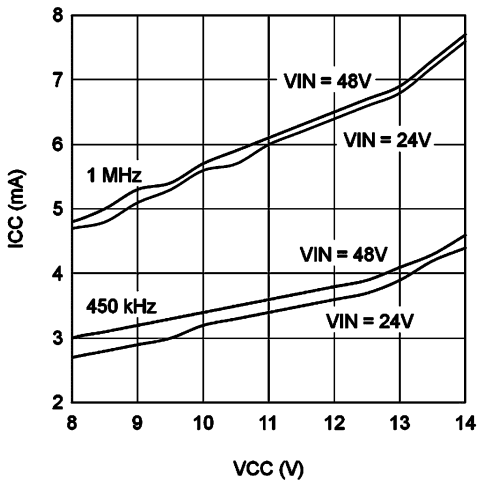


**Figure 4. $I_{CC}$ vs External $V_{CC}$**

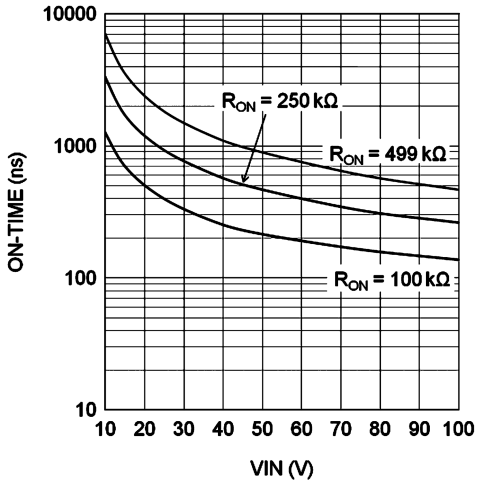


**Figure 5. $T_{ON}$ vs $V_{IN}$ and $R_{ON}$**

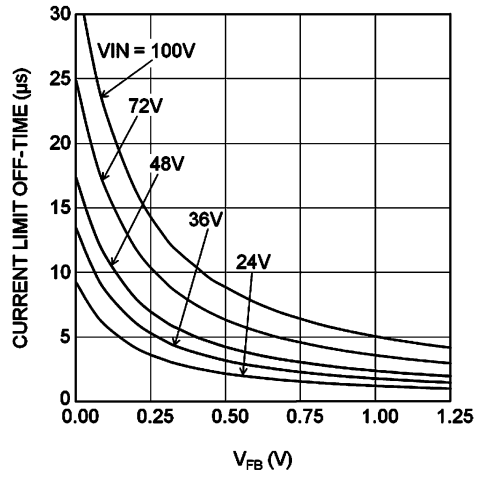


**Figure 6. $T_{OFF}$ ($I_{LIM}$) vs $V_{FB}$ and $V_{IN}$**

## Typical Characteristics (continued)

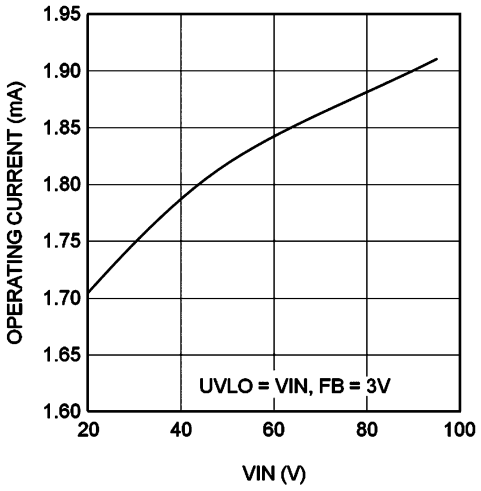


Figure 7. $I_{IN}$ vs $V_{IN}$ (Operating, Non-Switching)

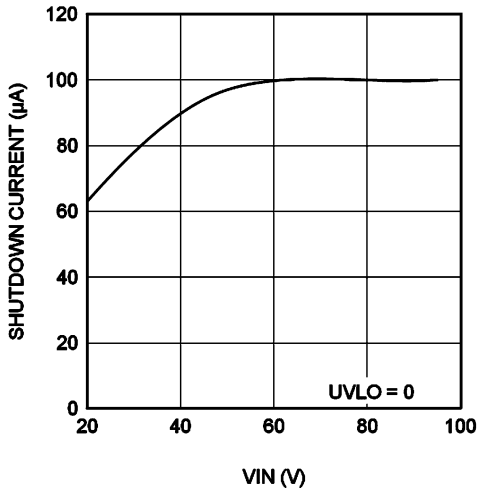


Figure 8. $I_{IN}$ vs $V_{IN}$ (Shutdown)


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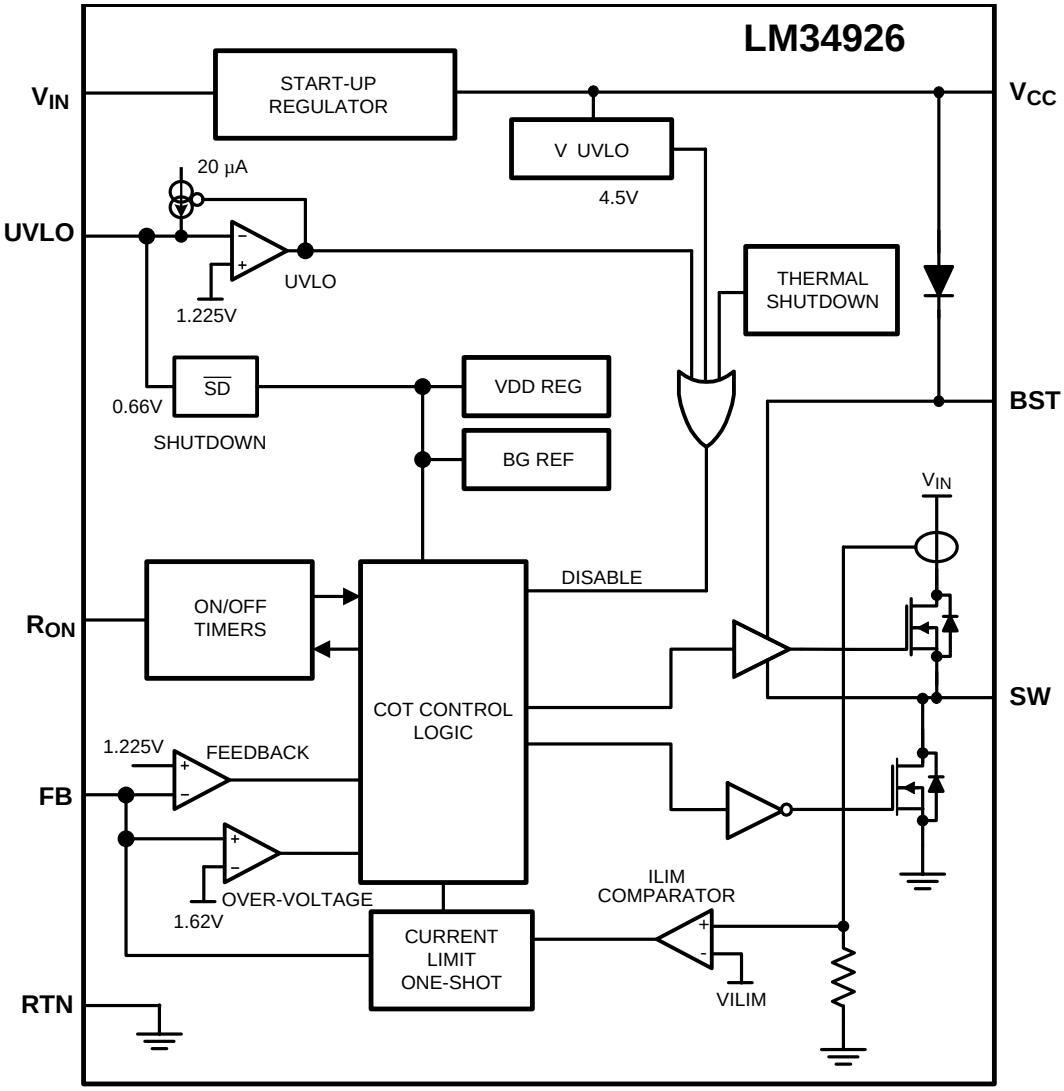
# 7 Detailed Description

## 7.1 Overview

The LM34926 step-down switching regulator features all the functions needed to implement a low-cost, efficient, isolated bias supply. This high-voltage regulator contains 100-V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to $V_{IN}$. This control scheme does not require loop compensation. Current limit is implemented with forced off-time inversely proportional to $V_{OUT}$. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM34926 device is shown in *Functional Block Diagram*.

The LM34926 device can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48-V telecom and automotive power bus ranges. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Control Overview

The LM34926 regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference the internal buck switch is switched on for the one-shot timer period, which is a function of the input voltage and the programming resistor (RT). Following the on-time the switch remains off until the FB voltage falls below the reference, and the forced minimum off-time has expired. When the FB pin voltage falls below the reference and the off-time one-shot period expires, the buck switch is then turned on for another on-time one-shot period. This continues until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typical).

In a synchronous buck converter, the low-side (sync) FET is on when the high-side (buck) FET is off. The inductor current ramps up when the high-side switch is on and ramps down when the high-side switch is off. There is no diode emulation feature in this IC, and therefore, the inductor current may ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be determined from Equation 1.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}}$$

where

$$K = 9 \times 10^{-11} \quad (1)$$

The output voltage ($V_{OUT}$) is set by two external resistors ($R_{FB1}$, $R_{FB2}$). The regulated output voltage is determined from Equation 2.

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \quad (2)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor ($C_{OUT}$). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM34926 device. In cases where the capacitor ESR is too small, additional series resistance may be required ($R_C$ in Figure 9).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 9. However, $R_C$ slightly degrades the load regulation.

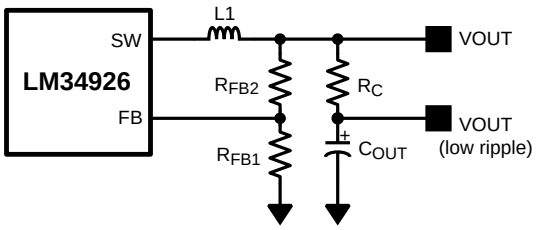



**Figure 9. Low Ripple Output Configuration**

### 7.3.2 $V_{CC}$ Regulator

The LM34926 device contains an internal high-voltage linear regulator with a nominal output of 7.6 V. The input pin ($V_{IN}$) can be connected directly to the line voltages up to 100 V. The $V_{CC}$ regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at $V_{CC}$. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the $V_{CC}$ pin reaches the UVLO threshold of 4.5 V, the IC is enabled.

The $V_{CC}$ regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when the SW pin is low.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## Feature Description (continued)

At high input voltages, the power dissipated in the high-voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the $V_{CC}$ regulator may supply up to 7 mA of current resulting in 48 V × 7 mA = 336 mW of power dissipation. If the $V_{CC}$ voltage is driven externally by an alternate voltage source, from 8.55 V to 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

### 7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225 V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high-side switch stays on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high-side switch stays off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage is below 1.225 V at the end of each on-time, causing the high-side switch to turn on immediately after the minimum forced off-time of 144 ns. The high-side switch can be turned off before the on-time is complete if peak current in the inductor reaches the current limit threshold.

### 7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62 V reference. If the voltage at FB rises above 1.62-V the on-time pulse is immediately terminated. This condition can occur if the input voltage and/or the output load changes suddenly. The high-side switch will not turn on again until the voltage at FB falls below 1.225 V.

### 7.3.5 On-Time Generator

The on-time for the LM34926 device is determined by the $R_{ON}$ resistor, and is inversely proportional to the input voltage ($V_{IN}$), resulting in a nearly constant frequency as $V_{IN}$ is varied over its range. The on-time equation for the LM34926 is determined be Equation 3.

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \tag{3}$$

See Figure 5. $R_{ON}$ should be selected for a minimum on-time (at maximum $V_{IN}$) greater than 100 ns, for proper operation. This requirement limits the maximum frequency for each application.

### 7.3.6 Current Limit

The LM34926 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds 575 mA, the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage $V_{IN}$. As an example, when FB = 0 V and $V_{IN}$ = 48 V, a maximum off-time is set to 16 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from Equation 4.

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2\ V}\ \mu s \tag{4}$$

The current limit protection feature is peak limited, the maximum average output will be less than the peak.

### 7.3.7 N-Channel Buck Switch and Driver

The LM34926 device integrates an N-channel buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.01-uF ceramic capacitor connected between the BST and SW pins provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from $V_{CC}$ through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

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## Feature Description (continued)

### 7.3.8 Synchronous Rectifier

The LM34926 device provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation. This feature specifically allows the user to design a secondary regulator using a transformer winding off the main inductor to generate the alternate regulated output voltage.

### 7.3.9 Undervoltage Detector

The LM34926 device contains a dual-level UVLO circuit. A summary of threshold voltages and operational states is provided in *Device Functional Modes*. When the UVLO pin voltage is below 0.66 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode the $V_{CC}$ bias regulator is active while the regulator output is disabled. When the $V_{CC}$ pin exceeds the $V_{CC}$ undervoltage thresholds and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from $V_{IN}$ to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance $R_{UV2}$.

If the UVLO pin is wired directly to the $V_{IN}$ pin, the regulator will begin operation once the $V_{CC}$ undervoltage is satisfied.

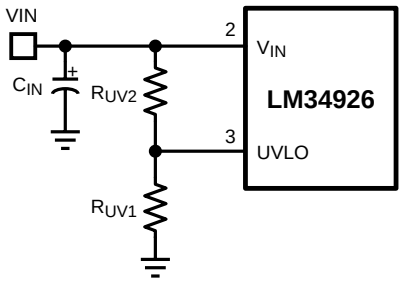


**Figure 10. UVLO Resistor Setting**

### 7.3.10 Thermal Protection

The LM34926 device should be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM34926 device in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the buck switch and the $V_{CC}$ regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature falls below 145°C (typical hysteresis = 20°C), the $V_{CC}$ regulator is enabled, and normal operation is resumed.

### 7.3.11 Ripple Configuration

LM34926 uses constant on-time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage ($V_{FB}$) falling below the reference voltage ($V_{REF}$). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore this change in feedback voltage ($\Delta V_{FB}$) during off-time must be large enough to suppress any noise component present at the feedback node.


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## Feature Description (continued)

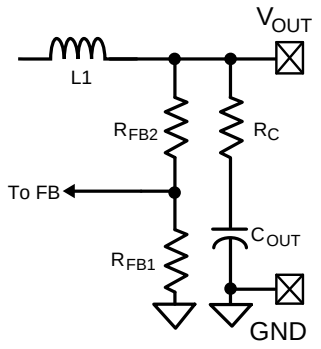
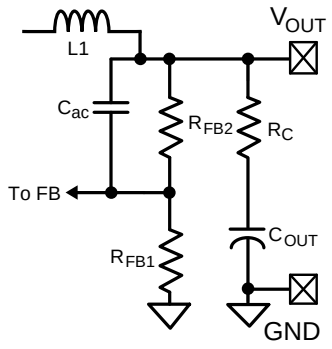
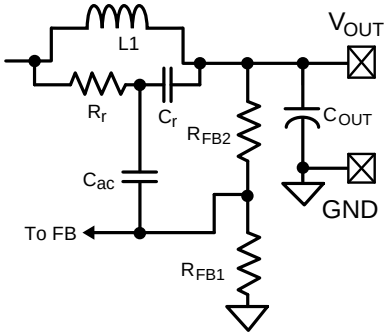
Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging and discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during off-time. The resistive ripple must exceed the capacitive ripple at the output node ($V_{OUT}$) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses $R_r$ and $C_r$ and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is AC-coupled using $C_{ac}$ to the feedback node (FB). Because this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details for each ripple generation method.

**Table 1. Ripple Configuration**

| TYPE 1<br>LOWEST COST CONFIGURATION | TYPE 2<br>REDUCED RIPPLE CONFIGURATION | TYPE 3<br>MINIMUM RIPPLE CONFIGURATION |
|---|---|---|
|  |  |  |
| $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ | $C \geq \frac{5}{f_{sw}(R_{FB2} \| R_{FB1})}$<br>$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$ | $C_r = 3300\ pF$<br>$C_{ac} = 100\ nF$<br>$R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$ |

### 7.3.12 Soft Start

A soft-start feature can be implemented with the LM34926 device using an external circuit. As shown in Figure 11, the soft-start circuit consists of one capacitor $C_1$, two resistors $R_1$ and $R_2$, and a diode D. During the initial start-up, the VCC voltage is established before the $V_{OUT}$ voltage. Capacitor $C_1$ is discharged and diode D is thereby forward biased to pull up the FB voltage. The FB voltage exceeds the reference voltage (1.225 V) and switching is therefore disabled. As capacitor $C_1$ charges, the voltage at node B gradually decreases and switching commences. $V_{OUT}$ will gradually rise to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above the FB voltage, the soft-start sequence is finished and D is reverse-biased.

During the initial part of the start-up, the FB voltage can be approximated as shown in Equation 5. The effect of $R_1$ has been ignored to simplify the calculation.

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (5)$$

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C1 is charged after the first start up. Diode D1 is optional and can be added to discharge C1 when the input voltage experiences a momentary drop to initialize the soft-start sequence.

To achieve the desired soft start, the following design guidance is recommended:

1. $R_2$ is selected so that $V_{FB}$ is higher than 1.225 V for a $V_{CC}$ of 4.5 V, but is lower than 5 V when $V_{CC}$ is 8.55 V. If an external $V_{CC}$ is used, $V_{FB}$ should not exceed 5 V at maximum $V_{CC}$.
2. $C_1$ is selected to achieve the desired start-up time which can be determined from .

$$t_S = C_1 \times \left(R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}}\right)$$

3. $R_1$ is used to maintain the node B voltage at zero after the soft start is finished. A value larger than the feedback resistor divider is preferred. The effect of resistor R1 is ignored.

Using the component values shown in Figure 12, selecting $C_1$ = 1 uF, $R_2$ = 1 kΩ, $R_1$ = 30 kΩ results in a soft-start time of about 2 ms.

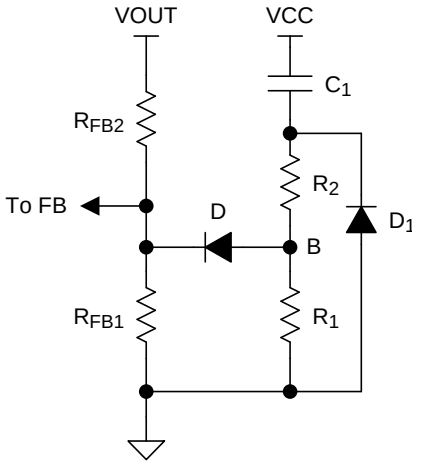


**Figure 11. Soft-Start Circuit**

## 7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM34926 device (see Table 2 for the detailed functional states).

**Table 2. UVLO Mode**

| UVLO | $V_{CC}$ | MODE | DESCRIPTION |
|---|---|---|---|
| < 0.66 V | Disabled | Shutdown | $V_{CC}$ regulator disabled.<br>Switching disabled. |
| 0.66 V — 1.225 V | Enabled | Standby | $V_{CC}$ regulator enabled.<br>Switching disabled. |
| > 1.225 V | $V_{CC}$ < 4.5 V | Standby | $V_{CC}$ regulator enabled.<br>Switching disabled. |
| | $V_{CC}$ > 4.5 V | Operating | $V_{CC}$ enabled.<br>Switching enabled. |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM34926 device is step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 300 mA. Use the following design procedure to select component values for the LM34926 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

## 8.2 Typical Application

Application Circuit: 20-V to 95-V Input and 10-V, 250-mA Output Isolated Fly-Buck™ Converter

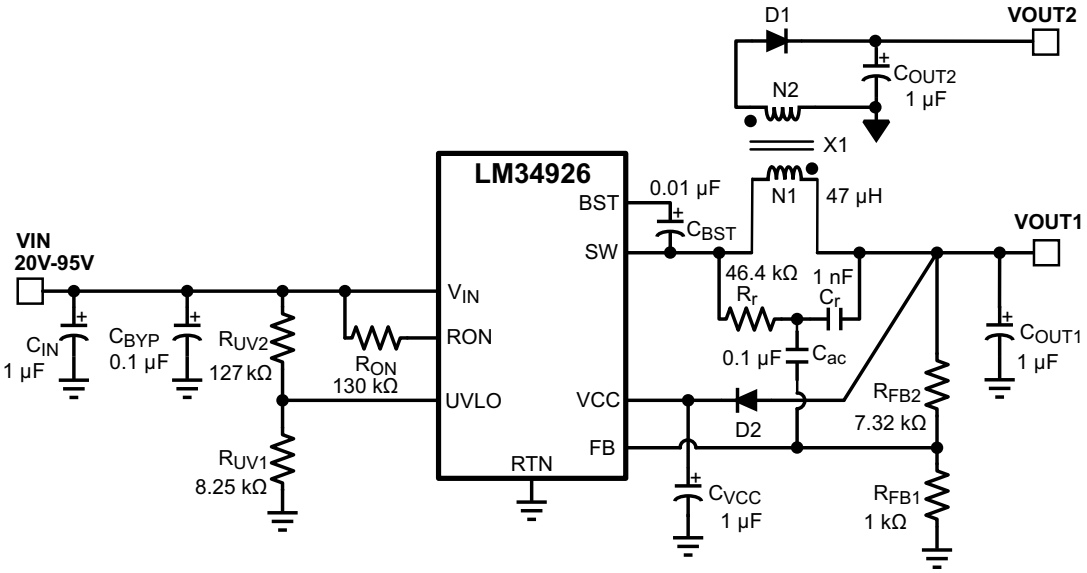


**Figure 12. Isolated Fly-Buck™ Converter Using LM34926**

### 8.2.1 Design Requirements

Selection of external components is illustrated through a design example. Table 3 lists the design example specifications.

**Table 3. Buck Converter Design Specifications**

| DESIGN PARAMETERS | VALUE |
|---|---|
| Input Voltage Range | 20 V to 95 V |
| Primary Output Voltage | 10 V |
| Secondary (Isolated) Output Voltage | 9.5 V |
| Maximum Output Current (Primary + Secondary) | 250 mA |
| Maximum Power Output | 2.5 W |
| Nominal Switching Frequency | 750 kHz |

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### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM34926 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.2.2 Transformer Turns Ratio

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary (isolated) output voltage. In this design example, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected. Therefore, N2 / N1 = 1.

If the secondary (isolated) output voltage is significantly higher or lower than the primary output voltage, a turns ratio less than or greater than 1 is recommended. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. This condition is satisfied if VOUT1 < $V_{IN_MIN}$ / 2

#### 8.2.2.3 Total IOUT

The total primary referred load current is calculated by multiplying the isolated output loads by the turns ratio of the transformer as shown in Equation 6.

$$I_{OUT(MAX)} = I_{OUT1} + I_{OUT2} \times \frac{N2}{N1} = 0.25\ A \tag{6}$$

#### 8.2.2.4 RFB1, RFB2

The feedback resistors are selected to set the primary output voltage. The selected value for $R_{FB1}$ is 1 kΩ. $R_{FB2}$ can be calculated using the following equations to set $V_{OUT1}$ to the specified value of 10 V. A standard resistor value of 7.32 kΩ is selected for $R_{FB2}$.

$$V_{OUT1} = 1.225V \times \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \tag{7}$$

$$\rightarrow R_{FB2} = \left(\frac{V_{OUT1}}{1.225} - 1\right) \times R_{FB1} = 7.16\ k\Omega \tag{8}$$

#### 8.2.2.5 Frequency Selection

Equation 1 is used to calculate the value of $R_{ON}$ required to achieve the desired switching frequency.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}}$$

where

$$K = 9 \times 10^{-11} \tag{9}$$

For $V_{OUT1}$ of 10 V and $f_{SW}$ of 750 kHz, the calculated value of $R_{ON}$ is 148 kΩ. A lower value of 130 kΩ is selected for this design to allow for second-order effects at high switching frequency that are not included in Equation 9.


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#### 8.2.2.6 Transformer Selection

A coupled inductor or a flyback-type transformer is required for this topology. Energy is transferred from primary to secondary when the low-side synchronous switch of the buck converter is conducting.

The maximum inductor primary ripple current that can be tolerated without exceeding the buck switch peak current limit threshold (0.39-A minimum) is given by Equation 10.

$$\Delta I_{L1} = \left(0.39\ A - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}\right) \times 2 = 0.28\ A \tag{10}$$

Using the maximum peak-to-peak inductor ripple current $\Delta I_{L1}$ from Equation 10, the minimum inductor value is given by Equation 11.

$$L1 = \frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L1} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 42.6\ \mu H \tag{11}$$

A higher value of 47 µH is selected to insure the high-side switch current does not exceed the minimum peak current limit threshold.

#### 8.2.2.7 Primary Output Capacitor

In a conventional buck converter the output ripple voltage is calculated as shown in Equation 12.

$$\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}} \tag{12}$$

To limit the primary output ripple voltage $\Delta V_{OUT1}$ to approximately 50 mV, an output capacitor $C_{OUT1}$ of 0.93 µF is required.

Figure 13 shows the primary winding current waveform (IL1) of a fly-buck converter. The reflected secondary winding current adds to the primary winding current during the buck switch off-time. Because of this increased current, the output voltage ripple is not the same as in conventional buck converter. The output capacitor value calculated in Equation 12 should be used as the starting point. Optimization of output capacitance over the entire line and load range must be done experimentally. If the majority of the load current is drawn from the secondary isolated output, a better approximation of the primary output voltage ripple is given by Equation 13.

$$\Delta V_{OUT1} = \frac{\left(I_{OUT2} \times \frac{N2}{N1}\right) \times T_{ON(MAX)}}{C_{OUT1}} \approx 0.16\ V \tag{13}$$

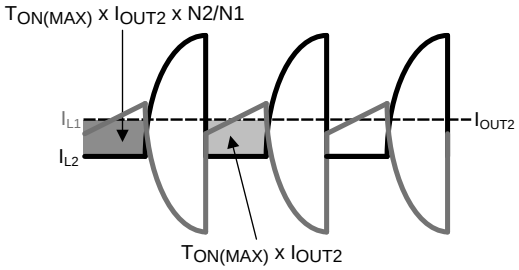


**Figure 13. Current Waveforms for $C_{OUT1}$ Ripple Calculation**

A standard 1-µF, 25-V capacitor is selected for this design. If lower output voltage ripple is required, a higher value should be selected for $C_{OUT1}$ and/or $C_{OUT2}$.

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### 8.2.2.8 Secondary Output Capacitor

A simplified waveform for secondary output current ($I_{OUT2}$) is shown in Figure 14.

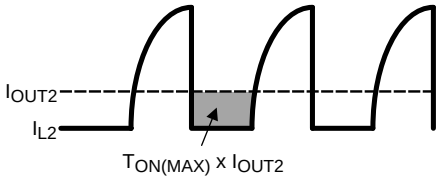


**Figure 14. Secondary Current Waveforms for $C_{OUT2}$ Ripple Calculation**

The secondary output current ($I_{OUT2}$) is sourced by $C_{OUT2}$ during on-time of the buck switch, $T_{ON}$. Ignoring the current transition times in the secondary winding, the secondary output capacitor ripple voltage can be calculated using Equation 14.

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON\,(MAX)}}{C_{OUT2}} \tag{14}$$

For a 1:1 transformer turns ratio, the primary and secondary voltage ripple equations are identical. Therefore, $C_{OUT2}$ is chosen to be equal to $C_{OUT1}$ (1 µF) to achieve comparable ripple voltages on primary and secondary outputs.

If lower output voltage ripple is required, a higher value should be selected for $C_{OUT1}$ and/or $C_{OUT2}$.

### 8.2.2.9 Type III Feedback Ripple Circuit

Type III ripple circuit as described in *Ripple Configuration* is required for the Fly-Buck topology. Type I and Type II ripple circuits use series resistance and the triangular inductor ripple current to generate ripple at $V_{OUT}$ and the FB pin. The primary ripple current of a Fly-Buck is the combination or primary and reflected secondary currents as shown in Figure 13. In the fly-buck topology, Type I and Type II ripple circuits suffer from large jitter as the reflected load current affects the feedback ripple.

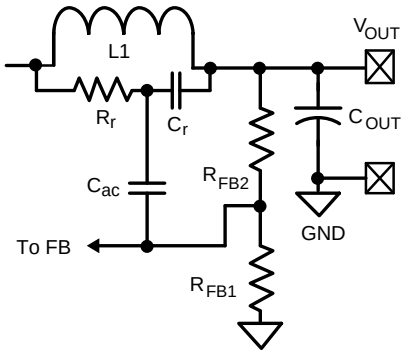


**Figure 15. Type III Ripple Circuit**

Selecting the Type III ripple components using the equations from *Ripple Configuration* ensures that the FB pin ripple is be greater than the capacitive ripple from the primary output capacitor $C_{OUT1}$. The feedback ripple component values are chosen as shown in Equation 15.

$C_r$ = 1000 pF

$C_{ac}$ = 0.1 µF

$$R_r C_r \le \frac{(V_{IN\,(MIN)} - V_{OUT}) \times T_{ON}}{50\ mV} \tag{15}$$

The calculated value for Rr is 66 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance should be selected to allow for variations in $T_{ON}$, $C_{OUT1}$ and other components. For this design, Rr value of 46.4 kΩ is selected.


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#### 8.2.2.10 Secondary Diode

The reverse voltage across secondary-rectifier diode D1 when the high-side buck switch is off can be calculated using Equation 16.

$$V_{D1} = \frac{N2}{N1} V_{IN} \tag{16}$$

For a $V_{IN_MAX}$ of 95 V and the 1:1 turns ratio of this design, a 100-V Schottky is selected.

#### 8.2.2.11 $V_{CC}$ and Bootstrap Capacitor

A 1-µF capacitor of 16-V or higher rating is recommended for the $V_{CC}$ regulator bypass capacitor.

A good value for the BST pin bootstrap capacitor is 0.01-µF with a 16-V or higher rating.

#### 8.2.2.12 Input Capacitor

The input capacitor is typically a combination of a smaller bypass capacitor located near the regulator IC and a larger bulk capacitor. The total input capacitance should be large enough to limit the input voltage ripple to a desired amplitude. For input ripple voltage $\Delta V_{IN}$, $C_{IN}$ can be calculated using Equation 17.

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f \times \Delta V_{IN}} \tag{17}$$

Choosing a $\Delta V_{IN}$ of 0.5 V gives a minimum $C_{IN}$ of 0.167 µF. A standard value of 0.1 µF is selected for $C_{BYP}$ in this design. A bulk capacitor of higher value reduces voltage spikes due to parasitic inductance between the power source to the converter. A standard value of 1 µF is selected for $C_{IN}$ in this design. The voltage ratings of the two input capacitors should be greater than the maximum input voltage under all conditions.

#### 8.2.2.13 UVLO Resistors

UVLO resistors $R_{UV1}$ and $R_{UV2}$ set the undervoltage lockout threshold and hysteresis according to Equation 18 and Equation 19.

$$V_{IN\ (HYS)} = I_{HYS} \times R_{UV2}$$

where

$I_{HYS}$ = 20 µA, typical (18)

$$V_{IN}(\text{UVLO, rising}) = 1.225\text{V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \tag{19}$$

For a UVLO hysteresis of 2.5 V and UVLO rising threshold of 20 V, Equation 18 and Equation 19 require $R_{UV1}$ of 8.25 kΩ and $R_{UV2}$ of 127 kΩ and these values are selected for this design example.

#### 8.2.2.14 $V_{CC}$ Diode

Diode D2 is an optional diode connected between $V_{OUT1}$ and the $V_{CC}$ regulator output pin. When $V_{OUT1}$ is more than one diode drop greater than the $V_{CC}$ voltage, the $V_{CC}$ bias current is supplied from $V_{OUT1}$. This results in reduced power losses in the internal $V_{CC}$ regulator which improves converter efficiency. $V_{OUT1}$ must be set to a voltage at least one diode drop higher than 8.55 V (the maximum $V_{CC}$ voltage) if D2 is used to supply bias current.

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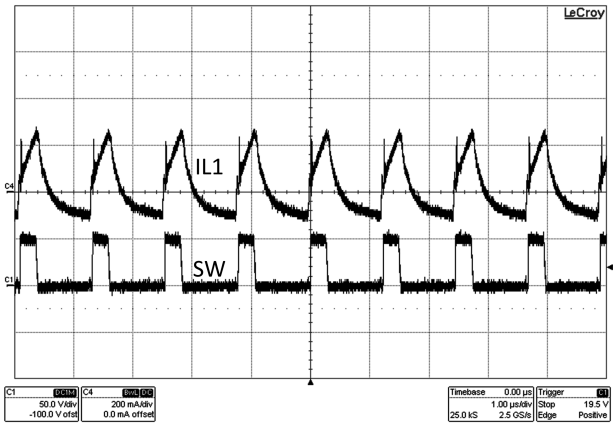
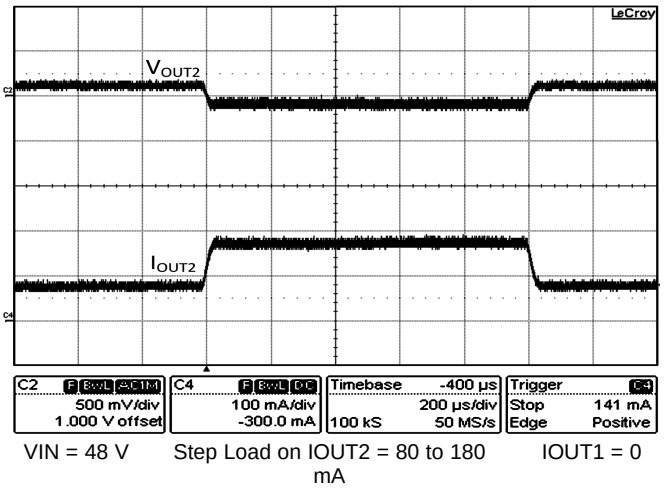
### 8.2.3 Application Curves



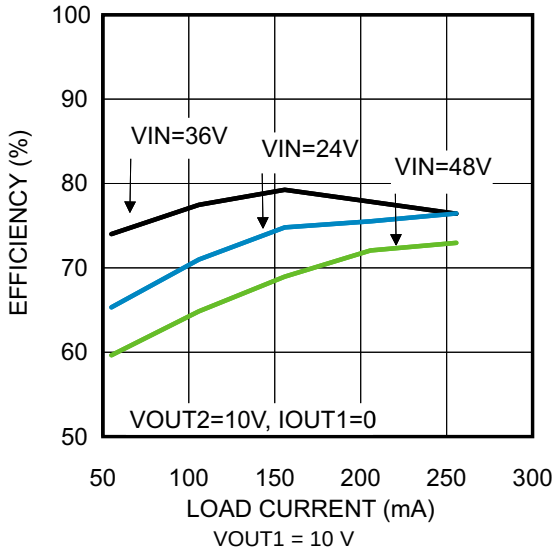

VIN = 48 V IOUT1 = 0 mA IOUT2 = 100 mA

**Figure 16. Steady-State Waveform**




VIN = 48 V Step Load on IOUT2 = 80 to 180 mA IOUT1 = 0

**Figure 17. Step Load Response**




VOUT1 = 10 V

**Figure 18. Efficiency at 750 kHz**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# 9 Power Supply Recommendations

LM34926 is a power-management device. The power supply for the device is any DC voltage source within the specified input range.

# 10 Layout

## 10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. To ensure proper layout, observe the following guidelines:

1. $C_{IN}$: The loop consisting of input capacitor ($C_{IN}$), $V_{IN}$ pin, and RTN pin carries switching currents. Therefore, place the input capacitor close to the IC, directly across $V_{IN}$ and RTN pins, and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the $V_{IN}$ and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see Figure 19).
2. $C_{VCC}$ and $C_{BST}$: The $V_{CC}$ and bootstrap (BST) bypass capacitors supply switching currents to the high and low-side gate drivers. Place these two capacitors as close to the IC as possible, and the connecting trace lengths and loop area should be minimized (see Figure 19).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM34926. Therefore take care while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: SW node switches rapidly between $V_{IN}$ and GND every cycle and is therefore a possible source of noise. SW node area should be minimized. In particular SW node should not be inadvertently connected to a copper plane or pour.

## 10.2 Layout Example

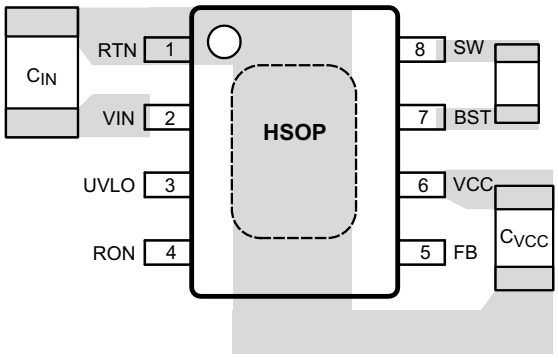


**Figure 19. Placement of Bypass Capacitors**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the LM34926 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

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## 11.4 Trademarks

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## 11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.


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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM34926MR/NOPB | Active | Production | SO PowerPAD (DDA) \| 8 | 95 \| TUBE | Yes | SN | Level-3-260C-168 HR | -40 to 125 | S000XB |
| LM34926MR/NOPB.A | Active | Production | SO PowerPAD (DDA) \| 8 | 95 \| TUBE | Yes | SN | Level-3-260C-168 HR | -40 to 125 | S000XB |
| LM34926MRX/NOPB | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | S000XB |
| LM34926MRX/NOPB.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | S000XB |
| LM34926SD/NOPB | Active | Production | WSON (NGU) \| 8 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L34926 |
| LM34926SD/NOPB.A | Active | Production | WSON (NGU) \| 8 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L34926 |
| LM34926SDX/NOPB | Active | Production | WSON (NGU) \| 8 | 4500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L34926 |
| LM34926SDX/NOPB.A | Active | Production | WSON (NGU) \| 8 | 4500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | L34926 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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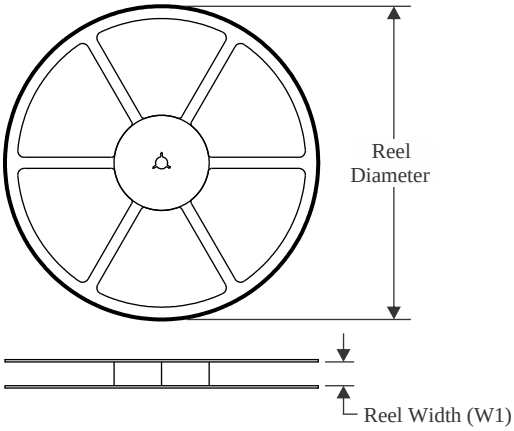
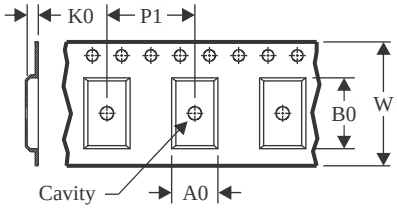
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

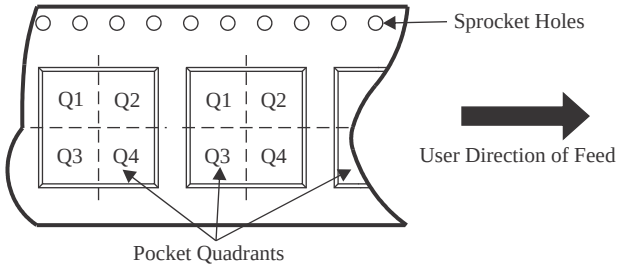



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

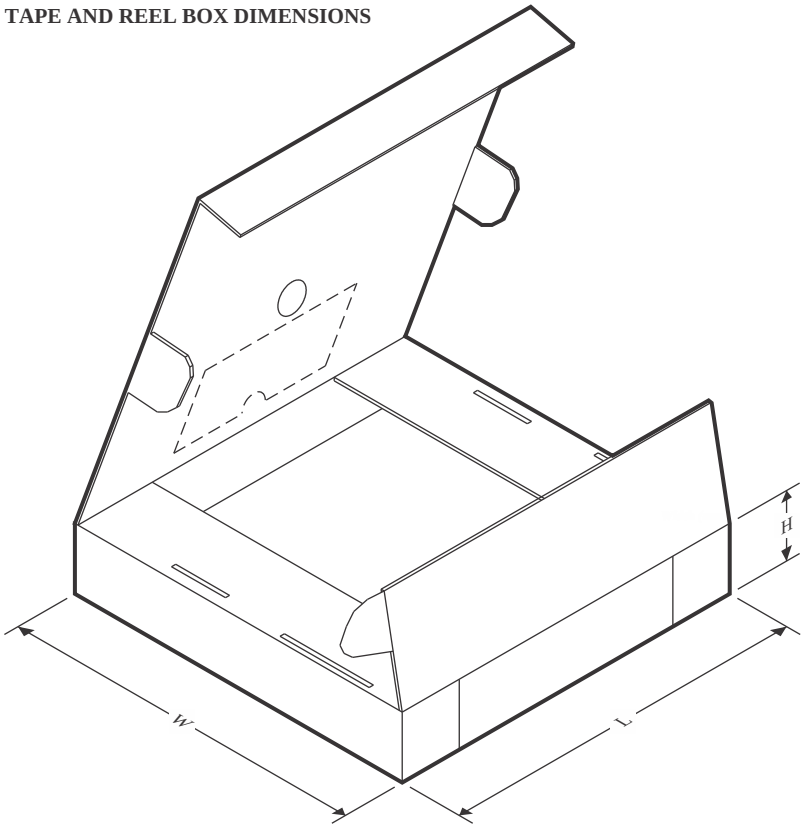
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM34926MRX/NOPB | SO PowerPAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM34926SD/NOPB | WSON | NGU | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM34926SDX/NOPB | WSON | NGU | 8 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

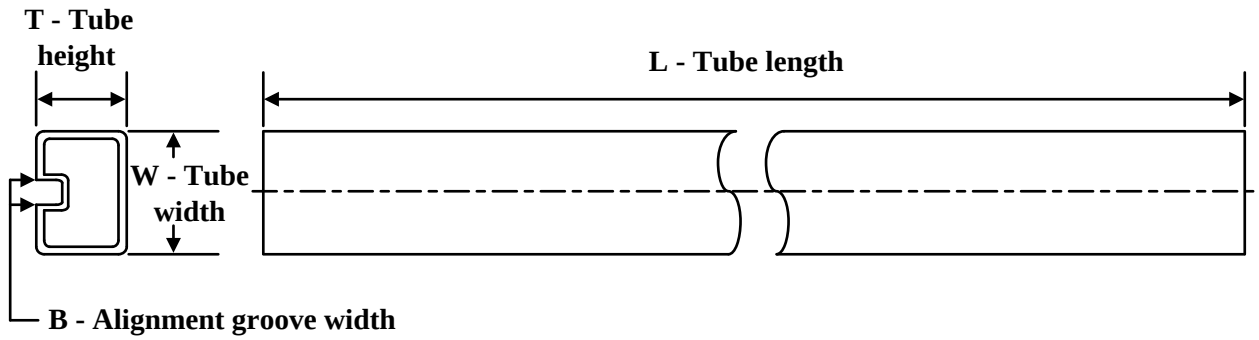
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM34926MRX/NOPB | SO PowerPAD | DDA | 8 | 2500 | 356.0 | 356.0 | 36.0 |
| LM34926SD/NOPB | WSON | NGU | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LM34926SDX/NOPB | WSON | NGU | 8 | 4500 | 367.0 | 367.0 | 35.0 |

## TUBE

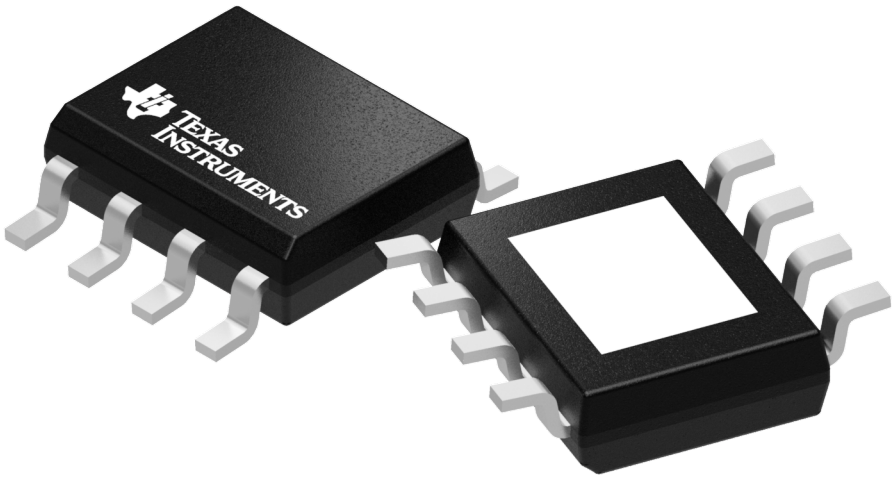



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM34926MR/NOPB | DDA | HSOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |
| LM34926MR/NOPB.A | DDA | HSOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |

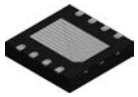
# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

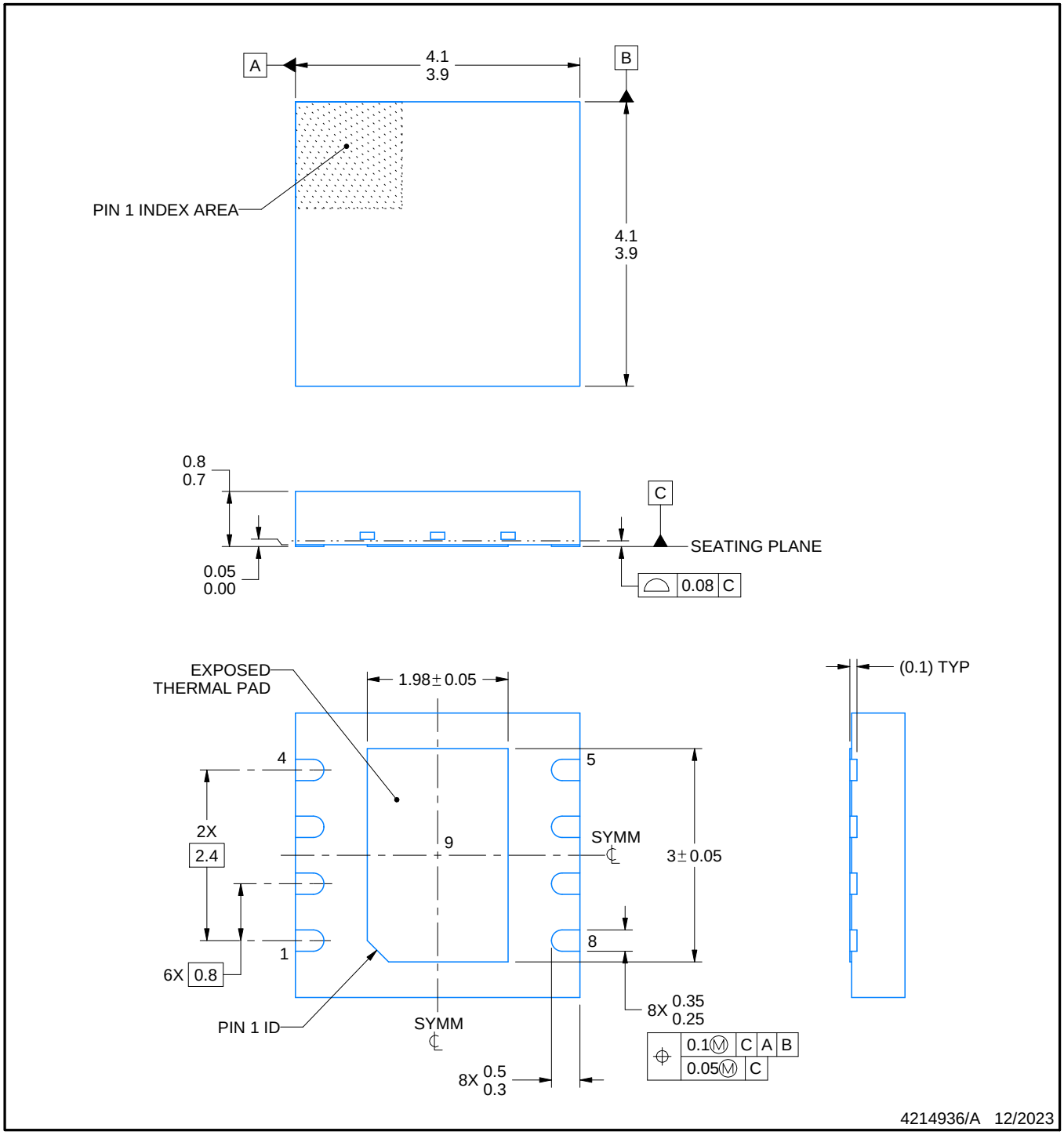
# NGU0008B



# PACKAGE OUTLINE

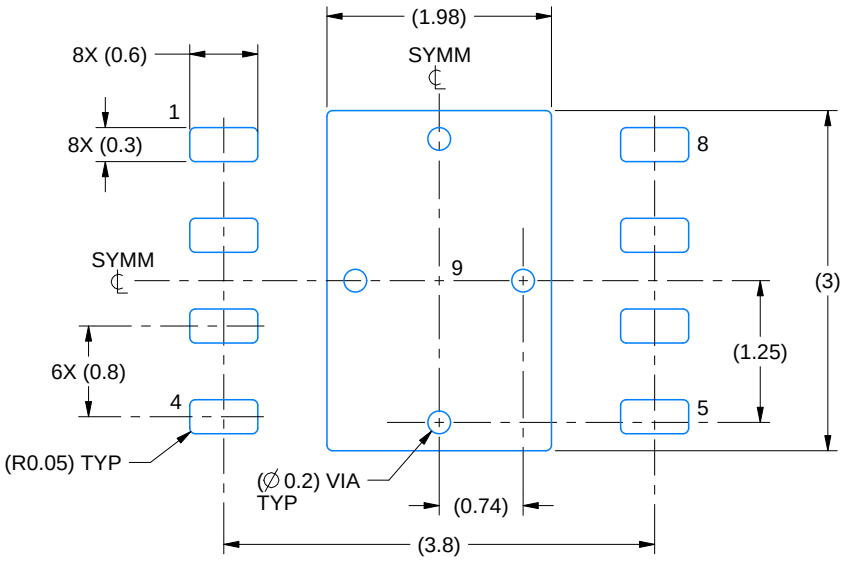
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

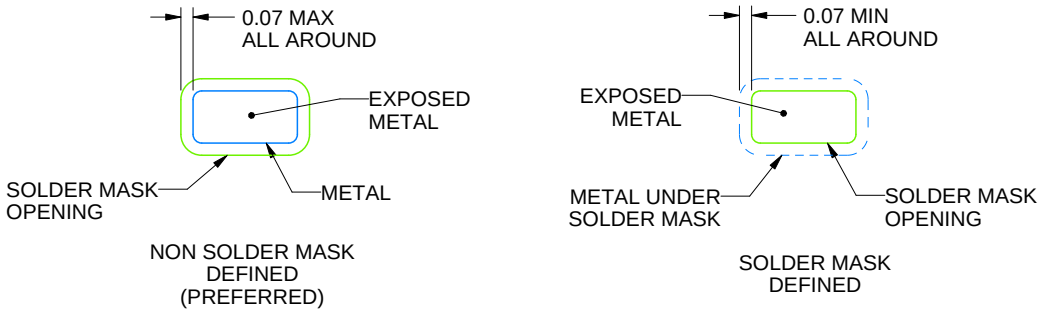



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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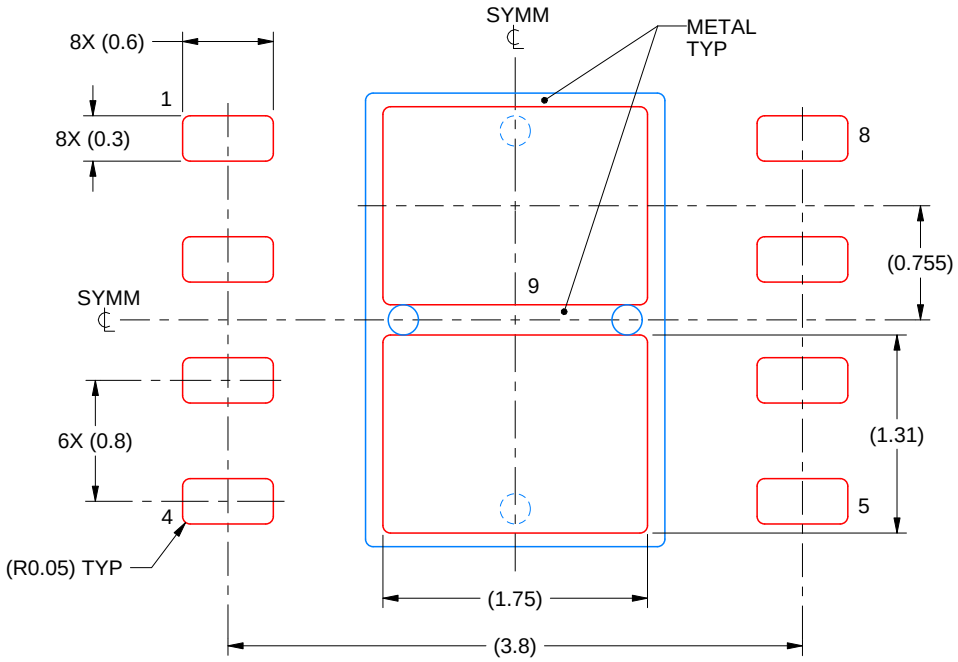
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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