TEXAS INSTRUMENTS
LM5018
JAJSBI5I – JANUARY 2012 – REVISED AUGUST 2021

LM5018 100V、300mA、コンスタント・オンタイム方式同期整流降圧 / Fly-Buck™ レギュレータ

1 特長

- 7.5V～100V の広い入力電圧範囲
- 300mA のハイサイドおよびローサイド・スイッチを内蔵
- ショットキー不要
- コンスタント・オンタイム制御
- ループ補償が不要
- 超高速の過渡応答
- ほぼ一定の動作周波数
- インテリジェントなピーク電流制限
- 出力電圧を 1.225V 以上で調整可能
- 2% の高精度帰還基準電圧
- 周波数を最大 1MHz まで調整可能
- 可変の低電圧誤動作防止
- リモート・シャットダウン
- サーマル・シャットダウン
- パッケージ:
  - WSON-8
  - SO PowerPAD™-8
- WEBENCH® Power Designer により、LM5018 を使用するカスタム設計を作成

2 アプリケーション

- スマート電力メータ
- 遠隔通信システム
- 自動車用エレクトロニクス
- 絶縁型バイアス電源 (Fly-Buck™)

3 概要

LM5018 は 100V、300mA の同期整流降圧型レギュレータで、ハイサイドとローサイドの MOSFET が内蔵されています。LM5018 に採用されているコンスタント・オンタイム (COT) 制御方式はループ補償が必要なく、過渡応答が非常に優れており、非常に高い降圧率を実現できます。オンタイムは入力電圧に反比例して変化し、入力電圧範囲の全体にわたって、周波数はほぼ一定に維持されます。高電圧のスタートアップ・レギュレータにより、IC の内部動作用および内蔵ゲート・ドライバ用にバイアス電力が供給されます。

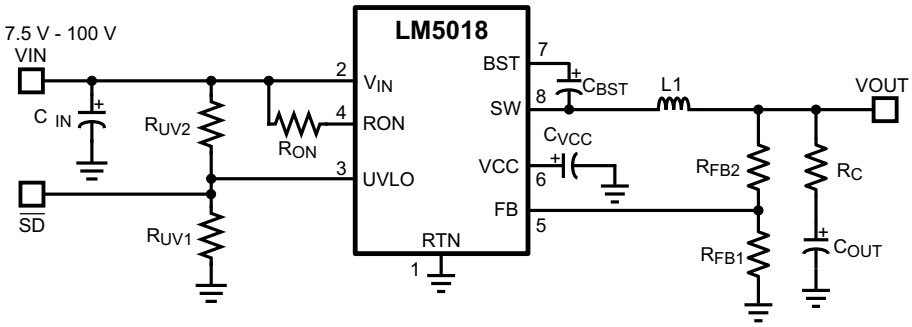
ピーク電流制限回路により、過負荷状態から保護します。低電圧誤動作防止 (UVLO) 回路は、入力低電圧スレッショルドとヒステリシスを別々にプログラム可能です。その他の保護機能として、サーマル・シャットダウンとバイアス電源低電圧誤動作防止が搭載されています。

LM5018 デバイスは、WSON-8 および SO PowerPAD-8 プラスチック・パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LM5018	SO PowerPAD (8)	4.89mm × 3.90mm
	WSON (8)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

Changes from Revision H (November 2017) to Revision I (August 2021) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- タイトルに「同期 Fly-Buck 」を追加 1
- アプリケーション の箇条書きにハイパーリンクを追加 1

Changes from Revision G (October 2015) to Revision H (November 2017) **Page**

- WEBENCH のリンクをデータシートに追加 1
- Deleted lead temperature from the *Absolute Maximum Ratings* table 4

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5 Pin Configuration and Functions

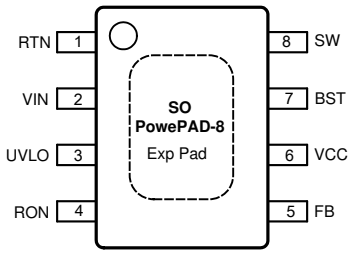

図 5-1. DDA Package 8-Pin SO PowerPAD Top View

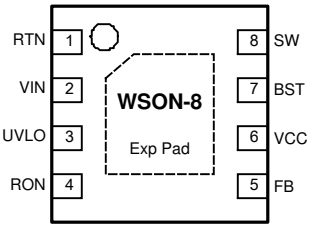

図 5-2. NGU Package 8-Pin WSON Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RTN	—	Ground	Ground connection of the integrated circuit
2	VIN	I	Input Voltage	Operating input range is 7.5 V to 100 V.
3	UVLO	I	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When UVLO pin is pulled below 0.66 V externally, the parts goes in shutdown mode.
4	RON	I	On-Time Control	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. Minimum recommended on-time is 100 ns at max input voltage.
5	FB	I	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	VCC	O	Output From the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0-µF decoupling capacitor is recommended.
7	BST	I	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01-µF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	O	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
—	EP	—	Exposed Pad	Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance.

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6 Specifications

6.1 Absolute Maximum Ratings

	MIN(1)	MAX	UNIT
V_{IN}, UVLO to RTN	–0.3	100	V
SW to RTN	–1.5	V_{IN} + 0.3	V
SW to RTN (100 ns transient)	–5	V_{IN} + 0.3	V
BST to V_{CC}		100	V
BST to SW		13	V
R_{ON} to RTN	–0.3	100	V
V_{CC} to RTN	–0.3	13	V
FB to RTN	–0.3	5	V
Maximum junction temperature(2)		150	°C
Storage temperature range, T_{stg}	–55	150	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *セクション 6.3* are conditions under which operation of the device is intended to be functional. For verified specifications and test conditions, see the *セクション 6.5*. The RTN pin is the GND reference electrically connected to the substrate.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} voltage	7.5	100	V
Operating junction temperature(2)	–40	125	°C

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see *セクション 6.5*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRICS(1)		LM5018		UNIT
		NGU (WSON)	DDA (SO PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ_{JB}	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	30.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W
Ψ_{JT}	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range, unless otherwise stated. V_{IN} = 48 V unless otherwise stated. See(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48 V, I_{CC} = 20 mA	6.25	7.6	8.55	V
	V_{CC} Current Limit	V_{IN} = 48 V(2)	26			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} increasing)		4.15	4.5	4.9	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 9 V, I_{CC} = 20 mA		2.3		V
	I_{IN} Operating Current	Nonswitching, FB = 3 V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0 V		50	225	µA
SWITCH CHARACTERISTICS						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200 mA, BST-SW = 7 V		0.8	1.8	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200 mA		0.45	1	Ω
	Gate Drive UVLO	V_{BST} – V_{SW} Rising	2.4	3	3.6	V
	Gate Drive UVLO Hysteresis			260		mV
CURRENT LIMIT						
	Current Limit Threshold		390	575	750	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	OFF-Time Generator (Test 1)	FB = 0.1 V, V_{IN} = 48 V		12		µs
	OFF-Time Generator (Test 2)	FB = 1.0 V, V_{IN} = 48 V		2.5		µs
REGULATION AND OVERVOLTAGE COMPARATORS						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	1.2	1.225	1.25	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
UNDERVOLTAGE SENSING FUNCTION						
	UV Threshold	UV Rising	1.19	1.225	1.26	V
	UV Hysteresis Input Current	UV = 2.5 V	–10	–20	–29	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	0.32	0.66		V
	Remote Shutdown Hysteresis			110		mV
THERMAL SHUTDOWN						
T_{sd}	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

6.6 Timing Requirements

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V, unless otherwise stated.

		MIN	NOM	MAX	UNIT
ON-TIME GENERATOR					
T_{ON} Test 1	V_{IN} = 32 V, R_{ON} = 100 kΩ	270	350	460	ns
T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 kΩ	188	250	336	ns
T_{ON} Test 3	V_{IN} = 75 V, R_{ON} = 250 kΩ	250	370	500	ns
T_{ON} Test 4	V_{IN} = 10 V, R_{ON} = 250 kΩ	1880	3200	4425	ns

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Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V, unless otherwise stated.

		MIN	NOM	MAX	UNIT
MINIMUM OFF-TIME					
Minimum Off-Timer	FB = 0 V		144		ns

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6.7 Typical Characteristics

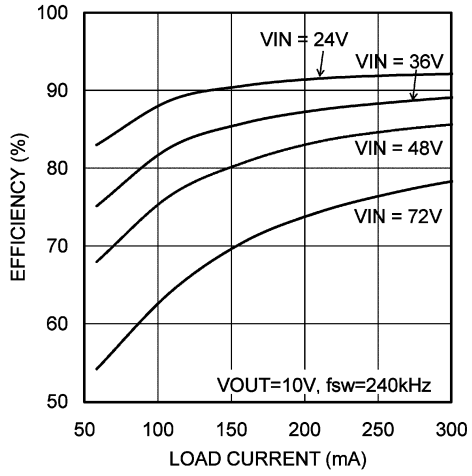

図 6-1. Efficiency at 240 kHz, 10 V

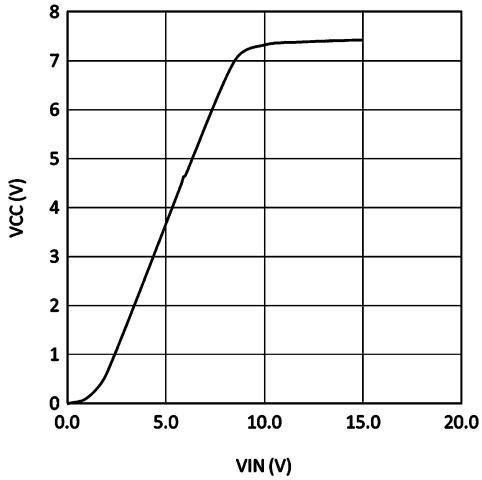

図 6-2. V_{CC} versus V_{IN}

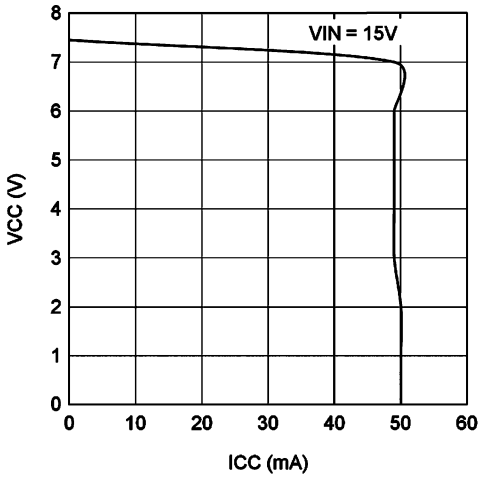

図 6-3. V_{CC} versus I_{CC}

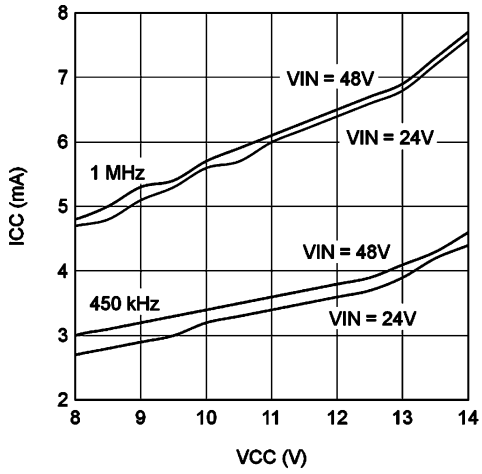

図 6-4. I_{CC} versus External V_{CC}

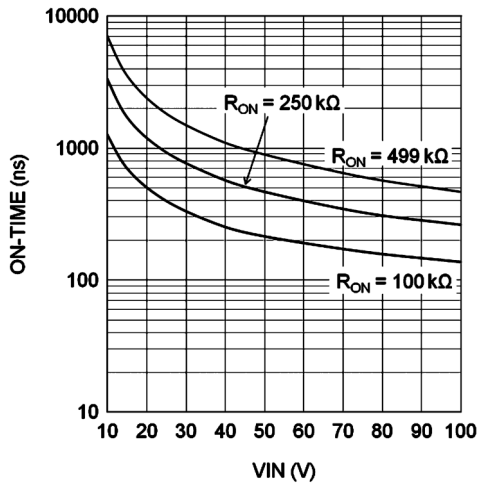

図 6-5. T_{ON} versus V_{IN} and R_{ON}

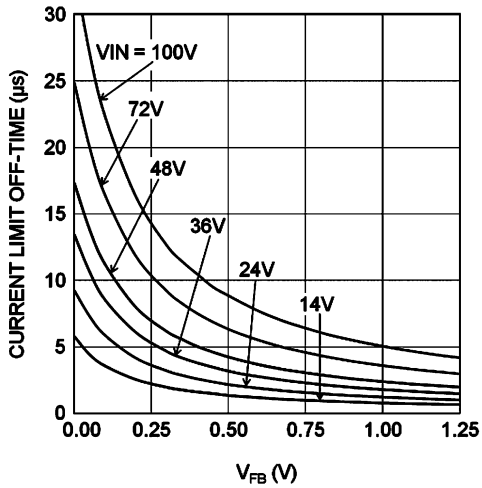

図 6-6. T_{OFF} (I_{LIM}) versus V_{FB} and V_{IN}

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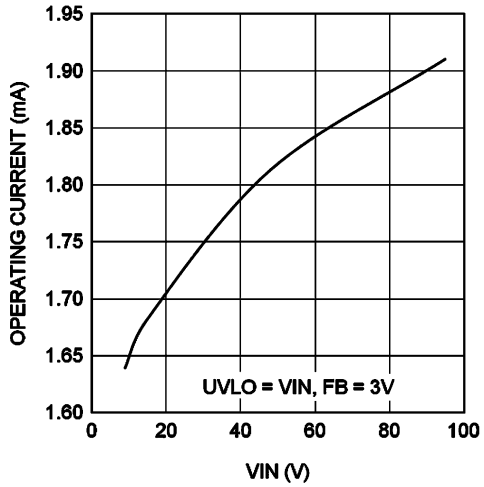

図 6-7. I_{IN} versus V_{IN} (Operating, Non-Switching)

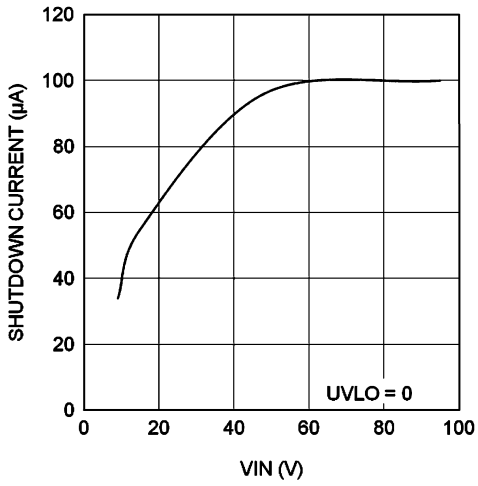

図 6-8. I_{IN} versus V_{IN} (Shutdown)

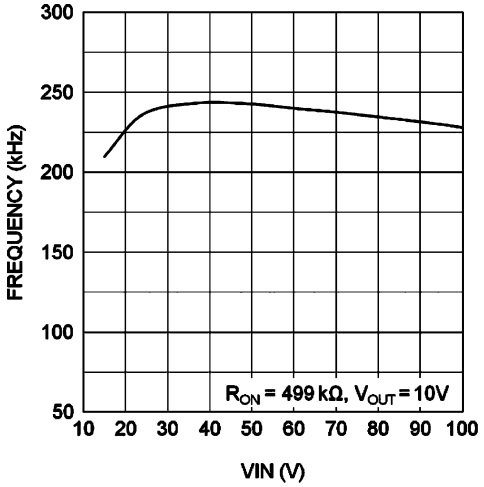

図 6-9. Switching Frequency versus V_{IN}

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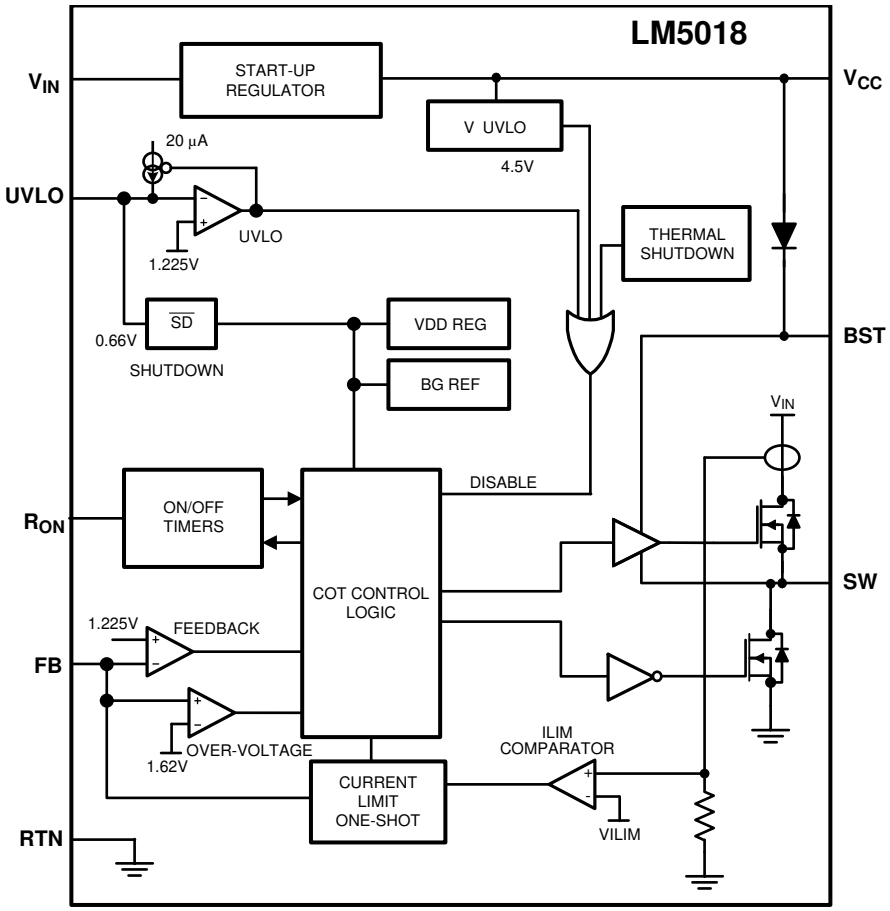
7 Detailed Description

7.1 Overview

The LM5018 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck converter capable of supplying up to 300 mA to the load. This high-voltage regulator contains 100 V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally-enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM5018 is shown in the セクション 7.2.

The LM5018 device can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well-suited for 48-V telecom and automotive power bus ranges. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Overview

The LM5018 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference, the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time, the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer. When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck

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switch is turned on for another on-time one-shot period. This continues until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low-side (sync) FET is 'on' when the high-side (buck) FET is 'off.' The inductor current ramps up when the high-side switch is ‘on’ and ramps down when the high-side switch is ‘off’. There is no diode emulation feature in this IC, therefore, the inductor current can ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as shown in 式 1.

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \tag{1}$$

where

- $K = 9 \times 10^{-11}$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as shown in 式 2.

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \tag{2}$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM5018. In cases where the capacitor ESR is too small, additional series resistance can be required (R_C in 図 7-1).

For applications where lower output voltage ripple is required, the output can be taken directly from a low ESR output capacitor, as shown in 図 7-1. However, R_C slightly degrades the load regulation.

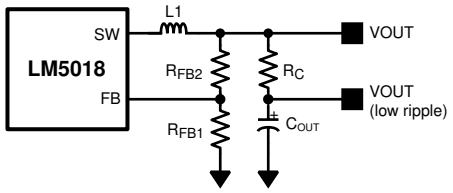

図 7-1. Low Ripple Output Configuration

7.3.2 V_{CC} Regulator

The LM5018 device contains an internal high-voltage linear regulator with a nominal output of 7.6 V. The input pin (V_{IN}) can be connected directly to the line voltages up to 100 V. The V_{CC} regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the undervoltage lockout (V_{CC} UVLO) threshold of 4.5 V, the IC is enabled.

An internal diode connected from V_{CC} to the BST pin replenishes the charge in the gate drive bootstrap capacitor when SW pin is low.

At high-input voltages, the power dissipated in the high-voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the V_{CC} regulator can supply up to 7 mA of current resulting in 48 V × 7 mA = 336 mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source between 8.55 V and 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225 V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high-side

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switch stays on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high-side switch stays off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage is below 1.225 V at the end of each on-time, causing the high-side switch to turn on immediately after the minimum forced off-time of 144 ns. The high-side switch can be turned off before the on-time is over if the peak current in the inductor reaches the current limit threshold.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62 V reference. If the voltage at FB rises above 1.62 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage and the output load changes suddenly. The high-side switch does not turn on again until the voltage at FB falls below 1.225 V.

7.3.5 On-Time Generator

The on-time for the LM5018 is determined by the R_{ON} resistor and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time for the LM5018 can be calculated using 式 3.

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \tag{3}$$

See 図 6-5. R_{ON} must be selected for a minimum on-time (at maximum V_{IN}) greater than 100 ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

7.3.6 Current Limit

The LM5018 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds 575 mA, the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0 V and V_{IN} = 48 V, the maximum off-time is set to 16 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from 式 4.

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2V} \ \mu s \tag{4}$$

The current limit protection feature is peak limited. The maximum average output is less than the peak.

7.3.7 N-Channel Buck Switch and Driver

The LM5018 device integrates an N-Channel Buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.01-µF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

7.3.8 Synchronous Rectifier

The LM5018 device provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

7.3.9 Undervoltage Detector

The LM5018 device contains a dual level undervoltage lockout (UVLO) circuit. A summary of threshold voltages and operational states is provided in the *セクション 7.4*. When the UVLO pin voltage is below 0.66 V, the regulator

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is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the regulator is in standby mode. In standby mode, the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

If the UVLO pin is connected directly to the V_{IN} pin, the regulator begins operation once the V_{CC} undervoltage is satisfied.

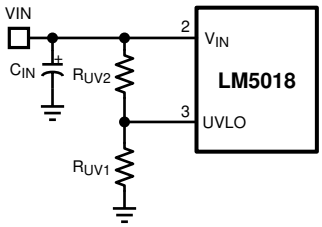

図 7-2. UVLO Resistor Setting

7.3.10 Thermal Protection

The LM5018 device must be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM5018 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

7.3.11 Ripple Configuration

The LM5018 uses Constant-On-Time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

表 7-1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac-coupled using C_{ac} to the feedback node (FB). Because this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See the *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details for each ripple generation method.

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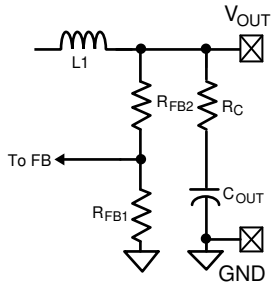
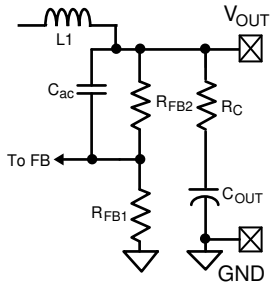
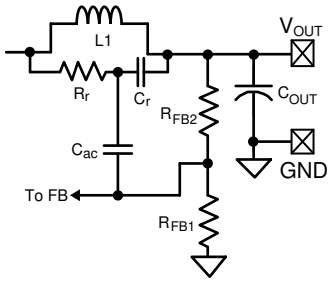
表 7-1. Ripple Configuration

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		
$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ (5)	$C \geq \frac{5}{f_{sw}(R_{FB2} \| \| R_{FB1})}$ $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$ (6)	$C_r = 3300\ pF$ $C_{ac} = 100\ nF$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$ (7)

7.3.12 Soft Start

A soft-start feature can be implemented with the LM5018 using an external circuit. As shown in 図 7-3, the soft-start circuit consists of one capacitor, C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established prior to the V_{OUT} voltage. Capacitor C_1 is discharged and D is thereby forward biased to pull up the FB voltage. The FB voltage exceeds the reference voltage (1.225 V) and switching is therefore disabled. As capacitor C_1 charges, the voltage at node B gradually decreases and switching commences. V_{OUT} gradually rises to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above FB voltage, the soft-start sequence is finished and D is reverse biased.

During the initial part of the start-up, the FB voltage can be approximated as follows. Note that the effect of R_1 has been ignored to simplify the calculation shown in 式 8.

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (8)$$

C1 is charged after the first start-up. Diode D1 is optional and can be added to discharge C1 and initialize the soft-start sequence when the input voltage experiences a momentary drop.

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To achieve the desired soft-start, the following design guidance is recommended:

1. R_2 is selected so that V_{FB} is higher than 1.225 V for a V_{CC} of 4.5 V, but is lower than 5 V when V_{CC} is 8.55 V. If an external V_{CC} is used, V_{FB} must not exceed 5 V at maximum V_{CC}.
2. C_1 is selected to achieve the desired start-up time that can be determined from 式 9.

$$t_S = C_1 \times \left(R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}}\right) \quad (9)$$

3. R_1 is used to maintain the node B voltage at zero after the soft start is finished. A value larger than the feedback resistor divider is preferred. Note that the effect of R_1 is ignored in the previous equations.

Based on the schematic shown in 図 8-1, selecting C_1 = 1 µF, R_2 = 1 kΩ, and R_1 = 30 kΩ results in a soft-start time of about 2 ms.

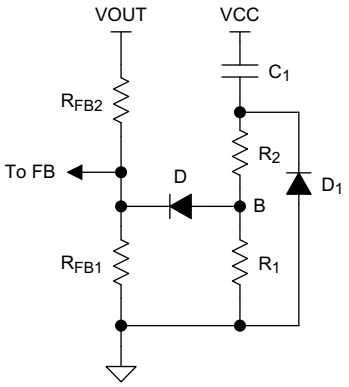

図 7-3. Soft-Start Circuit

7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM5018 device (see 表 7-2 for the detailed functional states).

表 7-2. UVLO Mode

UVLO	V_{CC}	MODE	DESCRIPTION
< 0.66 V	Disabled	Shutdown	V_{CC} regulator disabled. Switching disabled
0.66 V — 1.225 V	Enabled	Standby	V_{CC} regulator enabled Switching disabled
> 1.225 V	V_{CC} < 4.5 V	Standby	V_{CC} regulator enabled. Switching disabled
	V_{CC} > 4.5 V	Operating	V_{CC} enabled. Switching enabled

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM5018 device is a step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 300 mA. Use the following design procedure to select component values for the LM5018 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

8.2.1 Application Circuit: 12.5- to 95-V Input and 10-V, 300-mA Output Buck Converter

The application schematic of a buck supply is shown in 図 8-1. For output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (8.55 V, see the *セクション 6.5*), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), for higher efficiency and lower power dissipation in the IC.

The following design example uses equations from the *セクション 7.3* with component names provided in the 図 8-1. Corresponding component designators from 図 8-1 are also provided for each selected value.

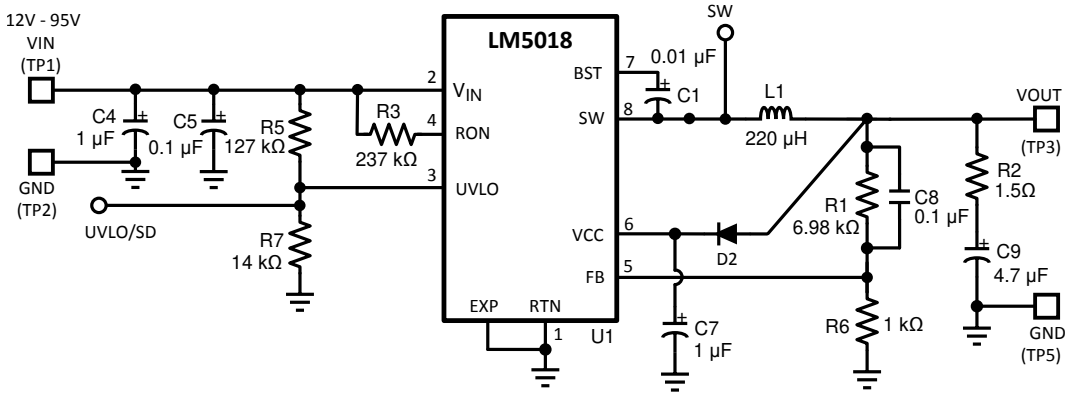

図 8-1. 12.5-V to 95-V Input and 10-V, 300-mA Output Buck Converter

8.2.1.1 Design Requirements

Selection of external components is illustrated through a design example. The design example specifications are shown in 表 8-1.

表 8-1. Buck Converter Design Specifications

DESIGN PARAMETERS	VALUE
Input Range	12.5 V to 95 V, transients up to 100 V
Output Voltage	10 V
Maximum Output Current	300 mA
Nominal Switching Frequency	≈ 440 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5018 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 RFB1, RFB2

$V_{OUT} = V_{FB} \times (R_{FB2} / R_{FB1} + 1)$, and since V_{FB} = 1.225 V, the ratio of R_{FB2} to R_{FB1} is calculated to be 7:1. Standard values are chosen with R_{FB2} = R1 = 6.98 kΩ and R_{FB1} = R6 = 1.00 kΩ. Other values can be used as long as the 7:1 ratio is maintained.

8.2.1.2.3 Frequency Selection

At the minimum input voltage, the maximum switching frequency of the LM5018 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as given by 式 10.

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ ns} = 1\ MHz \tag{10}$$

Similarly, at maximum input voltage, the maximum switching frequency of LM5018 is restricted by the minimum T_{ON} as given by 式 11.

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/48}{100\ ns} = 2.1\ MHz \tag{11}$$

Resistor R_{ON} sets the nominal switching frequency based on 式 12.

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \tag{12}$$

where

- $K = 9 \times 10^{-11}$

Operation at high switching frequency results in lower efficiency while providing the smallest solution. For this example, 440 kHz was selected, resulting in R_{ON} = 253 kΩ. A standard value for R_{ON} = R3 = 237 kΩ is selected.

8.2.1.2.4 Inductor Selection

The minimum inductance is selected to limit the inductor ripple current to 20 to 40 percent of the maximum load current. In addition, the peak inductor current at maximum load must be smaller than the minimum current limit threshold provided in the *セクション 6.5*. The inductor current ripple is given by 式 13.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{13}$$

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The maximum ripple is observed at maximum input voltage. Substituting V_{IN} = 95 V and Δ_{IL} = 40 percent × $I_{OUT(max)}$ results in L1 = 169 µH. The higher standard value of 220 µH is chosen. With this value of inductance, peak-to-peak minimum and maximum inductor current ripple of 27 mA and 92 mA occur at the minimum and maximum input voltages, respectively. The peak inductor and switch current is given by 式 14.

$$I_{LI}(peak) = I_{OUT} + \frac{\Delta I_L(max)}{2} = 346\ mA \tag{14}$$

The peak inductor current of 346 mA is smaller than the minimum current limit threshold of 390 mA. The selected inductor must be able to operate at the maximum current limit of 750 mA during start-up and overload conditions without saturating.

8.2.1.2.5 Output Capacitor

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is given by 式 15.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{ripple}} \tag{15}$$

where

- ΔV_{ripple} is the voltage ripple across the capacitor
- ΔI_L is the peak-to-peak inductor ripple current

Assuming V_{IN} = 95 V and substituting ΔV_{ripple} = 10 mV gives C_{OUT} = 2.6 µF. A 4.7-µF standard value is selected for C_{OUT} = C9. An X5R or X7R type capacitor with a voltage rating 16 V or higher must be selected.

8.2.1.2.6 Type II Ripple Circuit

A type II ripple circuit, as described in the *セクション 7.3.11,* section is chosen for this example. For a constant on-time converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on C_{OUT}.

Using type II ripple circuit equations with a minimum FB pin ripple of 25 mV, the values of the series resistor R_C and ac coupling capacitor C_{ac} can calculated.

$$C_{ac} \geq \frac{5}{f_{sw}(R_{FB2}||R_{FB1})}$$

$$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \tag{16}$$

Assuming R_{FB2} = 6.98 kΩ and R_{FB1} = 1 kΩ, the calculated minimum value of C_{ac} is 0.013 µF. A standard value of 0.1 µF is selected for C_{ac} = C8. The value of the series output resistor R_C is calculated for the minimum input voltage condition when the inductor ripple current as at a minimum. Using 式 13 and assuming V_{IN} = 12.5 V, the minimum inductor ripple current is 27 mA. The calculated minimum value of R_C is 0.93 Ω. A standard value of 1.5 Ω is selected for R_C = R2 to provide additional ripple for stable switching at low V_{IN}.

8.2.1.2.7 V_{CC} and Bootstrap Capacitor

The V_{CC} capacitor provides charge to bootstrap capacitor as well as internal circuitry and low side gate driver. The bootstrap capacitor provides charge to high-side gate driver. The recommended value for C_{VCC} = C7 = 1 µF. A good value for C_{BST} = C1 = 0.01 µF.

8.2.1.2.8 Input Capacitor

Input capacitor must be large enough to limit the input voltage ripple which can be calculated using 式 17.

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f_{SW} \times \Delta V_{IN}} \tag{17}$$

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Choosing a ΔV_{IN} = 0.5 V gives a minimum C_{IN} = 0.34 µF. A standard value of 1 µF is selected for C_{IN} = C4. The input capacitor must be rated for the maximum input voltage under all conditions. A 100 V X7R dielectric must be selected for this design.

Input capacitor must be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1-µF capacitor must be placed near the IC to provide a bypass path for the high frequency component of the switching current.

8.2.1.2.9 UVLO Resistors

The UVLO resistors R_{UV1} and R_{UV2} set the UVLO threshold and hysteresis according to the relationship shown in 式 18 and 式 19.

$$V_{IN}(HYS) = I_{HYS} \times R_{UV2} \tag{18}$$

where

- I_{HYS} = 20 µA

$$V_{IN}\,(UVLO,rising) = 1.225\ V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \tag{19}$$

Setting UVLO hysteresis of 2.5 V and UVLO rising threshold of 12 V results in R_{UV1} = 14.53 kΩ and R_{UV2} = 125 kΩ. Selecting standard values of R_{UV1} = R7 = 14 kΩ and R_{UV2} = R5 = 127 kΩ results in UVLO threshold and hysteresis of 12.4 V and 2.5 V, respectively.

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8.2.1.3 Application Curves

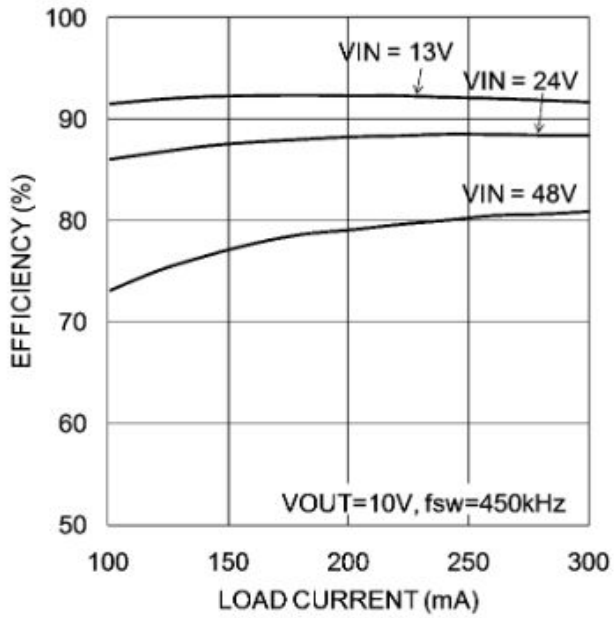

図 8-2. Efficiency versus Load Current

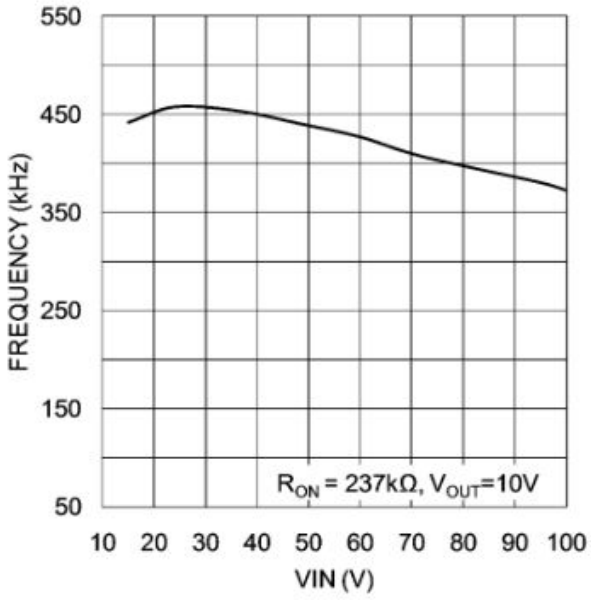

図 8-3. Frequency versus Input Voltage

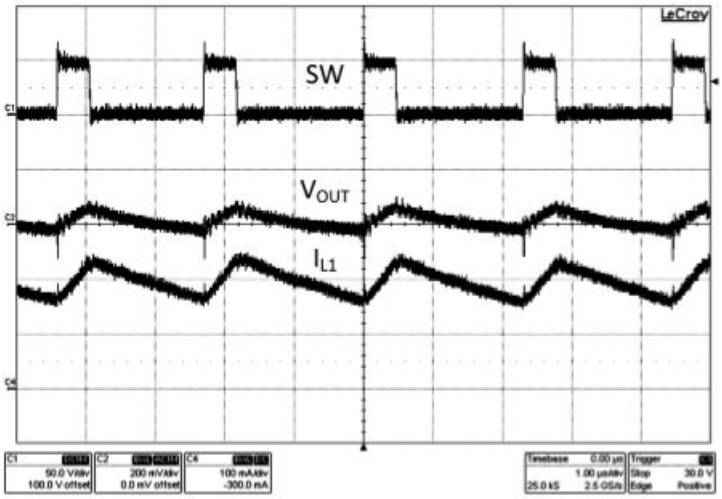

図 8-4. Typical Switching Waveform (V_{IN} = 48 V, I_{OUT} = 200 mA)

8.2.2 Typical Isolated DC-DC Converter Using LM5018

An isolated supply using LM5018 is shown in 図 8-5. Inductor (L) in a typical buck circuit is replaced with a coupled inductor (X1). A diode (D1) is used to rectify the voltage on a secondary output. The nominal voltage at the secondary output (V_{OUT2}) is given by 式 20.

$$V_{OUT2} = V_{OUT1} \times \frac{N_S}{N_P} - V_F \quad (20)$$

where

- V_F is the forward voltage drop of D1.
- N_P and N_S are the number of turns on the primary and secondary of coupled inductor X1.

For output voltage (V_{OUT1}) more than one diode drop above the maximum V_{CC} (8.55 V), the V_{CC} pin can be diode connected to V_{OUT1} for higher efficiency and low dissipation in the IC.

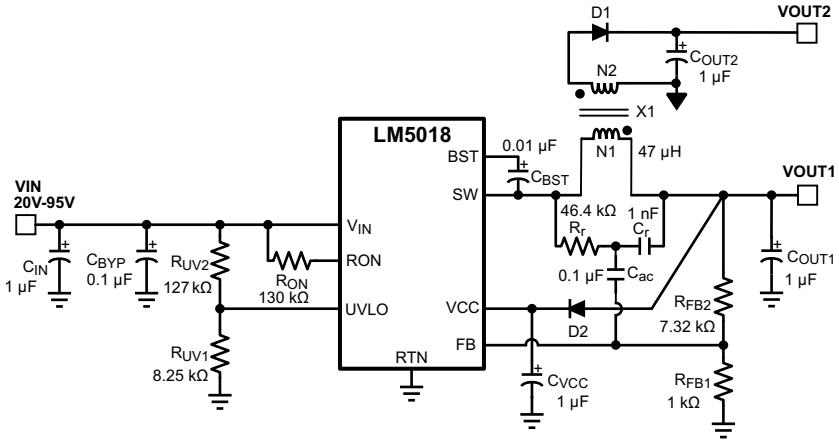

図 8-5. Isolated Fly-Buck™ Converter Using LM5018

8.2.2.1 Design Requirements

表 8-2 lists the design parameters of this example.

表 8-2. Buck Converter Design Specifications

DESIGN PARAMETERS	VALUE
Input Range	20 V to 100 V
Primary Output Voltage	10 V
Secondary (Isolated) Output Voltage	9.5 V
Maximum Output Current (Primary + Secondary)	250 mA
Maximum Power Output	2.5 W
Nominal Switching Frequency	750 kHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Transformer Turns Ratio

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary (isolated) output voltage. In this design example, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected. Therefore, N2 / N1 = 1. If the secondary (isolated) output voltage is significantly higher or lower than the primary output voltage, a turns ratio less than or greater than 1 is recommended. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. This condition is satisfied if VOUT1 < V_{IN_MIN} / 2.

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8.2.2.2.2 Total IOUT

The total primary referred load current is calculated by multiplying the isolated output load or loads by the turns ratio of the transformer as shown in 式 21.

$$I_{OUT(MAX)} = I_{OUT1} + I_{OUT2} \times \frac{N2}{N1} = 0.25\ A \tag{21}$$

8.2.2.2.3 RFB1, RFB2

The feedback resistors are selected to set the primary output voltage. The selected value for R_{FB1} is 1 kΩ. R_{FB2} can be calculated using the following equations to set V_{OUT1} to the specified value of 10 V. A standard resistor value of 7.32 kΩ is selected for R_{FB2}.

$$V_{OUT1} = 1.225V \text{ x } \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \tag{22}$$

$$\rightarrow R_{FB2} = \left(\frac{V_{OUT1}}{1.225} - 1\right) \text{ x } R_{FB1} = 7.16\ k\Omega \tag{23}$$

8.2.2.2.4 Frequency Selection

式 1 is used to calculate the value of R_{ON} required to achieve the desired switching frequency.

$$f_{SW} = \frac{V_{OUT1}}{K \text{ x } R_{ON}} \tag{24}$$

where

- $K = 9 \times 10^{-11}$

For V_{OUT1} of 10 V and f_{SW} of 750 kHz, the calculated value of R_{ON} is 148 kΩ. A lower value of 130 kΩ is selected for this design to allow for second order effects at high switching frequency that are not included in 式 24.

8.2.2.2.5 Transformer Selection

A coupled inductor or a flyback-type transformer is required for this topology. Energy is transferred from primary to secondary when the low-side synchronous switch of the buck converter is conducting.

The maximum inductor primary ripple current that can be tolerated without exceeding the buck switch peak current limit threshold (0.39 A minimum) is given by 式 25.

$$\Delta I_{L1} = \left(0.39\ A - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}\right) \times 2 = 0.28\ A \tag{25}$$

Using the maximum peak-to-peak inductor ripple current ΔI_{L1} from 式 25, the minimum inductor value is given by 式 26.

$$L1 = \frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L1} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 42.6\ \mu H \tag{26}$$

A higher value of 47 µH is selected to ensure the high-side switch current does not exceed the minimum peak current limit threshold.

8.2.2.2.6 Primary Output Capacitor

In a conventional buck converter, the output ripple voltage is calculated as shown in 式 27.

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$$\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}} \quad (27)$$

To limit the primary output ripple voltage ΔV_{OUT1} to approximately 50 mV, an output capacitor C_{OUT1} of 0.93 µF is required.

図 8-6 shows the primary winding current waveform (IL1) of a Fly-Buck converter. The reflected secondary winding current adds to the primary winding current during the buck switch off-time. Because of this increased current, the output voltage ripple is not the same as in conventional buck converter. The output capacitor value calculated in 式 27 must be used as the starting point. Optimization of output capacitance over the entire line and load range must be done experimentally. If the majority of the load current is drawn from the secondary isolated output, a better approximation of the primary output voltage ripple is given by 式 28.

$$\Delta V_{OUT1} = \frac{\left(I_{OUT2} \times \frac{N2}{N1}\right) \times T_{ON(MAX)}}{C_{OUT1}} \approx 0.16 \text{ V} \quad (28)$$

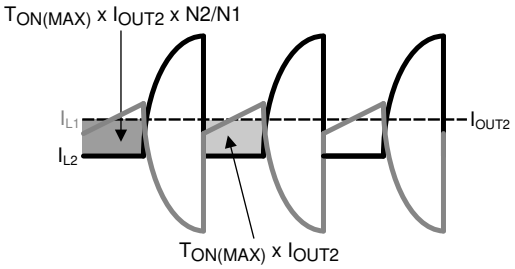

図 8-6. Current Waveforms for C_{OUT1} Ripple Calculation

A standard 1-µF, 25-V capacitor is selected for this design. If lower output voltage ripple is required, a higher value must be selected for C_{OUT1} and C_{OUT2}.

8.2.2.2.7 Secondary Output Capacitor

A simplified waveform for secondary output current (I_{OUT2}) is shown in 図 8-7.

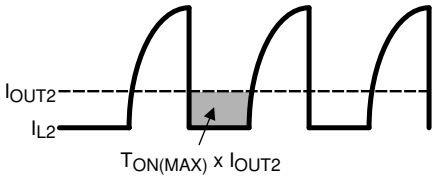

図 8-7. Secondary Current Waveforms for C_{OUT2} Ripple Calculation

The secondary output current (I_{OUT2}) is sourced by C_{OUT2} during on-time of the buck switch, T_{ON}. Ignoring the current transition times in the secondary winding, the secondary output capacitor ripple voltage can be calculated using 式 29.

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON\ (MAX)}}{C_{OUT2}} \quad (29)$$

For a 1:1 transformer turns ratio, the primary and secondary voltage ripple equations are identical. Therefore, C_{OUT2} is chosen to be equal to C_{OUT1} (1 µF) to achieve comparable ripple voltages on primary and secondary outputs.

If lower output voltage ripple is required, a higher value must be selected for C_{OUT1} and C_{OUT2}.

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8.2.2.2.8 Type III Feedback Ripple Circuit

A type III ripple circuit as described in *セクション 7.3.11* is required for the Fly-Buck topology. Type I and Type II ripple circuits use series resistance and the triangular inductor ripple current to generate ripple at V_{OUT} and the FB pin. The primary ripple current of a Fly-Buck is the combination or primary and reflected secondary currents as illustrated in 図 8-6. In the Fly-Buck topology, Type I and Type II ripple circuits suffer from large jitter as the reflected load current affects the feedback ripple.

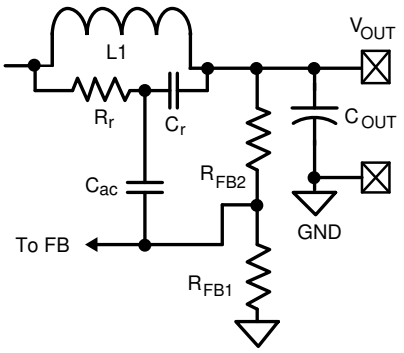

図 8-8. Type III Ripple Circuit

Selecting the Type III ripple components using the equations from *セクション 7.3.11* ensures that the FB pin ripple is be greater than the capacitive ripple from the primary output capacitor C_{OUT1}. The feedback ripple component values are chosen as shown in 式 30.

$$C_r = 1000 \text{ pF}$$
$$C_{ac} = 0.1 \ \mu\text{F}$$
$$R_r C_r \leq \frac{(V_{IN\,(MIN)} - V_{OUT}) \times T_{ON}}{50 \text{ mV}} \tag{30}$$

The calculated value for Rr is 66 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance must be selected to allow for variations in T_{ON}, C_{OUT1}, and other components. For this design, Rr value of 46.4 kΩ is selected.

8.2.2.2.9 Secondary Diode

The reverse voltage across secondary-rectifier diode D1 when the high-side buck switch is off can be calculated using 式 31.

$$V_{D1} = \frac{N2}{N1} V_{IN} \tag{31}$$

For a V_{IN_MAX} of 95 V and the 1:1 turns ratio of this design, a 100-V Schottky is selected.

8.2.2.2.10 V_{CC} and Bootstrap Capacitor

A 1-µF capacitor of 16 V or higher rating is recommended for the V_{CC} regulator bypass capacitor.

A good value for the BST pin bootstrap capacitor is 0.01-µF with a 16 V or higher rating.

8.2.2.2.11 Input Capacitor

The input capacitor is typically a combination of a smaller bypass capacitor located near the regulator IC and a larger bulk capacitor. The total input capacitance must be large enough to limit the input voltage ripple to a desired amplitude. For input ripple voltage ΔV_{IN}, C_{IN} can be calculated using 式 32.

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f \times \Delta V_{IN}} \tag{32}$$

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Choosing a ΔV_{IN} of 0.5 V gives a minimum C_{IN} of 0.167 µF. A standard value of 0.1 µF is selected for C_{BYP} in this design. A bulk capacitor of higher value reduces voltage spikes due to parasitic inductance between the power source to the converter. A standard value of 1 µF is selected for C_{IN} in this design. The voltage ratings of the two input capacitors must be greater than the maximum input voltage under all conditions.

8.2.2.2.12 UVLO Resistors

UVLO resistors R_{UV1} and R_{UV2} set the undervoltage lockout threshold and hysteresis according to 式 33 and 式 34.

$$V_{IN\,(HYS)} = I_{HYS} \times R_{UV2} \tag{33}$$

where

- I_{HYS} = 20 µA, typical

$$V_{IN}(\text{UVLO, rising}) = 1.225\text{V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \tag{34}$$

For a UVLO hysteresis of 2.5 V and UVLO rising threshold of 20 V, 式 33 and 式 34 require R_{UV1} of 8.25 kΩ and R_{UV2} of 127 kΩ and these values are selected for this design example.

8.2.2.2.13 V_{CC} Diode

Diode D2 is an optional diode connected between V_{OUT1} and the V_{CC} regulator output pin. When V_{OUT1} is more than one diode drop greater than the V_{CC} voltage, the V_{CC} bias current is supplied from V_{OUT1}. This results in reduced power losses in the internal V_{CC} regulator which improves converter efficiency. V_{OUT1} must be set to a voltage at least one diode drop higher than 8.55 V (the maximum V_{CC} voltage) if D2 is used to supply bias current.

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8.2.2.3 Application Curves

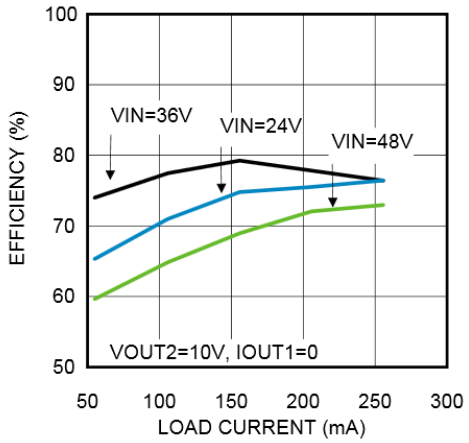

図 8-9. Efficiency at 750 kHz, VOUT1 = 10 V

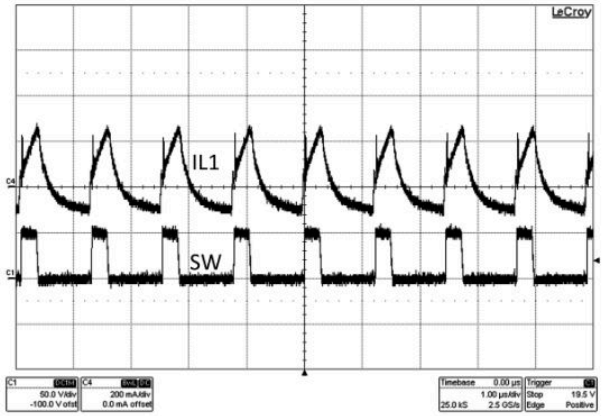

図 8-10. Steady-State Waveform (VIN = 48 V, I_{OUT1} = 0 mA, I_{OUT2} = 100 mA)

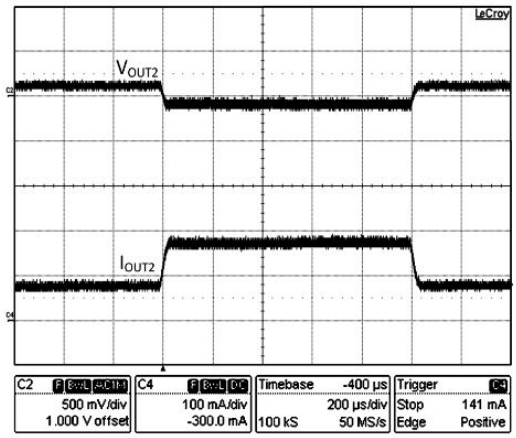

図 8-11. Step Load Response (VIN = 48 V, I_{OUT1} = 0, Step Load on I_{OUT2} = 80 mA to 180 mA)

9 Power Supply Recommendations

The LM5018 is a power management device. The power supply for the device is any DC voltage source within the specified input range.

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10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see 図 10-1).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see 図 10-1).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM5018. Therefore, care must be taken while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace must not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

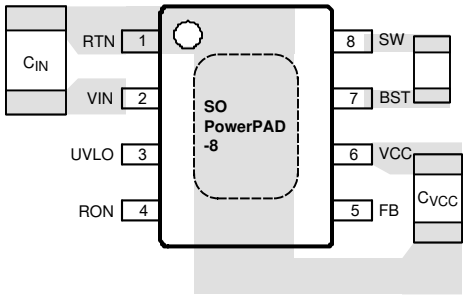

図 10-1. Placement of Bypass Capacitors

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5018 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

- *AN-2292 Designing an Isolated Buck (Flyback) Converter* (SNVA674)
- *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166)
- *AN-2239 LM5018 Isolated Evaluation Board* (SNVA667)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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WEBENCH® are registered trademarks of Texas Instruments.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5018MR/NOPB	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L5018 MR
LM5018MR/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L5018 MR
LM5018MRX/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L5018 MR
LM5018MRX/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L5018 MR
LM5018SD/NOPB	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5018
LM5018SD/NOPB.A	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5018
LM5018SDX/NOPB	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5018
LM5018SDX/NOPB.A	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5018

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

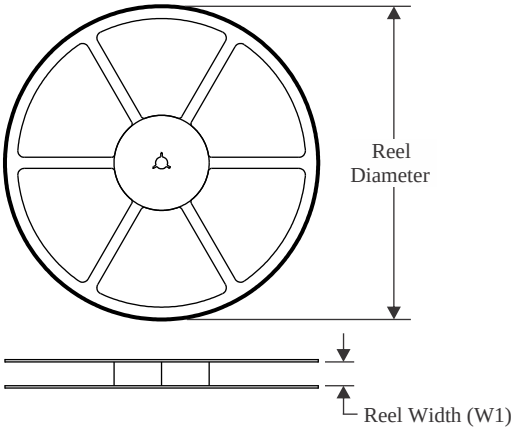
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

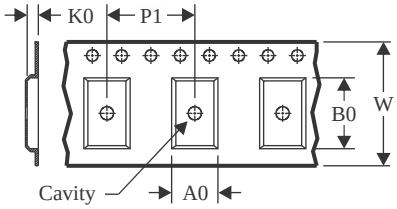
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

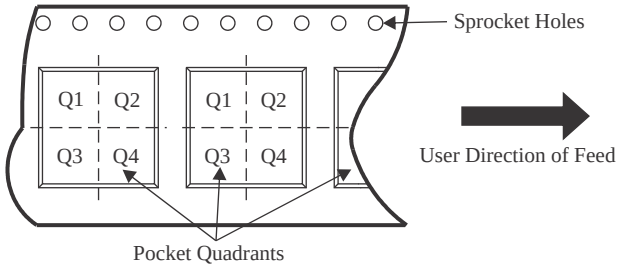


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

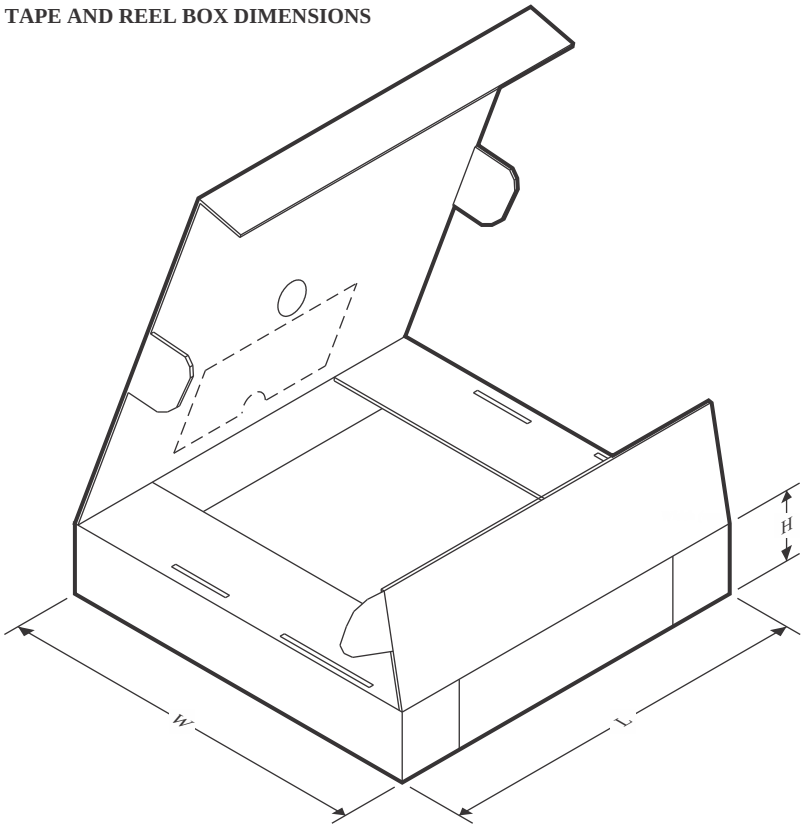
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5018MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5018SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5018SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

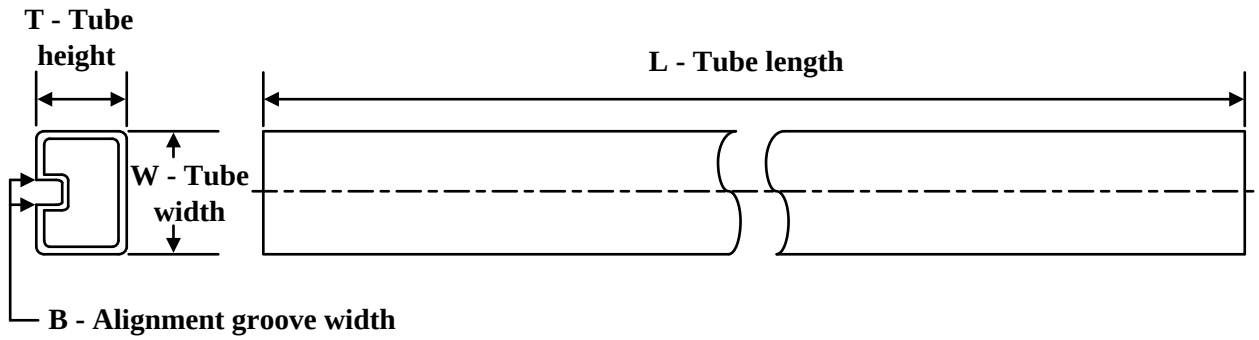
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5018MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LM5018SD/NOPB	WSON	NGU	8	1000	208.0	191.0	35.0
LM5018SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

TUBE

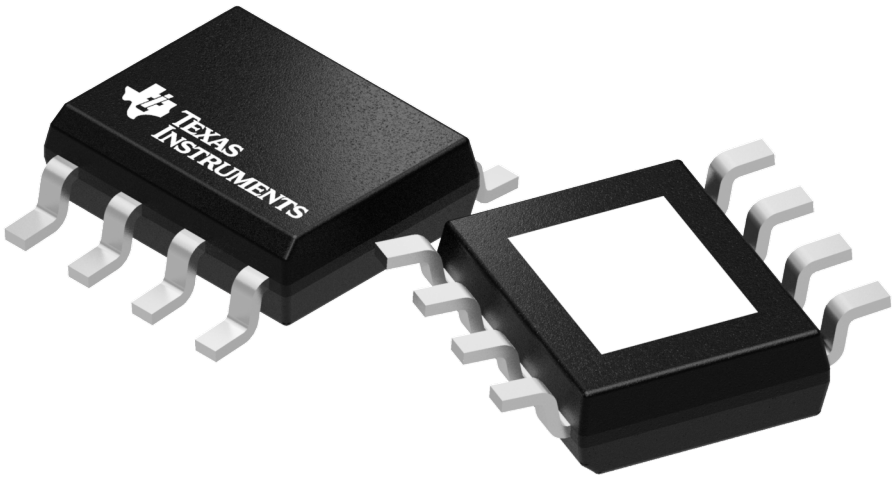


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5018MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM5018MR/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05

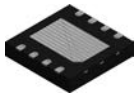
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

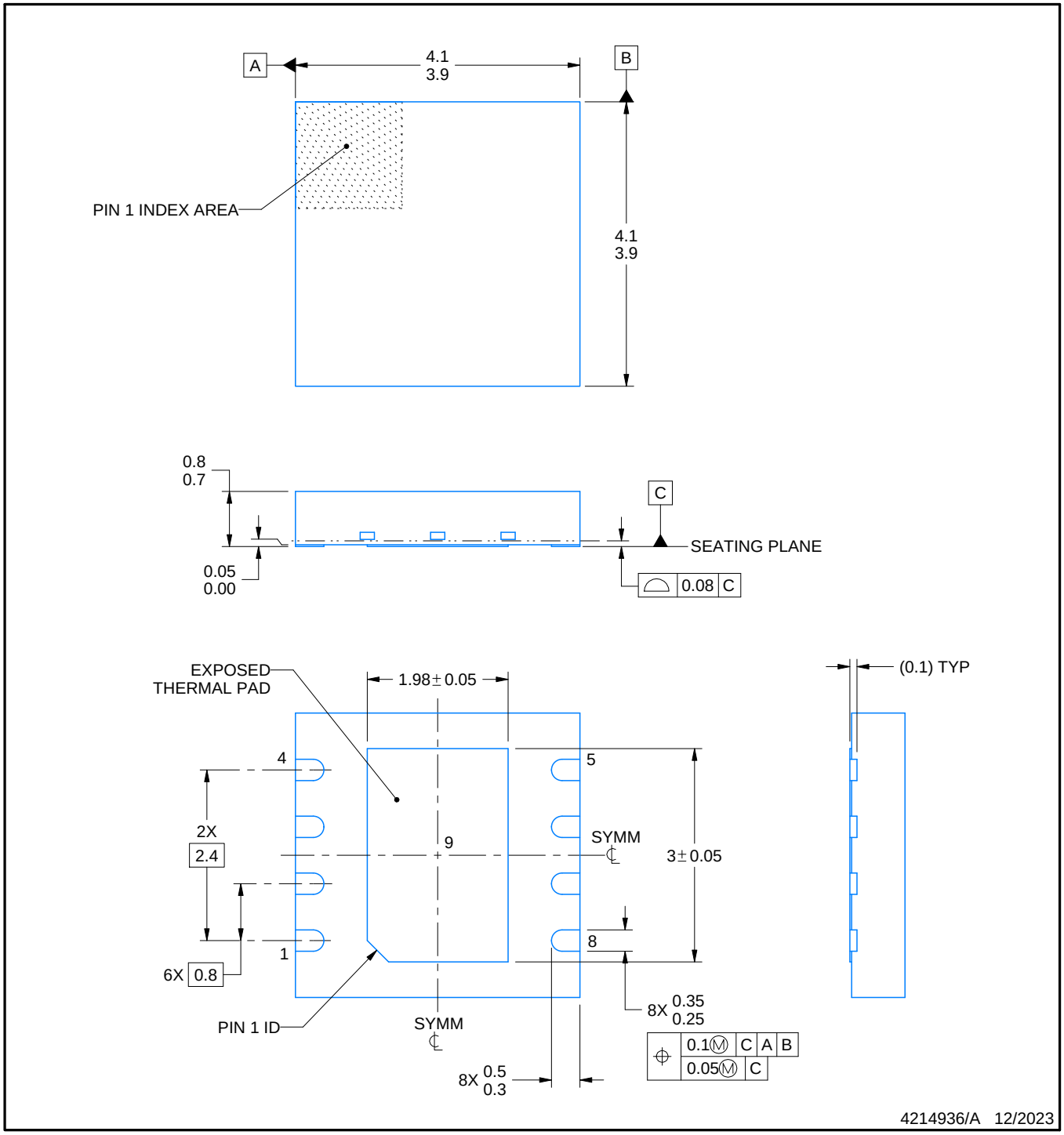
NGU0008B



PACKAGE OUTLINE

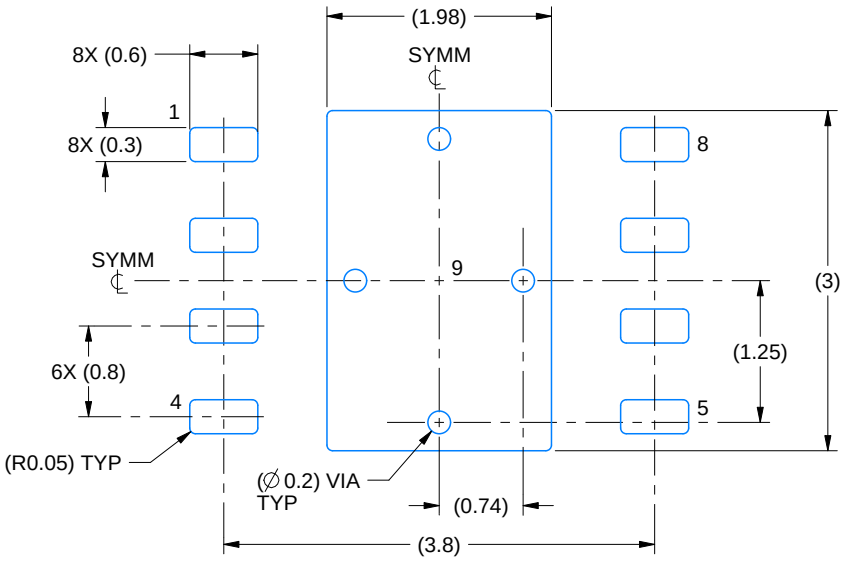
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

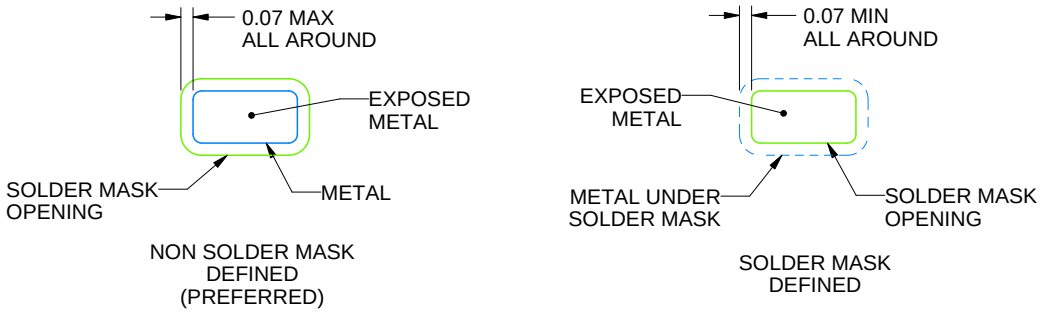


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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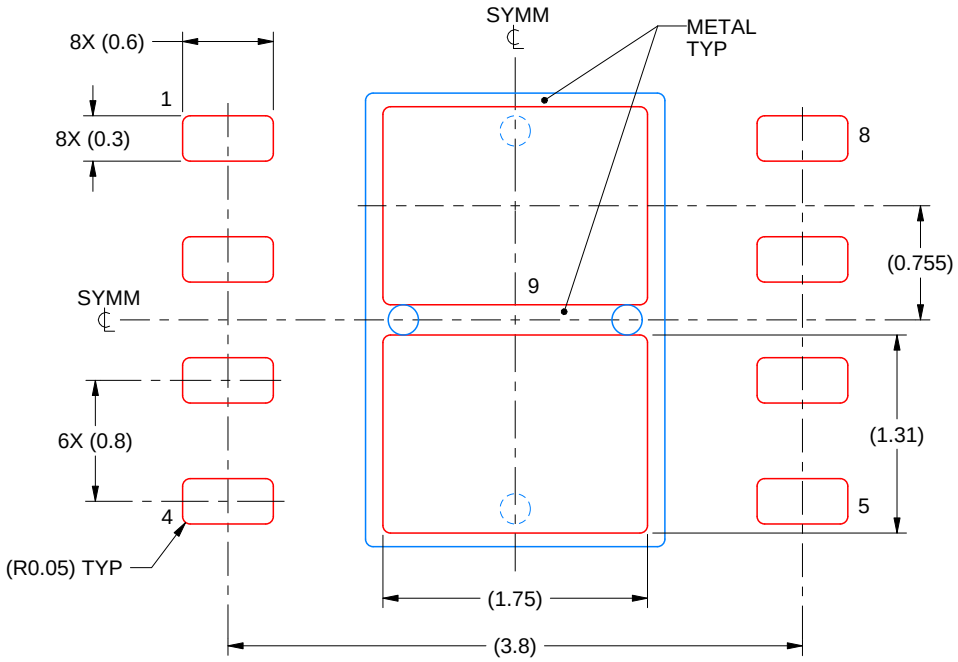
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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