# LM95233 Dual Remote Diode and Local Temperature Sensor with SMBus Interface and TruTherm™ Technology

**Check for Samples: LM95233**

## FEATURES

- **Accurately Senses Die Temperature of 2 Remote ICs or Diode Junctions and Local Temperature**
- **TruTherm BJT Beta Compensation Technology Accurately Senses Sub-Micron Process Thermal Diodes**
- **0.125°C LSb Temperature Resolution**
- **0.03125°C LSb Remote Temperature Resolution with Digital Filter Enabled**
- **+127.875°C/–128°C and 0°C/255°C Remote Ranges**
- **Programmable Digital Filters and Analog Front End Filter**
- **Remote Diode Fault Detection, Model Selection and Offset Correction**
- **Mask and Status Register Support**
- **3 Programmable $\overline{\text{TCRIT}}$ Outputs with Programmable Shared Hysteresis**
- **Programmable Conversion Rate and Shutdown Mode One-Shot Conversion Control**
- **SMBus 2.0 Compatible Interface, Supports TIMEOUT**
- **Three-Level Address Pin**
- **14-Pin WSON Package**

## APPLICATIONS

- **Processor/Computer System Thermal Management (e.g. Laptop, Desktop, Workstations, Server)**
- **Electronic Test Equipment**
- **Office Electronics**

## KEY SPECIFICATIONS

- **Local Temperature Accuracy: ±2.0 °C (max)**
- **Remote Diode Temperature Accuracy: ±0.875 °C (max)**
- **Supply Voltage: 3.0 to 3.6 V**
- **Average Supply Current (1Hz conversion rate): 0.57 mA (typ)**

## DESCRIPTION

LM95233 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of two remote diodes as well as its own temperature. The LM95233 can be used to very accurately monitor the temperature of up to two external devices such as microprocessors, graphics processors or diode-connected 2N3904s. The LM95233's TruTherm™ BJT beta compensation technology allows sensing of 90nm or 65nm process thermal diodes accurately.

The LM95233 reports temperature in two different formats for +127.875°C/–128°C range and 0°C/255°C range. The LM95233 $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ outputs are triggered when any unmasked channel exceeds its corresponding programmable limit and can be used to shutdown the system, to turn on the system fans or as a microcontroller interrupt function. The current status of the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ pins can be read back from the status registers. Mask registers are available for further control of the $\overline{\text{TCRIT}}$ outputs. LM95233's remote temperature channels have programmable digital filters to minimize unwanted $\overline{\text{TCRIT}}$ events when temperature spikes are encountered.

For optimum flexibility and accuracy each LM95233 channel includes, registers for sub-micron process or 2N3904 diode model selection as well as offset correction. A three level address pin allows connection of up to 3 LM95233s to the same SMBus master. The LM95233 includes power saving functions such as: programmable conversion rate, shutdown mode, and turn off of unused channels.

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## Connection Diagram

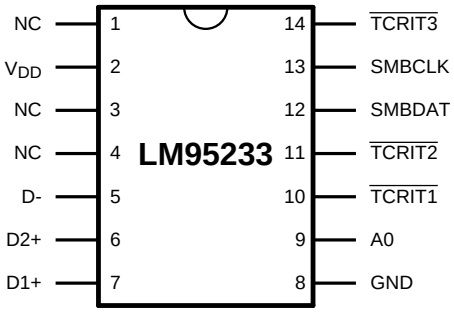
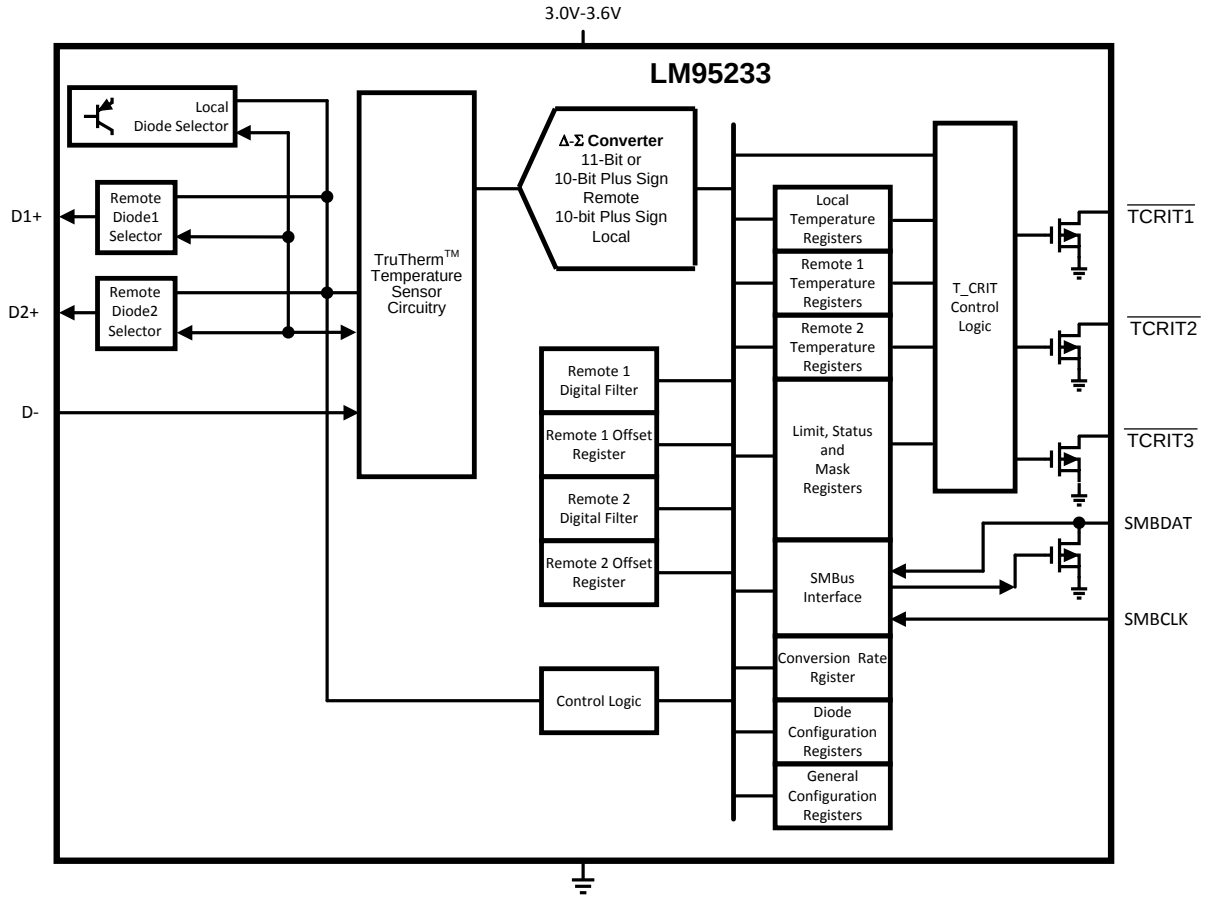



**Figure 1. 14-Lead WSON - TOP VIEW**
**See NHL0014B Package**

## Simplified Block Diagram





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## PIN DESCRIPTIONS

| Label | Pin # | Function | Typical Connection |
|---|---|---|---|
| NC | 1 | No Connect | Not connected. May be left floating, connected to GND or $V_{DD}$. |
| $V_{DD}$ | 2 | Positive Supply Voltage Input | DC Voltage from 3.0 V to 3.6 V. $V_{DD}$ should be bypassed with a 0.1µF capacitor in parallel with 100pF. The 100pF capacitor should be placed as close as possible to the power supply pin. Noise should be kept below 200 mVp-p, a 10 µF capacitor may be required to achieve this. |
| NC | 3 | No Connect | Not connected. May be left floating, connected to GND or $V_{DD}$. |
| NC | 4 | No Connect | Not connected. May be left floating, connected to GND or $V_{DD}$. |
| D− | 5 | Diode Return Current Sink | To all Diode Cathodes. Common D- pin for all two remote diodes. |
| D2+ | 6 | Diode Current Source | To second Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D2+ and D-. A 100 pF capacitor between D2+ and D- can be added and may improve perfomance in noisy systems. Float this pin if this thermal diode is not used. |
| D1+ | 7 | Diode Current Source | To first Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D1+ and D-. A 100 pF capacitor between D1+ and D- can be added and may improve perfomance in noisy systems. Float this pin if this thermal diode is not used. |
| GND | 8 | Power Supply Ground | System low noise ground. |
| A0 | 9 | Digital Input | SMBus slave address select pin. Selects one of three addresses. Can be tied to $V_{DD}$, GND, or to the middle of a resistor divider connected between $V_{DD}$ and GND. |
| $\overline{\text{TCRIT1}}$ | 10 | Digital Output, Open-Drain | Critical temperature output 1. Requires pull-up resistor. Active "LOW". |
| $\overline{\text{TCRIT2}}$ | 11 | Digital Output, Open-Drain | Critical temperature output 2. Requires pull-up resistor. Active "LOW". |
| SMBDAT | 12 | SMBus Bi-Directional Data Line, Open-Drain Output | From and to Controller; may require an external pull-up resistor |
| SMBCLK | 13 | SMBus Clock Input | From Controller; may require an external pull-up resistor |
| $\overline{\text{TCRIT3}}$ | 14 | Digital Output, Open-Drain | Critical temperature output 3. Requires pull-up resistor. Active "LOW". |
| N/A | N/A | Thermal pad | Connect the thermal pad to GND. |

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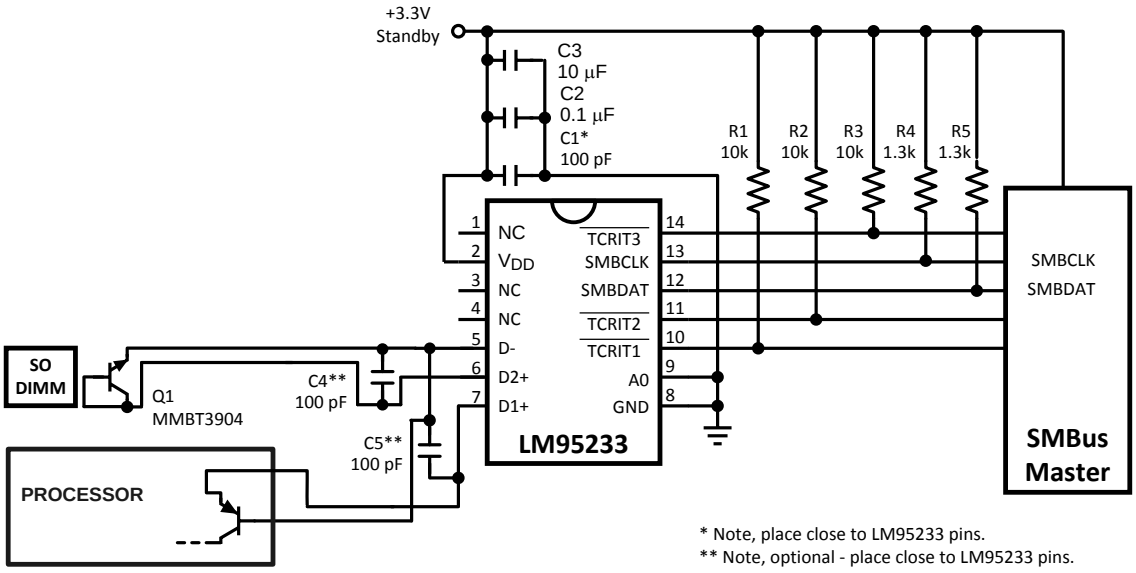
## Typical Application




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)

| | | |
|---|---|---|
| Supply Voltage | | −0.3V to 6.0V |
| Voltage at SMBDAT, SMBCLK, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ | | −0.5V to 6.0V |
| Voltage at Other Pins | | −0.3V to ($V_{DD}$ + 0.3V) |
| D− Input Current | | ±1 mA |
| Input Current at All Other Pins (2) | | ±5 mA |
| Package Input Current (2) | | 30 mA |
| SMBDAT, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ Output Sink Current | | 10 mA |
| Storage Temperature | | −65°C to +150°C |
| ESD Susceptibility (3) | Human Body Model | 2000V |
| | Machine Model | 200V |
| | Charge Device Model | 1000V |
| *Soldering process must comply with Texas Instruments' reflow temperature profile specifications. Refer to* SNOA549 (4) | | |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) When the input voltage ($V_I$) at any pin exceeds the power supplies ($V_I$ < GND or $V_I$ > $V_{DD}$), the current at that pin should be limited to 5 mA. Parasitic components and or ESD protection circuitry are shown in the table below for the LM95233's pins.
(3) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. Charged Device Model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(4) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not.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## Operating Ratings (1) (2) (3)

| | |
|---|---|
| Operating Temperature Range | −40°C to +140°C |
| Electrical Characteristics Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| LM95233CISD | $-40°C \le T_A \le +125°C$ |
| Supply Voltage Range ($V_{DD}$) | +3.0V to +3.6V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(3) Thermal resistance junction-to-ambient when attached to a 4 layer printed circuit board per JEDEC standard JESD51-7
(a) 14-lead WSON = 90°C/W (no thermal vias, no airflow)
(b) 14-lead WSON = 63°C/W (1 thermal via, no airflow)
(c) 14-lead WSON = 43°C/W(6 thermal vias, no airflow)
(d) 14-lead WSON = 31°C/W (6 thermal vias, 900 ln. ft. / min. airflow)
Note, all quoted values include +15% error factor from nominal value.

## Temperature-to-Digital Converter Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{DD}$ = +3.0Vdc to 3.6Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN} \le T_A \le T_{MAX}$; all other limits $T_A = T_J$ = +25°C, unless otherwise noted.**

| Parameter | Conditions | | Typical (1) | Limits (2) | Units (Limit) |
|---|---|---|---|---|---|
| Temperature Error Using Local Diode | $T_A$ = -40°C to +125°C, (3) | | ±1 | **±2** | °C (max) |
| Temperature Error Using Remote Diode (4) | $T_A$ = +25°C to +85°C<br>$T_D$ = +60°C to +100°C | 65 nm Intel Processor | | **±0.875** | °C (max) |
| | $T_A$ = +25°C to +85°C<br>$T_D$ = +60°C to +100°C | MMBT3904 Transistor | | **±1.1** | °C (max) |
| | $T_A$ = +25°C to +85°C<br>$T_D$ = 40°C to +125°C | 65 nm Intel Processor | | **±1.0** | °C (max) |
| | $T_A$ = +25°C to +85°C<br>$T_D$ = −40°C to +125°C | MMBT3904 Transistor | | **±1.3** | °C (max) |
| | $T_A$ = −40°C to +85°C<br>$T_D$ = −40°C to +125°C | 65 nm Intel Processor | | **±3.2** | °C (max) |
| | $T_A$ = −40°C to +85°C<br>$T_D$ = −40°C to +125°C | MMBT3904 Transistor | | **±3.0** | °C (max) |
| | $T_A$ = −40°C to +85°C<br>$T_D$ = 125°C to +140°C | MMBT3904 Transistor | | **±3.3** | °C (max) |
| Local Diode Measurement Resolution | | | 11 | | Bits |
| | | | 0.125 | | °C |
| Remote Diode Measurement Resolution | Digital Filter Off | | 11 | | Bits |
| | | | 0.125 | | °C |
| | Digital Filter On (Remote Diodes 1 and 2 only) | | 13 | | Bits |
| | | | 0.03125 | | °C |
| Conversion Time of All Temperatures at the Fastest Setting (5) | All Channels are Enabled in Default State | | 1100 | **1210** | ms (max) |
| | 1 External Channel TruTherm Active | | 34 | **37** | ms (max) |
| | 1 External Channel TruTherm Inactive | | 31 | **34** | ms (max) |
| | Local only | | 30 | **33** | ms (max) |

(1) Typicals are at $T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM95233 and the thermal resistance. See Note 2 of the Operating Ratings Table above for the thermal resistance to be used in the self-heating calculation.
(4) The accuracy of the LM95233CISD is ensured when using a typical thermal diode of an Intel processor on a 65 nm process or an MMBT3904 diode-connected transistor, as selected in the Remote Diode Model Select register. See Typical Performance Characteristics for performance with Intel processor on a 90 nm process. For further information on other thermal diodes see DIODE NON-IDEALITY
(5) This specification is provided only to indicate how often temperature data is updated. The LM95233 can be read at any time without regard to conversion state (and will yield last conversion result).

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## Temperature-to-Digital Converter Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{DD}$ = +3.0Vdc to 3.6Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN} \leq T_A \leq T_{MAX}$;** all other limits $T_A = T_J$ = +25°C, unless otherwise noted.

| Parameter | Conditions | Typical(1) | Limits(2) | Units (Limit) |
|---|---|---|---|---|
| Quiescent Current (6) | SMBus Inactive, 1Hz Conversion Rate, channels in default state | 570 | **800** | µA (max) |
| | Shutdown | 360 | | µA |
| D− Source Voltage | | 0.4 | | V |
| Remote Diode Source Current | High level | 160 | **230** | µA (max) |
| | Low level | 10 | | |
| Power-On Reset Threshold | Measured on $V_{DD}$ input, falling edge | | **2.8**<br>**1.6** | V (max)<br>V (min) |
| $\overline{\text{TCRIT1}}$ Pin Temperature Threshold | Default Diodes only | +110 | | °C |
| $\overline{\text{TCRIT2}}$ Pin Temperature Threshold | Default all channels | +85 | | °C |

(6) Quiescent current will not increase substantially with an SMBus communication.

## Logic Electrical Characteristics

### DIGITAL DC CHARACTERISTICS

Unless otherwise noted, these specifications apply for $V_{DD}$ = +3.0Vdc to 3.6Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$=+25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Typical(1) | Limits(2) | Units (Limit) |
|---|---|---|---|---|---|
| **SMBDAT, SMBCLK INPUTS** | | | | | |
| $V_{IN(1)}$ | Logical “1” Input Voltage | | | **2.1** | V (min) |
| $V_{IN(0)}$ | Logical “0”Input Voltage | | | **0.8** | V (max) |
| $V_{IN(HYST)}$ | SMBDAT and SMBCLK Digital Input Hysteresis | | 400 | | mV |
| $I_{IN(1)}$ | Logical “1” Input Current | $V_{IN} = V_{DD}$ | 0.005 | **10** | µA (max) |
| $I_{IN(0)}$ | Logical “0” Input Current | $V_{IN}$ = 0V | −0.005 | **-10** | µA (max) |
| $C_{IN}$ | Input Capacitance | | 5 | | pF |
| **A0 DIGITAL INPUT** | | | | | |
| $V_{IH}$ | Input High Voltage | | | **0.90 × $V_{DD}$** | V (min) |
| $V_{IM}$ | Input Middle Voltage | | | **0.57 × $V_{DD}$** | V (max) |
| | | | | **0.43 × $V_{DD}$** | V (min) |
| $V_{IL}$ | Input Low Voltage | | | **0.10 × $V_{DD}$** | V (max) |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{IN} = V_{DD}$ | −0.005 | **−10** | µA (min) |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{IN}$ = 0V | 0.005 | **10** | µA (max) |
| $C_{IN}$ | Input Capacitance | | 5 | | pF |
| **SMBDAT, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ DIGITAL OUTPUTS** | | | | | |
| $I_{OH}$ | High Level Output Current | $V_{OH} = V_{DD}$ | | **10** | µA (max) |
| $V_{OL(SMBDAT)}$ | SMBus Low Level Output Voltage | $I_{OL}$ = 4 mA<br>$I_{OL}$ = 6 mA | | **0.4**<br>**0.6** | V (max)<br>V (max) |
| $V_{OL(\overline{TCRIT})}$ | $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ Low Level Output Voltage | $I_{OL}$= 6 mA | | **0.4** | V (max) |
| $C_{OUT}$ | Digital Output Capacitance | | 5 | | pF |

(1) Typicals are at $T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).


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## SMBus DIGITAL SWITCHING CHARACTERISTICS

Unless otherwise noted, these specifications apply for $V_{DD}$=+3.0 Vdc to +3.6 Vdc, $C_L$ (load capacitance) on output lines = 80 pF. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = +25°C, unless otherwise noted.
The switching characteristics of the LM95233 fully meet or exceed the published specifications of the SMBus version 2.0. The following parameters are the timing relationships between SMBCLK and SMBDAT signals related to the LM95233. They adhere to but are not necessarily the SMBus bus specifications.

| Symbol | Parameter | Conditions | Typical (1) | Limits (2) | Units (Limit) |
|---|---|---|---|---|---|
| $f_{SMB}$ | SMBus Clock Frequency | | | **100**<br>**10** | kHz (max)<br>kHz (min) |
| $t_{LOW}$ | SMBus Clock Low Time | from $V_{IN(0)}$max to $V_{IN(0)}$max | | **4.7**<br>**25** | µs (min)<br>ms (max) |
| $t_{HIGH}$ | SMBus Clock High Time | from $V_{IN(1)}$min to $V_{IN(1)}$min | | **4.0** | µs (min) |
| $t_{R,SMB}$ | SMBus Rise Time | (3) | 1 | | µs (max) |
| $t_{F,SMB}$ | SMBus Fall Time | (4) | 0.3 | | µs (max) |
| $t_{OF}$ | Output Fall Time | $C_L$ = 400 pF,<br>$I_O$ = 3 mA, (4) | | **250** | ns (max) |
| $t_{TIMEOUT}$ | SMBDAT and SMBCLK Time Low for Reset of Serial Interface (5) | | | **25**<br>**35** | ms (min)<br>ms (max) |
| $t_{SU;DAT}$ | Data In Setup Time to SMBCLK High | | | **250** | ns (min) |
| $t_{HD;DAT}$ | Data Out Stable after SMBCLK Low | | | **300**<br>**1075** | ns (min)<br>ns (max) |
| $t_{HD;STA}$ | Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first clock falling edge) | | | **100** | ns (min) |
| $t_{SU;STO}$ | Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup) | | | **100** | ns (min) |
| $t_{SU;STA}$ | SMBus Repeated Start-Condition Setup Time, SMBCLK High to SMBDAT Low | | | **0.6** | µs (min) |
| $t_{BUF}$ | SMBus Free Time Between Stop and Start Conditions | | | **1.3** | µs (min) |

(1) Typicals are at $T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) The output rise time is measured from ($V_{IN(0)}$max − 0.15V) to ($V_{IN(1)}$min + 0.15V).
(4) The output fall time is measured from ($V_{IN(1)}$min + 0.15V) to ($V_{IN(0)}$max − 0.15V).
(5) Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the LM95233's SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

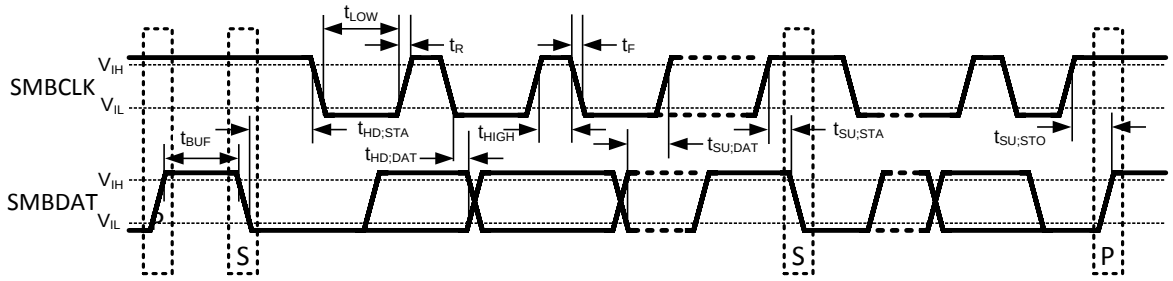
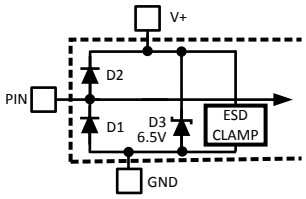
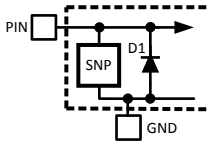



**Figure 2. SMBus Communication**

| Pin # | Label | Circuit | Circuits for Pin ESD Protection Structure |
|---|---|---|---|
| 1 | NC | – |   Figure 3. Circuit A |
| 2 | $V_{DD}$ | A | |
| 3 | NC | – | |
| 4 | NC | – | |
| 5 | D- | A | |
| 6 | D2+ | A | |
| 7 | D1+ | A | |
| 8 | GND | – |   Figure 4. Circuit B |
| 9 | A0 | B | |
| 10 | $\overline{\text{TCRIT1}}$ | B | |
| 11 | $\overline{\text{TCRIT2}}$ | B | |
| 12 | SMBDAT | B | |
| 13 | SMBCLK | B | |
| 14 | $\overline{\text{TCRIT2}}$ | B | |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## Typical Performance Characteristics

**Conversion Rate Effect on Average Power Supply Current**

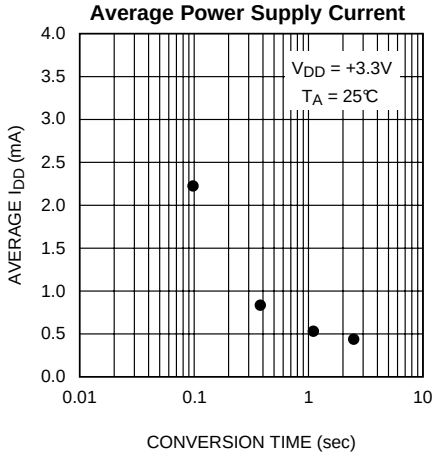


**Figure 5.**

**Thermal Diode Capacitor or PCB Leakage Current Effect on Remote Diode Temperature Reading**

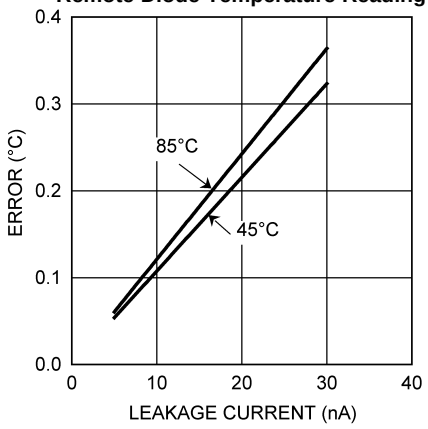


**Figure 6.**

**Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance, TruTherm Disabled**

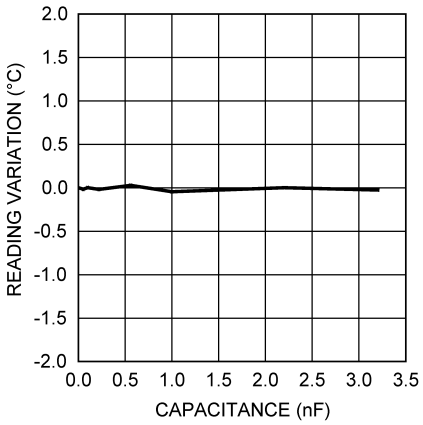


**Figure 7.**

**Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance, TruTherm Enabled**

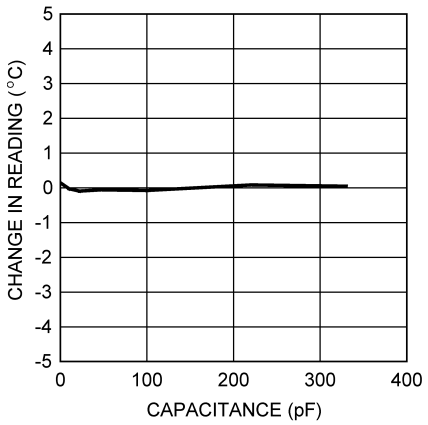


**Figure 8.**

**Intel Processor on 65 nm Process or 90 nm Process Thermal Diode Performance Comparison**

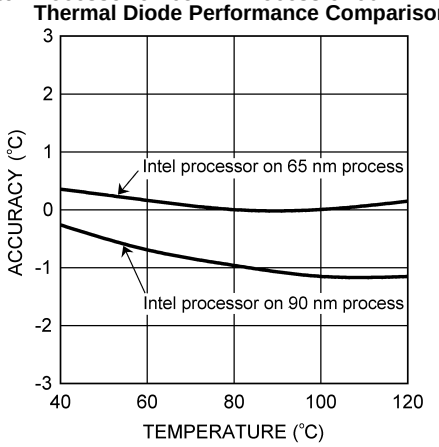


**Figure 9.**

## FUNCTIONAL DESCRIPTION

LM95233 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of two remote diodes as well as its own temperature. The LM95233 can be used to very accurately monitor the temperature of up to two external devices such as microprocessors, graphics processors or diode-connected 2N3904 transistor. The LM95233 includes TruTherm BJT beta compensation technology that allows sensing of Intel processors 90 nm or 65 nm process thermal diodes accurately.

The LM95233 reports temperature in two different formats for +127.875°C/–128°C range and 0°C/255°C range. The LM95233 has a Sigma-Delta ADC (Analog-to-Digital Converter) core which provides the first level of noise imunity. For improved performance in a noisy environment the LM95233 includes programmable digital filters for Remote Diode 1 and 2 temperature readings. When the digital filters are invoked the resolution for Remote Diode 1 and 2 readings increases to 0.03125°C. The LM95233 contains a diode model selection register that includes bits for each channel that select between thermal diodes of Intel processors on 65 nm process or 2N3904s. For maximum flexibility and best accuracy the LM95233 includes offset registers that allow calibration of other diode types.

Diode fault detection circuitry in the LM95233 can detect the absence or fault state of a remote diode: whether D+ is shorted to $V_{DD}$, D- or ground, or whether D+ is floating.

The LM95233 $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ active low outputs are triggered when any unmasked channel exceeds its corresponding programmable limit and can be used to shutdown the system, to turn on the system fans or as a microcontroller interrupt function. The current status of the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ pins can be read back from the status registers via the SMBus interface. The remote channels have two separate limits each that control the $\overline{\text{TCRIT1}}$ and $\overline{\text{TCRIT2}}$ pins. The $\overline{\text{TCRIT3}}$ pin shares the limits of the $\overline{\text{TCRIT2}}$ pin but allows for different masking options. All limits have a shared programmable hysteresis register.

Remote Diode temperature channels have programmable digital filters in order to avoid false triggering the $\overline{\text{TCRIT}}$ pins.

LM95233 has a three-level address pin to connect up to 3 devices to the same SMBus master. LM95233 also has programmable conversion rate register as well as a shutdown mode for power savings. One round of conversions can be triggered in shutdown mode by writing to the one-shot register through the SMBus interface. LM95233 can be programmed to turn off unused channels for more power savings.

The LM95233 register set has an 8-bit data structure and includes:

1. Temperature Value Registers with signed format
   - Most-Significant-Byte (MSB) and Least-Significant-Byte (LSB) Local Temperature
   - MSB and LSB Remote Temperature 1
   - MSB and LSB Remote Temperature 2
2. Temperature Value Registers with unsigned format
   - MSB and LSB Remote Temperature 1
   - MSB and LSB Remote Temperature 2
3. Diode Configuration Registers
   - Diode Model Select
   - Remote 1 Offset
   - Remote 2 Offset
4. General Configuration Registers
   - Configuration (Standby, Conversion Rate)
   - Channel Conversion Enable
   - Filter Setting for Remote 1 and 2
   - 1-Shot
5. Status Registers
   - Main Status Register (Busy bit, Not Ready, Status Register 1 to 4 Flags)
   - Status 1 (diode fault)
   - Status 2 (TCRIT1)
   - Status 3 (TCRIT2)


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- Status 4 (TCRIT3)
- Diode Model Status

6. Mask Registers
   - TCRIT1 Mask
   - TCRIT2 Mask
   - TCRIT3 Mask
7. Limit Registers
   - Local Tcrit Limit
   - Remote 1 Tcrit-1 Limit
   - Remote 2 Tcrit-1 Limit
   - Remote 1 Tcrit-2 and Tcrit-3 Limit
   - Remote 2 Tcrit-2 and Tcrit-3 Limit
   - Common Tcrit Hysteresis
8. Manufacturer ID Register
9. Revision ID Register

## CONVERSION SEQUENCE

The LM95233 takes approximately 95 ms to convert the Local Temperature, Remote Temperatures 1 and 2, and to update all of its registers. These conversions for each thermal diode are addressed in a round robin sequence. Only during the conversion process the busy bit (D7) in Status register (02h) is high. The conversion rate may be modified by the Conversion Rate bits found in the Configuration Register (03h). When the conversion rate is modified a delay is inserted between each round of conversions, the actual time for each round remains at 95 ms (typical all channels enabled). The time a round takes depends on the number of channels that are on. Different conversion rates will cause the LM95233 to draw different amounts of average supply current as shown in Figure 10. This curve assumes all the channels are on. If channels are turned off the average current will drop since the round robin time will decrease and the shutdown time will increase during each conversion interval.

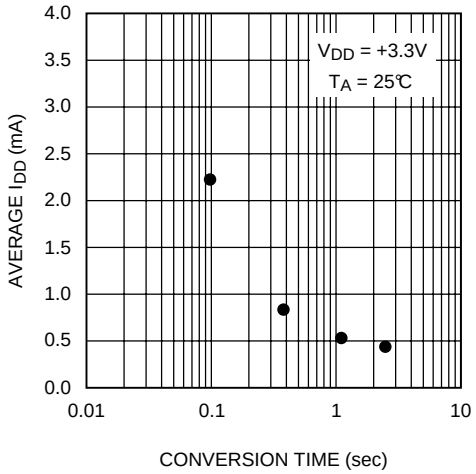


**Figure 10. Conversion Rate Effect on Power Supply Current**

## POWER-ON-DEFAULT STATES

LM95233 always powers up to these known default states. The LM95233 remains in these states until after the first conversion.

1. All Temperature readings set to 0°C until the end of the first conversion
2. Diode Model Select: Remote 1 set to 65 nm Intel processor, Remote 2 set to MMBT3904
3. Remote offset for all channels 0°C
4. Configuration: Active converting

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5. Continuous conversion with all channels enabled, time = 1s
6. Enhanced digital filter enabled for Remote 1 and 2
7. Status Registers depends on state of thermal diode inputs
8. Local and Remote Temperature Limits for $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ outputs:

| Output Pin | Temperature Channel Limit | | |
|---|---|---|---|
| | Remote 2 (°C) | Remote 1 (°C) | Local (°C) |
| $\overline{\text{TCRIT1}}$ | 110 | 110 | Masked, 85 |
| $\overline{\text{TCRIT2}}$ | 85 | 85 | 85 |
| $\overline{\text{TCRIT3}}$ | Masked, 85 | Masked, 85 | Masked, 85 |

1. Manufacturers ID set to 01h
2. Revision ID set to 79h

## SMBus INTERFACE

The LM95233 operates as a slave on the SMBus, so the SMBCLK line is an input and the SMBDAT line is bidirectional. The LM95233 never drives the SMBCLK line and it does not support clock stretching. According to SMBus specifications, the LM95233 has a 7-bit slave address. Three SMBus device address can be selected by connecting A0 (pin 6) to either Low, Mid-Supply or High voltages. The LM95233 has the following SMBus slave address:

| A0 Pin State | SMBus Device Address A[6:0] | |
|---|---|---|
| | Hex | Binary |
| Low | 18h | 001 1000 |
| Mid-Supply | 2Ah | 010 1010 |
| High | 2Bh | 010 1011 |

## TEMPERATURE CONVERSION SEQUENCE

Each of the3 temperature channels of LM95233 can be turned OFF independent from each other via the Channel Enable Register. Turning off unused channels will increase the conversion speed in the fastest conversion speed mode. If the slower conversion speed settings are used, disabling unused channels will reduce the average power consumption of LM95233.

## DIGITAL FILTER

In order to suppress erroneous remote temperature readings due to noise as well as increase the resolution of the temperature, the LM95233 incorporates a digital filter for Remote 1 and 2 Temperature Channels. When a filter is enabled the filtered readings are used for the TCRIT comparisons. There are two possible digital filter settings that are enabled through the Filter Setting Register at register address 0Fh. The filter for each channel can be set according to the following table:

| R1F[1:0] or R2F[1:0] | | Filter Setting |
|---|---|---|
| 0 | 0 | No Filter |
| 0 | 1 | Filter (equivalent to Level 2 filter of the LM86/LM89) |
| 1 | 0 | Reserved |
| 1 | 1 | Enhanced Filter (Filter with transient noise clipping) |


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Figure 11 describes the filter output in response to a step input and an impulse input.

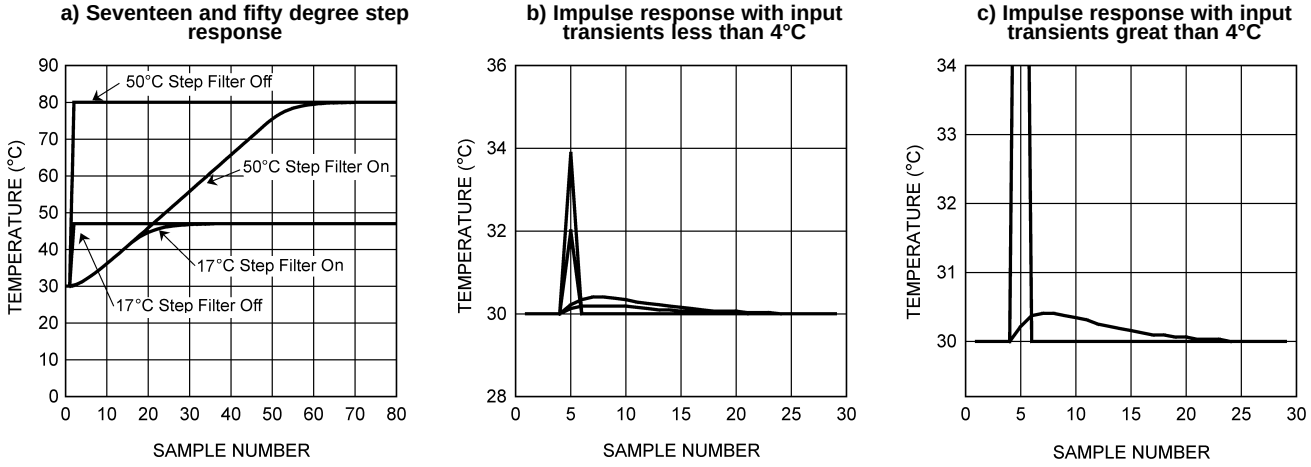


**Figure 11. Filter Impulse and Step Response Curves**

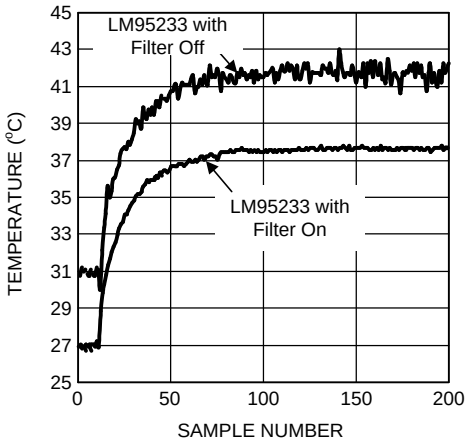


**Figure 12. Digital Filter Response in a typical Intel processor on a 65 nm or 90 nm process**

The filter curves were purposely offset for clarity.Figure 12 shows the filter in use in a typical Intel processor on a 65/90 nm process system. Note that the two curves have been purposely offset for clarity. Inserting the filter does not induce an offset as shown.

## TEMPERATURE DATA FORMAT

Temperature data can only be read from the Local and Remote Temperature value registers. The data format for all temperature values is left justified 16-bit word available in two 8-bit registers. Unused bits will always report "0". All temperature data is clamped and will not roll over when a temperature exceeds full-scale value.

Remote temperature data for all channels can be represented by an 11-bit, two's complement word or unsigned binary word with an LSb (Least Significant Bit) equal to 0.125°C.

**Table 1. 11-bit, 2's Complement (10-bit plus sign)**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +125°C | 0111 1101 0000 0000 | 7D00h |
| +25°C | 0001 1001 0000 0000 | 1900h |
| +1°C | 0000 0001 0000 0000 | 0100h |
| +0.125°C | 0000 0000 0010 0000 | 0020h |

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**Table 1. 11-bit, 2's Complement (10-bit plus sign) (continued)**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| 0°C | 0000 0000 0000 0000 | 0000h |
| −0.125°C | 1111 1111 1110 0000 | FFE0h |
| −1°C | 1111 1111 0000 0000 | FF00h |
| −25°C | 1110 0111 0000 0000 | E700h |
| −55°C | 1100 1001 0000 0000 | C900h |

**Table 2. 11-bit, Unsigned Binary**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +255.875°C | 1111 1111 1110 0000 | FFE0h |
| +255°C | 1111 1111 0000 0000 | FF00h |
| +201°C | 1100 1001 0000 0000 | C900h |
| +125°C | 0111 1101 0000 0000 | 7D00h |
| +25°C | 0001 1001 0000 0000 | 1900h |
| +1°C | 0000 0001 0000 0000 | 0100h |
| +0.125°C | 0000 0000 0010 0000 | 0020h |
| 0°C | 0000 0000 0000 0000 | 0000h |

When the digital filter is enabled on Remote 1 and 2 channels temperature data is represented by a 13-bit unsigned binary or 12-bit plus sign (two's complement) word with an LSb equal to 0.03125°C.

**Table 3. 13-bit, 2's Complement (12-bit plus sign)**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +125°C | 0111 1101 0000 0000 | 7D00h |
| +25°C | 0001 1001 0000 0000 | 1900h |
| +1°C | 0000 0001 0000 0000 | 0100h |
| +0.03125°C | 0000 0000 0000 1000 | 0008h |
| 0°C | 0000 0000 0000 0000 | 0000h |
| −0.03125°C | 1111 1111 1111 1000 | FFF8h |
| −1°C | 1111 1111 0000 0000 | FF00h |
| −25°C | 1110 0111 0000 0000 | E700h |
| −55°C | 1100 1001 0000 0000 | C900h |

**Table 4. 13-bit, Unsigned Binary**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +255.875°C | 1111 1111 1110 0000 | FFE0h |
| +255°C | 1111 1111 0000 0000 | FF00h |
| +201°C | 1100 1001 0000 0000 | C900h |
| +125°C | 0111 1101 0000 0000 | 7D00h |
| +25°C | 0001 1001 0000 0000 | 1900h |
| +1°C | 0000 0001 0000 0000 | 0100h |
| +0.03125°C | 0000 0000 0000 1000 | 0008h |
| 0°C | 0000 0000 0000 0000 | 0000h |


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Local Temperature data is only represented by an 11-bit, two's complement, word with an LSb equal to 0.125°C.

**Table 5. 11-bit, 2's Complement (10-bit plus sign)**

| Temperature | Digital Output | |
|---|---|---|
| | Binary | Hex |
| +125°C | 0111 1101 0000 0000 | 7D00h |
| +25°C | 0001 1001 0000 0000 | 1900h |
| +1°C | 0000 0001 0000 0000 | 0100h |
| +0.125°C | 0000 0000 0010 0000 | 0020h |
| 0°C | 0000 0000 0000 0000 | 0000h |
| −0.125°C | 1111 1111 1110 0000 | FFE0h |
| −1°C | 1111 1111 0000 0000 | FF00h |
| −25°C | 1110 0111 0000 0000 | E700h |
| −55°C | 1100 1001 0000 0000 | C900h |

## SMBDAT OPEN-DRAIN OUTPUT

The SMBDAT output is an open-drain output and does not have internal pull-ups. A “high” level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible without effecting the SMBus desired data rate. This will minimize any internal temperature reading errors due to internal heating of the LM95233. The maximum resistance of the pull-up to provide a 2.1V high level, based on LM95233 specification for High Level Output Current with the supply voltage at 3.0V, is 82 kΩ (5%) or 88.7 kΩ (1%).

## $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, AND $\overline{\text{TCRIT3}}$ OUTPUTS

The LM95233's $\overline{\text{TCRIT}}$ pins are active-low open-drain outputs and do not include internal pull-up resistors. A “high” level will not be observed on these pins until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible without effecting the performance of the device receiving the signal. This will minimize any internal temperature reading errors due to internal heating of the LM95233. The maximum resistance of the pull-up to provide a 2.1V high level, based on LM95233 specification for High Level Output Current with the supply voltage at 3.0V, is 82 kΩ (5%) or 88.7 kΩ (1%). The three $\overline{\text{TCRIT}}$ pins can each sink 6 mA of current and still ensure a "Logic Low" output voltage of 0.4V. If all three pins are set at maximum current this will cause a power dissipation of 7.2 mW. This power dissipation combined with a thermal resistance of 77.8°C/W will cause the LM95233's junction temperature to rise approximately 0.6°C and thus cause the Local temperature reading to shift. This can only be cancelled out if the environment that the LM95233 is enclosed in has stable and controlled air flow over the LM95233, as airflow can cause the thermal resistance to change dramatically.

## TCRIT LIMITS AND $\overline{\text{TCRIT}}$ OUTPUTS

Figure 13 describes a simplified diagram of the temperature comparison and status register logic. Figure 14 describes a simplified logic diagram of the circuitry associated with the status registers, mask registers and the $\overline{\text{TCRIT}}$ output pins.

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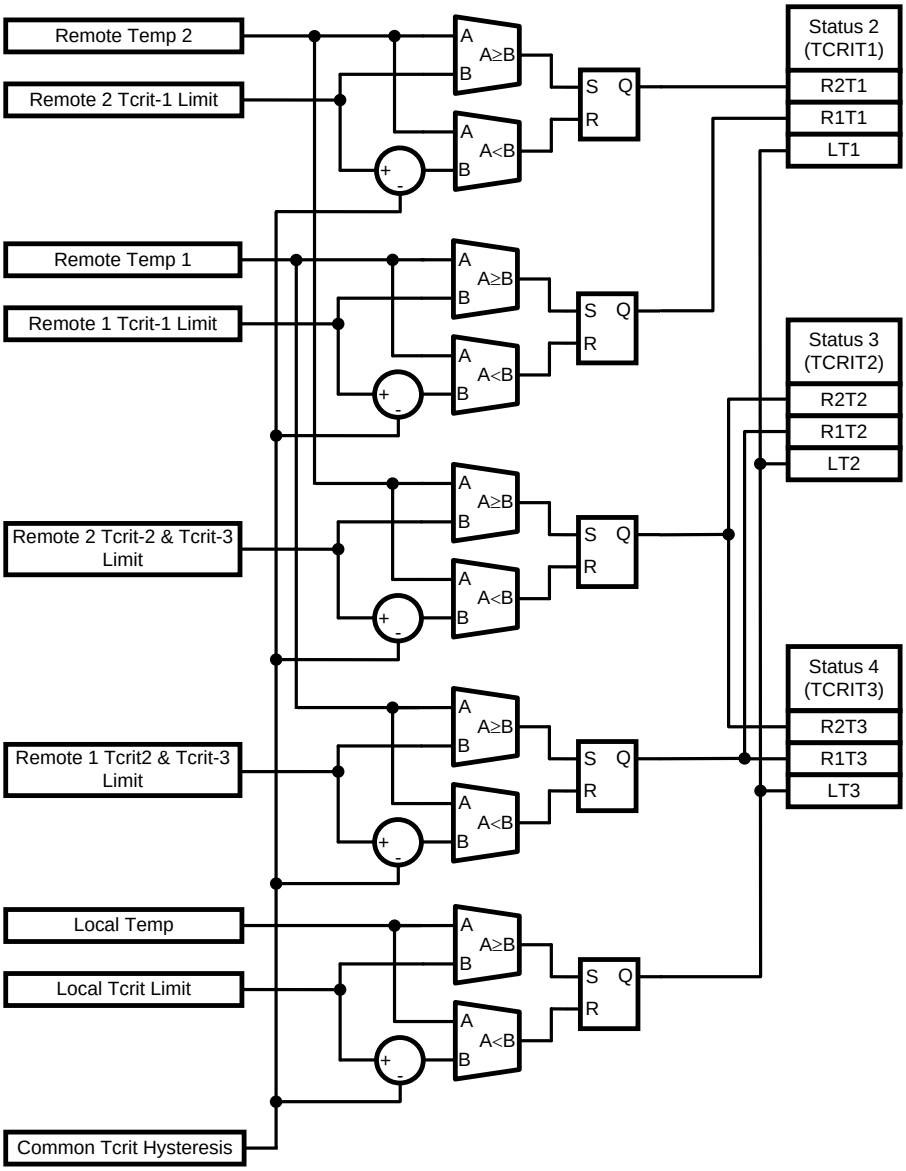


**Figure 13. Temperature Comparison Logic and Status Register Simplified Diagram**


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a) $\overline{\text{TCRIT1}}$ Mask Register, Status Register 1 and 2, and $\overline{\text{TCRIT1}}$ output logic diagram.

b) $\overline{\text{TCRIT2}}$ Mask Register, Status Register 1 and 3, and $\overline{\text{TCRIT2}}$ output logic diagram.

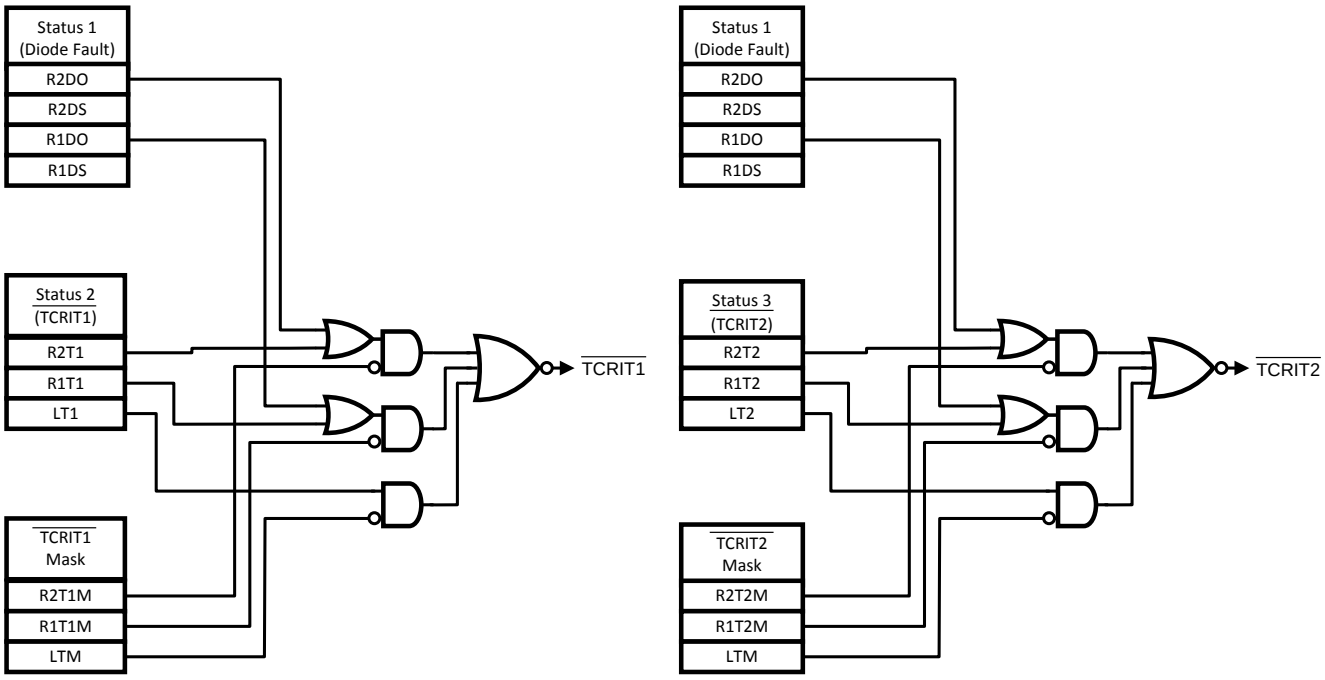
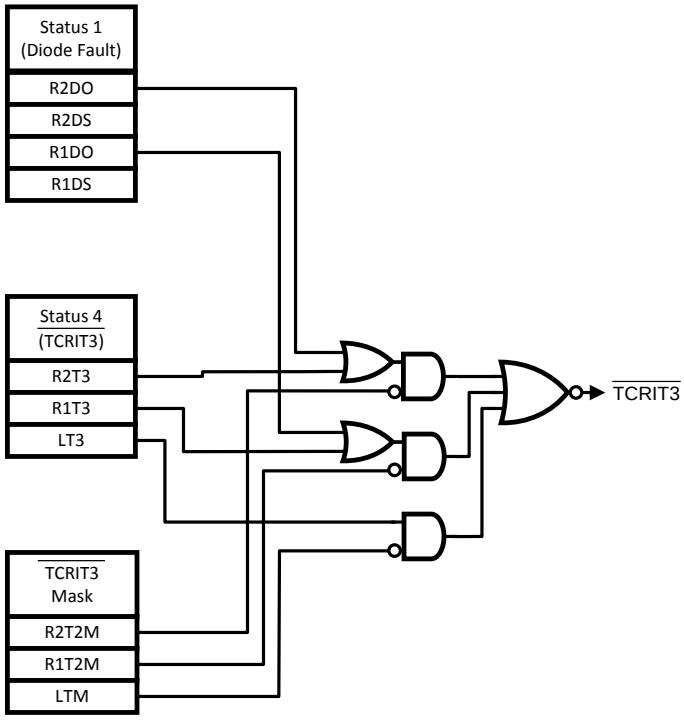



**Figure 14. Logic diagrams for the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ outputs**

c) $\overline{\text{TCRIT3}}$ Mask Register, Status Register 1 and 4, and $\overline{\text{TCRIT3}}$ output logic diagram.




If enabled, local temperature is compared to the user programmable Local Tcrit Limit Register (Default Value = 85°C). The result of this comparison is stored in Status Register 2, Status Register 3 and Status Register 4 (see Figure 13).The comparison result can trigger $\overline{\text{TCRIT1}}$ pin, $\overline{\text{TCRIT2}}$ pin or $\overline{\text{TCRIT3}}$ pin depending on the settings in the TCRIT1 Mask, TCRIT2 Mask and TCRIT3 Mask Registers (see Figure 14). The comparison result can also be read back from the Status Register 2, Status Register 3 and Status Register 4.

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If enabled, remote temperature 1 is compared to the user programmable Remote 1 Tcrit-1 Limit Register (Default Value 110°C) and Remote 1 Tcrit-2 Limit Register (Default Value = 85°C). The result of this comparison is stored in Status Register 2, Status Register 3 and Status Register 4 (see Figure 13). The comparison result can trigger $\overline{\text{TCRIT1}}$ pin, $\overline{\text{TCRIT2}}$ pin or $\overline{\text{TCRIT3}}$ pin depending on the settings in the $\overline{\text{TCRIT1}}$ Mask, $\overline{\text{TCRIT2}}$ Mask and $\overline{\text{TRCIT3}}$ Mask Registers (see Figure 14). The comparison result can also be read back from the Status Register 2, Status Register 3 and Status Register 4. The remote temperature 2 operates in a similar manner to remote temperature 1 using its associated user programmable limit registers: Remote 2 Tcrit-1 Limit Register (Default Value 110°C) and Remote 2 Tcrit-2 Limit Register (Default Value = 85°C).

**Table 6. Limit assignments for each $\overline{\text{TCRIT}}$ output pin:**

| | $\overline{\text{TCRIT1}}$ | $\overline{\text{TCRIT2}}$ | $\overline{\text{TCRIT3}}$ |
|---|---|---|---|
| **Remote 2** | Remote 2<br>Tcrit-1 Limit | Remote 2<br>Tcrit-2 Limit | Remote 2<br>Tcrit-2 Limit |
| **Remote 1** | Remote 1<br>Tcrit-1 Limit | Remote 1<br>Tcrit-2 Limit | Remote 1<br>Tcrit-2 Limit |
| **Local** | Local<br>Tcrit Limit | Local<br>Tcrit Limit | Local<br>Tcrit Limit |

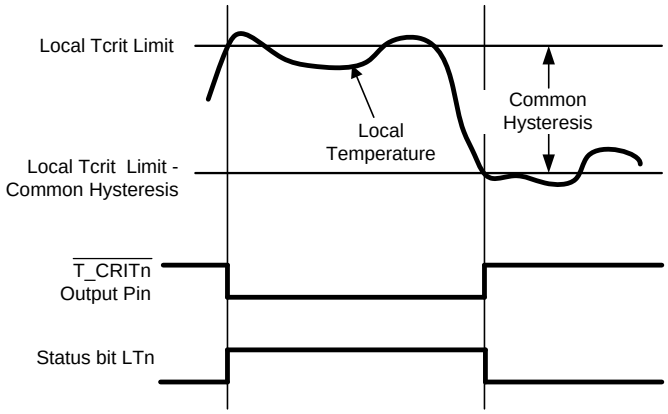


**Figure 15. TCRIT response diagram (masking options not included)**

The TCRIT response diagram of Figure 15 shows the local temperature interaction with the Tcrit limit and hysteresis value. As can be seen in the diagram when the local temperature exceeds the Tcrit limit register value the LTn Status bit is set and the $\overline{\text{T_CRITn}}$ output(s) is/are activated. The Status bit(s) and outputs are not deactivated until the temperature goes below the value calculated by subtracting the Common Hysteresis value programmed from the limit. This diagram mainly shows an example function of the hysteresis and is not meant to show complete function of the possible settings and options of all the TCRIT outputs and limit values.

## DIODE FAULT DETECTION

The LM95233 is equipped with operational circuitry designed to detect fault conditions concerning the remote diodes. In the event that the D+ pin is detected as shorted to GND, D−, $V_{DD}$ or D+ is floating, the Remote Temperature reading is –128.000 °C if signed format is selected and 0 °C if unsigned format is selected. In addition, the appropriate status register bits RD1M or RD2M (D1 or D0) are set.

## COMMUNICATING WITH THE LM95233

The data registers in the LM95233 are selected by the Command Register. At power-up the Command Register is set to “00”, the location for the Read Local Temperature Register. The Command Register latches the last location it was set to. Each data register in the LM95233 falls into one of three types of user accessibility:

1. Read only
2. Write only
3. Write/Read same address


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A **Write** to the LM95233 will always include the address byte and the command byte. A write to any register requires one data byte.

**Reading** the LM95233 can take place either of two ways:

1. If the location latched in the Command Register is correct (most of the time it is expected that the Command Register will point to one of the Read Temperature Registers because that will be the data most frequently read from the LM95233), then the read can simply consist of an address byte, followed by retrieving the data byte.
2. If the Command Register needs to be set, then an address byte, command byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, the LM95233 can accept either acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes the LM95233 95 ms (typical, all channels enabled) to measure the temperature of the remote diodes and internal diode. When retrieving all 11 bits from a previous remote diode temperature measurement, the master must insure that all 11 bits are from the same temperature conversion. This may be achieved by reading the MSB register first. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in.

### SMBus Timing Diagrams

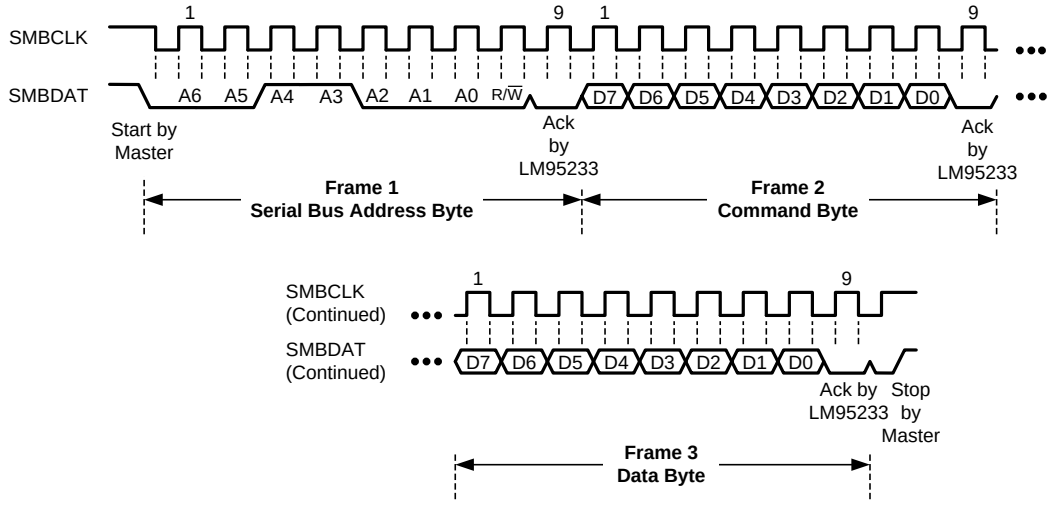


**Figure 16. (a) Serial Bus Write to the internal Command Register followed by a the Data Byte**

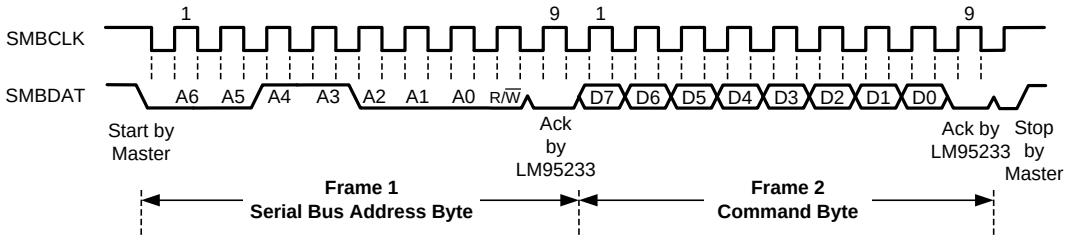


**Figure 17. (b) Serial Bus Write to the Internal Command Register**

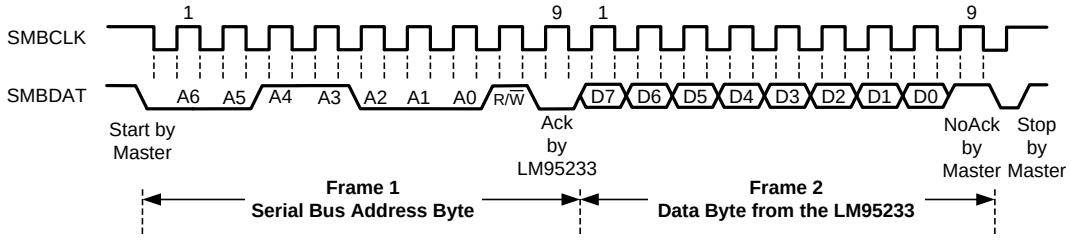


**Figure 18. (c) Serial Bus Read from a Register with the Internal Command Register preset to desired value.**

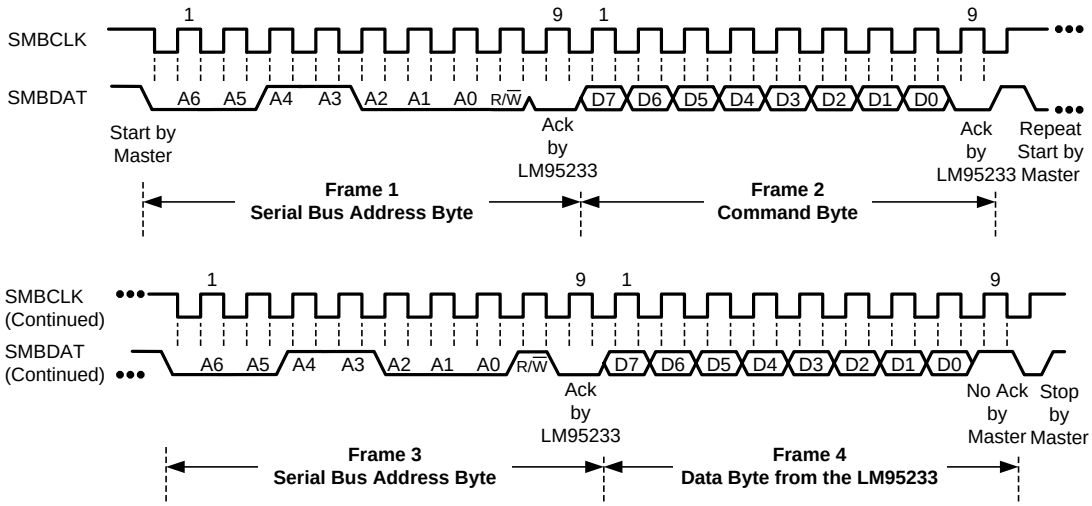


**Figure 19. (d) Serial Bus Write followed by a Repeat Start and Immediate Read**

## SERIAL INTERFACE RESET

In the event that the SMBus Master is RESET while the LM95233 is transmitting on the SMBDAT line, the LM95233 must be returned to a known state in the communication protocol. This may be done in one of two ways:

1. When SMBDAT is LOW, the LM95233 SMBus state machine resets to the SMBus idle state if either SMBDAT or SMBCLK are held low for more than 35ms ($t_{TIMEOUT}$). Note that according to SMBus specification 2.0 all devices are to timeout when either the SMBCLK or SMBDAT lines are held low for 25-35ms. Therefore, to insure a timeout of all devices on the bus the SMBCLK or SMBDAT lines must be held low for at least 35ms.
2. When SMBDAT is HIGH, have the master initiate an SMBus start. The LM95233 will respond properly to an SMBus start condition at any point during the communication. After the start the LM95233 will expect an SMBus Address address byte.

## ONE-SHOT CONVERSION

The One-Shot register is used to initiate a round of conversions and comparisons when the device is in standby mode, after which the device returns to standby. This is not a data register and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register. All the channels that are enabled in the Channel Enable Register will be converted once and the $\overline{TCRIT1}$, $\overline{TCRIT2}$ and $\overline{TCRIT3}$ pins will reflect the comparison results based on this round of conversion results of the channels that are not masked.


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## LM95233 Registers

Command register selects which registers will be read from or written to. Data for this register should be transmitted during the Command Byte of the SMBus write communication.

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| Command Byte | | | | | | | |

P0-P7: Command

**Table 7. Register Summary**

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Local Temp MSB | 0x10 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Local Temp LSB | 0x20 | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 1 MSB – Signed | 0x11 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 1 LSB – Signed, Digital Filter Off | 0x21 | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 1 LSB – Signed, Digital Filter On | | | | | | 1/16 | 1/32 | | | | |
| Remote Temp 2 MSB – Signed | 0x12 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 2 LSB – Signed, Digital Filter Off | 0x22 | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 2 LSB – Signed, Digital Filter On | | | | | | 1/16 | 1/32 | | | | |
| Remote Temp 1 MSB – Unsigned | 0x19 | RO | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 1 LSB – Unsigned, Digital Filter Off | 0x29 | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 1 LSB – Unsigned, Digital Filter On | | | | | | 1/16 | 1/32 | | | | |
| Remote Temp 2 MSB – Unsigned | 0x1A | RO | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 2 LSB – Unsigned, Digital Filter Off | 0x2A | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 2 LSB – Unsigned, Digital Filter On | | | | | | 1/16 | 1/32 | | | | |
| Diode Model Select | 0x30 | R/W | 0 | 0 | 0 | 0 | 0 | R2TE | R1TE | 0 | 0x02 |
| Remote 1 Offset | 0x31 | R/W | SIGN | 32 | 16 | 8 | 4 | 2 | 1 | 1/2 | 0x00 |
| Remote 2 Offset | 0x32 | R/W | SIGN | 32 | 16 | 8 | 4 | 2 | 1 | 1/2 | 0x00 |
| Configuration | 0x03 | R/W | – | STBY | – | – | – | – | – | – | 0x00 |
| Conversion Rate | 0x04 | R/W | – | – | – | – | – | – | CR1 | CR0 | 0x02 |
| Channel Conversion Enable | 0x05 | R/W | – | – | – | – | – | R2CE | R1CE | LCE | 0x1F |
| Filter Setting | 0x06 | R/W | – | – | – | – | R2F1 | R2F0 | R1F1 | R1F0 | 0x0F |
| 1-shot | 0x0F | WO | – | – | – | – | – | – | – | – | – |
| Common Status Register | 0x02 | RO | BUSY | NR | – | – | SR4F | SR3F | SR2F | SR1F | 0x00 |
| Status 1 (Diode Fault) | 0x07 | RO | – | – | – | – | R2DO | R2DS | R1DO | R1DS | – |
| Status 2 ($\overline{\text{TCRIT1}}$) | 0x08 | RO | – | – | – | – | – | R2T1 | R1T1 | LT1 | – |
| Status 3 ($\overline{\text{TCRIT2}}$) | 0x09 | RO | – | – | – | – | – | R2T2 | R1T2 | LT2 | – |
| Status 4 ($\overline{\text{TCRIT3}}$) | 0x0A | RO | – | – | – | – | – | R2T3 | R1T3 | LT3 | – |
| Diode Model Status (TruTherm on and 3904 connected) | 0x38 | RO | – | – | – | – | – | R2TD | R1TD | – | – |
| TCRIT1 Mask | 0x0C | R/W | – | – | – | – | – | R2T1M | R1T1M | LTM | 0x01 |
| TCRIT2 Mask | 0x0D | R/W | – | – | – | – | – | R2T2M | R1T2M | LTM | 0x00 |
| TCRIT3 Mask | 0x0E | R/W | – | – | – | – | – | R2T2M | R1T2M | LTM | 0x07 |

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**Table 7. Register Summary (continued)**

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Local Tcrit Limit | 0x40 | R/W | 0 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |
| Remote 1 Tcrit-1 Limit | 0x41 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x6E |
| Remote 2 Tcrit-1 Limit | 0x42 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x6E |
| Remote 1 Tcrit-2 and Tcrit-3 Limit | 0x49 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |
| Remote 2 Tcrit-2 and Tcrit-3 Limit | 0x4A | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |
| Common Tcrit Hysteresis | 0x5A | R/W | 0 | 0 | 0 | 16 | 8 | 4 | 2 | 1 | 0x0A |
| Manufacturer ID | 0xFE | RO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x01 |
| Revision ID | 0xFF | RO | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0x89 |

## VALUE REGISTERS

For data synchronization purposes, the MSB register should be read first if the user wants to read both MSB and LSB registers. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in

### *Local Value Registers*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Local Temp MSB | 0x10 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Local Temp LSB | 0x20 | RO | 1/2 | 1/4 | 1/8 | 0 | 0 | 0 | 0 | 0 | – |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7 | SIGN | RO | Sign bit | The Local temperature MSB value register range is +127°C to −128°C. The value programmed in this register is used to determine a local temperature error event. |
| 6 | 64 | RO | bit weight 64°C | |
| 5 | 32 | RO | bit weight 32°C | |
| 4 | 16 | RO | bit weight 16°C | |
| 3 | 8 | RO | bit weight 8°C | |
| 2 | 4 | RO | bit weight 4°C | |
| 1 | 2 | RO | bit weight 2°C | |
| 0 | 1 | RO | bit weight 1°C | |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7 | 1/2 | RO | bit weight 1/2°C (0.5°C) | The Local Limit register range is 0°C to 127°C. The value programmed in this register is used to determine a local temperature error event. |
| 6 | 1/4 | RO | bit weight 1/4°C (0.25°C) | |
| 5 | 1/8 | RO | bit weight 1/8°C (0.125°C) | |
| 4-0 | 0 | RO | Reserved – will report "0" when read. | |


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### *Remote Temperature Value Registers with Signed Format*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Remote Temp 1 MSB – Signed | 0x11 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 1 LSB – Signed, Digital Filter Off | 0x21 | RO | 1/2 | 1/8 | 0 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 1 LSB – Signed, Digital Filter On | | | | | 1/16 | 1/32 | | | | | |
| Remote Temp 2 MSB – Signed | 0x12 | RO | SIGN | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 2 LSB – Signed, Digital Filter Off | 0x22 | RO | 1/2 | 1/8 | 0 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 2 LSB – Signed, Digital Filter On | | | | | 1/16 | 1/32 | | | | | |

The Local temperature MSB value register range is +127°C to −128°C. The value programmed in this register is used to determine a local temperature error event.

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | SIGN | RO | Sign bit |
| 6 | 64 | RO | bit weight 64°C |
| 5 | 32 | RO | bit weight 32°C |
| 4 | 16 | RO | bit weight 16°C |
| 3 | 8 | RO | bit weight 8°C |
| 2 | 4 | RO | bit weight 4°C |
| 1 | 2 | RO | bit weight 2°C |
| 0 | 1 | RO | bit weight 1°C |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | 1/2 | RO | bit weight 1/2°C (0.5°C) |
| 6 | 1/4 | RO | bit weight 1/4°C (0.25°C) |
| 5 | 1/8 | RO | bit weight 1/8°C (0.125°C) |
| 4 | 0 or 1/16 | RO | When the digital filter is disabled this bit will always read "0".<br>When the digital filter is enabled this bit will report 1/16°C (0.0625°C) bit state. |
| 3 | 0 or 1/32 | RO | When the digital filter is disabled this bit will always read "0".<br>When the digital filter is enabled this bit will report 1/32°C (0.03125°C) bit state. |
| 2-0 | 0 | RO | Reserved – will report "0" when read. |

### *Remote Temperature Value Registers with Unsigned Format*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Remote Temp 1 MSB – Unsigned | 0x19 | RO | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 1 LSB – Unsigned, Digital Filter Off | 0x29 | RO | 1/2 | 1/8 | 0 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 1 LSB – Unsigned, Digital Filter On | | | | | 1/16 | 1/32 | | | | | |
| Remote Temp 2 MSB – Unsigned | 0x1A | RO | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | – |
| Remote Temp 2 LSB – Unsigned, Digital Filter Off | 0x2A | RO | 1/2 | 1/8 | 0 | 0 | 0 | 0 | 0 | 0 | – |
| Remote Temp 2 LSB – Unsigned, Digital Filter On | | | | | 1/16 | 1/32 | | | | | |

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| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | SIGN | RO | bit weight 128°C |
| 6 | 64 | RO | bit weight 64°C |
| 5 | 32 | RO | bit weight 32°C |
| 4 | 16 | RO | bit weight 16°C |
| 3 | 8 | RO | bit weight 8°C |
| 2 | 4 | RO | bit weight 4°C |
| 1 | 2 | RO | bit weight 2°C |
| 0 | 1 | RO | bit weight 1°C |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | 1/2 | RO | bit weight 1/2°C (0.5°C) |
| 6 | 1/4 | RO | bit weight 1/4°C (0.25°C) |
| 5 | 1/8 | RO | bit weight 1/8°C (0.125°C) |
| 4 | 0 or 1/16 | RO | When the digital filter is disabled this bit will always read "0".<br>When the digital filter is enabled this bit will report 1/16°C (0.0625°C) bit state. |
| 3 | 0 or 1/32 | RO | When the digital filter is disabled this bit will always read "0".<br>When the digital filter is enabled this bit will report 1/32°C (0.03125°C) bit state. |
| 2-0 | 0 | RO | Reserved – will report "0" when read. |

## DIODE CONFIGURATION REGISTERS

### *Diode Model Select*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Diode Model Select | 0x30 | R/W | 0 | 0 | 0 | 0 | 0 | R2TE | R1TE | 0 | 0x02 |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7-3 | 0 | RO | Reserved – will report "0" when read. | |
| 2 | R2TE | R/W | Remote 2 TruTherm Enable | logic 1 selects diode model 1 TruTherm™ BJT beta compensation technology enabled (Ex: Intel 65 nm technology)<br>logic 0 selects diode model 2 MMBT3904 |
| 1 | R1TE | R/W | Remote 1 TruTherm Enable | |
| 0 | 0 | RO | Reserved - will report "0" when read. | |


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### *Remote 1-2 Offset*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Remote 1 Offset | 0x31 | R/W | SIGN | 32 | 16 | 8 | 4 | 2 | 1 | 1/2 | 0x00 |
| Remote 2 Offset | 0x32 | R/W | SIGN | 32 | 16 | 8 | 4 | 2 | 1 | 1/2 | 0x00 |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7 | SIGN | R/W | Sign bit | All registers have 2's complement format. The offset range for each remote is +63.5°C/−64°C. The value programmed in this register is directly added to the actual reading of the ADC and the modified number is reported in the remote value registers. |
| 6 | 32 | R/W | bit weight 32°C | |
| 5 | 16 | R/W | bit weight 16°C | |
| 4 | 8 | R/W | bit weight 8°C | |
| 3 | 4 | R/W | bit weight 4°C | |
| 2 | 2 | R/W | bit weight 2°C | |
| 1 | 1 | R/W | bit weight 1°C | |
| 0 | 1/2 | R/W | bit weight 1/2°C (0.5°C) | |

## CONFIGURATION REGISTERS

### *Main Configuration Register*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Configuration | 0x03 | R/W | – | STBY | – | – | – | – | – | – | 0x00 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | – | RO | Reserved will report "0" when read. |
| 6 | STBY | R/W | Software Standby<br>1 – standby (when in this mode one conversion sequence can be initiated by writing to the one-shot register)<br>0 – active/converting |
| 5–0 | – | RO | Reserved – will report "0" when read. |

### *Conversion Rate Register*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Conversion Rate | 0x04 | R/W | – | – | – | – | – | – | CR1 | CR0 | 0x02 |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7-2 | – | RO | Reserved – will report "0" when read. | |
| 1-0 | CR[1:0] | R/W | Conversion rate control bits modify the time interval for conversion of the channels enabled. The channels enabled are converted sequentially then standby mode enabled for the remainder of the time interval. | |
| | | | **CR[1:0]** | **Conversion Rate** |
| | | | 00 | continuous (30 ms to 104 ms) |
| | | | 01 | 0.364 s |
| | | | 10 | 1s |
| | | | 11 | 2.5 s |

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### *Channel Conversion Enable*

When a conversion is disabled for a particular channel it is skipped. The continuous conversion rate is effected all other conversion rates are not effected as extra standby time is inserted in order to compensate. See Conversion Rate Register description.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Channel Conversion Enable | 0x05 | R/W | – | – | – | – | – | R2CE | R1CE | LCE | 0x1F |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7–3 | – | RO | Reserved – will report "0" when read. |
| 2 | R2CE | R/W | Remote 2 Temperature Conversion Enable<br>1– Remote 2 temp conversion enabled<br>0– Remote 2 temp conversion disabled |
| 1 | R1CE | R/W | Remote 1 Temperature Conversion Enable<br>1– Remote 1 temp conversion enabled<br>0– Remote 1 temp conversion disabled |
| 0 | LCE | R/W | Local Temperature Conversion Enable<br>1– Local temp conversion enabled<br>0– Local temp conversion disabled |

### *Filter Setting*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Filter Setting | 0x06 | R/W | – | – | – | – | R2F1 | R2F0 | R1F1 | R1F0 | 0x0F |

| Bit(s) | Bit Name | Read/ Write | Description | |
|---|---|---|---|---|
| 7–4 | – | RO | Reserved – will report "0" when read. | |
| 3–2 | R2F[1:0] | R/W | Remote Channel 2 Filter Enable Bits | |
| | | | **R2F[1:0]** | **Digital Filter State** |
| | | | 00 | disable all digital filtering |
| | | | 01 | enable basic filter |
| | | | 10 | reserved (do not use) |
| | | | 11 | enable enhanced filter |
| 1–0 | R1F[1:0] | R/W | Remote Channel 1 Filter Enable | |
| | | | **R1F[1:0]** | **Filter State** |
| | | | 00 | disable all digital filtering |
| | | | 01 | enable basic filter |
| | | | 10 | reserved (do not use) |
| | | | 11 | enable enhanced filter |

### *1-Shot*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1-Shot | 0x0F | WO | – | – | – | – | – | – | – | – | – |


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| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7–0 | - | WO | Writing to this register activates one conversion for all the enabled channels if the chip is in standby mode (i.e. standby bit = 1). The actual data written does not matter and is not stored. |

## STATUS REGISTERS

### *Common Status Register*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Status Register | 0x02 | RO | BUSY | NR | – | – | SR4F | SR3F | SR2F | SR1F | 0x00 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | BUSY | RO | Busy bit (device converting) |
| 6 | NR | RO | Not Ready bit (30 ms), indicates power up initialization sequence is in progress |
| 5–4 | – | RO | Reserved – will report "0" when read. |
| 3 | SR4F | RO | Status Register 4 Flag:<br>1 – indicates that Status Register 4 has at least one bit set<br>0 – indicates that all of Status Register 4 bits are cleared |
| 2 | SR3F | RO | Status Register 3 Flag:<br>1 – indicates that Status Register 3 has at least one bit set<br>0 – indicates that all of Status Register 3 bits are cleared |
| 1 | SR2F | RO | Status Register 2 Flag:<br>1 – indicates that Status Register 2 has at least one bit set<br>0 – indicates that all of Status Register 2 bits are cleared |
| 0 | SR1F | RO | Status Register 1 Flag:<br>1 – indicates that Status Register 1 has at least one bit set<br>0 – indicates that all of Status Register 1 bits are cleared |

### *Status 1 Register (Diode Fault)*

Status fault bits for open or shorted diode (i.e. Short Fault: D+ shorted to Ground or D-; Open Fault: D+ shorted to $V_{DD}$, or floating). During fault conditions the temperature reading is 0 °C if unsigned value registers are read or –128.000 °C if signed value registers are read.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Status 1 (Diode Fault) | 0x07 | RO | 0 | 0 | 0 | 0 | R2DO | R2DS | R1DO | R1DS | – |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7-4 | – | RO | Reserved – will report "0" when read. |
| 3 | R2DO | RO | Remote 2 diode open fault status:<br>1 – indicates that remote 2 diode has an "open" fault<br>0 – indicates that remote 2 diode does not have an "open" fault |
| 2 | R2DS | RO | Remote 2 diode short fault status:<br>1 – indicates that remote 2 diode has a "short" fault<br>0 – indicates that remote 2 diode does not have a "short" fault |
| 1 | R1DO | RO | Remote 1 diode open fault status:<br>1 – indicates that remote 1 diode has an "open" fault<br>0 – indicates that remote 1 diode does not have an "open" fault |
| 0 | R1DS | RO | Remote 1 diode short fault status:<br>1 – indicates that remote 1 diode has a "short" fault<br>0 – indicates that remote 1 diode does not have a "short" fault |

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### *Status 2 ($\overline{TCRIT1}$)*

Status bits for $\overline{TCRIT1}$. When one or more of these bits are set and if not masked the $\overline{TCRIT1}$ output will activate. $\overline{TCRIT1}$ will deactivate when all these bits are cleared.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Status 2 ($\overline{TCRIT1}$) | 0x08 | RO | – | – | – | – | – | R2T1 | R1T1 | LT1 | – |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7–3 | - | RO | Reserved – will report "0" when read. |
| 2 | R2T1 | RO | Remote 2 Tcrit-1 Status:<br>1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-1 Limit register<br>0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-1 Limit register minus the Common Hysteresis value |
| 1 | R1T1 | RO | Remote 1 Tcrit-1 Status:<br>1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-1 Limit register<br>0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-1 Limit register minus the Common Hysteresis value |
| 0 | LT1 | RO | Local Tcrit Status:<br>1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register<br>0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value |

### *Status 3 ($\overline{TCRIT2}$)*

Status bits for $\overline{TCRIT2}$. When one or more of these bits are set and if not masked the $\overline{TCRIT2}$ output will activate. $\overline{TCRIT2}$ will deactivate when all these bits are cleared.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Status 3 ($\overline{TCRIT2}$) | 0x09 | RO | – | – | – | – | – | R2T2 | R1T2 | LT2 | – |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7–3 | - | RO | Reserved – will report "0" when read. |
| 2 | R2T2 | RO | Remote 2 Tcrit-2 Status:<br>1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-2 Limit register<br>0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-2 Limit register minus the Common Hysteresis value |
| 1 | R1T2 | RO | Remote 1 Tcrit-2 Status:<br>1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-2 Limit register<br>0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-2 Limit register minus the Common Hysteresis value |
| 0 | LT2 | RO | Local Tcrit Status:<br>1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register<br>0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value |


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### *Status 4 ($\overline{TCRIT3}$)*

Status bits for $\overline{TCRIT3}$. When one or more of these bits are set and if not masked the $\overline{TCRIT3}$ output will activate. $\overline{TCRIT3}$ will deactivate when all these bits are cleared.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Status 4 ($\overline{TCRIT3}$) | 0x0A | RO | – | – | – | – | – | R2T3 | R1T3 | LT3 | – |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7–3 | - | RO | Reserved – will report "0" when read. |
| 2 | R2T3 | RO | Remote 2 Tcrit-2 Status:<br>1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-2 Limit register<br>0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-2 Limit register minus the Common Hysteresis value |
| 1 | R1T3 | RO | Remote 1 Tcrit-2 Status:<br>1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-2 Limit register<br>0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-2 Limit register minus the Common Hysteresis value |
| 0 | LT3 | RO | Local Tcrit Status:<br>1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register<br>0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value |

### *Diode Model Status*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Diode Model Status (TruTherm on and 3904 connected) | 0x38 | RO | – | – | – | – | – | R2TD | R1TD | – | – |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7-3 | – | RO | Reserved – will report "0" when read. |
| 2 | R2TD | RO | Remote 2 TruTherm BJT beta compensation on and 3904 detect:<br>1 – indicates that for channel 2 TruTherm is ON and 3904 connected<br>0 – indicates proper operation |
| 1 | R1TD | RO | Remote 1 TruTherm BJT beta compensation on and 3904 detect:<br>1 – indicates that for channel 4 TruTherm is ON and 3904 connected<br>0 – indicates proper operation |
| 0 | – | RO | Reserved – will report "0" when read. |

## MASK REGISTERS

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### *TCRIT1 Mask Register*

The mask bits in this register allow control over which error events propagate to the $\overline{\text{TCRIT1}}$ pin.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{TCRIT1}}$ Mask | 0x0C | R/W | – | – | – | – | – | R2T1M | R1T1M | LTM | 0x01 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7-3 | – | RO | Reserved – will report "0" when read. |
| 2 | R2T1M | R/W | Remote 2 Tcrit-1 Mask:<br>1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin<br>0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin |
| 1 | R1T1M | R/W | Remote 1 Tcrit-1 Mask:<br>1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin<br>0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin |
| 0 | LTM | R/W | Local Tcrit Mask:<br>1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin<br>0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin |

### *$\overline{\text{TCRIT2}}$ Mask Registers*

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{TCRIT2}}$ Mask | 0x0D | R/W | – | – | – | – | – | R2T2M | R1T2M | LTM | 0x00 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7-3 | – | RO | Reserved – will report "0" when read. |
| 2 | R2T2M | R/W | Remote 2 Tcrit-2 Mask:<br>1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin<br>0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin |
| 1 | R1T2M | R/W | Remote 1 Tcrit-2 Mask:<br>1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin<br>0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin |
| 0 | LTM | R/W | Local Tcrit Mask:<br>1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin<br>0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin |

### *$\overline{\text{TCRIT3}}$ Mask Register*

The mask bits in this register allow control over which error events propagate to the $\overline{\text{TCRIT3}}$ pin.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{TCRIT3}}$ Mask | 0x0E | R/W | – | – | – | – | – | R2T2M | R1T2M | LTM | 0x07 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7-3 | – | RO | Reserved – will report "0" when read. |
| 2 | R2T2M | R/W | Remote 2 Tcrit-2 Mask:<br>1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin<br>0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin |


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| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 1 | R1T2M | R/W | Remote 1 Tcrit-2 Mask:<br>1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin<br>0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin |
| 0 | LTM | R/W | Local Tcrit Mask:<br>1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin<br>0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin |

## LIMIT REGISTERS

### *Local Limit Register*

The Local Limit register range is 0°C to 127°C. The value programmed in this register is used to determine a local temperature error event.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Local Tcrit Limit | 0x40 | R/W | 0 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | 0 | R0 | Read only bit will always report "0". |
| 6 | 64 | R/W | bit weight 64°C |
| 5 | 32 | R/W | bit weight 32°C |
| 4 | 16 | R/W | bit weight 16°C |
| 3 | 8 | R/W | bit weight 8°C |
| 2 | 4 | R/W | bit weight 4°C |
| 1 | 2 | R/W | bit weight 2°C |
| 0 | 1 | R/W | bit weight 1°C |

### *Remote Limit Registers*

The range for these registers is 0°C to 255°C.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Remote 1 Tcrit-1 Limit (used by $\overline{\text{TCRIT1}}$ error events) | 0x41 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x6E |
| Remote 2 Tcrit-1 Limit (used by $\overline{\text{TCRIT1}}$ error events) | 0x42 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x6E |
| Remote 1 Tcrit-2 and Tcrit3 Limit (used by $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events) | 0x49 | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |
| Remote 2 Tcrit-2 and Tcrit3 Limit (used by $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events) | 0x4A | R/W | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0x55 |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | 128 | R/W | bit weight 128°C |
| 6 | 64 | R/W | bit weight 64°C |
| 5 | 32 | R/W | bit weight 32°C |
| 4 | 16 | R/W | bit weight 16°C |
| 3 | 8 | R/W | bit weight 8°C |
| 2 | 4 | R/W | bit weight 4°C |
| 1 | 2 | R/W | bit weight 2°C |

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| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 0 | 1 | R/W | bit weight 1°C |

**Table 8. Limit assignments for each $\overline{\text{TCRIT}}$ output pin:**

| Output Pin | Remote 2 | Remote 1 | Local |
|---|---|---|---|
| $\overline{\text{TCRIT1}}$ | Remote 2 Tcrit-1 Limit | Remote 1 Tcrit-1 Limit | Local Tcrit Limit |
| $\overline{\text{TCRIT2}}$ | Remote 2 Tcrit-2 Limit | Remote 1 Tcrit-2 Limit | Local Tcrit Limit |
| $\overline{\text{TCRIT3}}$ | Remote 2 Tcrit-2 Limit | Remote 1 Tcrit-2 Limit | Local Tcrit Limit |

### *Common Tcrit Hysteresis Register*

The hysteresis register range is 0°C to 32°C. The value programmed in this register is used to modify all the limit values for decreasing temperature.

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Tcrit Hysteresis | 0x5A | R/W | 0 | 0 | 0 | 16 | 8 | 4 | 2 | 1 | 0x0A |

| Bit(s) | Bit Name | Read/ Write | Description |
|---|---|---|---|
| 7 | 0 | RO | Read only bit will always report "0". |
| 6 | 0 | RO | Read only bit will always report "0". |
| 5 | 0 | RO | Read only bit will always report "0". |
| 4 | 16 | R/W | bit weight 16°C |
| 3 | 8 | R/W | bit weight 8°C |
| 2 | 4 | R/W | bit weight 4°C |
| 1 | 2 | R/W | bit weight 2°C |
| 0 | 1 | R/W | bit weight 1°C |

### IDENTIFICATION REGISTERS

| Register Name | Command Byte (Hex) | Read/ Write | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID | 0xFE | RO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x01 |
| Revision ID | 0xFF | RO | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0x89 |

## Applications Hints

The LM95233 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the LM95233's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the LM95233 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

To measure temperature external to the LM95233's die, incorporates remote diode sensing technology. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM95233's temperature. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads. Most silicon diodes do not lend themselves well to this application. It is recommended that an MMBT3904 transistor base emitter junction be used with the collector tied to the base.


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The LM95233's TruTherm BJT beta compensation technology allows accurate sensing of integrated thermal diodes, such as those found on most processors. With TruTherm BJT beta compensation technology turned off, the LM95233 can measure a diode-connected transistor such as the MMBT3904 or the thermal diode found in an AMD processor.

The LM95233 has been optimized to measure the remote thermal diode integrated in a typical Intel processor on 65 nm or 90 nm process or an MMBT3904 transistor. Using the Remote Diode Model Select register any of the four remote inputs can be optimized for a typical Intel processor on 65 nm or 90 nm process or an MMBT3904.

## DIODE NON-IDEALITY

### *Diode Non-Ideality Factor Effect on Accuracy*

When a transistor is connected as a diode, the following relationship holds for variables $V_{BE}$, T and $I_F$:

$$I_F = I_S \times \left[ e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} - 1 \right]$$

where

- $$V_t = \frac{kT}{q}$$ (2)
- q = $1.6\times10^{-19}$ Coulombs (the electron charge),
- T = Absolute Temperature in Kelvin
- k = $1.38\times10^{-23}$ joules/K (Boltzmann's constant),
- η is the non-ideality factor of the process the diode is manufactured on,
- $I_S$ = Saturation Current and is process dependent,
- $I_f$ = Forward Current through the base-emitter junction
- $V_{BE}$ = Base-Emitter Voltage drop (2)

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \times \left[ e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} \right] \quad (3)$$

In Equation 3, η and $I_S$ are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ratio($I_{F2}$ / $I_{F1}$) and measuring the resulting voltage difference, it is possible to eliminate the $I_S$ term. Solving for the forward voltage difference yields the relationship:

$$\Delta V_{BE} = \eta \times \left(\frac{kT}{q}\right) \times \ln\left(\frac{I_{F2}}{I_{F1}}\right) \quad (4)$$

Solving Equation 4 for temperature yields:

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{F2}}{I_{F1}}\right)} \quad (5)$$

Equation 5 holds true when a diode connected transistor such as the MMBT3904 is used. When this "diode" equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in Figure 20 it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that Equation 5 is an approximation.

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TruTherm BJT beta compensation technology uses the transistor equation, Equation 6, which is a more accurate representation of the topology of the thermal diode found in an FPGA or processor.

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{C2}}{I_{C1}}\right)} \quad (6)$$

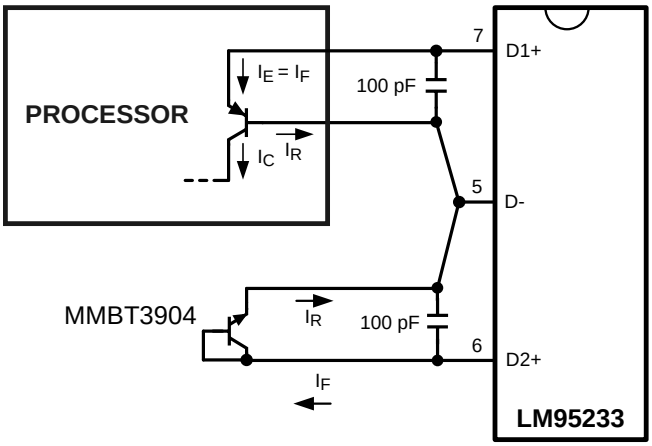


**Figure 20. Thermal Diode Current Paths**

TruTherm BJT beta compensation should only be enabled when measuring the temperature of a transistor integrated as shown in the processor of Figure 20, because Equation 6 only applies to this topology.

### *Calculating Total System Accuracy*

The voltage seen by the LM95233 also includes the $I_F R_S$ voltage drop of the series resistance. The non-ideality factor, η, is the only other parameter not accounted for and depends on the diode that is used for measurement. Since $\Delta V_{BE}$ is proportional to both η and T, the variations in η cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the for Intel processor on 65 nm process, Intel specifies a +4.06%/−0.897% variation in η from part to part when the processor diode is measured by a circuit that assumes diode equation, Equation 5, as true. As an example, assume a temperature sensor has an accuracy specification of ±1.0°C at a temperature of 80°C (353 Kelvin) and the processor diode has a non-ideality variation of +1.19%/−0.27%. The resulting system accuracy of the processor temperature being sensed will be:

$$T_{ACC} = + 1.0°C + (+4.06\% \text{ of } 353 \text{ K}) = +15.3 °C \quad (7)$$

and

$$T_{ACC} = - 1.0°C + (-0.89\% \text{ of } 353 \text{ K}) = -4.1 °C \quad (8)$$

TrueTherm technology uses the transistor equation, Equation 5, resulting in a non-ideality spread that truly reflects the process variation which is very small. The transistor equation non-ideality spread is ±0.39% for the Intel processor on 90 nm process. The resulting accuracy when using TruTherm technology improves to:

$$T_{ACC} = \pm 0.75°C + (\pm 0.39\% \text{ of } 353 \text{ K}) = \pm 2.16 °C \quad (9)$$


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The next error term to be discussed is that due to the series resistance of the thermal diode and printed circuit board traces. The thermal diode series resistance is specified on most processor data sheets. For Intel processors in 65 nm process, this is specified at 4.52Ω typical. The LM95233 accommodates the typical series resistance of Intel Processor on 65 nm process. The error that is not accounted for is the spread of the processor's series resistance, that is 2.79Ω to 6.24Ω or ±1.73Ω. The equation to calculate the temperature error due to series resistance ($T_{ER}$) for the LM95233 is simply:

$$T_{ER} = \left(0.62 \frac{^{o}C}{\Omega}\right) \times R_{PCB} \tag{10}$$

Solving Equation 10 for $R_{PCB}$ equal to ±1.73Ω results in the additional error due to the spread in the series resistance of ±1.07°C. The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

Equation 10 can also be used to calculate the additional error caused by series resistance on the printed circuit board. Since the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the LM95233.

| Processor Family | Transistor Equation $\eta_T$, non-ideality | | | Series R,Ω |
|---|---|---|---|---|
| | min | typ | max | |
| Intel Processor on 65 nm process | 0.997 | 1.001 | 1.005 | 4.52 |

| Processor Family | Diode Equation $\eta_D$, non-ideality | | | Series R,Ω |
|---|---|---|---|---|
| | min | typ | max | |
| Pentium III CPUID 67h | 1 | 1.0065 | 1.0125 | |
| Pentium III CPUID 68h/PGA370Socket/ Celeron | 1.0057 | 1.008 | 1.0125 | |
| Pentium 4, 423 pin | 0.9933 | 1.0045 | 1.0368 | |
| Pentium 4, 478 pin | 0.9933 | 1.0045 | 1.0368 | |
| Pentium 4 on 0.13 micron process, 2 - 3.06 GHz | 1.0011 | 1.0021 | 1.0030 | 3.64 |
| Pentium 4 on 90 nm process | 1.0083 | 1.011 | 1.023 | 3.33 |
| Intel Processor on 65 nm process | 1.000 | 1.009 | 1.050 | 4.52 |
| Pentium M (Centrino) | 1.00151 | 1.00220 | 1.00289 | 3.06 |
| MMBT3904 | | 1.003 | | |
| AMD Athlon MP model 6 | 1.002 | 1.008 | 1.016 | |
| AMD Athlon 64 | 1.008 | 1.008 | 1.096 | |
| AMD Opteron | 1.008 | 1.008 | 1.096 | |
| AMD Sempron | | 1.00261 | | 0.93 |

### *Compensating for Different Non-Ideality*

In order to compensate for the errors introduced by non-ideality, the temperature sensor is calibrated for a particular processor. Texas Instruments temperature sensors are always calibrated to the typical non-ideality and series resistance of a given processor type. The LM95233 is calibrated for two non-ideality factors and series resistance values thus supporting the MMBT3904 transistor and Intel processors on 65 nm process without the requirement for additional trims. For most accurate measurements TruTherm BJT beta compensation mode should be turned on when measuring the Intel processor on 65 nm process to minimize the error introduced by the false non-ideality spread (see Diode Non-Ideality Factor Effect on Accuracy). When a temperature sensor calibrated for a particular processor type is used with a different processor type, additional errors are introduced.

Temperature errors associated with non-ideality of different processor types may be reduced in a specific temperature range of concern through use of software calibration. Typical Non-ideality specification differences cause a gain variation of the transfer function, therefore the center of the temperature range of interest should be the target temperature for calibration purposes. The following equation can be used to calculate the temperature correction factor ($T_{CF}$) required to compensate for a target non-ideality differing from that supported by the LM95233.

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$$T_{CF} = \left( \frac{\eta_S - \eta_{PROCESSOR}}{\eta_S} \right) x \, (T_{CR} + 273K)$$

where

- $\eta_S$ = LM95233 non-ideality for accuracy specification
- $\eta_{PROCESSOR}$ = Processor thermal diode typical non-ideality
- $T_{CR}$ = center of the temperature range of interest in °C (11)

The correction factor should be directly added to the temperature reading produced by the LM95233. For example when using the LM95233, with the 3904 mode selected, to measure a AMD Athlon processor, with a typical non-ideality of 1.008, for a temperature range of 60 °C to 100 °C the correction factor would calculate to:

$$T_{CF} = \left( \frac{1.003 - 1.008}{1.003} \right) \cdot (80 + 273) = -1.75^{o}C \quad (12)$$

Therefore, 1.75°C should be subtracted from the temperature readings of the LM95233 to compensate for the differing typical non-ideality target.

## PCB LAYOUT FOR MINIMIZING NOISE

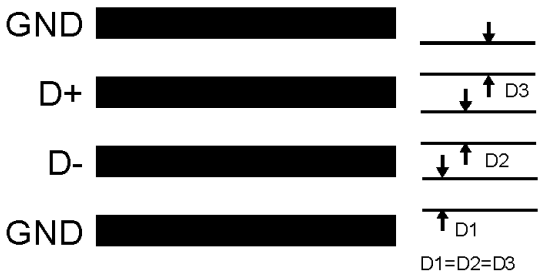


**Figure 21. Ideal Diode Trace Layout**

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM95233 can cause temperature conversion errors. Keep in mind that the signal level the LM95233 is trying to measure is in microvolts. The following guidelines should be followed:

1. $V_{DD}$ should be bypassed with a 0.1 µF capacitor in parallel with 100 pF. The 100 pF capacitor should be placed as close as possible to the power supply pin. A bulk capacitance of approximately 10 µF needs to be in the near vicinity of the LM95233.
2. A 100 pF diode bypass capacitor is recommended to filter high frequency noise but may not be necessary. Make sure the traces to the 100 pF capacitor are matched. Place the filter capacitors close to the LM95233 pins.
3. Ideally, the LM95233 should be placed within 10 cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1Ω can cause as much as 0.62°C of error. This error can be compensated by using simple software offset compensation.
4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D− lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D− lines.
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2 cm apart from the high speed digital traces.
7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. The ideal place to connect the LM95233's GND pin is as close as possible to the Processors GND associated with the sense diode.
9. Leakage current between D+ and GND and between D+ and D− should be kept to a minimum. Thirteen


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nano-amperes of leakage can cause as much as 0.2°C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible will minimize leakage current.

Noise coupling into the digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV below GND, may prevent successful SMBus communication with the LM95233. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the SMBus maximum frequency of communication is rather low (100 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. An RC lowpass filter with a 3 dB corner frequency of about 40 MHz is included on the LM95233's SMBCLK input. Additional resistance can be added in series with the SMBDAT and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

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## REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 37 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM95233CISD | NRND | Production | WSON (NHL) \| 14 | 1000 \| SMALL T&R | No | Call TI | Level-1-260C-UNLIM | -40 to 140 | 95233CI |
| LM95233CISD.A | NRND | Production | WSON (NHL) \| 14 | 1000 \| SMALL T&R | No | Call TI | Call TI | -40 to 140 | 95233CI |
| LM95233CISD/NOPB | Obsolete | Production | WSON (NHL) \| 14 | - | - | Call TI | Call TI | -40 to 140 | 95233CI |
| LM95233CISDX/NOPB | Active | Production | WSON (NHL) \| 14 | 4500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 140 | 95233CI |
| LM95233CISDX/NOPB.A | Active | Production | WSON (NHL) \| 14 | 4500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 140 | 95233CI |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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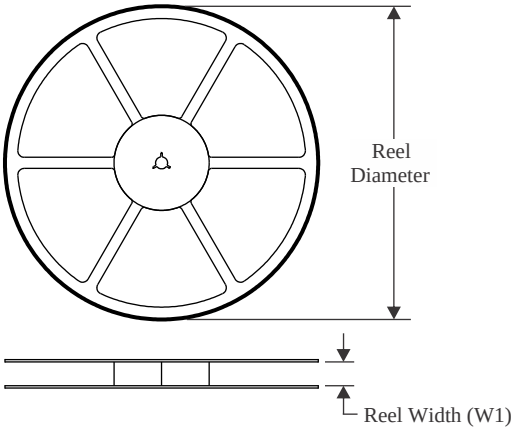
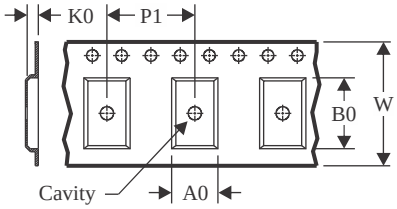
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

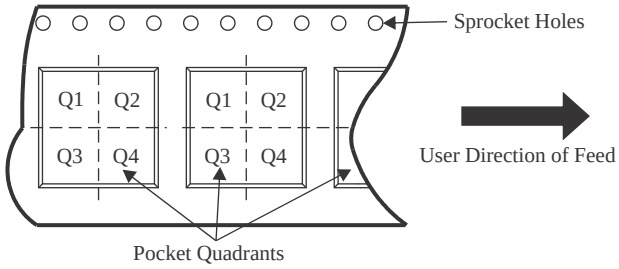



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

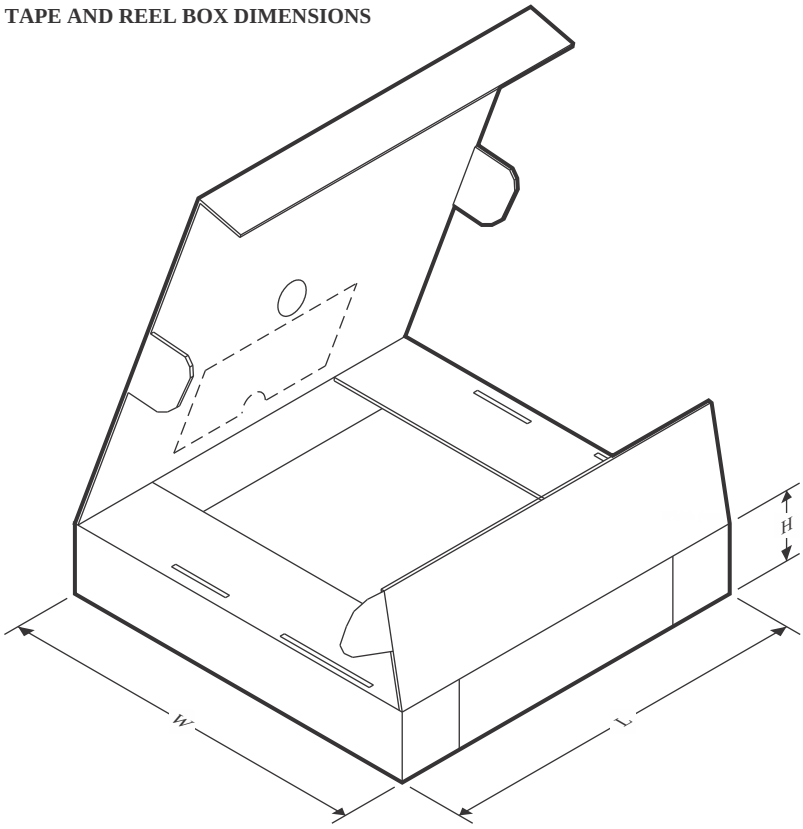
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM95233CISD | WSON | NHL | 14 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM95233CISDX/NOPB | WSON | NHL | 14 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

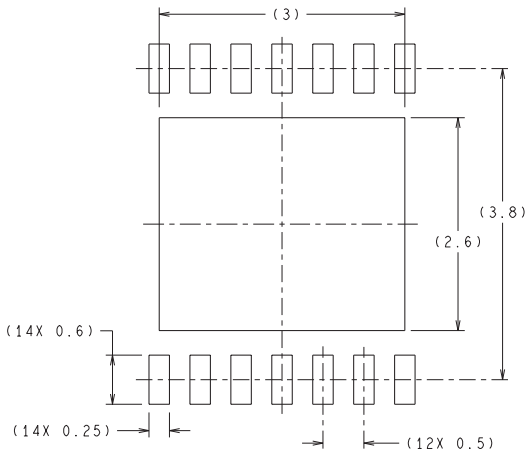
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

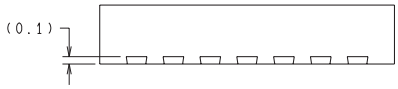
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM95233CISD | WSON | NHL | 14 | 1000 | 208.0 | 191.0 | 35.0 |
| LM95233CISDX/NOPB | WSON | NHL | 14 | 4500 | 367.0 | 367.0 | 35.0 |

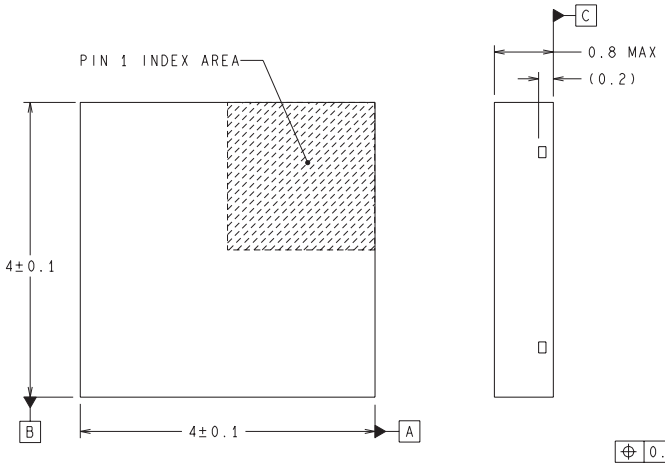
# NHL0014B

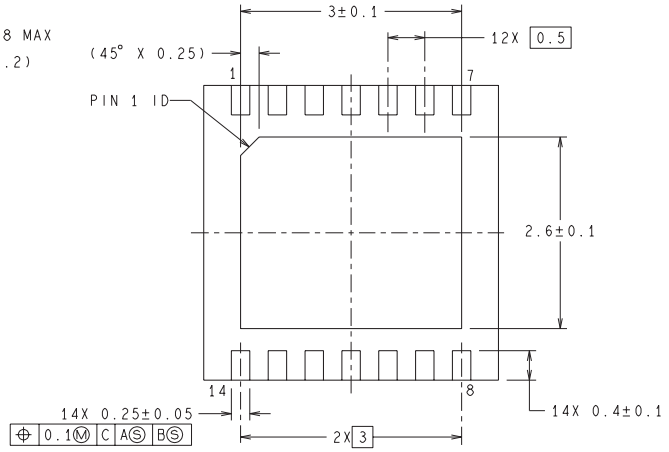



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY




SDA14B (Rev A)

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