



# LMR33610 SIMPLE SWITCHER® 3.8V~36V、1A 同期整流降圧コンバータ

## 1 特長

- 堅牢な産業用アプリケーション向けの構成
  - 入力電圧範囲: 3.8V~36V
  - 出力電圧範囲: 1V~24V
  - ピーク電流モード制御
  - 接合部温度範囲: -40°C~+125°C
  - 使いやすい SOIC パッケージ
- スケーラブルな産業用電源に最適
  - 次の製品とピン互換
    - LMR33620、LMR33630、LMR33640 (36V、2A、3A または 4A)
    - LMR36510 および LMR36520 (65V、1A または 2A)
  - 400kHz および 1.4MHz の周波数
  - 補償機能を内蔵しているためソリューションの小型化、コスト削減、設計の簡素化が可能
- 高効率のソリューション
  - ピーク効率: 95%超
  - 低いシャットダウン時静止電流: 5μA
  - 低い動作時静止電流: 25μA
- 柔軟なシステム・インターフェイス
  - パワー・グッド・フラグおよび高精度イネーブル
- WEBENCH® Power Designer により、LMR33610 を使用するカスタム設計を作成

## 2 アプリケーション

- モータ・ドライブ・システム: ドローン、AC インバータ、VF ドライブ、サーボ
- 工場およびビルディング・オートメーション・システム: PLC、HMI、HVAC システム、エレベータのメイン制御パネル
- 広 VIN DC/DC 電源

## 3 概要

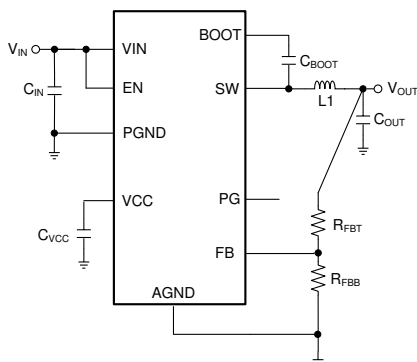
LMR33610 SIMPLE SWITCHER®レギュレータは使いやすい同期整流降圧DC/DCコンバータで、堅牢な産業用アプリケーション向けに、クラス最高の効率を実現しています。最大 36V の入力から最大 1 A の負荷電流を駆動でき、軽負荷時の効率と出力精度も優れています。パワー・グッド・フラグや高精度イネーブルなどの特長から、広範なアプリケーションにおいて、柔軟で使いやすいソリューションとなります。軽負荷時には、効率向上のため自動的に周波数をフォールドバックします。保護機能として、サーマル・シャットダウン、入力低電圧誤動作防止、サイクル単位の電流制限、ヒックアップ短絡保護機能が搭載されています。統合と内部補償により、多くの外付け部品が不要で、PCB レイアウトが単純になるようにピン配置が設計されています。本デバイスの一連の機能は、広範な最終機器の実装が簡単になるよう設計されています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LMR33610	HSOIC (8)	5.00mmx4.00mm

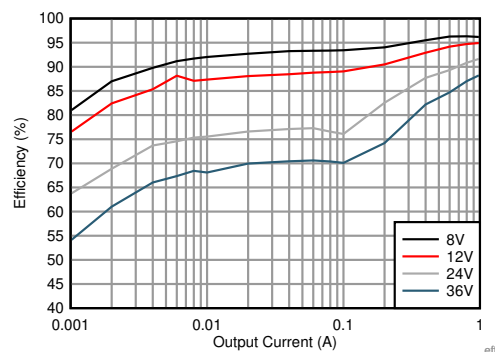
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



効率と出力電流との関係

V<sub>OUT</sub> = 5V, 400kHz



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019 年 10 月	*	初版

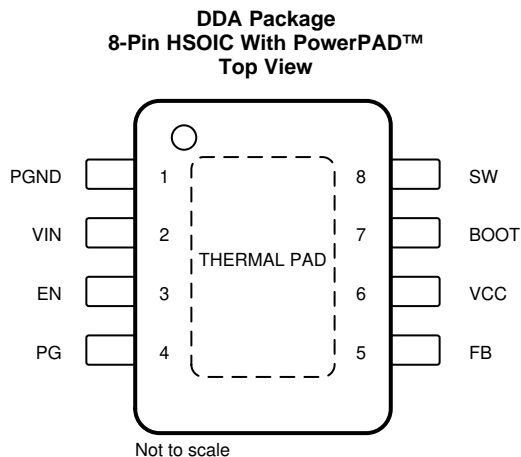
## 5 概要（続き）

LMR33610 は LMR33620、LMR33630、LMR33640 (36V、2A/3A/4A)、LMR36510 (65V、1A)、LMR36520 (65V、2A) とピン互換性があり、拡張性の高い **SIMPLE SWITCHER** 電源ファミリを構成する製品です。そのため、基板レイアウトの変更に伴うコストと労力が最小限で済みます。LMR33610 は 8 ピンの **HSOIC** パッケージで供給されます。

## 6 Device Comparison Table

DEVICE OPTION	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
LMR33610ADDAR	DDA (8-pin HSOIC) 5 × 4 mm	400 kHz	1 A	Adjustable
LMR33610BDDAR		1400 kHz	1 A	

## 7 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
2	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND.
3	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; <i>Do not float.</i>
4	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
5	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. <i>Do not float. Do not ground.</i>
6	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-μF capacitor from this pin to GND.
7	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. This simplifies the connection from the C <sub>BOOT</sub> capacitor to the SW pin.
8	SW	P	Regulator switch node. Connect to power inductor. This simplifies the connection from the C <sub>BOOT</sub> capacitor to the SW pin.
THERMAL PAD	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.

A = Analog, P = Power, G = Ground

## 8 Specifications

### 8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range<sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	−0.3	38	V
	EN to AGND <sup>(2)</sup>	−0.3	V <sub>IN</sub> + 0.3	
	FB to AGND	−0.3	5.5	
	PG to AGND <sup>(2)</sup>	0	22	
	AGND to PGND	−0.3	0.3	
	SW to PGND	−0.3	V <sub>IN</sub> + 0.3	V
	SW to PGND less than 100-ns transients	−3.5	38	
	BOOT to SW	−0.3	5.5	
	VCC to AGND <sup>(3)</sup>	−0.3	5.5	
T <sub>J</sub>	Junction temperature <sup>(4)</sup>	−40	150	°C
T <sub>stg</sub>	Storage temperature	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
- (3) Under some operating conditions the VCC LDO voltage may increase beyond 5.5 V.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM) <sup>(1)</sup>	±2500	V
		Charged-device model (CDM) <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of −40°C to 125°C (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN <sup>(2)</sup>	0	V <sub>IN</sub>	
	PG <sup>(2)</sup>	0	18	
Adjustable output voltage	V <sub>OUT</sub> <sup>(3)</sup>	1	24	V
Output current	I <sub>OUT</sub>	0	1	A
Temperature	Operating junction temperature, T <sub>J</sub> <sup>(4)</sup>	−40	125	°C

- (1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see [Electrical Characteristics](#).
- (2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
- (3) The maximum output voltage can be extended to 95% of V<sub>IN</sub>; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.
- (4) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

## 8.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		LMR33610	UNIT
		DDA (HSOIC)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	72.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	23.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	23.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).
- The value of R<sub>θJA</sub> given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the [Maximum Ambient Temperature](#) section.

## 8.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T<sub>J</sub>) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V<sub>IN</sub> = 12 V, V<sub>EN</sub> = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE</b>						
V <sub>IN</sub>	Minimum operating input voltage				3.8	V
I <sub>Q</sub>	Non-switching input current; measured at VIN pin <sup>(1)</sup>	V <sub>FB</sub> = 1.2 V		24	34	μA
I <sub>SD</sub>	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	μA
<b>ENABLE</b>						
V <sub>EN-VCC-H</sub>	EN input level required to turn on internal LDO	Rising threshold			1	V
V <sub>EN-VCC-L</sub>	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V <sub>EN-H</sub>	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V <sub>EN-HYS</sub>	Hysteresis below V <sub>EN-H</sub>	Hysteresis below V <sub>EN-H</sub> ; falling		100		mV
I <sub>LKG-EN</sub>	Enable input leakage current	V <sub>EN</sub> = 3.3 V		0.2		nA
<b>INTERNAL SUPPLIES</b>						
V <sub>CC</sub>	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V <sub>IN</sub> ≤ 36 V	4.75	5	5.25	V
V <sub>BOOT-UVLO</sub>	Bootstrap voltage undervoltage lock-out threshold <sup>(2)</sup>			2.2		V
<b>VOLTAGE REFERENCE (FB PIN)</b>						
V <sub>FB</sub>	Feedback voltage		0.985	1	1.015	V
I <sub>FB</sub>	Current into FB pin	FB = 1 V		0.2	50	nA
<b>CURRENT LIMITS<sup>(3)</sup></b>						
I <sub>ZC</sub>	Zero current detector threshold			0.01		A
<b>SOFT START</b>						
t <sub>SS</sub>	Internal soft-start time		2.9	4	6	ms
<b>POWER GOOD (PG PIN)</b>						
V <sub>PG-HIGH-UP</sub>	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

(2) When the voltage across the C<sub>BOOT</sub> capacitor falls below this voltage, the low side MOSFET is turned on to recharge C<sub>BOOT</sub>.

(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

## Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $V_{EN} = 4\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>PG-HIGH-DN</sub>	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
V <sub>PG-LOW-UP</sub>	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
V <sub>PG-LOW-DN</sub>	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t <sub>PG</sub>	Power-good glitch filter delay <sup>(4)</sup>		60		170	μs
R <sub>PG</sub>	Power-good flag R <sub>DS(on)</sub>	V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 4 V		76	150	Ω
		V <sub>EN</sub> = 0 V		35	60	
V <sub>IN-PG</sub>	Minimum input voltage for proper PG function	50-μA, EN = 0 V			2	V
V <sub>PG</sub>	PG logic low output	50-μA, EN = 0 V, V <sub>IN</sub> = 2V			0.2	V
OSCILLATOR						
f <sub>SW</sub>	Switching frequency	"A" Version	340	400	460	kHz
f <sub>SW</sub>	Switching frequency	"B" Version	1.2	1.4	1.6	MHz
MOSFETS						

(4) See [Power-Good Flag Output](#) for details.

## 8.6 Timing Characteristics

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $V_{EN} = 4\text{ V}$ .

	MIN	NOM	MAX	UNIT
$t_{ON-MAX}$		7	9	$\mu\text{s}$

## 8.7 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to  $T_J = 25^{\circ}\text{C}$  only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . *These specifications are not ensured by production testing.*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Operating input voltage range	$V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ A}$	3.8	36	V
$V_{OUT}$	Output voltage regulation for $V_{OUT} = 5\text{ V}$ <sup>(1)</sup>	$V_{OUT} = 5\text{ V}$ , $V_{IN} = 7\text{ V}$ to $36\text{ V}$ , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%	2.5%	
		$V_{OUT} = 5\text{ V}$ , $V_{IN} = 7\text{ V}$ to $36\text{ V}$ , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%	1.5%	
	Output voltage regulation for $V_{OUT} = 3.3\text{ V}$ <sup>(1)</sup>	$V_{OUT} = 3.3\text{ V}$ , $V_{IN} = 3.8\text{ V}$ to $36\text{ V}$ , $I_{OUT} = 0\text{ A}$ to max. load	-1.5%	2.5%	
		$V_{OUT} = 3.3\text{ V}$ , $V_{IN} = 3.8\text{ V}$ to $36\text{ V}$ , $I_{OUT} = 1\text{ A}$ to max. load	-1.5%	1.5%	
$I_{SUPPLY}$	Input supply current when in regulation	$V_{IN} = 12\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ A}$ , $R_{FBT} = 1\text{ M}\Omega$	25		$\mu\text{A}$
$V_{DROP}$	Dropout voltage; ( $V_{IN} - V_{OUT}$ )	$V_{OUT} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$ Dropout at -1% of regulation, $f_{SW} = 140\text{ kHz}$	150		mV
$D_{MAX}$	Maximum switch duty cycle <sup>(2)</sup>	$V_{IN} = V_{OUT} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$	98%		

(1) Deviation is with respect to  $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ .

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately:  $f_{MIN} = 1 / (t_{ON-MAX} + t_{OFF-MIN})$ .  $D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + t_{OFF-MIN})$ .



## System Characteristics (continued)

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to  $T_J = 25^{\circ}\text{C}$  only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HC}$	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
$t_{HC}$	Time between current-limit hiccup burst			94		ms
$t_D$	Switch voltage dead time			2		ns
$T_{SD}$	Thermal shutdown temperature	Shutdown temperature		165		$^{\circ}\text{C}$
		Recovery temperature		148		$^{\circ}\text{C}$

## 8.8 Typical Characteristics

Unless otherwise specified the following conditions apply:  $T_A = 25^\circ\text{C}$  and  $V_{IN} = 12\text{ V}$

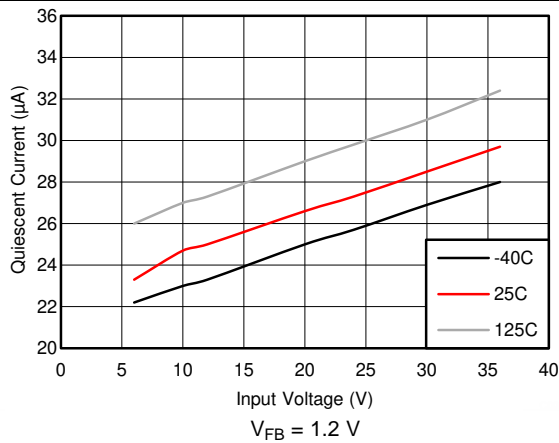


图 1. Non-Switching Input Supply Current

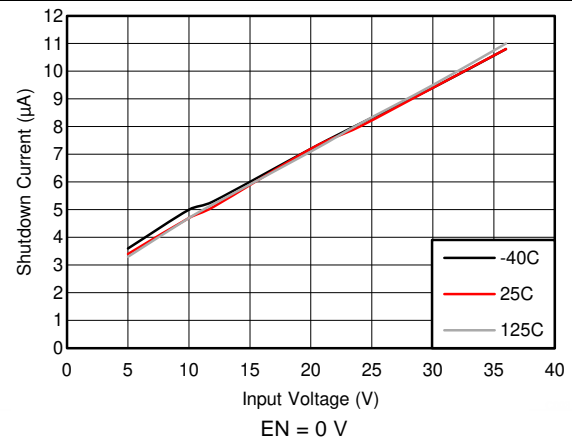


图 2. Shutdown Supply Current

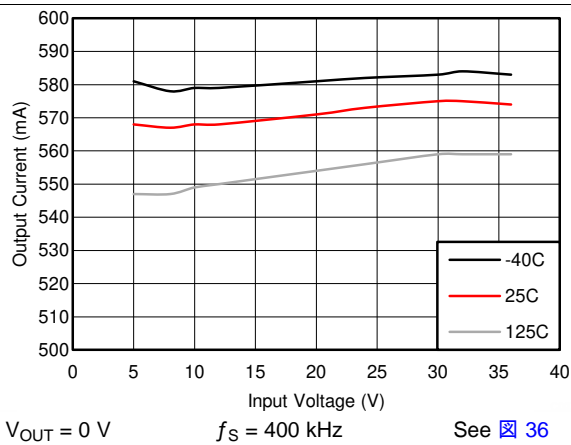


图 3. Short-Circuit Output Current

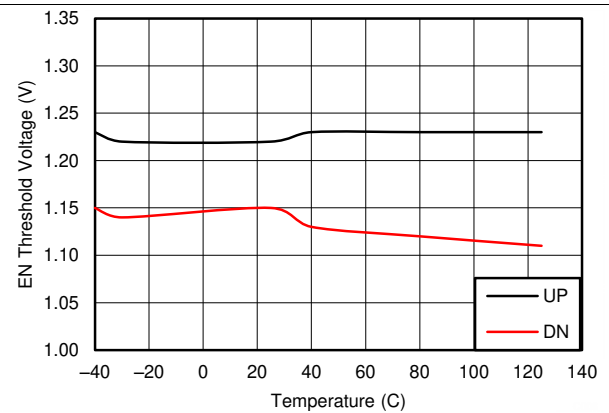


图 4. Precision Enable Thresholds

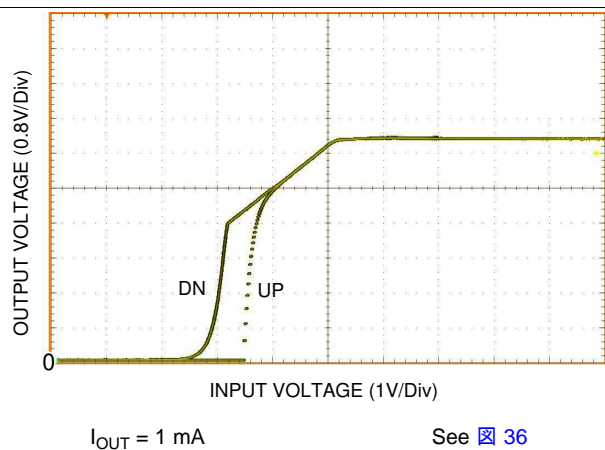


图 5. UVLO Thresholds

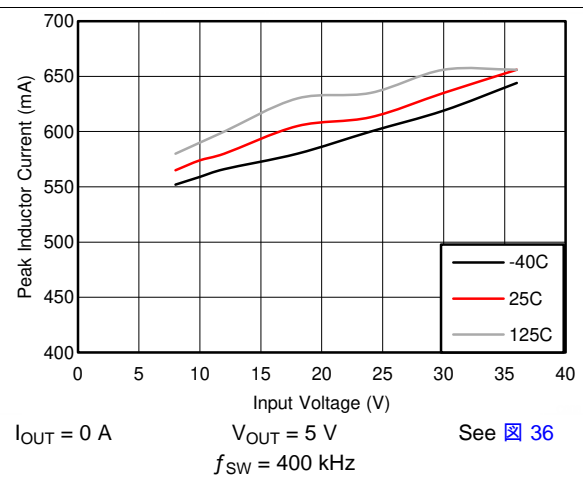


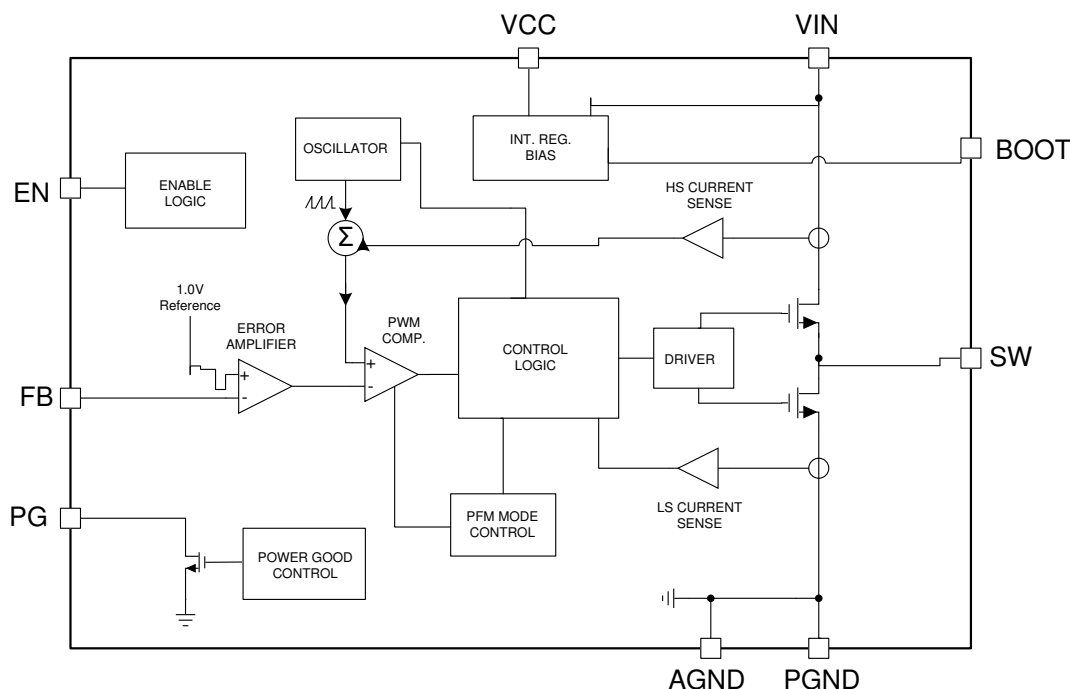
图 6.  $I_{PEAK-MIN}$

## 9 Detailed Description

### 9.1 Overview

The LMR33610 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. Advanced high speed circuitry allows the device to regulate from an input voltage of 20 V, while providing an output voltage of 3.3 V at a switching frequency of 1.4 MHz. The innovative architecture allows the device to regulate a 3.3 V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM, depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

### 9.2 Functional Block Diagram

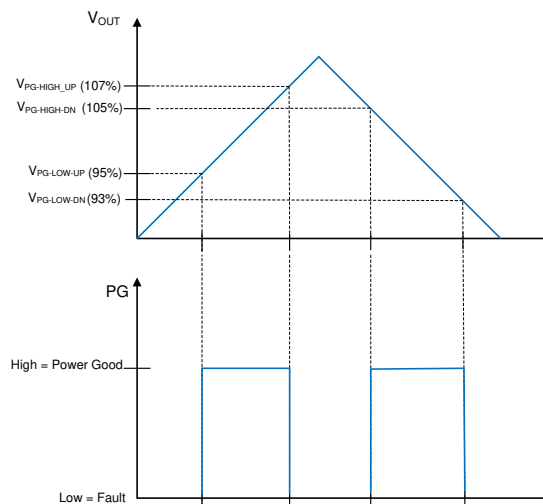


## 9.3 Feature Description

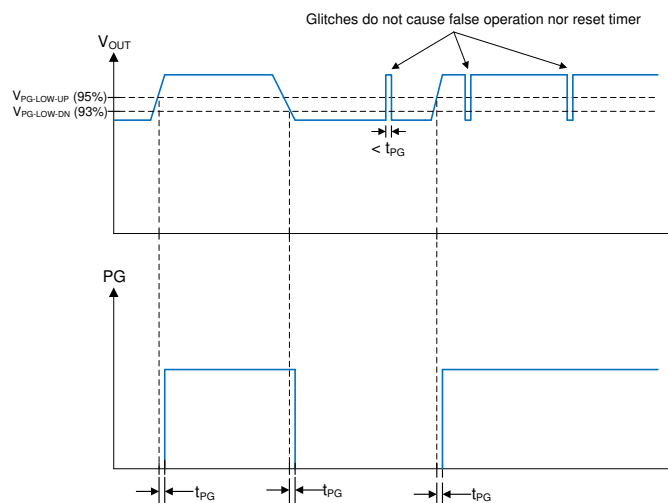
### 9.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33610 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the [Electrical Characteristics](#) table. Output voltage excursions lasting less than  $t_{PG}$  do not trip the power-good flag. Power-good operation can best be understood by reference to [Figure 7](#) and [Figure 8](#). Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V<sub>OUT</sub> through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.



**Figure 7. Static Power-Good Operation**



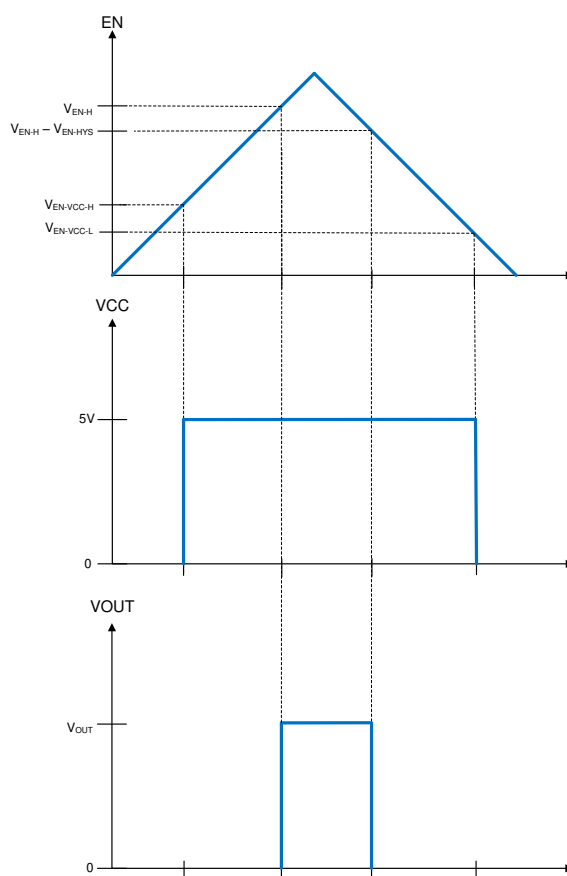
**Figure 8. Power-Good-Timing Behavior**

## Feature Description (continued)

### 9.3.2 Enable and Start-up

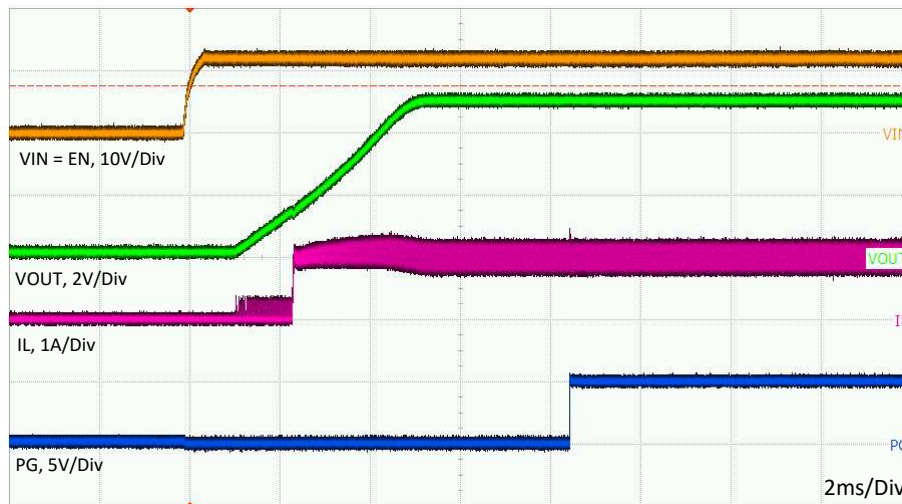
Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the [External UVLO](#) section). Applying a voltage of  $\geq V_{\text{EN-VCC\_H}}$  causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to  $V_{\text{EN-H}}$  fully enables the device, allowing it to enter start-up mode and begin the soft-start period. When the EN input is brought below  $V_{\text{EN-H}}$  by  $V_{\text{EN-HYS}}$ , the regulator stops running and enters standby mode. Further decrease in the EN voltage to below  $V_{\text{EN-VCC-L}}$  completely shuts down the device. [Figure 9](#) shows this behavior. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the [Electrical Characteristics](#) table.

The device uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. [Figure 10](#) shows a typical start-up waveform, indicating typical timings. The rise time of the output voltage is about 4 ms (see the [Electrical Characteristics](#) section).



**Figure 9. Precision Enable Behavior**

## Feature Description (continued)



**图 10. Typical Start-up Behavior**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$

### 9.3.3 Current Limit and Short Circuit

The LMR33610 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the [Glossary](#)). The typical value of this current limit is found under  $I_{ZC}$  in the section.

When the device is overloaded, the valley of the inductor current may not reach below  $I_{LIMIT}$ , (see the [Electrical Characteristics](#) table) before the next clock cycle. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit,  $I_{SC}$  (see the [Electrical Characteristics](#) table), the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 式 1.

$$I_{OUT}|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If, during current limit, the voltage on the FB input falls below about 0.4 V, due to a short circuit, the device enters hiccup mode. In this mode, the device stops switching for  $t_{HC}$  (see the [System Characteristics](#) section), or about 94 ms, and then goes through a normal restart with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in 图 11, as long as the short-circuit-condition persists. This mode of operation reduces the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode (see the [Typical Characteristics](#) section). Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in 图 12.

## Feature Description (continued)

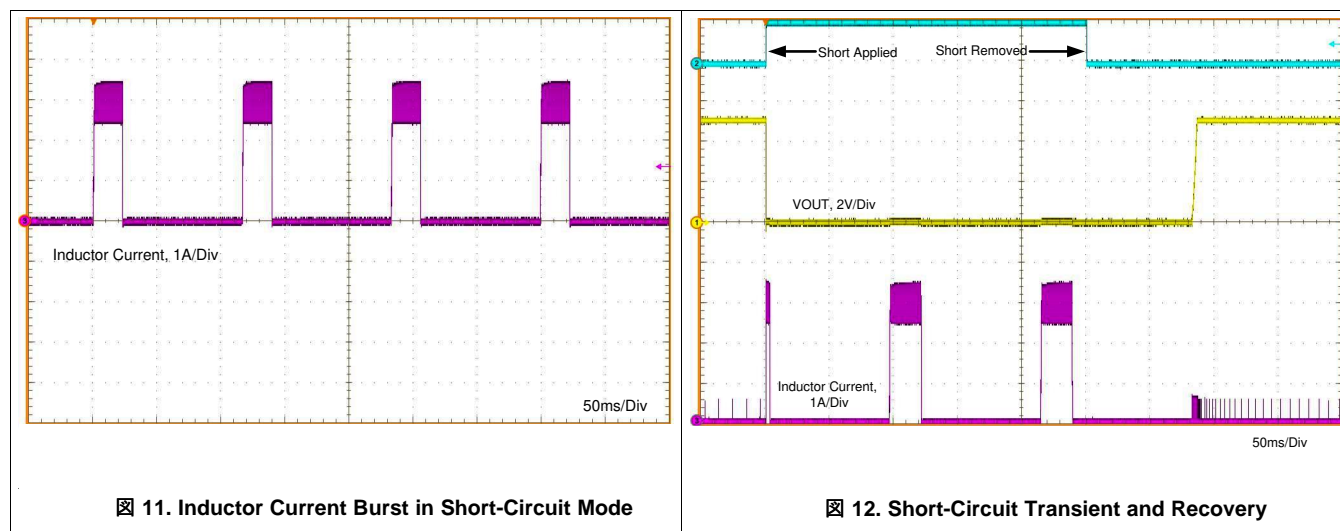


Figure 11. Inductor Current Burst in Short-Circuit Mode

Figure 12. Short-Circuit Transient and Recovery

### 9.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33610 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V, the device is ready to receive an EN signal and start up. When VCC falls below about 3 V, the device shuts down, regardless of EN status. Since the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C, the device shuts down. Restart occurs when the temperature falls to about 148°C.

## 9.4 Device Functional Modes

### 9.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in the [Application Curves](#) section. The output current at which the device changes modes depends on the input voltage, inductor value, and the nominal switching frequency. The device is in PWM mode for output currents above the curve. The device is in PFM for currents below the curve. The curves apply for a nominal switching frequency of 400 kHz and the BOM shown in the [Application Curves](#). At higher switching frequencies, the load at which the mode change occurs is greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode, the regulator operates as a constant frequency converter, using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach  $I_{PEAK-MIN}$ . The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see the [Glossary](#)). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Figure 13 and Figure 14 show typical switching waveforms in PFM and PWM. See the [Application Curves](#) section for output voltage variation with load in auto mode.

## Device Functional Modes (continued)

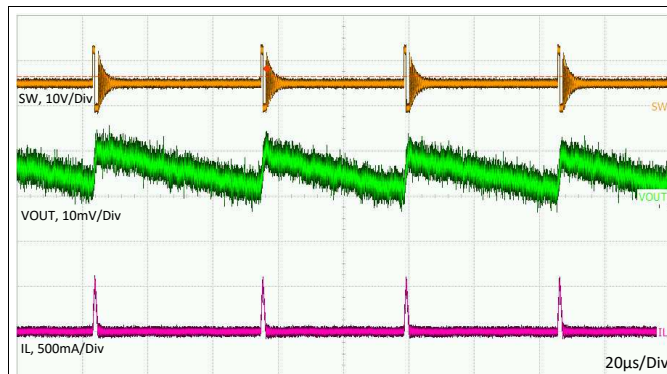


FIG 13. Typical PFM Switching Waveforms  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $I_{OUT} = 10\text{ mA}$

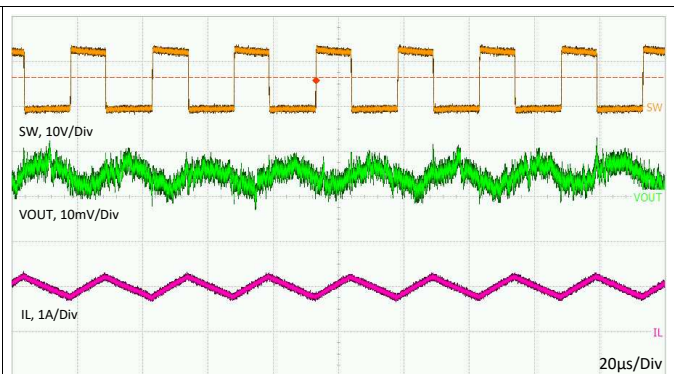


FIG 14. Typical PWM Switching Waveforms  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $f_s = 400\text{ kHz}$

### 9.4.2 Dropout

The dropout performance of any buck regulator is affected by the  $R_{DS(on)}$  of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high side MOSFET starts to approach the minimum value (see the [Timing Characteristics](#) section). Beyond this point, the switching can become erratic and the output voltage falls out of regulation. To avoid this problem, the LMR33610 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical dropout characteristics can be found in [FIG 15](#) and [FIG 16](#).

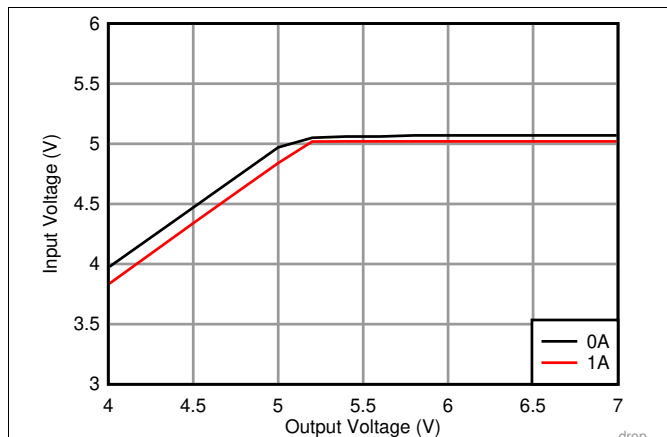


FIG 15. Overall Dropout Characteristic  
 $V_{OUT} = 5\text{ V}$

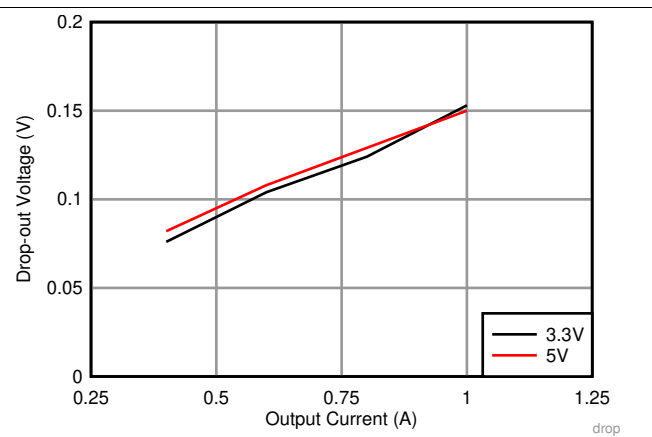


FIG 16. Typical Dropout Voltage versus Output Current in Frequency Foldback  
 $f_{sw} = 140\text{ kHz}$



## Device Functional Modes (continued)

### 9.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR33610 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use 式 2 to estimate the approximate input voltage for a given output voltage before frequency foldback occurs. The values of  $t_{ON}$  and  $f_{SW}$  can be found in the [Electrical Characteristics](#) table. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \quad (2)$$

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The LMR33610 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMR33610. Alternately, the WEBENCH Design Tool can be used to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

### 注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

### 10.2 Typical Application

Figure 17 shows a typical application circuit for the LMR33610. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, Table 2 provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application.

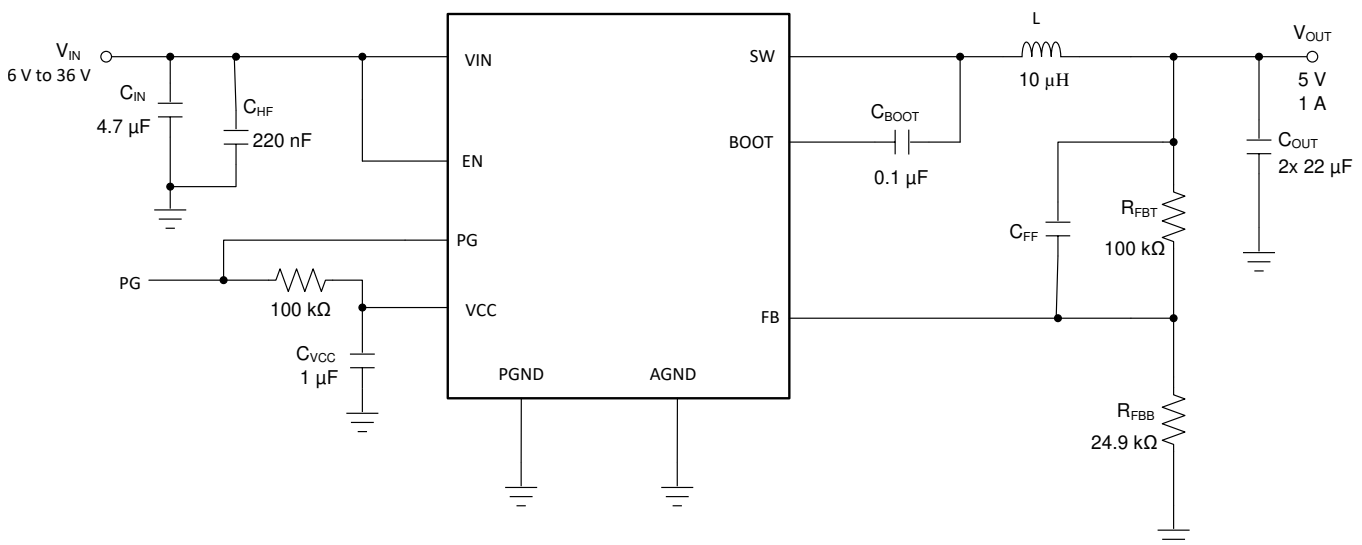


Figure 17. Example Application Circuit (400 kHz)

## Typical Application (continued)

### 10.2.1 Design Requirements

表 1 provides the parameters for the detailed design procedure example.

**表 1. Detailed Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 1 A
Switching frequency	400 kHz

**表 2. Typical External Component Values**

$f_{sw}$ (kHz)	$V_{OUT}$ (V)	L ( $\mu$ H)	$C_{OUT}$ (RATED CAPACITANCE )	$R_{FBT}$ ( $\Omega$ )	$R_{FBB}$ ( $\Omega$ )	$C_{IN} + C_{HF}$	$C_{BOOT}$	$C_{VCC}$	$C_{FF}$
400	3.3	10	2 × 22 $\mu$ F	100 k	43.2 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open
1400	3.3	2.2	1 × 22 $\mu$ F	100 k	43.2 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open
400	5	10	2 × 22 $\mu$ F	100 k	24.9 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open
1400	5	2.2	1 × 22 $\mu$ F	100 k	24.9 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open
400	12	15	2 × 22 $\mu$ F	100 k	9.09 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open
1400	12	4.7	2 × 10 $\mu$ F	100 k	9.09 k	4.7 $\mu$ F + 220 nF	100 nF	1 $\mu$ F	Open

### 10.2.2 Detailed Design Procedure

The following design procedure applies to 图 17 and 表 1.

#### 10.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the LMR33610 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WBENCH](http://www.ti.com/WBENCH).

#### 10.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors hence, a more compact design. 400 kHz was chosen for this example.

### 10.2.2.3 Setting the Output Voltage

The output voltage of LMR33610 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the table. The divider network is comprised of  $R_{FBT}$  and  $R_{FBB}$  and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage,  $V_{REF}$ . The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for  $R_{FBT}$  is 100 k $\Omega$  with a maximum value of 1 M $\Omega$ . If a 1 M $\Omega$  is selected for  $R_{FBT}$ , then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see the [C<sub>FF</sub> Selection](#) section). Once  $R_{FBT}$  is selected, use [式 3](#) to select  $R_{FBB}$ .  $V_{REF}$  is nominally 1 V (see the section for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[ \frac{V_{OUT}}{V_{REF}} - 1 \right]} \quad (3)$$

For this 5-V example,  $R_{FBT} = 100$  k $\Omega$  and  $R_{FBB} = 24.9$  k $\Omega$  are chosen.

### 10.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Use the maximum device current when selecting the ripple current for application with a much smaller maximum load than the maximum available from the device. Use [式 4](#) to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example,  $K = 0.3$  and an inductance of was found. The next standard value of was selected.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUTmax}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit,  $I_{SC}$  (see the [Electrical Characteristics](#) section). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit,  $I_{LIMIT}$ , is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit,  $I_{LIMIT}$  (see the [Electrical Characteristics](#) section). To avoid subharmonic oscillation, the inductance value must not be less than that given in [式 5](#). The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.36 \cdot \frac{V_{OUT}}{f_{SW}} \quad (5)$$

### 10.2.2.5 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements rather than the output voltage ripple. Use [式 6](#) to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[ (1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[ 1+K + \frac{K^2}{12} \cdot \left( 1 + \frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- $\Delta V_{OUT}$  = output voltage transient
- $\Delta I_{OUT}$  = output current transient
- $K$  = ripple factor from [Inductor Selection](#)

(6)

Once the output capacitor and ESR have been calculated, use [式 7](#) to check the peak-to-peak output voltage ripple,  $V_r$ .

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$

(7)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

This example requires a  $\Delta V_{OUT} \leq 250$  mV for an output current step of  $\Delta I_{OUT} = 1$  A. [式 6](#) gives a minimum value of 25  $\mu$ F and a maximum ESR of 0.21  $\Omega$ . Assuming a 20% tolerance and a 10% bias de-rating, there is a minimum capacitance of 35  $\mu$ F. This can be achieved with a bank of 2  $\times$  22- $\mu$ F, 16-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general, use a capacitor of at least 10 V for output voltages of 3.3 V or less, while a capacitor of 16 V or more must be used for output voltages of 5 V and above.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance must be limited to about 10 times the design value, or 1000  $\mu$ F, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

### 10.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 4.7  $\mu$ F of ceramic capacitance is required on the input of the LMR33610. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 220-nF ceramic capacitor must be used at the input as close as possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 4.7- $\mu$ F, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate worst case RMS value of this current can be calculated from 式 8 and must be checked against the manufacturers' maximum ratings.

$$I_{\text{RMS}} \cong \frac{I_{\text{OUT}}}{2} \quad (8)$$

#### 10.2.2.7 $C_{\text{BOOT}}$

The LMR33610 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

#### 10.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-μF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see the [Power-Good Flag Output](#) section). A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see the [Electrical Characteristics](#) section for limits. Do not short this output to ground or any other external voltage.

#### 10.2.2.9 $C_{\text{FF}}$ Selection

In some cases, a feedforward capacitor can be used across  $R_{\text{FBT}}$  to improve the load transient response or improve the loop-phase margin. This is especially true when values of  $R_{\text{FBT}} > 100 \text{ k}\Omega$  are used. Large values of  $R_{\text{FBT}}$ , in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A  $C_{\text{FF}}$  can help mitigate this effect. Use 式 9 to estimate the value of  $C_{\text{FF}}$ . The value found with 式 9 is a starting point; use lower values to determine if any advantage is gained by the use of a  $C_{\text{FF}}$  capacitor. The [Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report](#) is helpful when experimenting with a feedforward capacitor.

$$C_{\text{FF}} < \frac{V_{\text{OUT}} \cdot C_{\text{OUT}}}{120 \cdot R_{\text{FBT}} \cdot \sqrt{\frac{V_{\text{REF}}}{V_{\text{OUT}}}}} \quad (9)$$

#### 10.2.2.10 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 18. The input voltage at which the device turns on is designated  $V_{\text{ON}}$  while the turnoff voltage is  $V_{\text{OFF}}$ . First, a value for  $R_{\text{ENB}}$  is chosen in the range of 10 kΩ to 100 kΩ and then 式 10 is used to calculate  $R_{\text{ENT}}$  and  $V_{\text{OFF}}$ .

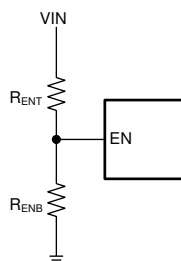


图 18. Set-Up for External UVLO Application

$$R_{ENT} = \left( \frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left( 1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right)$$

where

- $V_{ON} = V_{IN}$  turnon voltage
- $V_{OFF} = V_{IN}$  turnoff voltage

(10)

### 10.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the LMR33610 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature ( $T_J$ ) is a function of the ambient temperature, the power loss, and the effective thermal resistance,  $R_{\theta JA}$ , of the device and PCB combination. The maximum internal die temperature for the LMR33610 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures ( $T_A$ ) and larger values of  $R_{\theta JA}$  reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of  $R_{\theta JA}$  is more difficult to estimate. As stated in the [Semiconductor and IC Package Thermal Metrics Application Report](#), the value of  $R_{\theta JA}$  given in the table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1 - \eta)} \cdot \frac{1}{V_{OUT}}$$

where

- $\eta$  = efficiency

(11)

The effective  $R_{\theta JA}$  is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The HSOIC (DDA) package uses a die attach paddle or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of  $R_{\theta JA}$  versus copper board area can be found in 图 19. The copper area given in the graph is for each layer; the top and bottom layers are 2 ounce copper each, while the inner layers are 1 ounce.

图 20 and 图 21 shows the typical curves of maximum output current versus ambient temperature. This data was taken with a device and PCB combination, giving an  $R_{\theta JA}$  as noted in the graph. It must be remembered that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.

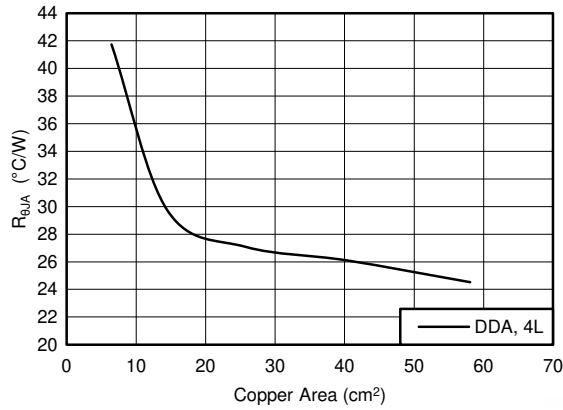


Figure 19. Typical  $R_{\theta JA}$  versus Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

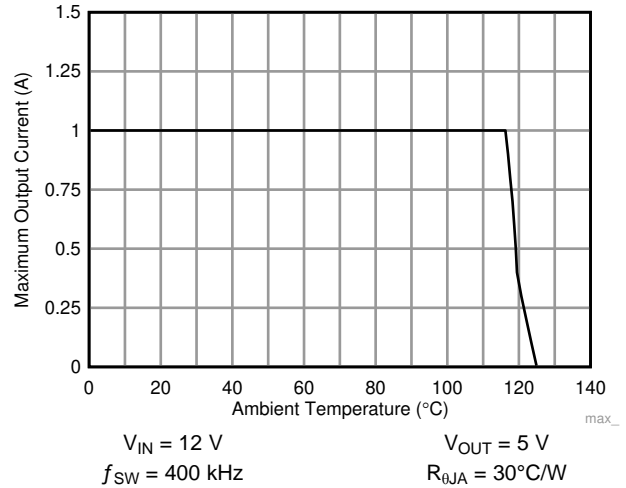


Figure 20. Maximum Output Current versus Ambient Temperature

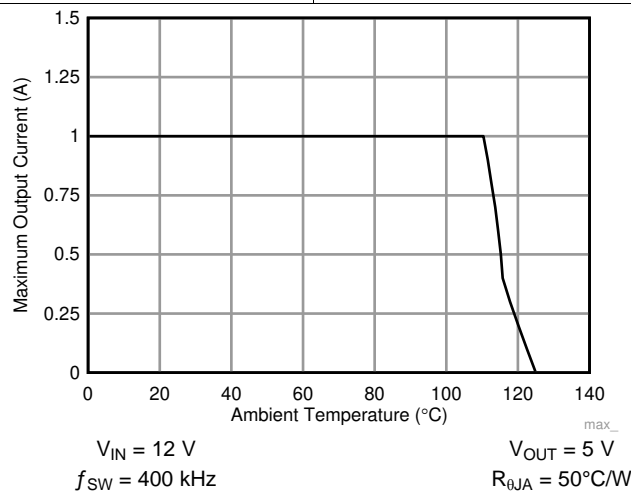


Figure 21. Maximum Output Current versus Ambient Temperature



Use the following resources as a guide to optimal thermal PCB design and estimating  $R_{\theta JA}$  for a given application environment:

- [\*Thermal Design by Insight not Hindsight Application Report\*](#)
- [\*A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report\*](#)
- [\*Semiconductor and IC Package Thermal Metrics Application Report\*](#)
- [\*Thermal Design Made Simple with LM43603 and LM43602 Application Report\*](#)
- [\*PowerPAD™ Thermally Enhanced Package Application Report\*](#)
- [\*PowerPAD™ Made Easy Application Report\*](#)
- [\*Using New Thermal Metrics Application Report\*](#)

### 10.2.3 Application Curves

Unless otherwise specified the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . [Figure 36](#) shows the circuit with the appropriate BOM from [Table 3](#).

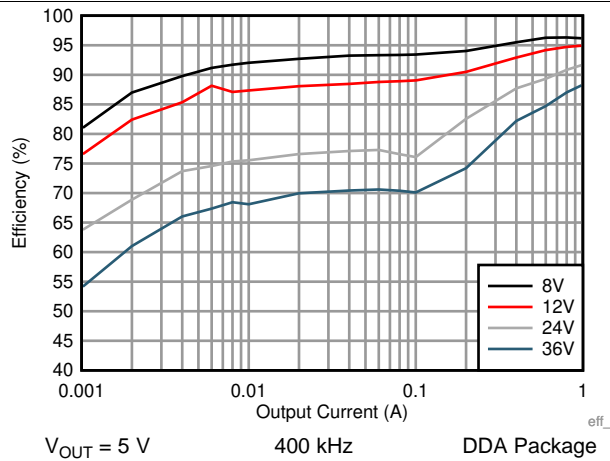


Figure 22. Efficiency

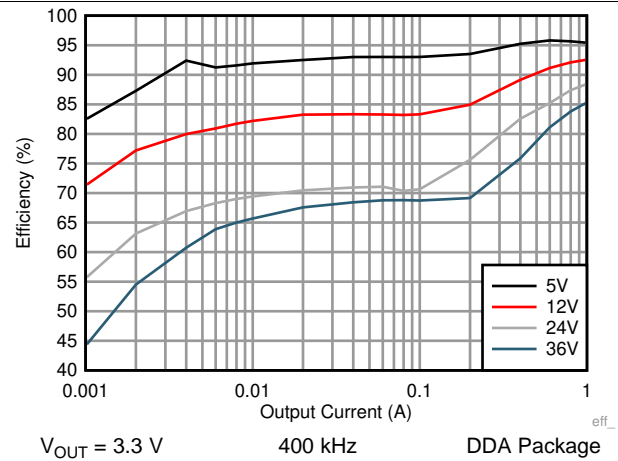


Figure 23. Efficiency

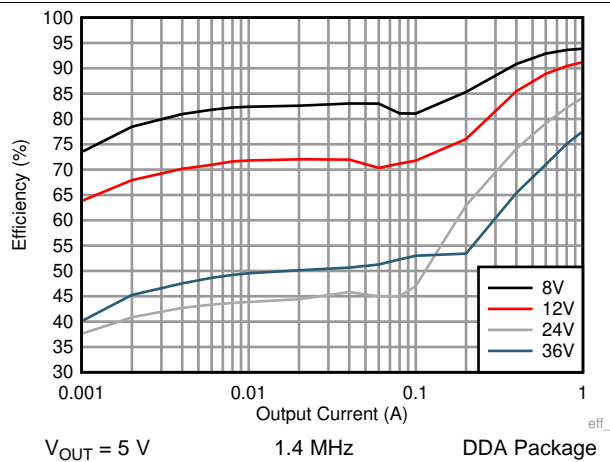


Figure 24. Efficiency

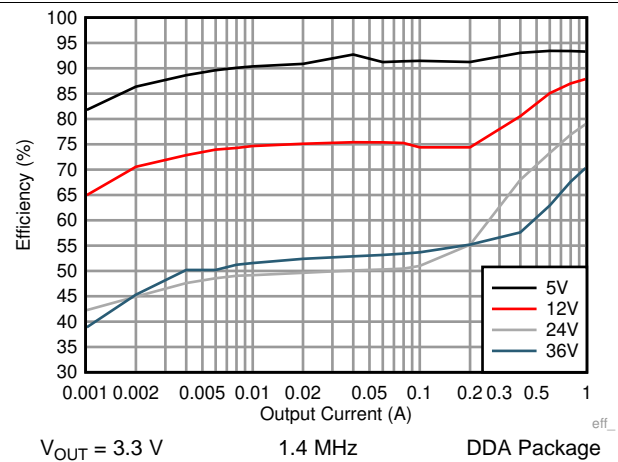


Figure 25. Efficiency

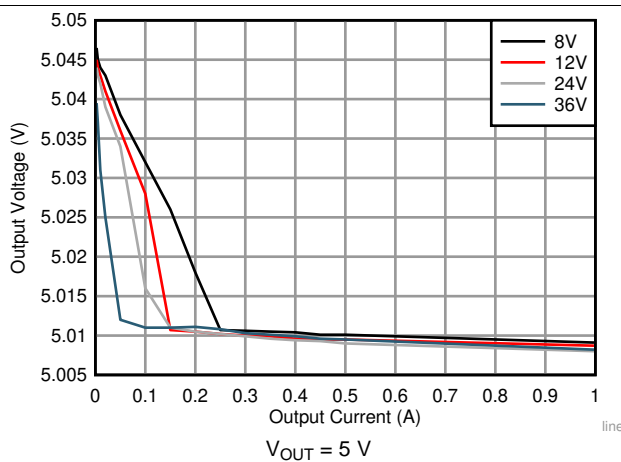


Figure 26. Line and Load Regulation

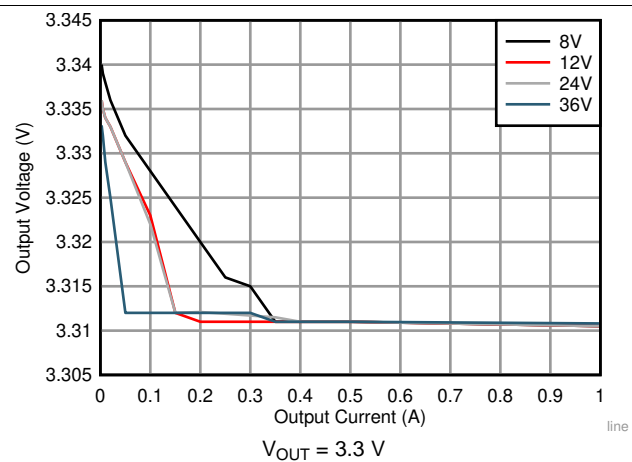


Figure 27. Line and Load Regulation

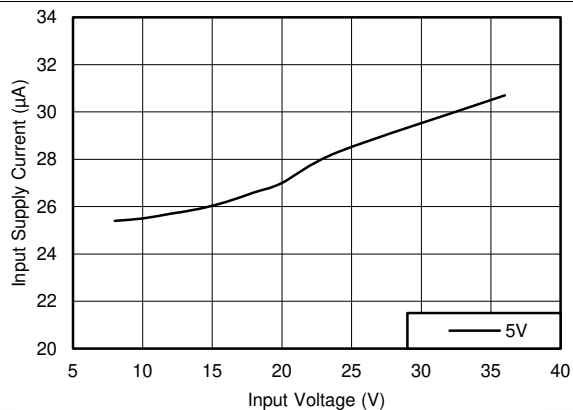


図 28. Input Supply Current

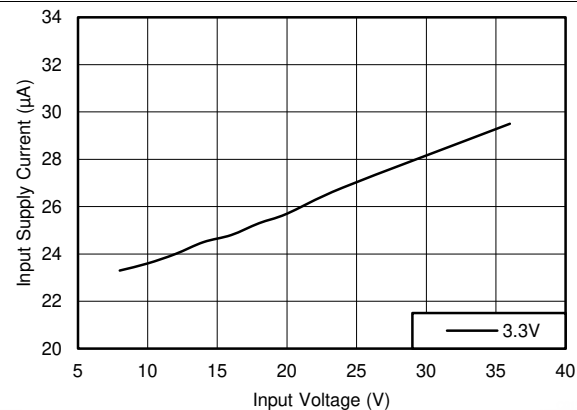


図 29. Input Supply Current

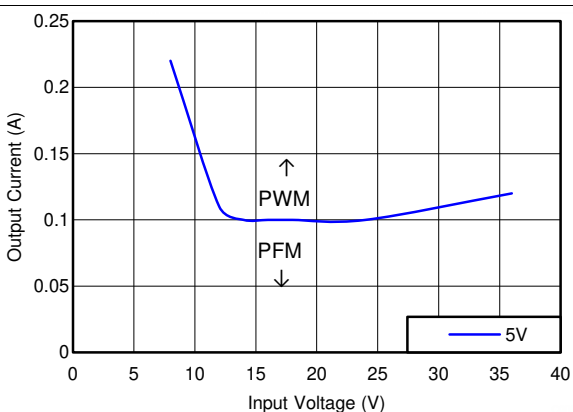


図 30. Mode Change Thresholds

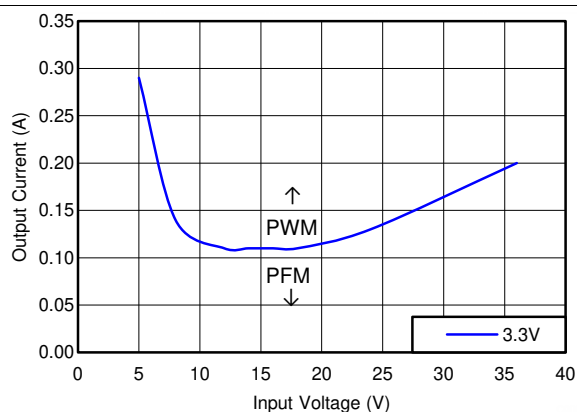


図 31. Mode Change Thresholds

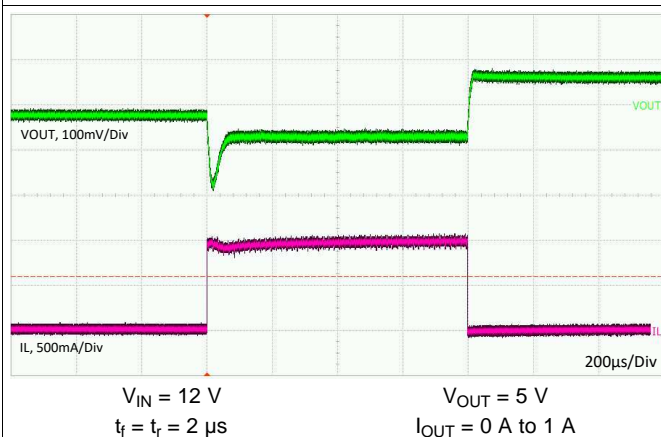


図 32. Load Transient

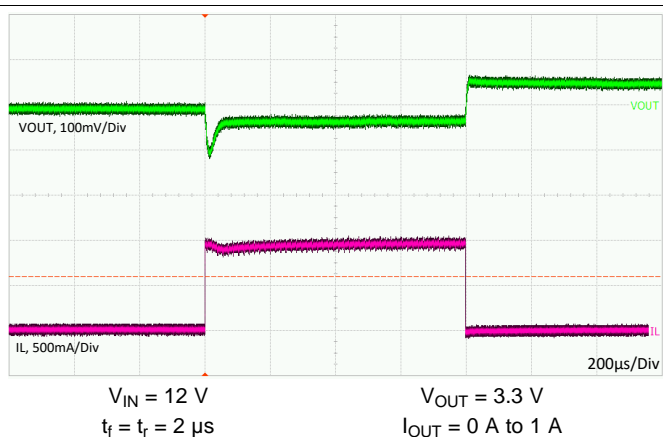
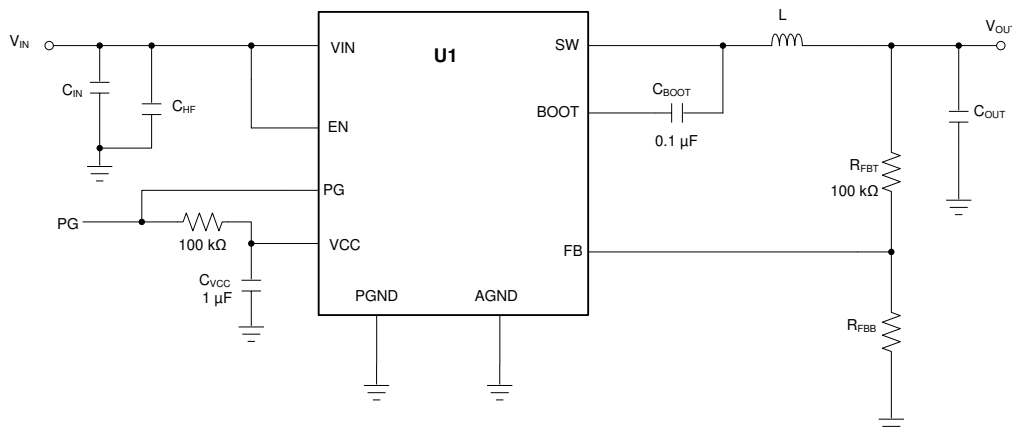
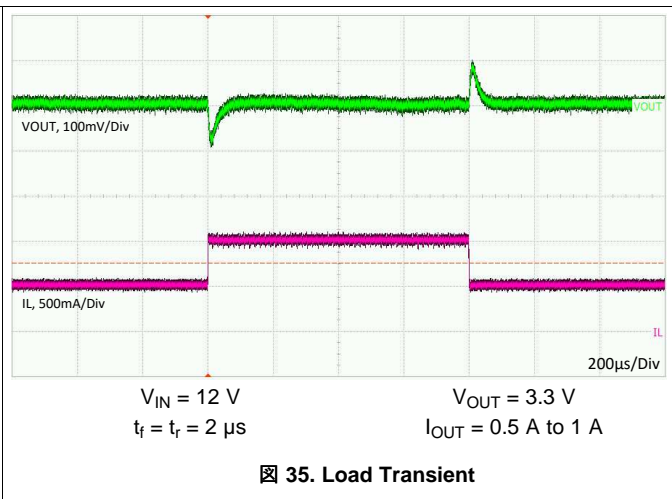
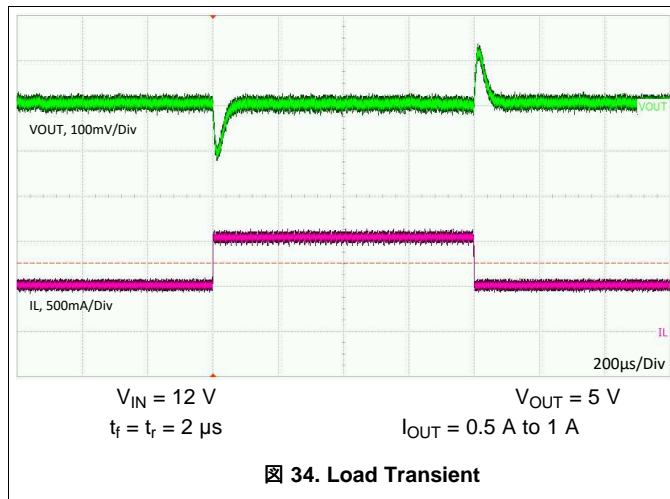


図 33. Load Transient



**表 3. BOM for Typical Application Curves DDA Package<sup>(1)</sup>**

V <sub>OUT</sub>	FREQUENCY	R <sub>FBB</sub>	C <sub>OUT</sub>	C <sub>IN</sub> + C <sub>HF</sub>	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 14 mΩ	LMR33610ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33610BDDBA
5 V	400 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	8.2 µH, 14 mΩ	LMR33610ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33610BDDBA

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

### 10.3 What to Do and What Not to Do

- Do not exceed the [Absolute Maximum Ratings](#).
- Do not exceed the [ESD Ratings](#).
- Do not exceed the [Recommended Operating Conditions](#).
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of R<sub>θJA</sub> given in the [Thermal Information](#) table to design your application. Use the information in the [Maximum Ambient Temperature](#) section.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see the [サポート・リソース](#)).

## 11 Power Supply Recommendations

The characteristics of the input supply must be compatible with the and found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. Use 式 12 to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}$$

where

- $\eta$  is the efficiency (12)

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20  $\mu$ F to 100  $\mu$ F is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The [AN-2162 Simple Success With Conducted EMI From DCDC Converters User's Guide](#) provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.

## 12 Layout

### 12.1 Layout Guidelines

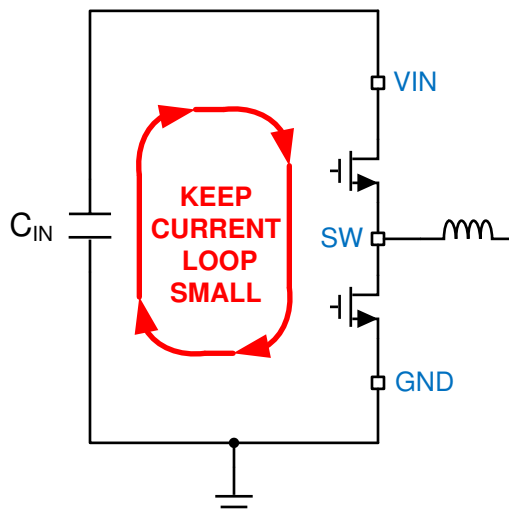
The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in [Figure 37](#). This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. [Figure 38](#) shows recommended layouts for the critical components of the LMR33610.

1. *Place the input capacitor or capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement. A wide VIN plane must be used on a lower layer to connect both of the VIN pairs together to the input supply.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C<sub>BOOT</sub> capacitor.* Place C<sub>BOOT</sub> close to the device with short, wide traces to the BOOT and SW pins.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R<sub>FBB</sub>, R<sub>FBT</sub>, and C<sub>FF</sub>, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V<sub>OUT</sub> can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and a heat dissipation path.
6. *Connect the thermal pad to the ground plane.* The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective R<sub>θJA</sub> of the application.
7. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. *Provide enough PCB area for proper heat sinking.* As stated in the [Maximum Ambient Temperature](#) section, enough copper area must be used to ensure a low R<sub>θJA</sub>, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- [Layout Guidelines for Switching Power Supplies Application Report](#)
- [Simple Switcher PCB Layout Guidelines Application Report](#)
- [Construction Your Power Supply- Layout Considerations Seminar](#)
- [Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report](#)

## Layout Guidelines (continued)



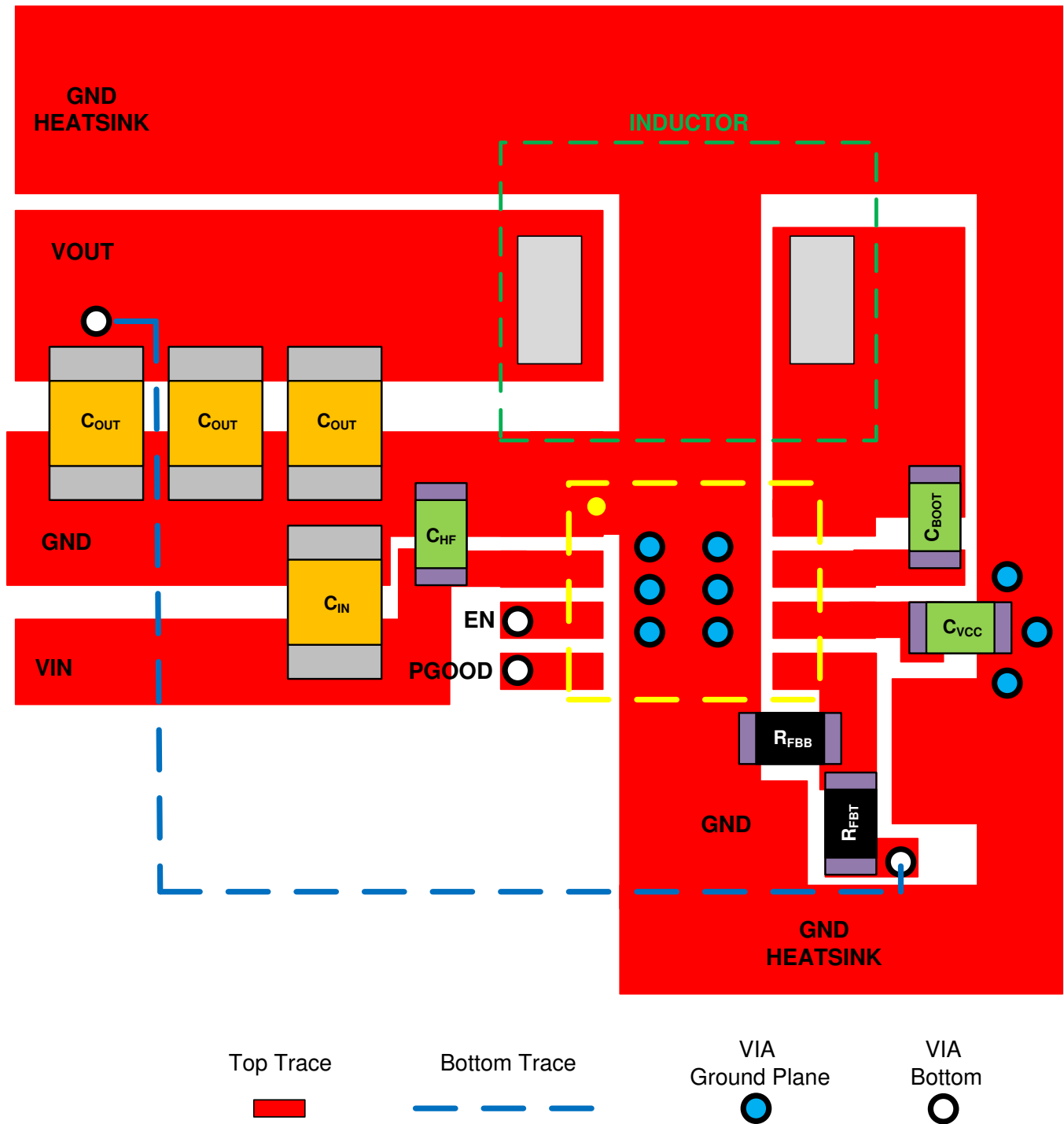
✶ 37. Current Loops with Fast Edges

### 12.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible. For system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

## 12.2 Layout Example



38. Example Layout for HSOIC (DDA) Package



## 13 デバイスおよびドキュメントのサポート

### 13.1 デバイス・サポート

#### 13.1.1 開発サポート

##### 13.1.1.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designer により、LM33610 を使用するカスタム設計を作成できます。

1. 最初に、入力電圧( $V_{IN}$ )、出力電圧( $V_{OUT}$ )、出力電流( $I_{OUT}$ )の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、[www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)でご覧になれます。

### 13.2 ドキュメントのサポート

#### 13.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[AN-2020 Thermal Design By Insight, Not Hindsight](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ『[AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[Semiconductor and IC Package Thermal Metrics](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[Thermal Design made Simple with LM43603 and LM46002](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[PowerPAD™ Thermally Enhanced Package](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[PowerPAD™ Made Easy](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[Using New Thermal Metrics](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[AN-1149 Layout Guidelines for Switching Power Supplies](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ『[AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines](#)』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『[Construction Your Power Supply- Layout Considerations Seminar](#)』(英語)
- テキサス・インスツルメンツ、『[Low Radiated EMI Layout Made Simple with LM4360x and LM4600x](#)』アプリケーション・レポート (英語)

### 13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 13.4 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 13.5 商標

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SIMPLE SWITCHER, WEBENCH are registered trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.6 静電気放電に関する注意事項



これらのデバイスは、限定的なESD (静電破壊) 保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMR33610ADDAR</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33610A
LMR33610ADDAR.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33610A
LMR33610ADDARG4	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33610A
LMR33610ADDARG4.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33610A
<a href="#">LMR33610BDDAR</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33610B
LMR33610BDDAR.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33610B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

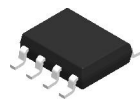
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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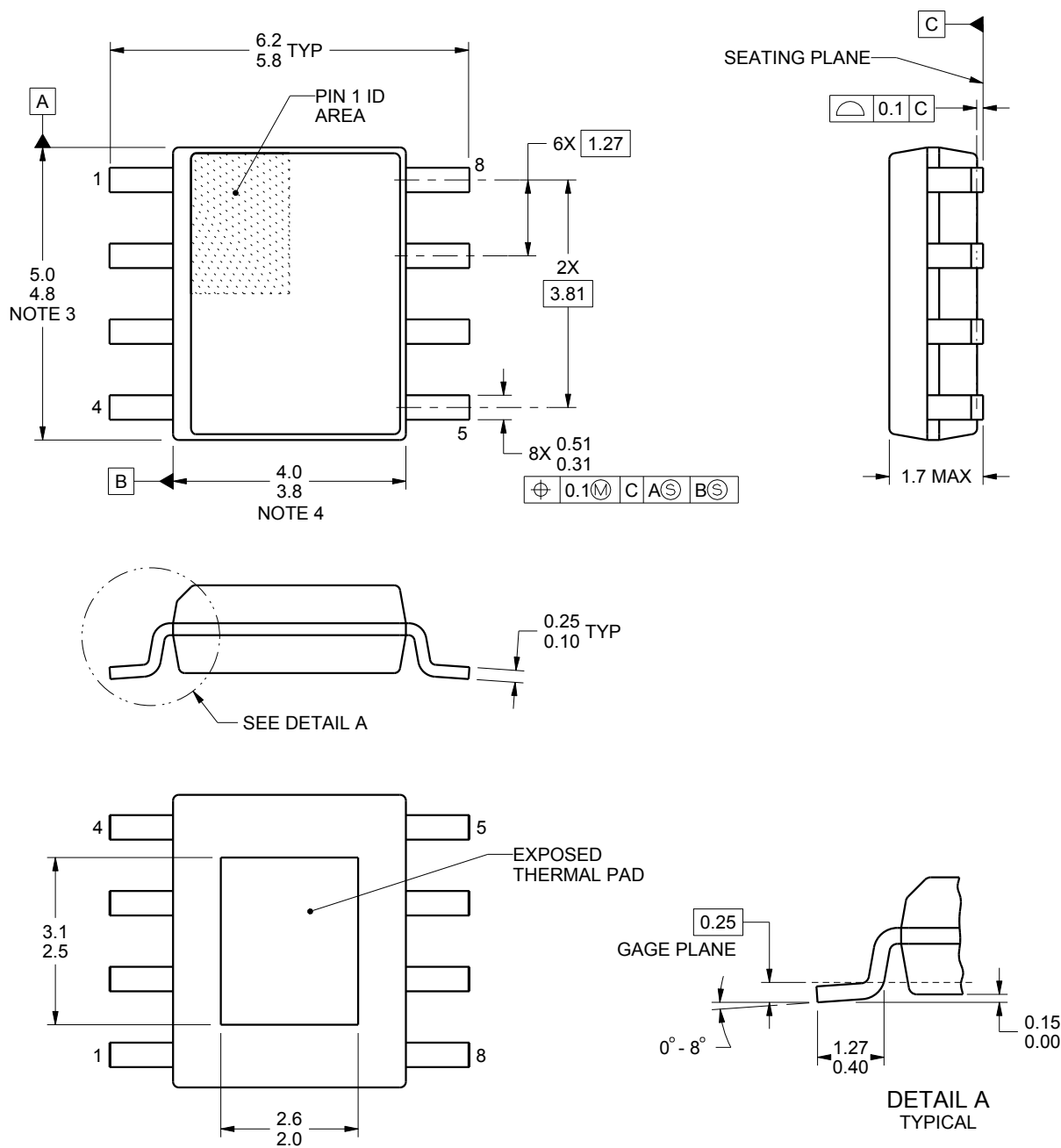
DDA0008J



# PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

## NOTES:

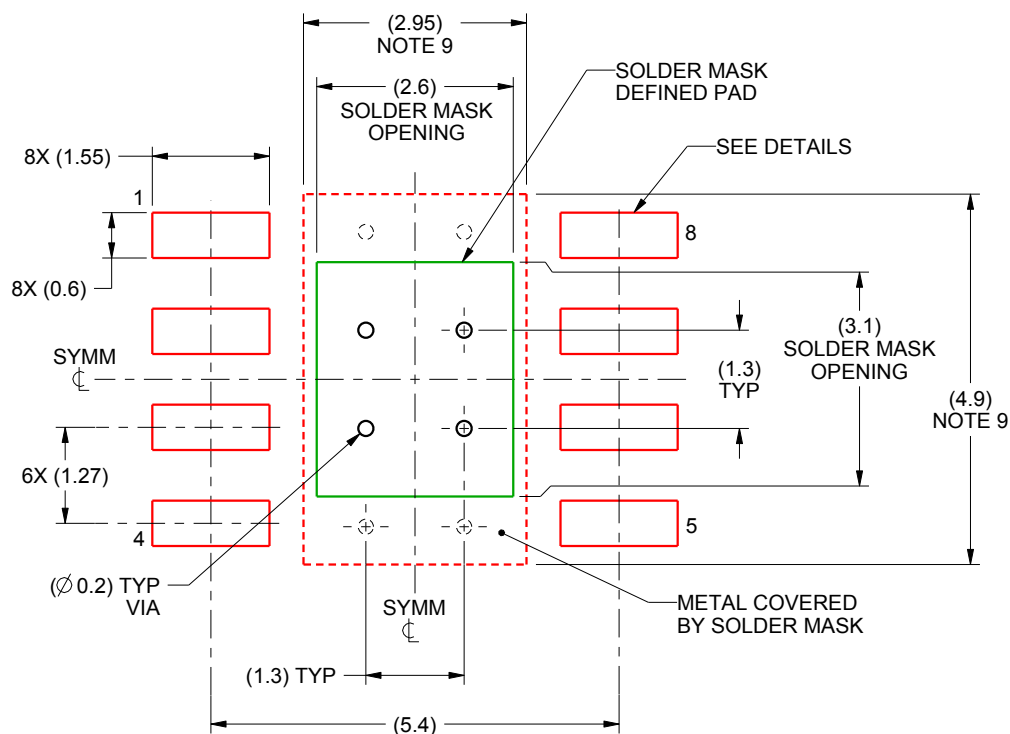
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

# EXAMPLE BOARD LAYOUT

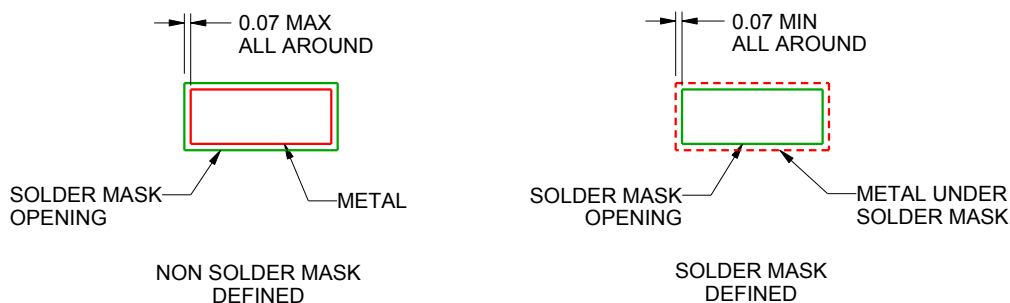
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

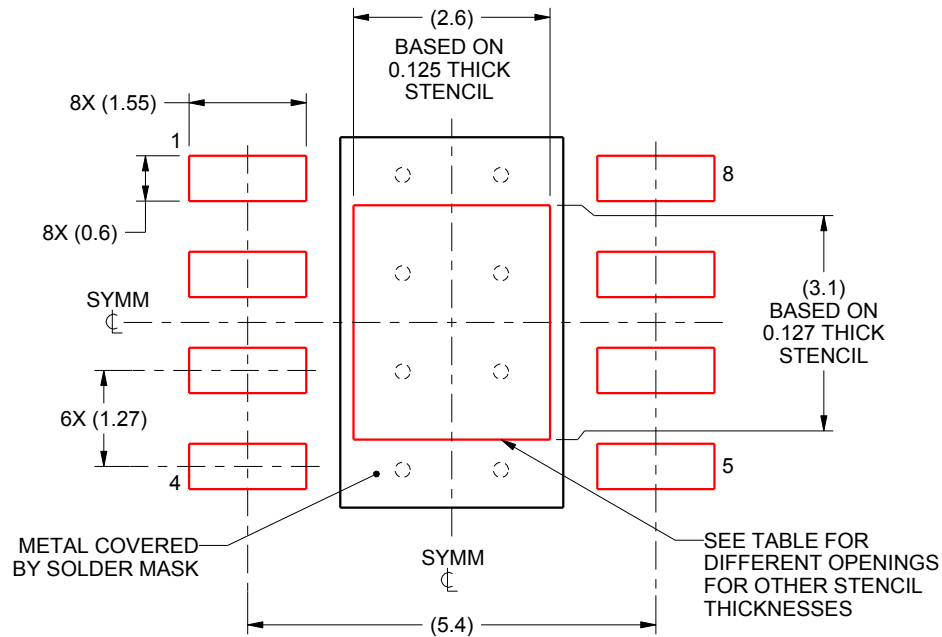
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



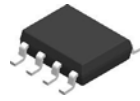
**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

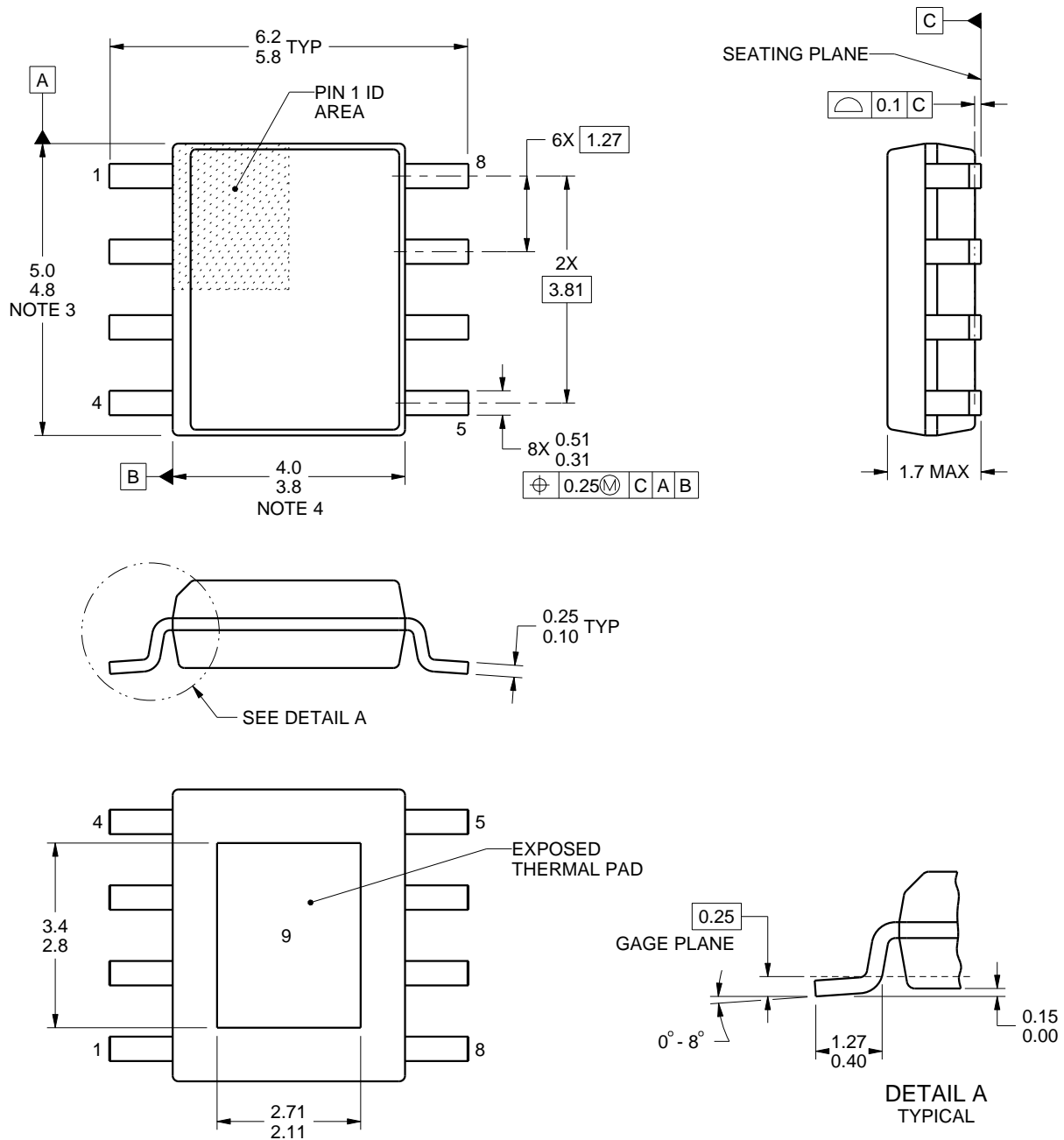
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

**DDA0008B**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

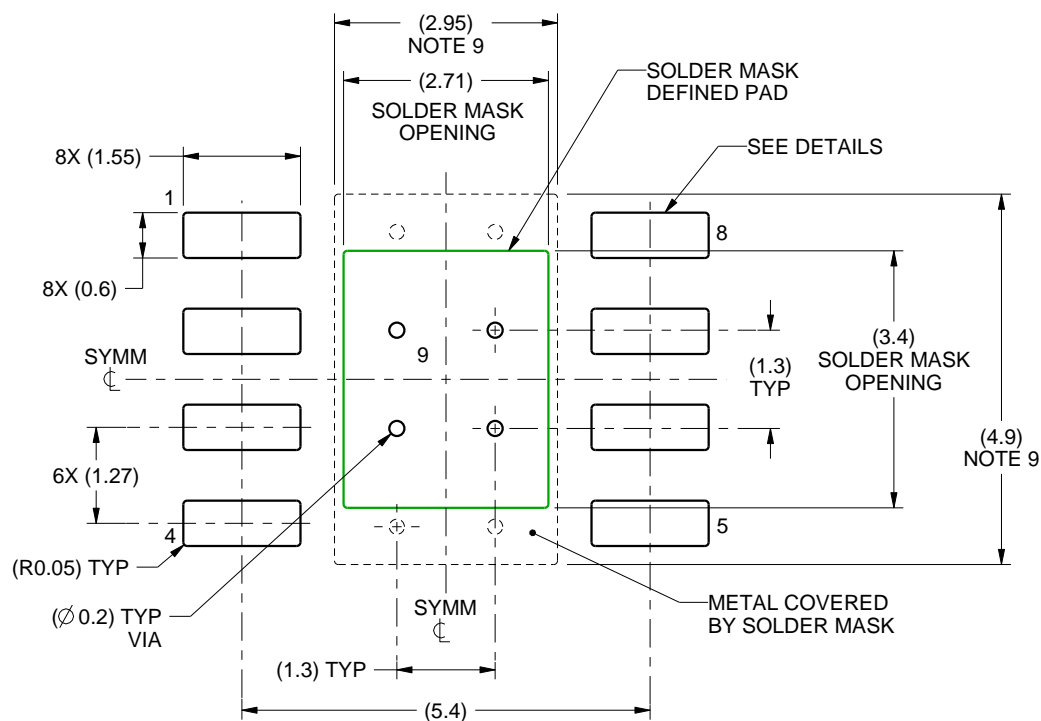


# EXAMPLE BOARD LAYOUT

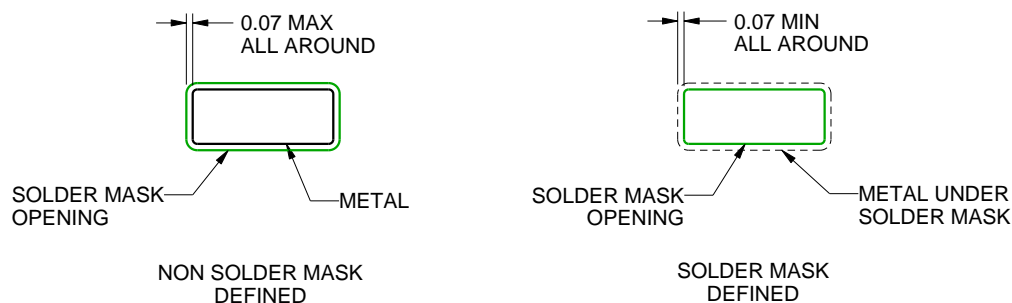
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

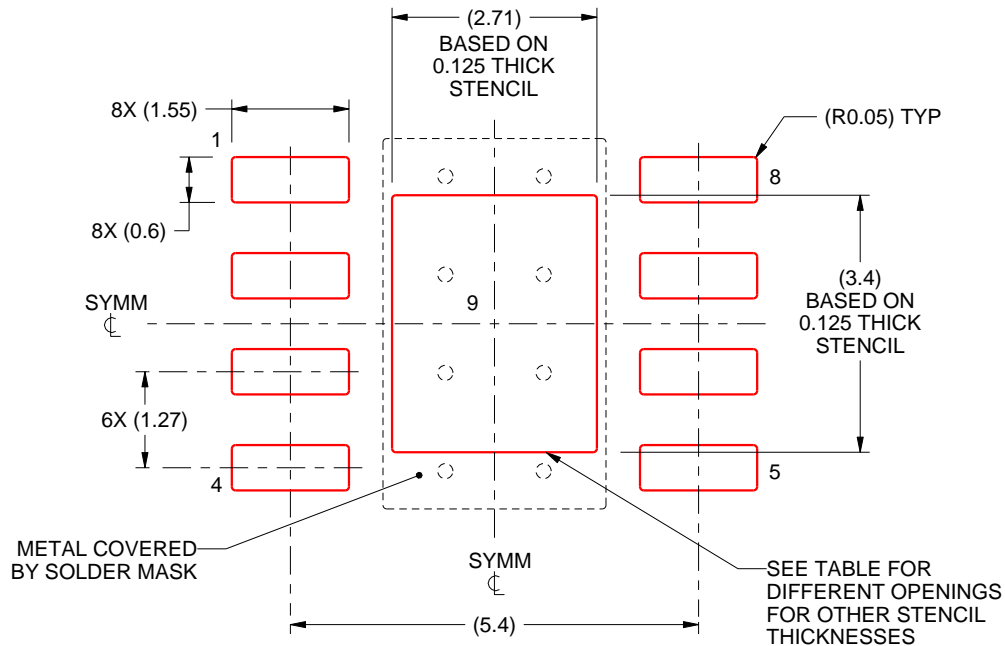
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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