LP3988 Micropower, 150-mA Ultra-Low-Dropout CMOS Voltage Regulator With Power Good

1 Features

- Input Voltage Range: 2.5 V to 6 V
- Output Current: 150 mA
- PSRR at 10 kHz: 40 dB
- Quiescent Current When Shut Down: ≤ 1µA
- Fast Turnon Time: 100 µs (Typical)
- Dropout With 150-mA load: 80 mV (Typical)
- Junction Temperature Range for Operation: −40°C to +125°C
- Power-Good Flag Output
- Logic Controlled Enable
- Thermal Shutdown and Short-Circuit Current Limit
- Stable with Ceramic and High-Quality Tantalum Capacitors

2 Applications

- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- GSM Cellular Handsets
- Portable Information Appliances
- Tiny 3.3 V ± 5% to 2.85 V, 150-mA Converter

3 Description

The LP3988 is a 150-mA low dropout regulator designed specially to meet requirements of portable battery applications. The LP3988 is designed to work with space-saving, small 1-µF ceramic capacitors. The LP3988 features a Power Good (PG) output that indicates a faulty output condition. The device is ideal for mobile phone and similar battery-powered wireless applications. It provides up to 150 mA output current from a 2.5-V to 6-V input, consuming less than 1 µA in disable mode and has fast turnon time less than 200 µs.

The LP3988 device's performance is optimized for battery-powered systems to deliver low noise, extremely low dropout voltage, and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power-supply rejection is maintained down to lower input-voltage levels common to battery-operated circuits.

The LP3988 is available in a 5-pin SOT-23 package and a 5-pin thin DSBGA package. Performance is specified for −40°C to +125°C temperature range. For all available output voltage and package options, see the Package Option Addendum (POA) at the end of the data sheet.

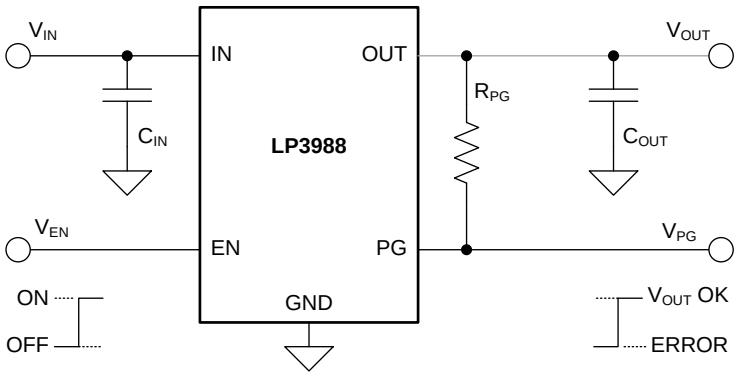
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3988	SOT-23 (5)	2.90 mm × 1.60 mm
	DSBGA (5)	1.502 mm × 1.045 mm(2)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Body size dimension is maximum.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2013) to Revision E — **Page**

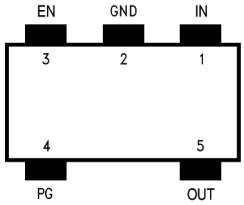
- Changed "−40°C to +80°C" to "−40°C to +125°C" under *Features* ... 1
- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Updated *Thermal Information* ... 5

Changes from Revision C (May 2013) to Revision D — **Page**

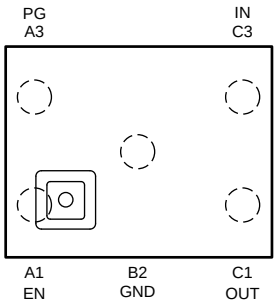
- Changed layout of National Data Sheet to TI format ... 11

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



YZR Package
5-Pin DSBGA
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DSBGA	SOT-23		
EN	A1	3	Input	Enable input logic, enable high
GND	B2	2	Ground	Common ground
IN	C3	1	Input	Input voltage of the LDO
PG	A3	4	Output	Power Good flag (output): open-drain output, connected to an external pullup resistor. Active low indicates an output voltage out of tolerance condition.
OUT	C1	5	Output	Output voltage of the LDO

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
IN pin		−0.3	6.5	V
OUT, EN, PG pins		−0.3	See(4)	V
Junction temperature, T_J			150	°C
Power dissipation(5)	SOT-23-5		469	mW
	DSBGA		441	
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The lesser of V_{IN} + 0.3 V or 6 V.
(5) The absolute maximum power dissipation depends on the ambient temperature and the $R_{\theta JA}$ value; it can be calculated using the formula: $P_D = (T_J – T_A)/R_{\theta JA}$ where $T_{J(MAX)}$ is the maximum junction temperature, $T_{A(MAX)}$ is the maximum expected ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance.The 469-mW rating for the SOT-23-5 package results from substituting the junction temperature, 150°C, for $T_{J(MAX)}$, 70°C for T_A, and 181.2°C/W for $R_{\theta JA}$. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The absolute maximum power dissipation can be increased by 5.86 mW for each degree below 70°C, and it must be derated by 5.86 mW for each degree above 70°C. Same principle applies to the DSBGA package.

6.2 ESD Ratings

			VALUE	UNIT
LP3988 IN SOT-23 PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±150	
LP3988 IN DSBGA PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	NOM	MAX	UNIT
V_{IN}		2.5(3)		6	V
V_{OUT}, V_{EN}		0		V_{IN}	V
V_{PG}		0		6	V
I_{PG}		0		500	µA
Junction temperature, T_J		–40		125	°C
Maximum power dissipation(4)	SOT-23			322	mW
	DSBGA			303	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) The minimum V_{IN} is dependant on the device output option. For $V_{OUT(NOM)}$ < 2.5 V, $V_{IN(MIN)}$ equals 2.5 V. For $V_{OUT(NOM)}$ ≥ 2.5 V, $V_{IN(MIN)}$ equals $V_{OUT(NOM)}$ + 200 mV.
(4) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 322-mW rating appearing under *Recommended Operating Conditions* for the SOT-23-5 package results from substituting the maximum junction temperature for operation, 125°C, for $T_{J(MAX)}$, 70°C for $T_{A(MAX)}$, and 181.2°C/W for $R_{\theta JA}$. More power can be dissipated at ambient temperatures below 70°C . Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 4.5 mW for each degree below 70°C, and it must be derated by 5.86 mW for each degree above 70°C. The same principle applies to the DSBGA package.

6.4 Thermal Information

THERMAL METRIC(1)		LP3988		UNIT
		DBV (SOT-23)	YZR (DSBGA)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.5	181.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.4	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.9	107.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.4	107.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF; typical values and limits are for T_J = 25°C, and minimum and maximum values and limits apply over the entire junction temperature range for operation, −40°C to +125°C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage volerance		−2		2	% of $V_{OUT(NOM)}$
		−20°C ≤ T_J ≤ 125°C, SOT-23-5	–3		3	
		SOT-23-5	–3.5		3.5	
		DSBGA	–3		3	
	Line regulation error	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V to 6 V T_J = 25°C	−0.15		0.15	%/V
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V to 6 V	–0.2		0.2	
	Load regulation error(3)	I_{OUT} = 1 mA to 150 mA, T_J = 25°C			0.005	%/mA
		I_{OUT} = 1 mA to 150 mA			0.007	
PSRR	Power Supply Rejection Ratio	V_{IN} = $V_{OUT(NOM)}$ + 1 V, f = 1 kHz, I_{OUT} = 50 mA (See Figure 11)		65		dB
		V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 10 kHz, I_{OUT} = 50 mA (See Figure 11)		45		
I_Q	Quiescent current	V_{EN} = 1.4 V, I_{OUT} = 0 mA, T_J = 25°C		85	120	µA
		V_{EN} = 1.4 V, I_{OUT} = 0 to 150 mA		140	200	
		V_{EN} = 0.4 V		0.003	1	
	Dropout voltage(4)	I_{OUT} = 1 mA		1	5	mV
		I_{OUT} = 150 mA, T_J = 25°C		80	115	
		I_{OUT} = 150 mA			150	
I_{SC}	Short circuit current limit	See(5)		600		mA
e_n	Output noise voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1 µF		220		μV_{RMS}
C_{OUT}	Output capacitor	Capacitance(6)	1		20	µF
		ESR(6)	5		500	mΩ
TSD	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
ENABLE CONTROL CHARACTERISTICS						
I_{EN}	Maximum input current at EN	V_{EN} = 0 V and V_{IN} = 6 V			0.1	µA
V_{IL}	Logic low input threshold	V_{IN} = 2.5 V to 6 V			0.5	V
V_{IH}	Logic high input threshold	V_{IN} = 2.5 V to 6 V	1.2			V

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(NOM)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(5) Short-circuit current is measured on input supply line after pulling down V_{OUT} to 95% $V_{OUT(NOM)}$.
(6) Specified by design. Not production tested. The capacitor tolerance should be ±30% or better over the full temperature range. The full range of operating conditions such as temperature, DC bias and even capacitor case size for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range.

Electrical Characteristics (continued)

Unless otherwise specified: V_{EN} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF; typical values and limits are for T_J = 25°C, and minimum and maximum values and limits apply over the entire junction temperature range for operation, −40°C to +125°C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
V_{THL}	PG low threshold (See Figure 10)	% of V_{OUT} (PG ON), T_J = 25°C	90%	93%	95%	
V_{THH}	PG high threshold (See Figure 10)	% of V_{OUT} (PG OFF), T_J = 25°C(7)	92%	95%	98%	
V_{OL}	PG output logic low voltage	I_{PULLUP} = 100 µA, fault condition		0.02	0.1	V
I_{PGL}	PG output leakage current	PG off, V_{PG} = 6 V		0.02		µA

(7) The low and high thresholds are generated together. Typically a 2.6% difference is seen between these thresholds.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
T_{ON}	PG turnon time(1), V_{IN} = 4.2 V		10		µs
T_{OFF}	PG turnoff time(1), V_{IN} = 4.2 V		10		µs

(1) Turnon time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

6.7 Typical Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF ceramic, V_{IN} = V_{OUT} + 0.2 V, T_A = 25°C, EN pin is tied to V_{IN}.

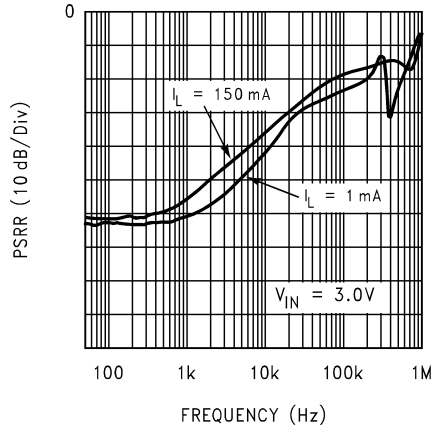


Figure 1. Ripple Rejection Ratio (LP3988-2.6 V)

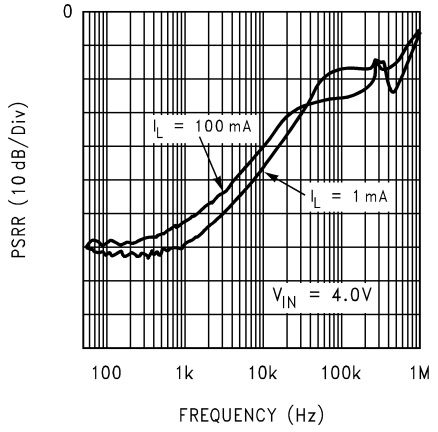


Figure 2. Ripple Rejection Ratio (LP3988-2.6 V)

Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 0.2$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

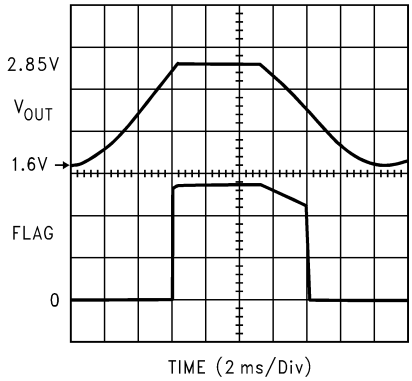


Figure 3. Power-Good Response Time (LP3988-2.85 V) (Flag Pin Pulled To V_{OUT} Through a 100-kΩ Resistor)

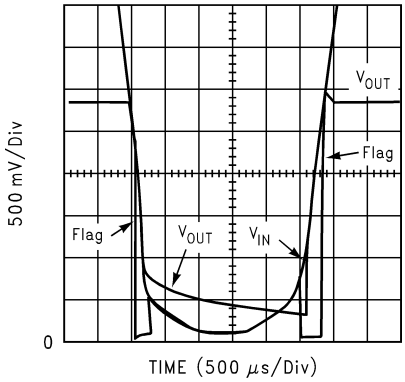


Figure 4. Power-Good Response Time (LP3988-2.85 V) (Flag Pin Pulled To V_{IN} Through a 100-kΩ Resistor)

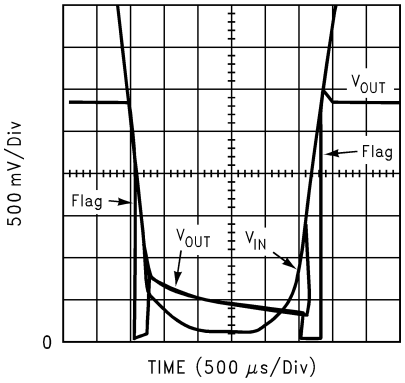


Figure 5. Power-Good Response Time (LP3988-2.85) (Flag Pin Pulled To V_{OUT} Through a 100-kΩ Resistor)

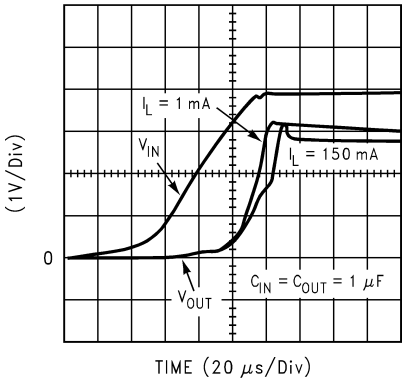


Figure 6. Power-Up Response

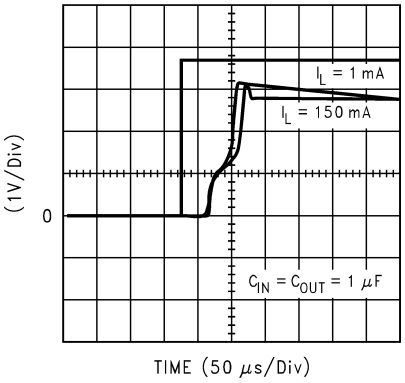


Figure 7. Enable Response

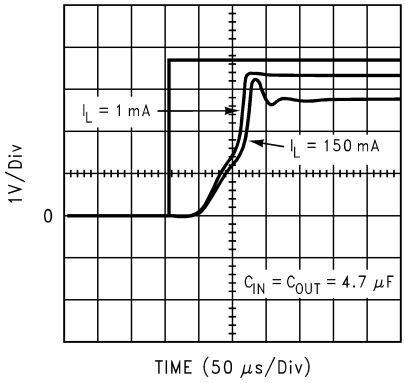


Figure 8. Enable Response

7 Parameter Measurement Information

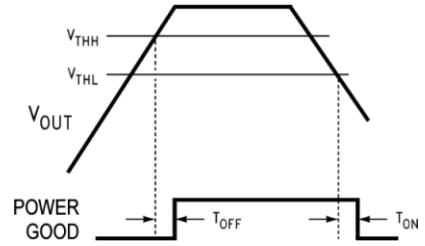


Figure 9. Power Good Flag Timing

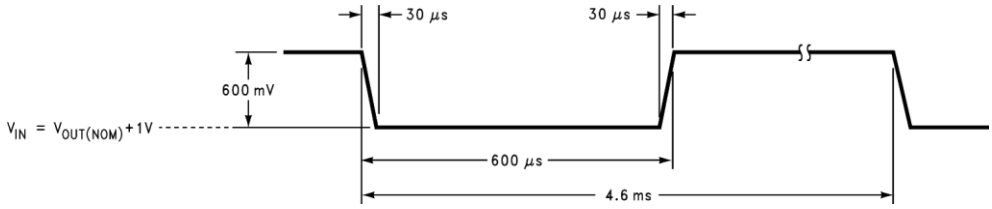


Figure 10. Line Transient Response Input Perturbation

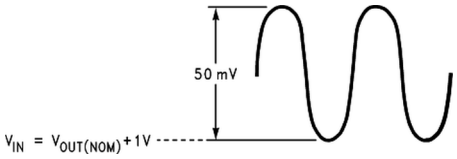


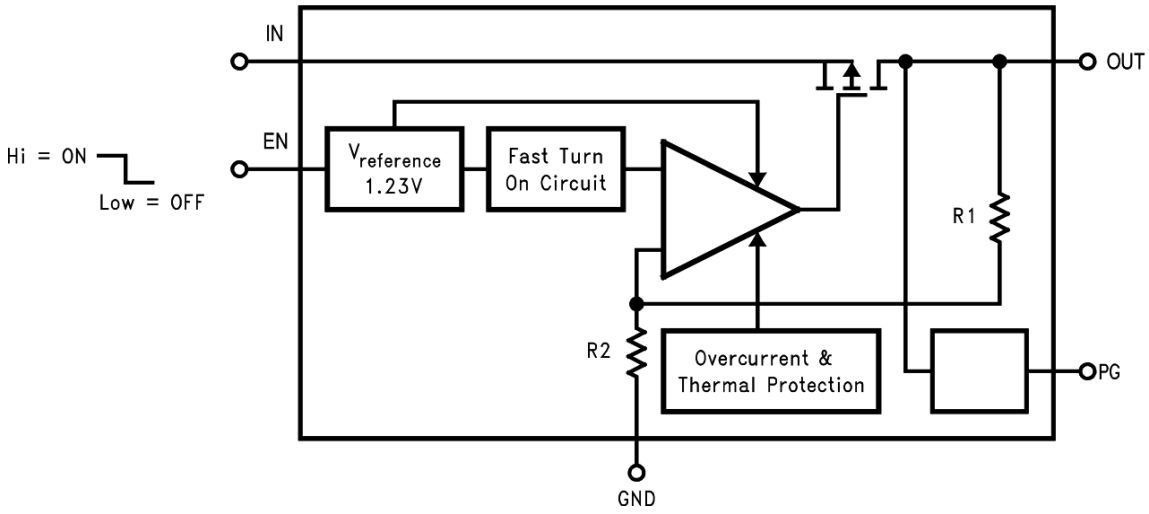
Figure 11. PSRR Input Perturbation

8 Detailed Description

8.1 Overview

The LP3988 is a combination of a low-dropout linear regulator with an enable function, along with a Power Good (PG) output. The enable function allows the LP3988 output to be selectively enabled, or disabled, as needed. The PG output goes high when the LP3988 output voltage is typically above 95% of nominal.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN)

A high input on the EN pin ($V_{EN} \geq V_{IH}$) actives the device which turns the regulator to an ON state. A low input on the EN pin ($V_{EN} \leq V_{IL}$) disables the device which turns the regulator to an OFF state. Operating with V_{EN} between the V_{IL} and the V_{IH} thresholds is not recommended as the device status cannot be assured. For self-bias applications where the EN function is not needed, connect the EN pin to the IN pin.

8.3.2 Regulated Output (OUT)

The OUT pin is the regulated output voltage based on the internally pre-programmed voltage. The output has current limitation. In the event that the regulator drops out of regulation due to low input voltage, the output tracks the input minus a drop based on the load current. There is no UVLO circuitry. Device behavior is undefined when V_{IN} is below the minimum operating input voltage of either 2.5 V, or V_{OUT} + 200 mV, whichever is greater.

8.3.3 Power Good (PG) Output

The PG pin is an open-drain output and can be pulled up to any 6 V, or lower rail through an external pullup resistor. The PG pin is high-impedance when V_{OUT} is greater than the PG trip high threshold (V_{THH}). If V_{OUT} is less than the PG trip low threshold (V_{THL}), the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND. The behavior of the power-good feature is not ensured when V_{IN} is less than 2.5 V.

8.3.4 PG Delay Time

The power-good delay times (t_{ON}, t_{OFF}) are defined as the time period from when V_{OUT} crosses either the PG high trip threshold voltage (V_{THH}), or the PG low trip threshold voltage (V_{THL}), to when the PG output changes to the appropriate state. The power-good delay times are set internally, and both are typically 10 µs. There is no external adjustment available to alter the delay times.

Feature Description (continued)

8.3.5 Current Limit

The fixed current limit (I_{SC}) of the LP3988 helps protect the regulator during output fault conditions. The maximum amount of current the device can source is typically 600 mA, and is largely independent of input and output voltage. For reliable operation, do not operate the device in current limit for extended periods of time. Depending on power dissipation, thermal resistance, and ambient temperature, operating at the current limit may activate the thermal shutdown circuitry.

8.3.6 Thermal Shutdown (T_{SD})

Thermal shutdown (T_{SD}) protection disables the output when the junction temperature rises to approximately 160°C, This shutdown causes the device dissipation to go to zero, which allows the device to cool. When the device junction temperature cools to approximately 140°C, the output circuitry is automatically enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating. The thermal shutdown circuitry of the LP3988 has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the LP3988 device in T_{SD} may degrade device reliability and lifetime.

8.3.7 Fast Turnon Time

The LP3988 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turnon time.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage (V_{IN}) is at least either 2.5 V, or V_{OUT} + 200 mV, whichever is greater.
- The enable voltage (V_{EN}) is at least 1.2 V (V_{IH}).
- The output current is no more than the maximum rated current of 150 mA.
- The device junction temperature (T_J) is no more than the maximum specified operating junction temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage (V_{DO}), but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (PMOS transistor), no longer controls the current through the LDO. Line or load transients while operating in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- V_{EN} is no more than 0.6 V (V_{IL}).
- T_J is greater than the thermal shutdown temperature.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3988 voltage regulator offers the benefit of ultra-low-dropout voltage, low noise, very low standby current, and miniaturized surface-mount packaging. The LP3988 is designed for continuous, or sporadic (power backup), battery-operated applications where very low standby current is critical to extending system battery life.

9.2 Typical Application

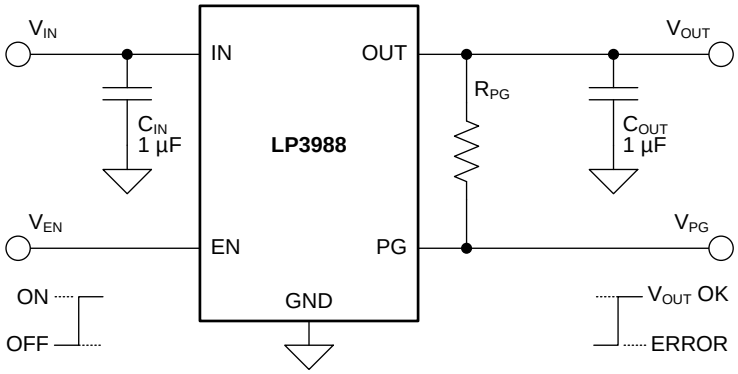


Figure 12. LP3988 Typical Application

9.2.1 Design Requirements

For typical CMOS voltage regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Output voltages	various
Output current	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitors

Like any low-dropout regulator, the LP3988 requires external capacitors for regulator stability. The LP3988 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2 Input Capacitor

An input capacitance of at least 1 µF is required between the LP3988 IN pin and ground (the amount of the capacitance may be increased without limit). This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is at least 1 µF over the entire operating temperature range.

9.2.2.3 Output Capacitors

The LP3988 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1-µF to 22-µF range with 5-mΩ to 500-mΩ ESR range is suitable in the LP3988 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR value which is within a stable range (5 mΩ to 500 mΩ).

9.2.2.4 No-Load Stability

The LP3988 remains stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

9.2.2.5 Capacitor Characteristics

The LP3988 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3988.

Capacitance of the ceramic capacitor can vary with temperature. Most large-value ceramic capacitors (around 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C. A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

9.2.2.6 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT(MAX)} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the DSBGA (YKA) package, the primary conduction path for heat is through the four bumps to the PCB.

On the SOT-23 (BDV) package, the primary conduction path for heat is through the device leads to the PCB, predominately device lead 2 (GND). It is recommended that the trace from lead 2 be extended under the package body and connected to an internal ground plane with thermal vias.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

9.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 1.
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 1.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the TI Application Report: *Semiconductor and IC Package Thermal Metrics* (SPRA953), available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report: *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), available for download at www.ti.com.

9.2.3 Application Curves

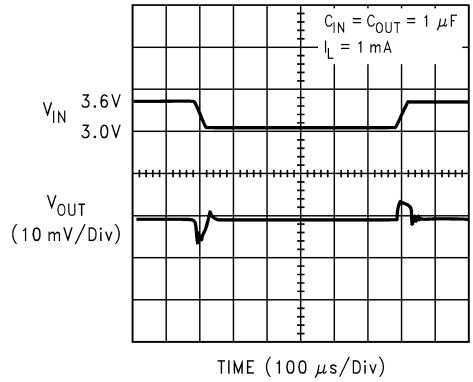


Figure 13. Line Transient Response (LP3988-2.85 V)

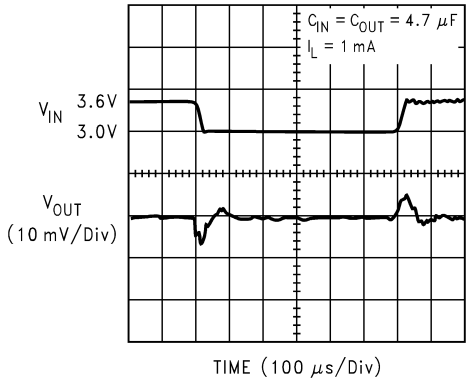


Figure 14. Line Transient Response (LP3988-2.85 V)

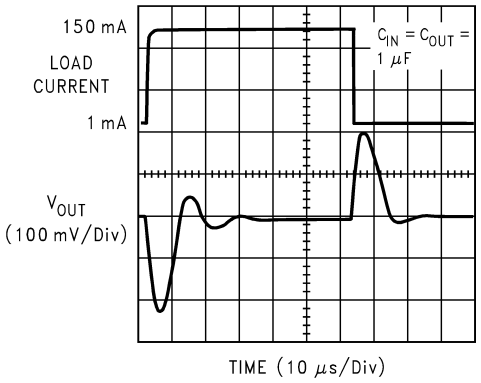


Figure 15. Load Transient Response

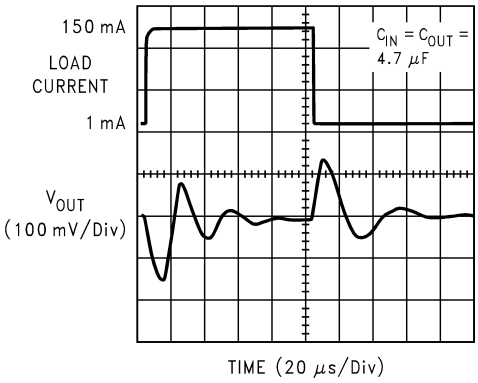


Figure 16. Load Transient Response

10 Power Supply Recommendations

The LP3988 device is designed to operate from an input supply voltage range of 2.5 V to 6 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP3988 output voltage is well regulated and dynamic performance is optimum, the input supply voltage is recommended to be at least the greater of either V_{OUT} + 200 mV, or 2.5 V.

11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP3988 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP3988.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP3988 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP3988 GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths, narrow trace widths, and/or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

The PG pin pullup resistor should be connected to the LP3988 OUT pin, with the pullup resistor located as close to the PG pin as is practical.

11.2 Layout Examples

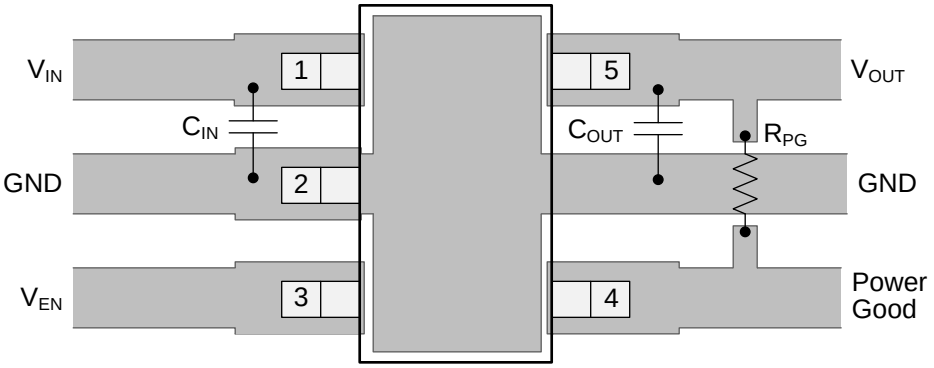


Figure 17. LP3988 SOT-23 Layout Example

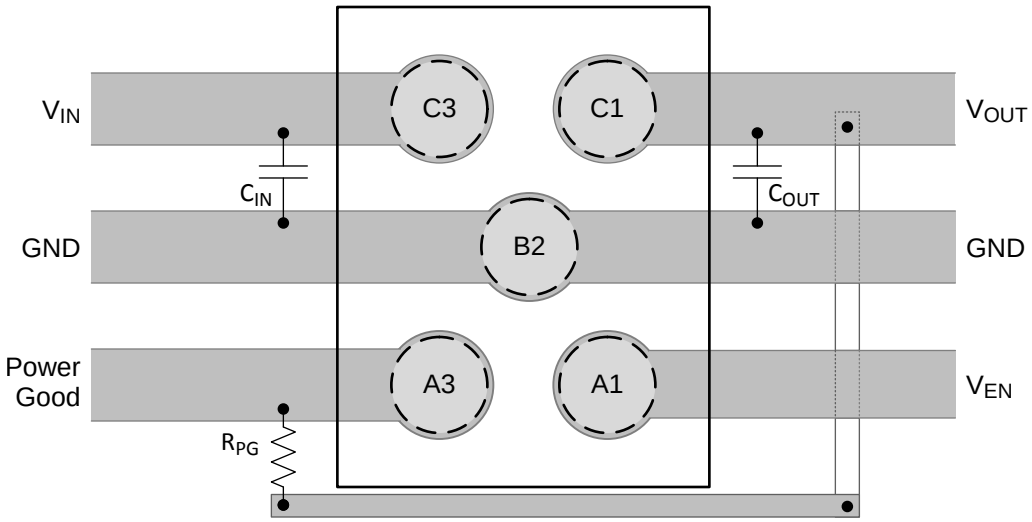


Figure 18. LP3988 DSBGA Layout Example

11.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

12 Device and Documentation Support

12.1 Related Documentation

For additional information, see the following:

- TI Application Note *DSBGA Wafer Level Chip Scale Package* (SNVA009)
- TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- TI Application Report *Using New Thermal Metrics* (SBVA025)
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3988IMF-2.5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LFSB
LP3988IMF-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LFAB
LP3988IMF-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	LH5B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LP3988 :

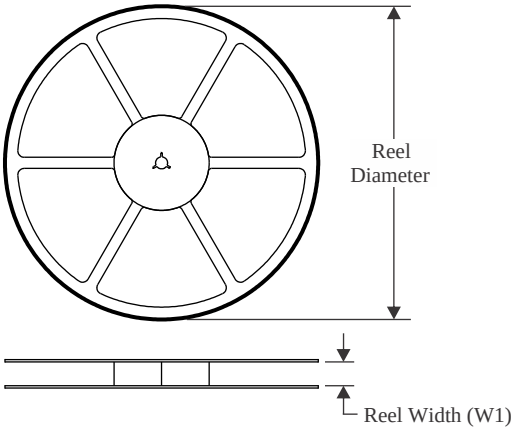
- Automotive : LP3988-Q1

NOTE: Qualified Version Definitions:

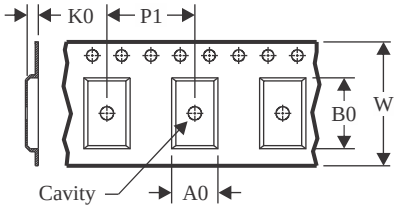
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

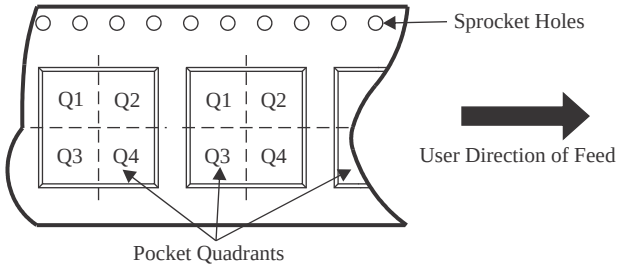


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

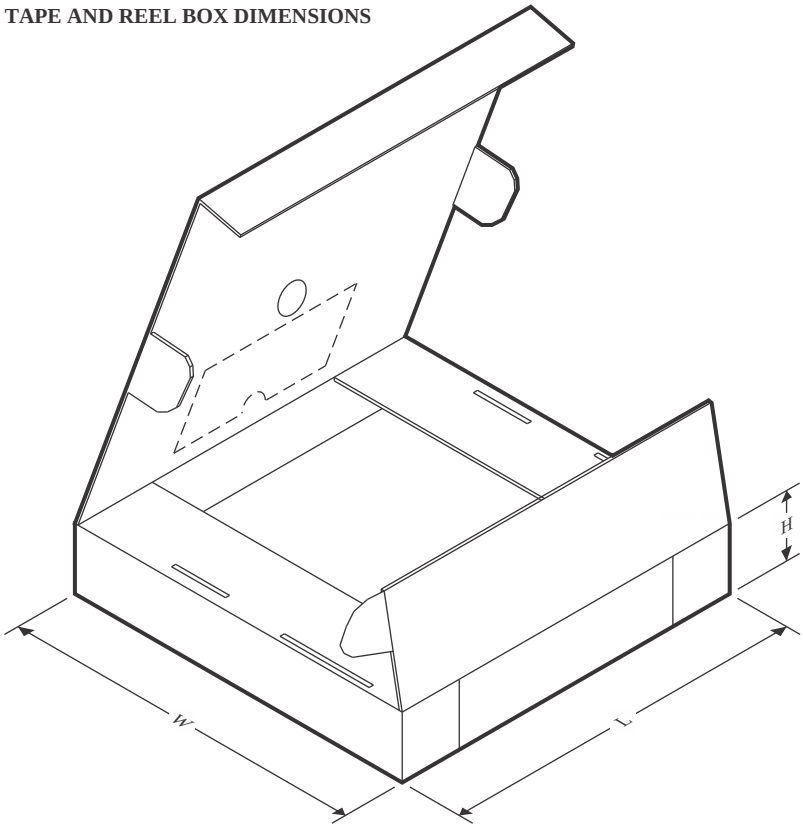
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3988IMF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMF-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988IMFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3988ITL-1.85/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

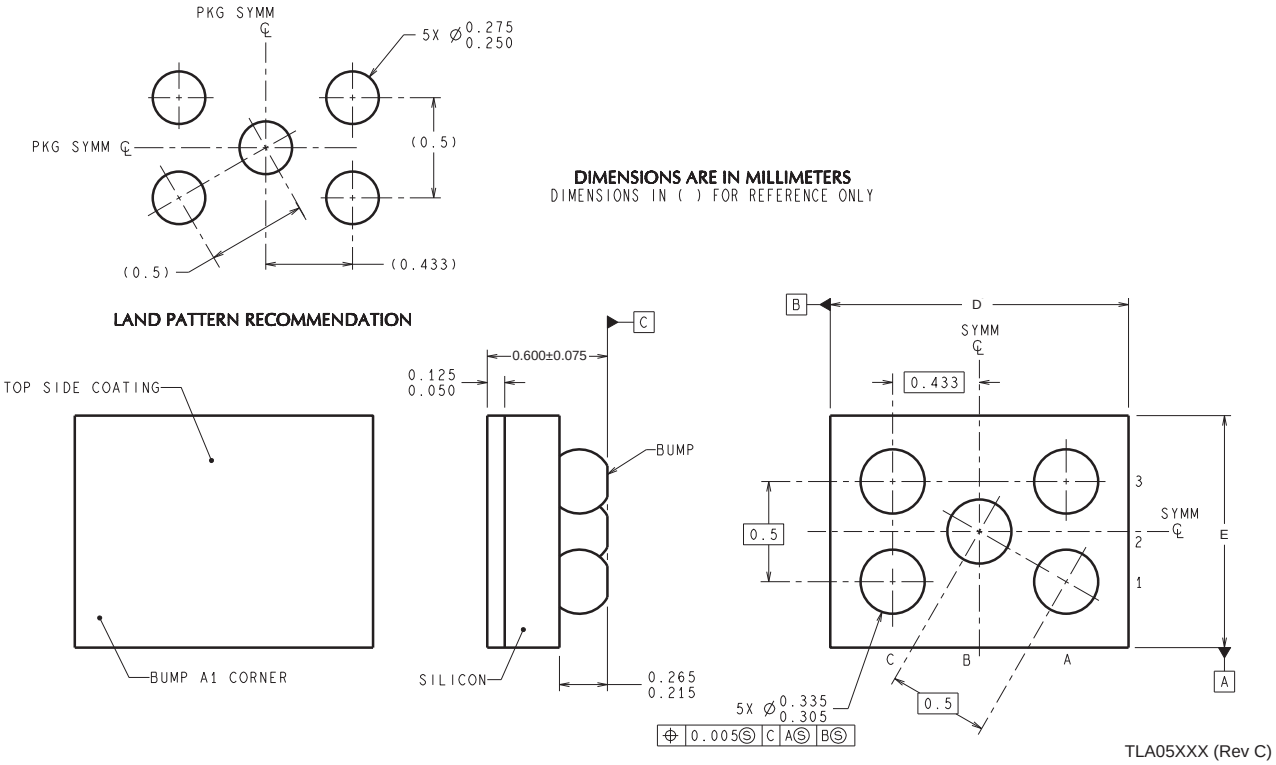
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3988IMF-2.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3988IMF-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3988IMF-3.3/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3988IMFX-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3988IMFX-2.85/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3988IMFX-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3988ITL-1.85/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0

YZR0005



D: Max = 1.502 mm, Min =1.441 mm

E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

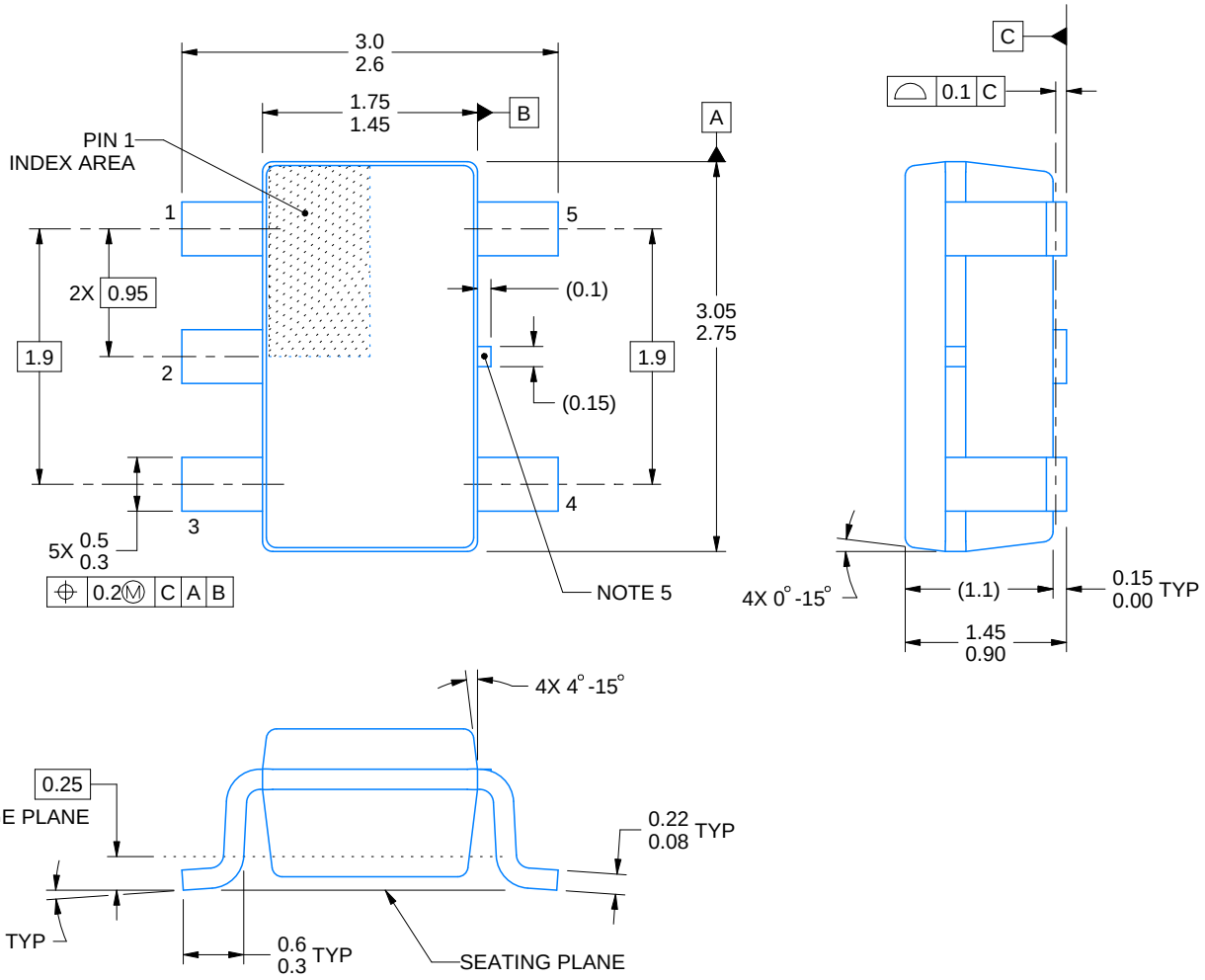
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

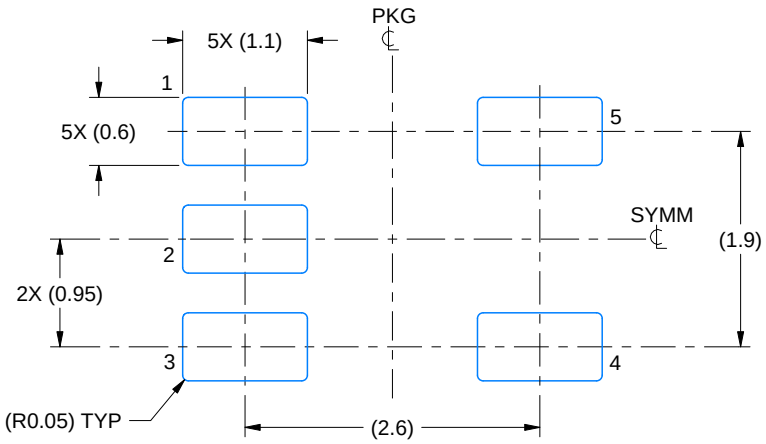
SMALL OUTLINE TRANSISTOR



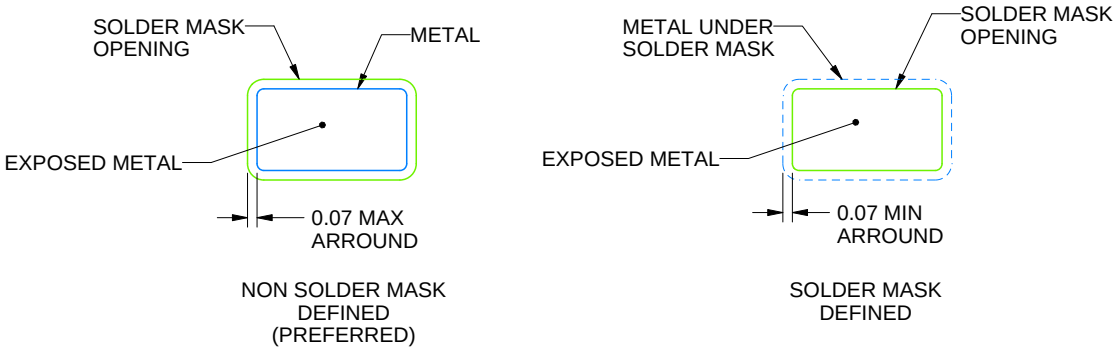
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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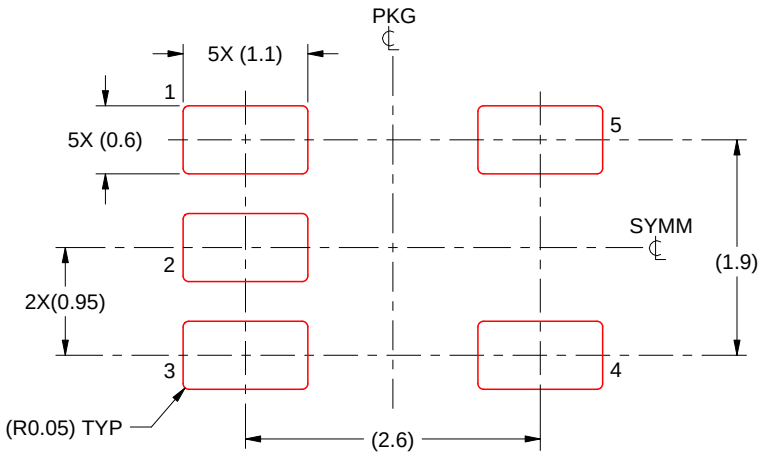
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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