MSP430F5510、MSP430F550x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 低い電源電圧範囲: 3.6Vから最低1.8Vまで
- 超低消費電力
  - アクティブ・モード(AM)
    すべてのシステム・クロックがアクティブ
    - 195µA/MHz (8MHz、3V)、フラッシュ・プログラム実行時（標準値）
    - 115µA/MHz (8MHz、3V)、RAMプログラム実行時（標準値）
  - スタンバイ・モード(LPM3)
    - 水晶振動子を内蔵するリアルタイム・クロック(RTC)、ウォッチドッグ、および電源スーパーバイザが動作、RAMデータ完全保持、高速ウェークアップ：
      1.9µA (2.2V)、2.1µA (3V)（標準値）
    - 低消費電力発振器(VLO)、汎用カウンタ、ウォッチドッグ、および電源スーパーバイザが動作、RAMデータ完全保持、高速ウェークアップ：
      1.4µA (3V)（標準値）
  - オフ・モード(LPM4)
    RAMデータ完全保持、電源スーパーバイザが動作、高速ウェークアップ：
    1.1µA (3V)（標準値）
  - シャットダウン・モード(LPM4.5)
    0.18µA (3V)（標準値）
- スタンバイ・モードから5µs以内にウェークアップ
- 16ビットRISCアーキテクチャ、拡張メモリ、最大25MHzのシステム・クロック
- 柔軟な電力管理システム
  - プログラム可能な、レギュレートされたコア電源電圧を持つ、完全に統合されたLDO
  - 電源電圧の管理、監視、およびブラウンアウト
- 統合クロック・システム
  - FLL制御ループによる周波数安定化
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 低周波数のトリムされた内部基準ソース(REFO)
  - 32kHzの時計用水晶振動子(XT1)
  - 最高32MHzの高周波数水晶振動子(XT2)
- 16 ビット・タイマ TA0：5個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16 ビット・タイマ TA1：3個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16 ビット・タイマ TA2：3個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16ビット・タイマTB0：7個のキャプチャ/コンペア・シャドウ・レジスタを備えたTimer_B
- 2つのユニバーサル・シリアル通信インターフェイス(USCI)
  - USCI_A0、USCI_A1がそれぞれ次の機能をサポート
    - 自動ボーレート検出機能付きの拡張UART
    - IrDAエンコーダおよびデコーダ
    - 同期SPI
  - USCI_B0、USCI_B1がそれぞれ次の機能をサポート
    - I^2C
    - 同期SPI
- フルスピードUSB
  - USB-PHY内蔵
  - 3.3V/1.8V USB電源システム内蔵
  - USB-PLL内蔵
  - 8入力/8出力のエンドポイント
- ウィンドウ・コンパレータ付き10ビット・アナログ/デジタル・コンバータ(ADC)
- コンパレータ
- ハードウェア乗算器で32ビットの演算をサポート
- シリアルのオンボード・プログラミング、外部からのプログラミング電圧は不要
- 3チャネルの内蔵DMA
- RTC機能付き基本タイマ
- デバイスの比較 に、供給中の製品ファミリを掲載

1.2 アプリケーション

- アナログおよびデジタル・センサ・システム
- データ・ロギング
- USBホストへの接続
- ワイヤレス・ヘッドセット

1.3 概要

TI MSPファミリの超低消費電力マイクロコントローラは複数のデバイスで構成され、それぞれが各種のアプリケーションを対象とする異なるペリフェラルを搭載しています。アーキテクチャに多様な低消費電力モードを組み合わせ、携帯型測定機器で長いバッテリ駆動時間を実現するように最適化しています。強力な16ビットRISC CPU、16ビット・レジスタ、および定数ジェネレータが搭載されているため、最高水準のコード効率を実現できます。また、デジタル制御発振器(DCO)により、低消費電力モードからアクティブ・モードへ5µs未満でウェークアップできます。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

MSP430F5510、MSP430F5509、MSP430F5508は、USB 2.0対応のUSB PHY、4つの16ビット・タイマ、高性能10ビットADC、2つのUSCI [(1)]、ハードウェア・マルチプライヤ、DMA、アラーム機能付きRTCモジュール、31または47のI/Oピンを搭載したマイクロコントローラです。

MSP430F5507、MSP430F5506、MSP430F5505、MSP430F5504は、USB 2.0対応のUSB PHY、4つの16ビット・タイマ、高性能10ビットADC、1つのUSCI、ハードウェア乗算器、DMA、アラーム機能付きRTCモジュール、31のI/Oピンを搭載したマイクロコントローラです。

MSP430F5503、MSP430F5502、MSP430F5501、MSP430F5500は、10ビットADCではなくコンパレータを搭載しており、それ以外のペリフェラルについてはMSP430F5507、MSP430F5506、MSP430F5505、MSP430F5504と同様です。

代表的な用途は、さまざまなUSBホストへの接続を要するアナログ/デジタル・センサ・システムやデータ・ロガーなどです。

モジュールの完全な説明については、*『MSP430FR5xxおよびMSP430FR6xxファミリ ユーザー・ガイド』*を参照してください。

(1) 48ピン・パッケージの場合、ピンに割り当てることができるUSCI機能は、ポート・マッピング・コントローラを使用してユーザーがポート4で設定したものに限られます。すべての機能を同時に利用できるとは限りません。

製品情報[(1)]

型番	パッケージ	本体サイズ[(2)]
MSP430F5510IRGC	VQFN (64)	9mm×9mm
MSP430F5510IZQE	BGA (80)	5mm×5mm
MSP430F5510IPT	LQFP (48)	7mm×7mm
MSP430F5510IRGZ	VQFN (48)	7mm×7mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については 8の「*付録:パッケージ・オプション*」またはwww.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、8の「*メカニカル・データ*」を参照してください。

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1.4 機能ブロック図

図 1-1 にRGC/ZQEパッケージ版MSP430F5510、MSP430F5509、MSP430F5508の機能ブロック図を示します。

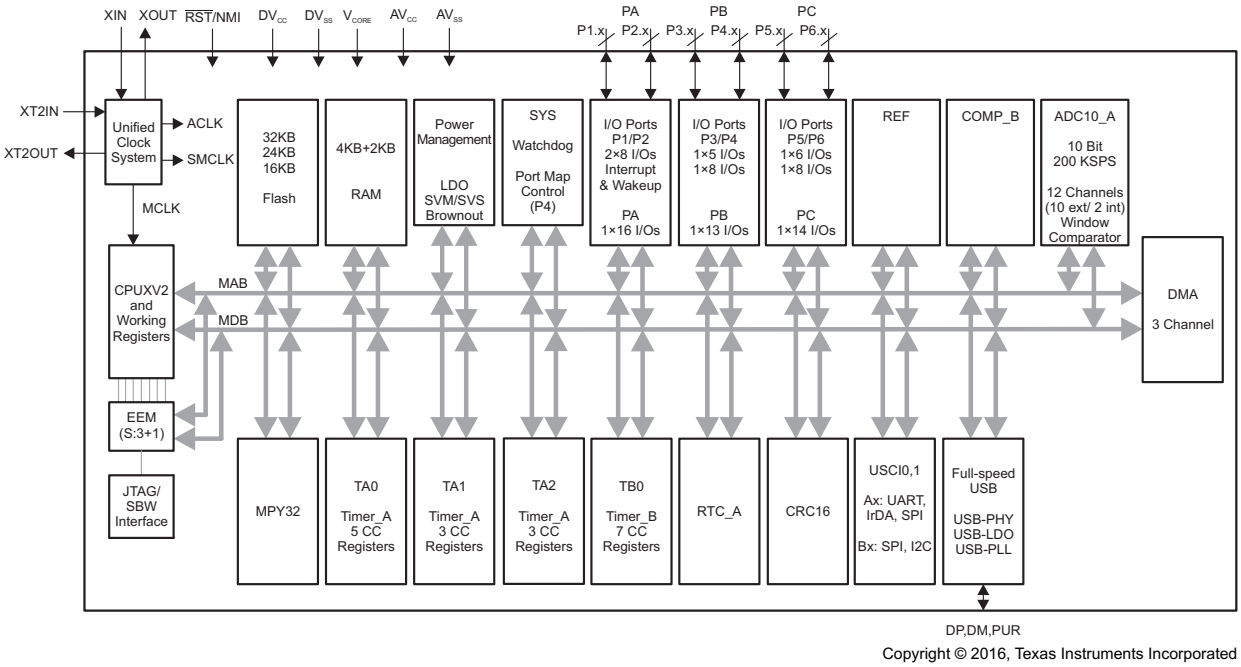
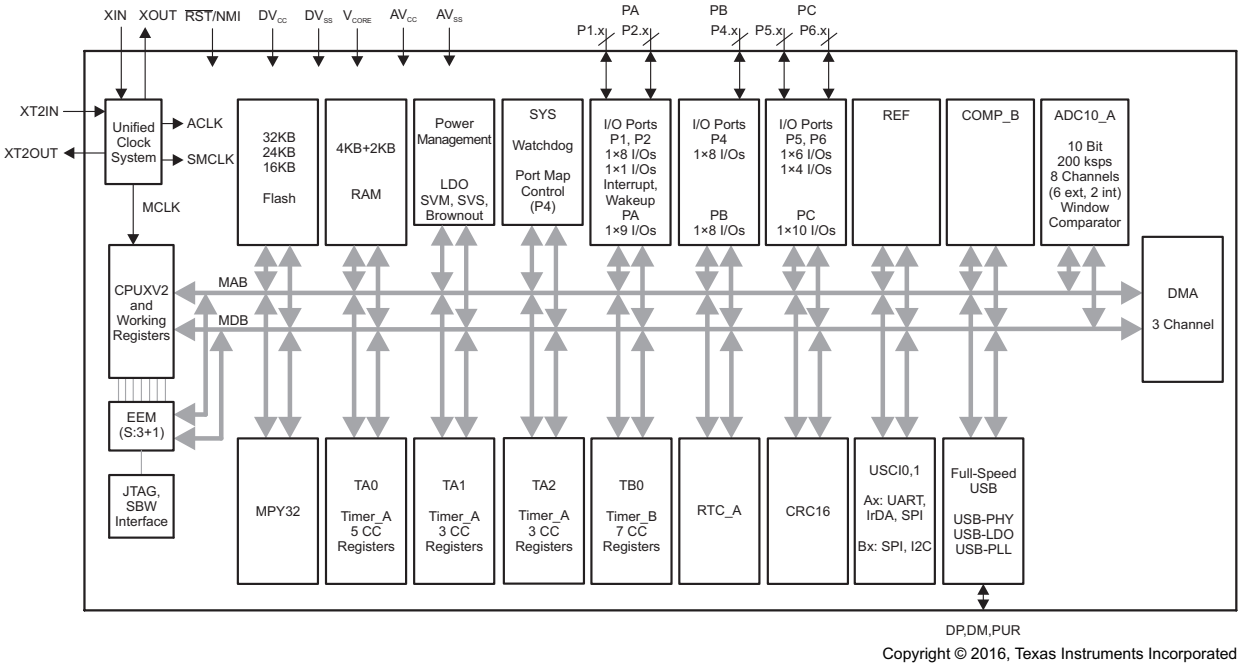


図 1-1. 機能ブロック図 – MSP430F5510IRGC、MSP430F5509IRGC、MSP430F5508IRGC、MSP430F5510IZQE、MSP430F5509IZQE、MSP430F5508IZQE

図 1-2 にRGZ/PTパッケージ版MSP430F5510、MSP430F5509、MSP430F5508の機能ブロック図を示します。



NOTE: USCIモジュール信号の同時利用制限については、Table 3-1を参照してください。

図 1-2. 機能ブロック図 – MSP430F5510IRGZ、MSP430F5509IRGZ、MSP430F5508IRGZ、MSP430F5510IPT、MSP430F5509IPT、MSP430F5508IPT

図 1-3 にRGZパッケージ版MSP430F5507、MSP430F5506、MSP430F5505、およびRGZ/PTパッケージ版MSP430F5504の機能ブロック図を示します。

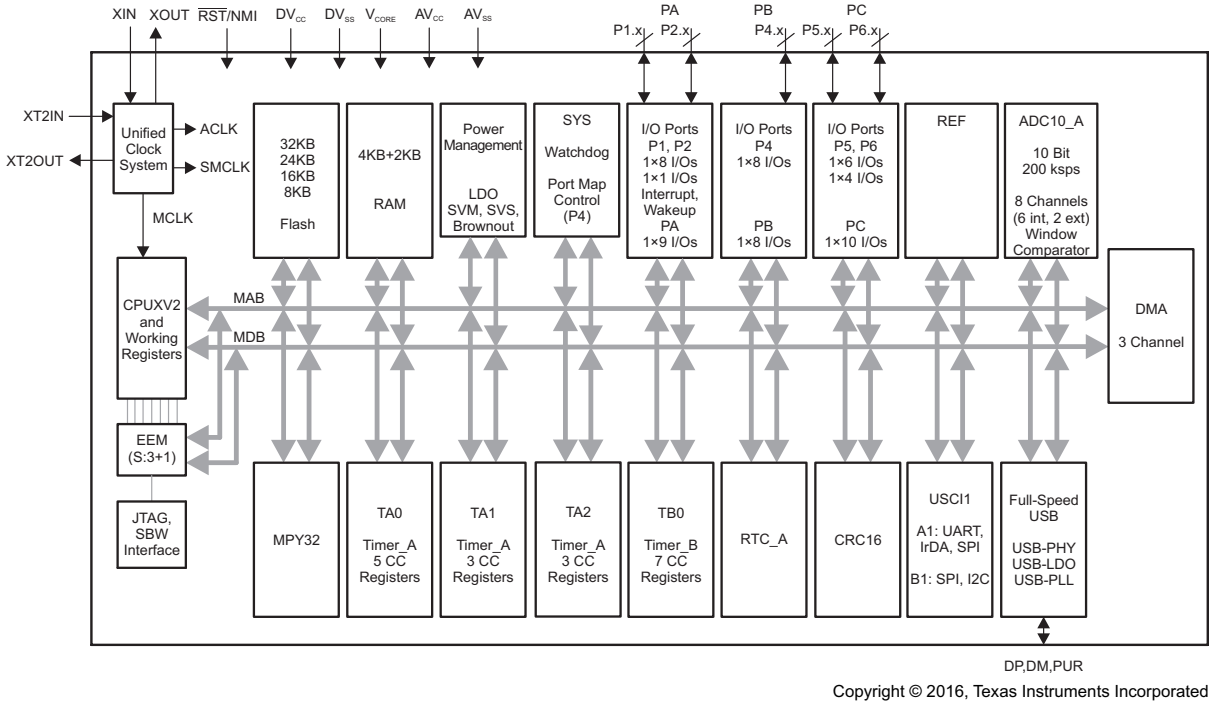


図 1-3. 機能ブロック図 – MSP430F5507IRGZ、MSP430F5506IRGZ、MSP430F5505IRGZ、MSP430F5504IRGZ、MSP430F5504IPT

図 1-4 にRGZパッケージ版MSP430F5503、MSP430F5502、MSP430F5501、MSP430F5500の機能ブロック図を示します。

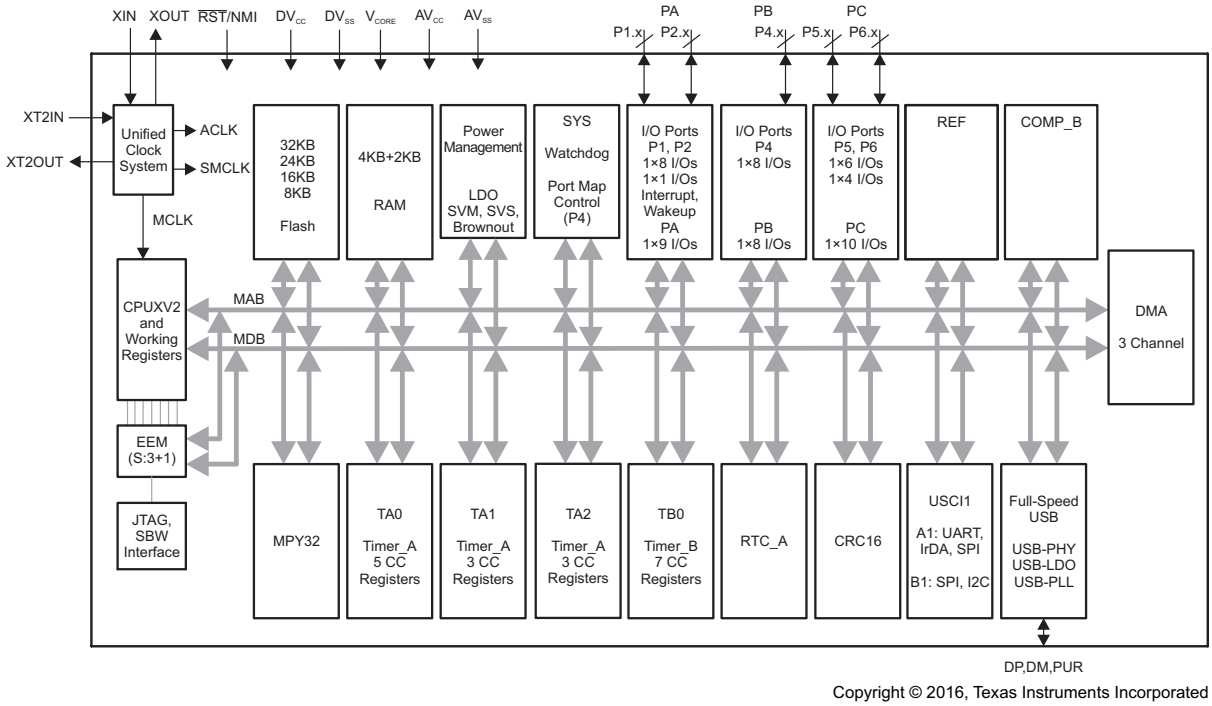


図 1-4. 機能ブロック図 – MSP430F5503IRGZ、MSP430F5502IRGZ、MSP430F5501IRGZ、MSP430F5500IRGZ

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2 改訂履歴

2015年5月1日発行分から2018年09月20日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 8
- Added typical conditions statements at the beginning of Section 5, *Specifications* 19
- Changed the MIN value of the $V_{(DVCC_BOR_hys)}$ parameter from 60 mV to 50 mV in Section 5.20, *PMM, Brownout Reset (BOR)* 32
- Updated notes (1) and (2) and added note (3) in , *Wake-up Times From Low-Power Modes and Reset* 35
- Removed ADC10DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Section 5.36, *10-Bit ADC, Timing Parameters*, because ADC10CLK is after division 41
- Changed the MAX value of the t_{EN_CMP} parameter with Test Conditions of "CBPWRMD = 10" from 1.5 µs to 100 µs in Section 5.40, *Comparator_B* 44
- Updated note (1) on Section 5.47, *JTAG and Spy-Bi-Wire Interface* 48
- Throughout document, changed all instances of "bootstrap loader" to "bootloader" 53
- Corrected spelling of NMIIFG in Table 6-9, *System Module Interrupt Vector Registers* 58
- Corrected register acronyms in Table 6-43, *USB Configuration Registers*, and Table 6-44, *USB Control Registers* . 76
- 従来の「*開発ツールのサポート*」セクションを 7.3、「*ツールとソフトウェア*」に置き換え 102
- 7.4「*ドキュメントのサポート*」を更新 104

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3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	PROGRAM MEMORY (KB)	SRAM (KB)(3)	Timer_A(4)	Timer_B(5)	USCI		ADC10_A (CH)	Comp_B (CH)	I/Os	PACKAGE
					CHANNEL A: UART, LIN, IrDA, SPI	CHANNEL B: SPI, I²C				
MSP430F5510	32	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2(6)	2(6)	6 ext, 2 int	4	31	48 PT, 48 RGZ
MSP430F5509	24	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2(6)	2(6)	6 ext, 2 int	4	31	48 PT, 48 RGZ,
MSP430F5508	16	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
					2(6)	2(6)	6 ext, 2 int	4	31	48 PT, 48 RGZ,
MSP430F5507	32	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	–	31	48 RGZ
MSP430F5506	24	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	–	31	48 RGZ
MSP430F5505	16	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	–	31	48 RGZ
MSP430F5504	8	4 + 2	5, 3, 3	7	1	1	6 ext, 2 int	–	31	48 PT, 48 RGZ
MSP430F5503	32	4 + 2	5, 3, 3	7	1	1	–	4	31	48 RGZ
MSP430F5502	24	4 + 2	5, 3, 3	7	1	1	–	4	31	48 RGZ
MSP430F5501	16	4 + 2	5, 3, 3	7	1	1	–	4	31	48 RGZ
MSP430F5500	8	4 + 2	5, 3, 3	7	1	1	–	4	31	48 RGZ

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in 8, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) The additional 2KB USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.
(4) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(5) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(6) Two USCIs are available; however, pinned out functions are limited to what the user configures on port 4 with the port mapping controller (see Section 6.9.2). It may not be possible to bring out all functions simultaneously.

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Companion Products for MSP430F5510 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430F5510 TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

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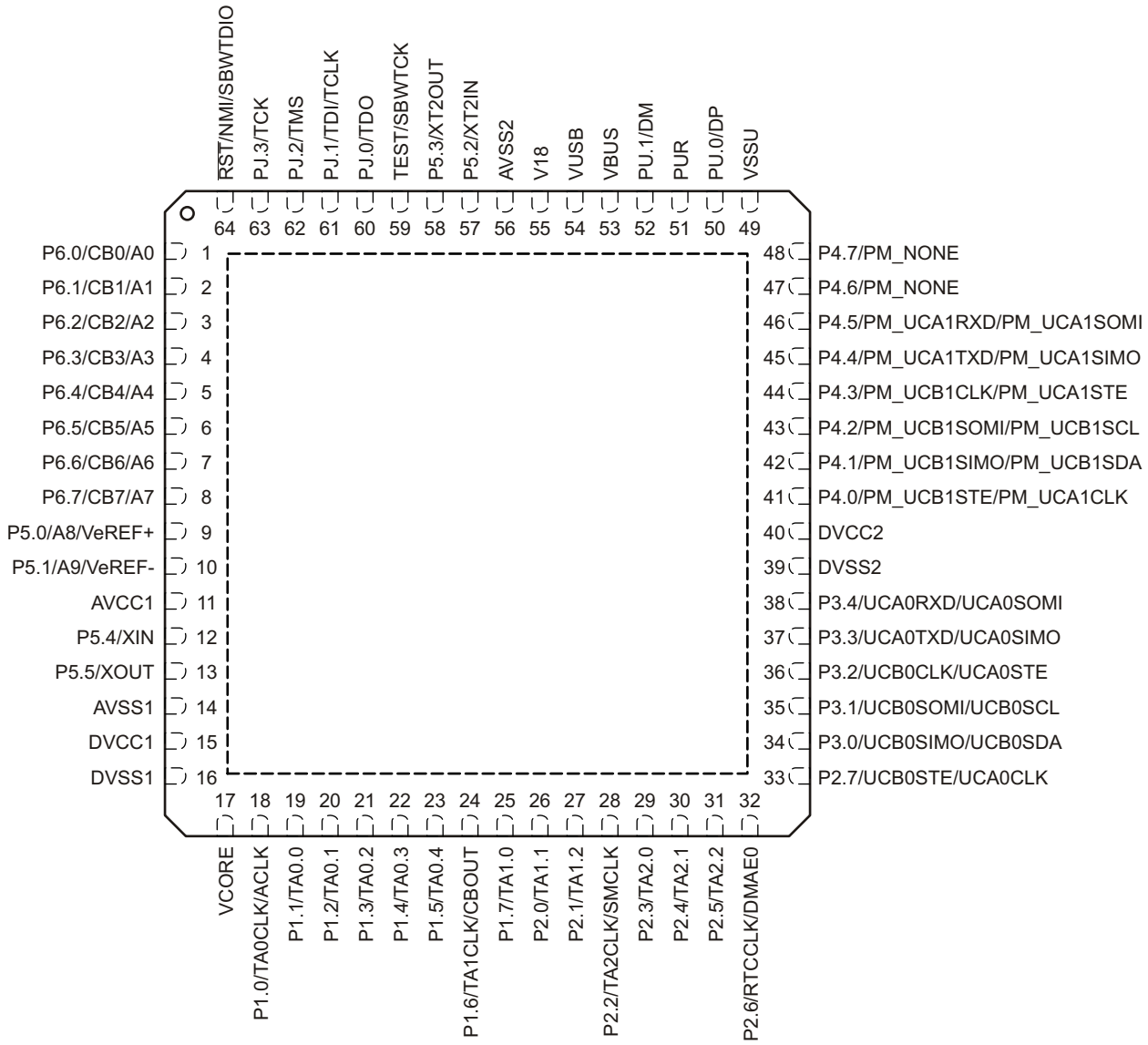
4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 64-pin RGC package of the MSP430F5510, MSP430F5509, and MSP430F5508 MCUs.



NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Figure 4-1. 64-Pin RGC Package (Top View) – F5510, F5509, F5508

Figure 4-2 shows the pinout for the 80-pin ZQE package of the MSP430F5510, MSP430F5509, and MSP430F5508 MCUs. See Section 4.2 for the pin assignments.

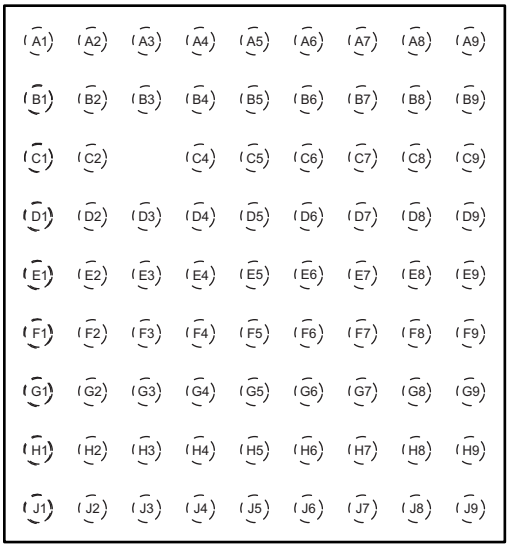


Figure 4-2. 80-Pin ZQE Package (Top View) – F5510, F5509, F5508

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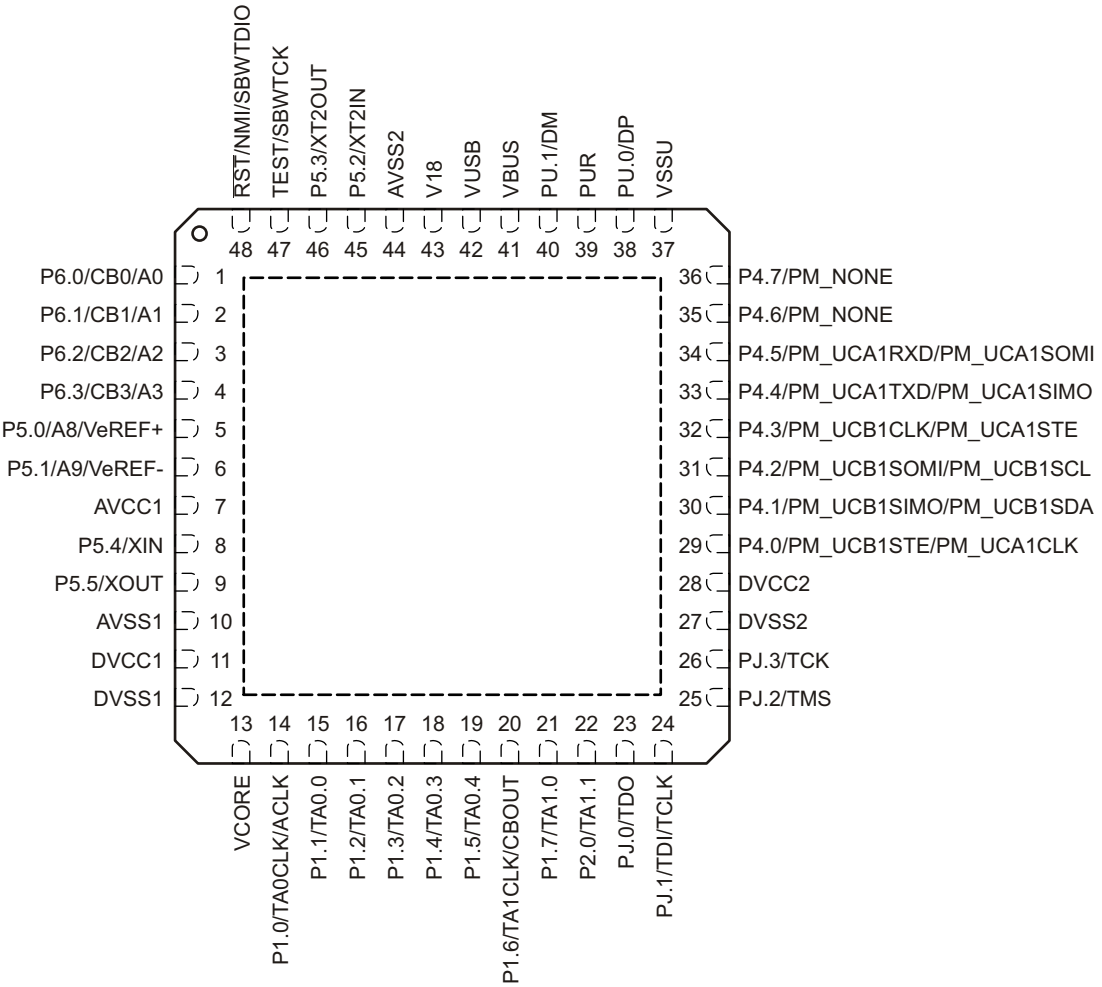
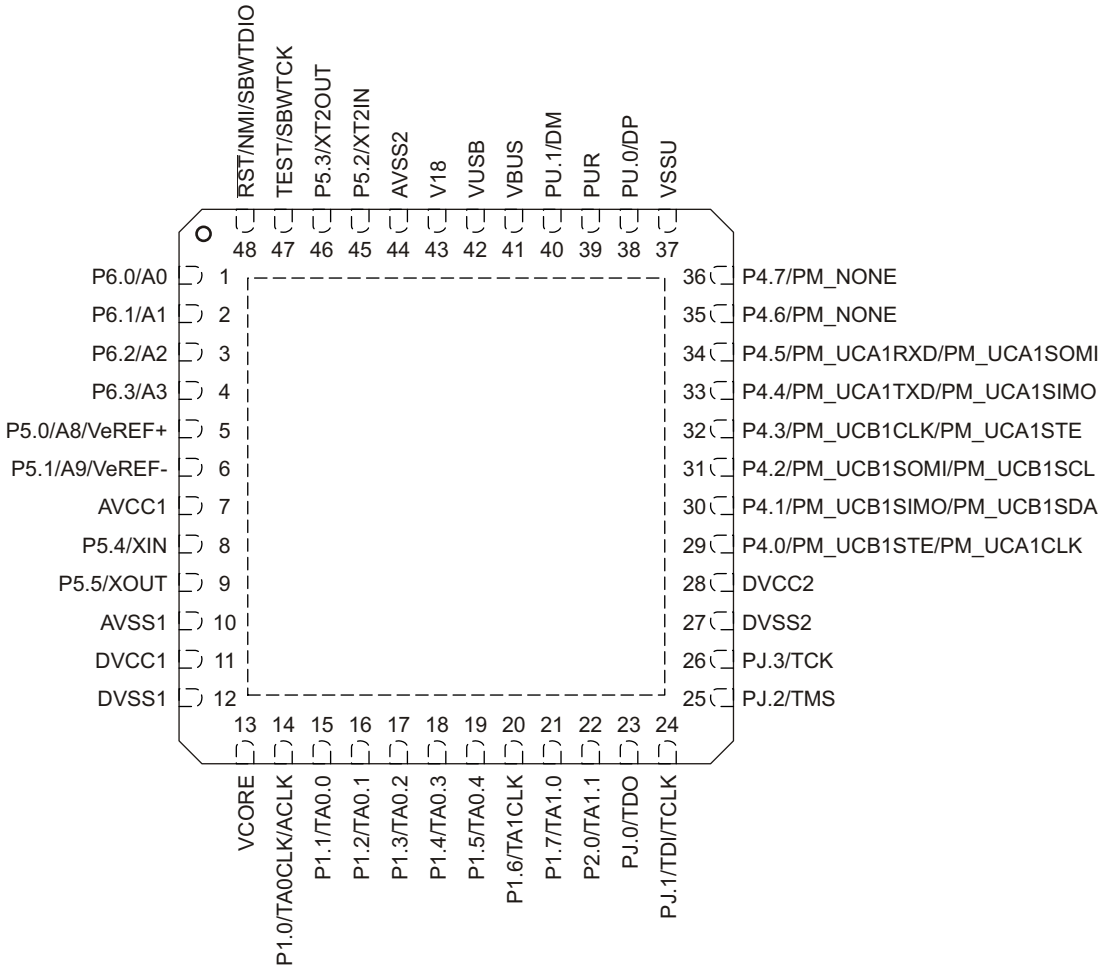
Figure 4-3 shows the pinout for 48-pin RGZ and PT packages of the MSP430F5510, MSP430F5509, and MSP430F5508 MCUs.



NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Figure 4-3. 48-Pin RGZ or PT Package (Top View) – F5510, F5509, F5508

Figure 4-4 shows the pinout for the 48-pin RGZ and PT packages of the MSP430F5507, MSP430F5506, MSP430F5505, and MSP430F5504 MCUs.



NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Figure 4-4. 48-Pin RGZ or PT Package (Top View) – F5507, F5506, F5505, F5504

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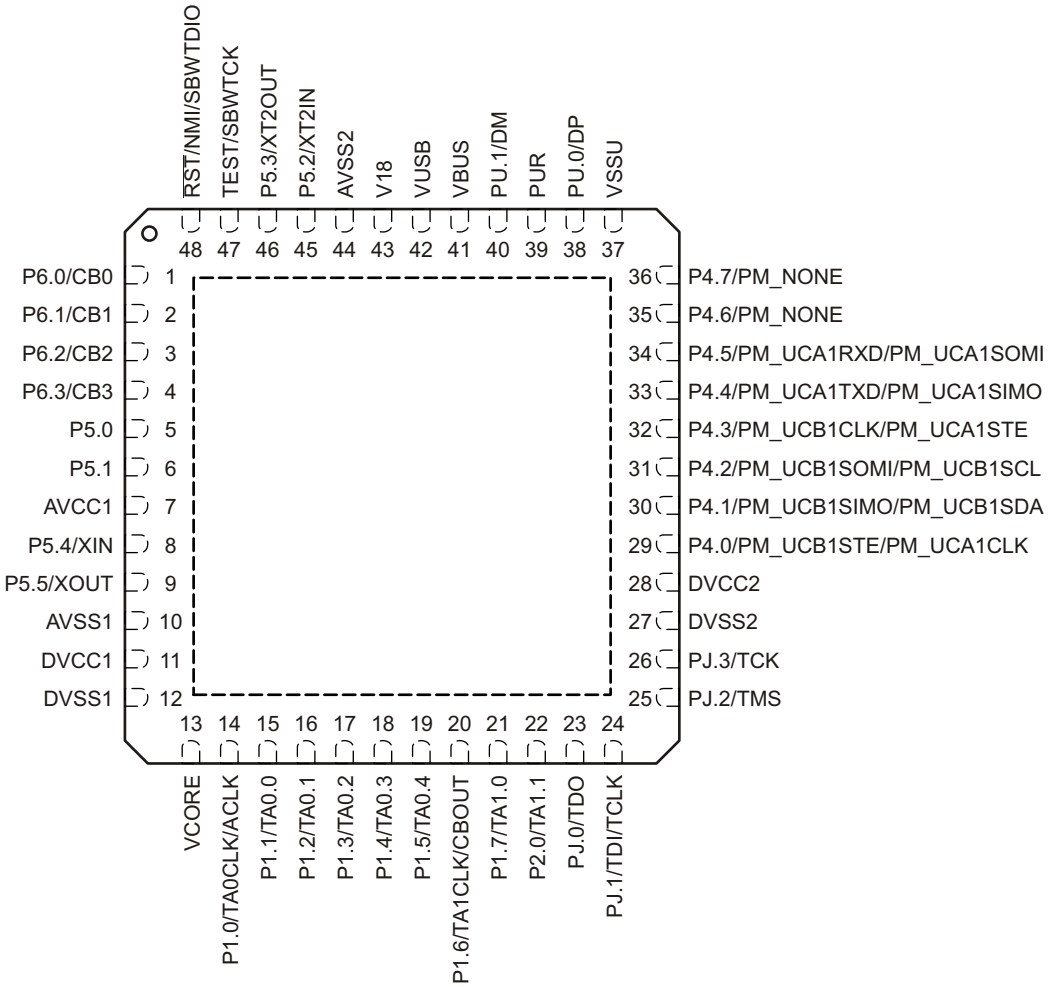
Figure 4-5 shows the pinout for the 48-pin RGZ package of the MSP430F5503, MSP430F5502, MSP430F5501, and MSP430F5500 MCUs.



NOTE: TI recommends connection of the exposed thermal pad to V_{SS}.

Figure 4-5. 48-Pin RGZ Package (Top View) – F5503, F5502, F5501, F5500

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Terminal Functions

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P6.4/CB4/A4	5	N/A	C1	I/O	General-purpose digital I/O Comparator_B input CB4 (not available on PT and RGZ package devices) Analog input A4 – ADC (not available on PT and RGZ package devices)
P6.5/CB5/A5	6	N/A	D2	I/O	General-purpose digital I/O Comparator_B input CB5 (not available on PT and RGZ package devices) Analog input A5 – ADC (not available on PT and RGZ package devices)
P6.6/CB6/A6	7	N/A	D1	I/O	General-purpose digital I/O Comparator_B input CB6 (not available on PT and RGZ package devices) Analog input A6 – ADC (not available on PT and RGZ package devices)
P6.7/CB7/A7	8	N/A	D3	I/O	General-purpose digital I/O Comparator_B input CB7 (not available on PT and RGZ package devices) Analog input A7 – ADC (not available on PT and RGZ package devices)
P5.0/A8/VeREF+	9	5	E1	I/O	General-purpose digital I/O Analog input A8 – ADC (not available on F5503, F5502, F5501, F5500 devices) Input for an external reference voltage to the ADC (not available on F5503, F5502, F5501, F5500 devices)
P5.1/A9/VeREF-	10	6	E2	I/O	General-purpose digital I/O Analog input A9 – ADC (not available on F5503, F5502, F5501, F5500 devices) Negative terminal for an externally provided ADC reference (not available on F5503, F5502, F5501, F5500 devices)
AVCC1	11	7	F2		Analog power supply
P5.4/XIN	12	8	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	9	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	14	10	G2		Analog ground supply
DVCC1	15	11	H1		Digital power supply
DVSS1	16	12	J1		Digital ground supply
VCORE[2]	17	13	J2		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	18	14	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	19	15	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	20	16	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input

(1) I = input, O = output, N/A = not available
(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE} (see Section 5.3).

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Table 4-1. Terminal Functions (continued)

TERMINAL				I/O(1)	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P1.3/TA0.2	21	17	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	22	18	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	23	19	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	24	20	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	25	21	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.0/TA1.1	26	22	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	27	N/A	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	28	N/A	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input SMCLK output
P2.3/TA2.0	29	N/A	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	30	N/A	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output
P2.5/TA2.2	31	N/A	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	32	N/A	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK	33	N/A	H7	I/O	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	34	N/A	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I^2C data – USCI_B0 I^2C mode
P3.1/UCB0SOMI/UCB0SCL	35	N/A	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I^2C clock – USCI_B0 I^2C mode
P3.2/UCB0CLK/UCA0STE	36	N/A	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	37	N/A	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode

Table 4-1. Terminal Functions (continued)

TERMINAL				I/O(1)	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
P3.4/UCA0RXD/UCA0SOMI	38	N/A	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P4.0/PM_UCB1STE/ PM_UCA1CLK	41	29	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	42	30	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I^2C data – USCI_B1 I^2C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	43	31	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I^2C clock – USCI_B1 I^2C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE	44	32	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	39	27	F9		Digital ground supply
DVCC2	40	28	E9		Digital power supply
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	45	33	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	46	34	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	47	35	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function
P4.7/PM_NONE	48	36	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function
VSSU	49	37	B8, B9		USB PHY ground supply
PU.0/DP	50	38	A9	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DP
PUR	51	39	B7	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See Section 6.5.1 for more information.
PU.1/DM	52	40	A8	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DM
VBUS	53	41	A7		USB LDO input (connect to USB power source)
VUSB	54	42	A6		USB LDO output

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Table 4-1. Terminal Functions (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	RGC	RGZ, PT	ZQE		
V18	55	43	B6		USB regulated power (internal use only, no external current loading)
AVSS2	56	44	A5		Analog ground supply
P5.2/XT2IN	57	45	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	58	46	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK	59	47	A4	I	Test mode pin – select digital I/O on JTAG pins Spy-By-Wire input clock
PJ.0/TDO	60	23	C5	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	61	24	C4	I/O	General-purpose digital I/O Test data input Test clock input
PJ.2/TMS	62	25	A3	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	63	26	B3	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO	64	48	A2	I/O	Reset input, active low[3] Nonmaskable interrupt input Spy-By-Wire data input/output
P6.0/CB0/A0	1	1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 (not available on F5507, F5506, F5505, F5504 devices) Analog input A0 – ADC (not available on F5503, F5502, F5501, F5500 devices)
P6.1/CB1/A1	2	2	B2	I/O	General-purpose digital I/O Comparator_B input CB1 (not available on F5507, F5506, F5505, F5504 devices) Analog input A1 – ADC (not available on F5503, F5502, F5501, F5500 devices)
P6.2/CB2/A2	3	3	B1	I/O	General-purpose digital I/O Comparator_B input CB2 (not available on F5507, F5506, F5505, F5504 devices) Analog input A2 – ADC (not available on F5503, F5502, F5501, F5500 devices)
P6.3/CB3/A3	4	4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 (not available on F5507, F5506, F5505, F5504 devices) Analog input A3 – ADC (not available on F5503, F5502, F5501, F5500 devices)
Reserved	N/A	N/A	[4]		Reserved. Connect to ground.
QFN Pad	Pad	Pad	N/A		Exposed QFN package pad (not available on PT package devices). TI recommends connecting to V_{SS}.

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.
(4) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

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5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

5.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE, VBUS, V18)[2]	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		95	°C
Storage temperature, T_{stg}[3]	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming(AV_{CC} = DV_{CC})[1][2]	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
$V_{CC,USB}$	Supply voltage during USB operation, USB PLL disabled, USB_EN = 1, UPLLEN = 0	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
	Supply voltage during USB operation, USB PLL enabled[3], USB_EN = 1, UPLLEN = 1	PMMCOREVx = 2	2.2		3.6	
		PMMCOREVx = 2, 3	2.4		3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS1} = DV_{SS2} = DV_{SS})			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
C_{VCORE}	Capacitor at VCORE[4]			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.22 threshold parameters for the exact values and further details.
(3) USB operation with USB PLL enabled requires PMMCOREVx ≥ 2 for proper operation.
(4) A capacitor tolerance of ±20% or better is required.

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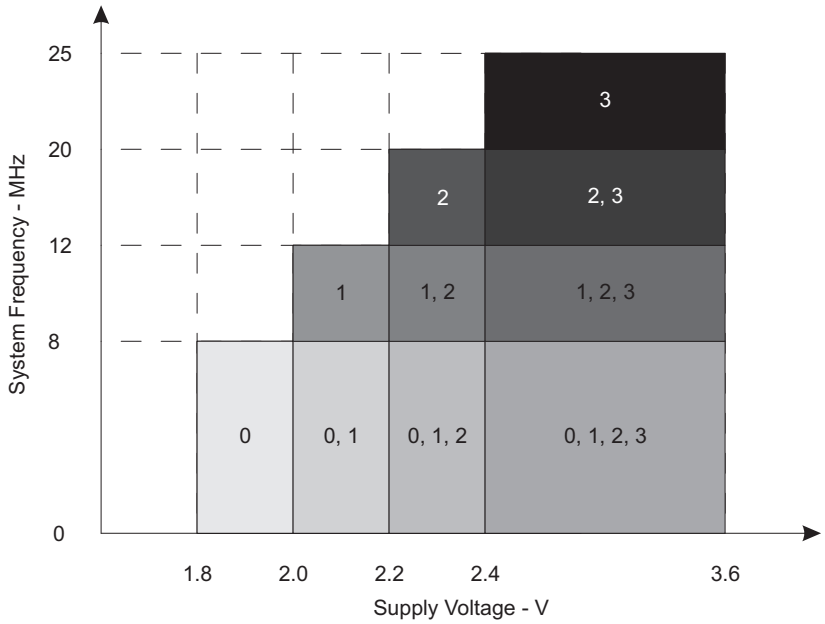
Recommended Operating Conditions *(continued)*

			MIN	NOM	MAX	UNIT
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(5) (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12.0	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20.0	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25.0	
f_{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5			MHz
USB_wait	Wait state cycles during USB operation			16		cycles

(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

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5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ Flash}$	Flash	3 V	0	0.25	0.27	1.55	1.68							mA
			1	0.28		1.74		2.58	2.78					
			2	0.30		1.91		2.84		4.68	5.06			
			3	0.32		2.09		3.10		5.13		6.0	6.5	
$I_{AM,\ RAM}$	RAM	3 V	0	0.17	0.19	0.91	1.00							mA
			1	0.19		1.03		1.54	1.67					
			2	0.20		1.16		1.73		2.84	3.11			
			3	0.21		1.24		1.87		3.1		3.9	4.3	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing. USB disabled (VUSBEN = 0, SLDOEN = 0).
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	TEMPERATURE (T_A)								UNIT
				–40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3)(4)	2.2 V	0	73		77	85	80		85	97	µA
		3 V	3	79		83	92	88		95	105	
I_{LPM2}	Low-power mode 2(5)(4)	2.2 V	0	6.5		6.5	8	7.5		8	11	µA
		3 V	3	7.0		7.0	9	7.9		8.9	13	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	2.2 V	0	1.60		1.90		2.6		3.4		µA
			1	1.65		2.00		2.7		3.6		
			2	1.75		2.15		2.9		3.8		
		3 V	0	1.8		2.1	2.6	2.8		3.6	6.0	
			1	1.9		2.3		2.9		3.8		
			2	2.0		2.4		3.0		4.0		
			3	2.0		2.5	3.0	3.1		4.0	6.5	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7)(4)	3 V	0	1.1		1.3	1.8	1.9		2.7	5.0	µA
			1	1.1		1.4		2.0		2.8		
			2	1.2		1.5		2.1		2.9		
			3	1.3		1.5	2.0	2.2		3.0	5.5	
I_{LPM4}	Low-power mode 4(8)(4)	3 V	0	0.9		1.1	1.5	1.8		2.5	4.8	µA
			1	1.1		1.2		2.0		2.6		
			2	1.2		1.2		2.1		2.7		
			3	1.3		1.3	1.6	2.2		2.8	5.0	
$I_{LPM4.5}$	Low-power mode 4.5(9)	3 V		0.15		0.18	0.35	0.26		0.45	0.80	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz USB disabled (VUSBEN = 0, SLDOEN = 0).
(4) Current for brownout, high-side supervisor (SVS_H) normal mode included. Low-side supervisor (SVS_L) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled. USB disabled (VUSBEN = 0, SLDOEN = 0)
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)
(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz USB disabled (VUSBEN = 0, SLDOEN = 0)
(9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

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5.6 Thermal Resistance Characteristics

			VALUE[(1)]	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air[(2)]	VQFN (RGC)	30	°C/W
		VQFN (RGZ)	28.6	
		LQFP (PT)	62.8	
		BGA (ZQE)	55.5	
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[(3)]	VQFN (RGC)	15.6	°C/W
		VQFN (RGZ)	14.4	
		LQFP (PT)	18.2	
		BGA (ZQE)	21.2	
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[(4)]	VQFN(RGC)	1.6	°C/W
		VQFN (RGZ)	1.6	
		LQFP (PT)	N/A	
		BGA (ZQE)	N/A	
θ_{JB}	Junction-to-board thermal resistance[(5)]	VQFN (RGC)	8.9	°C/W
		VQFN (RGZ)	5.5	
		LQFP (PT)	28.3	
		BGA (ZQE)	19.3	

(1) N/A = not applicable
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

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5.7 Schmitt-Trigger Inputs – General-Purpose I/O (1) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		1.8 V	0.3		0.85	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor (2)	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).
(2) Also applies to the $\overline{RST}$ pin when its pullup or pullup resistor is enabled.

5.8 Inputs – Ports P1 and P2 (1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing (2)	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)} = –3$ mA (1)	1.8 V	$V_{CC} – 0.25$	V_{CC}	V
		$I_{(OHmax)} = –10$ mA (2)		$V_{CC} – 0.60$	V_{CC}	
		$I_{(OHmax)} = –5$ mA (1)	3 V	$V_{CC} – 0.25$	V_{CC}	
		$I_{(OHmax)} = –15$ mA (2)		$V_{CC} – 0.60$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)} = 3$ mA (1)	1.8 V	V_{SS}	$V_{SS} + 0.25$	V
		$I_{(OLmax)} = 10$ mA (2)		V_{SS}	$V_{SS} + 0.60$	
		$I_{(OLmax)} = 5$ mA (1)	3 V	V_{SS}	$V_{SS} + 0.25$	
		$I_{(OLmax)} = 15$ mA (2)		V_{SS}	$V_{SS} + 0.60$	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

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5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA[2]	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA[3]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA[2]	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA[3]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA[2]	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA[3]		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA[2]	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA[3]		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)		[1][2] V_{CC} = 1.8 V PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	ACLK SMCLK MCLK C_L = 20 pF[2]	V_{CC} = 1.8 V PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

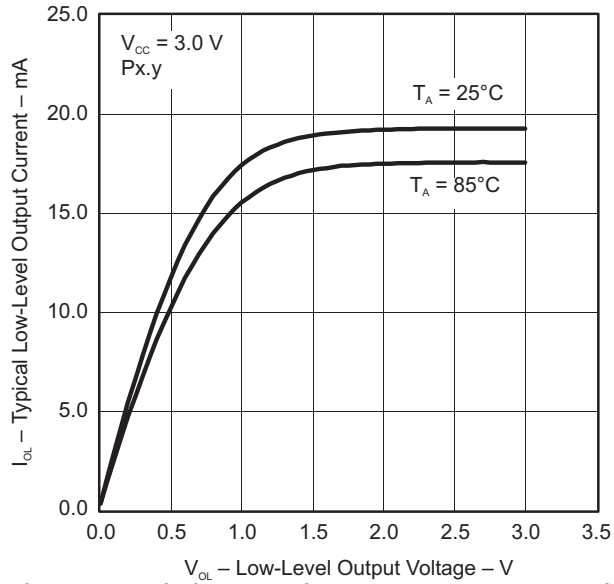

Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

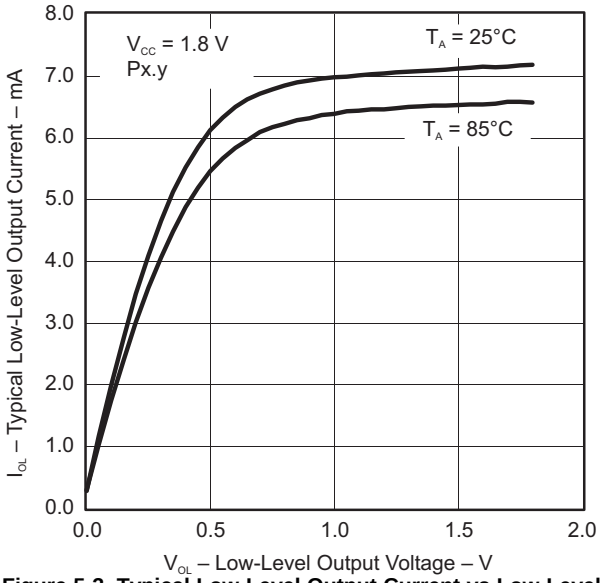

Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

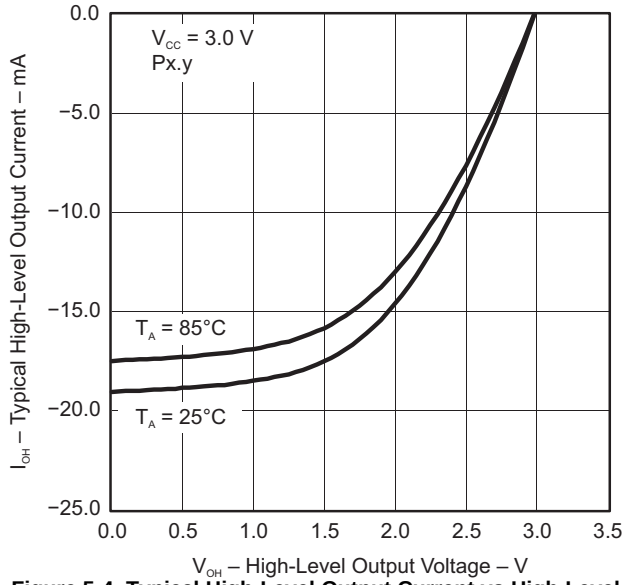

Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

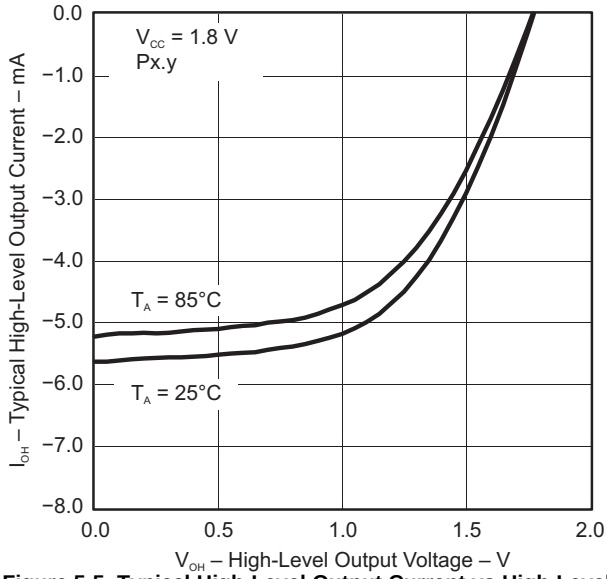

Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

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5.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

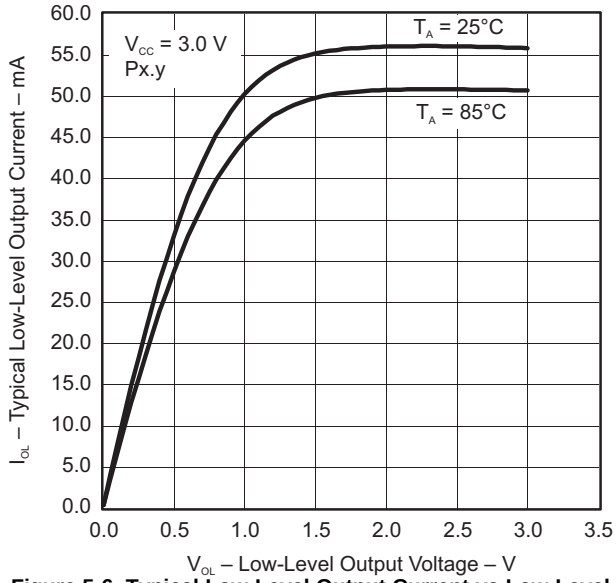

Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

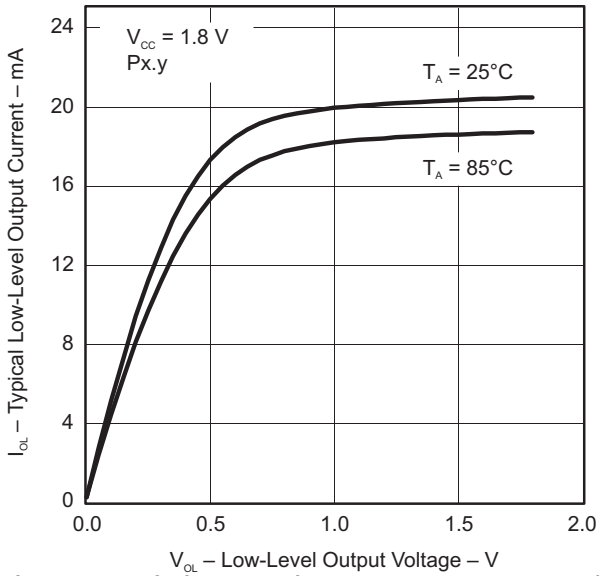

Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

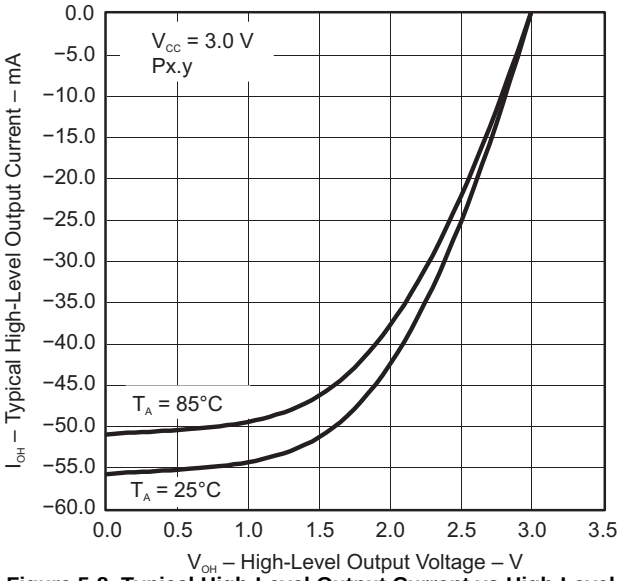

Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

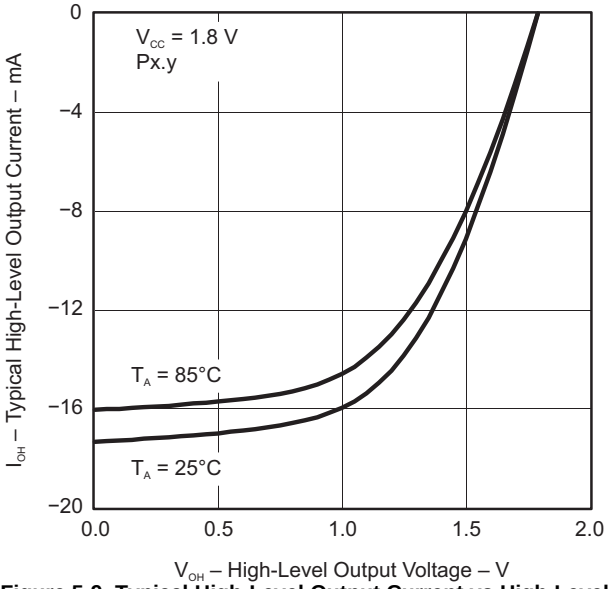

Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

5.15 Crystal Oscillator, XT1, Low-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1[2] [3]		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals[4]	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode[5]	XTS = 0, XCAPx = 0[6]			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode[7]	XTS = 0[8]		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF
- For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le$ 9 pF
- For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le$ 10 pF
- For XT1DRIVEx = 3, $C_{L,eff} \ge 6$ pF

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

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5.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1(4) (3)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Start-up time	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

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5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

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5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT	DCO frequency temperature drift(2)	f_{DCO} = 1 MHz,		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift(3)	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \le f_{DCO} \le f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Figure 5-10. Typical DCO Frequency

5.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC_BOR_IT-)}$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s			1.45	V
$V_{(DVCC_BOR_IT+)}$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.80	1.30	1.50	V
$V_{(DVCC_BOR_hys)}$	BOR_H hysteresis		50		250	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

5.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		V

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5.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
		SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
		SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVSHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVSHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt	DVCC rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and use.

5.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on or off voltage level(1)	SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and use.

5.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0 → 1, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, SVSLFP = 0		100		

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5.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, SVMLFP = 0		100		

5.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	f_{MCLK} ≥ 4.0 MHz			5	µs
			f_{MCLK} < 4.0 MHz			6	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(2)(3)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM4.5 to active mode(4)				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode(4)				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-FAST}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-SLOW}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
(4) This value represents the time from the wake-up event to the reset vector execution.

5.27 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture.	1.8 V, 3 V	20		ns

5.28 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20		ns

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5.29 USCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

5.30 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
t_τ	UART receive deglitch time(1)	2.2 V	50	600	ns
		3 V	50	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.31 USCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz

5.32 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see Figure 5-11 and Figure 5-12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55		ns
			3 V	38		
		PMMCOREV = 3	2.4 V	30		
			3 V	25		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0		ns
			3 V	0		
		PMMCOREV = 3	2.4 V	0		
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		20	ns
			3 V		18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		16	
			3 V		15	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	–10		ns
			3 V	–8		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	–10		
			3 V	–8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-11 and Figure 5-12.

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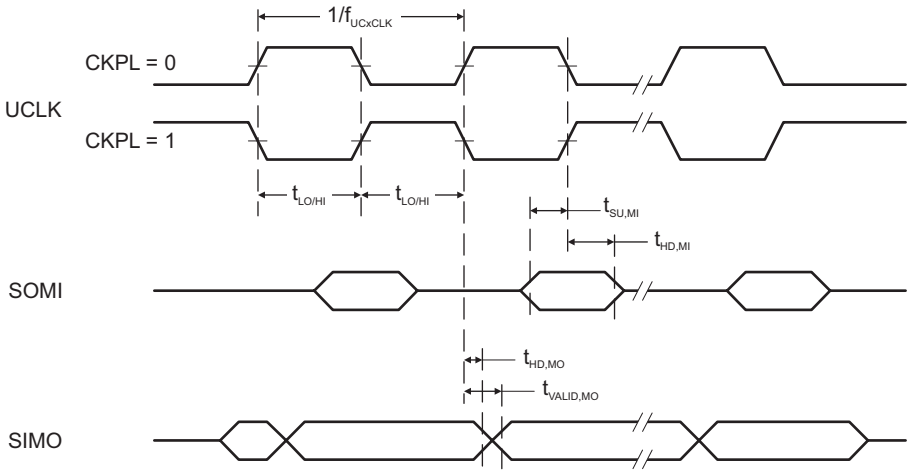

Figure 5-11. SPI Master Mode, CKPH = 0

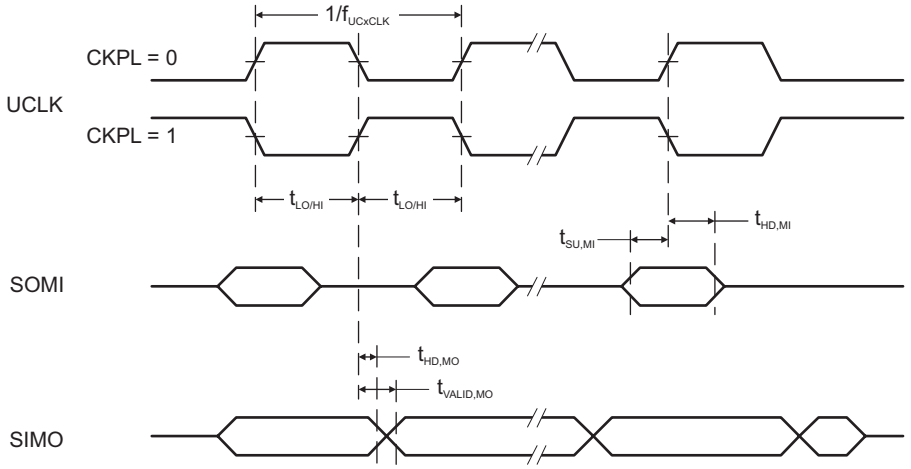

Figure 5-12. SPI Master Mode, CKPH = 1

5.33 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]
(see Figure 5-13 and Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11		ns
			3 V	8		
		PMMCOREV = 3	2.4 V	7		
			3 V	6		
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3		ns
			3 V	3		
		PMMCOREV = 3	2.4 V	3		
			3 V	3		
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V		66	ns
			3 V		50	
		PMMCOREV = 3	2.4 V		36	
			3 V		30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V		30	ns
			3 V		23	
		PMMCOREV = 3	2.4 V		16	
			3 V		13	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	2		
			3 V	2		
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	5		
			3 V	5		
$t_{VALID,SO}$	SOMI output data valid time[2]	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		76	ns
			3 V		60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		44	
			3 V		40	
$t_{HD,SO}$	SOMI output data hold time[3]	C_L = 20 pF, PMMCOREV = 0	1.8 V	18		ns
			3 V	12		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	10		
			3 V	8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.

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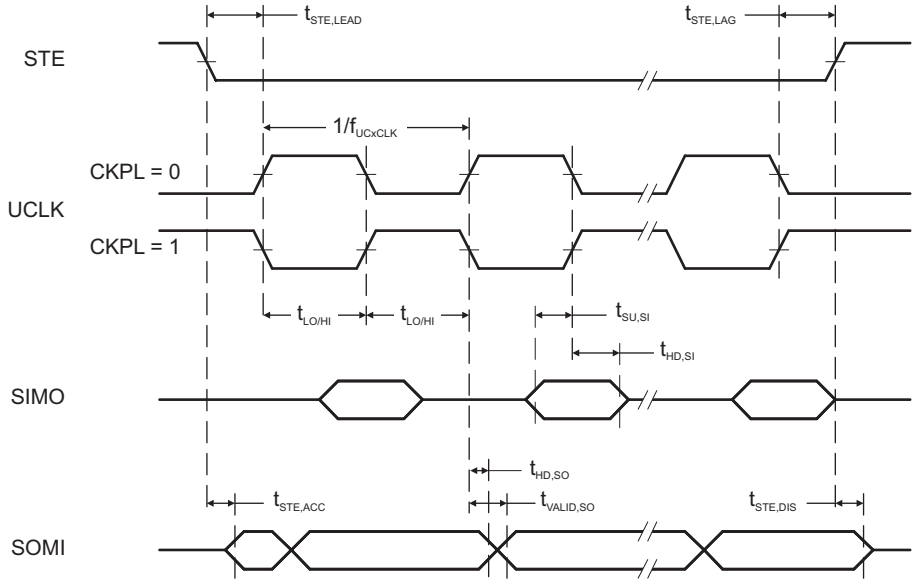

Figure 5-13. SPI Slave Mode, CKPH = 0

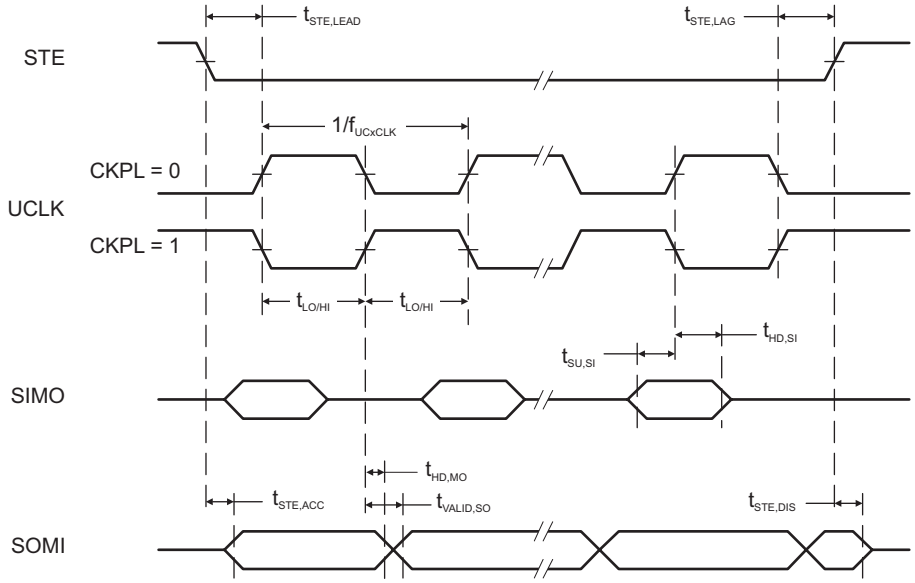

Figure 5-14. SPI Slave Mode, CKPH = 1

5.34 USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7		µs
		f_{SCL} > 100 kHz		0.6		
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0		ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250		ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
			3 V	50	600	

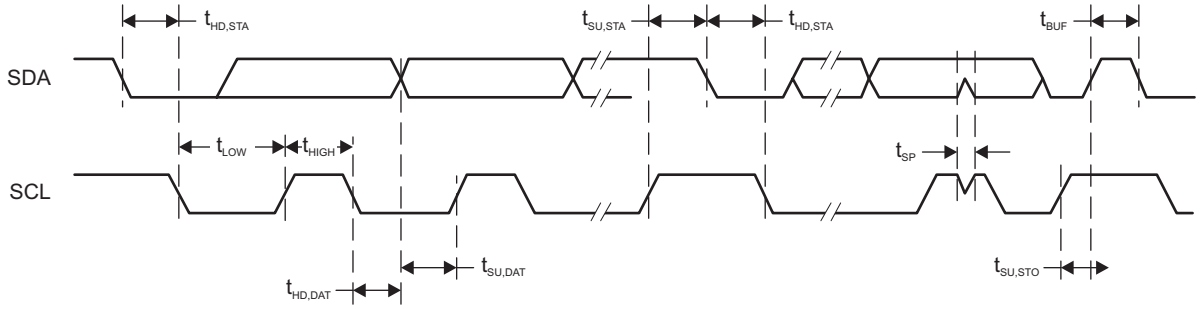

Figure 5-15. I^2C Mode Timing

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5.35 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		1.8		3.6	V
$V_{(Ax)}$	Analog input voltage range[2]	All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals		0		AV_{CC}	V
I_{ADC10_A}	Operating supply current into AVCC terminal, REF module and reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		60	100	µA
			3 V		75	110	
	Operating supply current into AVCC terminal, REF module on, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		113	150	
	Operating supply current into AVCC terminal, REF module off, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		105	140	
	Operating supply current into AVCC terminal, REF module off, reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		70	110	
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad.	2.2 V		3.5		pF
R_I	Input MUX ON resistance	AV_{CC} > 2.0 V, 0 V ≤ V_{Ax} ≤ AV_{CC}				36	kΩ
		1.8V < AV_{CC} < 2.0 V, 0 V ≤ V_{Ax} ≤ AV_{CC}				96	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 µF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

5.36 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
$f_{ADC10OSC}$	Internal ADC10_A oscillator[1]	ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0			12 × 1 / $f_{ADC10CLK}$		
$t_{ADC10ON}$	Turn-on settling time of the ADC	See [2]				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 96 kΩ, C_I = 3.5 pF[3]	1.8 V	3			µs
		R_S = 1000 Ω, R_I = 36 kΩ, C_I = 3.5 pF[3]	3 V	1			

(1) The ADC10OSC is sourced directly from MODOSC in the UCS.
(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately 8 Tau (τ) are required for an error of less than ±0.5 LSB

5.37 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4\ V \le (V_{eREF+} - V_{eREF-}) \le 1.6\ V$, $C_{VeREF+} = 20\ pF$	2.2 V, 3 V			±1.0	LSB
		$1.6\ V < (V_{eREF+} - V_{eREF-}) \le V_{AVCC}$, $C_{VeREF+} = 20\ pF$				±1.0	
E_D	Differential linearity error	$1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$	2.2 V, 3 V			±1.0	LSB
E_O	Offset error	$1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, Internal impedance of source $R_S < 100\ \Omega$	2.2 V, 3 V			±1.0	LSB
E_G	Gain error	$1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, ADC10SREFx = 11b	2.2 V, 3 V			±1.0	LSB
E_T	Total unadjusted error	$1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$, ADC10SREFx = 11b	2.2 V, 3 V		±1.0	±2.0	LSB

5.38 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}$ (2)		1.4		AV_{CC}	V
V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}$ (3)		0		1.2	V
$(V_{eREF+} - V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}$ (4)		1.4		AV_{CC}	V
I_{VeREF+} I_{VeREF-}	Static input current	$1.4\ V \le V_{eREF+} \le V_{AVCC}$, $V_{eREF-} = 0\ V$, $f_{ADC10CLK} = 5\ MHz$, ADC10SHTx = 0x0001, Conversion rate 200 ksps	2.2 V, 3 V		±8.5	±26	µA
		$1.4\ V \le V_{eREF+} \le V_{AVCC}$, $V_{eREF-} = 0\ V$, $f_{ADC10CLK} = 5\ MHZ$, ADC10SHTX = 0x1000, Conversion rate 20 ksps	2.2 V, 3 V			±1	
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	(5)		10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

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5.39 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage	REFVSEL = {2} for 2.5 V, REFON = 1	3 V		2.51	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	3 V		1.99	±1.5%	
		REFVSEL = {0} for 1.5 V, REFON = 1	2.2 V, 3 V		1.5	±1.5%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal[2]	$f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V	3 V		18	24	µA
		$f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V	3 V		15.5	21	
		$f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V	3 V		13.5	21	
TC_{REF+}	Temperature coefficient of built-in reference[3]	I_{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1			30	50	ppm/°C
I_{SENSOR}	Operating supply current into AVCC terminal[4]	REFON = 0, INCH = 0Ah, ADC10ON = N/A, T_A = 30°C	2.2 V		20	22	µA
			3 V		20	22	
V_{SENSOR}	See [5]	ADC10ON = 1, INCH = 0Ah, T_A = 30°C	2.2 V		770		mV
			3 V		770		
V_{MID}	AVCC divider at channel 11	ADC10ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected[6]	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB		30			µs
$t_{VMID(sample)}$	Sample time required if channel 11 is selected[7]	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB		1			µs
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1			120		µV/V
PSRR_AC	Power supply rejection ratio (AC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1			6.4		mV/V
t_{SETTLE}	Settling time of reference voltage[8]	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), REFVSEL = {0, 1, 2}, REFON = 0 → 1			75		µs

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The internal reference current is supplied from terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(5) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on-time $t_{SENSOR(on)}$.
(7) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
(8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.40 Comparator B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRS = 00	1.8 V			40	µA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01, CBON = 1, CBRS = 00	2.2 V, 3 V		10	17	
		CBPWRMD = 10, CBON = 1, CBRS = 00	2.2 V, 3 V		0.1	0.5	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Includes REF module current	CBREFACC = 1, CBREFLx = 01, CBRS = 10, REFON = 0, CBON = 0	2.2 V, 3 V		10	17	µA
		CBREFACC = 0, CBREFLx = 01, CBRS = 10, REFON = 0, CBON = 0	2.2 V, 3 V			22	
V_{IC}	Common mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01 or 10				±10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.0	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t_{EN_CMP}	Comparator enable time	CBON = 0 to CBON = 1 CBPWRMD = 00 or 01			1	2	µs
		CBON = 0 to CBON = 1 CBPWRMD = 10				100	
t_{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	µs
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

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5.41 Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{USB} = 3.3 V ±10%, I_{OH} = –25 mA. See Figure 5-17 for typical characteristics	2.4		V
V_{OL}	Low-level output voltage	V_{USB} = 3.3 V ±10%, I_{OL} = 25 mA. See Figure 5-16 for typical characteristics		0.4	V
V_{IH}	High-level input voltage	V_{USB} = 3.3 V ±10% See Figure 5-18 for typical characteristics	2.0		V
V_{IL}	Low-level input voltage	V_{USB} = 3.3 V ±10% See Figure 5-18 for typical characteristics		0.8	V

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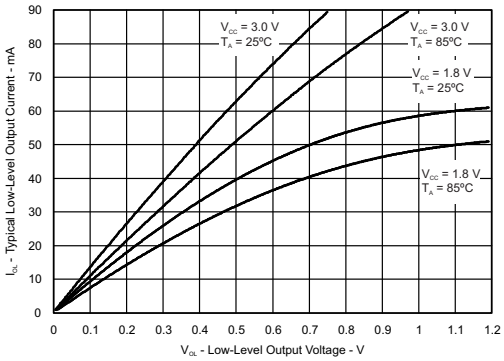

Figure 5-16. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

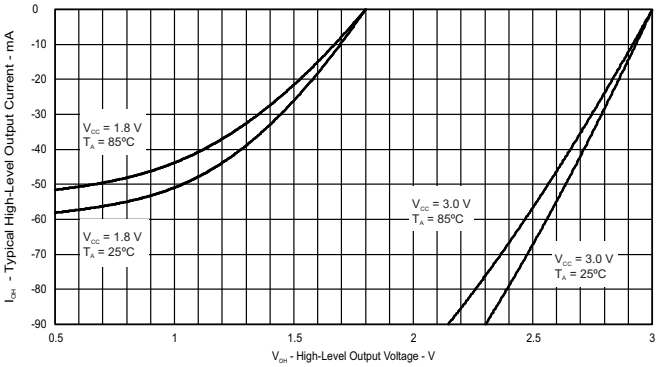

Figure 5-17. Ports PU.0, PU.1 Typical High-Level Output Characteristics

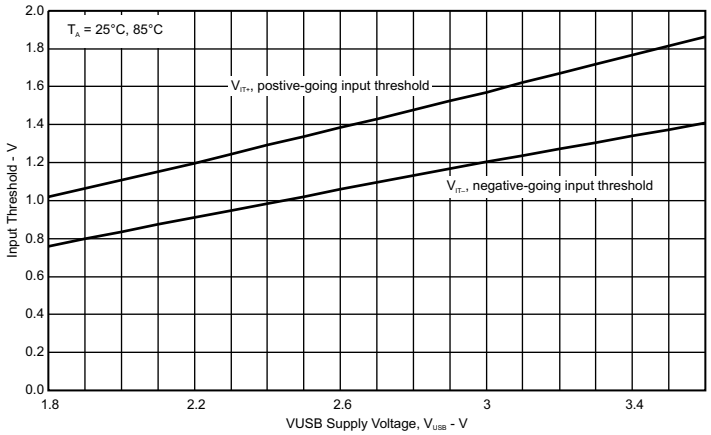

Figure 5-18. Ports PU.0, PU.1 Typical Input Threshold Characteristics

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5.42 USB Output Ports (DP and DM)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D- single ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D- single ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D- impedance	Including external series resistor of 27 Ω	28	44	Ω
t_{RISE}	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_{FALL}	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

5.43 USB Input Ports (DP and DM)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
V_{CM}	Differential input common mode range	0.8	2.5	V
Z_{IN}	Input impedance	300		kΩ
V_{CRS}	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic low level		0.8	V
V_{IH}	Static SE input logic high level	2.0		V
V_{DI}	Differential input voltage		0.2	V

5.44 USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{LAUNCH}	V_{BUS} detection threshold					3.75	V
V_{BUS}	USB bus voltage	Normal operation		3.76		5.5	V
V_{USB}	USB LDO output voltage				3.3	±9%	V
V_{18}	Internal USB voltage (1)				1.8		V
I_{USB_EXT}	Maximum external current from VUSB terminal (2)	USB LDO is on				12	mA
I_{DET}	USB LDO current overload detection (3)			60		100	mA
$I_{SUSPEND}$	Operating supply current into VBUS terminal (4)	USB LDO on, USB PLL disabled				250	µA
I_{USB_LDO}	Operating supply current into VBUS terminal, Represents the current of the 3.3-V LDO only	USB LDO on, USB 1.8-V LDO disabled, V_{BUS} = 5 V, USBDETEN = 0 or 1	1.8 V, 3 V		60		µA
I_{VBUS_DETECT}	Operating supply current into VBUS terminal, Represents the current of the VBUS detection logic	USB LDO disabled, USB 1.8-V LDO disabled, VBUS > V_{LAUNCH}, USBDETEN = 1	1.8 V, 3 V		30		µA
C_{BUS}	VBUS terminal recommended capacitance				4.7		µF
C_{USB}	VUSB terminal recommended capacitance				220		nF
C_{18}	V18 terminal recommended capacitance				220		nF
t_{ENABLE}	Settling time V_{USB} and V_{18}	Within 2%, recommended capacitances				2	ms
R_{PUR}	Pullup resistance of PUR terminal (5)			70	110	150	Ω

(1) This voltage is for internal use only. No external DC loading should be applied.
(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.
(3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.
(4) Does not include current contribution of Rpu and Rpd as outlined in the USB specification.
(5) This value, in series with an external resistor between PUR and D+, produces the Rpu as outlined in the USB specification.

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5.45 USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
I_{PLL}	Operating supply current			7	mA
f_{PLL}	PLL frequency		48		MHz
f_{UPD}	PLL reference frequency	1.5		3	MHz
t_{LOCK}	PLL lock time			2	ms
t_{Jitter}	PLL jitter		1000		ps

5.46 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_J	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
$t_{READMARGIN}$	Read access time during marginal mode				200	ns
I_{PGM}	Supply current from DVCC during program			3	5	mA
I_{ERASE}	Supply current from DVCC during erase			2	6.5	mA
I_{MERASE}, I_{BANK}	Supply current from DVCC during mass erase or bank erase			2	6.5	mA
t_{CPT}	Cumulative program time(1)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	25°C	100			years
t_{Word}	Word or byte program time(2)		64		85	µs
$t_{Block, 0}$	Block program time for first byte or word(2)		49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word(2)		37		49	µs
$t_{Block, N}$	Block program time for last byte or word(2)		55		73	µs
t_{Erase}	Erase time for segment, mass erase, and bank erase when available(2)		23		32	ms

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word write, individual byte write, and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

5.47 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency for 4-wire JTAG(2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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6 Detailed Description

6.1 CPU (Link to User's Guide)

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

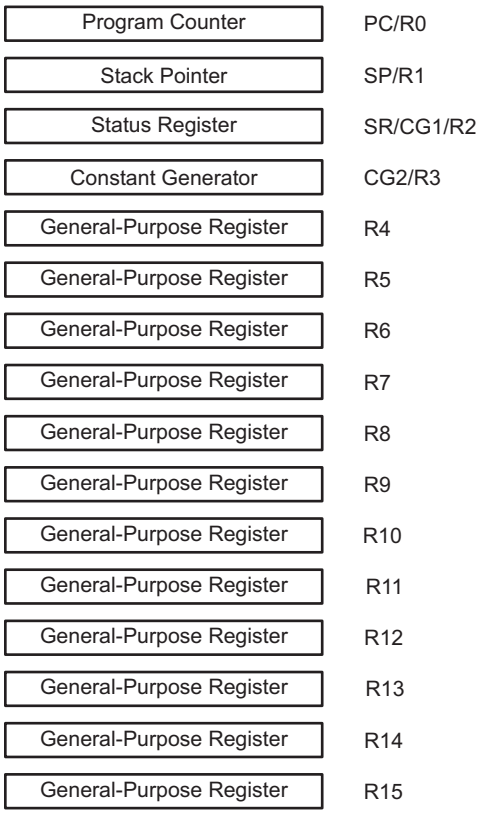

Figure 6-1. Integrated CPU Registers

6.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following seven operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, P1, and P2.

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6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-1). The vector contains the 16-bit address of the interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation	WDTIFG, KEYV (SYSRSTIV)(1) (2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBINIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1) (2)	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV)(1) (3)	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 (3)	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV)(1) (3)	Maskable	0FFF4h	58
Watchdog Timer_A interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (3)	Maskable	0FFF0h	56
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (3)	Maskable	0FFEEh	55
ADC10_A	ADC10IFG0(1) (3) (4)	Maskable	0FFECh	54
TA0	TA0CCR0 CCIFG0(3)	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (3)	Maskable	0FFE8h	52
USB_UBM	USB interrupts (USBIV)(1) (3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1) (3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (3)	Maskable	0FFE0h	48
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV)(1) (3)	Maskable	0FFDEh	47
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (3)	Maskable	0FFDCh	46
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (3)	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0(3)	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1) (3)	Maskable	0FFD6h	43
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)(1) (3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1) (3)	Maskable	0FFD2h	41
Reserved	Reserved(5)		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(3) Interrupt flags are in the module.
(4) Only on devices with ADC, otherwise reserved.
(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

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6.4 Memory Organization

Table 6-2 summarizes the memory map of all device variants.

Table 6-2. Memory Organization(1)

		MSP430F5504 MSP430F5500	MSP430F5508 MSP430F5505 MSP430F5501	MSP430F5509 MSP430F5506 MSP430F5502	MSP430F5510 MSP430F5507 MSP430F5503
Memory (flash) Main: interrupt vector Main: code memory	Total Size	8KB 00FFFFh–00FF80h 00FFFFh–00E000h	16KB 00FFFFh–00FF80h 00FFFFh–00C000h	24KB 00FFFFh–00FF80h 00FFFFh–00A000h	32KB 00FFFFh–00FF80h 00FFFFh–008000h
RAM	Sector 1	2KB 0033FFh–002C00h	2KB 0033FFh–002C00h	2KB 0033FFh–002C00h	2KB 0033FFh–002C00h
	Sector 0	2KB 002BFFh–002400h	2KB 002BFFh–002400h	2KB 002BFFh–002400h	2KB 002BFFh–002400h
USB RAM(2)		2KB 0023FFh–001C00h	2KB 0023FFh–001C00h	2KB 0023FFh–001C00h	2KB 0023FFh–001C00h
Information memory (flash)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootloader (BSL) memory (flash)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–0h	4KB 000FFFh–0h	4KB 000FFFh–0h	4KB 000FFFh–0h

(1) N/A = Not available
(2) USB RAM can be used as general purpose RAM when not used for USB operation.

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6.5 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory through the BSL is protected by an user-defined password. For complete description of the features of the BSL and its implementation, see *MSP430 Programming With the Bootloader (BSL)*.

6.5.1 USB BSL

All devices come preprogrammed with the USB BSL. Use of the USB BSL requires external access to six pins (see Table 6-3). In addition to these pins, the application must support external components necessary for normal USB operation (for example, proper crystal on XT2IN and XT2OUT and proper decoupling). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-3. USB BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
PU.0/DP	USB data terminal DP
PU.1/DM	USB data terminal DM
PUR	USB pullup resistor terminal
VBUS	USB bus power supply
VSSU	USB ground supply

NOTE

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the BSL should be invoked, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-MΩ resistor to ground.

6.5.2 UART BSL

A UART BSL is also available that can be programmed by the user into the BSL memory by replacing the pre-programmed factory-supplied USB BSL. Use of the UART BSL requires external access to six pins (see Table 6-4). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

Table 6-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

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6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-5 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For complete description of the features of the JTAG interface and its implementation, see the *MSP430 Memory Programming With the JTAG Interface*.

Table 6-5. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-6 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For complete description of the features of the JTAG interface and its implementation, see the *MSP430 Memory Programming With the JTAG Interface*.

Table 6-6. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 Flash Memory (Link to User's Guide)

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

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6.8 RAM (Link to User's Guide)

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in Section 6.4.
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

6.9.1 Digital I/O (Link to User's Guide)

Up to six 8-bit I/O ports are implemented: for 64-pin options, P1, P2, P4, P6, and are complete, P5 is reduced to 6-bit I/O, and P3 to 5-bit I/O. For 48-pin options, P6 is reduced to 4-bit I/O, P2 to 1-bit I/O, and P3 is completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wake-up input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P6) or word-wise in pairs (PA through PC).

6.9.2 Port Mapping Controller (Link to User's Guide)

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see Table 6-7). Table 6-8 lists the default settings for all pins that support port mapping.

Table 6-7. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT0	–	Comparator_B output
	PM_TB0CLK	TB0 clock input	–
2	PM_ADC10CLK	–	ADC10CLK
	PM_DMAE0	DMAE0 input	–
3	PM_SVMOUT	–	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	–
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI – input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	

Table 6-7. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI – output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I2C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I2C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19	PM_RTCCLK	None	RTCCLK output
20	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI – input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
21	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI – output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
22	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI)	
23	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I2C clock (open drain and direction controlled by USCI)	
24	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I2C data (open drain and direction controlled by USCI)	
25	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI)	
26–30	Reserved	None	DVSS
31 (0FFh) (1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

Table 6-8. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I2C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I2C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI – output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI – input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

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6.9.3 Oscillator and System Clock (Link to User's Guide)

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the XT1, XT2, VLO, REFO, or DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power-Management Module (PMM) (Link to User's Guide)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier (MPY) (Link to User's Guide)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.9.6 Real-Time Clock (RTC_A) (Link to User's Guide)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.9.7 Watchdog Timer (WDT_A) (Link to User's Guide)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 System Module (SYS) (Link to User's Guide)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. Table 6-9 lists the SYS module interrupt vector registers.

Table 6-9. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wake up from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

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6.9.9 DMA Controller (Link to User's Guide)

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion register to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 6-10 lists the DMA trigger assignments, which are also used by the USB timestamp generator.

Table 6-10. DMA Trigger Assignments(1)

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC10IFG0(2)	ADC10IFG0(2)	ADC10IFG0(2)
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	USB FNRXD	USB FNRXD	USB FNRXD
28	USB ready	USB ready	USB ready
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no Trigger1 is generated.
(2) Only on devices with ADC. Reserved on devices without ADC.

6.9.10 Universal Serial Communication Interface (USCI) (Links to User's Guide: UART Mode, SPI Mode, I²C Mode)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I²C.

The MSP430F55xx series includes two complete USCI modules (n = 0, 1).

6.9.11 TA0 (Link to User's Guide)

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-11). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
18, H2-P1.0	14-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
18, H2-P1.0	14-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
19, H3-P1.1	15-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	19, H3-P1.1	15-P1.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
20, J3-P1.2	16-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	20, J3-P1.2	16-P1.2
		CBOUT (internal)	CCI1B				ADC10 (internal)(1) ADC10SHSx = {1}	ADC10 (internal)(1) ADC10SHSx = {1}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
21, G4-P1.3	17-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	21, G4-P1.3	17-P1.3
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
22, H4-P1.4	18-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	22, H4-P1.4	18-P1.4
		DV_{SS}	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
23, J4-P1.5	19-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	23, J4-P1.5	19-P1.5
		DV_{SS}	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Only on devices with ADC.

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6.9.12 TA1 (Link to User's Guide)

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-12). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
24, G5-P1.6	20-P1.6	TA1CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
24, G5-P1.6	20-P1.6	TA1CLK	$\overline{\text{TACLK}}$					
25, H5-P1.7	21-P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	25, H5-P1.7	21-P1.7
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
26, J5-P2.0	22-P2.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	26, J5-P2.0	22-P2.0
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
27, G6-P2.1		TA1.2	CCI2A	CCR2	TA2	TA1.2	27, G6-P2.1	
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

6.9.13 TA2 (Link to User's Guide)

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE	RGZ, PT						RGC, ZQE	RGZ, PT
28, J6-P2.2		TA2CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
28, J6-P2.2		TA2CLK	$\overline{\text{TACLK}}$					
29, H6-P2.3		TA2.0	CCI0A	CCR0	TA0	TA2.0	29, H6-P2.3	
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
30, J7-P2.4		TA2.1	CCI1A	CCR1	TA1	TA2.1	30, J7-P2.4	
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
31, J8-P2.5		TA2.2	CCI2A	CCR2	TA2	TA2.2	31, J8-P2.5	
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

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6.9.14 TB0 (Link to User's Guide)

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-14). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-14. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, ZQE(1)	RGZ, PT(1)						RGC, ZQE(1)	RGZ, PT(1)
		TB0CLK	TBCLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
		TB0CLK	$\overline{\text{TBCLK}}$					
		TB0.0	CCI0A	CCR0	TB0	TB0.0	ADC10 (internal)(2) ADC10SHSx = {2}	ADC10 (internal)(2) ADC10SHSx = {2}
		TB0.0	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.1	CCI1A	CCR1	TB1	TB0.1	ADC10 (internal) ADC10SHSx = {3}	ADC10 (internal) ADC10SHSx = {3}
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.2	CCI2A	CCR2	TB2	TB0.2		
		TB0.2	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.3	CCI3A	CCR3	TB3	TB0.3		
		TB0.3	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.4	CCI4A	CCR4	TB4	TB0.4		
		TB0.4	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.5	CCI5A	CCR5	TB5	TB0.5		
		TB0.5	CCI5B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
		TB0.6	CCI6A	CCR6	TB6	TB0.6		
		ACLK (internal)	CCI6B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Timer functions selectable through the port mapping controller.
(2) Only on devices with ADC.

6.9.15 Comparator_B (Link to User's Guide)

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.16 ADC10_A (Link to User's Guide)

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.9.17 CRC16 (Link to User's Guide)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.18 Reference (REF) Voltage Reference (Link to User's Guide)

The REF module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.19 Universal Serial Bus (USB) (Link to User's Guide)

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and supports a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

6.9.20 Embedded Emulation Module (EEM) (S Version) (Link to User's Guide)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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6.10 Peripheral File Map

Table 6-15 lists the base address for the registers of all supported peripherals.

Table 6-15. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-16)	0100h	000h–01Fh
PMM (see Table 6-17)	0120h	000h–010h
Flash Control (see Table 6-18)	0140h	000h–00Fh
CRC16 (see Table 6-19)	0150h	000h–007h
RAM Control (see Table 6-20)	0158h	000h–001h
Watchdog (see Table 6-21)	015Ch	000h–001h
UCS (see Table 6-22)	0160h	000h–01Fh
SYS (see Table 6-23)	0180h	000h–01Fh
Shared Reference (see Table 6-24)	01B0h	000h–001h
Port Mapping Control (see Table 6-25)	01C0h	000h–002h
Port Mapping Port P4 (see Table 6-25)	01E0h	000h–007h
Port P1, P2 (see Table 6-26)	0200h	000h–01Fh
Port P3, P4 (see Table 6-27)	0220h	000h–00Bh
Port P5, P6 (see Table 6-28)	0240h	000h–00Bh
Port PJ (see Table 6-29)	0320h	000h–01Fh
TA0 (see Table 6-30)	0340h	000h–02Eh
TA1 (see Table 6-31)	0380h	000h–02Eh
TB0 (see Table 6-32)	03C0h	000h–02Eh
TA2 (see Table 6-33)	0400h	000h–02Eh
Real-Time Clock (RTC_A) (see Table 6-34)	04A0h	000h–01Bh
32-Bit Hardware Multiplier (see Table 6-35)	04C0h	000h–02Fh
DMA General Control (see Table 6-36)	0500h	000h–00Fh
DMA Channel 0 (see Table 6-36)	0510h	000h–00Ah
DMA Channel 1 (see Table 6-36)	0520h	000h–00Ah
DMA Channel 2 (see Table 6-36)	0530h	000h–00Ah
USCI_A0 (see Table 6-37)	05C0h	000h–01Fh
USCI_B0 (see Table 6-38)	05E0h	000h–01Fh
USCI_A1 (see Table 6-39)	0600h	000h–01Fh
USCI_B1 (see Table 6-40)	0620h	000h–01Fh
ADC10_A (see Table 6-41)	0740h	000h–01Fh
Comparator_B (see Table 6-42)	08C0h	000h–00Fh
USB configuration (see Table 6-43)	0900h	000h–014h
USB control (see Table 6-44)	0920h	000h–01Fh

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Table 6-16. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-17. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-18. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-19. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-20. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-21. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

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Table 6-22. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 6-23. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-24. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 6-25. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key/ID	PMAPKEYID	00h
Port mapping control	PMAPCTL	02h
Port P4.0 mapping	P4MAP0	00h
Port P4.1 mapping	P4MAP1	01h
Port P4.2 mapping	P4MAP2	02h
Port P4.3 mapping	P4MAP3	03h
Port P4.4 mapping	P4MAP4	04h
Port P4.5 mapping	P4MAP5	05h
Port P4.6 mapping	P4MAP6	06h
Port P4.7 mapping	P4MAP7	07h

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Table 6-26. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-27. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

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Table 6-28. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 6-29. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 6-30. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

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Table 6-31. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-32. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-33. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

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Table 6-34. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter 1	RTCSEC/RTCNT1	10h
RTC minutes/counter 2	RTCMIN/RTCNT2	11h
RTC hours/counter 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

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Table 6-35. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

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Table 6-36. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 6-37. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-38. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 6-39. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 6-40. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

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Table 6-41. ADC10_A Registers (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A control 0	ADC10CTL0	00h
ADC10_A control 1	ADC10CTL1	02h
ADC10_A control 2	ADC10CTL2	04h
ADC10_A window comparator low threshold	ADC10LO	06h
ADC10_A window comparator high threshold	ADC10HI	08h
ADC10_A memory control 0	ADC10MCTL0	0Ah
ADC10_A conversion memory	ADC10MEM0	12h
ADC10_A interrupt enable	ADC10IE	1Ah
ADC10_A interrupt flags	ADC10IGH	1Ch
ADC10_A interrupt vector word	ADC10IV	1Eh

Table 6-42. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

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Table 6-43. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key/ID	USBKEYPID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB PLL control	USBPLLCTL	10h
USB PLL divider	USBPLLDIVB	12h
USB PLL interrupts	USBPLLIR	14h

Table 6-44. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint_0 configuration	USBIEPCNF_0	00h
Input endpoint_0 byte count	USBIEPCNT_0	01h
Output endpoint_0 configuration	USBOEPCNF_0	02h
Output endpoint_0 byte count	USBOEPCNT_0	03h
Input endpoint interrupt enables	USBIEPIE	0Eh
Output endpoint interrupt enables	USBOEPIE	0Fh
Input endpoint interrupt flags	USBIEPIFG	10h
Output endpoint interrupt flags	USBOEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	USBMAINT	16h
Time stamp	USBTSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	USBFUNADR	1Fh

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6.11 Input/Output Diagrams

6.11.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-45 summarizes the selection of the pin functions.

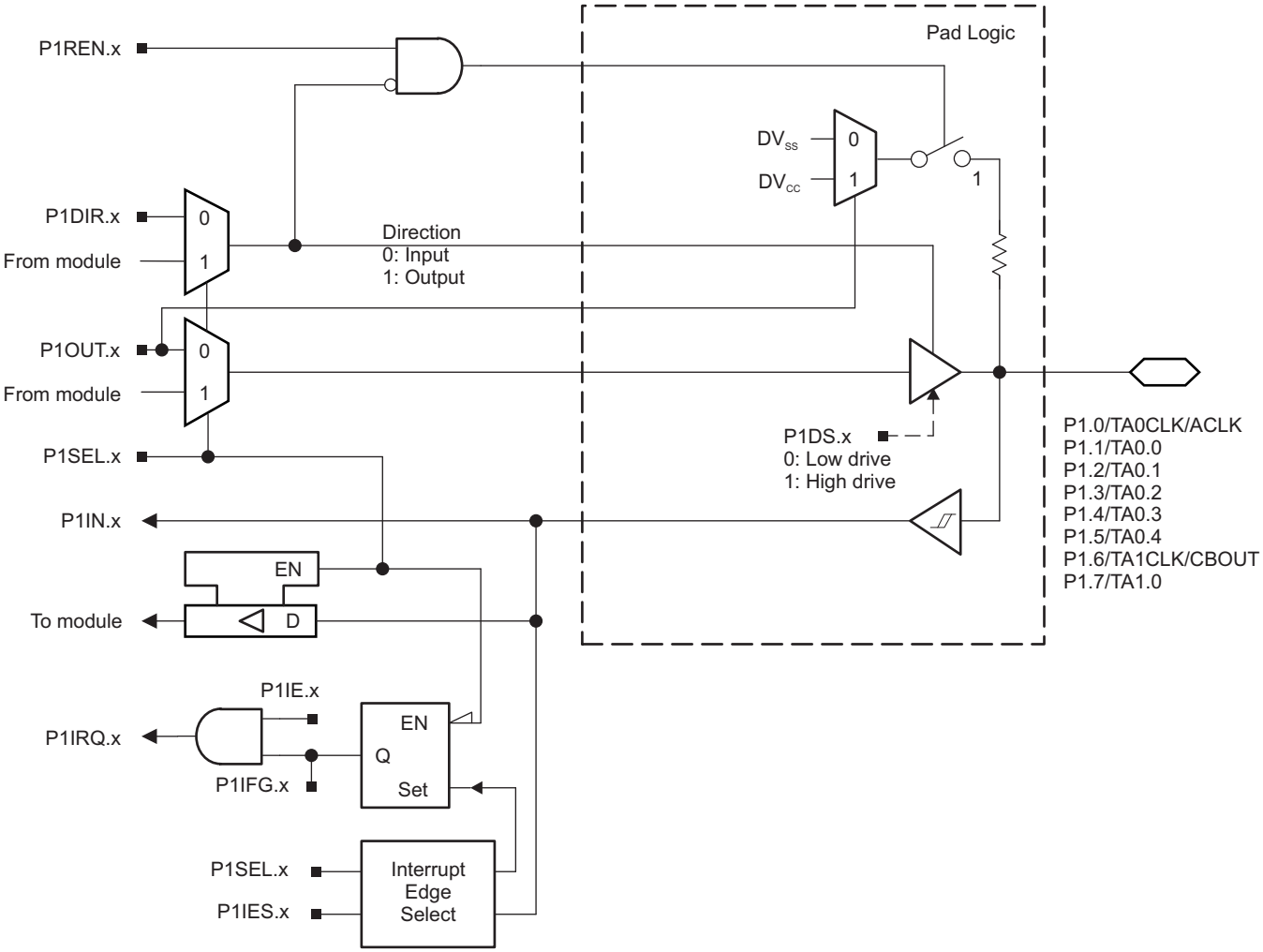

Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

Table 6-45. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

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6.11.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-46 summarizes the selection of the pin functions.

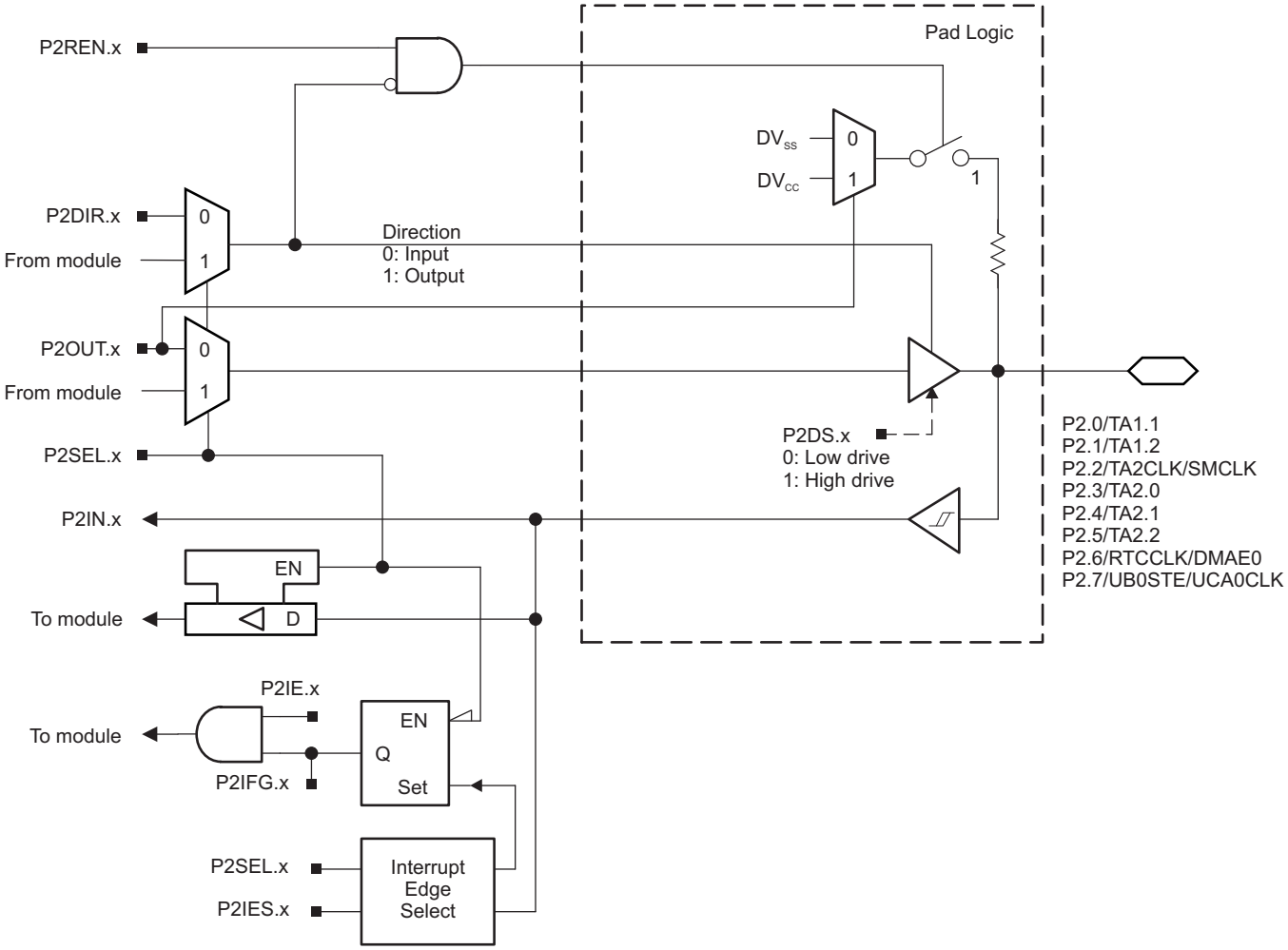

Figure 6-3. Port P2 (P2.0 to P2.7) Diagram

Table 6-46. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/TA2CLK/SMCLK	2	P2.2 (I/O)	I: 0; O: 1	0
		TA2CLK	0	1
		SMCLK	1	1
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.0	1	1
P2.4/TA2.1	4	P2.4 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.1	1	1
P2.5/TA2.2	5	P2.5 (I/O)	I: 0; O: 1	0
		TA2.CCI2A	0	1
		TA2.2	1	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK[2] [3]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

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6.11.3 Port P3 (P3.0 to P3.4) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

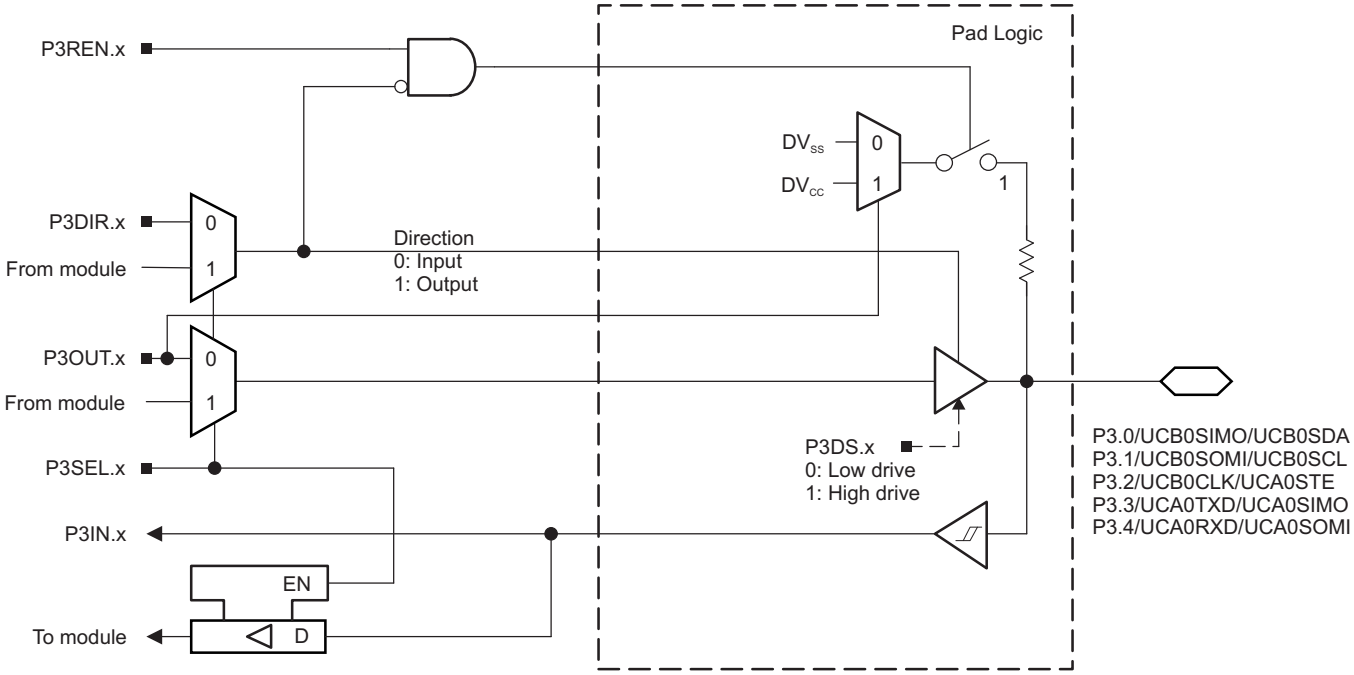

Figure 6-4. Port P3 (P3.0 to P3.7) Diagram

Table 6-47. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(2) (3)	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(2) (3)	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(2) (4)	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(2)	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(2)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.11.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-48 summarizes the selection of the pin functions.

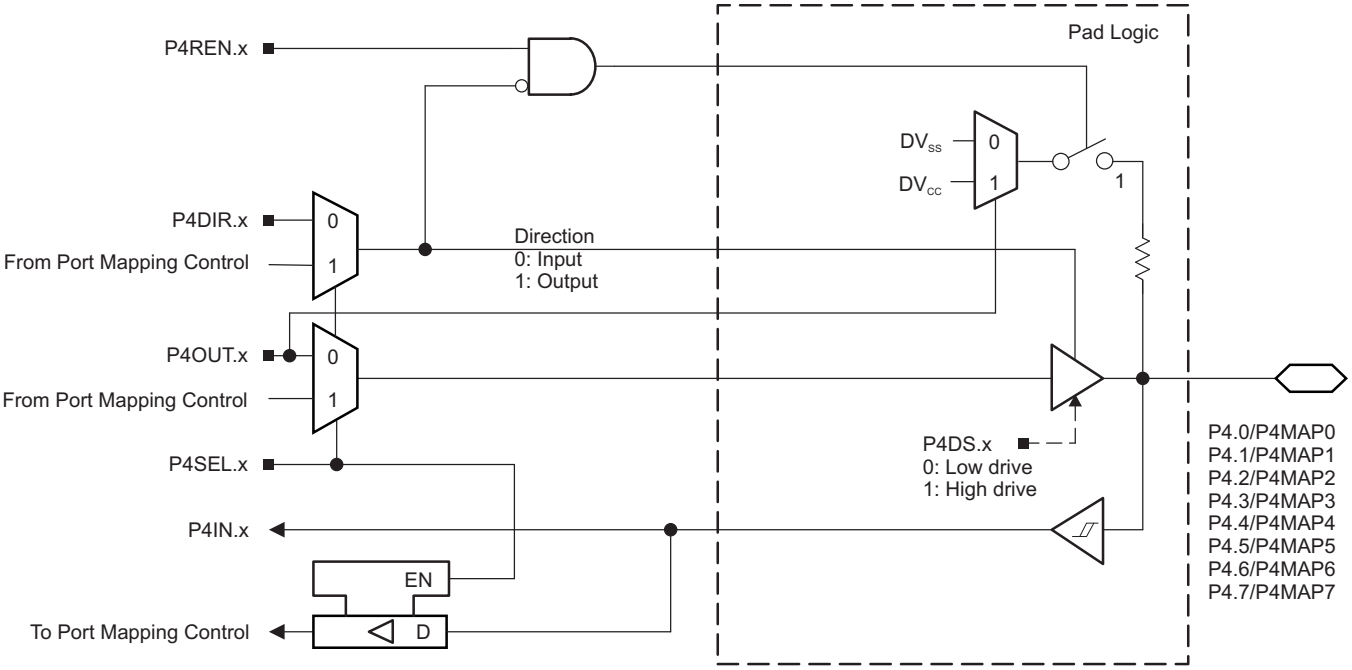

Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-48. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P4DIR.x(1)	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-7 for specific direction control information of mapped secondary functions.

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6.11.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-49 summarizes the selection of the pin functions.

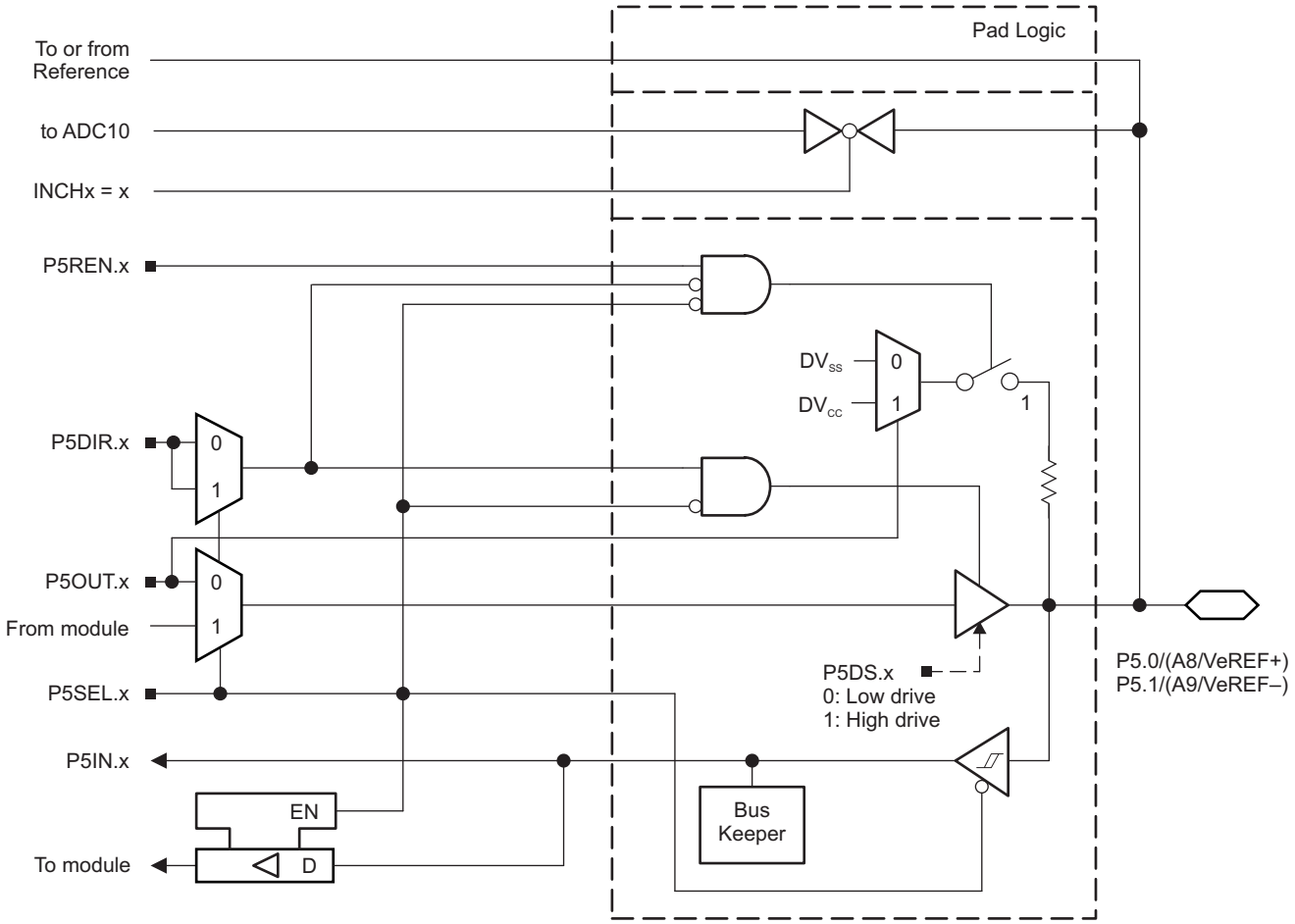

Figure 6-6. Port P5 (P5.0 and P5.1) Diagram

Table 6-49. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/A8/VeREF+(2)	0	P5.0 (I/O)(3)	I: 0; O: 1	0
		A8/VeREF+(4)	X	1
P5.1/A9/VeREF–(5)	1	P5.1 (I/O)(3)	I: 0; O: 1	0
		A9/VeREF–(6)	X	1

(1) X = Don't care
(2) VeREF+ available on devices with ADC10_A.
(3) Default condition
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10_A when available.
(5) VeREF- available on devices with ADC10_A.
(6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10_A when available.

6.11.6 Port P5 (P5.2) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

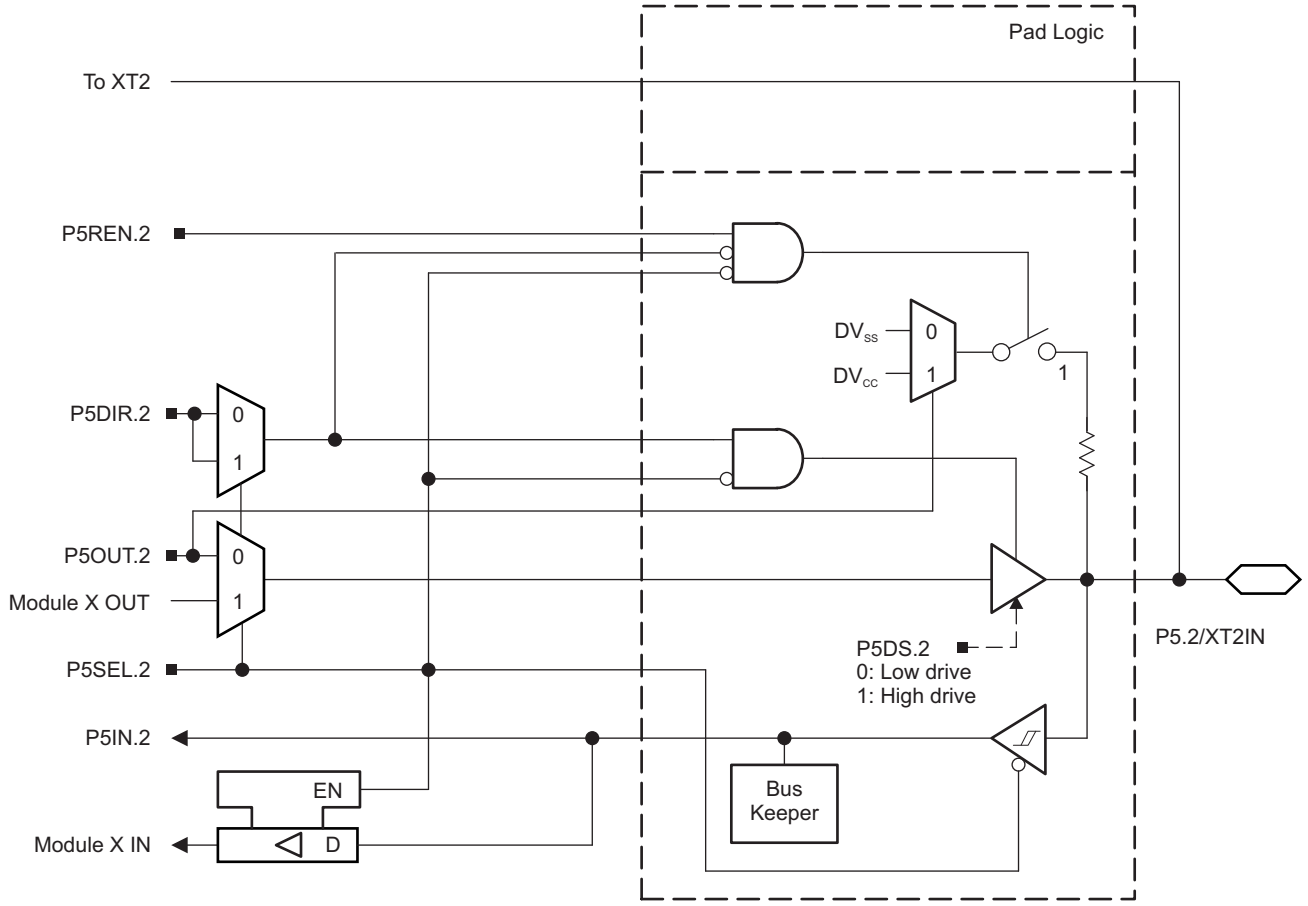

Figure 6-7. Port P5 (P5.2) Diagram

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6.11.7 Port P5 (P5.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

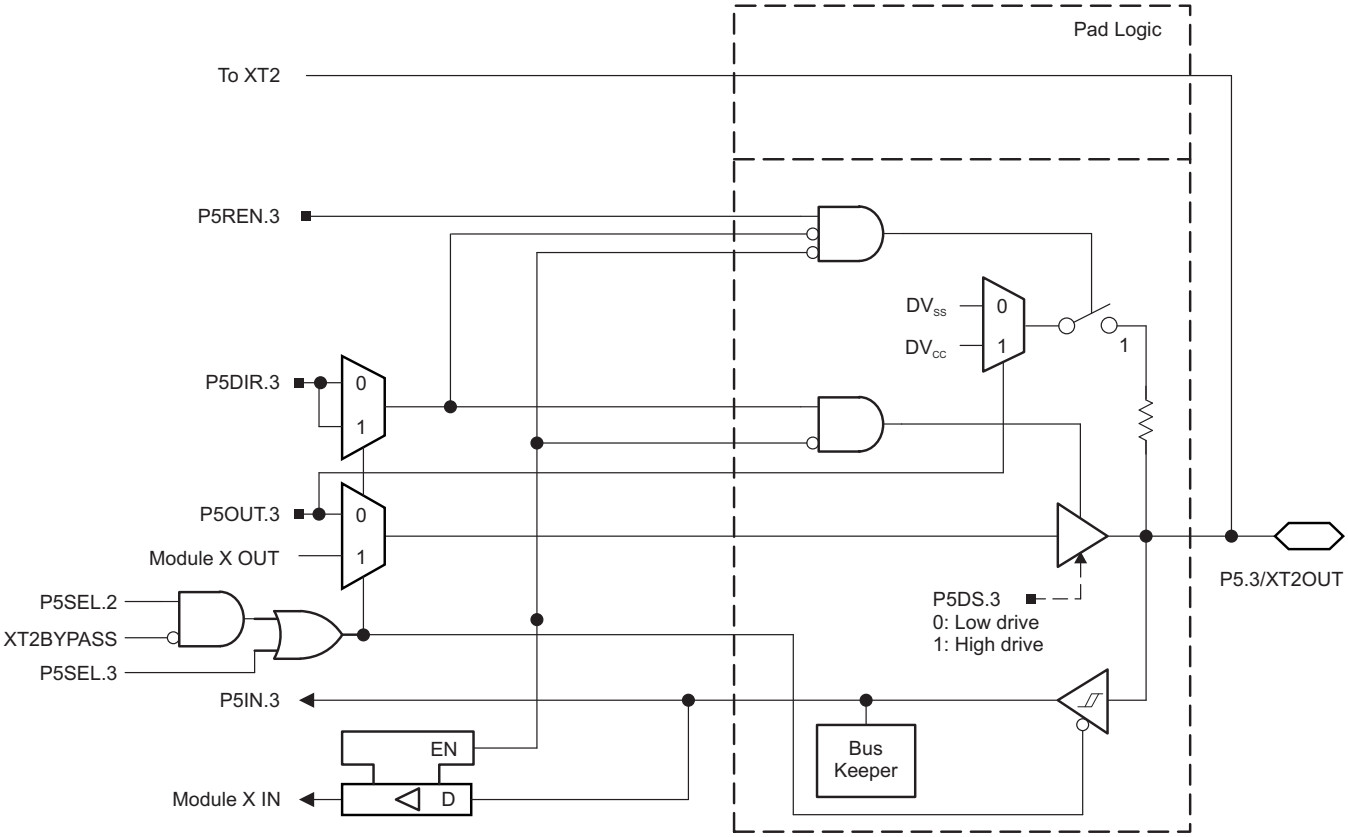

Figure 6-8. Port P5 (P5.3) Diagram

Table 6-50. Port P5 (P5.2 and P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	0	X
		XT2OUT crystal mode(3)	X	1	X	0
		P5.3 (I/O)(3)	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

6.11.8 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger

Figure 6-9 and Figure 6-10 show the port diagrams. Table 6-51 summarizes the selection of the pin functions.

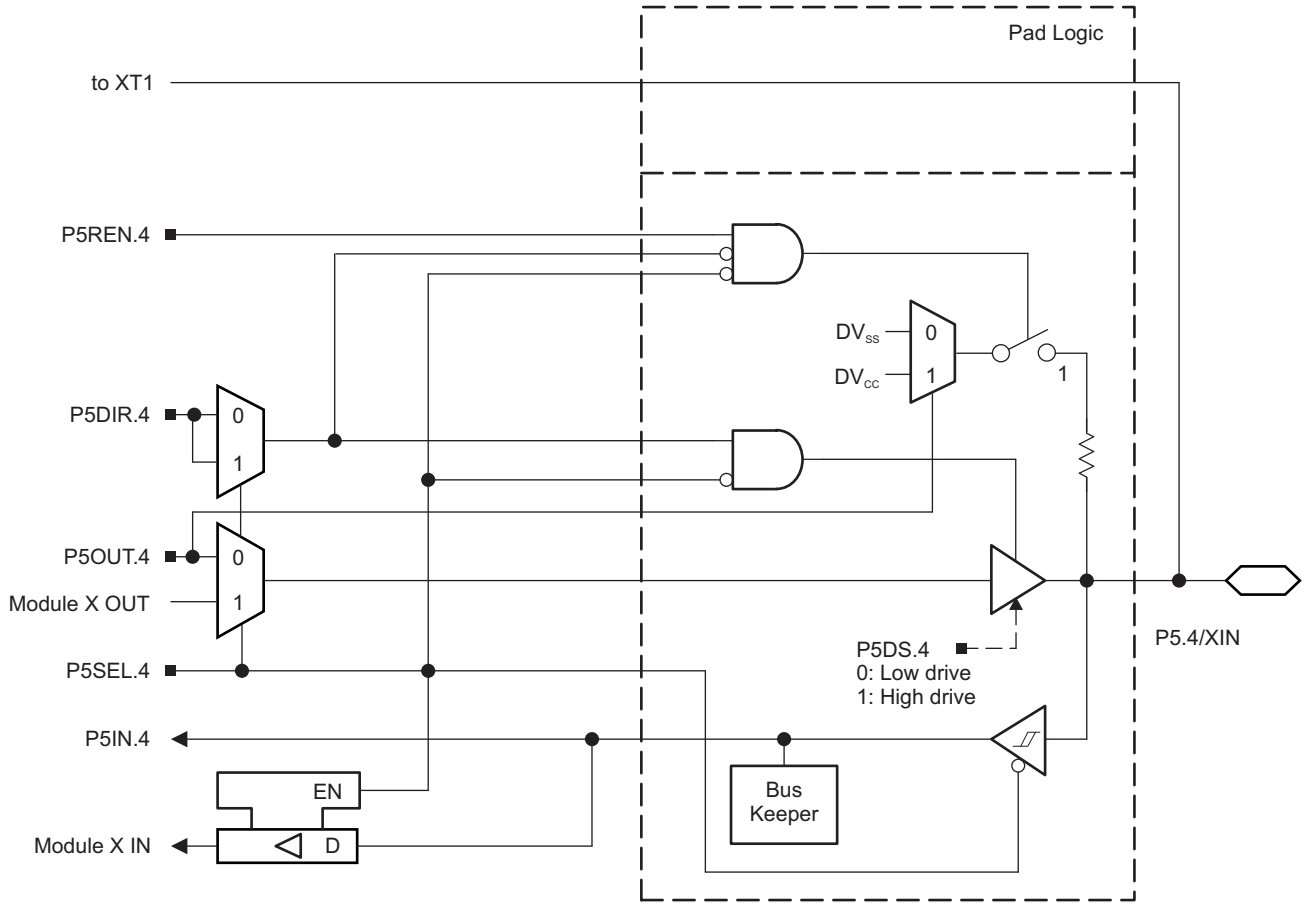

Figure 6-9. Port P5 (P5.4) Diagram

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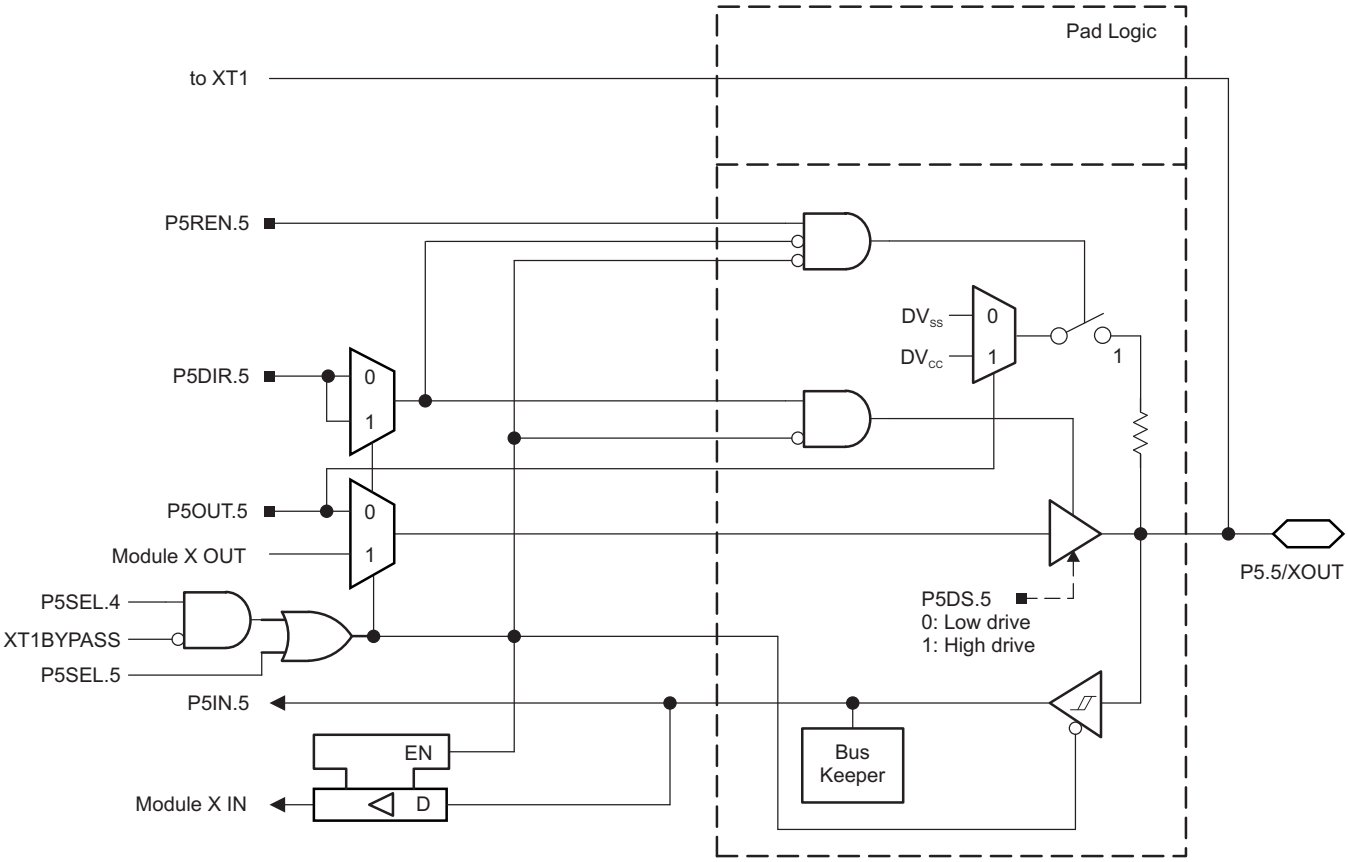

Figure 6-10. Port P5 (P5.5) Diagram

Table 6-51. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode[2]	X	1	X	0
		XIN bypass mode[2]	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	0	X
		XOUT crystal mode[3]	X	1	X	0
		P5.5 (I/O)[3]	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

6.11.9 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-52 summarizes the selection of the pin functions.

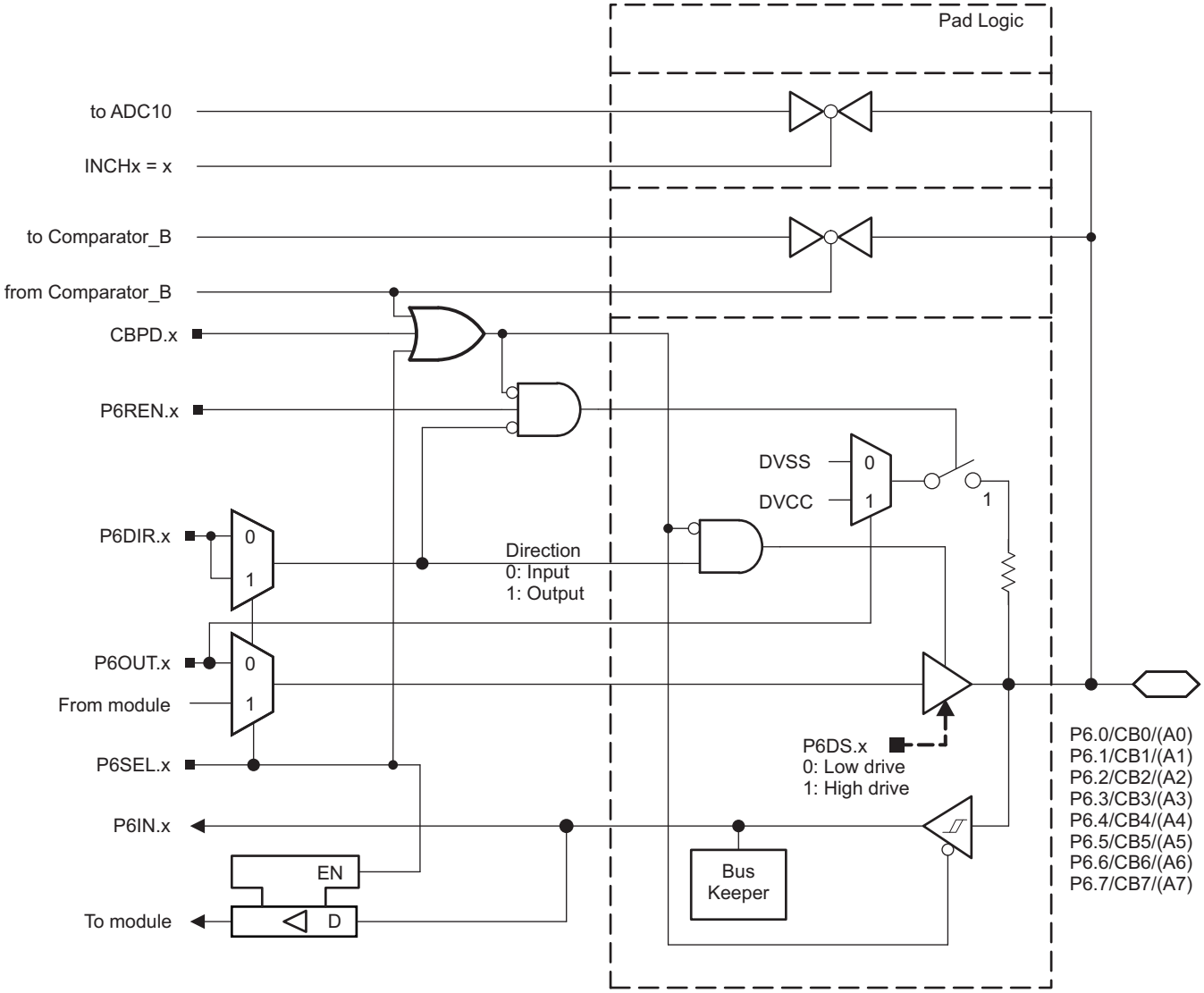

Figure 6-11. Port P6 (P6.0 to P6.7) Diagram

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Table 6-52. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P6DIR.x	P6SEL.x	CBPDx
P6.0/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (only on devices with ADC)	X	1	X
		CB0[(1)]	X	X	1
P6.1/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (only on devices with ADC)	X	1	X
		CB1[(1)]	X	X	1
P6.2/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (only on devices with ADC)	X	1	X
		CB2[(1)]	X	X	1
P6.3/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (only on devices with ADC)	X	1	X
		CB3[(1)]	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (only on devices with ADC)	X	1	X
		CB4[(1)]	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5 (only on devices with ADC)	X	1	X
		CB5[(1)]	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6 (only on devices with ADC)	X	1	X
		CB6[(1)]	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7 (only on devices with ADC)	X	1	X
		CB7[(1)]	X	X	1

(1) Setting the CBPDx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPDx bit.

6.11.10 Port U (PU.0/DP, PU.1/DM, PUR) USB Ports

Figure 6-12 shows the port diagram. Table 6-53 through Table 6-55 summarize the selection of the pin functions.

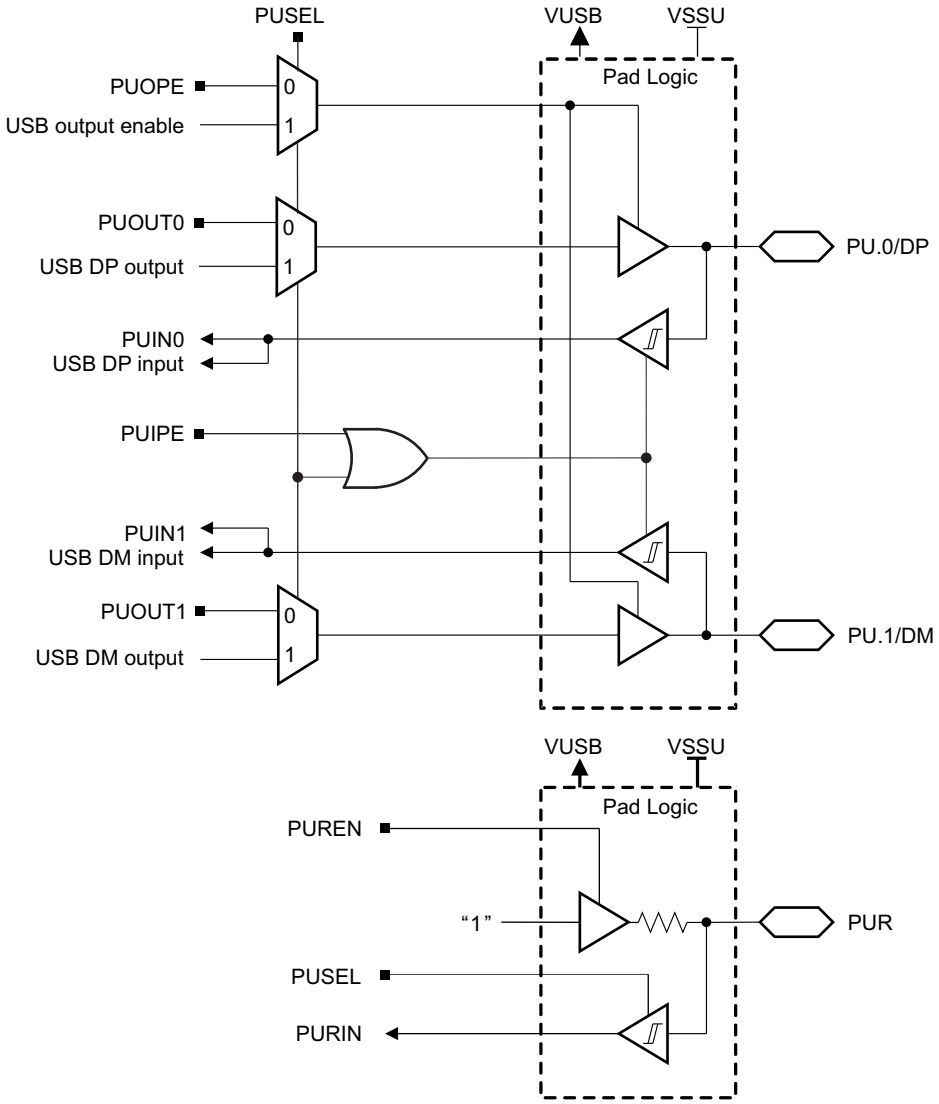

Figure 6-12. Port U (PU.0/DP, PU.1/DM, PUR) Diagram

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Table 6-53. Port U (PU.0/DP and PU.1/DM) Output Functions (1)

CONTROL BITS				PIN NAME	
PUSEL	PUOPE	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP
0	0	X	X	Output disabled	Output disabled
0	1	0	0	Output low	Output low
0	1	0	1	Output low	Output high
0	1	1	0	Output high	Output low
0	1	1	1	Output high	Output high
1	X	X	X	DM (2)	DP (2)

(1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.
(2) Output state set by the USB module.

Table 6-54. Port U (PU.0/DP and PU.1/DM) Input Functions (1)

CONTROL BITS		PIN NAME	
PUSEL	PUIPE	PU.1/DM	PU.0/DP
0	0	Input disabled	Input disabled
0	1	Input enabled	Input enabled
1	X	DM input	DP input

(1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.

Table 6-55. Port U (PUR) Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pullup disabled
0	1	Input disabled Pullup enabled
1	0	Input enabled Pullup disabled
1	1	Input enabled Pullup enabled

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6.11.11 Port J (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-13 shows the port diagram. Table 6-56 summarizes the selection of the pin functions.

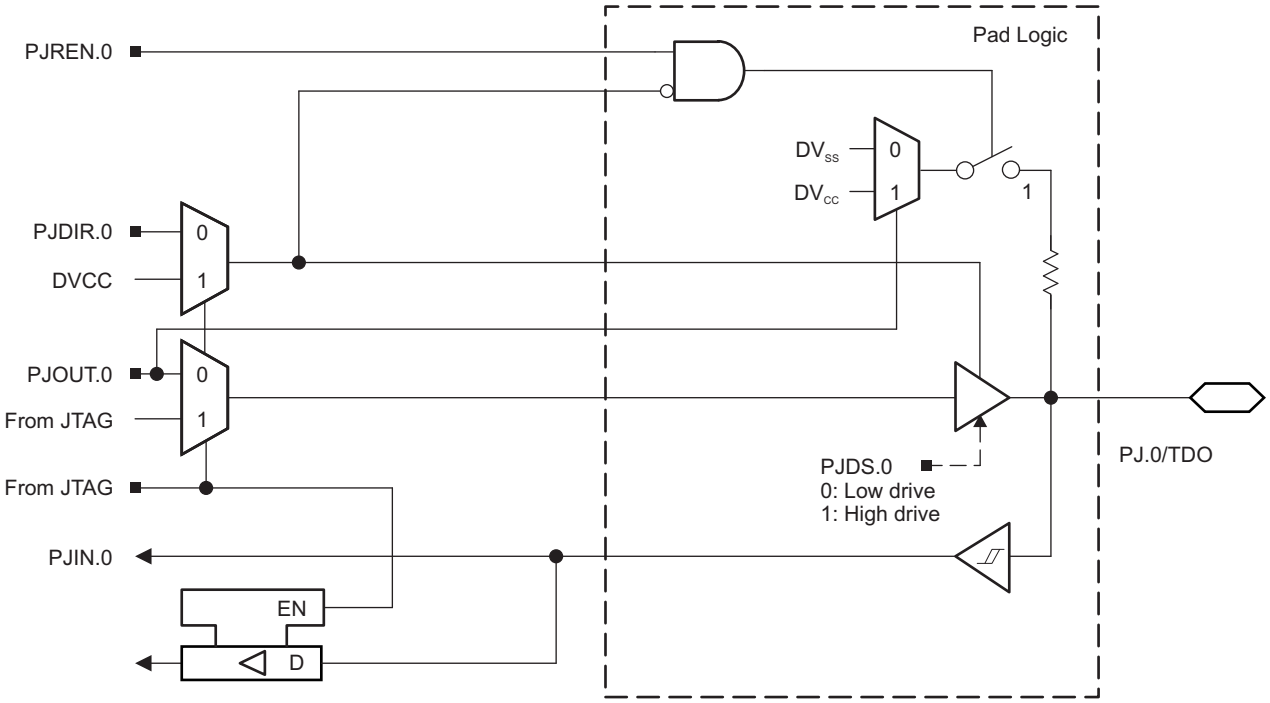

Figure 6-13. Port PJ (PJ.0) Diagram

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6.11.12 Port J (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-14 shows the port diagram. Table 6-56 summarizes the selection of the pin functions.

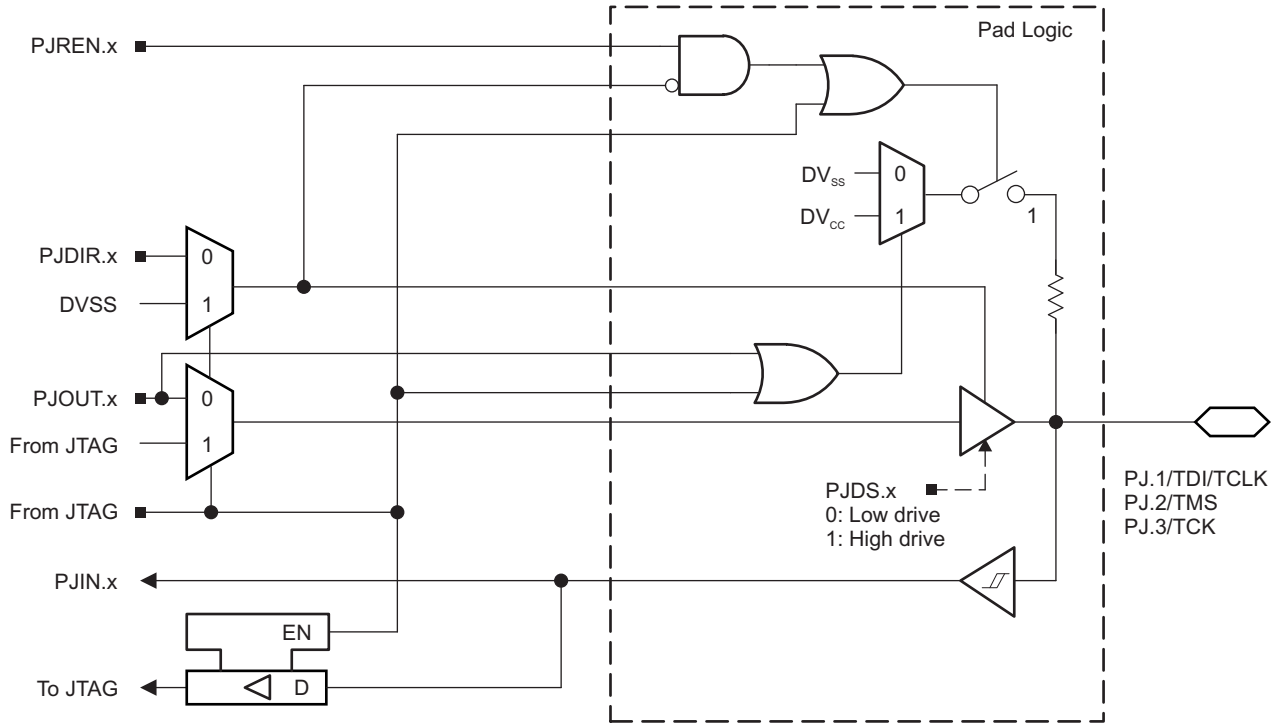

Figure 6-14. Port PJ (PJ.1 to PJ.3) Diagram

Table 6-56. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)(2)	I: 0; O: 1
		TDO(3)	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)(2)	I: 0; O: 1
		TDI/TCLK(3) (4)	X
PJ.2/TMS	2	PJ.2 (I/O)(2)	I: 0; O: 1
		TMS(3) (4)	X
PJ.3/TCK	3	PJ.3 (I/O)(2)	I: 0; O: 1
		TCK(3) (4)	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

6.12 Device Descriptors

Table 6-57 and Table 6-58 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-57. F5504 to F5510 Device Descriptor Table (1)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE									
				F5510		F5509		F5508		F5507	F5506	F5505	F5504
				RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT				
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	31h	31h	3Ah	3Ah	39h	39h	38h	37h	36h	35h
	Device ID	01A05h	1	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	ADC10 calibration tag	01A14h	1	13h	13h	13h	13h	13h	13h	13h	13h	13h	13h
	ADC10 calibration length	01A15h	1	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h
	ADC gain factor	01A16h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC offset	01A18h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temp. sensor 30°C	01A1Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temp. sensor 85°C	01A1Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temp. sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temp. sensor 85°C	01A20h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temp. sensor 30°C	01A22h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temp. sensor 85°C	01A24h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h	12h	12h	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

(1) N/A = Not applicable

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Table 6-57. F5504 to F5510 Device Descriptor Table [(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE									
				F5510		F5509		F5508		F5507	F5506	F5505	F5504
				RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT				
Peripheral Descriptor	Peripheral descriptor tag	01A2Eh	1	02h	02h	02h	02h	02h	02h	02h	02h	02h	02h
	Peripheral descriptor length	01A2Fh	1	61h	61h	62h	62h	61h	61h	5Dh	5Eh	5Dh	5Dh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	00Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	40h 92h	40h 92h	50h 91h	50h 91h	60h 90h	60h 90h	40h 92h	50h 91h	60h 90h	70h 8Eh
	Memory 6			N/A	N/A	8Eh	8Eh	N/A	N/A	N/A	8Eh	N/A	N/A
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	Peripheral count		1	20h	20h	20h	20h	20h	20h	1Eh	1Eh	1Eh	1Eh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-S		2	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h	00h 03h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1 and 2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3 and 4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5 and 6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h

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Table 6-57. F5504 to F5510 Device Descriptor Table [(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE									
				F5510		F5509		F5508		F5507	F5506	F5505	F5504
				RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT	RGC, ZQE	RGZ, PT				
Peripheral Descriptor (continued)	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A and USCI_B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	10h 90h	10h 90h	10h 90h	10h 90h
	USCI_A and USCI_B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	N/A	N/A	N/A	N/A
	ADC10_A		2	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h	14h D3h
	COMP_B		2	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h	18h A8h	N/A	N/A	N/A	N/A
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	1Ch 98h	1Ch 98h	1Ch 98h	1Ch 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h	A8h	01h	01h	01h	01h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h	90h	01h	01h	01h	01h
	USCI_B0		1	91h	91h	91h	91h	91h	91h	01h	01h	01h	01h
	ADC10_A		1	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h	68h	68h	68h	68h
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h

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Table 6-58. F5500 to F5503 Device Descriptor(1)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE			
				F5503	F5502	F5501	F5500
Info Block	Info length	01A00h	1	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	34h	33h	32h	3Bh
	Device ID	01A05h	1	80h	80h	80h	80h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	Empty tag	01A14h	1	05h	05h	05h	05h
	Empty tag length	01A15h	1	10h	10h	10h	10h
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit
Peripheral Descriptor	Peripheral descriptor tag	01A2Eh	1	02h	02h	02h	02h
	Peripheral descriptor length	01A2Fh	1	5Dh	5Eh	5Dh	5Dh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Ch	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	40h 92h	50h 91	60h 90h	70h 8Eh
	Memory 6		1	N/A	8E	N/A	N/A
	Delimiter		1	00h	00h	00h	00h
	Peripheral count		1	1Eh	1Eh	1Eh	1Eh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-S		2	00h 03h	00h 03h	00h 03h	00h 03h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h

(1) N/A = Not applicable

Table 6-58. F5500 to F5503 Device Descriptor[1] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE			
				F5503	F5502	F5501	F5500
Peripheral Descriptor (continued)	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1 and 2		2	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3 and 4		2	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5 and 6		2	02h 53h	02h 53h	02h 53h	02h 53h
	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A and USCI_B		2	10h 90h	10h 90h	10h 90h	10h 90h
	ADC10_A		2	N/A	N/A	N/A	N/A
	COMP_B		2	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h

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Table 6-58. F5500 to F5503 Device Descriptor[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE			
				F5503	F5502	F5501	F5500
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h
	USCI_A0		1	01h	01h	01h	01h
	USCI_B0		1	01h	01h	01h	01h
	ADC10_A		1	01h	01h	01h	01h
	TA0.CCIFG0		1	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h
	Delimiter		1	00h	00h	00h	00h

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7 デバイスおよびドキュメントのサポート

7.1 使い始めと次の手順

MSP430™ファミリのマイクロコントローラ、および開発に役立つツールやライブラリの詳細については、「MSP430 超低消費電力センシング/測定マイコンの概要」を参照してください。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 図 7-1 provides a legend for reading the complete device name.

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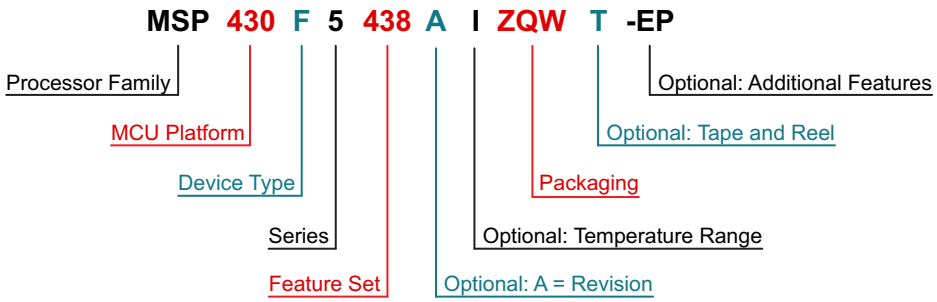

Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

図 7-1. Device Nomenclature

7.3 ツールとソフトウェア

すべてのMSPマイクロコントローラは、広範なソフトウェアおよびハードウェア開発ツールによりサポートされています。ツールは、TIおよびさまざまなサードパーティーから入手できます。すべての一覧は「MSP430超低消費電力マイコン – ツールとソフトウェア」で参照できます。

表 7-1 にMSP430F5510およびMSP430F550x MCUのデバッグ機能を示します。利用可能な機能の詳細については、*『MSP430用Code Composer Studio IDEユーザー・ガイド』*を参照してください。

表 7-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式JTAG	2線式JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート
MSP430Xv2	○	○	8	○	○	○	○	×

設計キットと評価モジュール

MSP430F5x MCU用の64ピン・ターゲット開発ボードとMSP-FETプログラマ・バンドル MSP-FET430U64USBは強力なフラッシュ・エミュレーション・ツールで、MSP430 MCUによるアプリケーション開発をすぐに開始できます。USBデバッグ・インターフェイスにより、JTAGインターフェイスまたは省ピンSpy Bi-Wire（2線式JTAG）プロトコルを使用してMSP430をインシステムでプログラミングおよびデバッグできます。MSP430のフラッシュ・メモリは、数回のキー操作により、数秒で消去およびプログラミングできます。また、極めて低消費電力であるため、外部電源は不要です。

MSP-TS430RGC64USB - MSP430F5x MCU用の64ピン・ターゲット開発ボード MSP-TS430RGC64USBはスタンドアロンの64ピンZIFソケット・ターゲット・ボードで、これによりJTAGインターフェイスまたはSpy Bi-Wire（2線式JTAG）プロトコルを使用してMSP430 MCUをインシステムでプログラミングおよびデバッグできます。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430用設計リソースの完全なコレクションに加えて、MSP430WareソフトウェアにはMSPドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430Wareソフトウェアは、 Code Composer Studio™IDEのコンポーネントとして、またはスタンドアロンのパッケージとして供給されています。

MSP430F550x、MSP430F5510 Cコード・サンプル すべてのMSPデバイス用に、内蔵する各ペリフェラルをさまざまな用途のニーズに合わせて構成するためのCコード・サンプルが用意されています。

MSPドライバ・ライブラリ ドライバ・ライブラリの抽象化APIで、使いやすい関数呼び出しが用意されており、MSP430ハードウェアのビットやバイトのレベルを意識せずに、より高水準の開発作業に集中できます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™テクノロジ MSP430マイクロコントローラ用のEnergyTraceテクノロジは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラ独自の超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorは、マイクロコントローラの熟練した開発者でも、新しい開発者でも使用でき、包括的なULPチェックリストと照らし合わせてコードのチェックを行い、アプリケーションの性能を最大限まで発揮できるようにします。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

MSP430 USB開発パッケージ MSP430 USB開発パッケージは、USBベースのMSP430プロジェクトの開発に必要なソース・コードとサンプル・アプリケーションがすべて揃ったソフトウェア・パッケージです。このパッケージはMSP430 USBデバイスのみをサポートします。

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IEC60730ソフトウェア・パッケージ IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ 低消費電力かつ低コストのマイクロコントローラ分野で継続的な革新を行うため、TIはMSPMATHLIBを提供しています。このスカラー関数の浮動小数点数値演算ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、最高26倍の性能を実現します。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio と IAR IDE の両方に組み込まれています。数値演算ライブラリと関連ベンチマークの詳細については、ユーザー・ガイドを参照してください。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studioは、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。Code Composer Studioは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。IDEは直感的で、アプリケーションの開発フローの各段階を、すべて同一のユーザー・インターフェイスで実行できます。使い慣れたユーティリティとインターフェイスにより、ユーザーは従来より迅速に作業を開始できます。Code Composer Studioは、Eclipseソフトウェア・フレームワークの利点と、TIの先進的な組み込みデバッグ機能の利点を組み合わせ、組み込み製品の開発者向けの魅力的な、豊富な機能を持つ開発環境を実現します。CCSをMSP MCUとともに使用すると、MSPマイクロコントローラを最大限に活用するための、ユニークで強力な一連のプラグインや組み込みソフトウェア・ユーティリティを利用できます。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txtまたは.hex) をMSPマイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合、デバッグ・プローブと呼ばれています。ユーザーはこのツールを使用して、MSP低消費電力マイクロコントローラ(MCU)のアプリケーション開発を迅速に開始できます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。MSP-FETは、ホスト・コンピュータとターゲットMSPの間で、デバッグ通信経路を提供します。さらに、MSP-FETはコンピュータのUSBインターフェイスとMSP UARTの間で、バックチャネルUART接続も提供します。これにより、MSPプログラマは、コンピュータ上で動作している端末ソフトウェアとMSPとの間で、シリアル通信を簡単に実行できます。また、UARTやI^2C通信プロトコルを経由するBSL (ブートローダー) を使用して、プログラム (多くの場合、ファームウェアと呼ばれます) をMSPターゲットにロードできます。

MSP-GANG量産プログラマ MSP Gang ProgrammerはMSP430またはMSP432用のデバイス・プログラマで、8つまでの同一のMSP430またはMSP432フラッシュまたはFRAMデバイスを同時にプログラムできます。MSP Gang Programmerは、標準のRS-232またはUSB接続を使用してホストPCに接続でき、柔軟なプログラミング・オプションにより、プロセスを完全にカスタマイズ可能です。MSP Gang Programmer には、Gang Splitter と呼ばれる拡張ボードが付属しており、MSP Gang Programmer と複数のターゲット・デバイスとの間で相互接続機能を実装します。拡張ボードと、8つのターゲット・デバイスとを接続するため、8本のケーブルが付属しています(JTAGまたはSpy-Bi-Wireコネクタ経由)。PCを使用してプログラムすることも、スタンドアロンのデバイスとしてプログラムすることもできます。PC側のグラフィカル・ユーザー・インターフェイスも用意されており、DLLベースです。

7.4 ドキュメントのサポート

以下のドキュメントはMSP430F550xマイクロコントローラについて記載したものです。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いの製品のフォルダへ移動します(プロダクト・フォルダへのリンクについては、表 7-2を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430F5510デバイス正誤表』 MSP430F5510の機能仕様における既知の例外が記載されています。

『MSP430F5509デバイス正誤表』 MSP430F5509の機能仕様における既知の例外が記載されています。

『MSP430F5508デバイス正誤表』 MSP430F5508の機能仕様における既知の例外が記載されています。

『MSP430F5507デバイス正誤表』 MSP430F5507の機能仕様における既知の例外が記載されています。

『MSP430F5506デバイス正誤表』 MSP430F5506の機能仕様における既知の例外が記載されています。

『MSP430F5505デバイス正誤表』 MSP430F5505の機能仕様における既知の例外が記載されています。

『MSP430F5504デバイス正誤表』 MSP430F5504の機能仕様における既知の例外が記載されています。

『MSP430F5503デバイス正誤表』 MSP430F5503の機能仕様における既知の例外が記載されています。

『MSP430F5502デバイス正誤表』 MSP430F5502の機能仕様における既知の例外が記載されています。

『MSP430F5501デバイス正誤表』 MSP430F5501の機能仕様における既知の例外が記載されています。

『MSP430F5500デバイス正誤表』 MSP430F5500の機能仕様における既知の例外が記載されています。

ユーザー・ガイド

『MSP430x5xxおよびMSP430x6xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なモジュールとペリフェラルについての詳細情報です。

『MSP430 フラッシュ・デバイス・ブートローダ(BSL)ユーザー・ガイド』 MSP430ブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430マイクロコントローラの組み込みメモリと通信を行うことができます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。このブートローダは、一部のデジタル・シグナル・プロセッサ(DSP)に見られる、外部メモリからDSPの内部メモリへプログラム・コード(およびデータ)を自動的にロードする、ブートストラップ・ローダ・プログラムとは異なることに注意してください。

『JTAGインターフェイスによるMSP430のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

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アプリケーション・レポート

『MSP430 32kHz水晶発振器』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。(1) コンポーネント・レベルESDテストとシステム・レベルESDテスト、その違い、コンポーネント・レベルESD評価ではシステム・レベルの耐性が保証されない理由。(2) 筐体、ケーブル、PCBレイアウト、オンボードのESD保護デバイスなど各レベルにおいてシステム・レベルのESD保護を行うための、一般的な設計ガイドライン。(3) System Efficient ESD Design (SEED)の概要、システム・レベルESD耐性を達成するオンボードおよびオンチップESD保護のコデザイン手法、サンプル・シミュレーションとテスト結果。現実世界でのシステム・レベルのESD保護設計の例のいくつかと、その結果についても解説します。

7.5 関連リンク

表 7-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430F5510	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5509	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5508	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5507	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5506	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5505	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5504	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5503	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5502	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5501	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5500	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 商標

MSP430, MSP430Ware, Code Composer Studio, EnergyTrace, ULP Advisor, E2E are trademarks of Texas Instruments.
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7.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

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7.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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8 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5500IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5500
MSP430F5500IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5500
MSP430F5500IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5500
MSP430F5500IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5500
MSP430F5501IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5501
MSP430F5501IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5501
MSP430F5501IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5501
MSP430F5501IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5501
MSP430F5502IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5502
MSP430F5502IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5502
MSP430F5502IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5502
MSP430F5502IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5502
MSP430F5503IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5503
MSP430F5503IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5503
MSP430F5503IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5503
MSP430F5503IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5503

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5504IPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5504
MSP430F5504IPT.B	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5504
MSP430F5504IPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5504
MSP430F5504IPTR.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5504
MSP430F5504IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5504
MSP430F5504IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5504
MSP430F5504IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5504
MSP430F5504IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5504
MSP430F5505IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5505
MSP430F5505IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5505
MSP430F5505IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5505
MSP430F5505IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5505
MSP430F5506IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5506
MSP430F5506IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5506
MSP430F5506IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5506
MSP430F5506IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5506
MSP430F5507IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5507
MSP430F5507IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5507

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5507IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5507
MSP430F5507IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5507
MSP430F5508IPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IPT.B	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IPTR.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5508
MSP430F5508IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5508
MSP430F5508IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5508
MSP430F5508IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5508
MSP430F5508IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5508
MSP430F5508IZXH	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5508
MSP430F5508IZXH.B	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5508
MSP430F5509IPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509
MSP430F5509IPT.B	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509
MSP430F5509IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509
MSP430F5509IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509
MSP430F5509IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509
MSP430F5509IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5509

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5509IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5509
MSP430F5509IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5509
MSP430F5509IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5509
MSP430F5509IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5509
MSP430F5509IZXH	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5509
MSP430F5509IZXH.B	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5509
MSP430F5509IZXHR	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5509
MSP430F5509IZXHR.B	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5509
MSP430F5510CY.B	Active	Production	DIESALE (Y) | 0	405 | NOT REQUIRED	Yes	Call TI	N/A for Pkg Type	0 to 70	
MSP430F5510IPT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IPT.B	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IPTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IPTR.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IPTRG4.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCTG4	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGCTG4.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5510
MSP430F5510IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510
MSP430F5510IRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510
MSP430F5510IRGZRG4	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F5510IRGZRG4.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510
MSP430F5510IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510
MSP430F5510IRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5510
MSP430F5510IZXH	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5510
MSP430F5510IZXH.B	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5510
MSP430F5510IZXHR	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5510
MSP430F5510IZXHR.B	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	F5510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

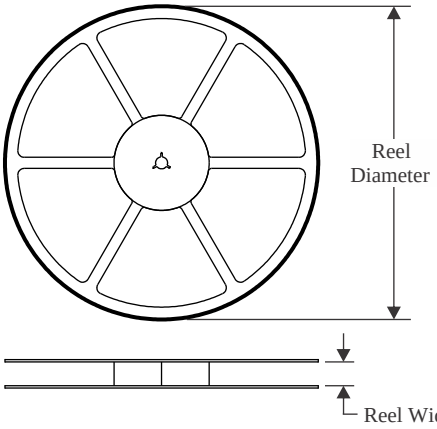
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

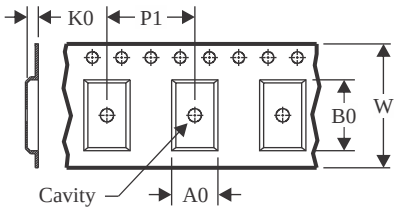
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

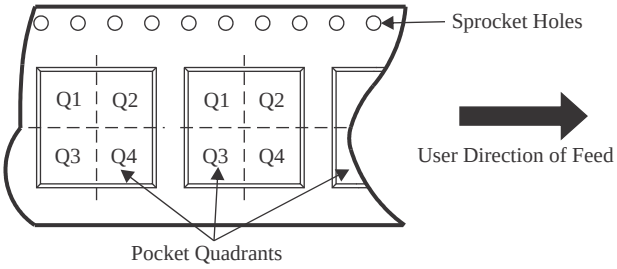


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

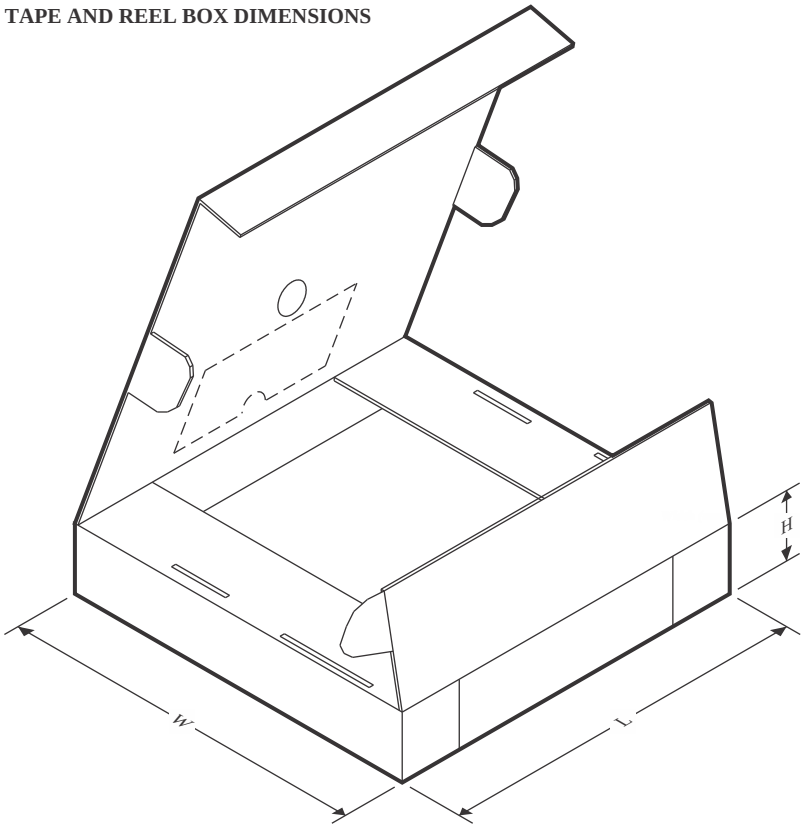


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5500IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5500IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5501IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5501IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5502IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5502IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5503IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5503IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5504IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5504IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5504IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5505IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5505IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5506IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5506IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5507IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5507IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5508IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5508IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5508IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5508IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5508IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5509IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5509IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5509IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5509IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5509IZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5510IPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430F5510IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5510IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5510IRGCTG4	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5510IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5510IRGZRG4	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5510IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F5510IZXHR	NFBGA	ZXH	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

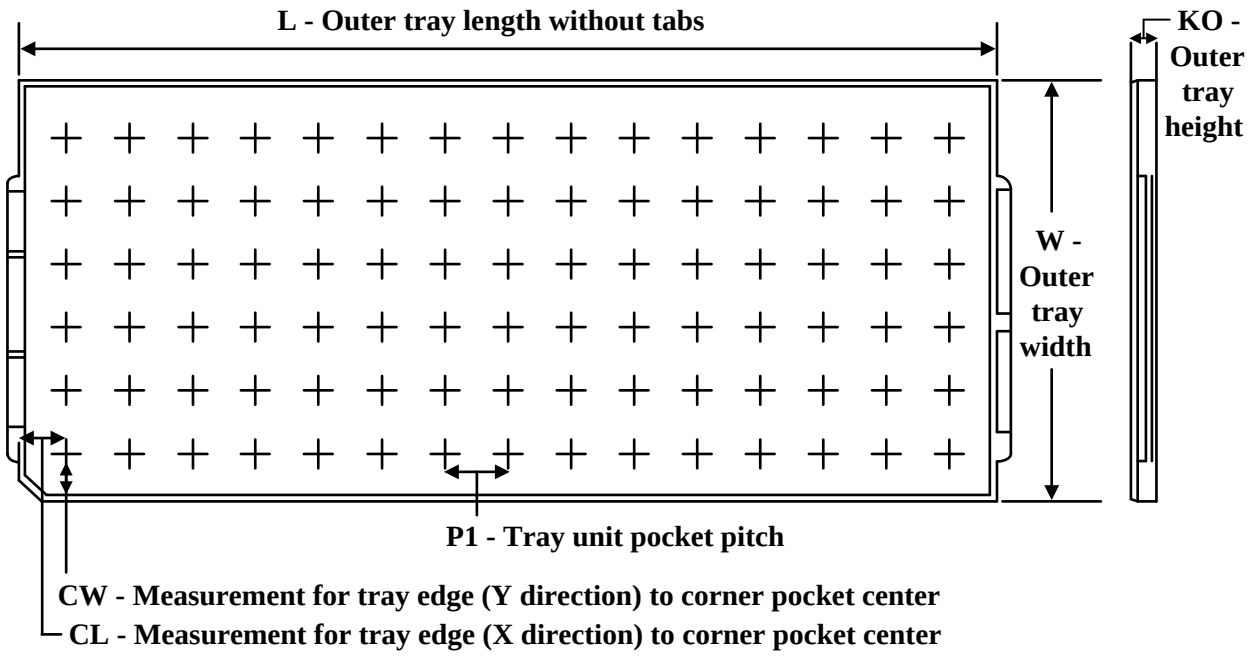


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5500IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5500IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5501IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5501IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5502IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5502IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5503IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5503IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5504IPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430F5504IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5504IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5505IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5505IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5506IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5506IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5507IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5507IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5508IPTR	LQFP	PT	48	1000	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5508IRGCR	VQFN	RGC	64	2000	356.0	356.0	35.0
MSP430F5508IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5508IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5508IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5509IRGCR	VQFN	RGC	64	2000	356.0	356.0	35.0
MSP430F5509IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5509IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5509IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5509IZXHR	NFBGA	ZXH	80	2500	350.0	350.0	43.0
MSP430F5510IPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430F5510IRGCR	VQFN	RGC	64	2000	356.0	356.0	35.0
MSP430F5510IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5510IRGCTG4	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5510IRGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5510IRGZRG4	VQFN	RGZ	48	2500	356.0	356.0	35.0
MSP430F5510IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5510IZXHR	NFBGA	ZXH	80	2500	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F5504IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5504IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5508IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5508IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5508IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5508IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5508IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5508IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5509IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5509IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IZXHR	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5509IZXHR.B	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IPT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F5510IPT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
MSP430F5510IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IZXH.B	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IZXHR	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
MSP430F5510IZXHR.B	ZXH	NFBGA	80	2500	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

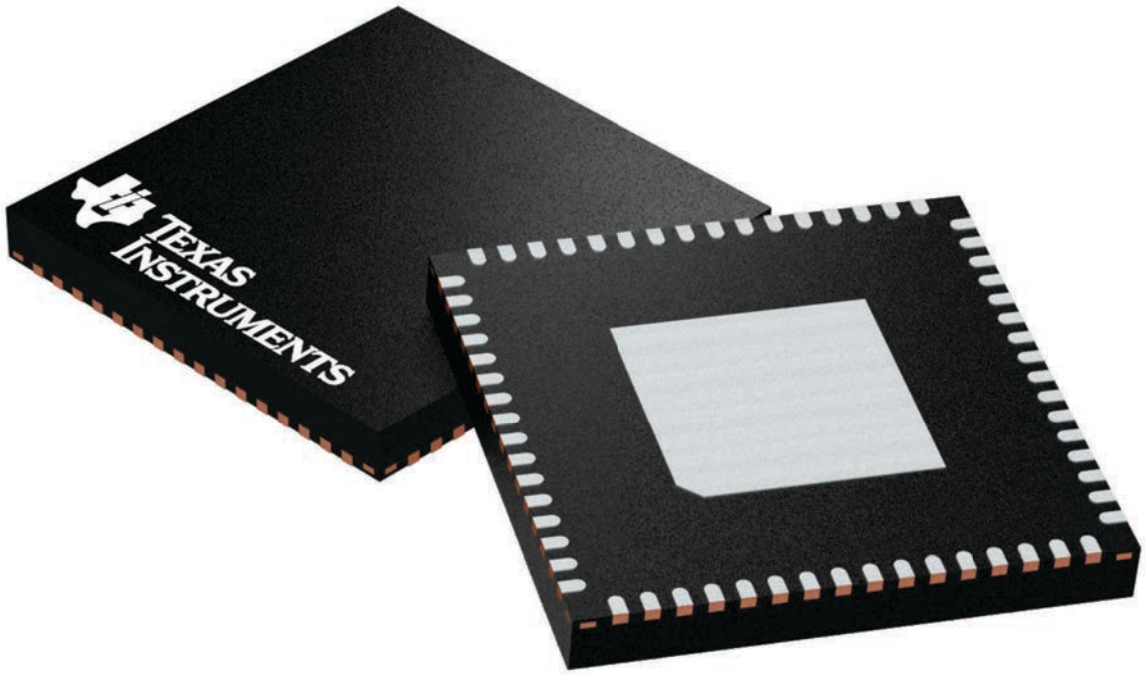
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

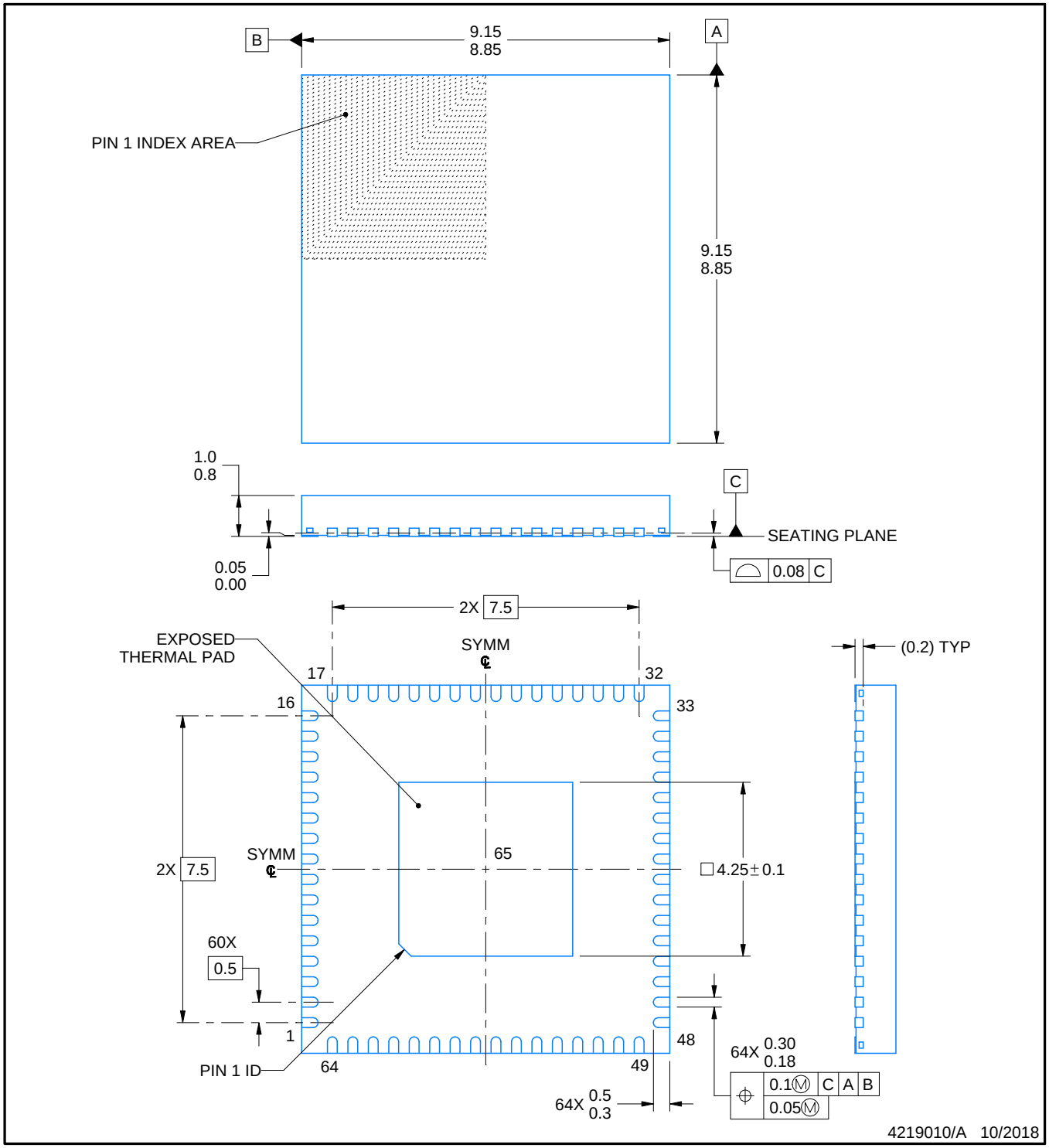
4224597/A

PACKAGE OUTLINE

RGC0064B

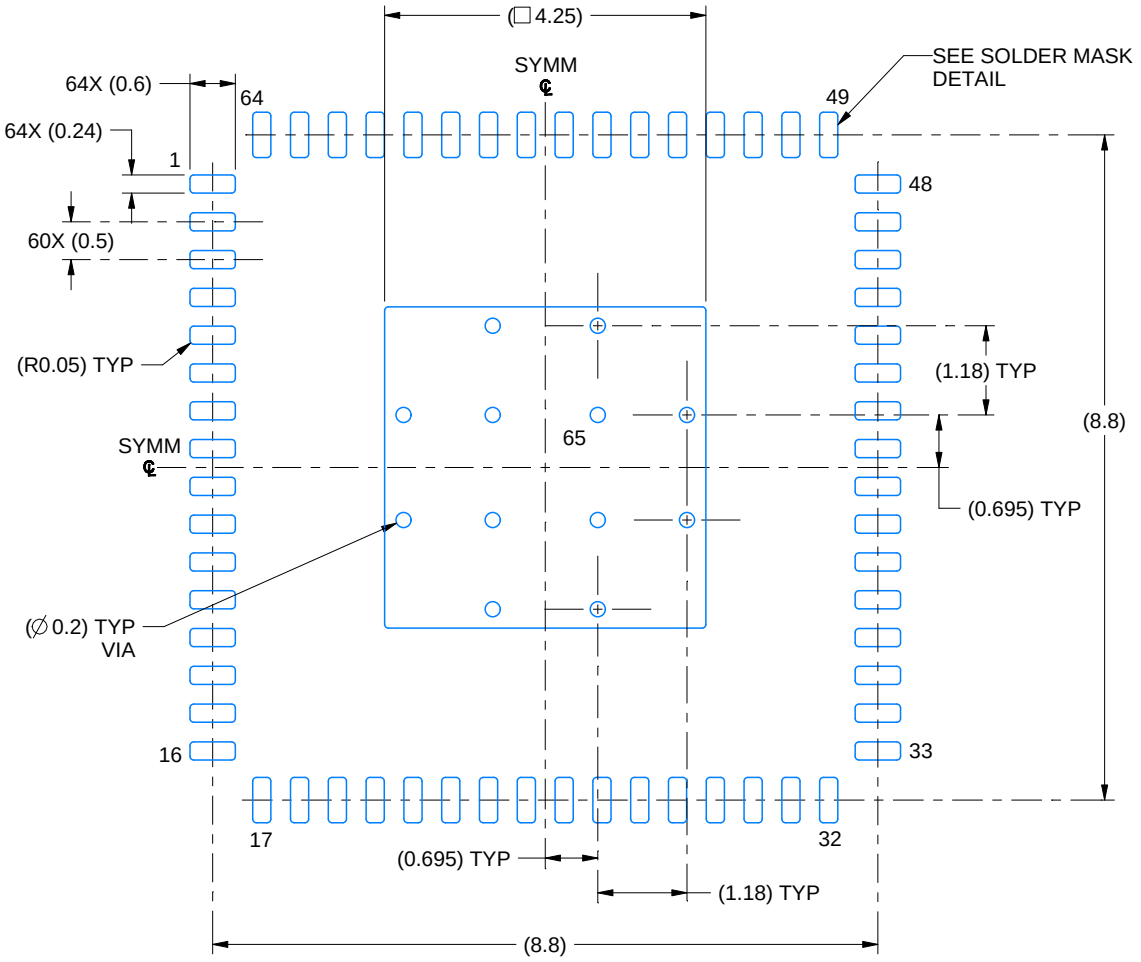
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

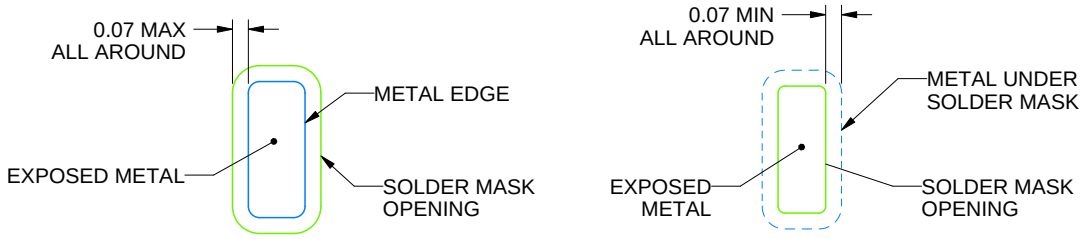


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

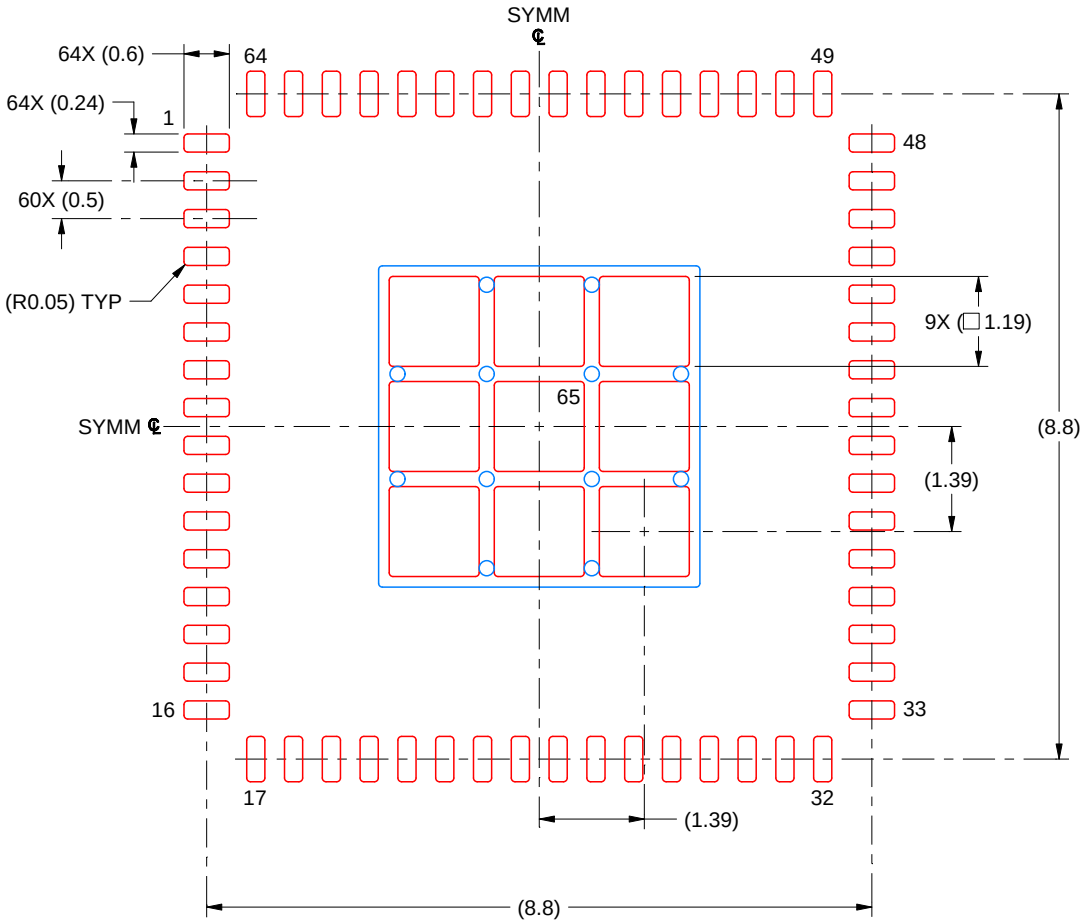
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

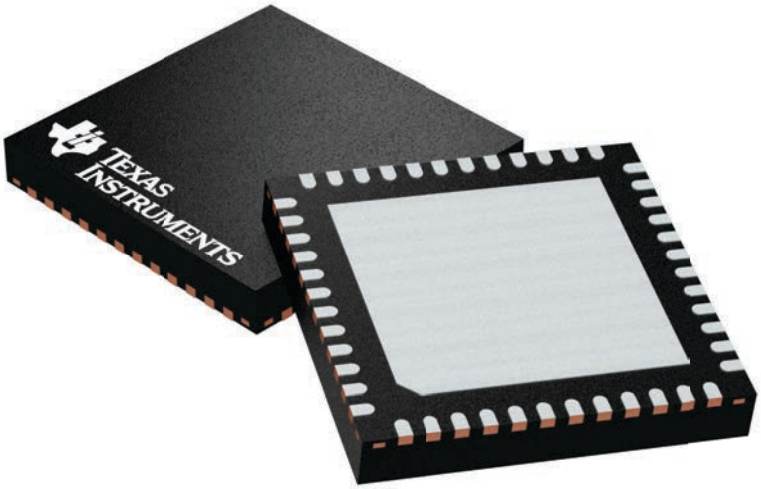
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

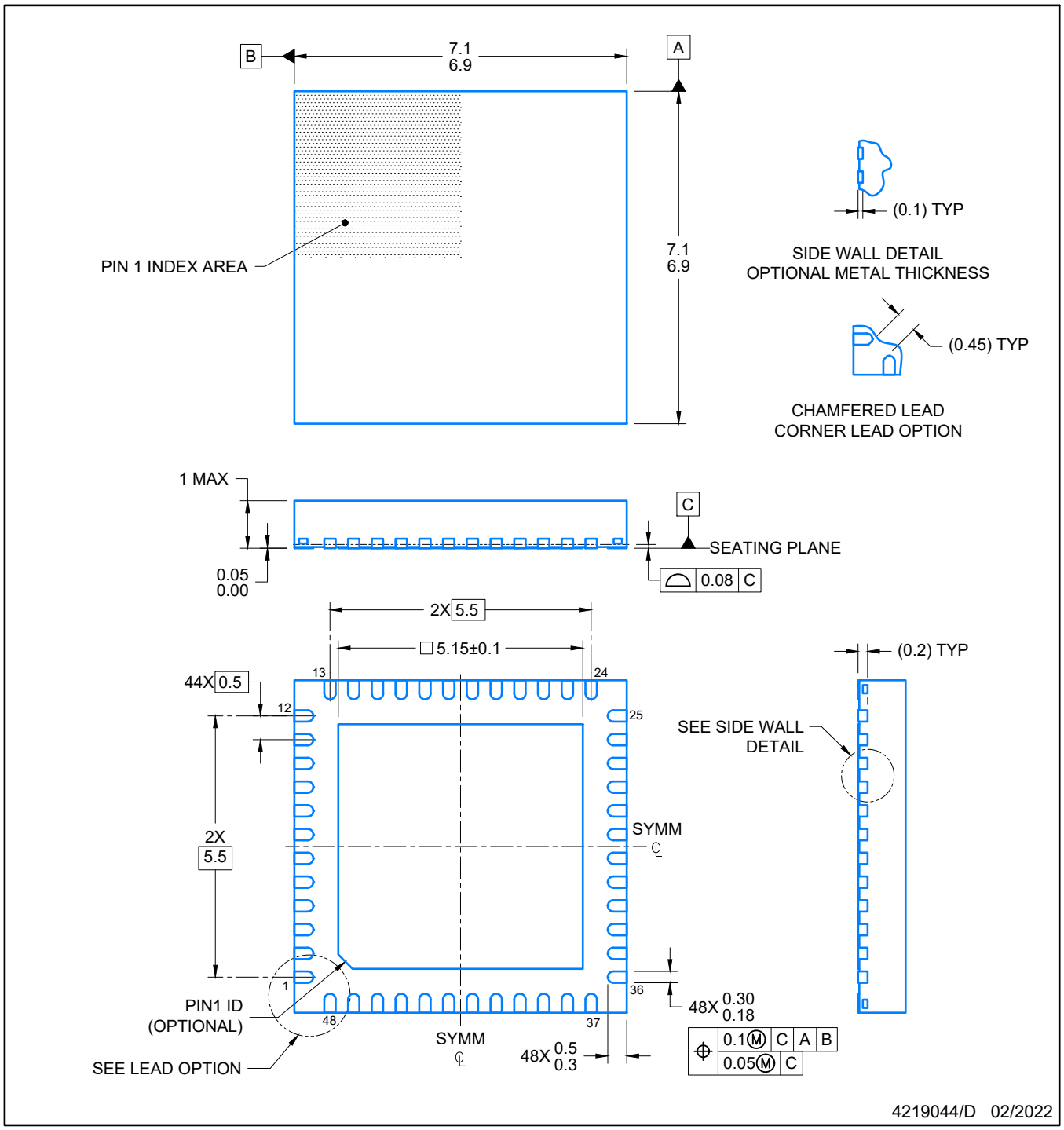
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



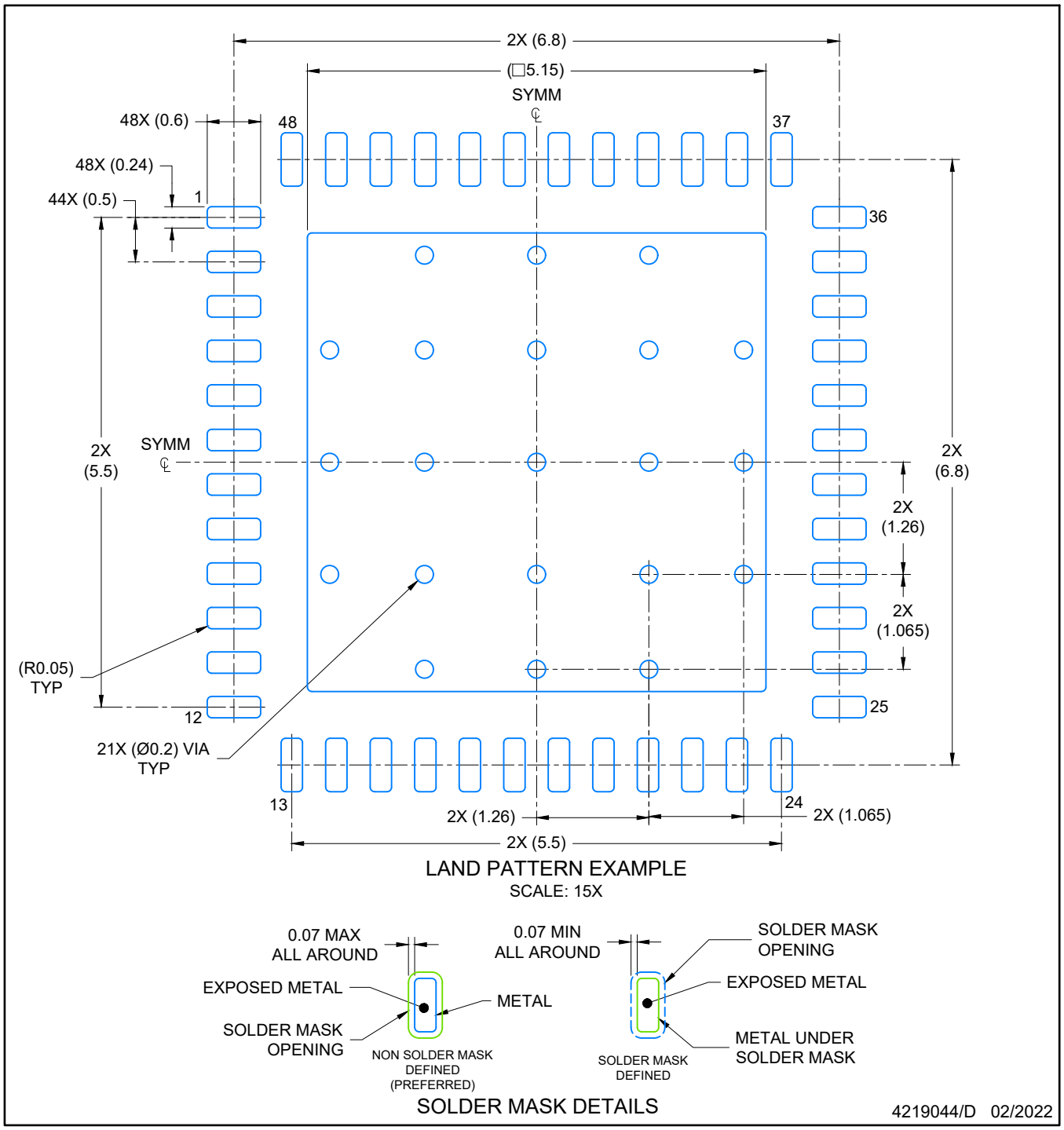
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



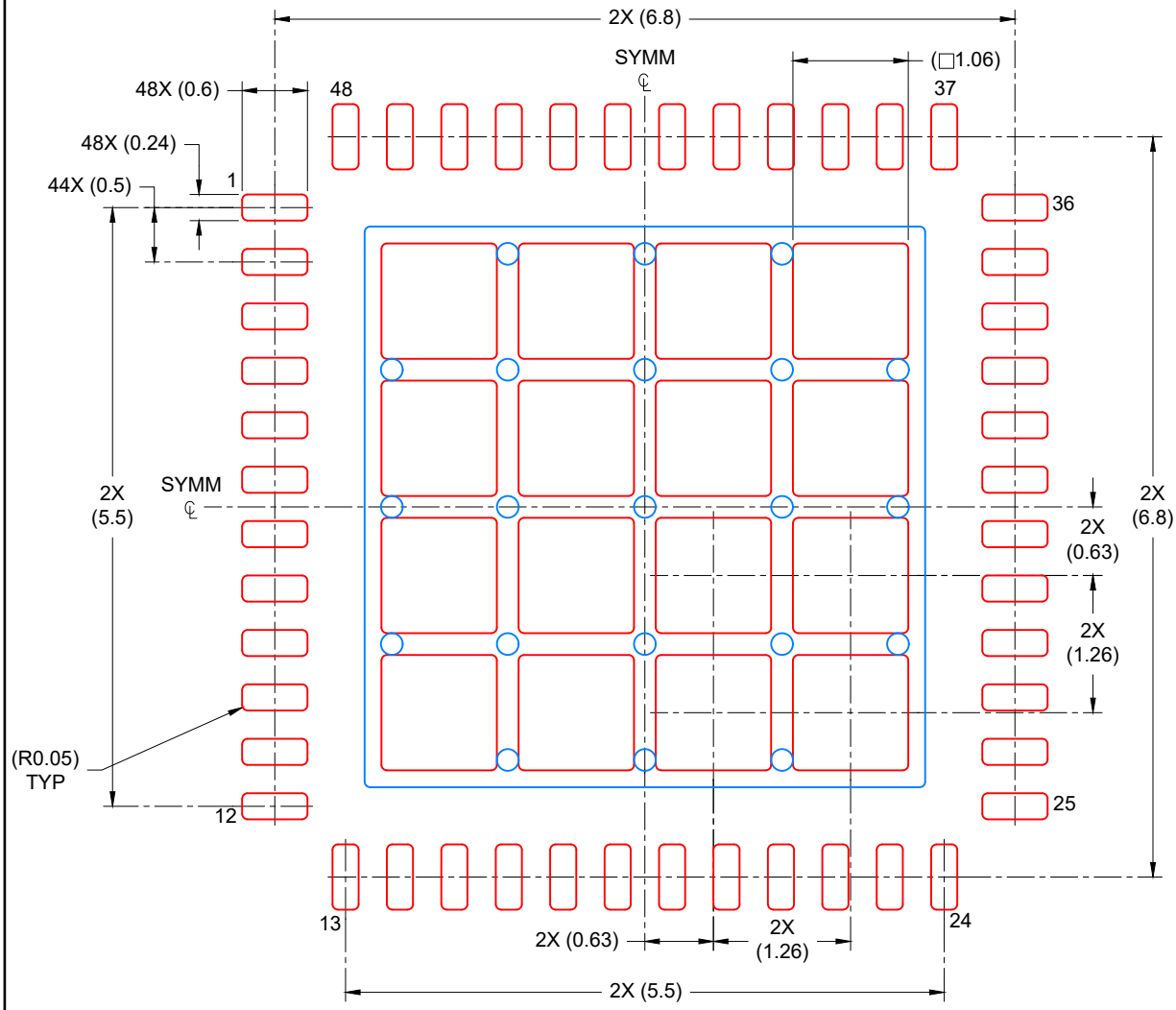
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



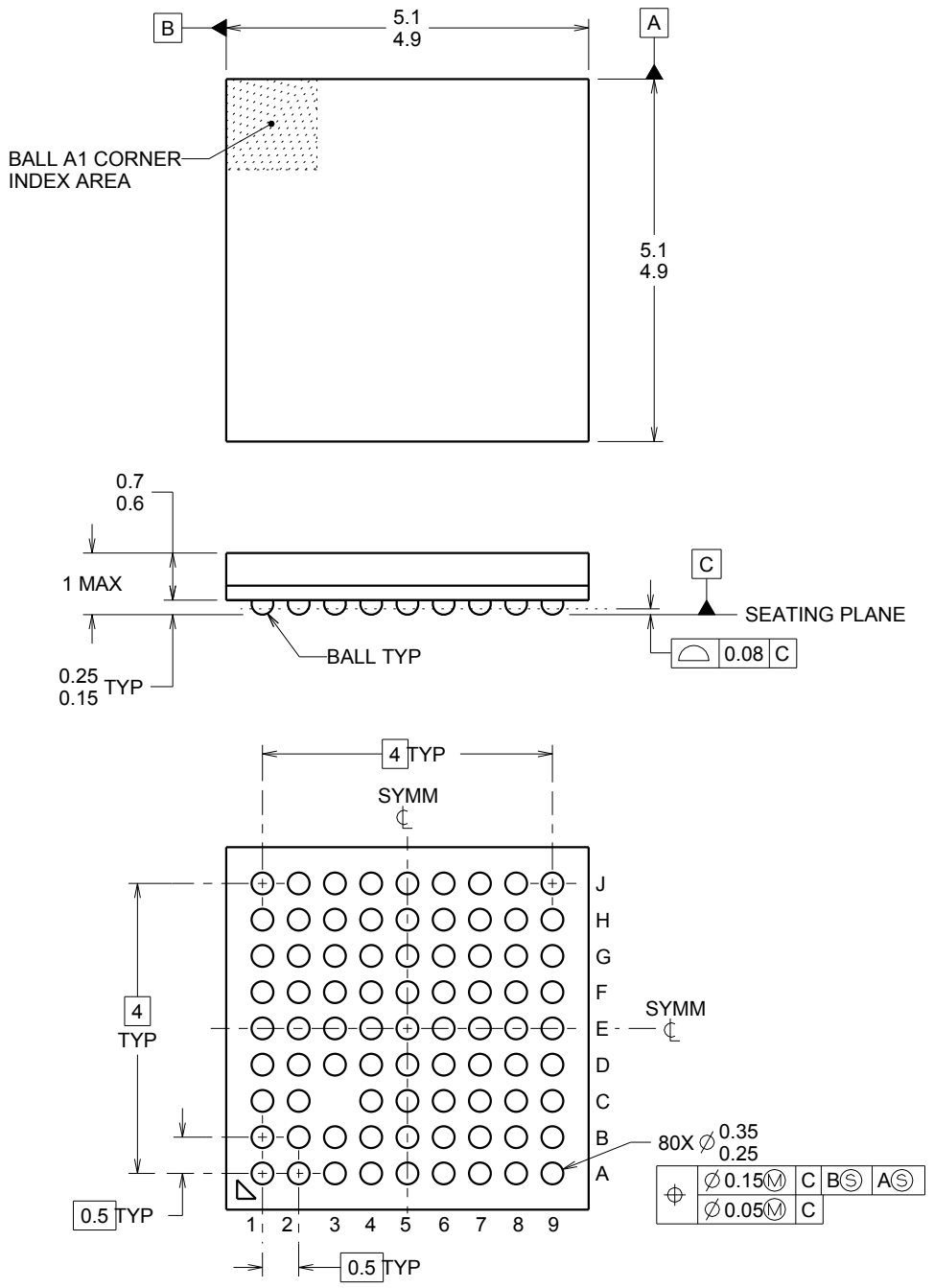
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

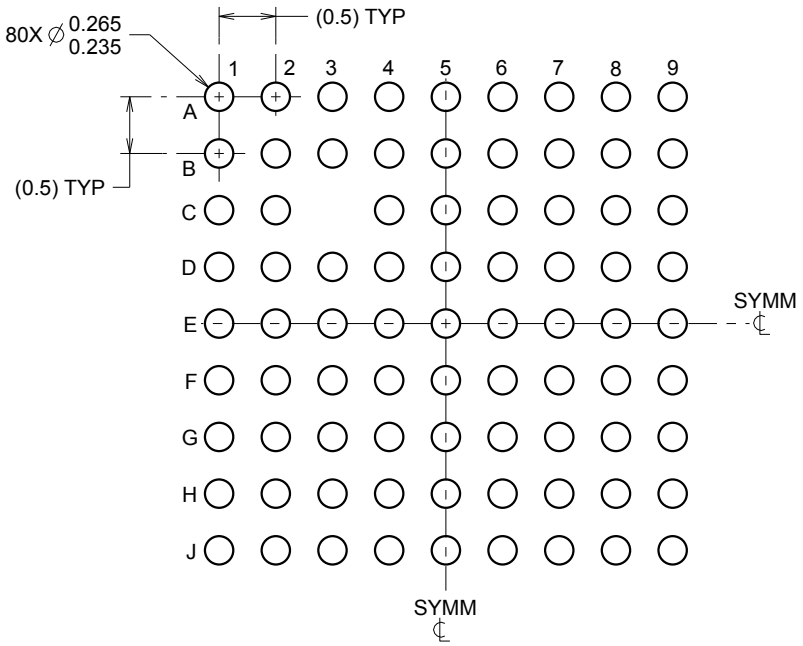
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

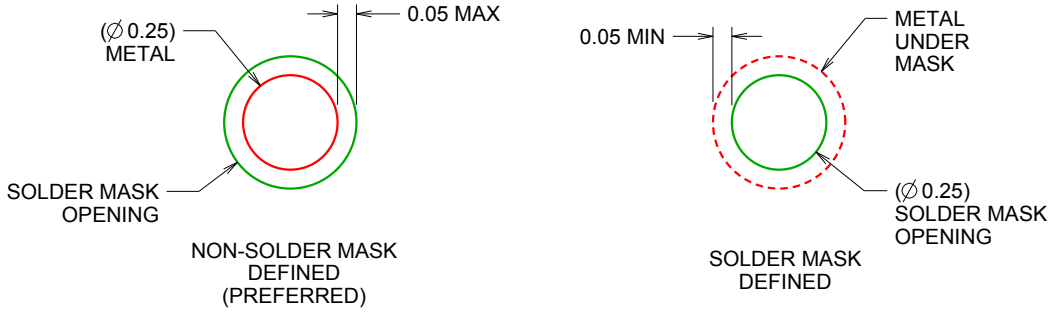


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
SCALE:15X

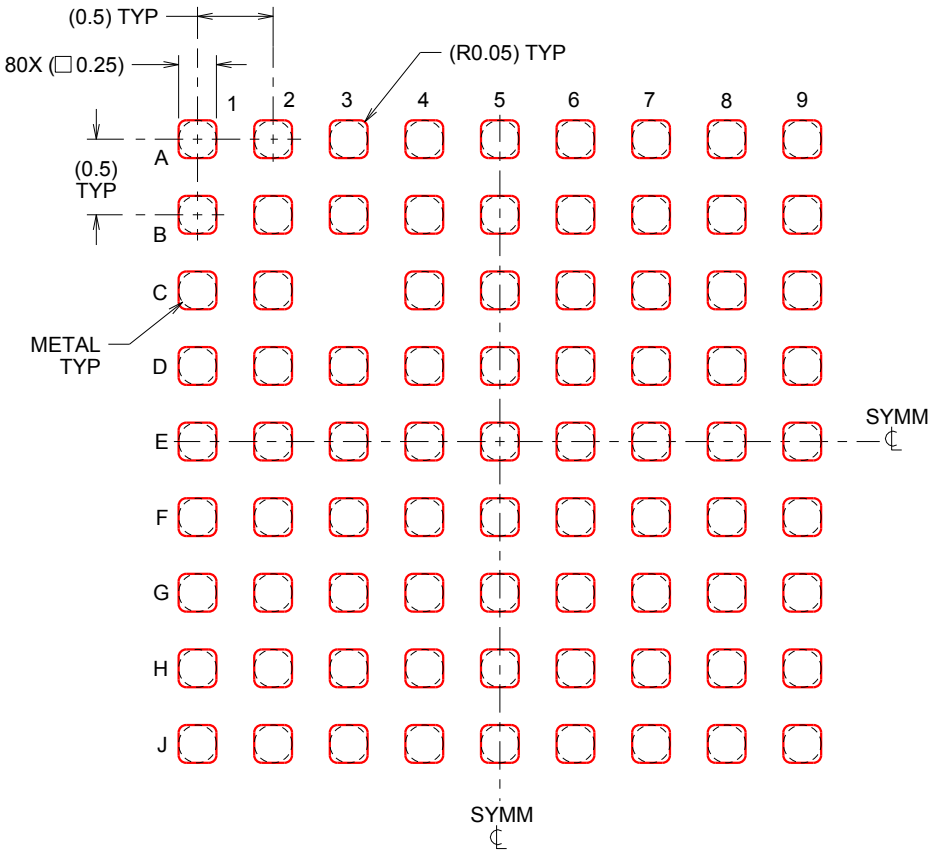


SOLDER MASK DETAILS
NOT TO SCALE

4221325/A 01/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).

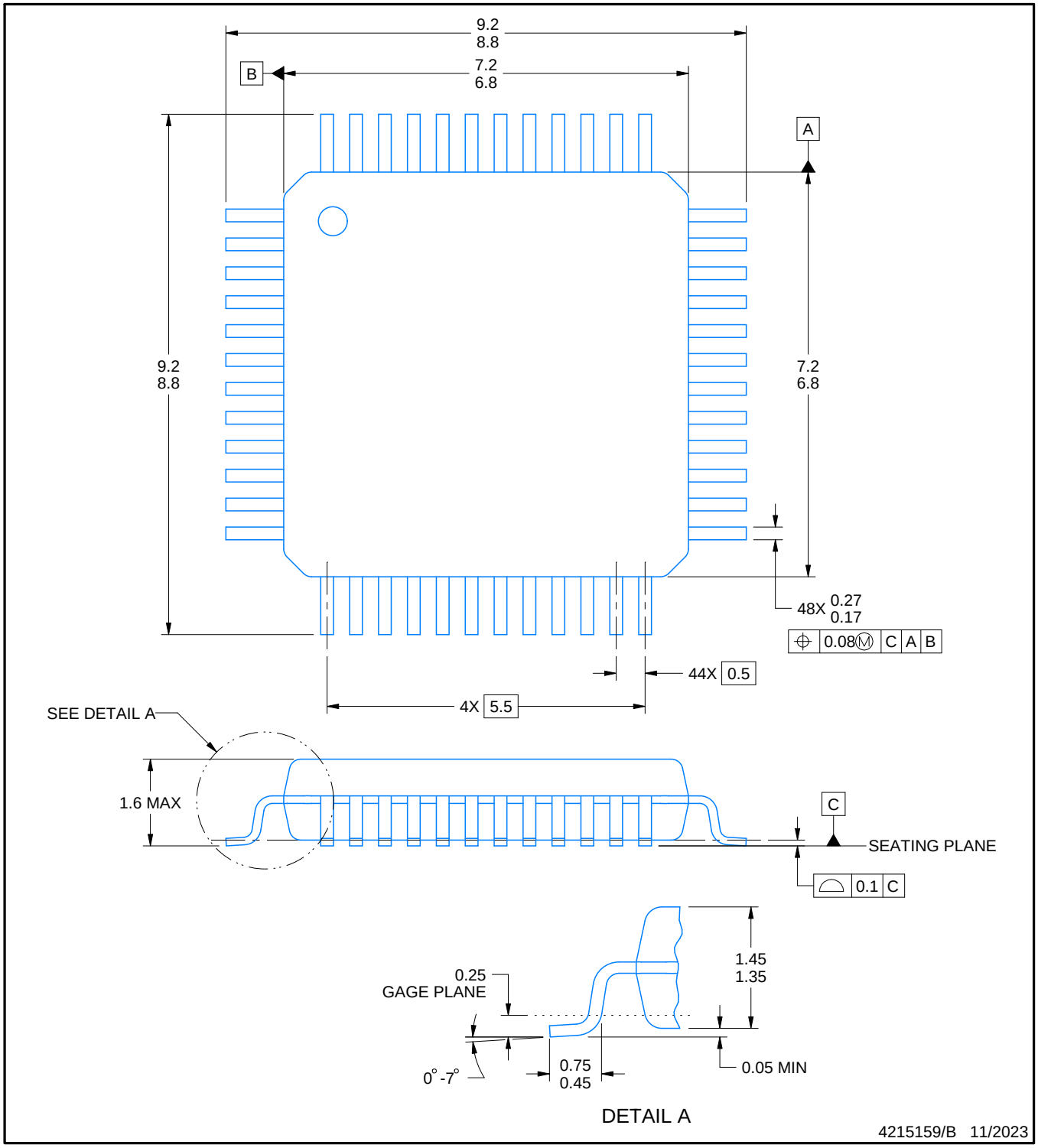


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

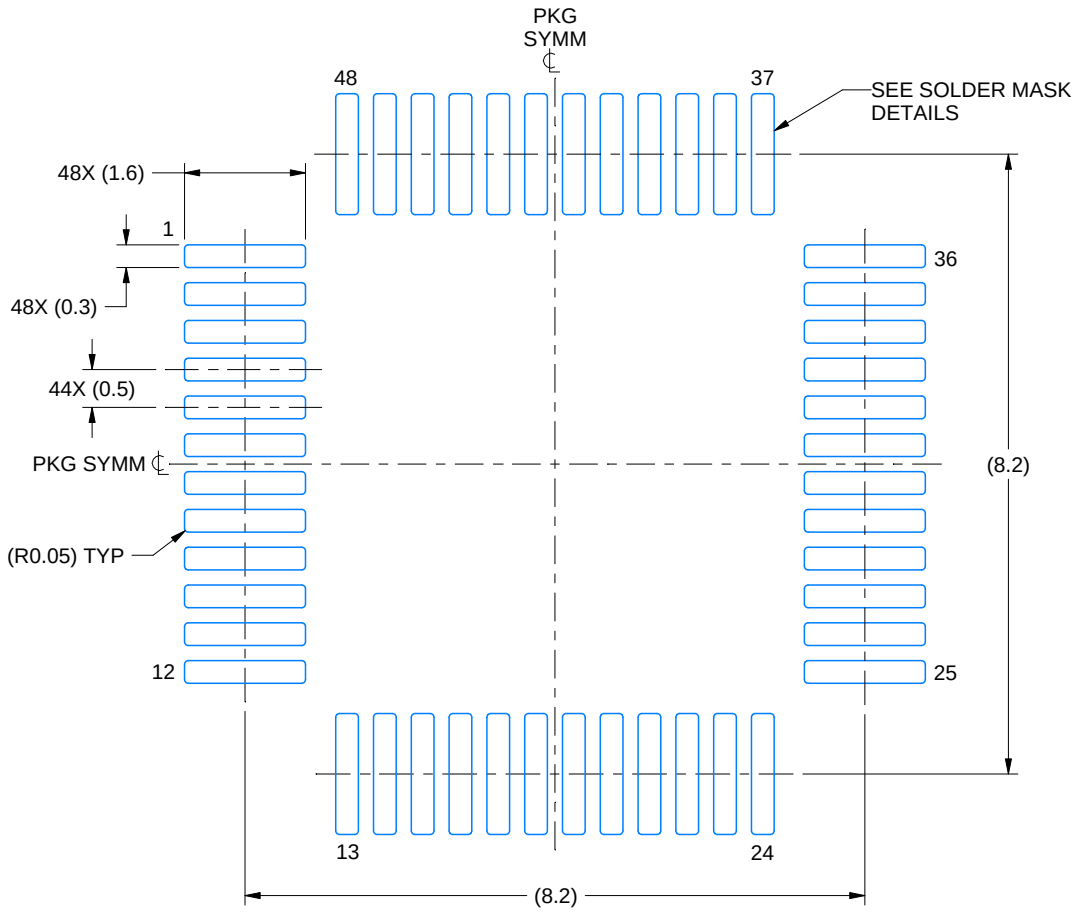
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

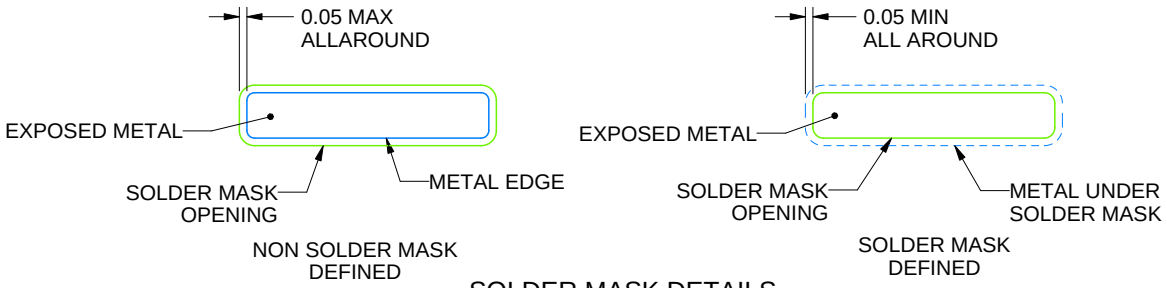


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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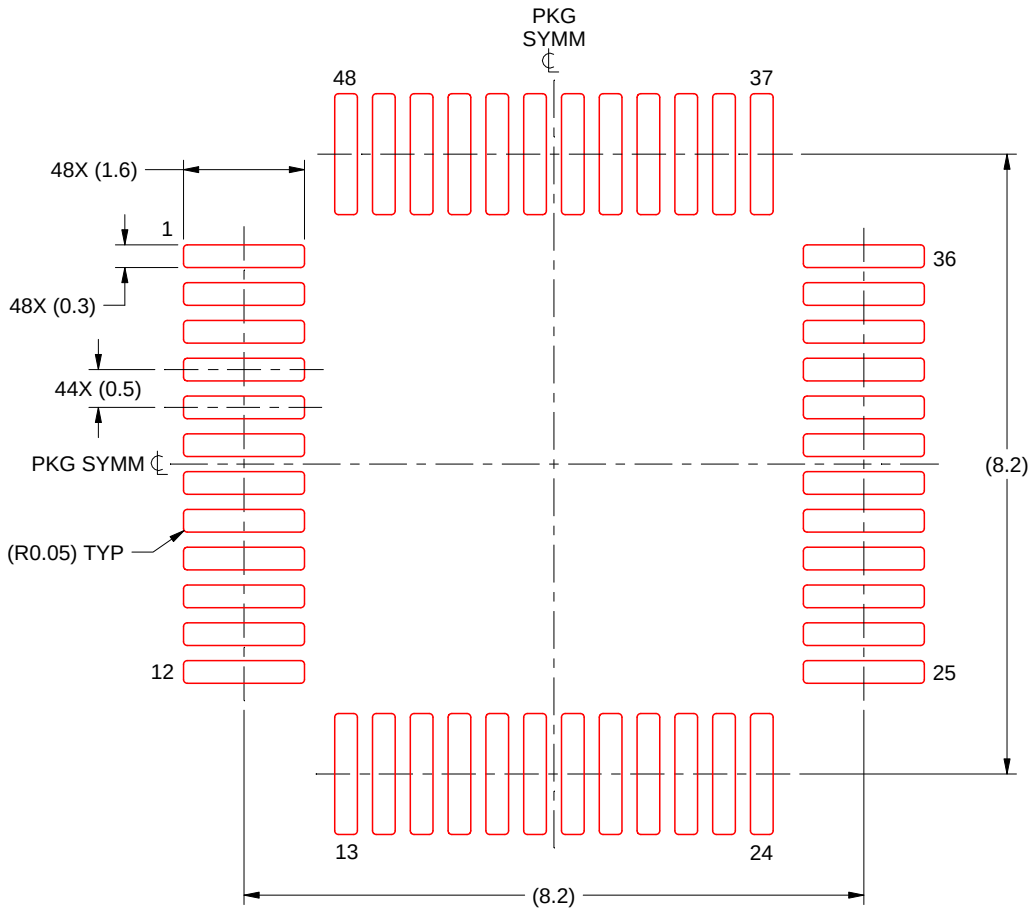
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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