# MSP430F563x ミクスト・シグナル・マイクロコントローラ

## 1 特長

- 低い電源電圧範囲:1.8V～3.6V
- 超低消費電力
  - アクティブ・モード (AM):
    すべてのシステム・クロックがアクティブ:
    270µA/MHz (8MHz、3.0V)、フラッシュ・プログラム実行時 (標準値)
  - スタンバイ・モード(LPM3):
    ウォッチドッグ (水晶振動子を使用)、電源スーパーバイザが動作、すべての RAM を保持、高速ウェークアップ:
    1.8µA (2.2V)、2.1µA (3.0V) (標準値)
  - シャットダウン・リアルタイム・クロック( RTC )モード (LPM3.5) :
    シャットダウン・モード、RTC (水晶振動子を使用) が動作:
    1.1µA (3.0V) (標準値)
  - シャットダウン・モード (LPM4.5):
    0.3µA (3.0V) (標準値)
- スタンバイ・モードから 3µs (標準値) でウェークアップ
- 16 ビット RISC アーキテクチャ、拡張メモリ、最大 20MHz のシステム・クロック
- 柔軟な電力管理システム
  - プログラム可能な、レギュレートされたコア電源電圧を持つ、完全に統合された LDO
  - 電源電圧の管理、監視、およびブラウンアウト
- 統合クロック・システム
  - FLL 制御ループによる周波数安定化
  - 低電力、低周波数の内部クロック・ソース (VLO)
  - 調整済みの低周波数内部基準源 (REFO)
  - 32kHz の水晶振動子 (XT1)
  - 最高 32MHz の高周波数水晶振動子( XT2)
- 4 個の 16 ビット・タイマと 3、5、または 7 個のキャプチャ/ 比較レジスタ
- 2 つのユニバーサル・シリアル通信インターフェイス (USCI)
  - USCI_A0、USCI_A1 がそれぞれ次の機能をサポート:
    - 自動ボーレート検出機能付きの拡張 UART
    - IrDA エンコーダおよびデコーダ
    - 同期 SPI
  - USCI_B0、USCI_B1 がそれぞれ次の機能をサポート:
    - $I^2C$
    - 同期 SPI
- フルスピード・ユニバーサル・シリアル・バス(USB)
  - USB-PHY 内蔵
  - 3.3V/1.8V USB 電源システム内蔵
  - USB-PLL 内蔵
  - 8 入力 / 8 出力のエンドポイント
- 共有基準電圧、サンプル・アンド・ホールド、自動スキャン機能を内蔵した 12 ビット A/D コンバータ(ADC)
- 同期機能付きの 2 つの 12 ビット D/A コンバータ (DAC)
- 電圧コンパレータ
- ハードウェア乗算器で 32 ビットの演算をサポート
- シリアルのオンボード・プログラミング、外部のプログラミング電圧不要
- 6 チャネルの内蔵 DMA
- 電源電圧バックアップ・スイッチ付きの RTC モジュール
- 「デバイスの比較」に、提供しているファミリ製品をまとめています。

## 2 アプリケーション

- アナログおよびデジタル・センサ・システム
- デジタル・モーター制御
- リモート・コントロール
- サーモスタット
- デジタル・タイマ
- ハンドヘルド・メータ

## 3 概要

TI MSP 430™ ファミリの超低消費電力マイクロコントローラは複数のデバイスで構成され、それぞれが各種のアプリケーションを対象とする異なるペリフェラルを搭載しています。このアーキテクチャは 5 つの低消費電力モードを持ち、携帯用測定器用途でバッテリ駆動時間を延長するよう最適化されています。このデバイスには、強力な 16 ビット RISC CPU、16 ビット・レジスタ、および定数ジェネレータが搭載されており、コード効率が最大限に発揮されます。デジタル制御発振器 (DCO) により、低消費電力モードからアクティブ・モードへ 3µs (標準値) でウェークアップできます。

MSP430F563x は、高性能 12 ビット ADC、コンパレータ、2 つの USCI、USB 2.0、ハードウェア乗算器、DMA、4 つの 16 ビット・タイマ、アラーム機能付き RTC モジュール、最大 74 本の I/O ピンを搭載したマイクロコントローラです。

モジュールの完全な説明については、『MSP430F5xx および MSP430F6xx ファミリ・ユーザー・ガイド』を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

## 製品情報

| 部品番号(1) | パッケージ | 本体サイズ(2) |
|---|---|---|
| MSP430F5638IPZ | LQFP (100) | 14mm × 14mm |
| MSP430F5638IZCA | nFBGA (113) | 7mm × 7mm |
| MSP430F5638IZQW(3) | MicroStar Junior™ BGA (113) | 7mm × 7mm |

(1) 最新のデバイス、パッケージ、および注文情報については、セクション 11 の「*付録: パッケージ・オプション*」または、www.tij.co.jp の TI Web サイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、セクション 11 の「*メカニカル・データ*」を参照してください。
(3) ZQW (MicroStar Junior BGA) パッケージのすべての注文可能な部品番号が「最終購入」のステータスに変更されました。このステータスの詳細については、製品ライフサイクルのページを参照してください。


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# 4 機能ブロック図

図 4-1 に MSP430F5638、MSP430F5637、MSP430F5636 の機能ブロック図を示します。

**図 4-1. 機能ブロック図 – MSP430F5638、MSP430F5637、MSP430F5636**

図 4-2 に MSP430F5635、MSP430F5634、MSP430F5633 の機能ブロック図を示します。

**図 4-2. 機能ブロック図 – MSP430F5635、MSP430F5634、MSP430F5633**

図 4-3 に MSP430F5632、MSP430F5631、MSP430F5630 の機能ブロック図を示します。

**図 4-3. 機能ブロック図 – MSP430F5632、MSP430F5631、MSP430F5630**


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## 5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from revision F to revision G

| Changes from September 18, 2018 to September 10, 2020 | Page |
|---|---|
| • 文書全体にわたってセクション、表、図、相互参照の採番方法を更新 | 1 |
| • 文書全体にわたって nFBGA パッケージ (ZCA) の情報を追加 | 1 |
| • Removed package options that are no longer available in 表 6-1, *Device Comparison* (MSP430F5637 and MSP430F5631 in ZQW) | 8 |
| • Updated the list of devices available in the 113-Pin ZQW package in the caption of 図 7-4 | 9 |
| • Changed the MAX value of the $I_{ERASE}$ and $I_{MERASE}$, $I_{BANK}$ parameters in セクション 8.54, *Flash Memory* | 53 |
| • Corrected the connection of the P7SEL.x signal in 図 9-11, *Port P7 (P7.4 to P7.7) Diagram* | 97 |

Changes from revision E to revision F

| Changes from December 9, 2015 to September 17, 2018 | Page |
|---|---|
| • Added セクション 6.1, *Related Products* | 8 |
| • Added typical conditions statements at the beginning of セクション 8, *Specifications* | 18 |
| • Changed the MIN value of the $V_{(DVCC_BOR_hys)}$ parameter from 60 mV to 50 mV in セクション 8.20, *PMM, Brownout Reset (BOR)* | 30 |
| • Updated notes (1) and (2) and added note (3) in セクション 8.26, *Wake-up Times From Low-Power Modes and Reset* | 32 |
| • Removed ADC12DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in セクション 8.35, *12-Bit ADC, Timing Parameters*, because ADC12CLK is after division | 40 |
| • Removed the note that started "This impedance depends on..." from the "Reference input resistance" parameter in セクション 8.45, *12-Bit DAC, Reference Input Specifications* | 48 |
| • Added second row for $t_{EN_CMP}$ with Test Conditions of "CBPWRMD = 10" and MAX value of 100 µs in セクション 8.48, *Comparator_B* | 50 |
| • Renamed FCTL4.MGR0 and MGR1 in the $f_{MCLK,MGR}$ parameter in セクション 8.54, *Flash Memory* to be consistent with header files | 53 |
| • Replaced former section *Development Tools Support* with セクション 10.3, *Tools and Software* | 107 |

Changes from revision D to revision E

| Changes from August 6, 2013 to December 8, 2015 | Page |
|---|---|
| • 全体を通してドキュメントのフォーマットと編成を変更、セクションの番号追加も含む | 1 |
| • すべての機能ブロック図をセクション 4「*機能ブロック図*」に移動 | 3 |
| • Added USB column to 表 6-1, *Family Members* | 8 |
| • Added セクション 6, *Device Comparison*, and moved 表 6-1 to it | 8 |
| • Added "Port U is supplied by the LDOO rail" to the PU.0 and PU.1 descriptions in セクション 7.2, *Signal Descriptions* | 13 |
| • Added セクション 8.2, *ESD Ratings* | 18 |
| • Added note to $C_{VCORE}$ | 18 |
| • Added note to $R_{Pull}$ | 22 |
| • Changed TYP value of $C_{L,eff}$ with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF | 26 |
| • In $V_{BAT3}$ parameter description, changed from "$V_{BAT3} \neq V_{BAT}/3$" to "$V_{BAT3} = V_{BAT}/3$" | 34 |
| • Changed from $f_{DAC12_0OUT}$ to $f_{DAC12_1OUT}$ in the first row of the Test Conditions for the "Channel-to-channel crosstalk" parameter | 49 |
| • Changed the value of DAC12_xDAT from 7F7h to F7Fh and changed the x-axis label from $f_{Toggle}$ to $1/f_{Toggle}$ in 図 8-22, *Crosstalk Test Conditions* | 49 |
| • Added note to $R_{PUR}$ | 52 |


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- Corrected the spelling of the MRG bits in the $f_{MCLK,MRG}$ parameter in セクション 8.54, *Flash Memory* ..... 53
- Removed RTC_B from LPM4.5 wake-up options..... 56
- Throughout document, changed all instances of "bootstrap loader" to "bootloader" ..... 59
- Added the paragraph that starts "*Using the MSP430 RTC_B Module With Battery Backup Supply* describes how..." ..... 63
- Corrected names of interrupt events PMMSWBOR (BOR) and PMMSWPOR (POR) in 表 9-11, *System Module Interrupt Vector Registers* ..... 64
- Corrected spelling of NMIIFG (added missing "I") in 表 9-11, *System Module Interrupt Vector Registers* ..... 64
- Corrected register acronyms (added "USB" prefix as required) in 表 9-50, *USB Control Registers* ..... 71
- Added P7SEL.2 and XT2BYPASS inputs with AND and OR gates in 図 9-10, *Port P7 (P7.3) Diagram* .....96
- Changed P7SEL.3 column from X to 0 for "P7.3 (I/O)" rows..... 96
- Added セクション 10 and moved *Development Tools Support*, *Device and Development Tool Nomenclature*, *Trademarks*, and *Electrostatic Discharge Caution* sections to it.....105
- Added セクション 11, *Mechanical, Packaging, and Orderable Information* ..... 112

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The following table lists the changes to this data sheet from the original release through revision D.

| REVISION | COMMENTS |
|---|---|
| SLAS650D<br>August 2013 | Signal Descriptions, Added note regarding pullup resistor to $\overline{RST}$/NMI/SBWTDIO pin.<br>Added Applications, Development Tools Support, and Device and Development Tool Nomenclature<br>セクション 9.12.1, Changed the description of the number of I/Os in each port.<br>表 9-19, Added PM5CTL0 register.<br>セクション 8.42, Fixed typo in $I_{DD}$ Test Conditions (changed from DAC12IOG to DAC12OG).<br>セクション 8.51, Corrected $V_{IL}$ and $V_{IH}$ limits.<br>セクション 8.54, Changed $I_{ERASE}$ and $I_{MERASE}$, $I_{BANK}$ limits. |
| SLAS650C<br>August 2012 | Changed description of ACLK and PUR in Signal Descriptions.<br>Changed typos to Interrupt Flag names on Timer TA2 rows in 表 9-3.<br>Changed SYSRSTIV, System Reset offset 1Ch to Reserved in 表 9-11.<br>Corrected names of SVMLVLRIFG and SVMHVLRIFG bits in 表 9-11.<br>Corrected right-most column in 表 9-4.<br>Added note regarding evaluation of PUR in セクション 9.7.1.<br>Changed notes on セクション 8.41.<br>Changed $t_{SENSOR(sample)}$ MIN to 100 µs in セクション 8.39.<br>Changed note (2) in セクション 8.39.<br>Editorial changes throughout. |
| SLAS650B<br>August 2011 | Production Data release |
| SLAS650A<br>July 2010 | Updated Product Preview including electrical specifications |
| SLAS650<br>May 2010 | Product Preview release |

# 6 Device Comparison

表 6-1 summarizes the available family members.

**表 6-1. Device Comparison**

| DEVICE(1) (2) | FLASH (KB) | SRAM (KB)(5) | Timer_A(3) | Timer_B(4) | USCI_A: UART, IrDA, SPI | USCI_B: SPI, I²C | ADC12_A (Ch) | DAC12_A (Ch) | Comp_B (Ch) | USB | I/O | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F5638 | 256 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | 2 | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5637 | 192 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | 2 | 12 | Yes | 74 | 100 PZ |
| MSP430F5636 | 128 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | 2 | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5635 | 256 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | – | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5634 | 192 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | – | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5633 | 128 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | 12 ext, 4 int | – | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5632 | 256 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | – | – | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5631 | 192 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | – | – | 12 | Yes | 74 | 100 PZ |
| MSP430F5630 | 128 | 16 + 2 | 5, 3, 3 | 7 | 2 | 2 | – | – | 12 | Yes | 74 | 100 PZ, 113 ZCA, 113 ZQW |

(1) For the most current package and ordering information, see the *Package Option Addendum* in セクション 11, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(5) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.

## 6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement MCUs

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430F5638

Review products that are frequently purchased or used in conjunction with this product.

Reference designs

Find reference designs leveraging the best in TI technology to solve your system-level challenges


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# 7 Terminal Configuration and Functions

## 7.1 Pin Diagrams

図 7-1 shows the pinout for the MSP430F5638, MSP430F5637, and MSP430F5636 devices in the 100-pin PZ package.

NOTE: DNC = Do not connect

**図 7-1. 100-Pin PZ Package (Top View) – MSP430F5638, MSP430F5637, MSP430F5636**

図 7-2 shows the pinout for the MSP430F5635, MSP430F5634, and MSP430F5633 devices in the 100-pin PZ package.

NOTE: DNC = Do not connect

**図 7-2. 100-Pin PZ Package (Top View) – MSP430F5635, MSP430F5634, MSP430F5633**


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図 7-3 shows the pinout for the MSP430F5632, MSP430F5631, and MSP430F5630 devices in the 100-pin PZ package.

NOTE: DNC = Do not connect

**図 7-3. 100-Pin PZ Package (Top View) – MSP430F5632, MSP430F5631, MSP430F5630**

図 7-4 shows the pinout for all devices in the 113-pin ZCA or ZQW package. See 表 7-1 for pin assignments and descriptions.

NOTE: For terminal assignments, see 表 7-1.

**図 7-4. 113-Pin ZCA or ZQW Package (Top View) – MSP430F5638, MSP430F5636, MSP430F5635, MSP430F5634, MSP430F5633, MSP430F5632, MSP430F5630**


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## 7.2 Signal Descriptions

表 7-1 describes the signals for all device variants and packages.

**表 7-1. Signal Descriptions**

| TERMINAL | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO.[4] | | | |
| | PZ | ZCA, ZQW | | |
| P6.4/CB4/A4 | 1 | A1 | I/O | General-purpose digital I/O<br>Comparator_B input CB4<br>Analog input A4 – ADC (not available on F5632, F5631, and F5630 devices) |
| P6.5/CB5/A5 | 2 | B2 | I/O | General-purpose digital I/O<br>Comparator_B input CB5<br>Analog input A5 – ADC (not available on F5632, F5631, and F5630 devices) |
| P6.6/CB6/A6/DAC0 | 3 | B1 | I/O | General-purpose digital I/O<br>Comparator_B input CB6<br>Analog input A6 – ADC (not available on F5632, F5631, and F5630 devices)<br>DAC12.0 output (not available on F5635, F5634, F5633, F5632, F5631, and F5630 devices) |
| P6.7/CB7/A7/DAC1 | 4 | C2 | I/O | General-purpose digital I/O<br>Comparator_B input CB7<br>Analog input A7 – ADC (not available on F5632, F5631, and F5630 devices)<br>DAC12.1 output (not available on F5635, F5634, F5633, F5632, F5631, and F5630 devices) |
| P7.4/CB8/A12 | 5 | C1 | I/O | General-purpose digital I/O<br>Comparator_B input CB8<br>Analog input A12 –ADC (not available on F5632, F5631, and F5630 devices) |
| P7.5/CB9/A13 | 6 | C3 | I/O | General-purpose digital I/O<br>Comparator_B input CB9<br>Analog input A13 – ADC (not available on F5632, F5631, and F5630 devices) |
| P7.6/CB10/A14/DAC0 | 7 | D2 | I/O | General-purpose digital I/O<br>Comparator_B input CB10<br>Analog input A14 – ADC (not available on F5632, F5631, and F5630 devices)<br>DAC12.0 output (not available on F5635, F5634, F5633, F5632, F5631, and F5630 devices) |
| P7.7/CB11/A15/DAC1 | 8 | D1 | I/O | General-purpose digital I/O<br>Comparator_B input CB11<br>Analog input A15 – ADC (not available on F5632, F5631, and F5630 devices)<br>DAC12.1 output (not available on F5635, F5634, F5633, F5632, F5631, and F5630 devices) |
| P5.0/VREF+/VeREF+ | 9 | D4 | I/O | General-purpose digital I/O<br>Output of reference voltage to the ADC<br>Input for an external reference voltage to the ADC |
| P5.1/VREF-/VeREF- | 10 | E4 | I/O | General-purpose digital I/O<br>Negative terminal for the reference voltage of the ADC for both sources, the internal reference voltage, or an external applied reference voltage |
| AVCC1 | 11 | E1, E2 | | Analog power supply |
| AVSS1 | 12 | F2 | | Analog ground supply |
| XIN | 13 | F1 | I | Input terminal for crystal oscillator XT1 |
| XOUT | 14 | G1 | O | Output terminal of crystal oscillator XT1 |
| AVSS2 | 15 | G2 | | Analog ground supply |

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**表 7-1. Signal Descriptions (continued)**

| TERMINAL | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO.[4] | | | |
| | PZ | ZCA, ZQW | | |
| P5.6/ADC12CLK/DMAE0 | 16 | H1 | I/O | General-purpose digital I/O<br>Conversion clock output ADC (not available on F5632, F5631, and F5630 devices)<br>DMA external trigger input |
| P2.0/P2MAP0 | 17 | G4 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output |
| P2.1/P2MAP1 | 18 | H2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave in/master out; USCI_B0 $I^2C$ data |
| P2.2/P2MAP2 | 19 | J1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 SPI slave out/master in; USCI_B0 $I^2C$ clock |
| P2.3/P2MAP3 | 20 | H4 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable |
| P2.4/P2MAP4 | 21 | J2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in/master out |
| P2.5/P2MAP5 | 22 | K1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: USCI_A0 UART receive data; USCI_A0 slave out/master in |
| P2.6/P2MAP6 | 23 | K2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: no secondary function |
| P2.7/P2MAP7 | 24 | L2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: no secondary function |
| DVCC1 | 25 | L1 | | Digital power supply |
| DVSS1 | 26 | M1 | | Digital ground supply |
| VCORE[2] | 27 | M2 | | Regulated core power supply (internal use only, no external current loading) |
| P5.2 | 28 | L3 | I/O | General-purpose digital I/O |
| DVSS | 29 | M3 | | Digital ground supply |
| DNC | 30 | J4 | | Do not connect. It is strongly recommended to leave this terminal open. |
| P5.3 | 31 | L4 | I/O | General-purpose digital I/O |
| P5.4 | 32 | M4 | I/O | General-purpose digital I/O |
| P5.5 | 33 | J5 | I/O | General-purpose digital I/O |
| P1.0/TA0CLK/ACLK | 34 | L5 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 clock signal TACLK input<br>ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| P1.1/TA0.0 | 35 | M5 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>BSL transmit output |
| P1.2/TA0.1 | 36 | J6 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>BSL receive input |
| P1.3/TA0.2 | 37 | H6 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output |
| P1.4/TA0.3 | 38 | M6 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR3 capture: CCI3A input compare: Out3 output |
| P1.5/TA0.4 | 39 | L6 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output |
| P1.6/TA0.1 | 40 | J7 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output |


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**表 7-1. Signal Descriptions (continued)**

| TERMINAL | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO.[4] | | | |
| | PZ | ZCA, ZQW | | |
| P1.7/TA0.2 | 41 | M7 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output |
| P3.0/TA1CLK/CBOUT | 42 | L7 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 clock input<br>Comparator_B output |
| P3.1/TA1.0 | 43 | H7 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR0: CCI0A/CCI0B input, compare: Out0 output |
| P3.2/TA1.1 | 44 | M8 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR1: CCI1A/CCI1B input, compare: Out1 output |
| P3.3/TA1.2 | 45 | L8 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 capture CCR2: CCI2A/CCI2B input, compare: Out2 output |
| P3.4/TA2CLK/SMCLK | 46 | J8 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 clock input<br>SMCLK output |
| P3.5/TA2.0 | 47 | M9 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR0: CCI0A/CCI0B input, compare: Out0 output |
| P3.6/TA2.1 | 48 | L9 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR1: CCI1A/CCI1B input, compare: Out1 output |
| P3.7/TA2.2 | 49 | M10 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 capture CCR2: CCI2A/CCI2B input, compare: Out2 output |
| P4.0/TB0.0 | 50 | J9 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output |
| P4.1/TB0.1 | 51 | M11 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output |
| P4.2/TB0.2 | 52 | L10 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output |
| P4.3/TB0.3 | 53 | M12 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output |
| P4.4/TB0.4 | 54 | L12 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output |
| P4.5/TB0.5 | 55 | L11 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output |
| P4.6/TB0.6 | 56 | K11 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output |
| P4.7/TB0OUTH/SVMOUT | 57 | K12 | I/O | General-purpose digital I/O with port interrupt<br>Timer TB0: Switch all PWM outputs high impedance<br>SVM output |
| P8.0/TB0CLK | 58 | J11 | I/O | General-purpose digital I/O<br>Timer TB0 clock input |
| P8.1/UCB1STE/UCA1CLK | 59 | J12 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave transmit enable; USCI_A1 clock input/output |
| P8.2/UCA1TXD/UCA1SIMO | 60 | H11 | I/O | General-purpose digital I/O<br>USCI_A1 UART transmit data; USCI_A1 SPI slave in/master out |
| P8.3/UCA1RXD/UCA1SOMI | 61 | H12 | I/O | General-purpose digital I/O<br>USCI_A1 UART receive data; USCI_A1 SPI slave out/master in |

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**表 7-1. Signal Descriptions (continued)**

| TERMINAL | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO.[4] | | | |
| | PZ | ZCA, ZQW | | |
| P8.4/UCB1CLK/UCA1STE | 62 | G11 | I/O | General-purpose digital I/O<br>USCI_B1 clock input/output; USCI_A1 SPI slave transmit enable |
| DVSS2 | 63 | G12 | | Digital ground supply |
| DVCC2 | 64 | F12 | | Digital power supply |
| P8.5/UCB1SIMO/UCB1SDA | 65 | F11 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave in/master out; USCI_B1 $I^2C$ data |
| P8.6/UCB1SOMI/UCB1SCL | 66 | G9 | I/O | General-purpose digital I/O<br>USCI_B1 SPI slave out/master in; USCI_B1 $I^2C$ clock |
| P8.7 | 67 | E12 | I/O | General-purpose digital I/O |
| P9.0 | 68 | E11 | I/O | General-purpose digital I/O |
| P9.1 | 69 | F9 | I/O | General-purpose digital I/O |
| P9.2 | 70 | D12 | I/O | General-purpose digital I/O |
| P9.3 | 71 | D11 | I/O | General-purpose digital I/O |
| P9.4 | 72 | E9 | I/O | General-purpose digital I/O |
| P9.5 | 73 | C12 | I/O | General-purpose digital I/O |
| P9.6 | 74 | C11 | I/O | General-purpose digital I/O |
| P9.7 | 75 | D9 | I/O | General-purpose digital I/O |
| VSSU | 76 | B11, B12 | | USB PHY ground supply |
| PU.0/DP | 77 | A12 | I/O | General-purpose digital I/O, controlled by USB control register. Port U is supplied by the LDOO rail.<br>USB data terminal DP |
| PUR | 78 | B10 | I/O | USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. TI recommends a 1-MΩ resistor to ground. See セクション 9.7.1 for more information. |
| PU.1/DM | 79 | A11 | I/O | General-purpose digital I/O, controlled by USB control register. Port U is supplied by the LDOO rail.<br>USB data terminal DM |
| VBUS | 80 | A10 | | USB LDO input (connect to USB power source) |
| VUSB | 81 | A9 | | USB LDO output |
| V18 | 82 | B9 | | USB regulated power (internal use only, no external current loading) |
| AVSS3 | 83 | A8 | | Analog ground supply |
| P7.2/XT2IN | 84 | B8 | I/O | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2 |
| P7.3/XT2OUT | 85 | B7 | I/O | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2 |
| VBAK | 86 | A7 | | Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see $C_{BAK}$ in セクション 8.3. |
| VBAT | 87 | D8 | | Backup or secondary supply voltage. If backup voltage is not supplied, connect to DVCC externally. |
| P5.7/RTCCLK | 88 | D7 | I/O | General-purpose digital I/O<br>RTCCLK output |
| DVCC3 | 89 | A6 | | Digital power supply |
| DVSS3 | 90 | A5 | | Digital ground supply |
| TEST/SBWTCK | 91 | B6 | I | Test mode pin; selects digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |


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**表 7-1. Signal Descriptions (continued)**

| TERMINAL | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO.[4] | | | |
| | PZ | ZCA, ZQW | | |
| PJ.0/TDO | 92 | B5 | I/O | General-purpose digital I/O<br>Test data output port |
| PJ.1/TDI/TCLK | 93 | A4 | I/O | General-purpose digital I/O<br>Test data input or test clock input |
| PJ.2/TMS | 94 | E7 | I/O | General-purpose digital I/O<br>Test mode select |
| PJ.3/TCK | 95 | D6 | I/O | General-purpose digital I/O<br>Test clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 96 | A3 | I/O | Reset input (active low)[3]<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |
| P6.0/CB0/A0 | 97 | B4 | I/O | General-purpose digital I/O<br>Comparator_B input CB0<br>Analog input A0 – ADC (not available on F5632, F5631, and F5630 devices) |
| P6.1/CB1/A1 | 98 | B3 | I/O | General-purpose digital I/O<br>Comparator_B input CB1<br>Analog input A1 – ADC (not available on F5632, F5631, and F5630 devices) |
| P6.2/CB2/A2 | 99 | A2 | I/O | General-purpose digital I/O<br>Comparator_B input CB2<br>Analog input A2 – ADC (not available on F5632, F5631, and F5630 devices) |
| P6.3/CB3/A3 | 100 | D5 | I/O | General-purpose digital I/O<br>Comparator_B input CB3<br>Analog input A3 – ADC (not available on F5632, F5631, and F5630 devices) |
| Reserved | N/A | E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9 | | Reserved. TI recommends connecting to ground (DVSS, AVSS). |

(1) I = input, O = output, N/A = not available on this package offering
(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.
(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.
(4) See the *Package Option Addendum* in セクション 11 to determine which devices are available in each package.

# 8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC}$ = 3.3 V and $T_A$ = 25°C, unless otherwise noted.

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | MIN | MAX | UNIT |
|---|---|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | –0.3 | 4.1 | V |
| Voltage applied to any pin (excluding VCORE, VBUS, V18)[2] | –0.3 | $V_{CC}$ + 0.3 | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, $T_J$ | | 95 | °C |
| Storage temperature, $T_{stg}$ [3] | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 8.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and flash programming (AVCC1 = DVCC1 = DVCC2 = DVCC3 = $DV_{CC}$ = $V_{CC}$)[1] [2] | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | | 3.6 | |
| $V_{CC,USB}$ | Supply voltage during USB operation, USB PLL disabled (USB_EN = 1, UPLLEN = 0) | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | | 3.6 | |
| | Supply voltage during USB operation, USB PLL enabled[6] (USB_EN = 1, UPLLEN = 1) | PMMCOREVx = 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 2, 3 | 2.4 | | 3.6 | |
| $V_{SS}$ | Supply voltage (AVSS1 = AVSS2 = AVSS3 = DVSS1 = DVSS2 = DVSS3 = $V_{SS}$) | | | 0 | | V |
| $V_{BAT,RTC}$ | Backup-supply voltage with RTC operational | $T_A$ = 0°C to 85°C | 1.55 | | 3.6 | V |
| | | $T_A$ = –40°C to +85°C | 1.70 | | 3.6 | |
| $V_{BAT,MEM}$ | Backup-supply voltage with backup memory retained | $T_A$ = –40°C to +85°C | 1.20 | | 3.6 | V |
| $T_A$ | Operating free-air temperature | I version | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | I version | –40 | | 85 | °C |
| $C_{BAK}$ | Capacitance at pin VBAK | | 1 | 4.7 | 10 | nF |
| $C_{VCORE}$ | Capacitor at VCORE[4] | | | 470 | | nF |


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## 8.3 Recommended Operating Conditions (continued)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{DVCC}/C_{VCORE}$ | Capacitor ratio of DVCC to VCORE | | 10 | | | |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(3) (5) (see 図 8-1) | PMMCOREVx = 0, 1.8 V ≤ $V_{CC}$ ≤ 3.6 V (default condition) | 0 | | 8.0 | MHz |
| | | PMMCOREVx = 1, 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 12.0 | |
| | | PMMCOREVx = 2, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 16.0 | |
| | | PMMCOREVx = 3, 2.4 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 20.0 | |
| $f_{SYSTEM_USB}$ | Minimum processor frequency for USB operation | | 1.5 | | | MHz |
| USB_wait | Wait state cycles during USB operation | | | 16 | | cycles |

(1) TI recommends powering $AV_{CC}$ and $DV_{CC}$ from the same source. A maximum difference of 0.3 V between $AV_{CC}$ and $DV_{CC}$ can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in セクション 8.22 for the exact values and more details.
(3) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(4) A capacitor tolerance of ±20% or better is required.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(6) USB operation with USB PLL enabled requires PMMCOREVx ≥ 2 for proper operation.

NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

**図 8-1. Frequency vs Supply Voltage**

## 8.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)[(1) (2) (3)]

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ | Flash | 3 V | 0 | 0.32 | 0.36 | 2.1 | 2.4 | | | | | mA |
| | | | 1 | 0.36 | | 2.4 | | 3.6 | 4.0 | | | |
| | | | 2 | 0.37 | | 2.5 | | 3.8 | | | | |
| | | | 3 | 0.39 | | 2.7 | | 4.0 | | 6.6 | | |
| $I_{AM, RAM}$ | RAM | 3 V | 0 | 0.18 | 0.21 | 1.0 | 1.2 | | | | | mA |
| | | | 1 | 0.20 | | 1.2 | | 1.7 | 1.9 | | | |
| | | | 2 | 0.22 | | 1.3 | | 2.0 | | | | |
| | | | 3 | 0.23 | | 1.4 | | 2.1 | | 3.6 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing. USB disabled (VUSBEN = 0, SLDOEN = 0).
$f_{ACLK}$ = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

## 8.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[(1) (2)]

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0[(3) (9)] | 2.2 V | 0 | 71 | | 75 | 87 | 81 | | 85 | 99 | µA |
| | | 3 V | 3 | 78 | | 83 | 98 | 89 | | 94 | 108 | |
| $I_{LPM2}$ | Low-power mode 2[(4) (9)] | 2.2 V | 0 | 6.3 | | 6.7 | 9.9 | 9.0 | | 11 | 16 | µA |
| | | 3 V | 3 | 6.6 | | 7.0 | 11 | 10 | | 12 | 18 | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode[(5) (9)] | 2.2 V | 0 | 1.6 | | 1.8 | 2.4 | 4.7 | | 6.5 | 10.5 | µA |
| | | | 1 | 1.6 | | 1.9 | | 4.8 | | 6.6 | | |
| | | | 2 | 1.7 | | 2.0 | | 4.9 | | 6.7 | | |
| | | 3 V | 0 | 1.9 | | 2.1 | 2.7 | 5.0 | | 6.8 | 10.8 | |
| | | | 1 | 1.9 | | 2.1 | | 5.1 | | 7.0 | | |
| | | | 2 | 2.0 | | 2.2 | | 5.2 | | 7.1 | | |
| | | | 3 | 2.0 | | 2.2 | 2.9 | 5.4 | | 7.3 | 12.6 | |
| $I_{LPM3, VLO,WDT}$ | Low-power mode 3, VLO mode, Watchdog enabled[(6) (9)] | 3 V | 0 | 0.9 | | 1.2 | 1.9 | 4.0 | | 5.9 | 10.3 | µA |
| | | | 1 | 0.9 | | 1.2 | | 4.1 | | 6.0 | | |
| | | | 2 | 1.0 | | 1.3 | | 4.2 | | 6.1 | | |
| | | | 3 | 1.0 | | 1.3 | 2.2 | 4.3 | | 6.3 | 11.3 | |
| $I_{LPM4}$ | Low-power mode 4[(7) (9)] | 3 V | 0 | 0.9 | | 1.1 | 1.8 | 3.9 | | 5.8 | 10 | µA |
| | | | 1 | 0.9 | | 1.1 | | 4.0 | | 5.9 | | |
| | | | 2 | 1.0 | | 1.2 | | 4.1 | | 6.1 | | |
| | | | 3 | 1.0 | | 1.2 | 2.1 | 4.2 | | 6.2 | 11 | |
| $I_{LPM3.5, RTC,VCC}$ | Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin $DV_{CC}$ [(10)] | 3 V | | | | 0.5 | | | | 0.8 | 1.4 | µA |


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## 8.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] [2]

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5,RTC,VBAT}$ | Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT[11] | 3 V | | | | 0.6 | | | | 0.8 | 1.4 | µA |
| $I_{LPM3.5,RTC,TOT}$ | Total low-power mode 3.5 (LPM3.5) current with active RTC[12] | 3 V | | 1.0 | | 1.1 | | 1.3 | | 1.6 | 2.8 | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5 (LPM4.5)[8] | 3 V | | 0.2 | | 0.3 | 0.6 | 0.7 | | 0.9 | 1.4 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 1 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(4) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
USB disabled (VUSBEN = 0, SLDOEN = 0).
(5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(6) Current for watchdog timer clocked by VLO included.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(7) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(8) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(9) Current for brownout included. Low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$) disabled. High-side supervisor ($SVS_H$) and high-side monitor ($SVM_H$) disabled. RAM retention enabled.
(10) $V_{VBAT}$ = $V_{CC}$ – 0.2 V, $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active
(11) $V_{VBAT}$ = $V_{CC}$ – 0.2 V, $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK
(12) $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

## 8.6 Thermal Resistance Characteristics

| PARAMETER | | | VALUE | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air[1] | LQFP (PZ) | 122 | °C/W |
| | | BGA (ZQW) | 108 | |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance[2] | LQFP (PZ) | 83 | °C/W |
| | | BGA (ZQW) | 72 | |
| $R\theta_{JB}$ | Junction-to-board thermal resistance[3] | LQFP (PZ) | 98 | °C/W |
| | | BGA (ZQW) | 76 | |

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

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## 8.7 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} – V_{IT-}$) | | 1.8 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor[2] | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).
(2) Also applies to $\overline{RST}$ pin when pullup or pulldown resistor is enabled.

## 8.8 Inputs – Ports P1, P2, P3, and P4

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing[2] | Port P1, P2, P3, P4: P1.x to P4.x,<br>External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

## 8.9 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.x)}$ | High-impedance leakage current | See [1] [2] | 1.8 V, 3 V | | ±50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

## 8.10 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)} = –3$ mA[1] | 1.8 V | $V_{CC} – 0.25$ | $V_{CC}$ | V |
| | | $I_{(OHmax)} = –10$ mA[2] | | $V_{CC} – 0.60$ | $V_{CC}$ | |
| | | $I_{(OHmax)} = –5$ mA[1] | 3 V | $V_{CC} – 0.25$ | $V_{CC}$ | |
| | | $I_{(OHmax)} = –15$ mA[2] | | $V_{CC} – 0.60$ | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)} = 3$ mA[1] | 1.8 V | $V_{SS}$ | $V_{SS} + 0.25$ | V |
| | | $I_{(OLmax)} = 10$ mA[2] | | $V_{SS}$ | $V_{SS} + 0.60$ | |
| | | $I_{(OLmax)} = 5$ mA[1] | 3 V | $V_{SS}$ | $V_{SS} + 0.25$ | |
| | | $I_{(OLmax)} = 15$ mA[2] | | $V_{SS}$ | $V_{SS} + 0.60$ | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.


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## 8.11 Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[3]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA[1] | 1.8 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA[2] | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA[1] | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA[2] | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA[1] | 1.8 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA[2] | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA[1] | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA[2] | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) Selecting reduced drive strength may reduce EMI.

## 8.12 Output Frequency – Ports P1, P2, and P3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | P3.4/TA2CLK/SMCLK/S27, $C_L$ = 20 pF, $R_L$ = 1 kΩ[1] or 3.2 kΩ[2] [3] | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 8 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 20 | |
| $f_{Port_CLK}$ | Clock output frequency | P1.0/TA0CLK/ACLK/S39, P3.4/TA2CLK/SMCLK/S27, P2.0/P2MAP0 (P2MAP0 = PM_MCLK ), $C_L$ = 20 pF[3] | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 8 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 20 | |

(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(3) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

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## 8.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

**図 8-2. Typical Low-Level Output Current vs Low-Level Output Voltage**

**図 8-3. Typical Low-Level Output Current vs Low-Level Output Voltage**

**図 8-4. Typical High-Level Output Current vs High-Level Output Voltage**

**図 8-5. Typical High-Level Output Current vs High-Level Output Voltage**


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## 8.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

**図 8-6. Typical Low-Level Output Current vs Low-Level Output Voltage**

**図 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage**

**図 8-8. Typical High-Level Output Current vs High-Level Output Voltage**

**図 8-9. Typical High-Level Output Current vs High-Level Output Voltage**

## 8.15 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[5]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $T_A$ = 25°C | 3 V | | 0.075 | | μA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, $T_A$ = 25°C | | | 0.170 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1[6] [7] | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals[8] | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 300 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode[1] | XTS = 0, XCAPx = 0[2] | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 12.0 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode[4] | XTS = 0[3] | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF | 3 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | | | 500 | | |

(1) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(2) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(3) Measured with logic-level input frequency but also applies to operation with crystals.
(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(5) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(6) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
(7) Maximum frequency of operation of the entire device cannot be exceeded.


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(8) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:

- For XT1DRIVEx = 0, $C_{L,eff} \leq 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\leq C_{L,eff} \leq$ 9 pF.
- For XT1DRIVEx = 2, 6 pF $\leq C_{L,eff} \leq$ 10 pF.
- For XT1DRIVEx = 3, $C_{L,eff} \geq 6$ pF.

## 8.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[2] [5]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DVCC,XT2}$ | XT2 oscillator crystal current consumption | $f_{OSC}$ = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, $T_A$ = 25°C | 3 V | | 200 | | µA |
| | | $f_{OSC}$ = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, $T_A$ = 25°C | | | 260 | | |
| | | $f_{OSC}$ = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, $T_A$ = 25°C | | | 325 | | |
| | | $f_{OSC}$ = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, $T_A$ = 25°C | | | 450 | | |
| $f_{XT2,HF0}$ | XT2 oscillator crystal frequency, mode 0 | XT2DRIVEx = 0, XT2BYPASS = 0[7] | | 4 | | 8 | MHz |
| $f_{XT2,HF1}$ | XT2 oscillator crystal frequency, mode 1 | XT2DRIVEx = 1, XT2BYPASS = 0[7] | | 8 | | 16 | MHz |
| $f_{XT2,HF2}$ | XT2 oscillator crystal frequency, mode 2 | XT2DRIVEx = 2, XT2BYPASS = 0[7] | | 16 | | 24 | MHz |
| $f_{XT2,HF3}$ | XT2 oscillator crystal frequency, mode 3 | XT2DRIVEx = 3, XT2BYPASS = 0[7] | | 24 | | 32 | MHz |
| $f_{XT2,HF,SW}$ | XT2 oscillator logic-level square-wave input frequency | XT2BYPASS = 1[6] [7] | | 0.7 | | 32 | MHz |
| $OA_{HF}$ | Oscillation allowance for HF crystals[8] | XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF | | | 450 | | Ω |
| | | XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF | | | 320 | | |
| | | XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF | | | 200 | | |
| | | XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF | | | 200 | | |
| $t_{START,HF}$ | Start-up time | $f_{OSC}$ = 6 MHz XT2BYPASS = 0, XT2DRIVEx = 0, $T_A$ = 25°C, $C_{L,eff}$ = 15 pF | 3 V | | 0.5 | | ms |
| | | $f_{OSC}$ = 20 MHz XT2BYPASS = 0, XT2DRIVEx = 3, $T_A$ = 25°C, $C_{L,eff}$ = 15 pF | | | 0.3 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, HF mode[1] [2] | | | | 1 | | pF |
| | Duty cycle | Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz | | 40% | 50% | 60% | |
| $f_{Fault,HF}$ | Oscillator fault frequency[4] | XT2BYPASS = 1[3] | | 30 | | 300 | kHz |

(1) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(2) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(3) Measured with logic-level input frequency but also applies to operation with crystals.

(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(5) To improve EMI on the XT2 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(6) When XT2BYPASS is set, the XT2 circuit is automatically powered down.
(7) Maximum frequency of operation of the entire device cannot be exceeded.
(8) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

## 8.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(–40°C to +85°C) – MIN(–40°C to +85°C)) / MIN(–40°C to +85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

## 8.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_A$ = 25°C | 1.8 V to 3.6 V | | 3 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | $T_A$ = 25°C | 3 V | | | ±1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | µs |

(1) Calculated using the box method: (MAX(–40°C to +85°C) – MIN(–40°C to +85°C)) / MIN(–40°C to +85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)


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## 8.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$ | 1.2 | | 2.3 | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$ | 1.02 | | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% | |
| $df_{DCO}/dT$ | DCO frequency temperature drift | $f_{DCO}$ = 1 MHz | | 0.1 | | %/°C |
| $df_{DCO}/dV_{CC}$ | DCO frequency voltage drift | $f_{DCO}$ = 1 MHz | | 1.9 | | %/V |

**図 8-10. Typical DCO Frequency**

## 8.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(DVCC_BOR_IT-)}$ | $BOR_H$ on voltage, $DV_{CC}$ falling level | $\lvert dDV_{CC}/d_t \rvert < 3$ V/s | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | $BOR_H$ off voltage, $DV_{CC}$ rising level | $\lvert dDV_{CC}/d_t \rvert < 3$ V/s | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | $BOR_H$ hysteresis | | 50 | | 250 | mV |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | 2 | | | µs |

## 8.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE3}$(AM) | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 21 mA | | 1.90 | | V |
| $V_{CORE2}$(AM) | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 21 mA | | 1.80 | | V |
| $V_{CORE1}$(AM) | Core voltage, active mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 17 mA | | 1.60 | | V |
| $V_{CORE0}$(AM) | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 mA ≤ I($V_{CORE}$) ≤ 13 mA | | 1.40 | | V |
| $V_{CORE3}$(LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.94 | | V |
| $V_{CORE2}$(LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.84 | | V |
| $V_{CORE1}$(LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.64 | | V |
| $V_{CORE0}$(LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V, 0 µA ≤ I($V_{CORE}$) ≤ 30 µA | | 1.44 | | V |


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## 8.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 1 | | 2.0 | | µA |
| $V_{(SVSH_IT-)}$ | $SVS_H$ on voltage level(1) | SVSHE = 1, SVSHRVL = 0 | 1.59 | 1.64 | 1.69 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.84 | 1.91 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.04 | 2.11 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.16 | 2.23 | |
| $V_{(SVSH_IT+)}$ | $SVS_H$ off voltage level(1) | SVSHE = 1, SVSMHRRL = 0 | 1.62 | 1.74 | 1.81 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.88 | 1.94 | 2.01 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.07 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.20 | 2.26 | 2.33 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVSH)}$ | $SVS_H$ propagation delay | SVSHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVSHFP = 1 | | 2.5 | | µs |
| | | SVSHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | $SVS_H$ on or off delay time | SVSHE = 0→1, SVSHFP = 1 | | 12.5 | | µs |
| | | SVSHE = 0→1, SVSHFP = 0 | | 100 | | |
| $dV_{DVCC}/dt$ | $DV_{CC}$ rise time | | 0 | | 1000 | V/s |

(1) The $SVS_H$ settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and usage.

## 8.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVMH)}$ | $SVM_H$ current consumption | SVMHE = 0, DVCC = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DVCC = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, DVCC = 3.6 V, SVMHFP = 1 | | 2.0 | | µA |
| $V_{(SVMH)}$ | $SVM_H$ on or off voltage level(1) | SVMHE = 1, SVSMHRRL = 0 | 1.65 | 1.74 | 1.86 | V |
| | | SVMHE = 1, SVSMHRRL = 1 | 1.85 | 1.94 | 2.02 | |
| | | SVMHE = 1, SVSMHRRL = 2 | 2.02 | 2.14 | 2.22 | |
| | | SVMHE = 1, SVSMHRRL = 3 | 2.18 | 2.26 | 2.35 | |
| | | SVMHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVMHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVMHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.75 | | |
| $t_{pd(SVMH)}$ | $SVM_H$ propagation delay | SVMHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVMHFP = 1 | | 2.5 | | µs |
| | | SVMHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | $SVM_H$ on or off delay time | SVMHE = 0→1, SVSMFP = 1 | | 12.5 | | µs |
| | | SVMHE = 0→1, SVMHFP = 0 | | 100 | | |

(1) The $SVM_H$ settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and usage.

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## 8.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSL)}$ | $SVS_L$ current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 2.0 | | µA |
| $t_{pd(SVSL)}$ | $SVS_L$ propagation delay | SVSLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVSLFP = 1 | | 2.5 | | µs |
| | | SVSLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | $SVS_L$ on or off delay time | SVSLE = 0→1, SVSLFP = 1 | | 12.5 | | µs |
| | | SVSLE = 0→1, SVSLFP = 0 | | 100 | | |

## 8.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVML)}$ | $SVM_L$ current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 2.0 | | µA |
| $t_{pd(SVML)}$ | $SVM_L$ propagation delay | SVMLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVMLFP = 1 | | 2.5 | | µs |
| | | SVMLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | $SVM_L$ on or off delay time | SVMLE = 0→1, SVMLFP = 1 | | 12.5 | | µs |
| | | SVMLE = 0→1, SVMLFP = 0 | | 100 | | |

## 8.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(1) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{MCLK} \geq 4$ MHz | | 3 | 6.5 | µs |
| | | | 1 MHz < $f_{MCLK}$ < 4 MHz | | 4 | 8.0 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(2) (3) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | | 150 | 165 | µs |
| $t_{WAKE-UP-LPM5}$ | Wake-up time from LPM3.5 or LPM4.5 to active mode(4) | | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from $\overline{RST}$ or BOR event to active mode(4) | | | | 2 | 3 | ms |

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-FAST}$ is possible with $SVS_L$ and $SVM_L$ in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the MSP430F5xx and MSP430F6xx Family User's Guide.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-SLOW}$ is set with $SVS_L$ and $SVM_L$ in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the MSP430F5xx and MSP430F6xx Family User's Guide.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.


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## 8.27 Timer_A, Timers TA0, TA1, and TA2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

## 8.28 Timer_B, Timer TB0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

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## 8.29 Battery Backup

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{VBAT}$ | Current into VBAT terminal if no primary battery is connected | VBAT = 1.7 V, DVCC not connected, RTC running | $T_A$ = –40°C | | | 0.43 | | µA |
| | | | $T_A$ = 25°C | | | 0.52 | | |
| | | | $T_A$ = 60°C | | | 0.58 | | |
| | | | $T_A$ = 85°C | | | 0.64 | | |
| | | VBAT = 2.2 V, DVCC not connected, RTC running | $T_A$ = –40°C | | | 0.50 | | |
| | | | $T_A$ = 25°C | | | 0.59 | | |
| | | | $T_A$ = 60°C | | | 0.64 | | |
| | | | $T_A$ = 85°C | | | 0.71 | | |
| | | VBAT = 3 V, DVCC not connected, RTC running | $T_A$ = –40°C | | | 0.68 | | |
| | | | $T_A$ = 25°C | | | 0.75 | | |
| | | | $T_A$ = 60°C | | | 0.79 | | |
| | | | $T_A$ = 85°C | | | 0.86 | | |
| $V_{SWITCH}$ | Switch-over level ($V_{CC}$ to VBAT) | $C_{VCC}$ = 4.7 µF | General | | | $V_{SVSH_IT-}$ | | V |
| | | | SVSHRL = 0 | | 1.59 | | 1.69 | |
| | | | SVSHRL = 1 | | 1.79 | | 1.91 | |
| | | | SVSHRL = 2 | | 1.98 | | 2.11 | |
| | | | SVSHRL = 3 | | 2.10 | | 2.23 | |
| $R_{ON_VBAT}$ | ON-resistance of switch between VBAT and VBAK | $V_{BAT}$ = 1.8 V | | 0 V | | 0.35 | 1 | kΩ |
| $V_{BAT3}$ | VBAT to ADC input channel 12: $V_{BAT}$ divided, $V_{BAT3}$ = $V_{BAT}$/3 | | | 1.8 V | | 0.6 | ±5% | V |
| | | | | 3 V | | 1.0 | ±5% | |
| | | | | 3.6 V | | 1.2 | ±5% | |
| $t_{Sample, VBAT3}$ | VBAT to ADC: Sampling time required if VBAT3 selected | ADC12ON = 1, Error of conversion result ≤ 1 LSB | | | 1000 | | | ns |
| $V_{CHVx}$ | Charger end voltage | CHVx = 2 | | | 2.65 | 2.7 | 2.9 | V |
| $R_{CHARGE}$ | Charge limiting resistor | CHCx = 1 | | | | | 5 | kΩ |
| | | CHCx = 2 | | | | | 10 | |
| | | CHCx = 3 | | | | | 20 | |


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## 8.30 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% | | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | | 1 | MHz |
| $t_T$ | UART receive deglitch time(1) | | 2.2 V | 50 | 600 | ns |
| | | | 3 V | 50 | 600 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

## 8.31 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see 図 8-11 and 図 8-12)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | SMCLK or ACLK,<br>Duty cycle = 50% ±10% | | | $f_{SYSTEM}$ | MHz |
| $t_{SU,MI}$ | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 55 | | ns |
| | | | 3 V | 38 | | |
| | | PMMCOREV = 3 | 2.4 V | 30 | | |
| | | | 3 V | 25 | | |
| $t_{HD,MI}$ | SOMI input data hold time | PMMCOREV = 0 | 1.8 V | 0 | | ns |
| | | | 3 V | 0 | | |
| | | PMMCOREV = 3 | 2.4 V | 0 | | |
| | | | 3 V | 0 | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | | 20 | ns |
| | | | 3 V | | 18 | |
| | | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | | 16 | |
| | | | 3 V | | 15 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | –10 | | ns |
| | | | 3 V | –8 | | |
| | | $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | –10 | | |
| | | | 3 V | –8 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 図 8-11 and 図 8-12.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 図 8-11 and 図 8-12.

**図 8-11. SPI Master Mode, CKPH = 0**

**図 8-12. SPI Master Mode, CKPH = 1**


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## 8.32 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]
(see 図 8-13 and 図 8-14)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 11 | | ns |
| | | | 3 V | 8 | | |
| | | PMMCOREV = 3 | 2.4 V | 7 | | |
| | | | 3 V | 6 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE high | PMMCOREV = 0 | 1.8 V | 3 | | ns |
| | | | 3 V | 3 | | |
| | | PMMCOREV = 3 | 2.4 V | 3 | | |
| | | | 3 V | 3 | | |
| $t_{STE,ACC}$ | STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | | 66 | ns |
| | | | 3 V | | 50 | |
| | | PMMCOREV = 3 | 2.4 V | | 36 | |
| | | | 3 V | | 30 | |
| $t_{STE,DIS}$ | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | | 30 | ns |
| | | | 3 V | | 23 | |
| | | PMMCOREV = 3 | 2.4 V | | 16 | |
| | | | 3 V | | 13 | |
| $t_{SU,SI}$ | SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 5 | | ns |
| | | | 3 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 2 | | |
| | | | 3 V | 2 | | |
| $t_{HD,SI}$ | SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 5 | | ns |
| | | | 3 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 5 | | |
| | | | 3 V | 5 | | |
| $t_{VALID,SO}$ | SOMI output data valid time[2] | UCLK edge to SOMI valid, $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | | 76 | ns |
| | | | 3 V | | 60 | |
| | | UCLK edge to SOMI valid, $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | | 44 | |
| | | | 3 V | | 40 | |
| $t_{HD,SO}$ | SOMI output data hold time[3] | $C_L$ = 20 pF, PMMCOREV = 0 | 1.8 V | 18 | | ns |
| | | | 3 V | 12 | | |
| | | $C_L$ = 20 pF, PMMCOREV = 3 | 2.4 V | 10 | | |
| | | | 3 V | 8 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 図 8-13 and 図 8-14.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 図 8-13 and 図 8-14.

**図 8-13. SPI Slave Mode, CKPH = 0**

**図 8-14. SPI Slave Mode, CKPH = 1**


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## 8.33 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-15)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK or ACLK,<br>External: UCLK<br>Duty cycle = 50% ±10% | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2.2 V, 3 V | 0 | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ ≤ 100 kHz | 2.2 V, 3 V | 4.0 | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ ≤ 100 kHz | 2.2 V, 3 V | 4.7 | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | |
| $t_{HD,DAT}$ | Data hold time | | 2.2 V, 3 V | 0 | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2.2 V, 3 V | 250 | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ ≤ 100 kHz | 2.2 V, 3 V | 4.0 | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | | 2.2 V | 50 | 600 | ns |
| | | | 3 V | 50 | 600 | |

**図 8-15. I²C Mode Timing**

## 8.34 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[2]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V | | 2.2 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range[3] | All ADC12 analog input pins Ax | | 0 | | $AV_{CC}$ | V |
| $I_{ADC12_A}$ | Operating supply current into $AV_{CC}$ terminal[4] | $f_{ADC12CLK}$ = 5 MHz[1] | 2.2 V | | 150 | 200 | µA |
| | | | 3 V | | 150 | 250 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time | 2.2 V | | 20 | 25 | pF |
| $R_I$ | Input MUX ON resistance | $0 V \le V_{IN} \le V_{(AVCC)}$ | | 10 | 200 | 1900 | Ω |

(1) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0
(2) The leakage current is specified by the digital I/O input leakage.
(3) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results. If the reference voltage is supplied by an external source or if the internal voltage is used and REFOUT = 1, then decoupling capacitors are required. See セクション 8.40 and セクション 8.41.
(4) The internal reference supply current is not included in current consumption parameter $I_{ADC12}$.

## 8.35 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC12CLK}$ | ADC conversion clock | For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference[1] | 2.2 V, 3 V | 0.45 | 4.8 | 5.0 | MHz |
| | | For specified performance of ADC12 linearity parameters using the internal reference[2] | | 0.45 | 2.4 | 4.0 | |
| | | For specified performance of ADC12 linearity parameters using the internal reference[3] | | 0.45 | 2.4 | 2.7 | |
| $f_{ADC12OSC}$ | Internal ADC12 oscillator[5] | ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock | 2.2 V, 3 V | 2.4 | | 3.1 | µs |
| | | External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0 | | | 13 × 1 / $f_{ADC12CLK}$ | | |
| $t_{Sample}$ | Sampling time | $R_S$ = 400 Ω, $R_I$ = 200 Ω, $C_I$ = 20 pF, $\tau = (R_S + R_I) \times C_I$ [4] | 2.2 V, 3 V | 1000 | | | ns |

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, $R_S$ = external source resistance
(5) The ADC12OSC is sourced directly from MODOSC inside the UCS.


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## 8.36 12-Bit ADC, Linearity Parameters Using an External Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error(2) | 1.4 V ≤ dVREF ≤ 1.6 V(1) | 2.2 V, 3 V | | | ±2 | LSB |
| | | 1.6 V < dVREF (1) | | | | ±1.7 | |
| $E_D$ | Differential linearity error(2) | See (1) | 2.2 V, 3 V | | | ±1 | LSB |
| $E_O$ | Offset error(3) | dVREF ≤ 2.2 V(1) | 2.2 V, 3 V | | ±3 | ±5.6 | LSB |
| | | dVREF > 2.2 V(1) | 2.2 V, 3 V | | ±1.5 | ±3.5 | |
| $E_G$ | Gain error(3) | See (1) | 2.2 V, 3 V | | ±1 | ±2.5 | LSB |
| $E_T$ | Total unadjusted error | dVREF ≤ 2.2 V(1) | 2.2 V, 3 V | | ±3.5 | ±7.1 | LSB |
| | | dVREF > 2.2 V(1) | 2.2 V, 3 V | | ±2 | ±5 | |

(1) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = $V_{R+}$ - $V_{R-}$. $V_{R+}$ < AVCC. $V_{R-}$ > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω, and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF+/VREF- to decouple the dynamic current. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.

## 8.37 12-Bit ADC, Linearity Parameters Using AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error(2) | See (1) | 2.2 V, 3 V | | | ±1.7 | LSB |
| $E_D$ | Differential linearity error(2) | See (1) | 2.2 V, 3 V | | | ±1 | LSB |
| $E_O$ | Offset error(3) | See (1) | 2.2 V, 3 V | | ±1 | ±2 | LSB |
| $E_G$ | Gain error(3) | See (1) | 2.2 V, 3 V | | ±2 | ±4 | LSB |
| $E_T$ | Total unadjusted error | See (1) | 2.2 V, 3 V | | ±2 | ±5 | LSB |

(1) AVCC as reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 0.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.

## 8.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error(2) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 4.0 MHz | 2.2 V, 3 V | | | ±1.7 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | | | ±2.5 | |
| $E_D$ | Differential linearity error(2) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 4.0 MHz | 2.2 V, 3 V | –1 | | +1.5 | LSB |
| | | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | | | ±1 | |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | –1 | | +2.5 | |
| $E_O$ | Offset error(3) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 4.0 MHz | 2.2 V, 3 V | | ±2 | ±4 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | | ±2 | ±4 | |
| $E_G$ | Gain error(3) | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 4.0 MHz | 2.2 V, 3 V | | ±1 | ±2.5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | | | ±1%(4) | VREF |
| $E_T$ | Total unadjusted error | ADC12SR = 0, REFOUT = 1 | $f_{ADC12CLK}$ ≤ 4.0 MHz | 2.2 V, 3 V | | ±2 | ±5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | $f_{ADC12CLK}$ ≤ 2.7 MHz | | | | ±1%(4) | VREF |

(1) The external reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 1. dVREF = $V_{R+}$ - $V_{R-}$.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and the total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

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## 8.39 12-Bit ADC, Temperature Sensor and Built-In $V_{MID}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | Temperature sensor voltage[2] (see )図 8-16 | ADC12ON = 1, INCH = 0Ah, $T_A$ = 0°C | 2.2 V | | 680 | | mV |
| | | | 3 V | | 680 | | |
| $TC_{SENSOR}$ | Temperature coefficient of sensor[2] | ADC12ON = 1, INCH = 0Ah | 2.2 V | | 2.25 | | mV/°C |
| | | | 3 V | | 2.25 | | |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected[3] | ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V | 100 | | | µs |
| | | | 3 V | 100 | | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$ | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected[4] | ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V, 3 V | 1000 | | | ns |

(1) The temperature sensor is provided by the REF module. See the REF module parametric, $I_{REF+}$, regarding the current consumption of the temperature sensor.
(2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times$ (Temperature,°C) + $V_{SENSOR}$, where $TC_{SENSOR}$ and $V_{SENSOR}$ can be computed from the calibration values for higher accuracy. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

**図 8-16. Typical Temperature Sensor Voltage**


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## 8.40 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ [2] | | 1.4 | $AV_{CC}$ | V |
| $V_{REF-}/V_{eREF-}$ | Negative external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ [3] | | 0 | 1.2 | V |
| $V_{eREF+} – V_{REF-}/V_{eREF-}$ | Differential external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ [4] | | 1.4 | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VREF-/VeREF-}$ | Static input current | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF-}$ = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksps | 2.2 V, 3 V | –26 | 26 | µA |
| | | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF-}$ = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, Conversion rate 20 ksps | 2.2 V, 3 V | –1.2 | +1.2 | |
| $C_{VREF+/-}$ | Capacitance at VREF+ or VREF- terminal[5] | | | 10 | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_i$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to let the charge settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Connect two decoupling capacitors, 10 µF and 100 nF, to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. Also see the MSP430F5xx and MSP430F6xx Family User's Guide.

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## 8.41 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1 , $I_{VREF+}$ = 0 A | | 3 V | | 2.5 | ±1% | V |
| | | REFVSEL = {1} for 2 V, REFON = REFOUT = 1, $I_{VREF+}$ = 0 A | | 3 V | | 2.0 | ±1% | |
| | | REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, $I_{VREF+}$ = 0 A | | 2.2 V, 3 V | | 1.5 | ±1% | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | | 2.2 | | | V |
| | | REFVSEL = {1} for 2 V | | | 2.3 | | | |
| | | REFVSEL = {2} for 2.5 V | | | 2.8 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal [2] [7] | ADC12SR = 1[8], REFON = 1, REFOUT = 0, REFBURST = 0 | | 3 V | | 70 | 100 | µA |
| | | ADC12SR = 1[8], REFON = 1, REFOUT = 1, REFBURST = 0 | | | | 0.45 | 0.75 | mA |
| | | ADC12SR = 0[8], REFON = 1, REFOUT = 0, REFBURST = 0 | | | | 210 | 310 | µA |
| | | ADC12SR = 0[8], REFON = 1, REFOUT = 1, REFBURST = 0 | | | | 0.95 | 1.7 | mA |
| $I_{L(VREF+)}$ | Load-current regulation, VREF+ terminal[3] | REFVSEL = {0, 1, 2}, $I_{VREF+}$ = +10 µA , –1000 µA, $AV_{CC}$ = $AV_{CC(min)}$ for each reference level, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1 | | | | 1500 | 2500 | µV/mA |
| $C_{VREF+}$ | Capacitance at VREF+ terminal | REFON = REFOUT = 1[6], 0 mA ≤ $I_{VREF+}$ ≤ $I_{VREF+}$(max) | | 2.2 V, 3 V | 20 | | 100 | pF |
| $TC_{REF+}$ | Temperature coefficient of built-in reference[4] | $I_{VREF+}$ is a constant in the range of 0 mA ≤ $I_{VREF+}$ ≤ –1 mA | REFOUT = 0 | 2.2 V, 3 V | | 20 | | ppm/°C |
| $TC_{REF+}$ | Temperature coefficient of built-in reference[4] | $I_{VREF+}$ is a constant in the range of 0 mA ≤ $I_{VREF+}$ ≤ –1 mA | REFOUT = 1 | 2.2 V, 3 V | | 20 | 50 | ppm/°C |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC}$(min) to $AV_{CC}$(max), $T_A$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | | 120 | 300 | µV/V |
| PSRR_AC | Power supply rejection ratio (AC) | $AV_{CC}$ = $AV_{CC}$(min) to $AV_{CC}$(max), $T_A$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | | 1 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage[5] | $AV_{CC}$ = $AV_{CC}$(min) to $AV_{CC}$(max), REFVSEL = {0, 1, 2}, REFOUT = 0, REFON = 0 → 1 | | | | 75 | | µs |
| | | $AV_{CC}$ = $AV_{CC}$(min) to $AV_{CC}$(max), $C_{VREF}$ = $C_{VREF}$(max), REFVSEL = {0, 1, 2}, REFOUT = 1, REFON = 0 → 1 | | | | 75 | | |

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the $V_{REF+}$ terminal. When REFOUT = 1, the reference is available at the $V_{REF+}$ terminal, as well as, used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
(2) The internal reference current is supplied by the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
(3) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB traces or other external factors.
(4) Calculated using the box method: (MAX(–40°C to +85°C) – MIN(–40°C to +85°C)) / MIN(–40°C to +85°C)/(85°C – (–40°C)).
(5) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.
(6) Connect two decoupling capacitors, 10 µF and 100 nF, to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. Also see the MSP430F5xx and MSP430F6xx Family User's Guide.


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(7) The temperature sensor is provided by the REF module. Its current is supplied by terminal AVCC and is equivalent to $I_{REF+}$ with REFON = 1 and REFOUT = 0.
(8) For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.

## 8.42 12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V | | 2.20 | | 3.60 | V |
| $I_{DD}$ | Supply current, single DAC channel(1) (2) | DAC12AMPx = 2, DAC12IR = 0, DAC12OG = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = 1.5 V | 3 V | | 65 | 110 | µA |
| | | DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = $AV_{CC}$ | 2.2 V, 3 V | | 125 | 165 | |
| | | DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = $AV_{CC}$ | | | 250 | 350 | |
| | | DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = $AV_{CC}$ | | | 750 | 1100 | |
| PSRR | Power supply rejection ratio(3) (4) | DAC12_xDAT = 800h, VeREF+ = 1.5 V, $\Delta AV_{CC}$ = 100 mV | 2.2 V | | 70 | | dB |
| | | DAC12_xDAT = 800h, VeREF+ = 1.5 V or 2.5 V, $\Delta AV_{CC}$ = 100 mV | 3 V | | 70 | | |

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = 20 log ($\Delta AV_{CC}$ / $\Delta V_{DAC12_xOUT}$)
(4) The internal reference is not used.

## 8.43 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-17)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | Resolution | 12-bit monotonic | | | 12 | | | bits |
| INL | Integral nonlinearity(2) | VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 2.2 V | | ±2 | ±4(1) | LSB |
| | | VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 3 V | | ±2 | ±4 | |
| DNL | Differential nonlinearity(2) | VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 2.2 V | | ±0.4 | ±1(1) | LSB |
| | | VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | | 3 V | | ±0.4 | ±1 | |
| $E_O$ | Offset voltage | Without calibration(2) (3) | VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±21(1) | mV |
| | | | VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | ±21 | |
| | | With calibration(2) (3) | VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V | | | ±1.5(1) | |
| | | | VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 3 V | | | ±1.5 | |
| $d_{E(O)}/d_T$ | Offset error temperature coefficient(2) | With calibration | | 2.2 V, 3 V | | ±10 | | µV/°C |
| $E_G$ | Gain error | VeREF+ = 1.5 V | | 2.2 V | | | ±2.5 | %FSR |
| | | VeREF+ = 2.5 V | | 3 V | | | ±2.5 | |
| $d_{E(G)}/d_T$ | Gain temperature coefficient(2) | | | 2.2 V, 3 V | | 10 | | ppm of FSR/ °C |
| $t_{Offset_Cal}$ | Time for offset calibration(4) | DAC12AMPx = 2 | | 2.2 V, 3 V | | | 165 | ms |
| | | DAC12AMPx = 3, 5 | | | | | 66 | |
| | | DAC12AMPx = 4, 6, 7 | | | | | 16.5 | |

(1) This parameter is not production tested.
(2) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + bx. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (VeREF+ / 4095) \times DAC12_xDAT$, DAC12IR = 1.
(3) The offset calibration works on the output operational amplifier. Offset calibration is triggered by setting the DAC12CALON bit.
(4) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends configuring the DAC12 module before initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

**図 8-17. Linearity Test Load Conditions and Gain and Offset Definitions**


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## 8.44 12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage range[(1)] (see 図 8-18) | No load, VeREF+ = $AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2 V, 3 V | 0 | | 0.005 | V |
| | | No load, VeREF+ = $AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | $AV_{CC}$ – 0.05 | | $AV_{CC}$ | |
| | | $R_{Load}$ = 3 kΩ, VeREF+ = $AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | | 0 | | 0.1 | |
| | | $R_{Load}$ = 3 kΩ, VeREF+ = $AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | $AV_{CC}$ – 0.13 | | $AV_{CC}$ | |
| $C_{L(DAC12)}$ | Maximum DAC12 load capacitance | | 2.2 V, 3 V | | | 100 | pF |
| $I_{L(DAC12)}$ | Maximum DAC12 load current | DAC12AMPx = 2, DAC12_xDAT = 0FFFh, $V_{O/P(DAC12)}$ > $AV_{CC}$ – 0.3 | 2.2 V, 3 V | –1 | | | mA |
| | | DAC12AMPx = 2, DAC12_xDAT = 0h, $V_{O/P(DAC12)}$ < 0.3 V | | | | 1 | |
| $R_{O/P(DAC12)}$ | Output resistance (see 図 8-18) | $R_{Load}$ = 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h | 2.2 V, 3 V | | 150 | 250 | Ω |
| | | $R_{Load}$ = 3 kΩ, $V_{O/P(DAC12)}$ > $AV_{CC}$ – 0.3 V, DAC12_xDAT = 0FFFh | | | 150 | 250 | |
| | | $R_{Load}$ = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)}$ ≤ $AV_{CC}$ – 0.3 V | | | | 6 | |

(1) Data is valid after the offset calibration of the output amplifier.

**図 8-18. DAC12_x Output Resistance Tests**

## 8.45 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VeREF+ | Reference input voltage range | DAC12IR = 0[(1) (2)] | 2.2 V, 3 V | | $AV_{CC}$ / 3 | $AV_{CC}$ + 0.2 | V |
| | | DAC12IR = 1[(3) (4)] | | | $AV_{CC}$ | $AV_{CC}$ + 0.2 | |
| $Ri_{(VREF+)}$, $Ri_{(VeREF+)}$ | Reference input resistance | DAC12_0 IR = DAC12_1 IR = 0 | 2.2 V, 3 V | 20 | | | MΩ |
| | | DAC12_0 IR = 1, DAC12_1 IR = 0 | | | 48 | | kΩ |
| | | DAC12_0 IR = 0, DAC12_1 IR = 1 | | | 48 | | |
| | | DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx[(5)] | | | 24 | | |

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AVCC).
(2) The maximum voltage applied at reference input voltage terminal VeREF+ = $(AV_{CC} – V_{E(O)}) / (3 × (1 + E_G))$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AVCC).
(4) The maximum voltage applied at reference input voltage terminal VeREF+ = $(AV_{CC} – V_{E(O)}) / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

## 8.46 12-Bit DAC, Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see 図 8-19 and 図 8-20), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{ON}$ | DAC12 on time | DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB[(1)] (see 図 8-19) | DAC12AMPx = 0 → {2, 3, 4} | 2.2 V, 3 V | | 60 | 120 | µs |
| | | | DAC12AMPx = 0 → {5, 6} | | | 15 | 30 | |
| | | | DAC12AMPx = 0 → 7 | | | 6 | 12 | |
| $t_{S(FS)}$ | Settling time, full scale | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2 V, 3 V | | 100 | 200 | µs |
| | | | DAC12AMPx = 3, 5 | | | 40 | 80 | |
| | | | DAC12AMPx = 4, 6, 7 | | | 15 | 30 | |
| $t_{S(C-C)}$ | Settling time, code to code | DAC12_xDAT = 3F8h → 408h → 3F8h, BF8h → C08h → BF8h | DAC12AMPx = 2 | 2.2 V, 3 V | | 5 | | µs |
| | | | DAC12AMPx = 3, 5 | | | 2 | | |
| | | | DAC12AMPx = 4, 6, 7 | | | 1 | | |
| SR | Slew rate | DAC12_xDAT = 80h → F7Fh → 80h[(2)] | DAC12AMPx = 2 | 2.2 V, 3 V | 0.05 | 0.35 | | V/µs |
| | | | DAC12AMPx = 3, 5 | | 0.35 | 1.10 | | |
| | | | DAC12AMPx = 4, 6, 7 | | 1.50 | 5.20 | | |
| | Glitch energy | DAC12_xDAT = 800h → 7FFh → 800h | DAC12AMPx = 7 | 2.2 V, 3 V | | 35 | | nV-s |

(1) $R_{Load}$ and $C_{Load}$ connected to $AV_{SS}$ (not $AV_{CC}/2$) in 図 8-19.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

**図 8-19. Settling Time and Glitch Energy Testing**


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**図 8-20. Slew Rate Testing**

## 8.47 12-Bit DAC, Dynamic Specifications (Continued)

over recommended ranges of supply voltage and $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $BW_{-3dB}$ | 3-dB bandwidth, $V_{DC}$ = 1.5 V, $V_{AC}$ = 0.1 $V_{PP}$ (see 図 8-21) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2 V, 3 V | 40 | | | kHz |
| | | DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | | 180 | | | |
| | | DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | | 550 | | | |
| | Channel-to-channel crosstalk(1) (see 図 8-22) | DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, $R_{Load}$ = 3 kΩ, $f_{DAC12_1OUT}$ = 10 kHz at 50/50 duty cycle | 2.2 V, 3 V | | –80 | | dB |
| | | DAC12_0DAT = 80h ↔ F7Fh, $R_{Load}$ = 3 kΩ, DAC12_1DAT = 800h, No load, $f_{DAC12_0OUT}$ = 10 kHz at 50/50 duty cycle | | | –80 | | |

(1) $R_{Load}$ = 3 kΩ, $C_{Load}$ = 100 pF

**図 8-21. Test Conditions for 3-dB Bandwidth Specification**

**図 8-22. Crosstalk Test Conditions**

## 8.48 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 1.8 | | 3.6 | V |
| $I_{AVCC_COMP}$ | Comparator operating supply current into AVCC terminal, excludes reference resistor ladder | CBPWRMD = 00 | 1.8 V | | | 40 | µA |
| | | | 2.2 V | | 30 | 50 | |
| | | | 3 V | | 40 | 65 | |
| | | CBPWRMD = 01 | 2.2 V, 3 V | | 10 | 30 | |
| | | CBPWRMD = 10 | 2.2 V, 3 V | | 0.1 | 0.5 | |
| $I_{AVCC_REF}$ | Quiescent current of local reference voltage amplifier into AVCC terminal | CBREFACC = 1, CBREFLx = 01 | | | | 22 | µA |
| $V_{IC}$ | Common-mode input range | | | 0 | | $V_{CC}$ – 1 | V |
| $V_{OFFSET}$ | Input offset voltage | CBPWRMD = 00 | | | | ±20 | mV |
| | | CBPWRMD = 01, 10 | | | | ±10 | |
| $C_{IN}$ | Input capacitance | | | | 5 | | pF |
| $R_{SIN}$ | Series input resistance | On (switch closed) | | | 3 | 4 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | | 450 | ns |
| | | CBPWRMD = 01, CBF = 0 | | | | 600 | |
| | | CBPWRMD = 10, CBF = 0 | | | | 50 | µs |
| $t_{PD,filter}$ | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00 | | 0.35 | 0.6 | 1.0 | µs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01 | | 0.6 | 1.0 | 1.8 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10 | | 1.0 | 1.8 | 3.4 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11 | | 1.8 | 3.4 | 6.5 | |
| $t_{EN_CMP}$ | Comparator enable time, settling time | CBON = 0 to CBON = 1, CBPWRMD = 00, 01 | | | 1 | 2 | µs |
| | | CBON = 0 to CBON = 1, CBPWRMD = 10 | | | | 100 | |
| $t_{EN_REF}$ | Resistor reference enable time | CBON = 0 to CBON = 1 | | | 0.3 | 1.5 | µs |
| $V_{CB_REF}$ | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V |


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## 8.49 Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{USB}$ = 3.3 V ±10%, $I_{OH}$ = –25 mA | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{USB}$ = 3.3 V ±10%, $I_{OL}$ = 25 mA | | 0.4 | V |
| $V_{IH}$ | High-level input voltage | $V_{USB}$ = 3.3 V ±10% | 2.0 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{USB}$ = 3.3 V ±10% | | 0.8 | V |

## 8.50 USB Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OH}$ | D+, D– single ended | USB 2.0 load conditions | 2.8 | 3.6 | V |
| $V_{OL}$ | D+, D– single ended | USB 2.0 load conditions | 0 | 0.3 | V |
| $Z_{(DRV)}$ | D+, D– impedance | Including external series resistor of 27 Ω | 28 | 44 | Ω |
| $t_{RISE}$ | Rise time | Full speed, differential, $C_L$ = 50 pF, 10%/90%, Rpu on D+ | 4 | 20 | ns |
| $t_{FALL}$ | Fall time | Full speed, differential, $C_L$ = 50 pF, 10%/90%, Rpu on D+ | 4 | 20 | ns |

## 8.51 USB Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{(CM)}$ | Differential input common-mode range | 0.8 | 2.5 | V |
| $Z_{(IN)}$ | Input impedance | 300 | | kΩ |
| $V_{CRS}$ | Crossover voltage | 1.3 | 2.0 | V |
| $V_{IL}$ | Static SE input logic low level | | 0.8 | V |
| $V_{IH}$ | Static SE input logic high level | 2.0 | | V |
| VDI | Differential input voltage | | 0.2 | V |

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## 8.52 USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{LAUNCH}$ | $V_{BUS}$ detection threshold | | | | 3.75 | V |
| $V_{BUS}$ | USB bus voltage | Normal operation | 3.76 | | 5.5 | V |
| $V_{USB}$ | USB LDO output voltage | | | 3.3 | ±9% | V |
| $V_{18}$ | Internal USB voltage(1) | | | 1.8 | | V |
| $I_{USB_EXT}$ | Maximum external current from VUSB terminal(2) | USB LDO is on | | | 12 | mA |
| $I_{DET}$ | USB LDO current overload detection(3) | | 60 | | 100 | mA |
| $I_{SUSPEND}$ | Operating supply current into VBUS terminal.(4) | USB LDO is on,<br>USB PLL disabled | | | 250 | µA |
| $C_{BUS}$ | VBUS terminal recommended capacitance | | | 4.7 | | µF |
| $C_{USB}$ | VUSB terminal recommended capacitance | | | 220 | | nF |
| $C_{18}$ | V18 terminal recommended capacitance | | | 220 | | nF |
| $t_{ENABLE}$ | Settling time $V_{USB}$ and $V_{18}$ | Within 2%,<br>recommended capacitances | | | 2 | ms |
| $R_{PUR}$ | Pullup resistance of PUR terminal(5) | | 70 | 110 | 150 | Ω |

(1) This voltage is for internal use only. No external DC loading should be applied.
(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.
(3) A current overload is detected when the total current supplied from the USB LDO, including $I_{USB_EXT}$, exceeds this value.
(4) Does not include current contribution of $R_{pu}$ and $R_{pd}$ as outlined in the USB specification.
(5) This value, in series with an external resistor between PUR and D+, produces the $R_{pu}$ as outlined in the USB specification.

## 8.53 USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{PLL}$ | Operating supply current | | | 7 | mA |
| $f_{PLL}$ | PLL frequency | | 48 | | MHz |
| $f_{UPD}$ | PLL reference frequency | 1.5 | | 3 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 2 | ms |
| $t_{Jitter}$ | PLL jitter | | 1000 | | ps |


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## 8.54 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| $I_{PGM}$ | Average supply current from DVCC during program | | | 3 | 5 | mA |
| $I_{ERASE}$ | Average supply current from DVCC during erase | | | 6 | 15 | mA |
| $I_{MERASE}$, $I_{BANK}$ | Average supply current from DVCC during mass erase or bank erase | | | 6 | 15 | mA |
| $t_{CPT}$ | Cumulative program time(1) | | | | 16 | ms |
| | Program and erase endurance | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | 25°C | 100 | | | years |
| $t_{Word}$ | Word or byte program time(2) | | 64 | | 85 | µs |
| $t_{Block, 0}$ | Block program time for first byte or word(2) | | 49 | | 65 | µs |
| $t_{Block, 1–(N–1)}$ | Block program time for each additional byte or word, except for last byte or word(2) | | 37 | | 49 | µs |
| $t_{Block, N}$ | Block program time for last byte or word(2) | | 55 | | 73 | µs |
| $t_{Seg\ Erase}$ | Erase time for segment, mass erase, and bank erase when available(2) | | 23 | | 32 | ms |
| $f_{MCLK,MGR}$ | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

## 8.55 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW, En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1) | 2.2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency (4-wire JTAG)(2) | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

# 9 Detailed Description

## 9.1 Overview

The MSP430F563x devices include a high-performance 12-bit ADC, a comparator, two USCIs, USB 2.0, a hardware multiplier, DMA, four 16-bit timers, an RTC module with alarm capabilities, and up to 74 I/O pins.

## 9.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see 図 9-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

**図 9-1. Integrated CPU Registers**


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## 9.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. 表 9-1 lists examples of the three types of instruction formats; 表 9-2 lists the address modes.

**表 9-1. Instruction Word Formats**

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

**表 9-2. Address Mode Descriptions**

| ADDRESS MODE | S(1) | D(1) | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV &MEM, &TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect auto-increment | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

## 9.4 Operating Modes

These devices have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No data retention
  - RTC enabled and clocked by low-frequency oscillator
  - Wake-up signal from $\overline{\text{RST}}$/NMI, RTC_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up signal from $\overline{\text{RST}}$/NMI, P1, P2, P3, and P4


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## 9.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see 表 9-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**表 9-3. Interrupt Sources, Flags, and Vectors of MSP430F563x Configurations**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power-Up, External Reset<br>Watchdog Time-out, Key Violation<br>Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV)(1) (3) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>PMM<br>Vacant Memory Access<br>JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>NMI<br>Oscillator Fault<br>Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1) (3) | (Non)maskable | 0FFFAh | 61 |
| Comp_B | Comparator B interrupt flags (CBIV)(1) (2) | Maskable | 0FFF8h | 60 |
| Timer TB0 | TB0CCR0 CCIFG0(2) | Maskable | 0FFF6h | 59 |
| Timer TB0 | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TBIV)(1) (2) | Maskable | 0FFF4h | 58 |
| Watchdog Interval Timer Mode | WDTIFG | Maskable | 0FFF2h | 57 |
| USCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (2) | Maskable | 0FFF0h | 56 |
| USCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (2) | Maskable | 0FFEEh | 55 |
| ADC12_A(5) | ADC12IFG0 to ADC12IFG15 (ADC12IV)(1) (2) | Maskable | 0FFECh | 54 |
| Timer TA0 | TA0CCR0 CCIFG0(2) | Maskable | 0FFEAh | 53 |
| Timer TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (2) | Maskable | 0FFE8h | 52 |
| USB_UBM | USB interrupts (USBIV)(1) (2) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG, DMA4IFG, DMA5IFG (DMAIV)(1) (2) | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0(2) | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (2) | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1) (2) | Maskable | 0FFDEh | 47 |
| USCI_A1 Receive or Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (2) | Maskable | 0FFDCh | 46 |
| USCI_B1 Receive or Transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (2) | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV)(1) (2) | Maskable | 0FFD8h | 44 |
| Reserved | Reserved | Maskable | 0FFD6h | 43 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1) (2) | Maskable | 0FFD4h | 42 |
| DAC12_A(6) | DAC12_0IFG, DAC12_1IFG(1) (2) | Maskable | 0FFD2h | 41 |
| Timer TA2 | TA2CCR0 CCIFG0(2) | Maskable | 0FFD0h | 40 |
| Timer TA2 | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1) (2) | Maskable | 0FFCEh | 39 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV)(1) (2) | Maskable | 0FFCCh | 38 |
| I/O Port P4 | P4IFG.0 to P4IFG.7 (P4IV)(1) (2) | Maskable | 0FFCAh | 37 |
| Reserved | Reserved(4) | | 0FFC8h | 36 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(1) Multiple source flags
(2) Interrupt flags are in the module.
(3) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

(5) Only on devices with peripheral module ADC12_A, otherwise reserved.
(6) Only on devices with peripheral module DAC12_A, otherwise reserved.

## 9.6 Memory

表 9-4 summarizes the memory map for all device variants.

**表 9-4. Memory Organization**

| (1) (3) | | MSP430F5636<br>MSP430F5633<br>MSP430F5630 | MSP430F5637<br>MSP430F5634<br>MSP430F5631 | MSP430F5638<br>MSP430F5635<br>MSP430F5632 |
|---|---|---|---|---|
| Memory (flash)<br>Main: interrupt vector | Total Size | 128KB<br>00FFFFh to 00FF80h | 192KB<br>00FFFFh to 00FF80h | 256KB<br>00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | N/A | N/A | 64KB<br>047FFFh to 038000h |
| | Bank 2 | N/A | 64KB<br>037FFFh to 028000h | 64KB<br>037FFFh to 028000h |
| | Bank 1 | 64KB<br>027FFFh to 018000h | 64KB<br>027FFFh to 018000h | 64KB<br>027FFFh to 018000h |
| | Bank 0 | 64KB<br>017FFFh to 008000h | 64KB<br>017FFFh to 008000h | 64KB<br>017FFFh to 008000h |
| RAM | Sector 3 | 4KB<br>0063FFh to 005400h | 4KB<br>0063FFh to 005400h | 4KB<br>0063FFh to 005400h |
| | Sector 2 | 4KB<br>0053FFh to 004400h | 4KB<br>0053FFh to 004400h | 4KB<br>0053FFh to 004400h |
| | Sector 1 | 4KB<br>0043FFh to 003400h | 4KB<br>0043FFh to 003400h | 4KB<br>0043FFh to 003400h |
| | Sector 0 | 4KB<br>0033FFh to 002400h | 4KB<br>0033FFh to 002400h | 4KB<br>0033FFh to 002400h |
| USB RAM(2) | Size<br>RAM | 2KB<br>0023FFh to 001C00h | 2KB<br>0023FFh to 001C00h | 2KB<br>0023FFh to 001C00h |
| Information memory (flash) | Info A | 128 bytes<br>0019FFh to 001980h | 128 bytes<br>0019FFh to 001980h | 128 bytes<br>0019FFh to 001980h |
| | Info B | 128 bytes<br>00197Fh to 001900h | 128 bytes<br>00197Fh to 001900h | 128 bytes<br>00197Fh to 001900h |
| | Info C | 128 bytes<br>0018FFh to 001880h | 128 bytes<br>0018FFh to 001880h | 128 bytes<br>0018FFh to 001880h |
| | Info D | 128 bytes<br>00187Fh to 001800h | 128 bytes<br>00187Fh to 001800h | 128 bytes<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 bytes<br>0017FFh to 001600h | 512 bytes<br>0017FFh to 001600h | 512 bytes<br>0017FFh to 001600h |
| | BSL 2 | 512 bytes<br>0015FFh to 001400h | 512 bytes<br>0015FFh to 001400h | 512 bytes<br>0015FFh to 001400h |
| | BSL 1 | 512 bytes<br>0013FFh to 001200h | 512 bytes<br>0013FFh to 001200h | 512 bytes<br>0013FFh to 001200h |
| | BSL 0 | 512 bytes<br>0011FFh to 001000h | 512 bytes<br>0011FFh to 001000h | 512 bytes<br>0011FFh to 001000h |
| Peripherals | Size | 4KB<br>000FFFh to 000000h | 4KB<br>000FFFh to 000000h | 4KB<br>000FFFh to 000000h |

(1) N/A = Not available.
(2) USB RAM can be used as general-purpose RAM when not used for USB operation.
(3) Backup RAM is accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.


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## 9.7 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using various serial interfaces. Access to the device memory by the BSL is protected by an user-defined password. For complete description of the features of the BSL and its implementation, see MSP430™ Flash Devices Bootloader (BSL) User's Guide.

### 9.7.1 USB BSL

All devices come preprogrammed with the USB BSL. Use of the USB BSL requires external access to six pins (see 表 9-5). In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT or proper decoupling.

**表 9-5. USB BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| PU.0/DP | USB data terminal DP |
| PU.1/DM | USB data terminal DM |
| PUR | USB pullup resistor terminal |
| VBUS | USB bus power supply |
| VSSU | USB ground supply |

**Note**

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If the PUR pin is pulled high externally, the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-MΩ resistor to ground.

### 9.7.2 UART BSL

A UART BSL is also available that can be programmed by the user into the BSL memory by replacing the preprogrammed, factory supplied, USB BSL. Use of the UART BSL requires external access to six pins (see 表 9-6).

**表 9-6. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.1 | Data transmit |
| P1.2 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

## 9.8 JTAG Operation

### 9.8.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. 表 9-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide. For a complete description of the features of the JTAG interface and its implementation, see MSP430 Programming With the JTAG Interface.

**表 9-7. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

### 9.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 9-8 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide. For a complete description of the features of the JTAG interface and its implementation, see MSP430 Programming With the JTAG Interface.

**表 9-8. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power supply |
| VSS | | Ground supply |

## 9.9 Flash Memory

The flash memory can be programmed by the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

## 9.10 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in セクション 9.6.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

## 9.11 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the Battery Backup System module is implemented.

Eight bytes of backup RAM are available. The backup RAM can be wordwise accessed by the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.


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## 9.12 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the MSP430F5xx and MSP430F6xx Family User's Guide.

### 9.12.1 Digital I/O

Up to nine 8-bit I/O ports are implemented: P1 through P6, P8, and P9 are complete, P7 contains six individual I/O ports, and PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- All eight bits of ports P1, P2, P3, and P4 support edge-selectable interrupt input.
- All instructions support read and write access to port-control registers.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PD).

### 9.12.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2. 表 9-9 lists the mnemonic for each function that can be assigned.

**表 9-9. Port Mapping Mnemonics and Functions**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 0 | PM_NONE | None | $DV_{SS}$ |
| 1 | PM_CBOUT | – | Comparator_B output |
| | PM_TB0CLK | Timer TB0 clock input | – |
| 2 | PM_ADC12CLK | – | ADC12CLK |
| | PM_DMAE0 | DMAE0 Input | – |
| 3 | PM_SVMOUT | – | SVM output |
| | PM_TB0OUTH | Timer TB0 high-impedance input TB0OUTH | – |
| 4 | PM_TB0CCR0B | Timer TB0 CCR0 capture input CCI0B | Timer TB0: TB0.0 compare output Out0 |
| 5 | PM_TB0CCR1B | Timer TB0 CCR1 capture input CCI1B | Timer TB0: TB0.1 compare output Out1 |
| 6 | PM_TB0CCR2B | Timer TB0 CCR2 capture input CCI2B | Timer TB0: TB0.2 compare output Out2 |
| 7 | PM_TB0CCR3B | Timer TB0 CCR3 capture input CCI3B | Timer TB0: TB0.3 compare output Out3 |
| 8 | PM_TB0CCR4B | Timer TB0 CCR4 capture input CCI4B | Timer TB0: TB0.4 compare output Out4 |
| 9 | PM_TB0CCR5B | Timer TB0 CCR5 capture input CCI5B | Timer TB0: TB0.5 compare output Out5 |
| 10 | PM_TB0CCR6B | Timer TB0 CCR6 capture input CCI6B | Timer TB0: TB0.6 compare output Out6 |
| 11 | PM_UCA0RXD | USCI_A0 UART RXD (Direction controlled by USCI – input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 12 | PM_UCA0TXD | USCI_A0 UART TXD (Direction controlled by USCI – output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 13 | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI – input) | |
| 14 | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 $I^2C$ clock (open drain and direction controlled by USCI) | |
| 15 | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 $I^2C$ data (open drain and direction controlled by USCI) | |
| 16 | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI – input) | |
| 17 | PM_MCLK | – | MCLK |

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**表 9-9. Port Mapping Mnemonics and Functions (continued)**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 18 | Reserved | Reserved for test purposes. Do not use this setting. | |
| 19 | Reserved | Reserved for test purposes. Do not use this setting. | |
| 20–30 | Reserved | None | DVSS |
| 31 (0FFh)(1) | PM_ANALOG | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a maximum value of 31.

表 9-10 lists the default values for all pins that support port mapping.

**表 9-10. Default Mapping**

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| P2.0/P2MAP0 | PM_UCB0STE, PM_UCA0CLK | USCI_B0 SPI slave transmit enable (direction controlled by USCI – input), USCI_A0 clock input/output (direction controlled by USCI) | |
| P2.1/P2MAP1 | PM_UCB0SIMO, PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 $I^2C$ data (open drain and direction controlled by USCI) | |
| P2.2/P2MAP2 | PM_UCB0SOMI, PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 $I^2C$ clock (open drain and direction controlled by USCI) | |
| P2.3/P2MAP3 | PM_UCB0CLK, PM_UCA0STE | USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI – input) | |
| P2.4/P2MAP4 | PM_UCA0TXD, PM_UCA0SIMO | USCI_A0 UART TXD (direction controlled by USCI – output), USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| P2.5/P2MAP5 | PM_UCA0RXD, PM_UCA0SOMI | USCI_A0 UART RXD (direction controlled by USCI – input), USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| P2.6/P2MAP6 | PM_NONE | – | DVSS |
| P2.7/P2MAP7 | PM_NONE | – | DVSS |

### 9.12.3 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch-crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### 9.12.4 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply


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voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

### 9.12.5 Hardware Multiplier (MPY) (Link to User's Guide)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 9.12.6 Real-Time Clock (RTC_B)

The RTC_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

Using the MSP430 RTC_B Module With Battery Backup Supply describes how to use the RTC_B with battery backup supply functionality to retain the time and keep the RTC counting through loss of main power supply, and how to perform correct reinitialization when the main power supply is restored.

### 9.12.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### 9.12.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

表 9-11 lists the SYS interrupt vector registers.

**表 9-11. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | RST/NMI (BOR) | | 04h | |
| | PMMSWBOR (BOR) | | 06h | |
| | LPM3.5 or LPM4.5 wakeup (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | SVSL (POR) | | 0Ch | |
| | SVSH (POR) | | 0Eh | |
| | SVML_OVP (POR) | | 10h | |
| | SVMH_OVP (POR) | | 12h | |
| | PMMSWPOR (POR) | | 14h | |
| | WDT time-out (PUC) | | 16h | |
| | WDT key violation (PUC) | | 18h | |
| | KEYV flash key violation (PUC) | | 1Ah | |
| | Reserved | | 1Ch | |
| | Peripheral area fetch (PUC) | | 1Eh | |
| | PMM key violation (PUC) | | 20h | |
| | Reserved | | 22h to 3Eh | Lowest |
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | |
| | SVMLIFG | | 02h | Highest |
| | SVMHIFG | | 04h | |
| | DLYLIFG | | 06h | |
| | DLYHIFG | | 08h | |
| | VMAIFG | | 0Ah | |
| | JMBINIFG | | 0Ch | |
| | JMBOUTIFG | | 0Eh | |
| | SVMLVLRIFG | | 10h | |
| | SVMHVLRIFG | | 12h | |
| | Reserved | | 14h to 1Eh | Lowest |
| SYSUNIV, User NMI | No interrupt pending | 019Ah | 00h | |
| | NMIIFG | | 02h | Highest |
| | OFIFG | | 04h | |
| | ACCVIFG | | 06h | |
| | BUSIFG | | 08h | |
| | Reserved | | 0Ah to 1Eh | Lowest |
| SYSBERRIV, Bus Error | No interrupt pending | 0198h | 00h | |
| | USB wait state time-out | | 02h | Highest |
| | Reserved | | 04h to 1Eh | Lowest |


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### 9.12.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 9-12 lists the trigger assignments for each DMA channel.

The USB timestamp generator also uses the channel 0, 1, and 2 DMA trigger assignments.

**表 9-12. DMA Trigger Assignments**

| TRIGGER(1) | CHANNEL | | | | | |
|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 |
| 0 | DMAREQ | | | | | |
| 1 | TA0CCR0 CCIFG | | | | | |
| 2 | TA0CCR2 CCIFG | | | | | |
| 3 | TA1CCR0 CCIFG | | | | | |
| 4 | TA1CCR2 CCIFG | | | | | |
| 5 | TA2CCR0 CCIFG | | | | | |
| 6 | TA2CCR2 CCIFG | | | | | |
| 7 | TBCCR0 CCIFG | | | | | |
| 8 | TBCCR2 CCIFG | | | | | |
| 9 | Reserved | | | | | |
| 10 | Reserved | | | | | |
| 11 | Reserved | | | | | |
| 12 | Reserved | | | | | |
| 13 | Reserved | | | | | |
| 14 | Reserved | | | | | |
| 15 | Reserved | | | | | |
| 16 | UCA0RXIFG | | | | | |
| 17 | UCA0TXIFG | | | | | |
| 18 | UCB0RXIFG | | | | | |
| 19 | UCB0TXIFG | | | | | |
| 20 | UCA1RXIFG | | | | | |
| 21 | UCA1TXIFG | | | | | |
| 22 | UCB1RXIFG | | | | | |
| 23 | UCB1TXIFG | | | | | |
| 24 | ADC12IFGx(2) | | | | | |
| 25 | DAC12_0IFG(3) | | | | | |
| 26 | DAC12_1IFG(3) | | | | | |
| 27 | USB FNRXD | | | | | |
| 28 | USB ready | | | | | |
| 29 | MPY ready | | | | | |
| 30 | DMA5IFG | DMA0IFG | DMA1IFG | DMA2IFG | DMA3IFG | DMA4IFG |
| 31 | DMAE0 | | | | | |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.
(2) Only on devices with peripheral module ADC12_A. Reserved on devices without ADC.
(3) Only on devices with peripheral module DAC12_A. Reserved on devices without DAC.

### 9.12.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 or 4 pin) or $I^2C$.

The MSP430F563x series includes two complete USCI modules (n = 0 or 1).

### 9.12.11 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see 表 9-13). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

**表 9-13. Timer TA0 Signal Connections**

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|---|---|---|---|---|---|---|---|---|
| PZ | ZCA, ZQW | | | | | | PZ | ZCA, ZQW |
| 34-P1.0 | L5-P1.0 | TA0CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 34-P1.0 | L5-P1.0 | TA0CLK | $\overline{TACLK}$ | | | | | |
| 35-P1.1 | M5-P1.1 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 35-P1.1 | M5-P1.1 |
| | | $DV_{SS}$ | CCI0B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 36-P1.2 | J6-P1.2 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 36-P1.2 | J6-P1.2 |
| 40-P1.6 | J7-P1.6 | TA0.1 | CCI1B | | | | 40-P1.6 | J7-P1.6 |
| | | $DV_{SS}$ | GND | | | | ADC12_A (internal)(1) ADC12SHSx = {1} | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 37-P1.3 | H6-P1.3 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 37-P1.3 | H6-P1.3 |
| 41-P1.7 | M7-P1.7 | TA0.2 | CCI2B | | | | 41-P1.7 | M7-P1.7 |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 38-P1.4 | M6-P1.4 | TA0.3 | CCI3A | CCR3 | TA3 | TA0.3 | 38-P1.4 | M6-P1.4 |
| | | $DV_{SS}$ | CCI3B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 39-P1.5 | L6-P1.5 | TA0.4 | CCI4A | CCR4 | TA4 | TA0.4 | 39-P1.5 | L6-P1.5 |
| | | $DV_{SS}$ | CCI4B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |

(1) Only on devices with peripheral module ADC12_A.


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### 9.12.12 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 supports multiple capture/compares, PWM outputs, and interval timing (see 表 9-14). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

**表 9-14. Timer TA1 Signal Connections**

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|---|---|---|---|---|---|---|---|---|
| PZ | ZCA, ZQW | | | | | | PZ | ZCA, ZQW |
| 42-P3.0 | L7-P3.0 | TA1CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 42-P3.0 | L7-P3.0 | TA1CLK | $\overline{\text{TACLK}}$ | | | | | |
| 43-P3.1 | H7-P3.1 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 43-P3.1 | H7-P3.1 |
| | | $DV_{SS}$ | CCI0B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 44-P3.2 | M8-P3.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 44-P3.2 | M8-P3.2 |
| | | CBOUT (internal) | CCI1B | | | | DAC12_A[(1)] DAC12_0, DAC12_1 (internal) | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 45-P3.3 | L8-P3.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 45-P3.3 | L8-P3.3 |
| | | ACLK (internal) | CCI2B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |

(1) Only on devices with peripheral module DAC12_A.

### 9.12.13 Timer TA2

Timer TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 supports multiple capture/compares, PWM outputs, and interval timing (see 表 9-15). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

**表 9-15. Timer TA2 Signal Connections**

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|---|---|---|---|---|---|---|---|---|
| PZ | ZCA, ZQW | | | | | | PZ | ZCA, ZQW |
| 46-P3.4 | J8-P3.4 | TA2CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 46-P3.4 | J8-P3.4 | TA2CLK | $\overline{\text{TACLK}}$ | | | | | |
| 47-P3.5 | M9-P3.5 | TA2.0 | CCI0A | CCR0 | TA0 | TA2.0 | 47-P3.5 | M9-P3.5 |
| | | $DV_{SS}$ | CCI0B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 48-P3.6 | L9-P3.6 | TA2.1 | CCI1A | CCR1 | TA1 | TA2.1 | 48-P3.6 | L9-P3.6 |
| | | CBOUT (internal) | CCI1B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 49-P3.7 | M10-P3.7 | TA2.2 | CCI2A | CCR2 | TA2 | TA2.2 | 49-P3.7 | M10-P3.7 |
| | | ACLK (internal) | CCI2B | | | | | |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |


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### 9.12.14 Timer TB0

Timer TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 supports multiple capture/compares, PWM outputs, and interval timing (see 表 9-16). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

**表 9-16. Timer TB0 Signal Connections**

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|---|---|---|---|---|---|---|---|---|
| PZ | ZCA, ZQW | | | | | | PZ | ZCA, ZQW |
| 58-P8.0 P2MAPx(3) | J11-P8.0 P2MAPx(3) | TB0CLK | TB0CLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 58-P8.0 P2MAPx(3) | J11-P8.0 P2MAPx(3) | TB0CLK | $\overline{\text{TB0CLK}}$ | | | | | |
| 50-P4.0 | J9-P4.0 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 50-P4.0 | J9-P4.0 |
| P2MAPx(3) | P2MAPx(3) | TB0.0 | CCI0B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | ADC12 (internal) (1) ADC12SHSx = {2} | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 51-P4.1 | M11-P4.1 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 51-P4.1 | M11-P4.1 |
| P2MAPx(3) | P2MAPx(3) | TB0.1 | CCI1B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | ADC12 (internal) (1) ADC12SHSx = {3} | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 52-P4.2 | L10-P4.2 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 52-P4.2 | L10-P4.2 |
| P2MAPx(3) | P2MAPx(3) | TB0.2 | CCI2B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | DAC12_A(2) (internal) DAC12_0, DAC12_1 | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 53-P4.3 | M12-P4.3 | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | 53-P4.3 | M12-P4.3 |
| P2MAPx(3) | P2MAPx(3) | TB0.3 | CCI3B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 54-P4.4 | L12-P4.4 | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | 54-P4.4 | L12-P4.4 |
| P2MAPx(3) | P2MAPx(3) | TB0.4 | CCI4B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 55-P4.5 | L11-P4.5 | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | 55-P4.5 | L11-P4.5 |
| P2MAPx(3) | P2MAPx(3) | TB0.5 | CCI5B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |
| 56-P4.6 | K11-P4.6 | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | 56-P4.6 | K11-P4.6 |
| P2MAPx(3) | P2MAPx(3) | TB0.6 | CCI6B | | | | P2MAPx(3) | P2MAPx(3) |
| | | $DV_{SS}$ | GND | | | | | |
| | | $DV_{CC}$ | $V_{CC}$ | | | | | |

(1) Only on devices with peripheral module ADC12_A.
(2) Only on devices with peripheral module DAC12_A.
(3) Timer functions selectable by the port mapping controller.

### 9.12.15 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 9.12.16 ADC12_A

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

The DAC12_A module is a 12-bit R-ladder voltage-output DAC. The DAC12_A may be used in 8-bit or 12-bit mode, and may be used with the DMA controller. When multiple DAC12_A modules are present, they may be grouped together for synchronous operation.

### 9.12.18 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### 9.12.19 Voltage Reference (REF) Module

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

### 9.12.20 USB Universal Serial Bus

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

### 9.12.21 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to 10 hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level


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### 9.12.22 Peripheral File Map

表 9-17 lists the register base address for all of the available peripheral modules.

**表 9-17. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE(1) |
|---|---|---|
| Special Functions (see 表 9-18) | 0100h | 000h to 01Fh |
| PMM (see 表 9-19) | 0120h | 000h to 010h |
| Flash Control (see 表 9-20) | 0140h | 000h to 00Fh |
| CRC16 (see 表 9-21) | 0150h | 000h to 007h |
| RAM Control (see 表 9-22) | 0158h | 000h to 001h |
| Watchdog (see 表 9-23) | 015Ch | 000h to 001h |
| UCS (see 表 9-24) | 0160h | 000h to 01Fh |
| SYS (see 表 9-25) | 0180h | 000h to 01Fh |
| Shared Reference (see 表 9-26) | 01B0h | 000h to 001h |
| Port Mapping Control (see 表 9-27) | 01C0h | 000h to 003h |
| Port Mapping Port P2 (see 表 9-27) | 01D0h | 000h to 007h |
| Port P1, P2 (see 表 9-28) | 0200h | 000h to 01Fh |
| Port P3, P4 (see 表 9-29) | 0220h | 000h to 01Fh |
| Port P5, P6 (see 表 9-30) | 0240h | 000h to 00Bh |
| Port P7, P8 (see 表 9-31) | 0260h | 000h to 00Bh |
| Port P9 (see 表 9-32) | 0280h | 000h to 00Bh |
| Port PJ (see 表 9-33) | 0320h | 000h to 01Fh |
| Timer TA0 (see 表 9-34) | 0340h | 000h to 02Eh |
| Timer TA1 (see 表 9-35) | 0380h | 000h to 02Eh |
| Timer TB0 (see 表 9-36) | 03C0h | 000h to 02Eh |
| Timer TA2 (see 表 9-37) | 0400h | 000h to 02Eh |
| Battery Backup (see 表 9-38) | 0480h | 000h to 01Fh |
| RTC_B (see 表 9-39) | 04A0h | 000h to 01Fh |
| 32-bit Hardware Multiplier (see 表 9-40) | 04C0h | 000h to 02Fh |
| DMA General Control (see 表 9-41) | 0500h | 000h to 00Fh |
| DMA Channel 0 (see 表 9-41) | 0510h | 000h to 00Ah |
| DMA Channel 1 (see 表 9-41) | 0520h | 000h to 00Ah |
| DMA Channel 2 (see 表 9-41) | 0530h | 000h to 00Ah |
| DMA Channel 3 (see 表 9-41) | 0540h | 000h to 00Ah |
| DMA Channel 4 (see 表 9-41) | 0550h | 000h to 00Ah |
| DMA Channel 5 (see 表 9-41) | 0560h | 000h to 00Ah |
| USCI_A0 (see 表 9-42) | 05C0h | 000h to 01Fh |
| USCI_B0 (see 表 9-43) | 05E0h | 000h to 01Fh |
| USCI_A1 (see 表 9-44) | 0600h | 000h to 01Fh |
| USCI_B1 (see 表 9-45) | 0620h | 000h to 01Fh |
| ADC12_A (see 表 9-46) | 0700h | 000h to 03Fh |
| DAC12_A (see 表 9-47) | 0780h | 000h to 01Fh |
| Comparator_B (see 表 9-48) | 08C0h | 000h to 00Fh |
| USB configuration (see 表 9-49) | 0900h | 000h to 014h |
| USB control (see 表 9-50) | 0920h | 000h to 01Fh |

(1) For a detailed description of the individual control register offset addresses, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

**表 9-18. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**表 9-19. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

**表 9-20. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

**表 9-21. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC result | CRC16INIRES | 04h |

**表 9-22. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RAM control 0 | RCCTL0 | 00h |

**表 9-23. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**表 9-24. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

**表 9-25. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |


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### 表 9-25. SYS Registers (Base Address: 0180h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

### 表 9-26. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

### 表 9-27. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P2: 01D0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port mapping password | PMAPPWD | 00h |
| Port mapping control | PMAPCTL | 02h |
| Port P2.0 mapping | P2MAP0 | 00h |
| Port P2.1 mapping | P2MAP1 | 01h |
| Port P2.2 mapping | P2MAP2 | 02h |
| Port P2.3 mapping | P2MAP3 | 03h |
| Port P2.4 mapping | P2MAP4 | 04h |
| Port P2.5 mapping | P2MAP5 | 05h |
| Port P2.6 mapping | P2MAP6 | 06h |
| Port P2.7 mapping | P2MAP7 | 07h |

### 表 9-28. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |

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**表 9-28. Port P1, P2 Registers (Base Address: 0200h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**表 9-29. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

**表 9-30. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pullup/pulldown enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pullup/pulldown enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

**表 9-31. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 input | P7IN | 00h |


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### 表 9-31. Port P7, P8 Registers (Base Address: 0260h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 pullup/pulldown enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 pullup/pulldown enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

### 表 9-32. Port P9 Register (Base Address: 0280h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 pullup/pulldown enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |

### 表 9-33. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

### 表 9-34. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| Capture/compare control 3 | TA0CCTL3 | 08h |
| Capture/compare control 4 | TA0CCTL4 | 0Ah |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| Capture/compare 3 | TA0CCR3 | 18h |
| Capture/compare 4 | TA0CCR4 | 1Ah |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

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### 表 9-35. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

### 表 9-36. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| Capture/compare control 3 | TB0CCTL3 | 08h |
| Capture/compare control 4 | TB0CCTL4 | 0Ah |
| Capture/compare control 5 | TB0CCTL5 | 0Ch |
| Capture/compare control 6 | TB0CCTL6 | 0Eh |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| Capture/compare 3 | TB0CCR3 | 18h |
| Capture/compare 4 | TB0CCR4 | 1Ah |
| Capture/compare 5 | TB0CCR5 | 1Ch |
| Capture/compare 6 | TB0CCR6 | 1Eh |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

### 表 9-37. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| Capture/compare control 2 | TA2CCTL2 | 06h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| Capture/compare 2 | TA2CCR2 | 16h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |


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### 表 9-38. Battery Backup Registers (Base Address: 0480h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Battery backup memory 0 | BAKMEM0 | 00h |
| Battery backup memory 1 | BAKMEM1 | 02h |
| Battery backup memory 2 | BAKMEM2 | 04h |
| Battery backup memory 3 | BAKMEM3 | 06h |
| Battery backup control | BAKCTL | 1Ch |
| Battery charger control | BAKCHCTL | 1Eh |

### 表 9-39. Real-Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-binary conversion | BCD2BIN | 1Eh |

### 表 9-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |

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**表 9-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**表 9-41. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA general control: DMA module control 0 | DMACTL0 | 00h |
| DMA general control: DMA module control 1 | DMACTL1 | 02h |
| DMA general control: DMA module control 2 | DMACTL2 | 04h |
| DMA general control: DMA module control 3 | DMACTL3 | 06h |
| DMA general control: DMA module control 4 | DMACTL4 | 08h |
| DMA general control: DMA interrupt vector | DMAIV | 0Ah |
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA channel 3 control | DMA3CTL | 00h |
| DMA channel 3 source address low | DMA3SAL | 02h |
| DMA channel 3 source address high | DMA3SAH | 04h |
| DMA channel 3 destination address low | DMA3DAL | 06h |
| DMA channel 3 destination address high | DMA3DAH | 08h |


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### 表 9-41. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 3 transfer size | DMA3SZ | 0Ah |
| DMA channel 4 control | DMA4CTL | 00h |
| DMA channel 4 source address low | DMA4SAL | 02h |
| DMA channel 4 source address high | DMA4SAH | 04h |
| DMA channel 4 destination address low | DMA4DAL | 06h |
| DMA channel 4 destination address high | DMA4DAH | 08h |
| DMA channel 4 transfer size | DMA4SZ | 0Ah |
| DMA channel 5 control | DMA5CTL | 00h |
| DMA channel 5 source address low | DMA5SAL | 02h |
| DMA channel 5 source address high | DMA5SAH | 04h |
| DMA channel 5 destination address low | DMA5DAL | 06h |
| DMA channel 5 destination address high | DMA5DAH | 08h |
| DMA channel 5 transfer size | DMA5SZ | 0Ah |

### 表 9-42. USCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI control 0 | UCA0CTL0 | 00h |
| USCI control 1 | UCA0CTL1 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

### 表 9-43. USCI_B0 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI synchronous control 0 | UCB0CTL0 | 00h |
| USCI synchronous control 1 | UCB0CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |

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**表 9-43. USCI_B0 Registers (Base Address: 05E0h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI interrupt vector word | UCB0IV | 1Eh |

**表 9-44. USCI_A1 Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI control 0 | UCA1CTL0 | 00h |
| USCI control 1 | UCA1CTL1 | 01h |
| USCI baud rate 0 | UCA1BR0 | 06h |
| USCI baud rate 1 | UCA1BR1 | 07h |
| USCI modulation control | UCA1MCTL | 08h |
| USCI status | UCA1STAT | 0Ah |
| USCI receive buffer | UCA1RXBUF | 0Ch |
| USCI transmit buffer | UCA1TXBUF | 0Eh |
| USCI LIN control | UCA1ABCTL | 10h |
| USCI IrDA transmit control | UCA1IRTCTL | 12h |
| USCI IrDA receive control | UCA1IRRCTL | 13h |
| USCI interrupt enable | UCA1IE | 1Ch |
| USCI interrupt flags | UCA1IFG | 1Dh |
| USCI interrupt vector word | UCA1IV | 1Eh |

**表 9-45. USCI_B1 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI synchronous control 0 | UCB1CTL0 | 00h |
| USCI synchronous control 1 | UCB1CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB1BR0 | 06h |
| USCI synchronous bit rate 1 | UCB1BR1 | 07h |
| USCI synchronous status | UCB1STAT | 0Ah |
| USCI synchronous receive buffer | UCB1RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh |
| USCI I2C own address | UCB1I2COA | 10h |
| USCI I2C slave address | UCB1I2CSA | 12h |
| USCI interrupt enable | UCB1IE | 1Ch |
| USCI interrupt flags | UCB1IFG | 1Dh |
| USCI interrupt vector word | UCB1IV | 1Eh |

**表 9-46. ADC12_A Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC12 control 0 | ADC12CTL0 | 00h |
| ADC12 control 1 | ADC12CTL1 | 02h |
| ADC12 control 2 | ADC12CTL2 | 04h |
| Interrupt flag | ADC12IFG | 0Ah |
| Interrupt enable | ADC12IE | 0Ch |
| Interrupt vector word | ADC12IV | 0Eh |
| ADC memory control 0 | ADC12MCTL0 | 10h |
| ADC memory control 1 | ADC12MCTL1 | 11h |
| ADC memory control 2 | ADC12MCTL2 | 12h |
| ADC memory control 3 | ADC12MCTL3 | 13h |


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### 表 9-46. ADC12_A Registers (Base Address: 0700h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC memory control 4 | ADC12MCTL4 | 14h |
| ADC memory control 5 | ADC12MCTL5 | 15h |
| ADC memory control 6 | ADC12MCTL6 | 16h |
| ADC memory control 7 | ADC12MCTL7 | 17h |
| ADC memory control 8 | ADC12MCTL8 | 18h |
| ADC memory control 9 | ADC12MCTL9 | 19h |
| ADC memory control 10 | ADC12MCTL10 | 1Ah |
| ADC memory control 11 | ADC12MCTL11 | 1Bh |
| ADC memory control 12 | ADC12MCTL12 | 1Ch |
| ADC memory control 13 | ADC12MCTL13 | 1Dh |
| ADC memory control 14 | ADC12MCTL14 | 1Eh |
| ADC memory control 15 | ADC12MCTL15 | 1Fh |
| Conversion memory 0 | ADC12MEM0 | 20h |
| Conversion memory 1 | ADC12MEM1 | 22h |
| Conversion memory 2 | ADC12MEM2 | 24h |
| Conversion memory 3 | ADC12MEM3 | 26h |
| Conversion memory 4 | ADC12MEM4 | 28h |
| Conversion memory 5 | ADC12MEM5 | 2Ah |
| Conversion memory 6 | ADC12MEM6 | 2Ch |
| Conversion memory 7 | ADC12MEM7 | 2Eh |
| Conversion memory 8 | ADC12MEM8 | 30h |
| Conversion memory 9 | ADC12MEM9 | 32h |
| Conversion memory 10 | ADC12MEM10 | 34h |
| Conversion memory 11 | ADC12MEM11 | 36h |
| Conversion memory 12 | ADC12MEM12 | 38h |
| Conversion memory 13 | ADC12MEM13 | 3Ah |
| Conversion memory 14 | ADC12MEM14 | 3Ch |
| Conversion memory 15 | ADC12MEM15 | 3Eh |

### 表 9-47. DAC12_A Registers (Base Address: 0780h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DAC12_A channel 0 control 0 | DAC12_0CTL0 | 00h |
| DAC12_A channel 0 control 1 | DAC12_0CTL1 | 02h |
| DAC12_A channel 0 data | DAC12_0DAT | 04h |
| DAC12_A channel 0 calibration control | DAC12_0CALCTL | 06h |
| DAC12_A channel 0 calibration data | DAC12_0CALDAT | 08h |
| DAC12_A channel 1 control 0 | DAC12_1CTL0 | 10h |
| DAC12_A channel 1 control 1 | DAC12_1CTL1 | 12h |
| DAC12_A channel 1 data | DAC12_1DAT | 14h |
| DAC12_A channel 1 calibration control | DAC12_1CALCTL | 16h |
| DAC12_A channel 1 calibration data | DAC12_1CALDAT | 18h |
| DAC12_A interrupt vector word | DAC12IV | 1Eh |

### 表 9-48. Comparator_B Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comp_B control 0 | CBCTL0 | 00h |

**表 9-48. Comparator_B Registers (Base Address: 08C0h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comp_B control 1 | CBCTL1 | 02h |
| Comp_B control 2 | CBCTL2 | 04h |
| Comp_B control 3 | CBCTL3 | 06h |
| Comp_B interrupt | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

**表 9-49. USB Configuration Registers (Base Address: 0900h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USB key/ID | USBKEYID | 00h |
| USB module configuration | USBCNF | 02h |
| USB PHY control | USBPHYCTL | 04h |
| USB power control | USBPWRCTL | 08h |
| USB power voltage setting | USBPWRVSR | 0Ah |
| USB PLL control | USBPLLCTL | 10h |
| USB PLL divider | USBPLLDIV | 12h |
| USB PLL interrupts | USBPLLIR | 14h |

**表 9-50. USB Control Registers (Base Address: 0920h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Input endpoint_0 configuration | USBIEPCNF_0 | 00h |
| Input endpoint_0 byte count | USBIEPCNT_0 | 01h |
| Output endpoint_0 configuration | USBOEPCNF_0 | 02h |
| Output endpoint_0 byte count | USBOEPCNT_0 | 03h |
| Input endpoint interrupt enables | USBIEPIE | 0Eh |
| Output endpoint interrupt enables | USBOEPIE | 0Fh |
| Input endpoint interrupt flags | USBIEPIFG | 10h |
| Output endpoint interrupt flags | USBOEPIFG | 11h |
| USB interrupt vector | USBIV | 12h |
| USB maintenance | USBMAINT | 16h |
| Timestamp | USBTSREG | 18h |
| USB frame number | USBFN | 1Ah |
| USB control | USBCTL | 1Ch |
| USB interrupt enables | USBIE | 1Dh |
| USB interrupt flags | USBIFG | 1Eh |
| Function address | USBFUNADR | 1Fh |


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## 9.13 Input/Output Diagrams

### 9.13.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

図 9-2 shows the pin diagram. 表 9-51 summarizes how to select the pin function.

**図 9-2. Port P1 (P1.0 to P1.7) Diagram**

### 表 9-51. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x |
| P1.0/TA0CLK/ACLK | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.TA0CLK | 0 | 1 |
| | | ACLK | 1 | 1 |
| P1.1/TA0.0 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI0A capture input | 0 | 1 |
| | | Timer TA0.0 output | 1 | 1 |
| P1.2/TA0.1 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI1A capture input | 0 | 1 |
| | | Timer TA0.1 output | 1 | 1 |
| P1.3/TA0.2 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI2A capture input | 0 | 1 |
| | | Timer TA0.2 output | 1 | 1 |
| P1.4/TA0.3 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI3A capture input | 0 | 1 |
| | | Timer TA0.3 output | 1 | 1 |
| P1.5/TA0.4 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI4A capture input | 0 | 1 |
| | | Timer TA0.4 output | 1 | 1 |
| P1.6/TA0.1 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI1B capture input | 0 | 1 |
| | | Timer TA0.1 output | 1 | 1 |
| P1.7/TA0.2 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA0.CCI2B capture input | 0 | 1 |
| | | Timer TA0.2 output | 1 | 1 |


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### 9.13.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

図 9-3 shows the pin diagram. 表 9-52 summarizes how to select the pin function.

**図 9-3. Port P2 (P2.0 to P2.7) Diagram**

### 表 9-52. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx |
| P2.0/P2MAP0 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.1/P2MAP1 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.2/P2MAP2 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.3/P2MAP3 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.4/P2MAP4 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.5/P2MAP5 | 5 | P2.5 (I/O | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.6/P2MAP6 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |
| P2.7/P2MAP7 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | |
| | | Mapped secondary digital function | X | 1 | ≤ 19 |


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### 9.13.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

図 9-4 shows the pin diagram. 表 9-53 summarizes how to select the pin function.

**図 9-4. Port P3 (P3.0 to P3.7) Diagram**

### 表 9-53. Port P3 (P3.0 to P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x |
| P3.0/TA1CLK/CBOUT | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA1.TA1CLK | 0 | 1 |
| | | CBOUT | 1 | 1 |
| P3.1/TA1.0 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA1.CCI0A capture input | 0 | 1 |
| | | Timer TA1.0 output | 1 | 1 |
| P3.2/TA1.1 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA1.CCI1A capture input | 0 | 1 |
| | | Timer TA1.1 output | 1 | 1 |
| P3.3/TA1.2 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA1.CCI2A capture input | 0 | 1 |
| | | Timer TA1.2 output | 1 | 1 |
| P3.4/TA2CLK/SMCLK | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA2.TA2CLK | 0 | 1 |
| | | SMCLK | 1 | 1 |
| P3.5/TA2.0 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA2.CCI0A capture input | 0 | 1 |
| | | Timer TA2.0 output | 1 | 1 |
| P3.6/TA2.1 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA2.CCI1A capture input | 0 | 1 |
| | | Timer TA2.1 output | 1 | 1 |
| P3.7/TA2.2 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TA2.CCI2A capture input | 0 | 1 |
| | | Timer TA2.2 output | 1 | 1 |


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### 9.13.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

図 9-5 shows the pin diagram. 表 9-54 summarizes how to select the pin function.

**図 9-5. Port P4 (P4.0 to P4.7) Diagram**

### 表 9-54. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x |
| P4.0/TB0.0 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI0A capture input | 0 | 1 |
| | | Timer TB0.0 output(1) | 1 | 1 |
| P4.1/TB0.1 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI1A capture input | 0 | 1 |
| | | Timer TB0.1 output(1) | 1 | 1 |
| P4.2/TB0.2 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI2A capture input | 0 | 1 |
| | | Timer TB0.2 output(1) | 1 | 1 |
| P4.3/TB0.3 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI3A capture input | 0 | 1 |
| | | Timer TB0.3 output(1) | 1 | 1 |
| P4.4/TB0.4 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI4A capture input | 0 | 1 |
| | | Timer TB0.4 output(1) | 1 | 1 |
| P4.5/TB0.5 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI5A capture input | 0 | 1 |
| | | Timer TB0.5 output(1) | 1 | 1 |
| P4.6/TB0.6 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.CCI6A capture input | 0 | 1 |
| | | Timer TB0.6 output(1) | 1 | 1 |
| P4.7/TB0OUTH/ SVMOUT | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.TB0OUTH | 0 | 1 |
| | | SVMOUT | 1 | 1 |

(1) Setting TB0OUTH causes all Timer_B configured outputs to be set to high impedance.


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### 9.13.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

図 9-6 shows the pin diagram. 表 9-55 summarizes how to select the pin function.

**図 9-6. Port P5 (P5.0 and P5.1) Diagram**

**表 9-55. Port P5 (P5.0 and P5.1) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x | REFOUT |
| P5.0/VREF+/VeREF+ | 0 | P5.0 (I/O)(2) | I: 0; O: 1 | 0 | X |
| | | VeREF+(3) | X | 1 | 0 |
| | | VREF+(4) | X | 1 | 1 |
| P5.1/VREF-/VeREF- | 1 | P5.1 (I/O)(2) | I: 0; O: 1 | 0 | X |
| | | VeREF-(5) | X | 1 | 0 |
| | | VREF-(6) | X | 1 | 1 |

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A VREF+ reference is available at the pin.
(5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A VREF- reference is available at the pin.

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### 9.13.6 Port P5 (P5.2 to P5.7) Input/Output With Schmitt Trigger

図 9-7 shows the pin diagram. 表 9-56 summarizes how to select the pin function.

**図 9-7. Port P5 (P5.2 to P5.7) Diagram**

**表 9-56. Port P5 (P5.2 to P5.7) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x |
| P5.2 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 |
| P5.3 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 |
| P5.4 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 |
| P5.5 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 |
| P5.6/ADC12CLK/DMAE0 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 |
| | | ADC12CLK | 1 | 1 |
| | | DMAE0 | 0 | 1 |
| P5.7/RTCCLK | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 |
| | | RTCCLK | 1 | 1 |

### 9.13.7 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

図 9-8 shows the pin diagram. 表 9-57 summarizes how to select the pin function.


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**図 9-8. Port P6 (P6.0 to P6.7) Diagram**

## 表 9-57. Port P6 (P6.0 to P6.7) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[1] | | | | |
|---|---|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL.x | CBPD.x | DAC12OPS | DAC12AMPx |
| P6.0/CB0/A0 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB0 | X | X | 1 | n/a | n/a |
| | | A0[1] [2] | X | 1 | X | n/a | n/a |
| P6.1/CB1/A1 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB1 | X | X | 1 | n/a | n/a |
| | | A1[1] [2] | X | 1 | X | n/a | n/a |
| P6.2/CB2/A2 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB2 | X | X | 1 | n/a | n/a |
| | | A2[1] [2] | X | 1 | X | n/a | n/a |
| P6.3/CB3/A3 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB3 | X | X | 1 | n/a | n/a |
| | | A3[1] [2] | X | 1 | X | n/a | n/a |
| P6.4/CB4/A4 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB4 | X | X | 1 | n/a | n/a |
| | | A4[1] [2] | X | 1 | X | n/a | n/a |
| P6.5/CB5/A5 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | CB5 | X | X | 1 | n/a | n/a |
| | | A5 [1] [2] | X | 1 | X | n/a | n/a |
| P6.6/CB6/A6/DAC0 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | CB6 | X | X | 1 | X | 0 |
| | | A6[1] [2] | X | 1 | X | X | 0 |
| | | DAC0 | X | X | X | 0 | >1 |
| P6.7/CB7/A7/DAC1 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | CB7 | X | X | 1 | X | 0 |
| | | A7[1] [2] | X | 1 | X | X | 0 |
| | | DAC1 | X | X | X | 0 | >1 |

(1) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) The ADC12_A channel Ax is connected internally to $AV_{SS}$ if not selected by the respective INCHx bits.


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### 9.13.8 Port P7 (P7.2) Input/Output With Schmitt Trigger

図 9-9 shows the pin diagram. 表 9-58 summarizes how to select the pin function.

**図 9-9. Port P7 (P7.2) Diagram**

### 9.13.9 Port P7 (P7.3) Input/Output With Schmitt Trigger

図 9-10 shows the pin diagram. 表 9-58 summarizes how to select the pin function.

**図 9-10. Port P7 (P7.3) Diagram**

**表 9-58. Port P7 (P7.2 and P7.3) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[(1)] | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.2 | P7SEL.3 | XT2BYPASS |
| P7.2/XT2IN | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2IN crystal mode[(1)] | X | 1 | X | 0 |
| | | XT2IN bypass mode[(1)] | X | 1 | X | 1 |
| P7.3/XT2OUT | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | XT2OUT crystal mode[(2)] | X | 1 | X | 0 |
| | | P7.3 (I/O)[(2)] | X | 1 | 0 | 1 |

(1) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.
(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.


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### 9.13.10 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

図 9-11 shows the pin diagram. 表 9-59 summarizes how to select the pin function.

**図 9-11. Port P7 (P7.4 to P7.7) Diagram**

### 表 9-59. Port P7 (P7.4 to P7.7) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[1] | | | | |
|---|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.x | CBPD.x | DAC12OPS | DAC12AMPx |
| P7.4/CB8/A12 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | Comparator_B input CB8 | X | X | 1 | n/a | n/a |
| | | A12[1] [2] | X | 1 | X | n/a | n/a |
| P7.5/CB9/A13 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 | n/a | n/a |
| | | Comparator_B input CB9 | X | X | 1 | n/a | n/a |
| | | A13[1] [2] | X | 1 | X | n/a | n/a |
| P7.6/CB10/A14/DAC0 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | Comparator_B input CB10 | X | X | 1 | X | 0 |
| | | A14[1] [2] | X | 1 | X | X | 0 |
| | | DAC12_A output DAC0 | X | X | X | 1 | >1 |
| P7.7/CB11/A15/DAC1 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 | X | 0 |
| | | Comparator_B input CB11 | X | X | 1 | X | 0 |
| | | A15[1] [2] | X | 1 | X | X | 0 |
| | | DAC12_A output DAC1 | X | X | X | 1 | >1 |

(1) Setting the P7SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) The ADC12_A channel Ax is connected internally to $AV_{SS}$ if not selected by the respective INCHx bits.


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### 9.13.11 Port P8 (P8.0 to P8.7) Input/Output With Schmitt Trigger

図 9-12 shows the pin diagram. 表 9-60 summarizes how to select the pin function.

**図 9-12. Port P8 (P8.0 to P8.7) Diagram**

**表 9-60. Port P8 (P8.0 to P8.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[(1)] | |
|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x |
| P8.0/TB0CLK | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 |
| | | Timer TB0.TB0CLK clock input | 0 | 1 |
| P8.1/UCB1STE/UCA1CLK | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1STE/UCA1CLK | X | 1 |
| P8.2/UCA1TXD/UCA1SIMO | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1TXD/UCA1SIMO | X | 1 |
| P8.3/UCA1RXD/UCA1SOMI | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1RXD/UCA1SOMI | X | 1 |
| P8.4/UCB1CLK/UCA1STE | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1CLK/UCA1STE | X | 1 |
| P8.5/UCB1SIMO/UCB1SDA | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SIMO/UCB1SDA | X | 1 |
| P8.6/UCB1SOMI/UCB1SCL | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SOMI/UCB1SCL | X | 1 |
| P8.7 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 |

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### 9.13.12 Port P9 (P9.0 to P9.7) Input/Output With Schmitt Trigger

図 9-13 shows the pin diagram. 表 9-61 summarizes how to select the pin function.

**図 9-13. Port P9 (P9.0 to P9.7) Diagram**

**表 9-61. Port P9 (P9.0 to P9.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x |
| P9.0 | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 |
| P9.1 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 |
| P9.2 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 |
| P9.3 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 |
| P9.4 | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 |
| P9.5 | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 |
| P9.6 | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 |
| P9.7 | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 |


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### 9.13.13 Port PU (PU.0/DP, PU.1/DM, PUR) USB Ports

図 9-14 shows the pin diagram. 表 9-62 summarizes how to select the pin function.

**図 9-14. Port PU (PU.0 and PU.1) Diagram**

**表 9-62. Port PU.0/DP and PU.1/DM Output Functions**

| CONTROL BITS | | | | PIN NAME | | FUNCTION |
|---|---|---|---|---|---|---|
| PUSEL | PUDIR | PUOUT1 | PUOUT0 | PU.1/DM | PU.0/DP | |
| 0 | 0 | X | X | Hi-Z | Hi-Z | Outputs off |
| 0 | 1 | 0 | 0 | 0 | 0 | Outputs enabled |
| 0 | 1 | 0 | 1 | 0 | 1 | Outputs enabled |
| 0 | 1 | 1 | 0 | 1 | 0 | Outputs enabled |
| 0 | 1 | 1 | 1 | 1 | 1 | Outputs enabled |
| 1 | X | X | X | DM | DP | Direction set by USB module |

**表 9-63. Port PUR Input Functions**

| CONTROL BITS | | FUNCTION |
|---|---|---|
| PUSEL | PUREN | |
| 0 | 0 | Input disabled<br>Pullup disabled |
| 0 | 1 | Input disabled<br>Pullup enabled |
| 1 | 0 | Input enabled<br>Pullup disabled |
| 1 | 1 | Input enabled<br>Pullup enabled |

### 9.13.14 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

図 9-15 shows the pin diagram. 表 9-64 summarizes how to select the pin function.

**図 9-15. Port J (PJ.0) Diagram**


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### 9.13.15 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

図 9-16 shows the pin diagram. 表 9-64 summarizes how to select the pin function.

**図 9-16. Port PJ (PJ.1 to PJ.3) Diagram**

**表 9-64. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS[(1)] |
|---|---|---|---|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O)[(1)] | I: 0; O: 1 |
| | | TDO[(2)] | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O)[(1)] | I: 0; O: 1 |
| | | TDI/TCLK[(2) (3)] | X |
| PJ.2/TMS | 2 | PJ.2 (I/O)[(1)] | I: 0; O: 1 |
| | | TMS[(2) (3)] | X |
| PJ.3/TCK | 3 | PJ.3 (I/O)[(1)] | I: 0; O: 1 |
| | | TCK[(2) (3)] | X |

(1) Default condition
(2) The pin direction is controlled by the JTAG module.
(3) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

## 9.14 Device Descriptors

表 9-65 list the contents of the device descriptor tag-length-value (TLV) structure.

**表 9-65. MSP430F563x Device Descriptor Table**

| DESCRIPTION[1] | | ADDRESS | SIZE (bytes) | VALUE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | F5638 | F5637 | F5636 | F5635 | F5634 | F5633 | F5632 | F5631 | F5630 |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 2 | 8014h | 8012h | 8010h | 800Eh | 8044h | 8042h | 8040h | 803Eh | 803Ch |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC12 Calibration | ADC12 calibration tag | 01A14h | 1 | 11h | 11h | 11h | 11h | 11h | 11h | 11h | 11h | 11h |
| | ADC12 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference temp. I 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |

(1) NA = Not applicable


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# 10 Device and Documentation Support

## 10.1 Getting Started and Next Steps

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430 ultra-low-power sensing & measurement MCUs overview.

## 10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 図 10-1 provides a legend for reading the complete device name.

| | | |
|---|---|---|
| **Processor Family** | CC = Embedded RF Radio<br>MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device | |
| **MCU Platform** | 430 = MSP430 low-power microcontroller platform | |
| **Device Type** | **Memory Type**<br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash<br>L = No nonvolatile memory | **Specialized Application**<br>AFE = Analog front end<br>BQ = Contactless power<br>CG = ROM medical<br>FE = Flash energy meter<br>FG = Flash medical<br>FW = Flash electronic flow meter |
| **Series** | 1 = Up to 8 MHz<br>2 = Up to 16 MHz<br>3 = Legacy<br>4 = Up to 16 MHz with LCD driver | 5 = Up to 25 MHz<br>6 = Up to 25 MHz with LCD driver<br>0 = Low-voltage series |
| **Feature Set** | Various levels of integration within a series | |
| **Optional: Revision** | Updated version of the base part number | |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = –40°C to 85°C<br>T = –40°C to 105°C | |
| **Packaging** | http://www.ti.com/packaging | |
| **Optional: Tape and Reel** | T = Small reel<br>R = Large reel<br>No markings = Tube or tray | |
| **Optional: Additional Features** | -EP = Enhanced product (–40°C to 105°C)<br>-HT = Extreme temperature parts (–55°C to 150°C)<br>-Q1 = Automotive Q100 qualified | |

**図 10-1. Device Nomenclature**


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## 10.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 ultra-low-power MCUs – Design & development.

表 10-1 lists the debug features of the MSP430F563x MCUs. See the Code Composer Studio™ IDE for MSP430™ MCUs User's Guide for details on the available features.

**表 10-1. Hardware Debug Features**

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT |
|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | Yes | Yes | 8 | Yes | Yes | Yes | Yes | No |

### Design Kits and Evaluation Modules

MSP-TS430PZ100USB - 100-pin Target Development Board for MSP430F5x and MSP430F6x MCUs

The MSP-TS430PZ100USB is a stand-alone 100-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

100-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F5x and MSP430F6x MCUs

The MSP-FET is a powerful flash emulation tool to quickly begin application development on the MSP430 MCU. It includes USB debugging interface used to program and debug the MSP430 in-system through the JTAG interface or the pin saving Spy Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and because the MSP430 flash is ultra-low power, no external power supply is required.

### Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430F563x, MSP430F663x Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP Driver Library

Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

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### ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

### IEC 60730 Software Package

The IEC 60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC 60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

### Fixed Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 MCUs. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

### Floating Point Math Library for MSP430

Continuing to innovate in the low-power and low-cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

**Development Tools**

### Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

The Code Composer Studio integrated development environment (IDE) supports all MSP microcontroller devices. The Code Composer Studio IDE comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. The Code Composer Studio IDE combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using the Code Composer Studio IDE with an MSP430 MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP430 microcontroller.

### Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.


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MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – that lets users quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This gives the MSP programmer a convenient method to communicate serially between the MSP and a terminal running on the computer. It also supports loading programs (often called firmware) to the MSP target using the BSL (bootloader) through the UART and $I^2C$ communication protocols.

MSP-GANG Production Programmer

The MSP Gang Programmer is a device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices. Eight cables are provided that connect the expansion board to eight target devices (through JTAG or Spy-Bi-Wire connectors). The programming can be done with a PC or as a stand-alone device. A PC-side graphical user interface is also available and is DLL-based.

## 10.4 Documentation Support

The following documents describe the MSP430F563x MCUs. Copies of these documents are available on the Internet at www.ti.com.

### Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folders, see セクション 10.5). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### Errata

MSP430F5638 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5637 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5636 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5635 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5634 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5633 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5632 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

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MSP430F5631 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

MSP430F5630 Device Erratasheet

Describes the known exceptions to the functional specifications for this device.

**User's Guides**

MSP430x5xx and MSP430x6xx Family User's Guide

Detailed information on the modules and peripherals available in this device family.

IAR Embedded Workbench IDE for MSP430 MCUs User's Guide

This manual describes the use of IAR Embedded Workbench (EW430) with the MSP430 ultra-low-power microcontrollers.

MSP430™ Flash Devices Bootloader (BSL) User's Guide

The MSP430 BSL lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

**Application Reports**

MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.


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## 10.5 Related Links

表 10-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 10-2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| MSP430F5638 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5637 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5636 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5635 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5634 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5633 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5632 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5631 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5630 | Click here | Click here | Click here | Click here | Click here |

## 10.6 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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## 10.7 Trademarks

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## 10.8 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 10.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 10.10 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430F5630IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5630 |
| MSP430F5630IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5630 |
| MSP430F5631IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5631 |
| MSP430F5631IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5631 |
| MSP430F5632IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5632 |
| MSP430F5632IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5632 |
| MSP430F5632IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5632 |
| MSP430F5632IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5632 |
| MSP430F5632IZCAR | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5632 |
| MSP430F5632IZCAR.B | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5632 |
| MSP430F5633IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5633 |
| MSP430F5633IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5633 |
| MSP430F5633IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5633 |
| MSP430F5633IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5633 |
| MSP430F5634IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5634 |
| MSP430F5634IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5634 |
| MSP430F5635IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5635 |
| MSP430F5635IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5635 |
| MSP430F5635IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5635 |
| MSP430F5635IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5635 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430F5635IZCAR | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5635 |
| MSP430F5635IZCAR.B | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5635 |
| MSP430F5635IZCAT | Active | Production | NFBGA (ZCA) \| 113 | 250 \| SMALL T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5635 |
| MSP430F5635IZCAT.B | Active | Production | NFBGA (ZCA) \| 113 | 250 \| SMALL T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5635 |
| MSP430F5636IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5636 |
| MSP430F5636IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5636 |
| MSP430F5636IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5636 |
| MSP430F5636IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5636 |
| MSP430F5636IZQWR | Obsolete | Production | BGA MICROSTAR JUNIOR (ZQW) \| 113 | - | - | Call TI | Call TI | - | M430F5636 |
| MSP430F5637IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5637 |
| MSP430F5637IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5637 |
| MSP430F5637IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5637 |
| MSP430F5637IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5637 |
| MSP430F5638IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5638 |
| MSP430F5638IPZ.B | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5638 |
| MSP430F5638IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5638 |
| MSP430F5638IPZR.B | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5638 |
| MSP430F5638IZCAR | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5638 |
| MSP430F5638IZCAR.B | Active | Production | NFBGA (ZCA) \| 113 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5638 |
| MSP430F5638IZCAT | Active | Production | NFBGA (ZCA) \| 113 | 250 \| SMALL T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5638 |
| MSP430F5638IZCAT.B | Active | Production | NFBGA (ZCA) \| 113 | 250 \| SMALL T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5638 |
| MSP430F5638IZQWR | Obsolete | Production | BGA MICROSTAR JUNIOR (ZQW) \| 113 | - | - | Call TI | Call TI | -40 to 85 | M430F5638 |
| MSP430F5638IZQWT | Obsolete | Production | BGA MICROSTAR JUNIOR (ZQW) \| 113 | - | - | Call TI | Call TI | -40 to 85 | M430F5638 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F5632IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5632IZCAR | NFBGA | ZCA | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F5633IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5635IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5635IZCAR | NFBGA | ZCA | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430F5637IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5638IZCAR | NFBGA | ZCA | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430F5632IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5632IZCAR | NFBGA | ZCA | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F5633IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5635IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5635IZCAR | NFBGA | ZCA | 113 | 2500 | 350.0 | 350.0 | 43.0 |
| MSP430F5637IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5638IZCAR | NFBGA | ZCA | 113 | 2500 | 350.0 | 350.0 | 43.0 |

## TRAY

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F5630IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5630IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5631IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5631IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5632IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5632IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5632IZCAR | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5632IZCAR.B | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5633IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5633IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5634IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5634IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5635IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5635IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5635IZCAR | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5635IZCAR.B | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5635IZCAT | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F5635IZCAT.B | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5636IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5636IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5637IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5637IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5638IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5638IPZ.B | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5638IZCAR | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5638IZCAR.B | ZCA | NFBGA | 113 | 2500 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5638IZCAT | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5638IZCAT.B | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |

PLASTIC BALL GRID ARRAY

4225149/A 08/2019

NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE

SCALE: 10X

SOLDER MASK DETAILS

NOT TO SCALE

4225149/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4225149/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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