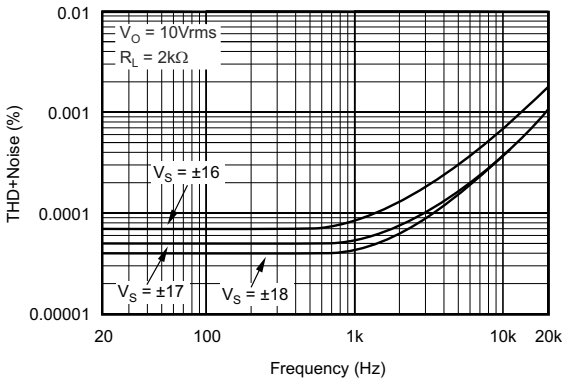
OPAx134 高性能、SoundPlus™ オーディオ オペアンプ

1 特長

- 優れた音質
- 超低歪:0.00008%
- 低ノイズ:8nV/√Hz
- 完全な FET 入力:I_B = 5pA
- 高速度:
  - スルーレート:20V/µs
  - 帯域幅:8MHz
- 高いオープン ループ ゲイン:120dB (2kΩ)
- 幅広い電源電圧範囲:±2.5V～±18V
- シングル、デュアル、クワッドの各バージョン

2 アプリケーション

- 業務用オーディオと音響機器
- ライン ドライバ
- ライン レシーバ
- マルチメディア オーディオ
- アクティブ フィルタ
- プリアンプ
- 積分器
- クロスオーバ ネットワーク



THD + ノイズと周波数との関係

3 概要

OPA134、OPA2134、OPA4134 (OPAx134) シリーズは、非常に低い歪み、低ノイズのオペアンプであり、オーディオ アプリケーション向けに完全に規定されています。完全な FET 入力段を内蔵しているため、優れた音質と速度で非常に優れたオーディオ性能を実現できます。この機能と、高い出力駆動能力および非常に優れた DC 性能との組み合わせにより、要求の厳しいさまざまなアプリケーションで使用できます。さらに、OPAx134 シリーズは、出力スイングがレールから 1V 以内と広く、ヘッドルームが大きいので、あらゆるオーディオ回路での使用に最適です。

OPAx134 SoundPlus™ オーディオ オペアンプは使いやすく、通常の FET 入力オペアンプでしばしば見られるような位相反転や過負荷の問題を引き起こしません。このデバイスは ±2.5V～±18V の電源で動作できます。入力カスコード回路は、優れた同相信号除去を実現し、広い入力電圧範囲にわたって低い入力バイアス電流を維持、歪みを最小限に抑えます。OPAx134 シリーズのオペアンプは、ユニティ ゲインにおいて安定であり、大きい負荷容量を含む幅広い負荷条件にわたって優れた動的挙動を示します。デュアルおよびクワッド バージョンは、完全に独立した回路を使用しているため、オーバードライブまたは過負荷時でも、クロストークが最小限に抑えられ、相互作用が発生しません。

シングルおよびデュアル バージョンは、標準構成の 8 ピン DIP および SO-8 表面実装パッケージで供給されます。クワッド バージョンは、SO-14 表面実装パッケージで供給されます。すべてのデバイスは -40℃～+85℃で動作が規定されています。設計解析用の SPICE マクロモデルが利用できます。

製品情報

部品番号	チャネル数	パッケージ (1)
OPA134	シングル	D (SOIC、8)
		P (PDIP、8)
OPA2134	デュアル	D (SOIC、8)
		P (PDIP、8)
OPA4134	クワッド	D (SOIC、14)

(1) 詳細については、セクション 10 を参照してください。

Table of Contents

4 Pin Configuration and Functions

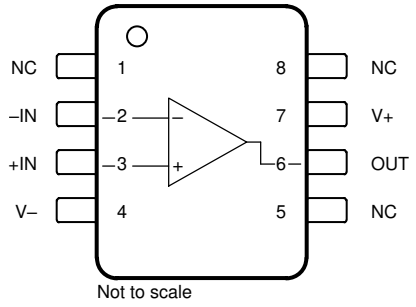


図 4-1. OPA134: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Pin Functions: OPA134

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	2	Input	Inverting input
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
Output	6	Output	Output
V+	7	Power	Positive power supply
V–	4	Power	Negative power supply

(1) Existing layouts for the OPA134 before revision B of this data sheet do not need to be redesigned.

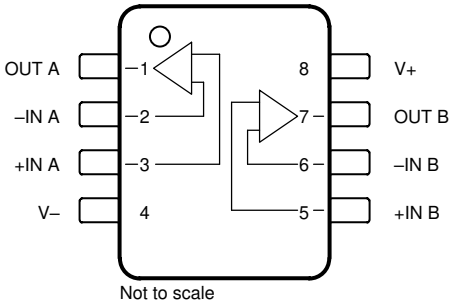


図 4-2. OPA2134: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions: OPA2134

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

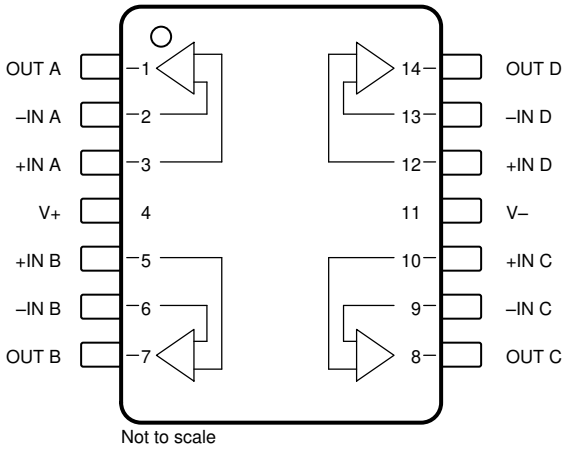


図 4-3. OPA4134: D Package, 14-Pin SOIC (Top View)

表 4-2. Pin Functions: OPA4134

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Single supply		36	V
	Input voltage(2)		(V–) – 0.5	(V+) + 0.5	V
	Input current(2)			±10	mA
I_{SC}	Output short-circuit(3)		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
OPA134 in SOIC and PDIP Packages, and OPA2134 in PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
OPA2134 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
OPA4134 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.5	±15	±18	V
		Single supply	5	30	36	
T_A	Ambient temperature		–40		+85	°C

5.4 Thermal Information - OPA134

THERMAL METRIC(1)		OPA134		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	73	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	17	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	35	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA2134

THERMAL METRIC(1)		OPA2134		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	71	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	16	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	35	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information - OPA4134

THERMAL METRIC(1)		OPA4132	UNIT
		D (SOIC)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3V_{rms}	R_L = 2kΩ		0.00008		%
			R_L = 600Ω		0.00015		
	Intermodulation distortion	f = 1kHz, G = 1, V_O = 1V_{PP}			–98		dB
	Headroom(1)	THD < 0.01%, R_L = 2kΩ, V_S = 18V			21.3		dBu
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				8		MHz
SR	Slew rate(2)				±20		V/µs
	Settling time	10V step, G = 1, C_L = 100pF	0.1%		0.7		µs
			0.01%		1		
FPBW	Full power bandwidth				1.3		MHz
	Overload recovery time	V_{IN} × G = V_S			0.6		µs
NOISE							
	Input voltage noise	f = 20Hz to 20kHz			1.2		μV_{rms}
e_n	Input voltage noise density	f = 1kHz			8		nV/√Hz
I_n	Input current noise density	f = 1kHz			3		fA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±3.5	mV
		T_A = –40°C to +85°C			±1		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2		µV/°C
PSRR	Power-supply rejection ratio	5V ≤ V_S ≤ 36V		90	106		dB
	Channel separation (dual, quad)	DC, R_L = 2kΩ			128		dB
		f = 20kHz, R_L = 2kΩ			126		
INPUT BIAS CURRENT							
I_B	Input bias current(3)				±5	±100	pA
		T_A = –40°C to +85°C			See セクション 5.8	±5	nA
I_{OS}	Input offset current(3)				±2	±50	pA
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2.5	±13	(V+) – 3.5	V
CMRR	Common-mode rejection ratio	–12.5V ≤ V_{CM} ≤ 11.5V		86	100		dB
			TA = –40°C to +85°C		90		
INPUT IMPEDANCE							
	Differential				10^{13} || 8		Ω || pF
	Common-mode	–12.5V ≤ V_{CM} ≤ 11.5V			10^{13} || 6		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10kΩ, –14.5V ≤ V_O ≤ 13.8V		104	120		dB
		R_L = 2kΩ, –13.8V ≤ V_O ≤ 13.5V		104	120		

5.7 Electrical Characteristics (続き)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output	R_L = 10kΩ	Positive	(V+) – 1.2			V
			Negative			(V–) + 0.5	
		R_L = 2kΩ	Positive	(V+) – 1.5			
			Negative			(V–) + 1.2	
I_{SC}	Short-circuit current	Sourcing			36		mA
		Sinking			–30		
Z_O	Output impedance	f = 10kHz	Closed-loop(4)		0.01		Ω
			Open-loop		10		
	Capacitive load drive	Stable operation			See *Typical Characteristics*		
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0mA			4	5	mA

(1) dBu = 20 × log (V_{rms} / 0.7746) where V_{rms} is the maximum output voltage for which THD+Noise is less than 0.01%. See *Total Harmonic Distortion*.
(2) Proposed by design.
(3) High-speed test at T_J = 25°C.
(4) See *Closed-Loop Output Impedance vs Frequency* in *Typical Characteristics*.

5.8 Typical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

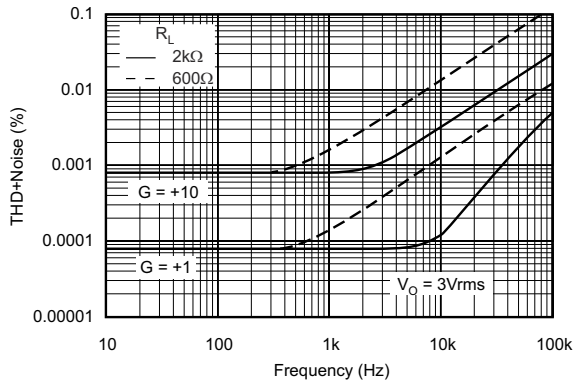


図 5-1. Total Harmonic Distortion + Noise vs Frequency

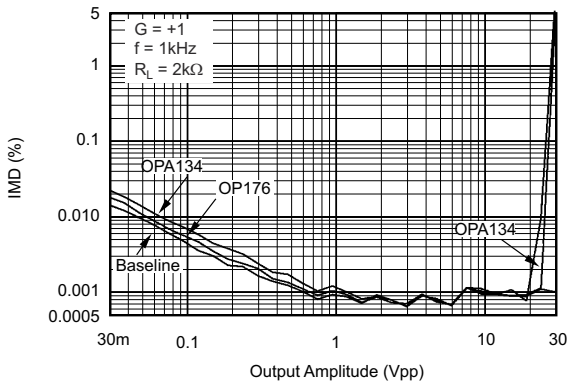


図 5-2. SMPTE Intermodulation Distortion vs Output Amplitude

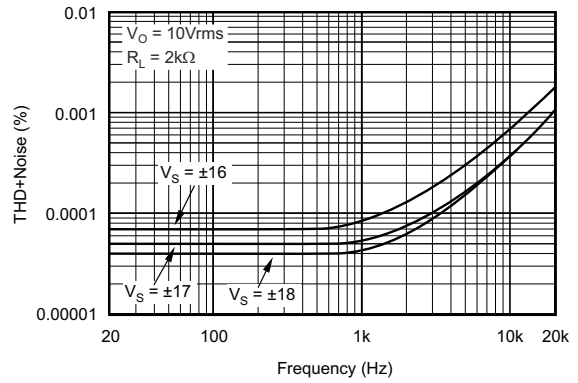


図 5-3. Total Harmonic Distortion + Noise vs Frequency

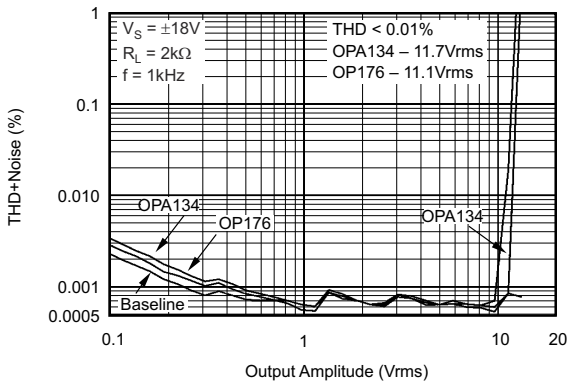


図 5-4. Headroom – Total Harmonic Distortion + Noise vs Output Amplitude

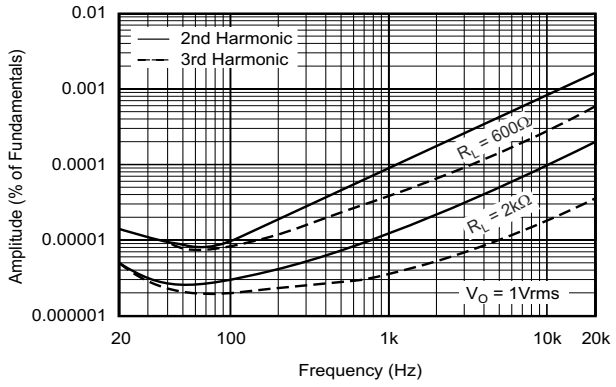


図 5-5. Harmonic Distortion + Noise vs Frequency

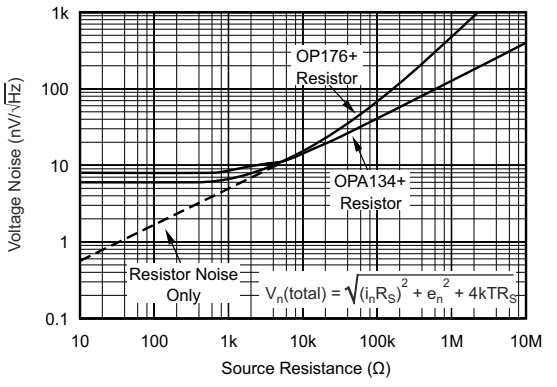


図 5-6. Voltage Noise vs Source Resistance

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

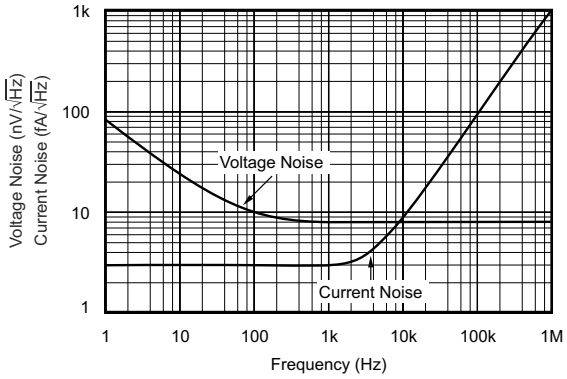


図 5-7. Input Voltage and Current Noise Spectral Density vs Frequency

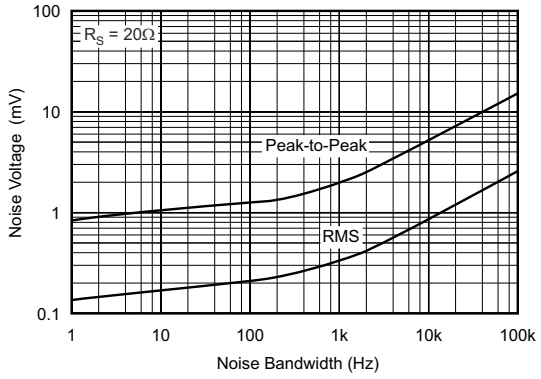


図 5-8. Input-Referred Noise Voltage vs Noise Bandwidth

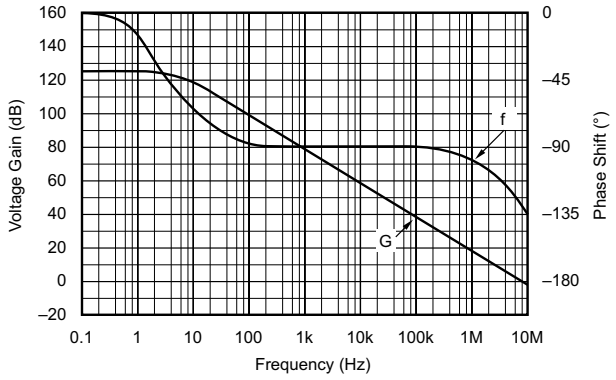


図 5-9. Open-Loop Gain and Phase vs Frequency

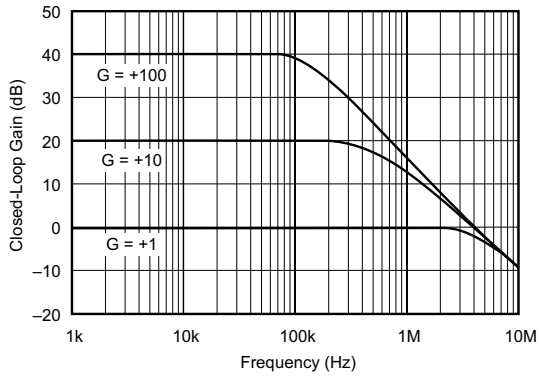


図 5-10. Closed-Loop Gain vs Frequency

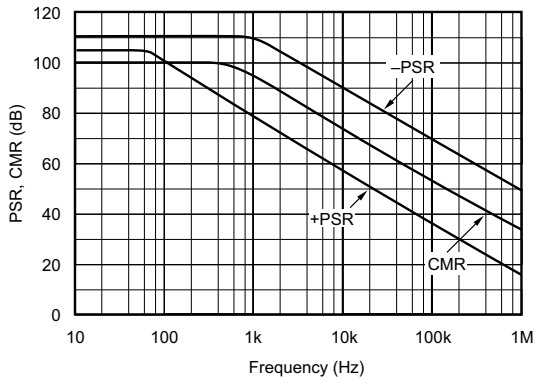


図 5-11. Power Supply and Common-Mode Rejection vs Frequency

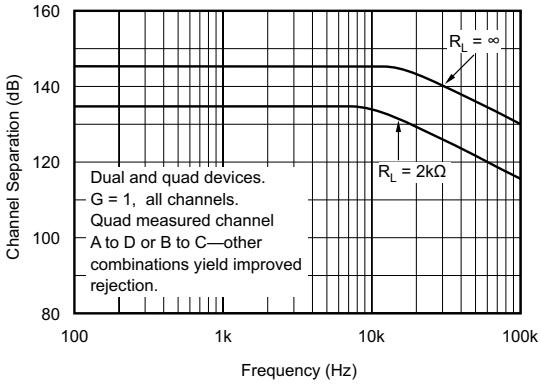


図 5-12. Channel Separation vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

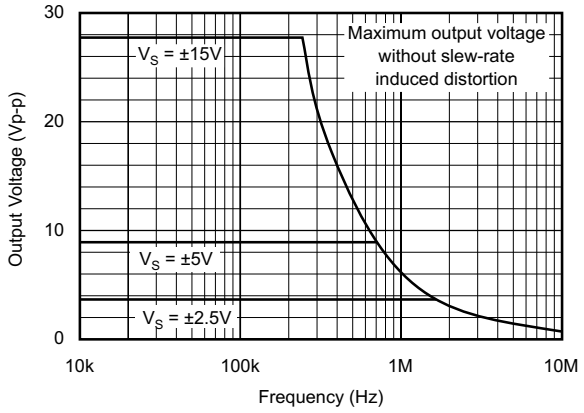


図 5-13. Maximum Output Voltage vs Frequency

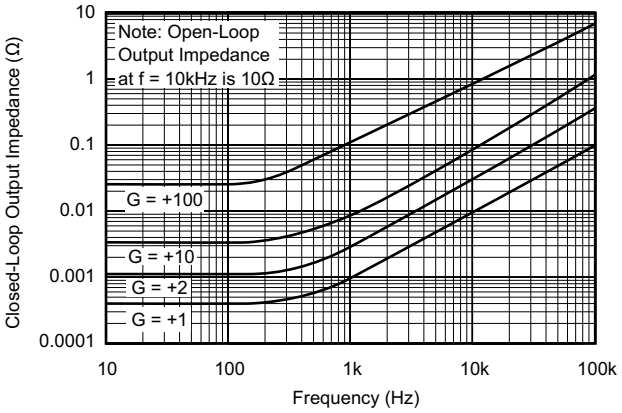


図 5-14. Closed-Loop Output Impedance vs Frequency

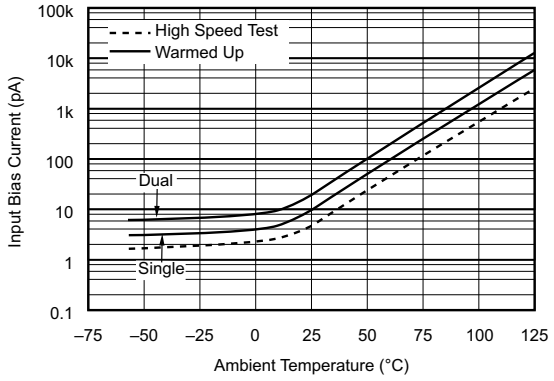


図 5-15. Input Bias Current vs Temperature

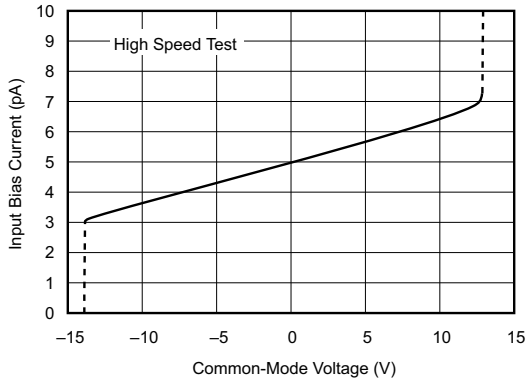


図 5-16. Input Bias Current vs Input Common-Mode Voltage

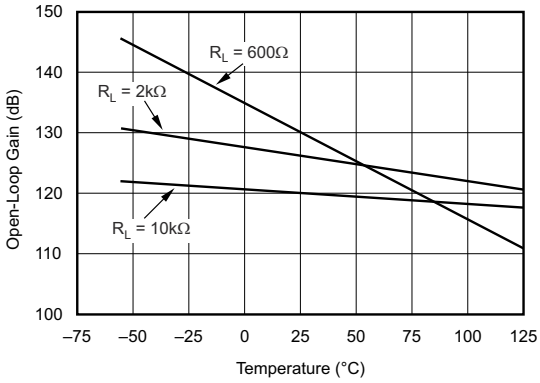


図 5-17. Open-Loop Gain vs Temperature

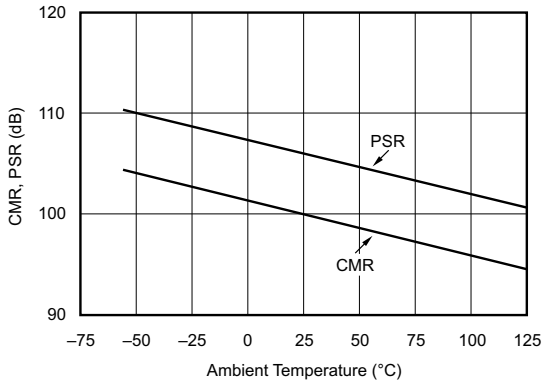


図 5-18. CMR, PSR vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

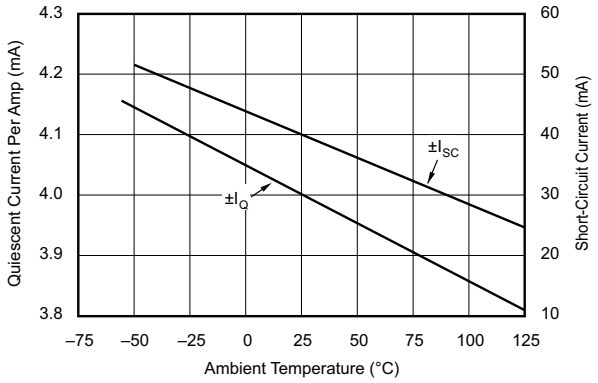


図 5-19. Quiescent Current and Short-Circuit Current vs Temperature

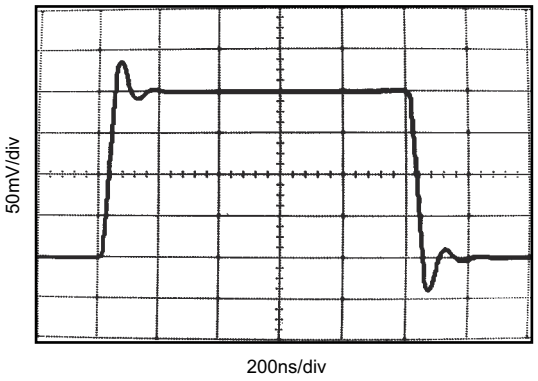


図 5-20. Small-Signal Step Response

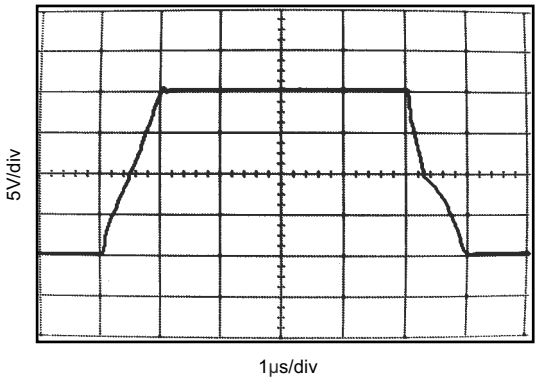


図 5-21. Large-Signal Step Response

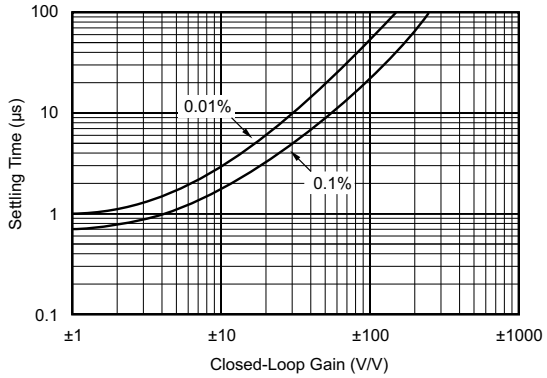
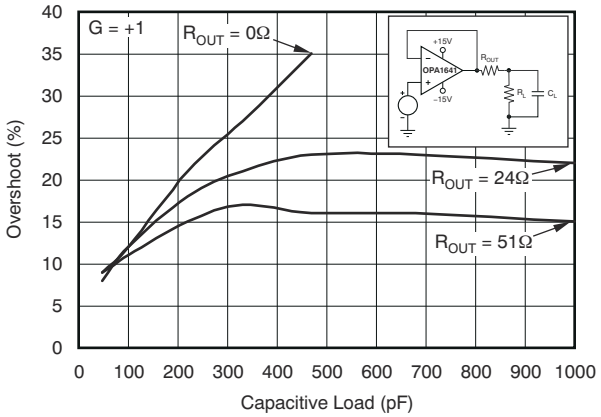
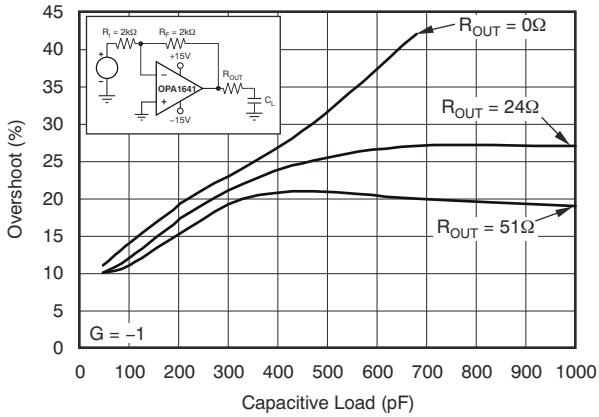


図 5-22. Settling Time vs Closed-Loop Gain



G = +1

図 5-23. Small-Signal Overshoot vs Load Capacitance



G = –1

図 5-24. Small-Signal Overshoot vs Load Capacitance

6 Detailed Description

6.1 Overview

The OPA134 series are ultra-low distortion, low-noise operational amplifiers fully specified for audio applications. A true FET input stage is incorporated to provide unmatched sound quality and speed for exceptional audio performance. This, in combination with high output drive capability and excellent DC performance, allows for use in a wide variety of demanding applications. In addition, the OPA134 has a wide output swing, to within 1V of the rails, allowing increased headroom and making this op amp an excellent choice for any audio circuit.

6.2 Feature Description

6.2.1 Total Harmonic Distortion

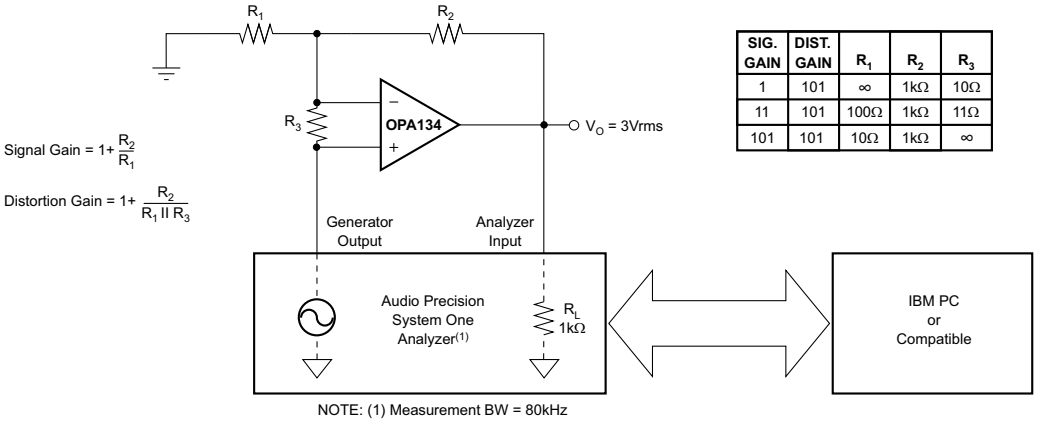
The OPAx134 series of operational amplifiers have excellent distortion characteristics. THD+Noise is below 0.0004% throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load. In addition, distortion remains relatively flat through the wide output voltage swing range, providing increased headroom compared to other audio amplifiers, including the OP176/275.

Headroom is a subjective measurement, and can be thought of as the maximum output amplitude allowed while still maintaining a low level of distortion. In an attempt to quantify headroom, TI defines very low distortion as 0.01%. Headroom is expressed as a ratio which compares the maximum allowable output voltage level to a standard output level (1mW into 600Ω, or 0.7746Vrms). Therefore, OPA134 series of operational amplifiers, which have a maximum allowable output voltage level of 11.7Vrms (THD+Noise < 0.01%), have a headroom specification of 23.6dBu. See 図 5-4.

6.2.2 Distortion Measurements

The distortion produced by OPAx134 series of operational amplifiers is below the measurement limit of all known commercially-available equipment. However, a special test circuit can extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source which can be referred to the input. 図 6-1 shows a circuit which causes the operational amplifier distortion to be 101 times greater than that which the operational amplifier normally produces. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. The input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. Keep the value of R_3 small to minimize effect on the distortion measurements.



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω
101	101	10Ω	1kΩ	∞

図 6-1. Distortion Test Circuit

This technique can be verified by duplicating measurements at high gain or high frequency, where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision distortion and noise analyzer, which greatly simplifies repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

6.2.3 Source Impedance and Distortion

For lowest distortion with a source or feedback network with an impedance greater than 2kΩ, match the impedance seen by the positive and negative inputs in noninverting applications. The p-channel JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage, because the inverting input is held at virtual ground. However, in noninverting applications the inputs do vary, and the gate-to-source voltage is not constant. The effect is increased distortion due to the varying capacitance for unmatched source impedances greater than 2kΩ.

To maintain low distortion, match unbalanced source impedance with the appropriate values in the feedback network as shown in 図 6-2. Of course, the unbalanced impedance can be from gain-setting resistors in the feedback path. If the parallel combination of R_1 and R_2 is greater than 2kΩ, use a matching impedance on the noninverting input. As always, minimize resistor values to reduce the effects of thermal noise.

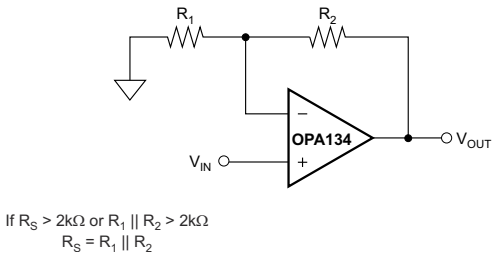


図 6-2. Impedance Matching for Maintaining Low Distortion in Noninverting Circuits

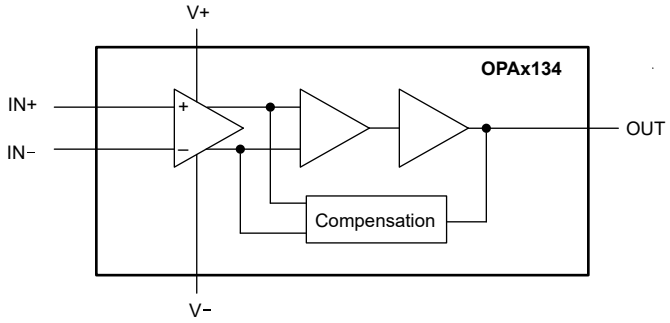
6.2.4 Phase Reversal Protection

The OPAx134 series of operational amplifiers are free from output phase-reversal problems. Many audio operational amplifiers, such as the OP176, exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPA134 series operational amplifiers are free from this undesirable behavior even with inputs of 10V beyond the input common-mode range.

6.2.5 Output Current Limit

Output current is limited by internal circuitry to approximately sourcing 36mA and sinking –30mA at 25°C. The limit current decreases with increasing temperature, as shown in 図 5-19.

6.3 Functional Block Diagram



6.4 Device Functional Modes

6.4.1 Noise Performance

Circuit noise is determined by the thermal noise of external resistors and operational amplifier noise. Operational amplifier noise is described by two parameters: noise voltage and noise current. The total noise is quantified by the equation:

$$V_n\left(total\right) = \sqrt{e_n^2 + \left(i_n R_S\right)^2 + 4kTR_S} \quad (1)$$

With low source impedance, the current noise term is insignificant and voltage noise dominates the noise performance. At high source impedance, the current noise term becomes the dominant contributor.

Low-noise bipolar operational amplifiers such as the OPA27 and OPA37 provide low voltage noise at the expense of a higher current noise. However, OPAx134 series operational amplifiers provide both low voltage noise and low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances; refer to 図 5-6. Above 2kΩ source resistance, the operational amplifier contributes little additional noise; the voltage and current terms in the total noise equation become insignificant and the source resistance term dominates. Below 2kΩ, operational amplifier voltage noise dominates over the resistor noise, but compares favorably with other audio operational amplifiers such as the OP176.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The OPAx134 series operational amplifiers are unity-gain stable, and an excellent choice for a wide range of audio and general-purpose applications. All circuitry is independent in the dual version, maintaining normal behavior when one amplifier in a package is overdriven or short-circuited. Bypass the power supply pins with 10nF ceramic capacitors or larger to minimize power supply noise.

7.1.1 Operating Voltage

The OPAx134 series of operational amplifiers operate with power supplies from ±2.5V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in *セクション 5.8*.

7.1.2 Offset Voltage Trim

Offset voltage of OPAx134 series amplifiers are laser-trimmed, and usually require no user adjustment. The OPAx134 provide less than ±2mV of input offset voltage and a typical input offset voltage drift of 10µV/°C over the operating temperature range.

7.2 Typical Application

The OPAx134 family offers outstanding dc precision and AC performance. These devices operate up to 36V supply rails and offer ultra-low distortion and noise, as well as 8MHz bandwidth and high capacitive load drive. These features make the OPAx134 a robust, high-performance operational amplifier for high-voltage professional audio applications.

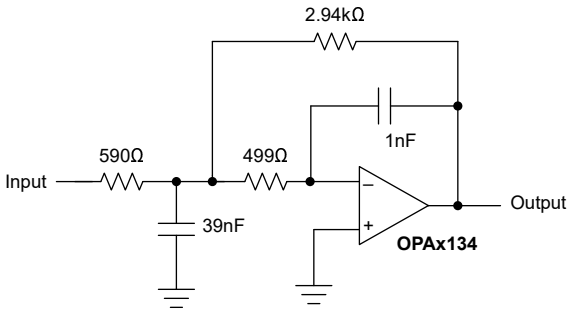


図 7-1. OPA134 2nd-Order, 30kHz, Low-Pass Filter Schematic

7.2.1 Design Requirements

- Gain = 5V/V (inverting)
- Low-pass cutoff frequency = 30kHz
- –40db/dec filter response
- Maintain less than 3dB gain peaking in the gain versus frequency response

7.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 図 7-1. The voltage transfer function is:

$$\frac{Output}{Input}(s) = \frac{\frac{-1}{R_1 R_3 C_2 C_5}}{s^2 + s\left(\frac{1}{C_2}\right)\left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_4}\right) + \left(\frac{1}{R_3 R_4 C_2 C_5}\right)} \tag{2}$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated using 式 3 and 式 4.

$$Gain = \frac{R_4}{R_1} \tag{3}$$

$$f_C = \frac{1}{2\pi}\sqrt{\frac{1}{R_3 R_4 C_2 C_5}} \tag{4}$$

WEBENCH® Circuit Designer creates customized power supply and active filter circuits based on your system requirements. The environment gives you end-to-end selection, design, and simulation capabilities that save you time during all phases of the analog design process.

Use our tools to help with your designs:

- Filter design tool
- Powerstage designer
- WEBENCH® Power designer
- PCB thermal calculator

7.2.3 Application Curve

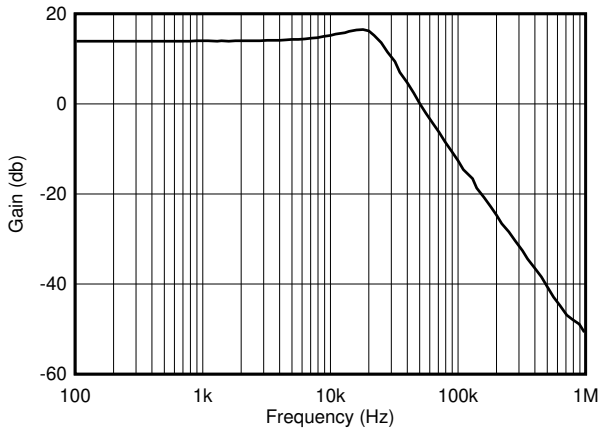


図 7-2. OPA134 2nd-Order, 30kHz, Low-Pass Filter Response

7.3 Power Supply Recommendations

The OPAx134 is specified for operation from 5V to 36V (±2.5V to ±18V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *セクション 5.8*.

> **注意**
>
> Supply voltages larger than 36V can permanently damage the device; see *セクション 5.1*.

Place 10nF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *セクション 7.4.1*.

7.4 Layout

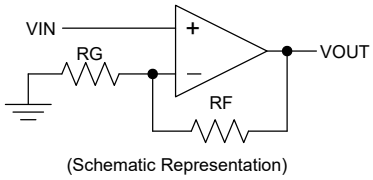
7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the operational amplifier and the power pins of the circuit as a whole. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 10nF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *セクション 7.4.2*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example



(Schematic Representation)

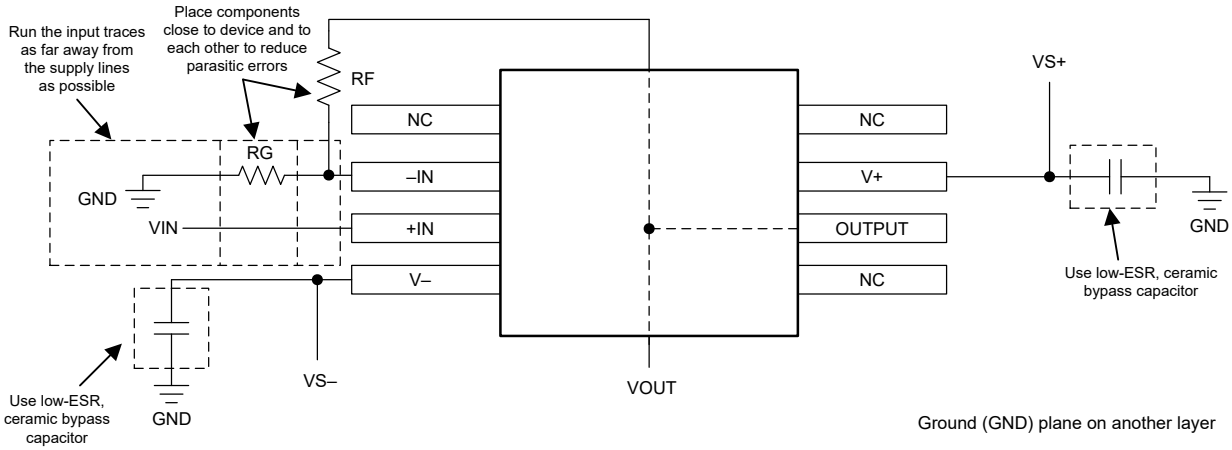


図 7-3. OPA134 Layout Example for the Noninverting Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Analog Filter Designer

Analog Filter Designer は、設計およびシミュレーション ツール Web ページから Web ベースのツールとして利用でき、包括的な複数段アクティブ フィルタ ソリューションの設計、最適化、シミュレーションをわずか数分で行います。

8.1.1.2 TINA-TI™シミュレーション ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション プログラムです。TINA-TI シミュレーション ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ モデルとアクティブ モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション ソフトウェアは設計およびシミュレーション ツール Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな形式で処理できる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック スタート ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア フォルダから、無償の TINA-TI シミュレーション ソフトウェアをダウンロードしてください。

8.1.1.3 TI のリファレンス・デザイン

TI のリファレンス・デザインは、TI の高精度アナログ・アプリケーション専門家により作成されたアナログ・ソリューションです。TI のリファレンス・デザインは、動作原理、部品の選択、シミュレーション、完全な PCB 回路図およびレイアウト、部品表、測定済みの性能を提供します。TI のリファレンス・デザインは、http://www.ti.com/ww/en/analog/precision-designs/ からオンラインで入手できます。

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following (available for download from www.ti.com):

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*
- Texas Instruments, *Circuit Board Layout Techniques*

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

SoundPlus™, TINA-TI™, and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2015) to Revision B (August 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」の開ループ ゲイン負荷条件を更新	1
• クワッド バージョン デバイスの PDIP パッケージ オプションを削除	1
• 「製品情報」表を更新	1
• 表紙の図で W の記号を Ω に変更 (誤字)	1
• Updated *Pin Configuration and Functions* format	3
• Changed OPA134 pin 1 and 8 from "Offset Trim" to "NC"	3
• Changed input voltage from (V–) – 0.7V to (V+) + 0.7V to (V–) – 0.5V to (V+) + 0.5V in *Absolute Maximum Ratings*	5
• Added input current and related footnote to *Absolute Maximum Ratings*	5
• Added *Thermal Information*	6
• Updated format of *Electrical Characteristics*	7
• Updated nominal conditions in the header of *Electrical Characteristics*	7
• Changed headroom from 23.6dB to 21.3dB	7
• Deleted slew rate MIN	7
• Changed overload recovery time from 0.5µs to 0.6µs	7
• Changed input offset voltage MIN from ±0.5mV to ±1mV and MAX from ±2mV to ±3.5mV	7
• Deleted input offset voltage over temperature MAX	7
• Changed channel separation from 135dB to 128dB for dc, and from 130dB to 126dB for f = 20kHz	7
• Deleted note 3	7
• Added ± to input bias current TYP	7
• Changed common-mode voltage MAX value from (V+) – 2.5V to (V+) – 3.5V	7
• Updated common-mode rejection ratio and common-mode input impedance test conditions	7
• Changed differential input impedance from $10^{13}\Omega$ || 2pF to $10^{13}\Omega$ || 8pF	7
• Changed common-mode input impedance from $10^{13}\Omega$ || 5pF to $10^{13}\Omega$ || 6pF	7
• Deleted open-loop voltage gain for R_L = 600Ω	7
• Deleted voltage output for R_L = 600Ω	7
• Moved voltage output negative MIN values to MAX values	7
• Deleted output current	7
• Deleted note 1 from *Electrical Characteristics*	7
• Changed typos in typical characteristic graphs; corrected ohms symbol (Ω) and radical symbol (√)	9
• Changed test condition for *Typical Characteristics* from V_S = 15V to V_S = ±15V (typo)	9
• Changed Figure 26, *Small-Signal Overshoot vs Load Capacitance* into new Figures 5-23 and 5-24	9
• Deleted old Figure 20, *Output Voltage Swing vs Output Current*, Figure 21, *Offset Voltage Production Distribution*, Figure 22, *Offset Voltage Drift Production Distribution*	9
• Updated *Functional Block Diagram*	15

- Updated *Offset Voltage Trim* 16
- Updated *OPA134 Layout Example for the Noninverting Configuration* 19

Changes from Revision * (September 2000) to Revision A (April 2015) **Page**

- ESD 定格の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA134PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	OPA134PA
OPA134PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA134PA
OPA134UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA
OPA134UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA
OPA134UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA
OPA134UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA
OPA2134PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2134PA
OPA2134PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2134PA
OPA2134PAG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	OPA2134PA
OPA2134UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA
OPA2134UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA
OPA2134UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA
OPA2134UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA
OPA4134UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA
OPA4134UA.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA
OPA4134UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA
OPA4134UA/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA
SN412008DRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

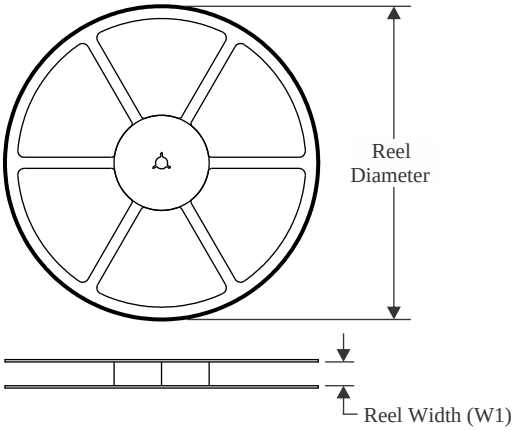
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

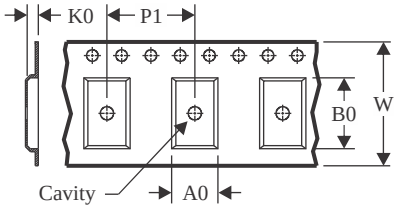
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

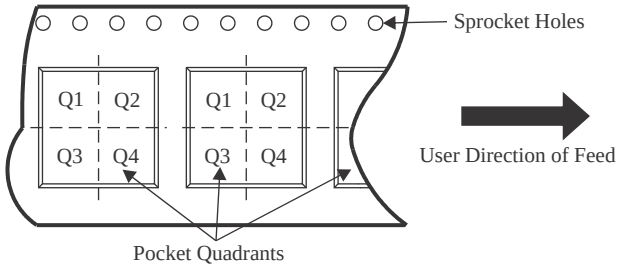


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

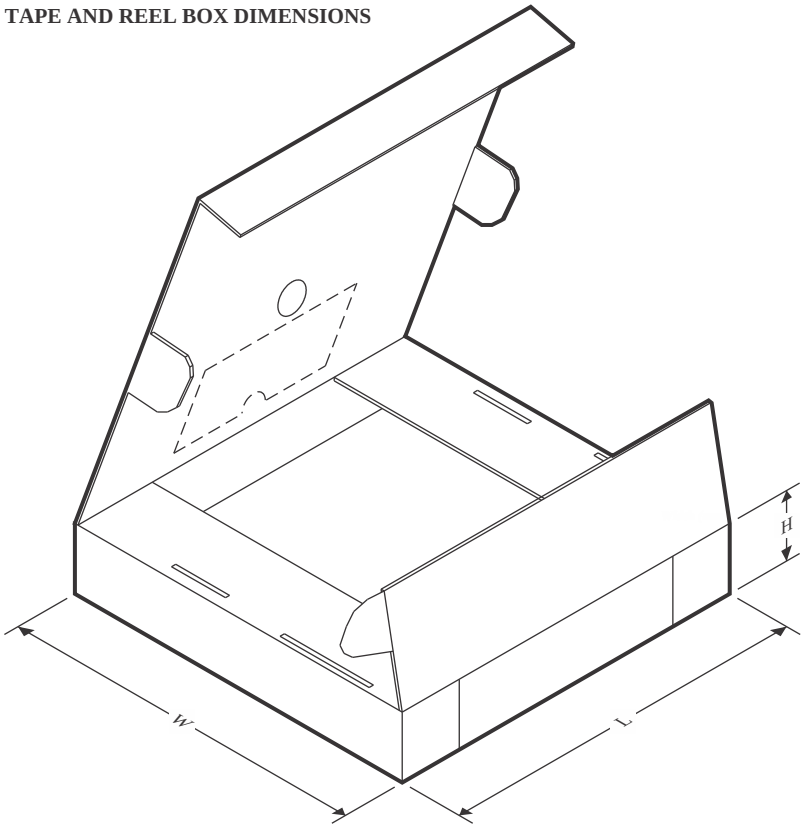
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4134UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

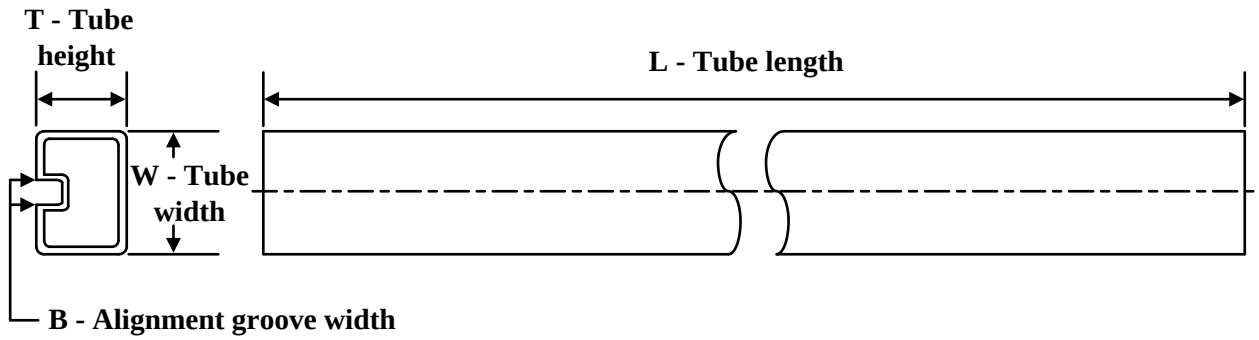
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

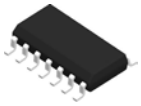
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA134UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA134UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2134UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2134UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4134UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA134PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA134PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA134UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA134UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2134PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2134PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA2134PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2134UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2134UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4134UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4134UA.B	D	SOIC	14	50	506.6	8	3940	4.32

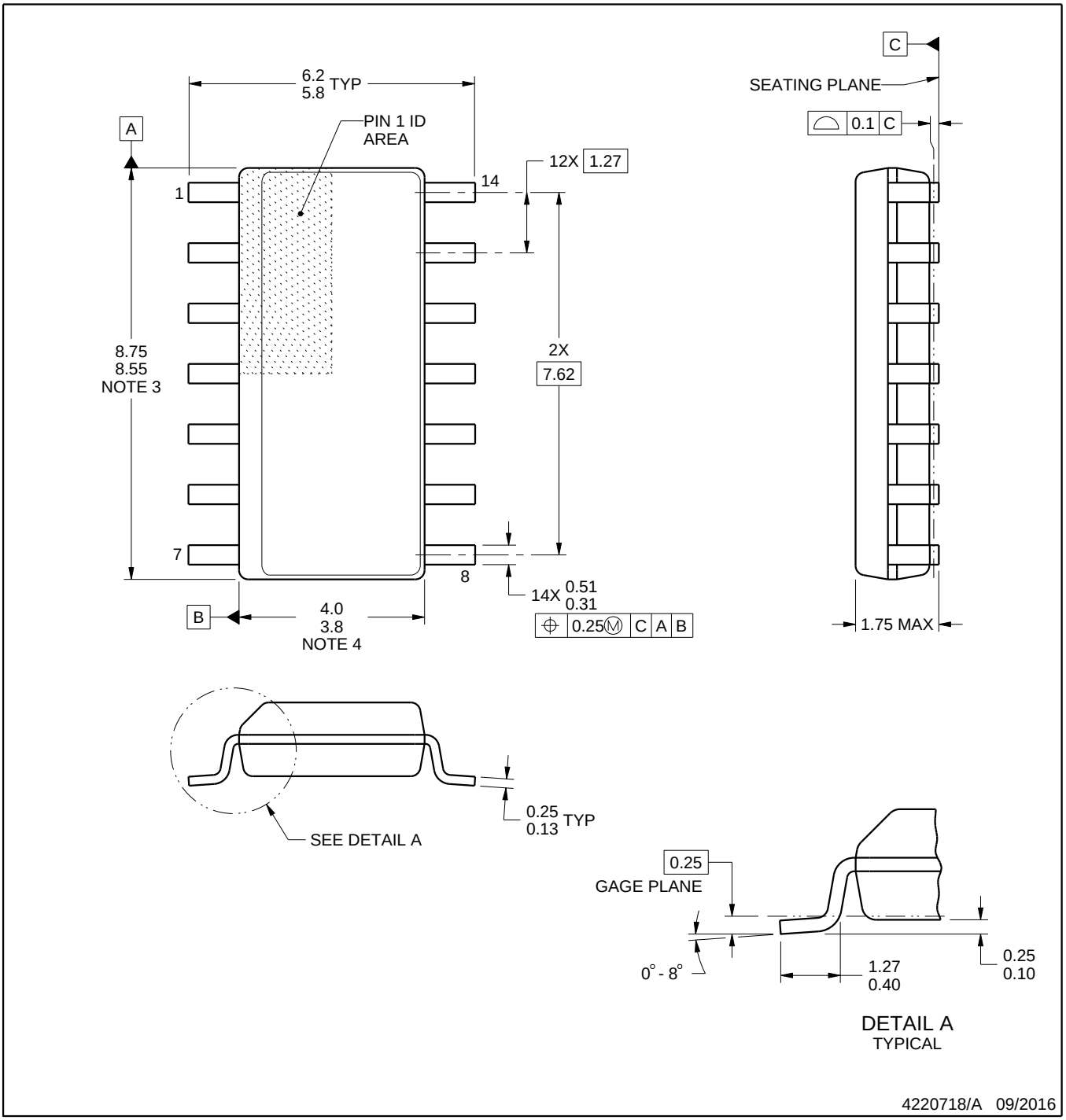


PACKAGE OUTLINE

D0014A

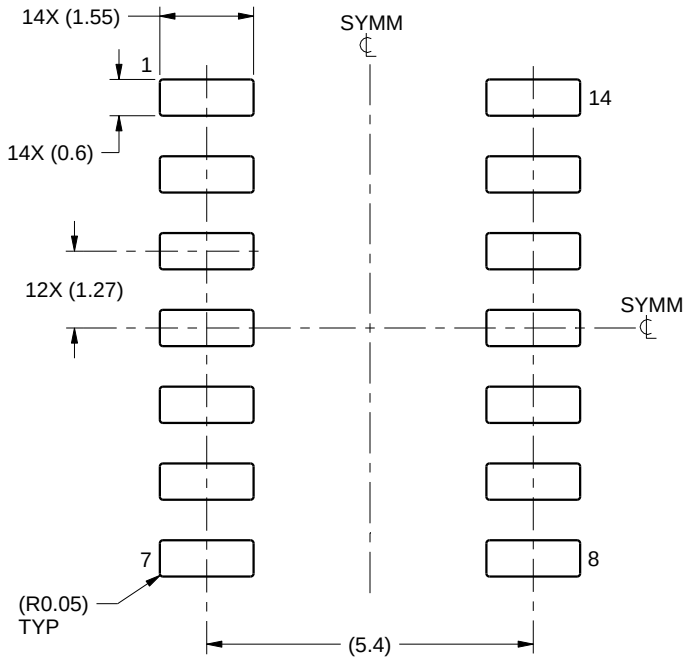
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

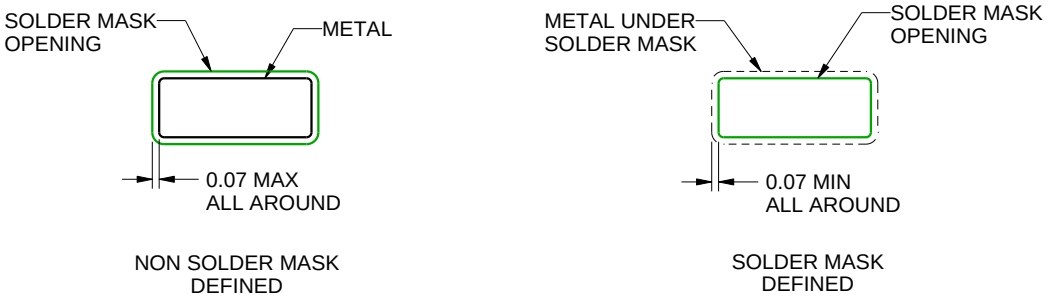


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

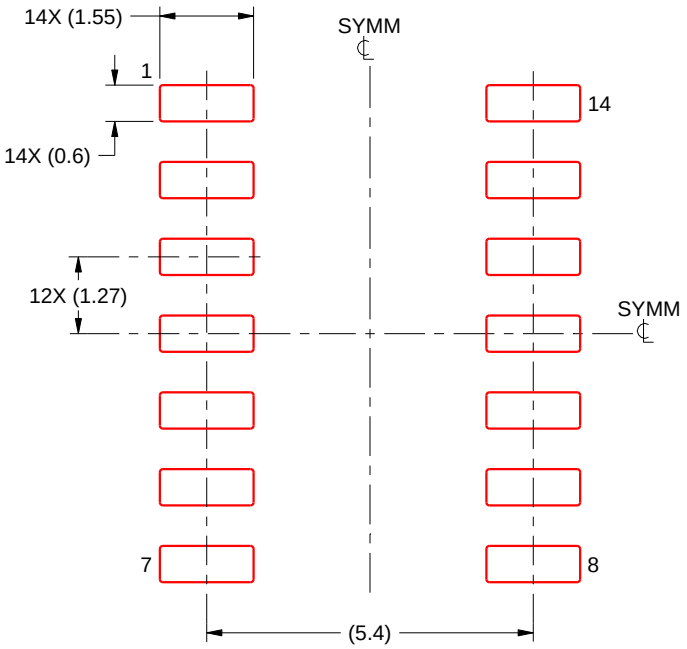
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

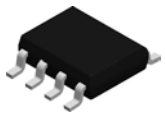


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

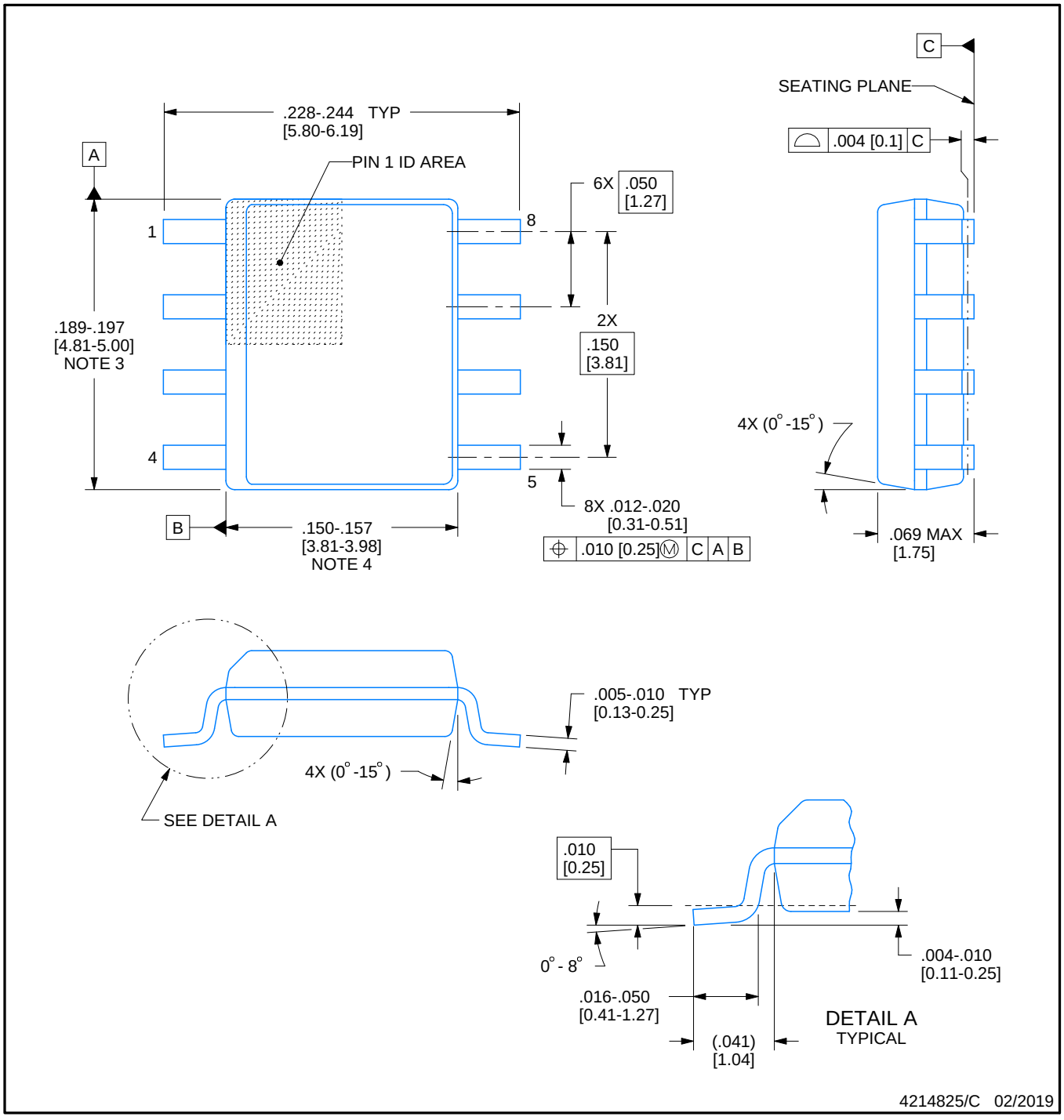


PACKAGE OUTLINE

D0008A

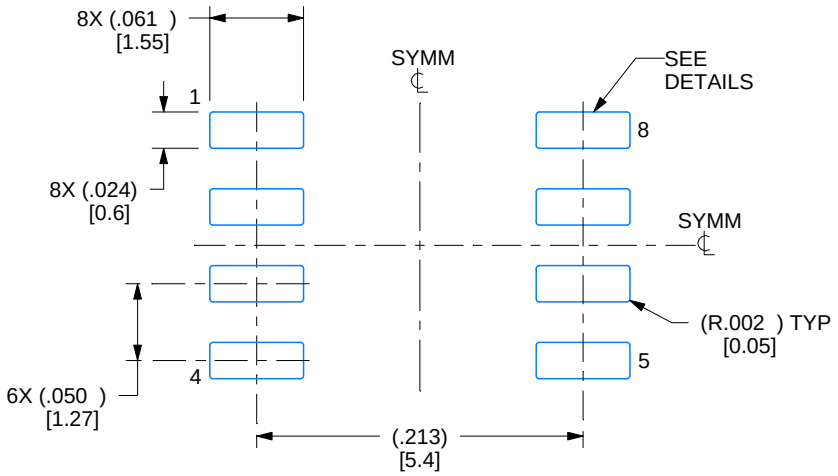
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

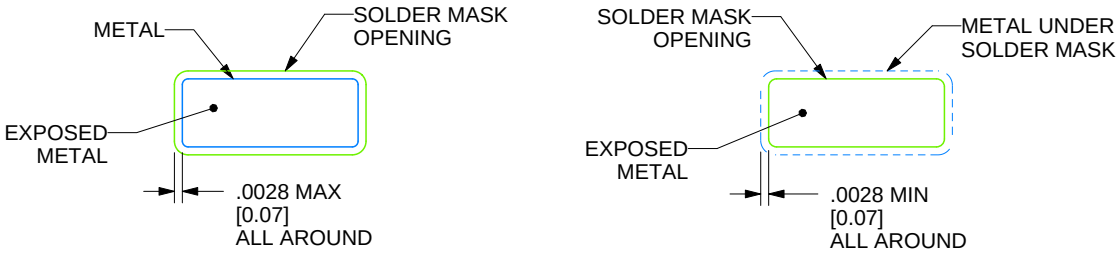


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

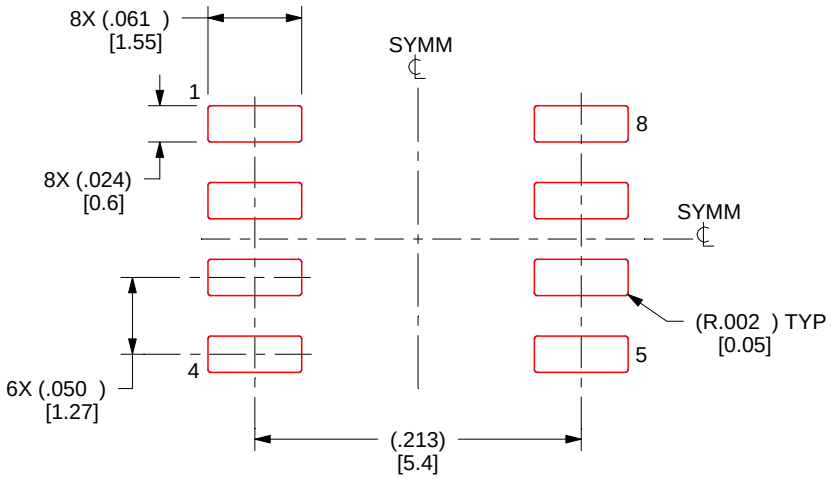
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



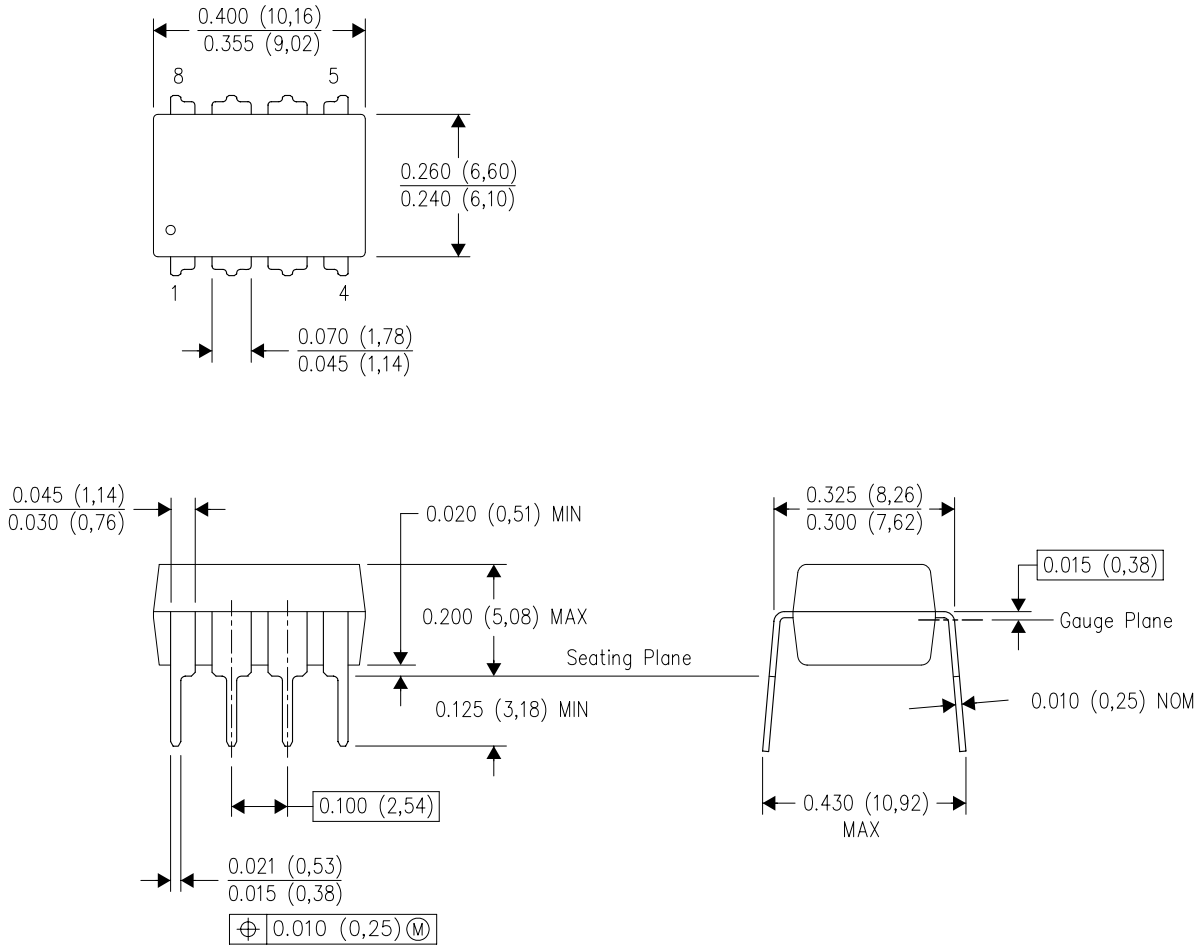
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265