OPAx314-Q1 3-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade : –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C6
- Low I_Q: 150 µA/ch
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 14 nV/√Hz at 1 kHz
- Gain Bandwidth: 3 MHz
- Low Input Bias Current: 0.2 pA
- Low Offset Voltage: 0.5 mV
- Unity-Gain Stable
- Internal RF and EMI Filter
- Specified Temperature Range: –40°C to +125°C

2 Applications

- Automotive Applications:
  - ADAS
  - Body Electronics and Lighting
  - Current Sensing
  - Battery Monitoring

3 Description

The OPAx314-Q1 series is a family of single–, and dual–, and quad-channel operational amplifiers (op amps) that represents a new generation of low-power, general-purpose CMOS amplifiers. Rail-to-rail input and output swings, low quiescent current (150 µA typically at 5 V_S) combined with a wide bandwidth of 3 MHz, and very low noise (14 nV/√Hz at 1 kHz) make this device family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low-input bias current supports applications with megaohm source impedances.

The robust design of the OPAx314-Q1 series provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 300 pF, an integrated RF and EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

The device is optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and is specified over the full extended temperature range of –40°C to +125°C.

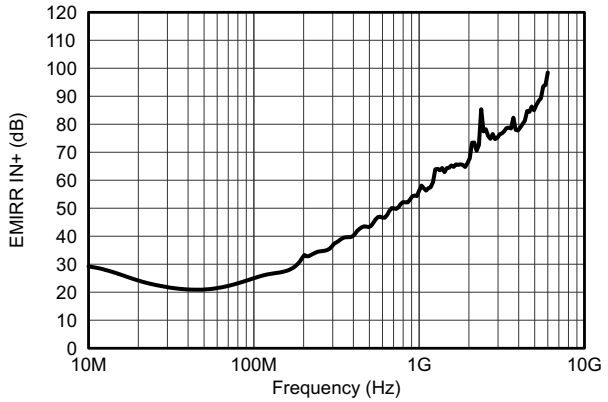
The single-channel device, OPA314-Q1, is offered in the SOT-23 package and the dual-channel device, OPA2314-Q1, is offered in the VSSOP (8) package. The quad-channel OPA4314-Q1 is available in the 14-pin TSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA314-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2314-Q1	VSSOP (8)	4.90 mm × 3.91 mm
OPA4314-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

EMIRR vs Frequency



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4 Revision History

Changes from Revision A (January 2015) to Revision B **Page**

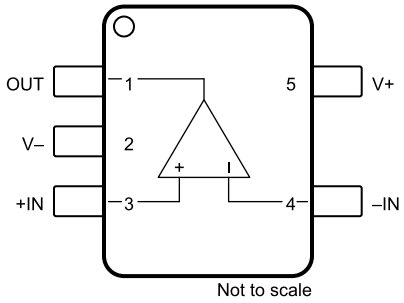
- Added part number OPA4314-Q1 to document ... 1
- Added part number OPA4314-Q1 to the *Device Information* table ... 1
- Changed OPA2314-Q1 package from SOIC (8) to VSSOP (8) in the *Device Information* table ... 1
- Added OPA314-Q1 (SOT-23 package) throughout document ... 3
- Added pinout drawing for the OPA4314-Q1 device in the *Pin Configurations and Functions* section ... 5
- Added the Pin Functions: OPA4314-Q1 table to the *Pin Configurations and Functions* section ... 5
- Changed formatting of all *Thermal Information* table notes ... 7
- Added footnotes to all *Thermal Information* tables ... 7
- Added *Thermal Information: OPA4314-Q1* table ... 9
- Changed formatting of application report reference in the *EMI Susceptibility and Input Filtering* section ... 20
- Changed package drawing to reflect an example of the 5-pin SOT-23 package in the *Layout Example* section ... 26
- Changed formatting of *Related Documentation* section ... 27
- Added part number OPA4314-Q1 to the *Related Links* table ... 27

Changes from Original (December 2014) to Revision A **Page**

- Changed the device status from *Product Preview* to *Production Data* ... 1

5 Pin Configuration and Functions

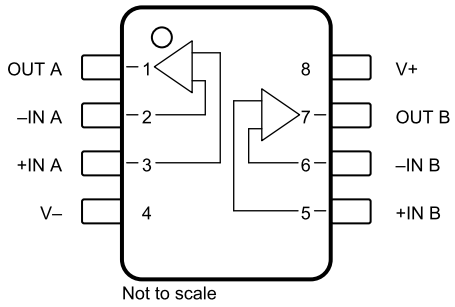
OPA314-Q1 DBV Package
5-Pin SOT-23
Top View



Pin Functions: OPA314-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative supply or ground (for single-supply operation).
V+	5	—	Positive supply

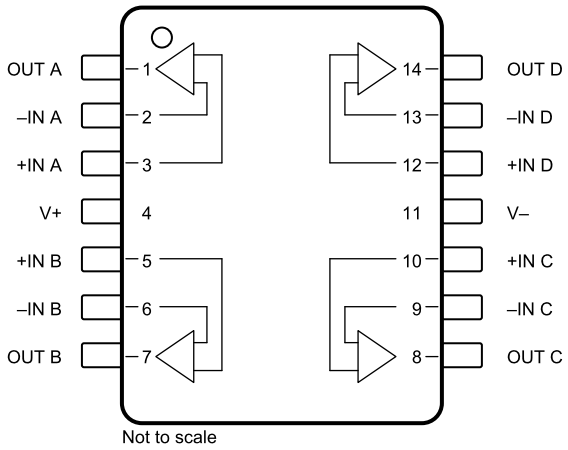
OPA2314-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2314-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative supply or ground (for single-supply operation).
V+	8	—	Positive supply

OPA4314-Q1 DGK Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions: OPA4314-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative supply or ground (for single-supply operation).
V+	4	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage			7	V
Voltage(2)	Signal input terminals	(V–) – 0.5	(V+) + 0.5	V
Current(2)	Signal input terminals		±10	mA
Output short-circuit(3)		Continuous		mA
Operating temperature, T_A		–40	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8 (±0.9)		5.5 (±2.75)	V
T_A	Ambient operating temperature	–40		125	°C

6.4 Thermal Information: OPA314-Q1

THERMAL METRIC[1]		OPA314-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	221.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	144.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	26.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	49	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Thermal Information: OPA2314-Q1

THERMAL METRIC[1]		OPA2314-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	138.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	89.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	78.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	29.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	78.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.6 Thermal Information: OPA4314-Q1

THERMAL METRIC(1)		OPA4314-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance(7)	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, V_S = 1.8 V to 5.5 V, unless otherwise noted. The phrase *overtemperature* refers to values over the specified temperature range of T_A = –40°C to 125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V_S+) – 1.3 V		0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature			1		µV/°C
PSRR	vs power supply	V_{CM} = (V_S+) – 1.3 V	78	92		dB
	Input offset voltage overtemperature		74			dB
	Channel separation, DC	At DC		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V to 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	75	96		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V (2)	66	80		dB
	Common-mode rejection ratio overtemperature	V_S = 1.8 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	70	86		dB
		V_S = 5.5 V, (V_S–) – 0.2 V < V_{CM} < (V_S+) – 1.3 V	73	90		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V (2)	60			dB
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
	Input bias current overtemperature				±600	pA
I_{OS}	Input offset current			±0.2	±10	pA
	Input offset current overtemperature				±600	pA
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5		$µV_{PP}$
e_n	Input voltage noise density	f = 10 kHz		13		$nV/\sqrt{Hz}$
		f = 1 kHz		14		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		5		$fA/\sqrt{Hz}$

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Overtemperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.

Electrical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, V_S = 1.8 V to 5.5 V, unless otherwise noted. The phrase *overtemperature* refers to values over the specified temperature range of T_A = –40°C to 125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CAPACITANCE						
C_{IN}	Differential	V_S = 5 V		1		pF
	Common-mode	V_S = 5 V		5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	90	115		dB
		V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	100	128		dB
		V_S = 1.8 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	90	100		dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ(2)	94	110		dB
	Open-loop voltage gain overtemperature	V_S = 5.5 V, 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	90	110		dB
		V_S = 5.5 V, 0.5 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ		100		dB
	Phase margin	V_S = 5 V, G = 1, R_L = 10 kΩ		65		degrees
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 1.8 V, R_L = 10 kΩ, C_L = 10 pF		2.7		MHz
		V_S = 5 V, R_L = 10 kΩ, C_L = 10 pF		3		MHz
SR	Slew rate (3)	V_S = 5 V, G = 1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1		2.3		µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1		3.1		µs
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S		5.2		µs
THD+N	Total harmonic distortion + noise (4)	V_S = 5 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.001%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ		5	15	mV
		V_S = 5.5 V, R_L = 10 kΩ		5	20	mV
		V_S = 1.8 V, R_L = 2 kΩ		15	30	mV
		V_S = 5.5 V, R_L = 2 kΩ		22	40	mV
	Voltage output swing from supply rails overtemperature	V_S = 5.5 V, R_L = 10 kΩ			30	mV
		V_S = 5.5 V, R_L = 2 kΩ		60		mV
I_{SC}	Short-circuit current	V_S = 5 V		±20		mA
R_O	Open-loop output impedance	V_S = 5.5 V, f = 100 Hz		570		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 1.8 V, I_O = 0 mA		130	180	µA
		V_S = 5 V, I_O = 0 mA		150	190	µA
	Quiescent current per amplifier overtemperature	V_S = 5 V, I_O = 0 mA			220	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		44		µs
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C
	Storage range		–65		150	°C

(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

6.8 Typical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted

Table 1. Characteristic Performance Measurements

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Open-Loop Gain and Phase vs Frequency	Figure 1
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EMIRR	Figure 32

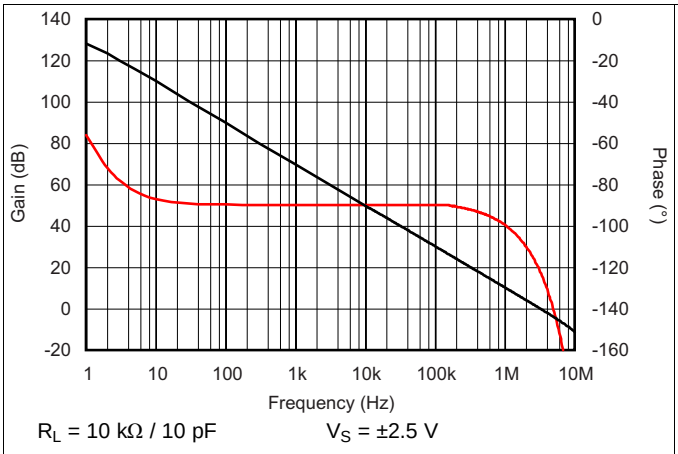


Figure 1. Open-loop Gain and Phase vs Frequency

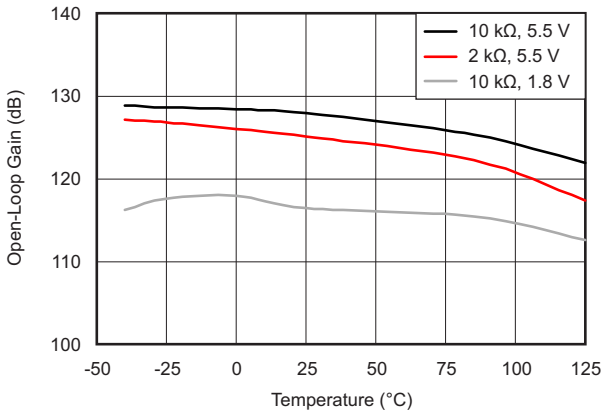


Figure 2. Open-Loop Gain vs Temperature

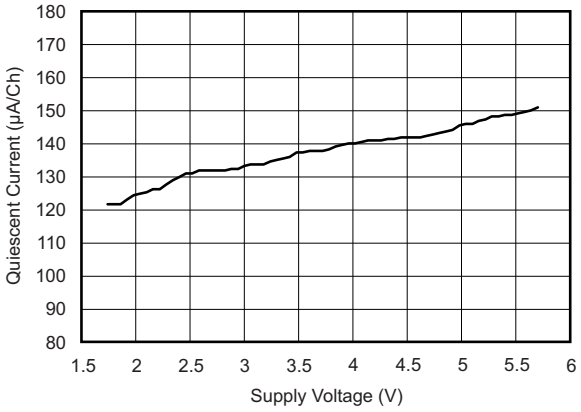


Figure 3. Quiescent Current vs Supply

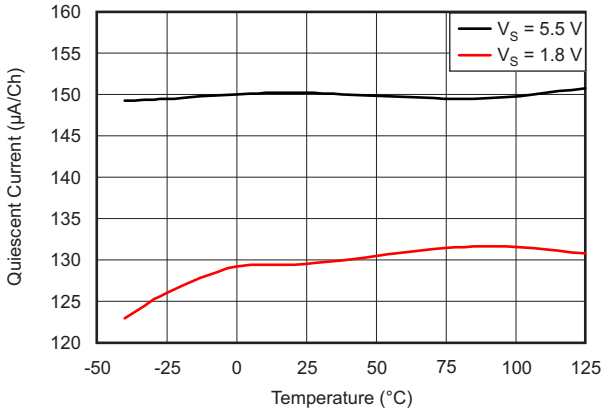


Figure 4. Quiescent Current vs Temperature

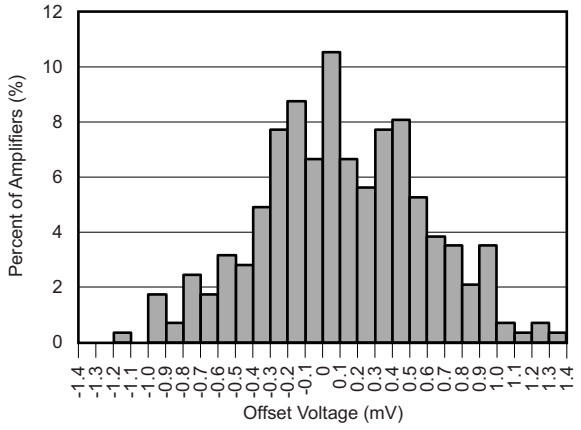


Figure 5. Offset Voltage Production Distribution

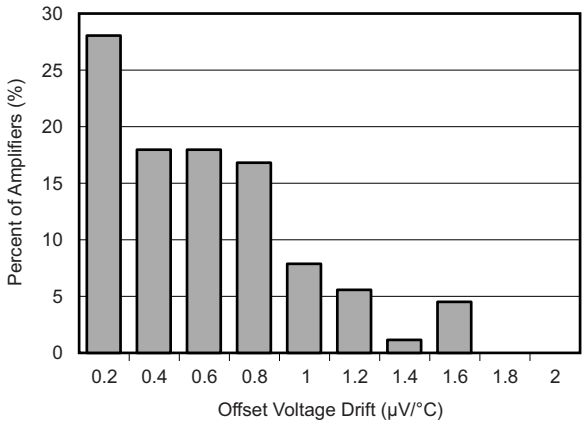


Figure 6. Offset Voltage Drift Distribution

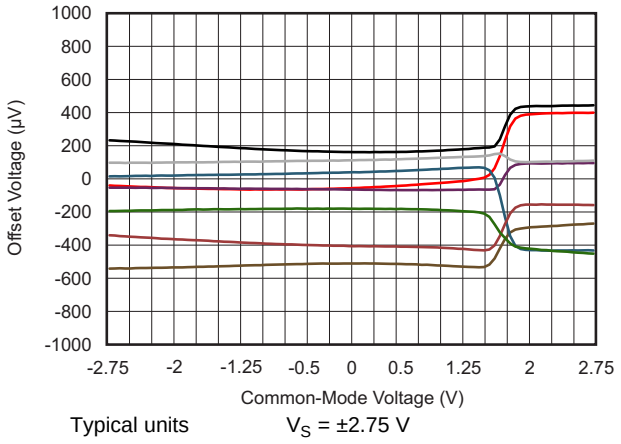


Figure 7. Offset Voltage vs Common-Mode Voltage

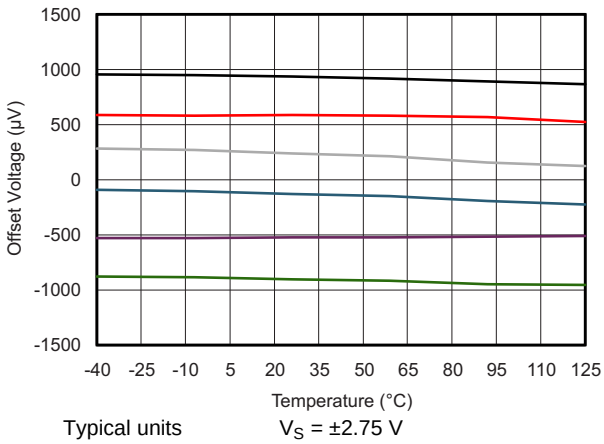


Figure 8. Offset Voltage vs Temperature

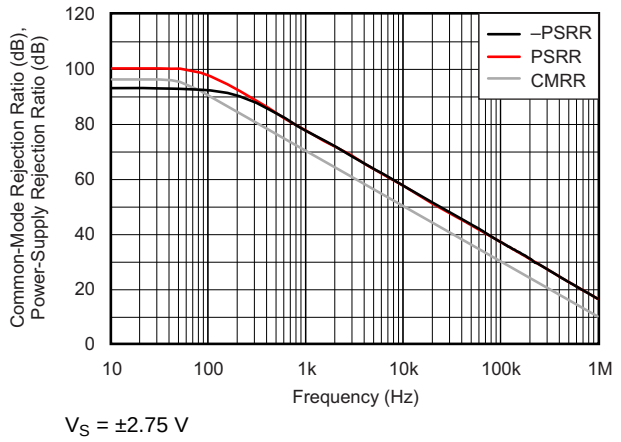


Figure 9. CMRR and PSRR vs Frequency (Referred-to-Input)

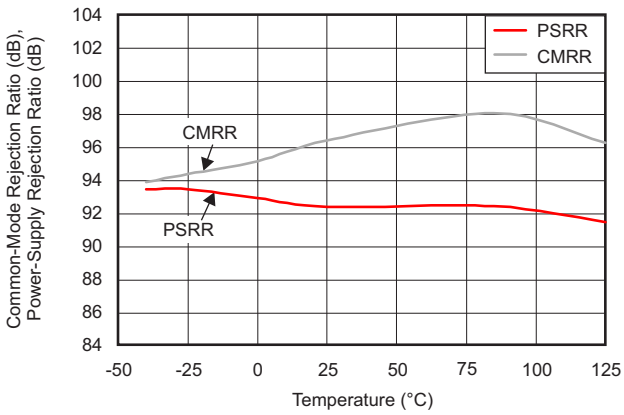


Figure 10. CMRR and PSRR vs Temperature

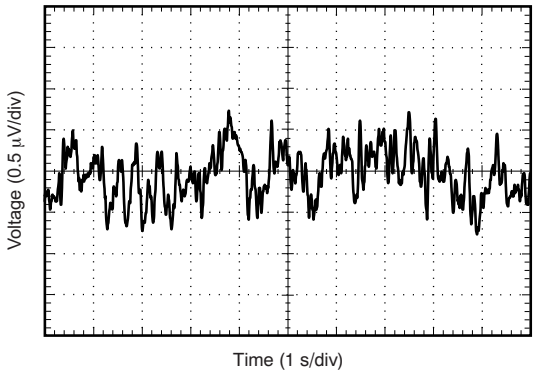


Figure 11. 0.1-Hz to 10-Hz Input Voltage Noise

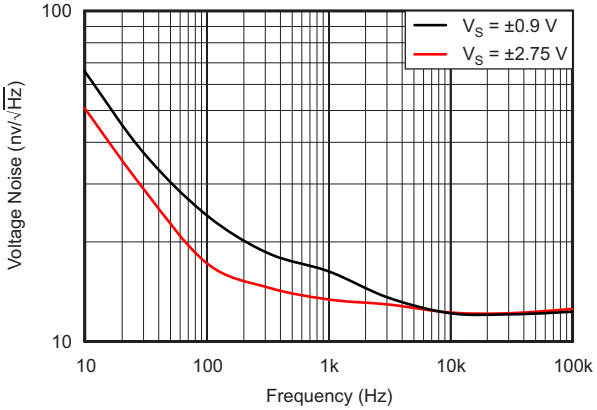


Figure 12. Input Voltage Noise Spectral Density vs Frequency

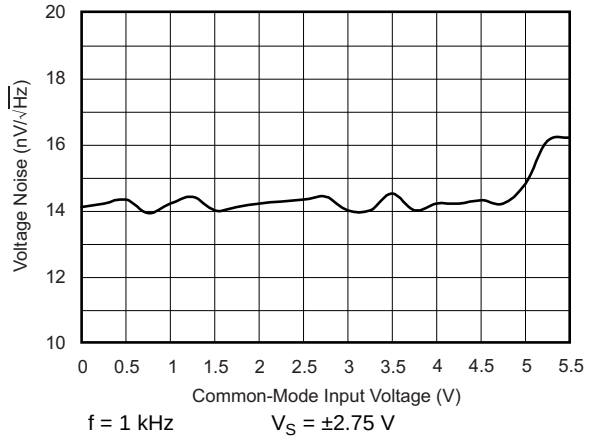


Figure 13. Voltage Noise vs Common-Mode Voltage

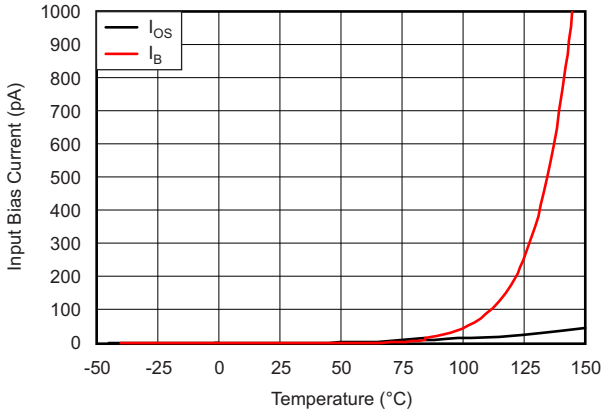


Figure 14. Input Bias and Offset Current vs Temperature

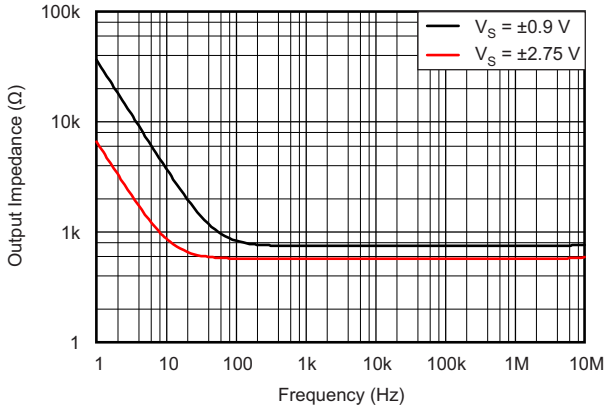


Figure 15. Open-Loop Output Impedance vs Frequency

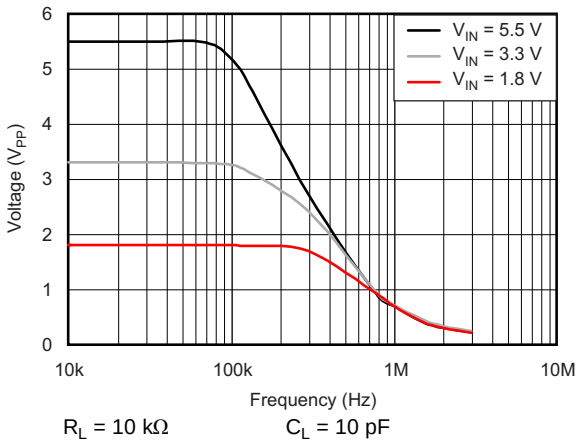


Figure 16. Maximum Output Voltage vs Frequency and Supply Voltage

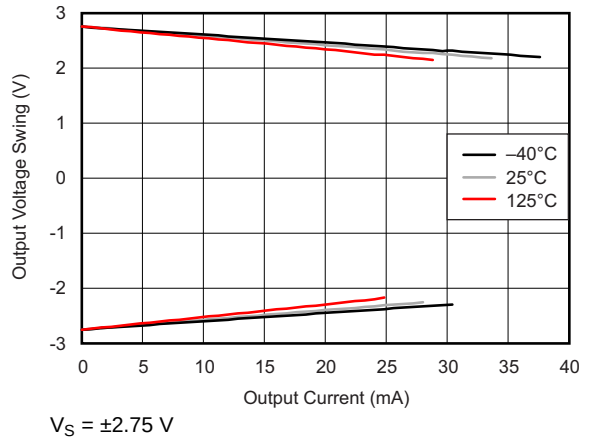


Figure 17. Output Voltage Swing vs Output Current (Overtemperature)

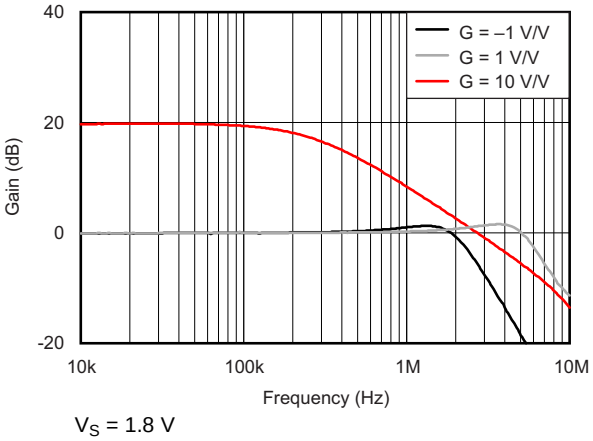
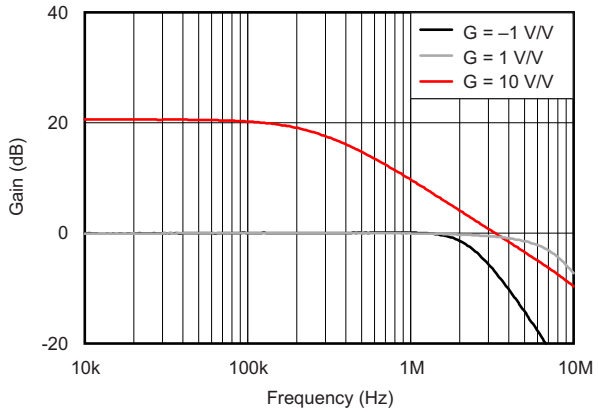
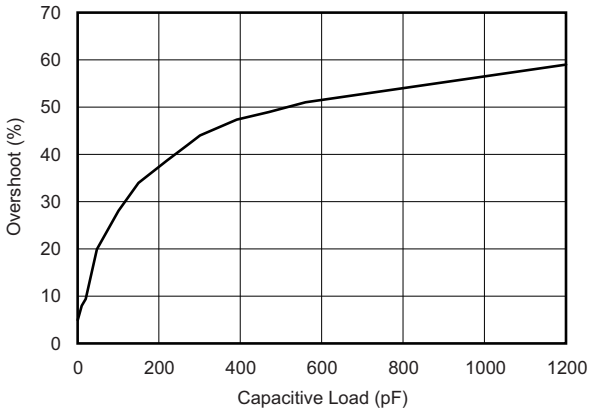


Figure 18. Closed-Loop Gain vs Frequency



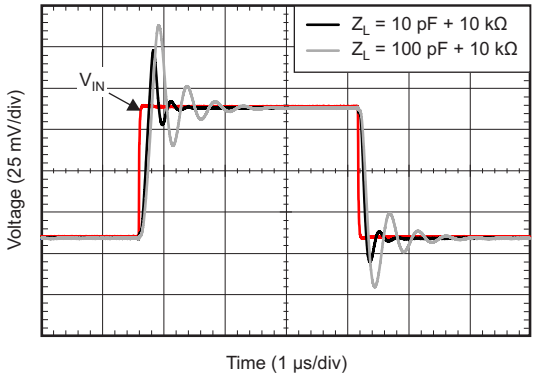
V_S = 5.5 V

Figure 19. Closed-Loop Gain vs Frequency



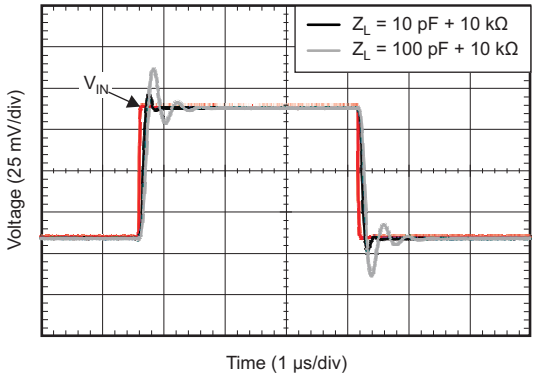
R_L = 10 kΩ V_S = ±2.75 V G = 1 V/V

Figure 20. Small-Signal Overshoot vs Load Capacitance



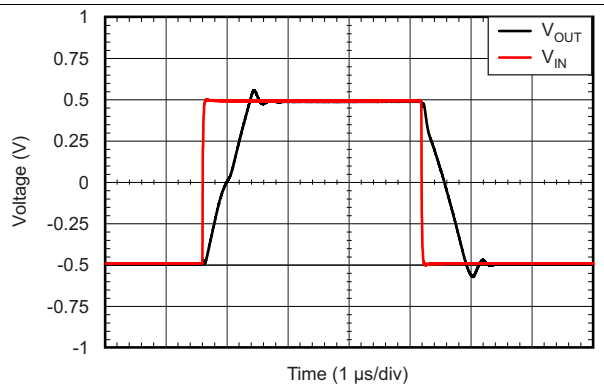
R_F = 10 kΩ V_S = ±0.9 V G = 1 V/V

Figure 21. Small-Signal Pulse Response (Noninverting)



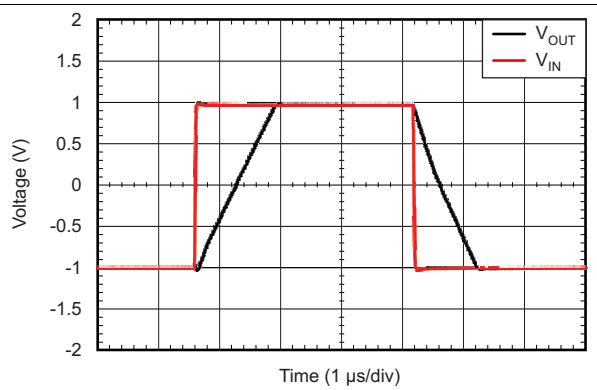
R_F = 10 kΩ V_S = ±2.75 V G = 1 V/V

Figure 22. Small-Signal Pulse Response (Inverting)



R_L = 10 kΩ V_S = ±0.9 V G = 1 V/V

Figure 23. Large-Signal Pulse Response (Noninverting)



R_L = 10 kΩ V_S = ±2.75 V G = 1 V/V

Figure 24. Large-Signal Pulse Response (Inverting)

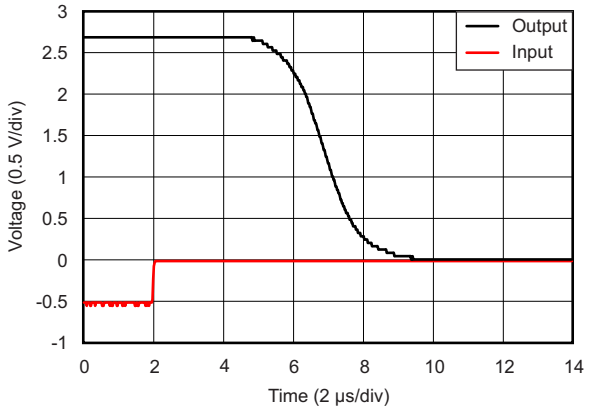


Figure 25. Positive Overload Recovery

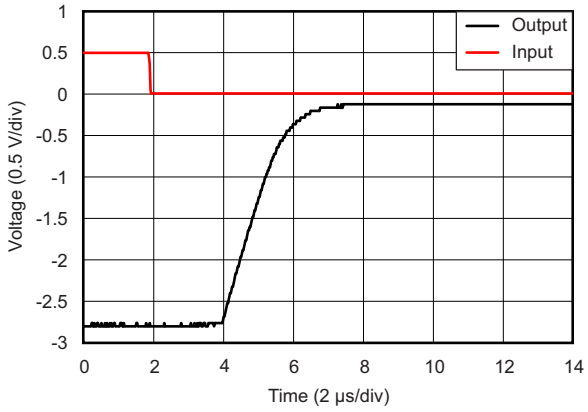


Figure 26. Negative Overload Recovery

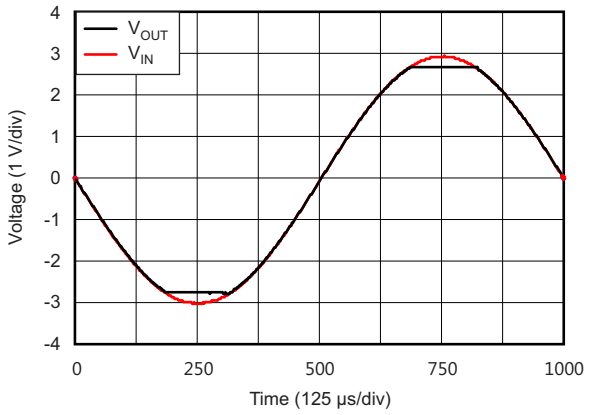
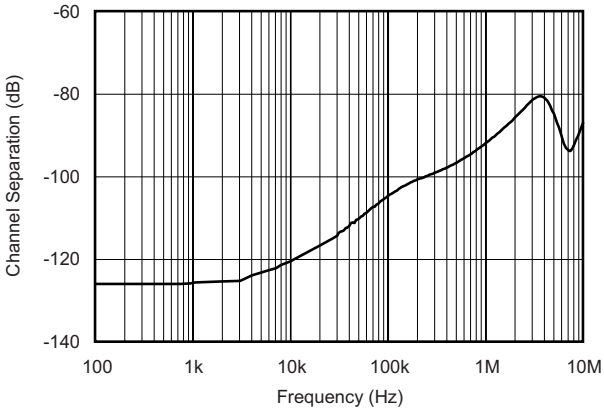
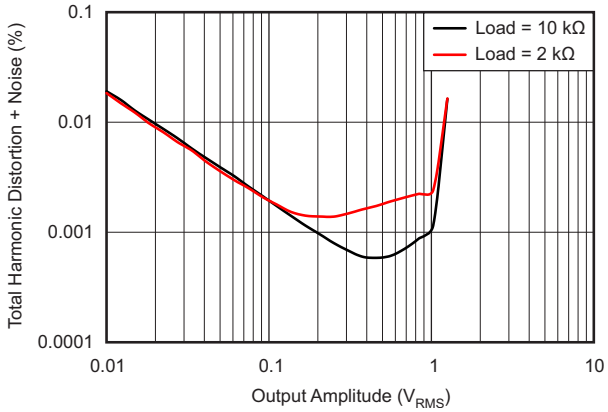


Figure 27. No Phase Reversal



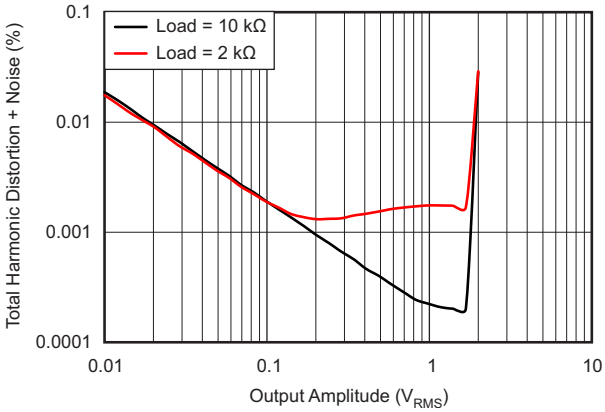
V_S = ±2.75 V

Figure 28. Channel Separation vs Frequency



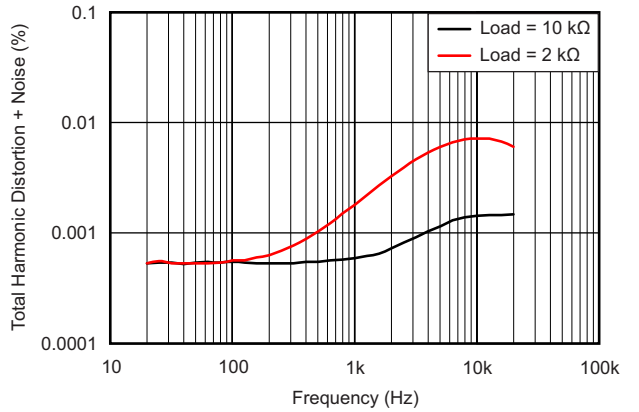
f = 1 kHz V_S = ±2.5 V G = 1 V/V
BW = 80 kHz

Figure 29. THD+N vs Output Amplitude (G = 1 V/V)



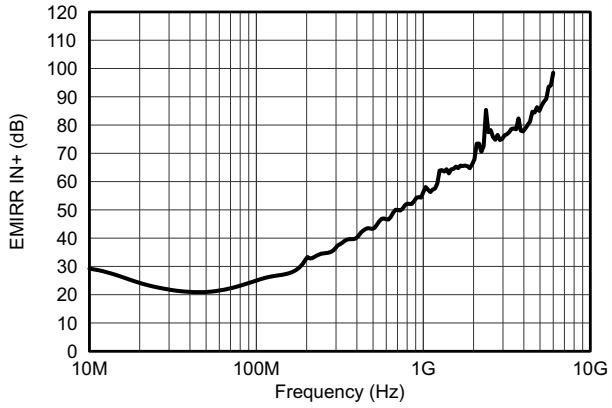
f = 1 kHz V_S = ±2.5 V G = –1 V/V
BW = 80 kHz

Figure 30. THD+N vs Output Amplitude (G = –1 V/V)



V_{OUT} = 0.5 V_{RMS} V_S = ±2.5 V G = 1 V/V
BW = 80 kHz

Figure 31. THD+N vs Frequency



P_{RF} = –10 dBm V_S = ±2.5 V V_{CM} = 0 V

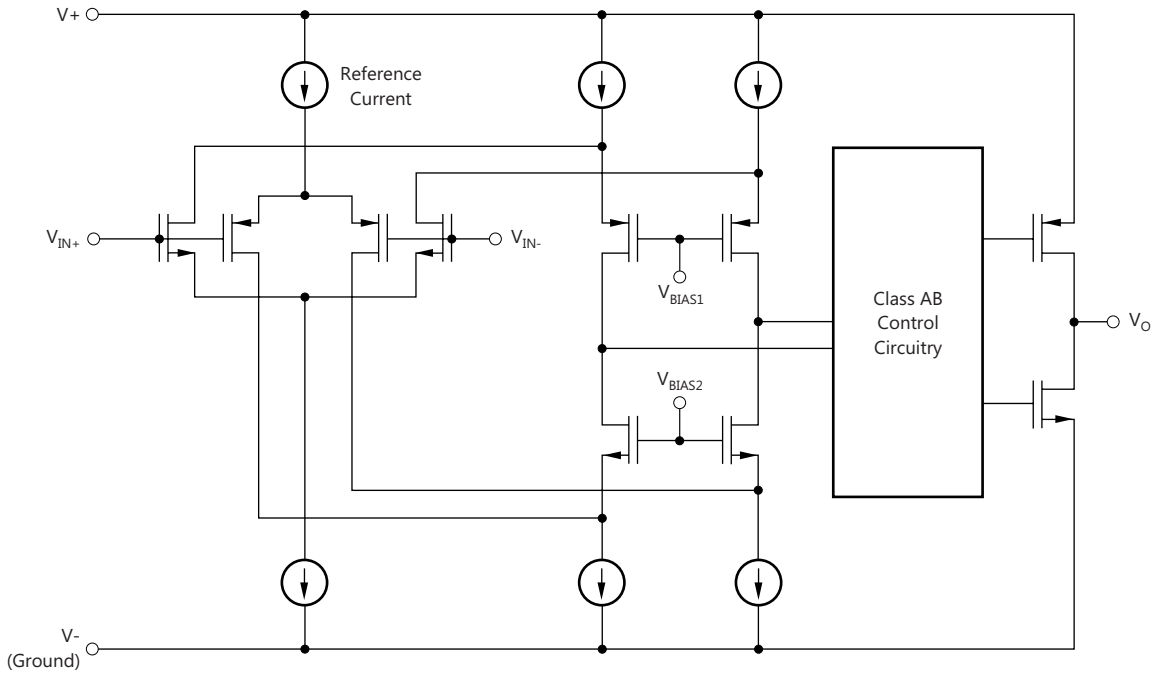
Figure 32. Electromagnetic Interference Rejection Ratio Referred To Noninverting Input (EMIRR IN+) vs Frequency

7 Detailed Description

7.1 Overview

The OPAx314-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPAx314-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx314-Q1 op-amp family is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* section. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx314-Q1 family extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply. The P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. A small transition region exists, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

Feature Description (continued)

7.3.3 Input and ESD Protection

The OPAx314-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 33 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

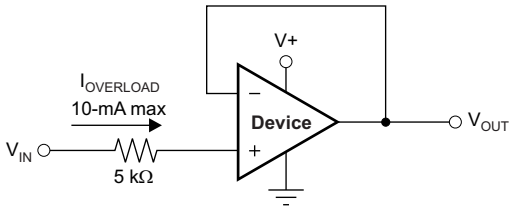


Figure 33. Input Current Protection

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPAx314-Q1 family is specified in several ways so the best match for a given application may be used; see the *Electrical Characteristics* table. First, the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region, as shown in Figure 7.

7.3.5 EMI Susceptibility and Input Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op-amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPAx314-Q1 family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Figure 32 shows the results of this testing on the OPAx314-Q1 family. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

7.3.6 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPAx314-Q1 family delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see Figure 17.

7.4 Device Functional Modes

The OPAx314-Q1 family is powered on when the supply is connected. The device can operate as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx314-Q1 family is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPAx314-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving sampling analog-to-digital converters (ADCs).

The OPAx314-Q1 family features a 3-MHz bandwidth and 1.5-V/μs slew rate with only 150-μA supply current per channel, providing good AC performance at very low power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/√Hz at 1 kHz, low-input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

8.1.1 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 34.

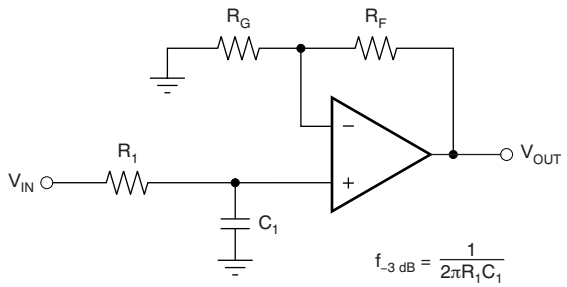


Figure 34. Single-Pole Low-Pass Filter

If additional attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as shown in Figure 35. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

Application Information (continued)

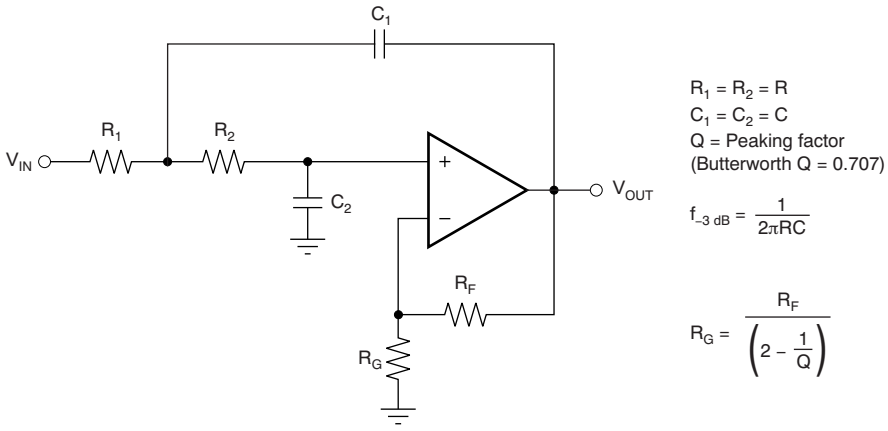


Figure 35. Two-Pole Low-Pass Sallen-Key Filter

8.1.2 Capacitive Load and Stability

The OPAx314-Q1 family is designed to be used in applications where driving a capacitive load is required. As with all op amps, specific instances can occur where the OPAx314-Q1 can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op-amp in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPAx314-Q1 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains; see , Figure 20.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 36. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

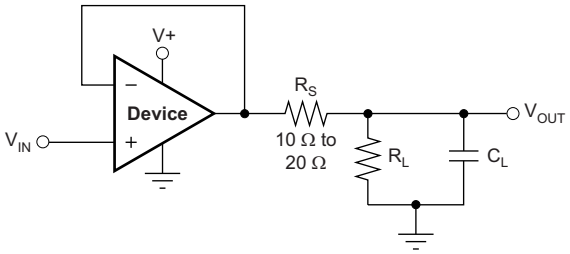


Figure 36. Improving Capacitive Load Drive

8.2 Typical Application

Some applications require differential signals. Figure 37 shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage (V_{OUT+}.) The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 0.1 V to 2.4 V. The difference (V_{DIFF}) is the difference between V_{OUT+} and $V_{OUT–}$. This makes the differential output voltage range 2.3 V.

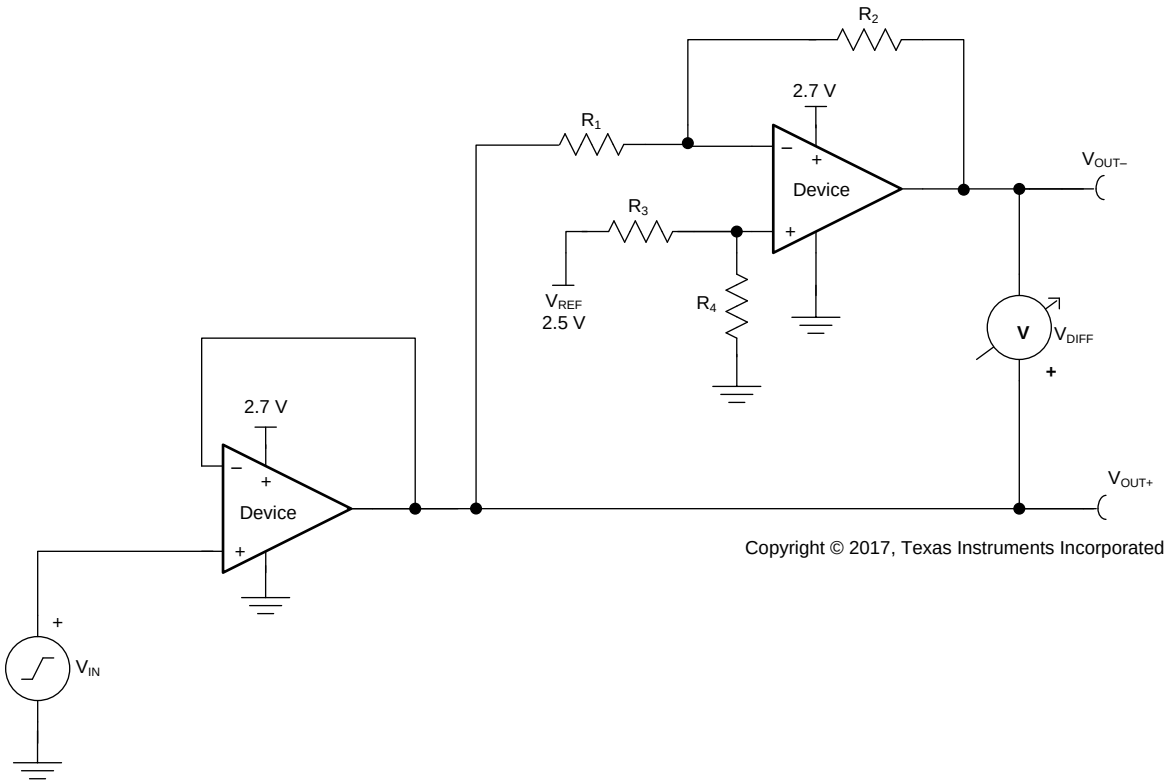


Figure 37. Schematic for a Single-Ended Input to Differential Output Conversion

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.1 V to 2.4 V
- Output differential: ±2.3 V
- Output common-mode voltage: 1.25 V
- Small-signal bandwidth: 1 MHz

8.2.2 Detailed Design Procedure

The circuit in Figure 37 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and $V_{OUT–}$ using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (as shown in Equation 1). $V_{OUT–}$ is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for $V_{OUT–}$ is given in Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT–} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) – V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

Typical Application (continued)

The differential output signal (V_{DIFF}) is the difference between the two single-ended output signals (V_{OUT+} and $V_{OUT–}$). Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to V_{REF}. The differential output range is 2 × V_{REF}. Furthermore, the common-mode voltage is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \quad (7)$$

8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPAx314-Q1 family is selected because the bandwidth is greater than the target of 1 MHz. The bandwidth and power ratio makes this device power efficient and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of $V_{OUT–}$ is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9 kΩ and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6 kΩ or lower) can be selected to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.2.3 Application Curves

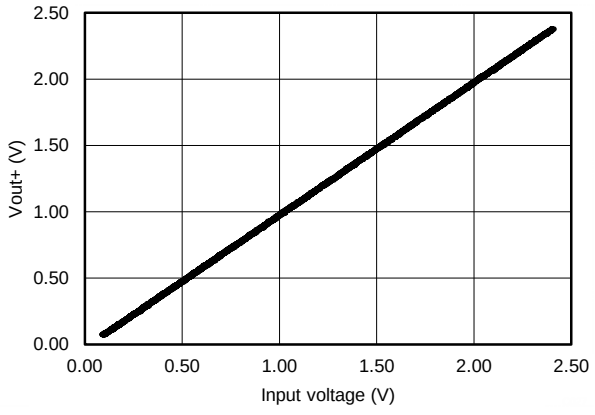


Figure 38. V_{OUT+} vs Input Voltage

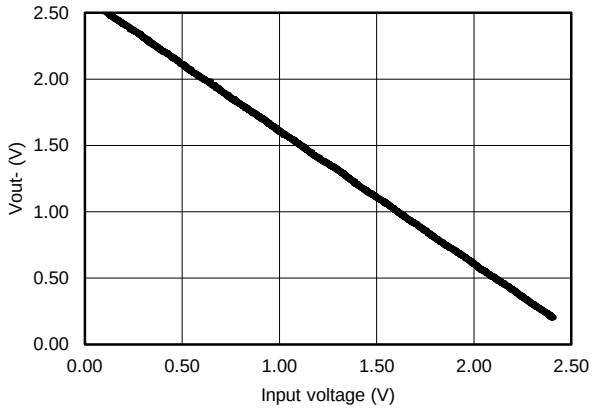


Figure 39. $V_{OUT–}$ vs Input Voltage

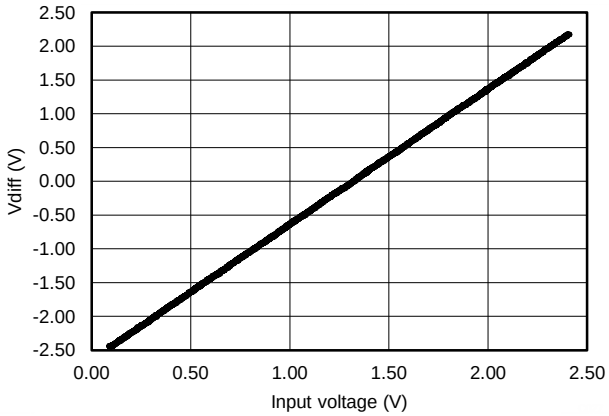


Figure 40. V_{DIFF} vs Input Voltage

9 Power Supply Recommendations

The OPAx314-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Figure 41.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

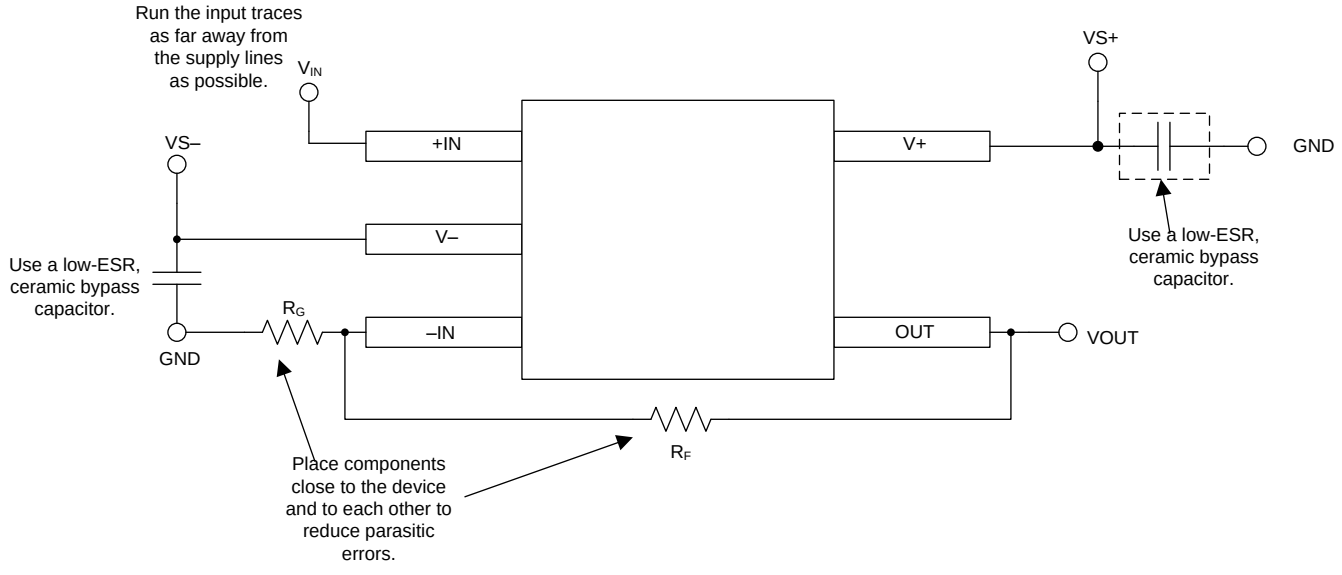


Figure 41. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *EMI Rejection Ratio of Operational Amplifiers*

11.1.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA314-Q1	Click here	Click here	Click here	Click here	Click here
OPA2314-Q1	Click here	Click here	Click here	Click here	Click here
OPA4314-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2314AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O2314Q
OPA2314AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	O2314Q
OPA314AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14ZD
OPA314AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14ZD
OPA314AQDBVTQ1	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14ZD
OPA314AQDBVTQ1.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14ZD
OPA4314AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4314Q1
OPA4314AQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4314Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2314-Q1, OPA314-Q1, OPA4314-Q1 :

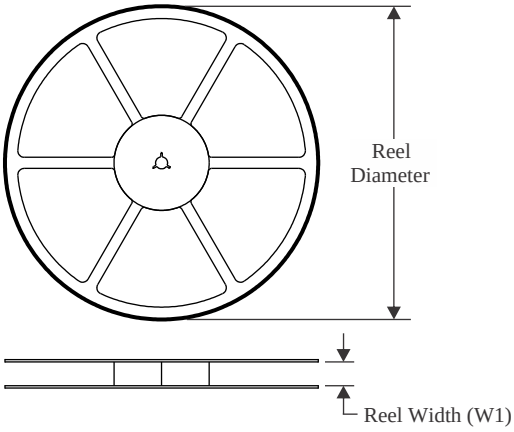
- Catalog : OPA2314, OPA314, OPA4314
- Enhanced Product : OPA2314-EP

NOTE: Qualified Version Definitions:

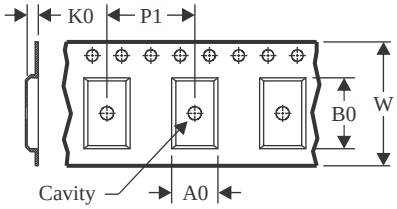
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

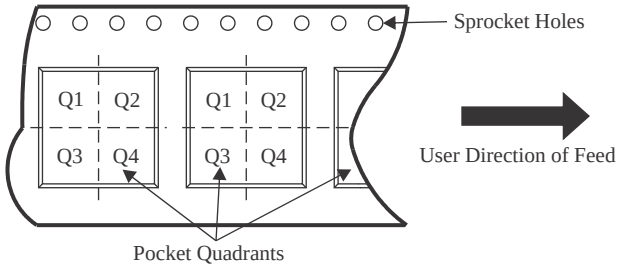


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

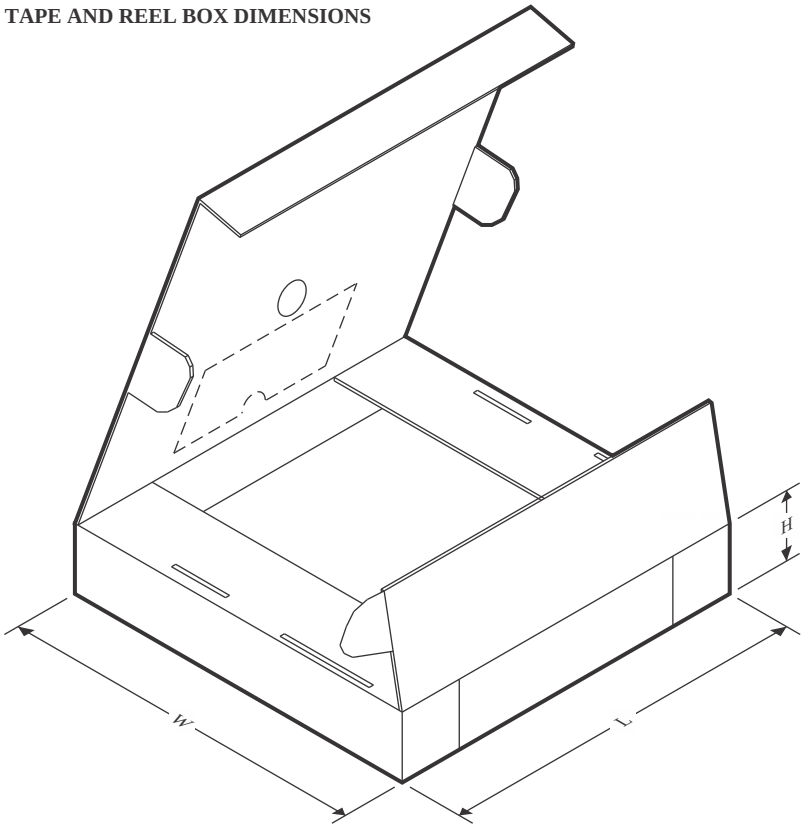
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2314AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA314AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA314AQDBVTQ1	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA4314AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

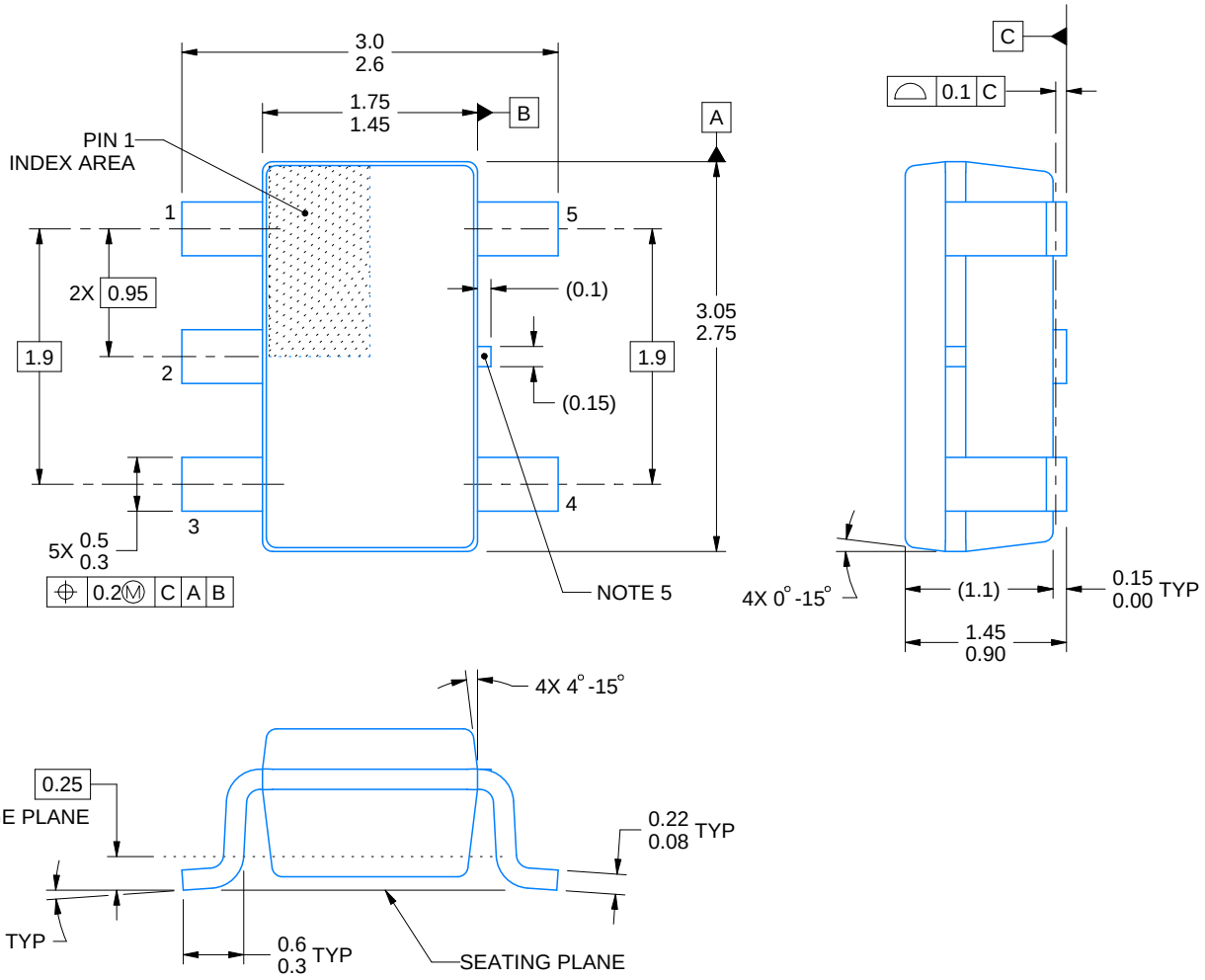
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2314AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
OPA314AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA314AQDBVTQ1	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA4314AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

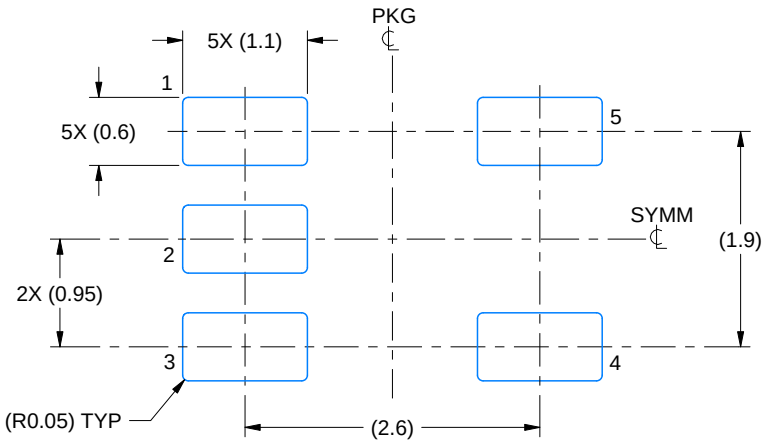
SMALL OUTLINE TRANSISTOR



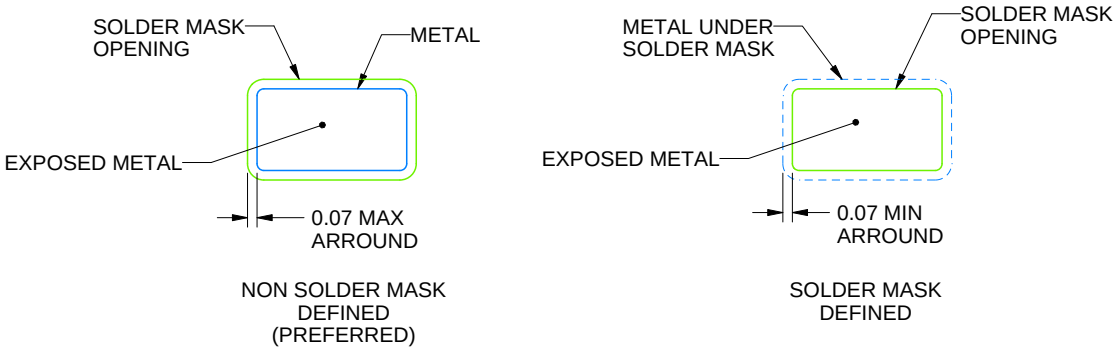
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

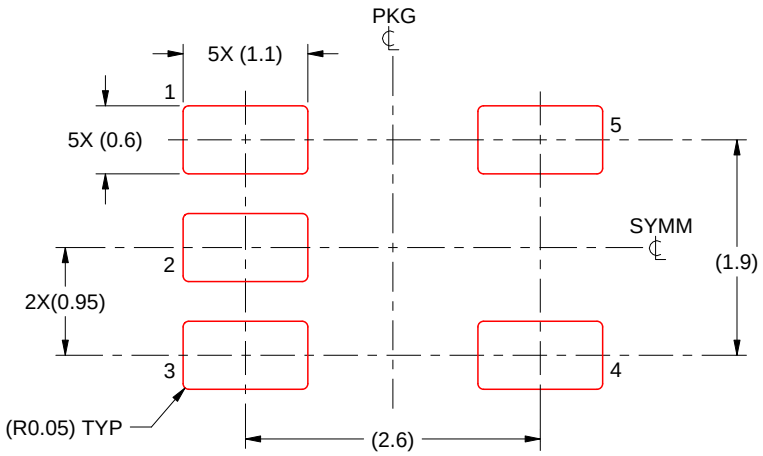


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

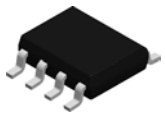


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

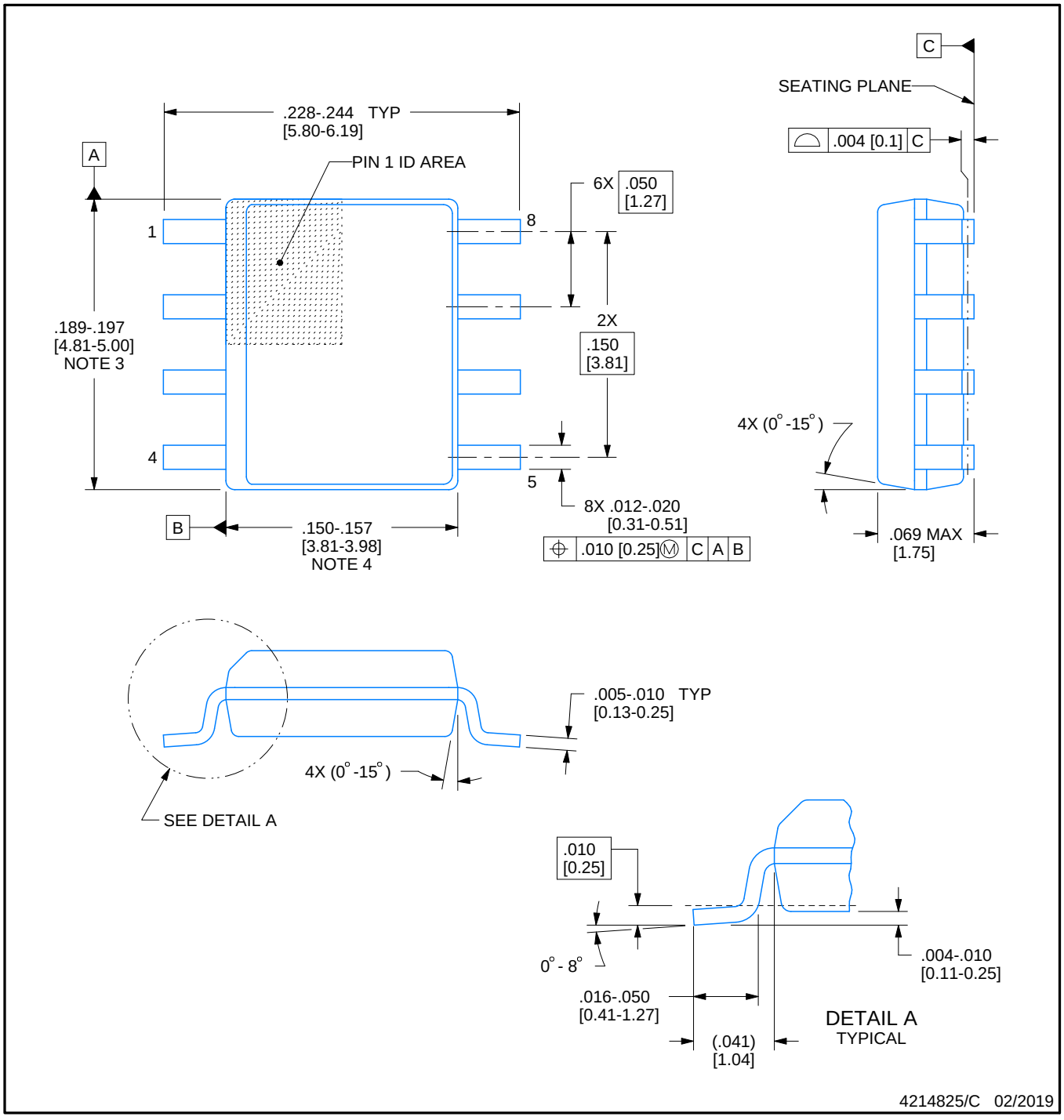


PACKAGE OUTLINE

D0008A

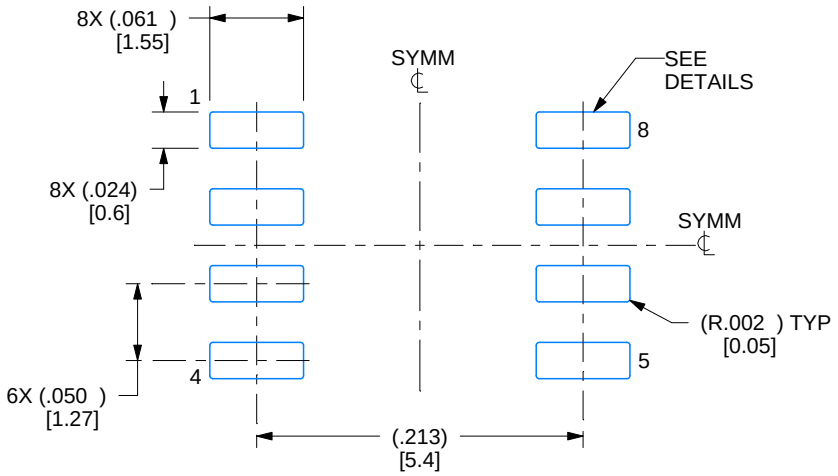
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

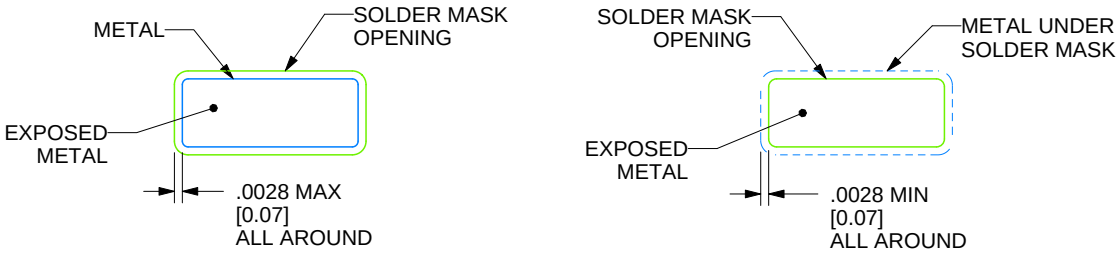


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

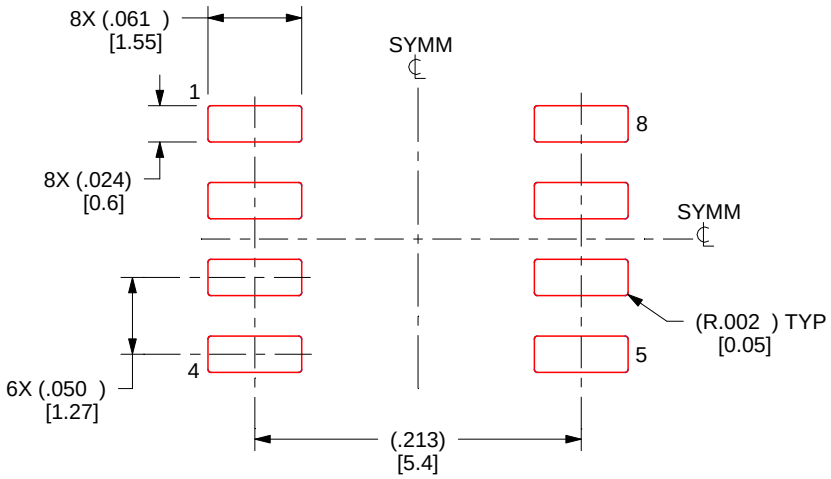
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

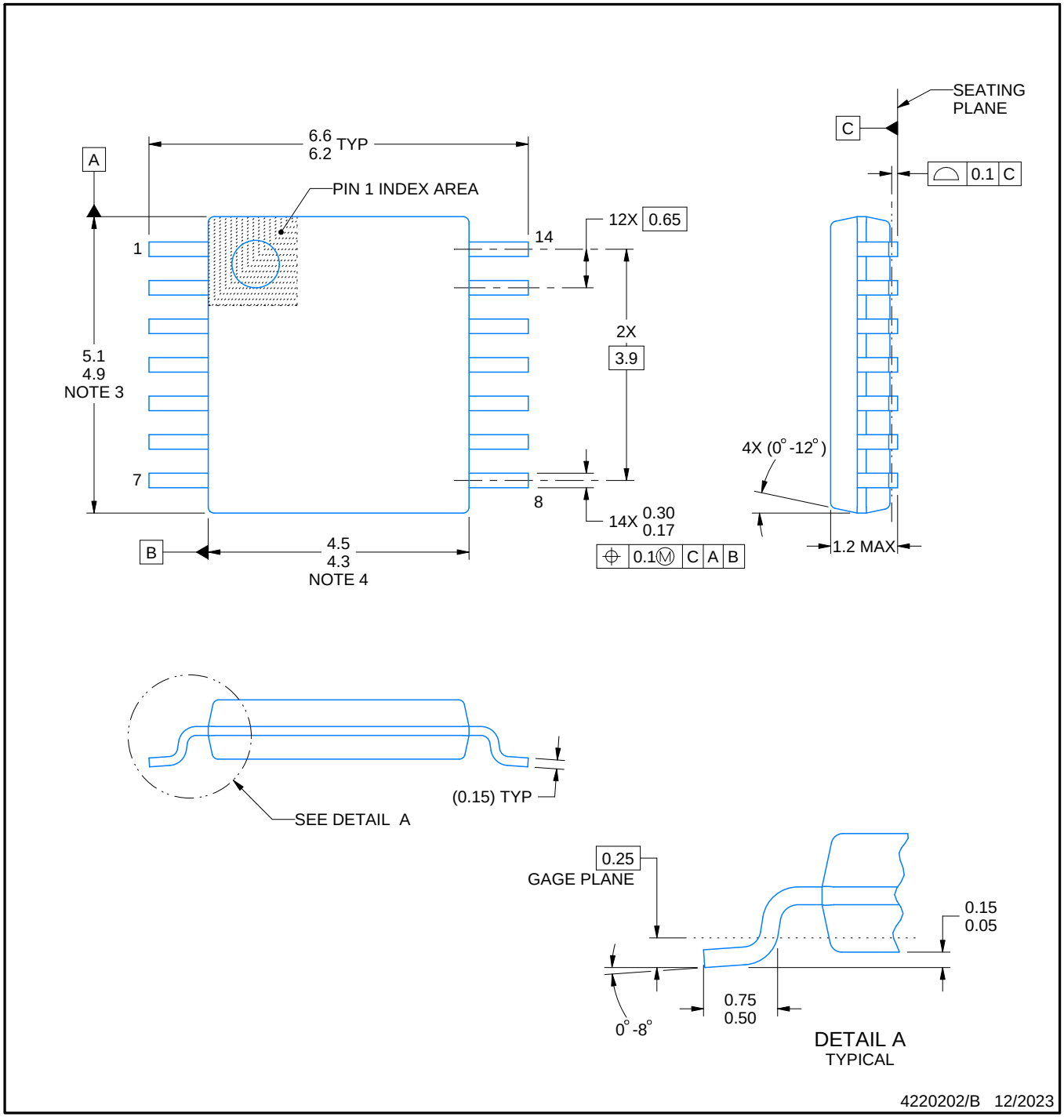
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

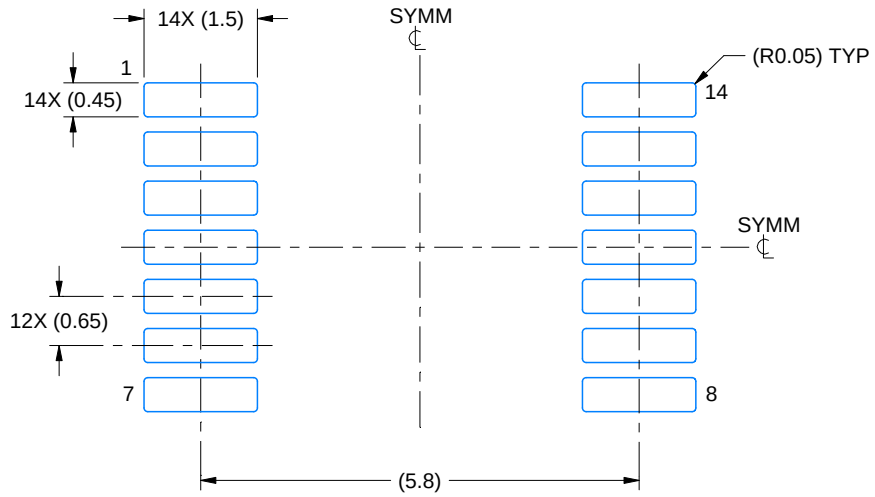
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

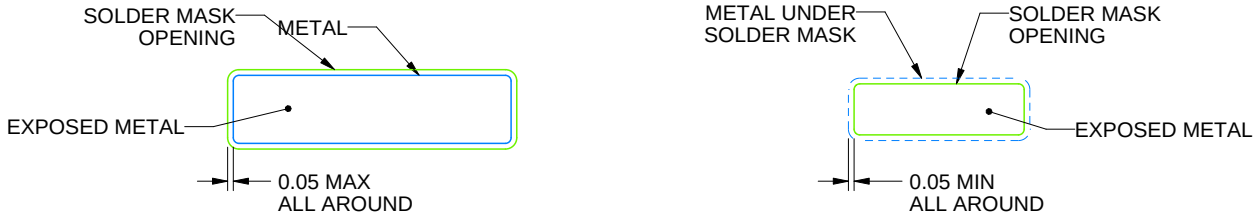


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

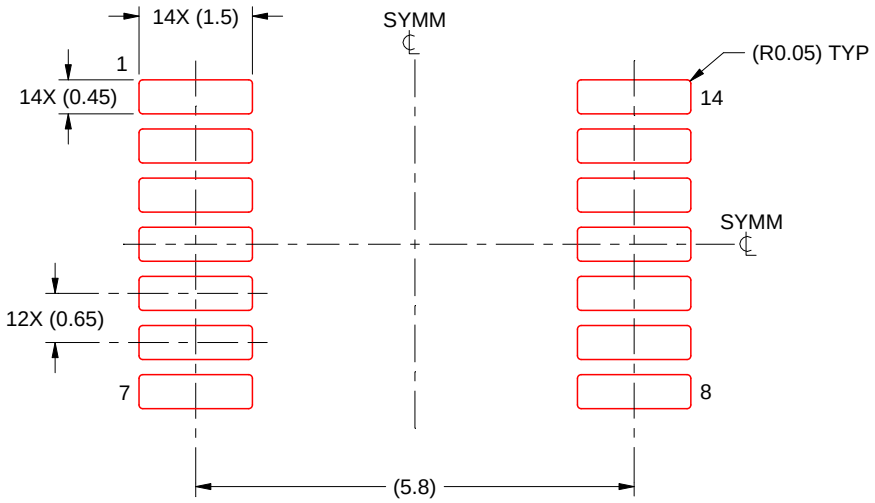


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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