PCA9557 リセットおよび構成レジスタを搭載したリモート 8 ビット I²C/SMBus 低消費電力 I/O エクスパンダ

1 特長

- 低いスタンバイ消費電流：1µA 以下
- I²C からパラレル ポートへのエクスパンダ
- 2.3V～5.5V の動作電源電圧範囲
- 5V 許容 I/O ポート
- 400kHz の Fast I²C バス
- 3 本のハードウェア アドレス ピンにより、最大 8 個のデバイスを I²C/SMBus に接続可能
- PCA9556 からの、より低電圧で高性能な移行パス
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- アクティブ LOW のリセット入力
- パワーオン リセット内蔵
- P0 上のハイ インピーダンス オープン ドレイン
- 電源投入時はすべてのチャネルが入力に構成された状態
- 電源オン時のグリッチなし
- SCL または SDA 入力のノイズ フィルタ
- 大電流の最大駆動能力を持つラッチ付き出力により LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン モデル (A115-A)
  - 荷電デバイス モデルで 1000V (C101)

2 アプリケーション

- テレコム シェルター：フィルタ ユニット
- サーバー
- ルーター (テレコム スイッチング機器)
- パーソナル コンピュータ
- パーソナル エレクトロニクス
- 産業用オートメーション
- GPIO が制限された製品

3 概要

この 2 線式双方向バス (I²C) 用 8 ビット I/O エクスパンダは、2.3V～5.5V の V_{CC} で動作するように設計されています。このデバイスは、I²C インターフェイス [シリアル クロック (SCL) およびシリアル データ (SDA)] により、ほとんどのマイクロコントローラ ファミリの汎用リモート I/O 拡張に使用できます。

PCA9557 には、8 ビットの構成レジスタ (入力 / 出力の選択) 1 つ、入力ポート、出力ポート、極性反転 (アクティブ High) レジスタがあります。電源オン時に、I/O は入力として構成されます。ただし、システム コントローラが I/O 構成ビットに書き込むことにより、I/O を入力または出力とすることができます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されています。入力ポート レジスタの極性は、極性反転レジスタで反転できます。すべてのレジスタは、システム コントローラで読み出すことができます。

本デバイスの出力 (ラッチ付き) は大電流駆動能力を備えているため、LED を直接駆動できます。本デバイスは低消費電流です。

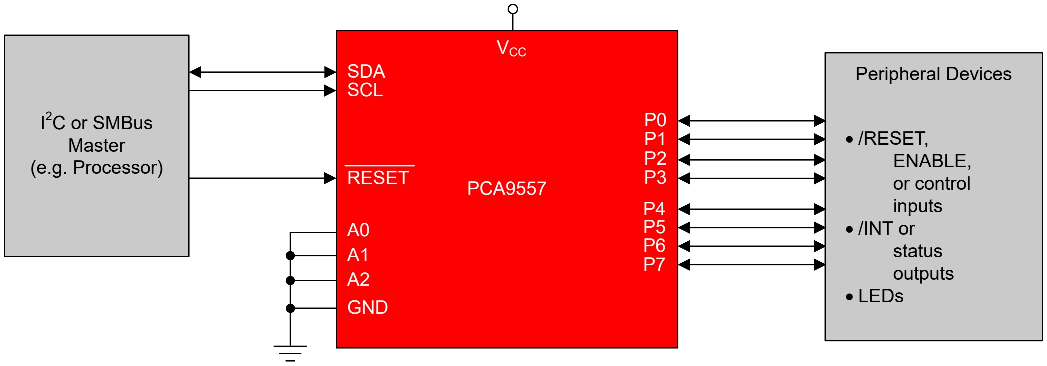
システム コントローラは、タイムアウトまたはその他の不適切な動作が発生した場合、アクティブ Low のリセット ($\overline{RESET}$) 入力を Low にアサートすることで PCA9557 をリセットできます。パワーオン リセットにより、レジスタはデフォルト状態に戻り、I²C/SMBus ステート マシンが初期化されます。$\overline{RESET}$ をアサートすると同じリセットと初期化が行われますが、デバイスの電源はオフになりません。

3 本のハードウェア ピン (A0、A1、A2) を使って固定 I²C アドレスをプログラムおよび変更することで、最大 8 つのデバイスが同じ I²C バスまたは SMBus を共有できます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
PCA9557	D (SOIC、16)	9.9mm × 6mm
	DB (SSOP、16)	6.2mm × 7.8mm
	DGV (TVSOP、16)	3.6mm × 6.4mm
	PW (TSSOP、16)	5mm × 6.4mm
	RGY (VQFN、16)	4mm × 3.5mm
	RGV (VQFN、16)	4mm × 4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。


I2C or SMBus
Master
(e.g. Processor)
VCC
SDA
SCL
RESET
PCA9557
A0
A1
A2
GND
P0
P1
P2
P3
P4
P5
P6
P7
Peripheral Devices
• /RESET,
ENABLE,
or control
inputs
• /INT or
status
outputs
• LEDs

ロジック図

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4 Pin Configuration and Functions

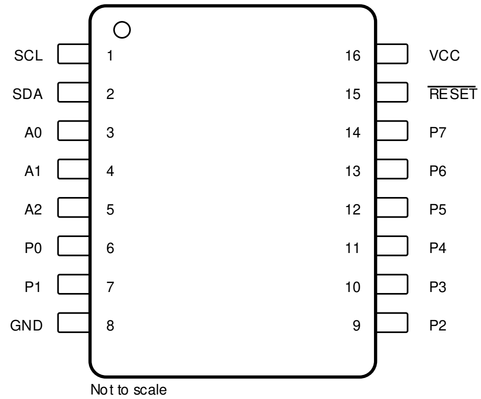


図 4-1. D, DB, DGV, PW Package, 16-Pin SOIC, SSOP, TVSOP, or TSSOP (Top View)

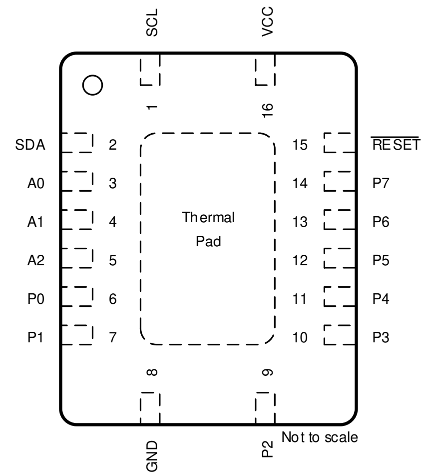


図 4-2. RGY or RGV Package, 16-Pin VQFN or VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SCL	1	I	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	2	I/O	Serial data bus. Connect to V_{CC} through a pullup resistor.
A0	3	I	Address input. Connect directly to V_{CC} or ground.
A1	4	I	Address input. Connect directly to V_{CC} or ground.
A2	5	I	Address input. Connect directly to V_{CC} or ground.
P0	6	I/O	P-port input/output. High impedance open-drain design structure. Connect to V_{CC} through a pullup resistor.
P1	7	I/O	P-port input/output. Push-pull design structure
GND	8	G	Ground
P2	9	I/O	P-port input/output. Push-pull design structure
P3	10	I/O	P-port input/output. Push-pull design structure
P4	11	I/O	P-port input/output. Push-pull design structure
P5	12	I/O	P-port input/output. Push-pull design structure
P6	13	I/O	P-port input/output. Push-pull design structure
P7	14	I/O	P-port input/output. Push-pull design structure
$\overline{RESET}$	15	I	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
V_{CC}	16	P	Supply voltage

(1) I = input, O = output, P = power, G = Ground

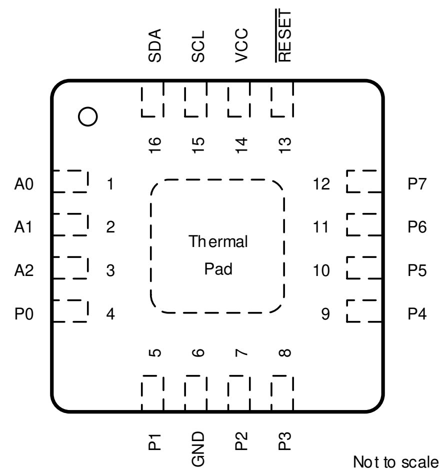


図 4-3. RGV Package, 16-Pin QFN (Top View)

表 4-2. Pin Functions, RGV

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A0	1	I	Address input. Connect directly to V_{CC} or ground.
A1	2	I	Address input. Connect directly to V_{CC} or ground.
A2	3	I	Address input. Connect directly to V_{CC} or ground.
P0	4	I/O	P-port input/output. High impedance open-drain design structure. Connect to V_{CC} through a pullup resistor.
P1	5	I/O	P-port input/output. Push-pull design structure
GND	6	G	Ground
P2	7	I/O	P-port input/output. Push-pull design structure
P3	8	I/O	P-port input/output. Push-pull design structure
P4	9	I/O	P-port input/output. Push-pull design structure
P5	10	I/O	P-port input/output. Push-pull design structure
P6	11	I/O	P-port input/output. Push-pull design structure
P7	12	I/O	P-port input/output. Push-pull design structure
$\overline{RESET}$	13	I	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
V_{CC}	14	P	Supply voltage
SCL	15	I	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	16	I/O	Serial data bus. Connect to V_{CC} through a pullup resistor.

(1) I = input, O = output, P = power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see [(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage [(2)]		–0.5	6	V
V_O	Output voltage [(2)]		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		–20	µA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommend Operating Conditions*. If briefly operating outside the *Recommend Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P7–P0, $\overline{\text{RESET}}$	2.2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A2–A0, P7–P0, ($\overline{\text{RESET}}$ $V_{CC} > 2.4V$)	–0.5	0.8	
		$\overline{\text{RESET}}$ $V_{CC} \le 2.4V$	–0.5	0.75	
I_{OH}	High-level output current	P7–P1		–10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		PCA9557						UNIT
		D (SSOP)	DB (SSOP)	DGV (SSOP)	PW (SSOP)	RGV (VQFN)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.2	82	120	98.0	44.5	47	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.0			30.7	40.1		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.2			52.7	20.2		°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.5			1.0	0.9		°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.8			52.1	20.2		°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A			N/A	5.7		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18mA	2.3V to 5.5V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.65	2.1	V
V_{OH}	P-port high-level output voltage [3]	I_{OH} = –8mA	2.3V	1.8			V
			3V	2.6			
			4.5V	3			
			4.75V	4.1			
		I_{OH} = –10mA	2.3V	1.5			
			3V	2.5			
			4.5V	3			
			4.75V	4			
I_{OL}	SDA	V_{OL} = 0.4V	2.3V to 5.5V	3			mA
	P port [2]	V_{OL} = 0.5V	2.3V to 5.5V	8	20		
		V_{OL} = 0.55V		8	20		
		V_{OL} = 0.7V		10	24		
I_{OH}	P port, except for P0[2]	V_{OH} = 2.3V	2.3V to 5.5V	–4			mA
	P0 [2]	V_{OH} = 4.6V	4.6V to 5.5V			1	µA
		V_{OH} = 3.3V	3.3V to 5.5V			1	
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3V to 5.5V			±1	µA
	A2–A0, $\overline{\text{RESET}}$					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3V to 5.5V			1	µA
I_{IL}	P port	V_I = GND	2.3V to 5.5V			1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	5.5V		19	25	µA
			3.6V		12	22	
			2.7V		8	20	
		$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 100 kHz	5.5V		1.5	5	
			3.6V		1	4	
			2.7V		0.6	3	
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz	5.5V		0.25	1	
			3.6V		0.25	0.9	
			2.7V		0.2	0.8	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP(1)	MAX	UNIT
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3V to 5.5V			0.2	mA
		Every LED I/O at V_I = 4.3 V, f_{SCL} = 0 kHz	5.5V			0.4	
C_I	SCL	V_I = V_{CC} or GND	2.3V to 5.5 V		4	6	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	2.3V to 5.5V		5.5	8	pF
	P port				7.5	9.5	

(1) All typical values are at nominal supply voltage (2.5, 3.3, or 5V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25mA, and the P port (P7–P0) must be limited to a maximum current of 200mA.
(3) The total current sourced by all I/Os must be limited to 85mA per bit.

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

		MIN	MAX	UNIT
STANDARD MODE				
f_{scl}	I²C clock frequency	100		kHz
t_{sch}	I²C clock high time	4		μs
t_{scl}	I²C clock low time	4.7		μs
t_{sp}	I²C spike time	50		ns
t_{sds}	I²C serial data setup time	250		ns
t_{sdh}	I²C serial data hold time		0	ns
t_{icr}	I²C input rise time		1000	ns
t_{icf}	I²C input fall time		300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7	μs
t_{sts}	I²C start or repeated start condition setup time		4.7	μs
t_{sth}	I²C start or repeated start condition hold time		4	μs
t_{sps}	I²C stop condition setup time		4	μs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid	1		μs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1	μs
C_b	I²C bus capacitive load		400	pF
FAST MODE				
f_{scl}	I²C clock frequency	400		kHz
t_{sch}	I²C clock high time	0.6		μs
t_{scl}	I²C clock low time	1.3		μs
t_{sp}	I²C spike time	50		ns
t_{sds}	I²C serial data setup time	100		ns
t_{sdh}	I²C serial data hold time		0	ns
t_{icr}	I²C input rise time	20 + 0.1C_b (1)	300	ns
t_{icf}	I²C input fall time	20 + 0.1C_b (1)	300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus	20 + 0.1C_b (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3	μs
t_{sts}	I²C start or repeated start condition setup time		0.6	μs
t_{sth}	I²C start or repeated start condition hold time		0.6	μs
t_{sps}	I²C stop condition setup time		0.6	μs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid	0.9		μs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		0.9	μs
C_b	I²C bus capacitive load		400	pF

(1) C_b = total capacitance of one bus line in pF

5.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-3)

		MIN	MAX	UNIT
STANDARD MODE and FAST MODE				
t_W	Reset pulse duration VCC ≤ 2.5V[2]		20	ns
	Reset pulse duration VCC > 2.5V[2]		16	ns
t_{REC}	Reset recovery time		0	ns
t_{RESET}	Time to reset[1]		400	ns

(1) The PCA9557 requires a minimum of 400 ns to be reset
(2) A pulse duration of 16 ns minimum must be applied to RESET to return the PCA9557 to its default state.

5.8 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER		FROM	TO	MIN	MAX	UNIT
STANDARD MODE and FAST MODE						
t_{pv}	Output data valid	SCL	P0		250	ns
		SCL	P1–P7		200	ns
t_{ps}	Input data setup time	P port	SCL	0		ns
t_{ph}	Input data hold time	P port	SCL	200		ns

5.9 Typical Characteristics

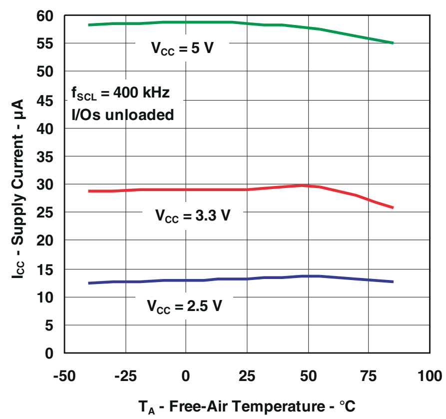


図 5-1. Supply Current vs Temperature

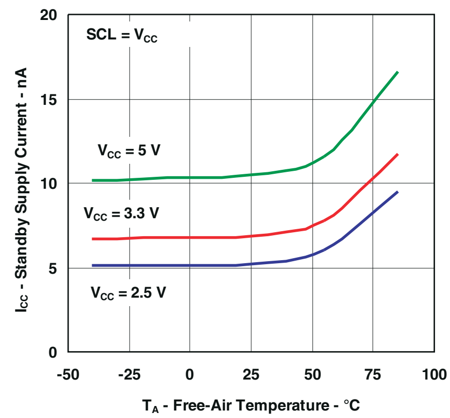


図 5-2. Standby Supply Current vs Temperature

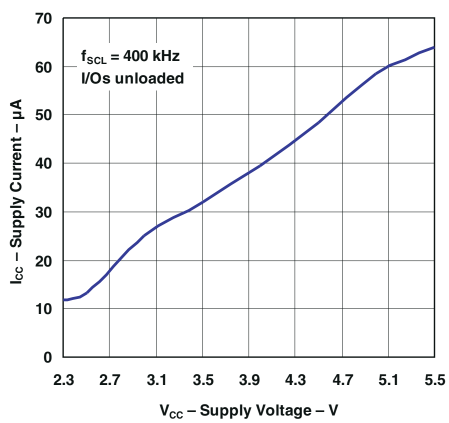


図 5-3. Supply Current vs Supply Voltage

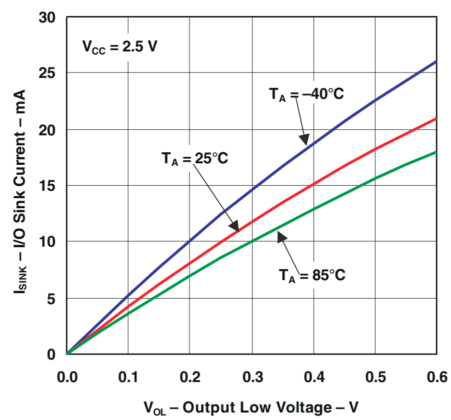


図 5-4. I/O Sink Current vs Output Low Voltage

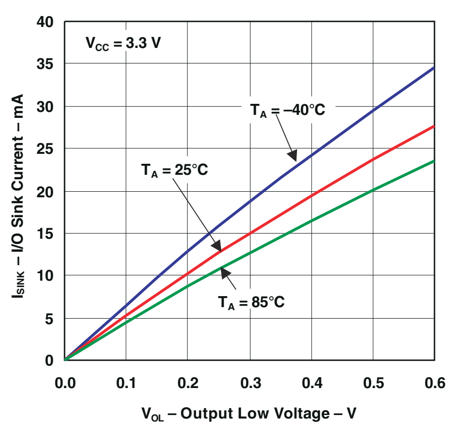


図 5-5. I/O Sink Current vs Output Low Voltage

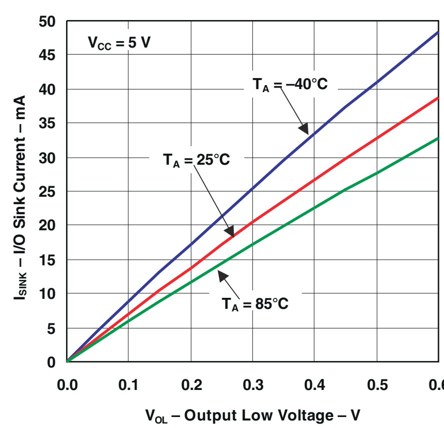


図 5-6. I/O Sink Current vs Output Low Voltage

5.9 Typical Characteristics (continued)

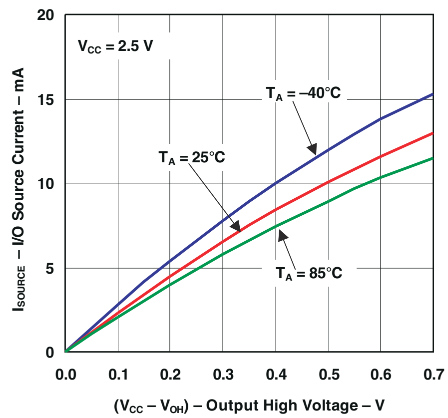


図 5-7. I/O Source Current vs Output High Voltage (P7–P1)

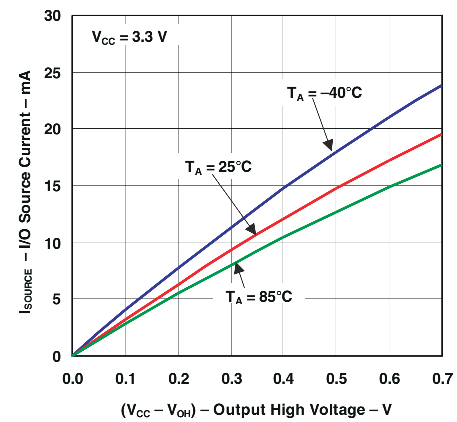


図 5-8. I/O Source Current vs Output High Voltage (P7–P1)

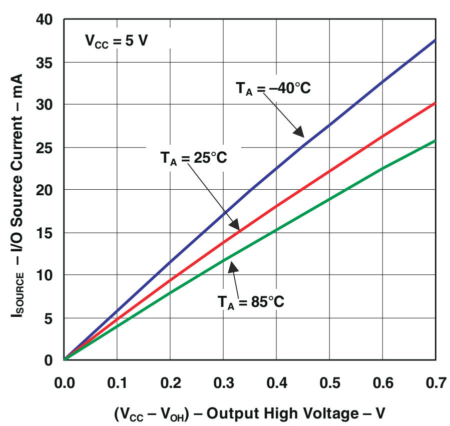


図 5-9. I/O Source Current vs Output High Voltage (P7–P1)

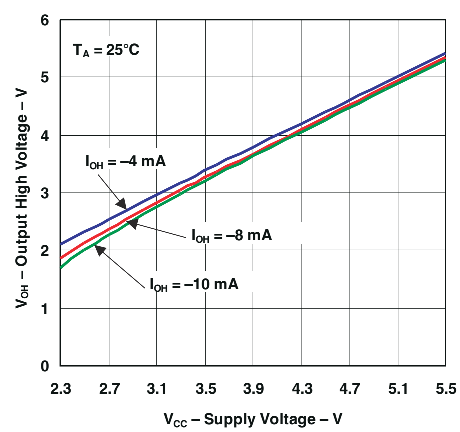


図 5-10. Output High Voltage vs Supply Voltage (P7–P1)

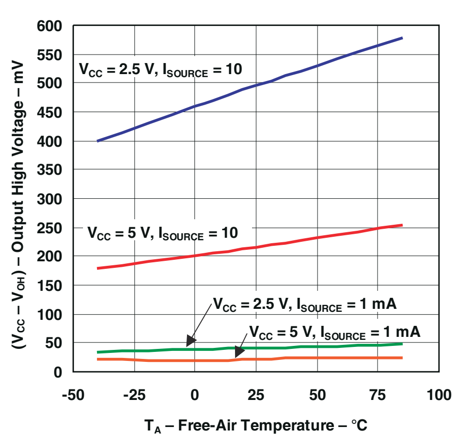


図 5-11. Output High Voltage vs Temperature (P7–P1)

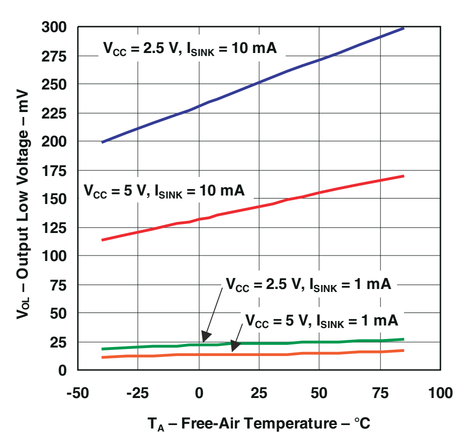
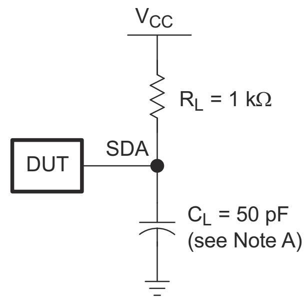
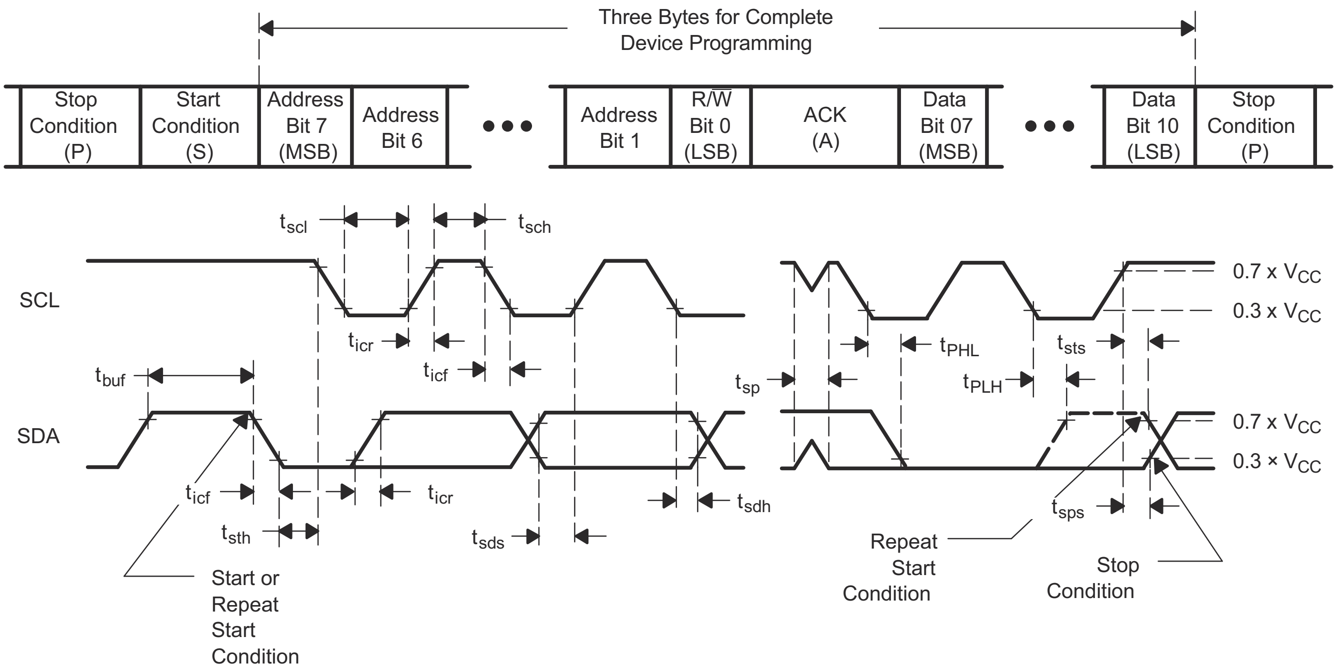


図 5-12. Output Low Voltage vs Temperature

6 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

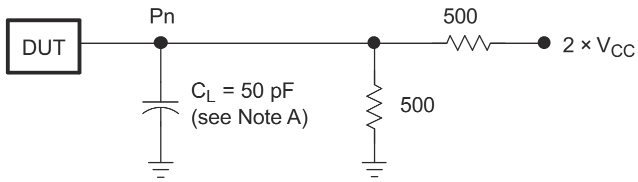
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

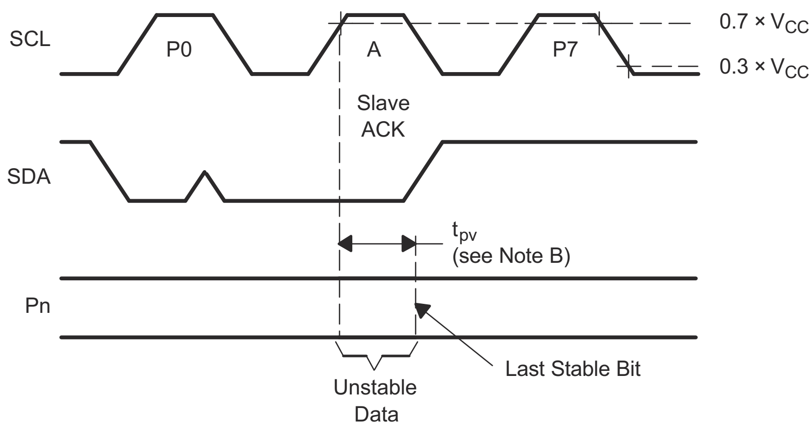
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

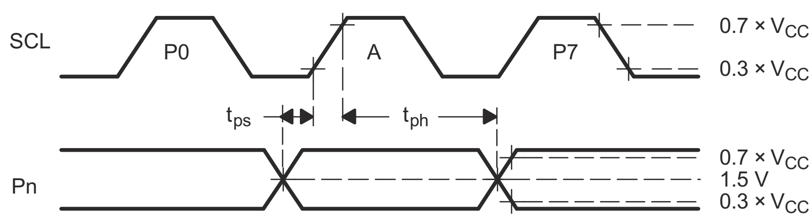
図 6-1. I^2C Interface Load Circuit and Voltage Waveforms



P-PORT LOAD CONFIGURATION



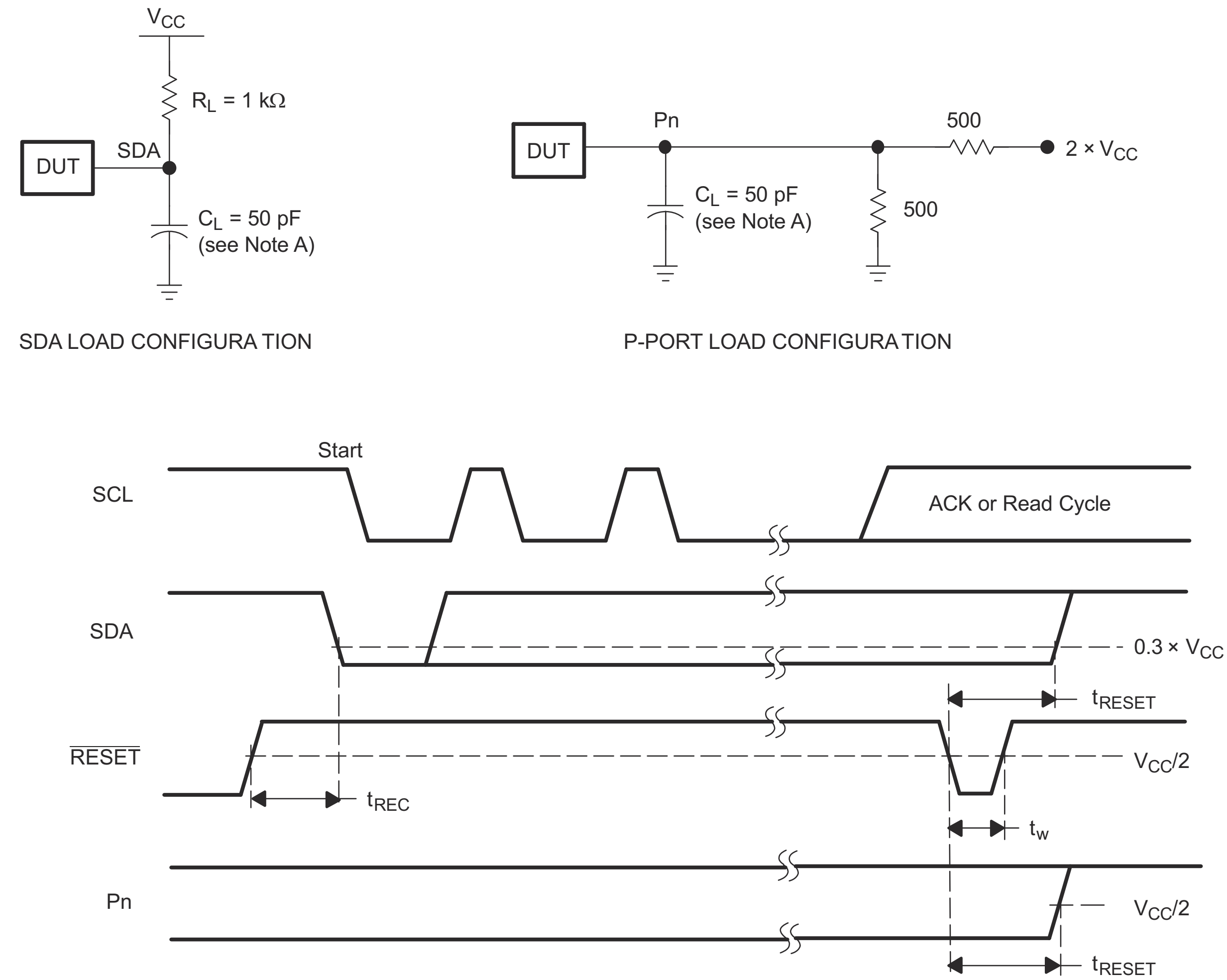
WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 6-2. P-Port Load Circuit and Voltage Waveforms

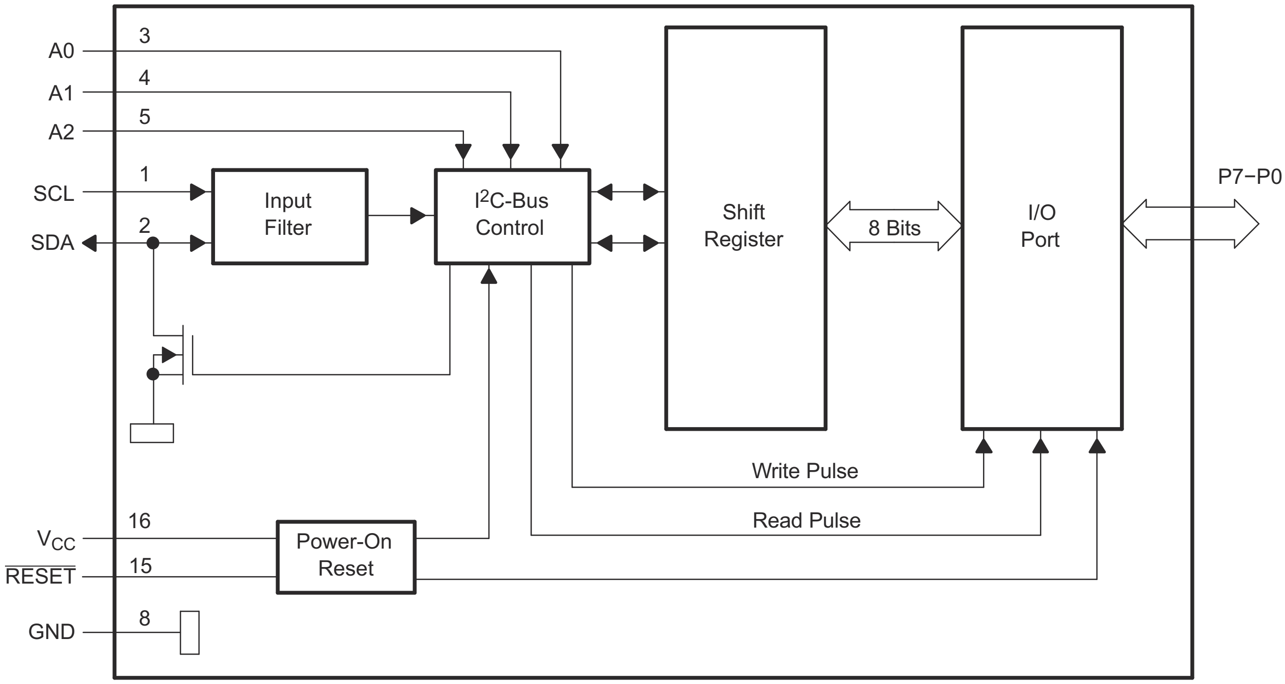


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. I/Os are configured as inputs.
D. All parameters and waveforms are not applicable to all devices.

図 6-3. Reset Load Circuits and Voltage Waveforms

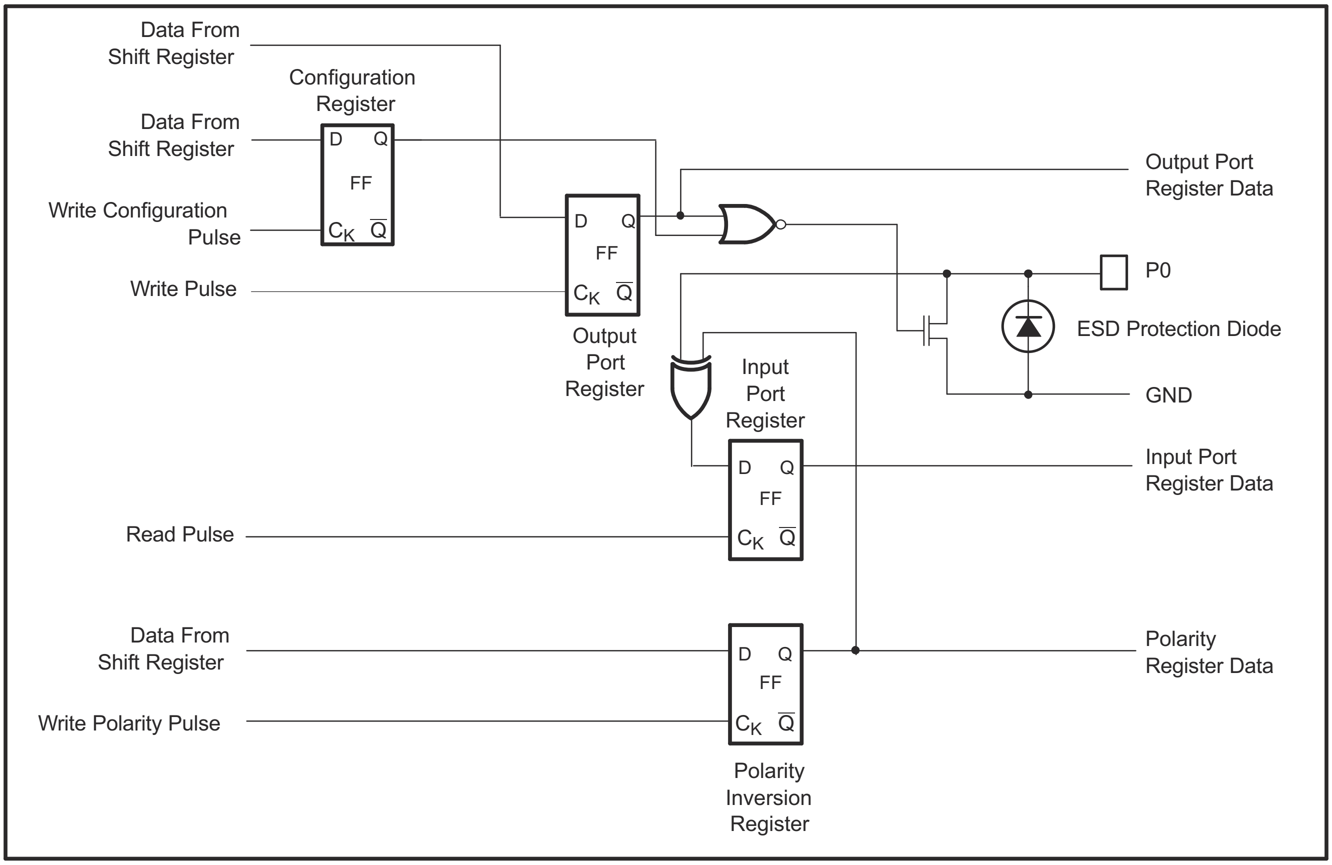
7 Detailed Description

7.1 Functional Block Diagram



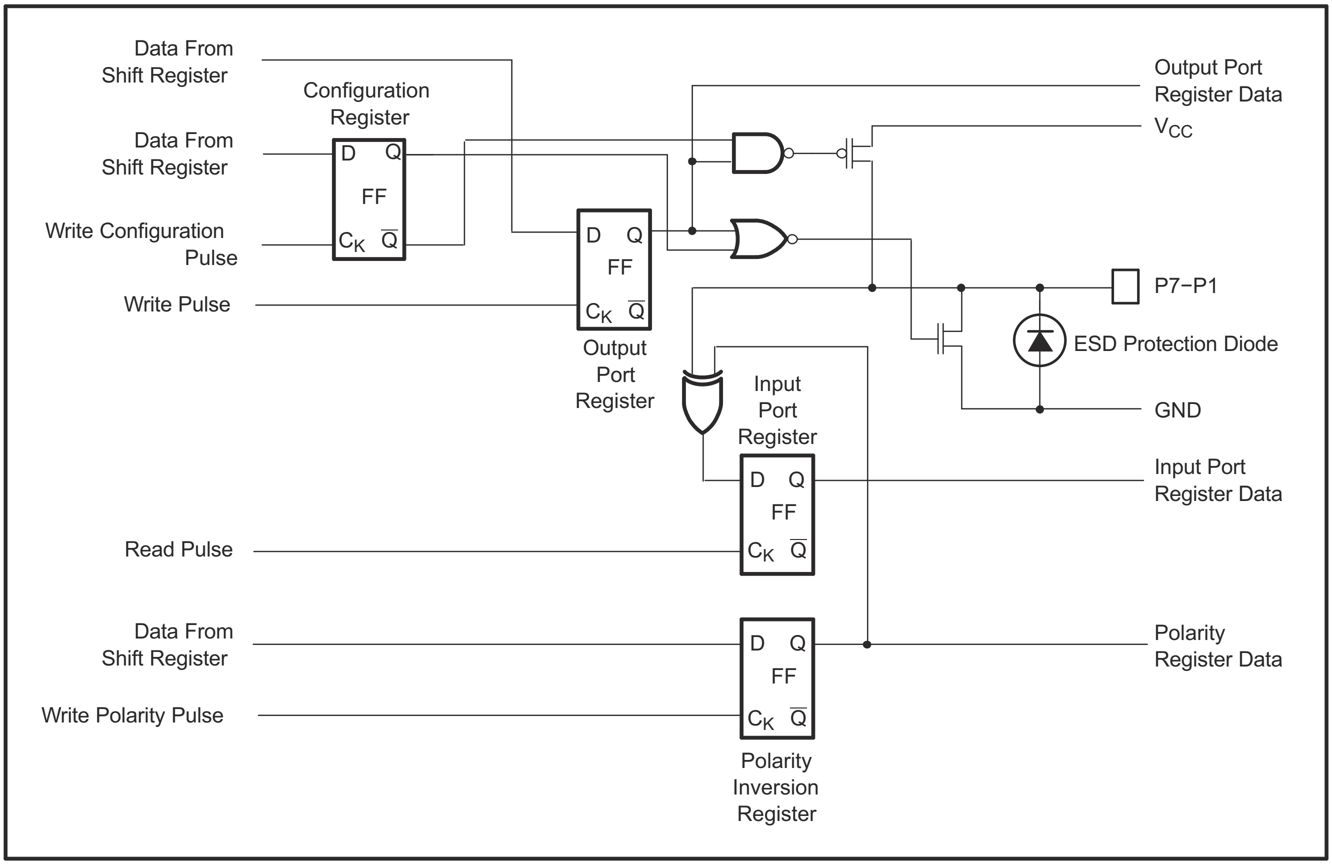
Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.
All I/Os are set to inputs at reset.

図 7-1. Logic Diagram (Positive Logic)



On power up or reset, all registers return to default values.

図 7-2. Simplified Schematic Diagram of P0



On power up or reset, all registers return to default values.

図 7-3. Simplified Schematic Diagram of P7–P1

7.2 Feature Description

7.2.1 $\overline{\text{RESET}}$

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA9557 registers and I^2C/SMBus state machine are held in their default states until $\overline{\text{RESET}}$ again is high. This input requires a pullup resistor to V_{CC} if no active connection is used.

7.2.1.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current will flow from $\overline{\text{RESET}}$ pin to VCC pin.

7.2.1.1.1 System Impact

VCC will be pulled above its regular voltage level.

7.2.1.1.2 System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC.

7.2.2 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9557 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the PCA9557 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle. The $\overline{\text{RESET}}$ input can be asserted to reset the system, while keeping the V_{CC} at its operating level.

See the *Power-On Reset Errata* section.

7.3 Programming

7.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a controller sending a start condition, a high-to-low transition on the SDA input and output while the SCL input is high (see 図 7-4). After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (A2–A0) inputs of the target device must not be changed between the start and the stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see 図 7-5).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see 図 7-4).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 7-6). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a stop condition.

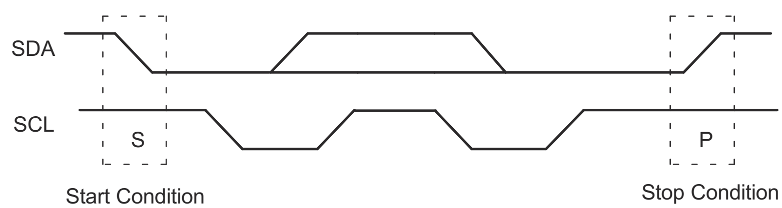


図 7-4. Definition of Start and Stop Conditions

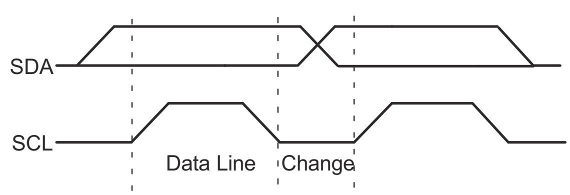


図 7-5. Bit Transfer

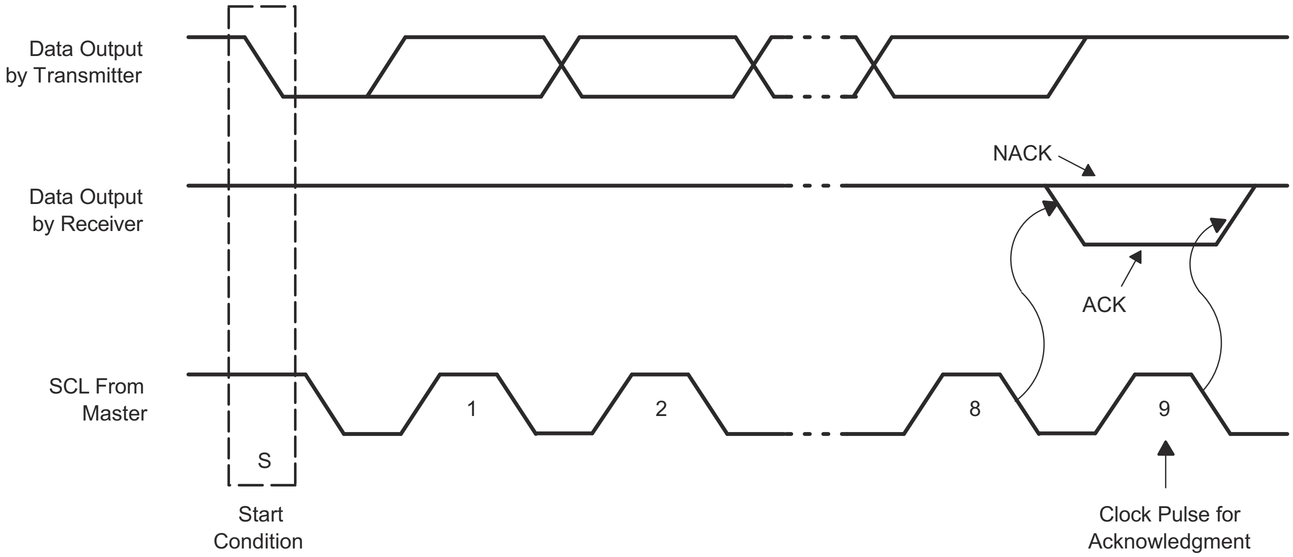


図 7-6. Acknowledgment on the I²C Bus

7.4 Register Maps

表 7-1 shows the PCA9557 interface definition.

表 7-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	L	H	H	A2	A1	A0	R/ $\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.4.1 Device Address

The address of the PCA9557 is shown in 図 7-7.

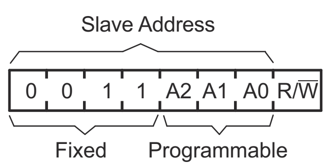


図 7-7. PCA9557 Address

The address reference of the PCA9557 is shown in 表 7-2.

表 7-2. Address Reference

INPUTS			I²C BUS TARGET ADDRESS
A2	A1	A0	
L	L	L	24 (decimal), 18 (hexadecimal)
L	L	H	25 (decimal), 19 (hexadecimal)
L	H	L	26 (decimal), 1A (hexadecimal)
L	H	H	27 (decimal), 1B (hexadecimal)
H	L	L	28 (decimal), 1C (hexadecimal)
H	L	H	29 (decimal), 1D (hexadecimal)
H	H	L	30 (decimal), 1E (hexadecimal)

表 7-2. Address Reference (続き)

INPUTS			I²C BUS TARGET ADDRESS
A2	A1	A0	
H	H	H	31 (decimal), 1F (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

7.4.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the PCA9557. Two bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion or configuration) that is affected. This register is written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a new command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. 図 7-8 shows the PCA9557 control register bits.

0	0	0	0	0	0	B1	B0

図 7-8. Control Register Bits

表 7-3 shows the PCA9557 command byte.

表 7-3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	×××× ××××
0	1	0×01	Output Port	Read/write byte	0000 0000
1	0	0×02	Polarity Inversion	Read/write byte	1111 0000
1	1	0×03	Configuration	Read/write byte	1111 1111

7.4.3 Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to signal the I^{2}C device that the input port register will be accessed next. See 表 7-4.

表 7-4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See 表 7-5.

表 7-5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	0	0	0	0	0	0	0	0

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained. See 表 7-6.

表 7-6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	1	1	1	1	0	0	0	0

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See 表 7-7.

表 7-7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

7.4.3.1 Bus Transactions

Data is exchanged between the master and PCA9557 through write and read commands.

7.4.3.1.1 Writes

Data is transmitted to the PCA9557 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see 図 7-7 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see 図 7-9 and 図 7-10).

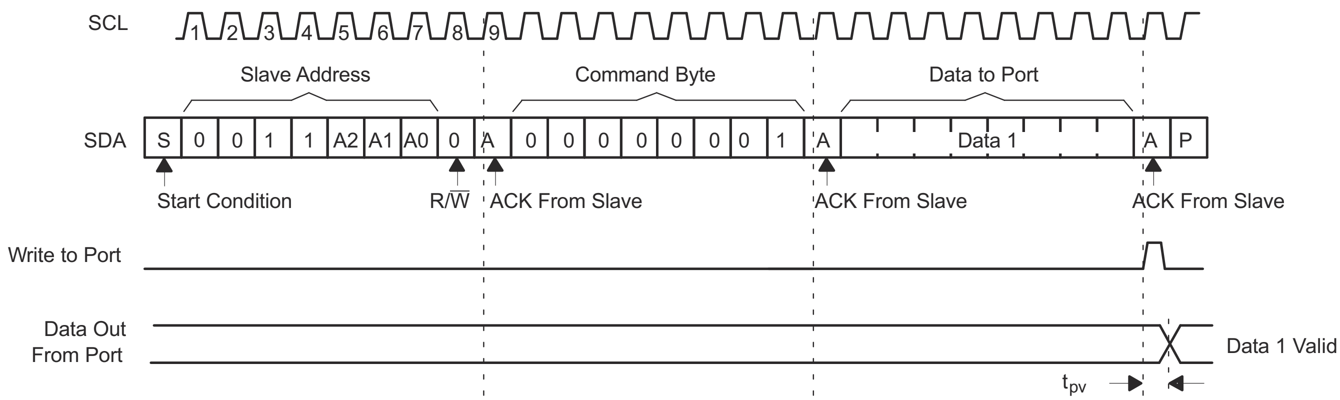


図 7-9. Write to Output Port Register

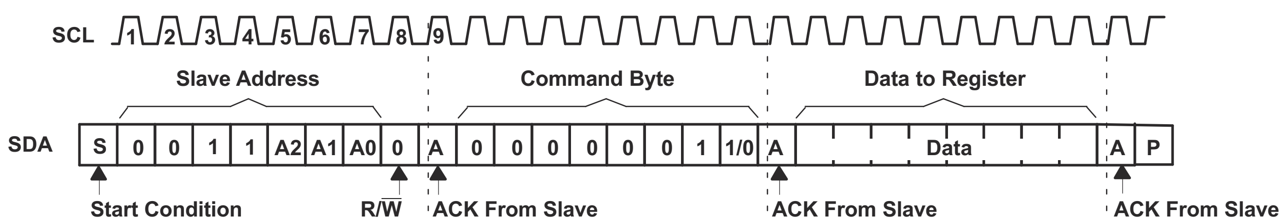


図 7-10. Write to Configuration or Polarity Inversion Registers

7.4.3.1.2 Reads

The bus master first must send the PCA9557 address with the LSB set to a logic 0 (see 図 7-7 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9557 (see 図 7-11 and 図 7-12). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

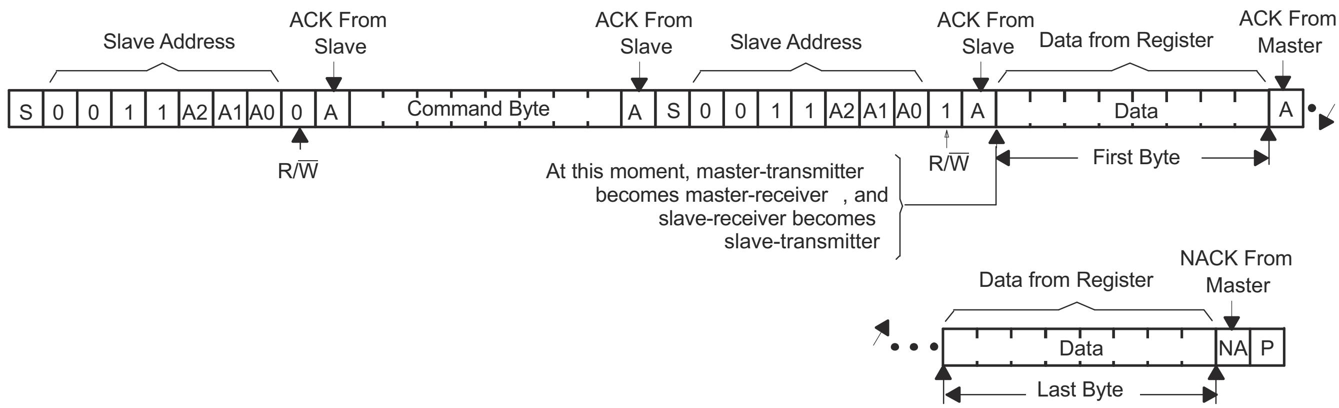
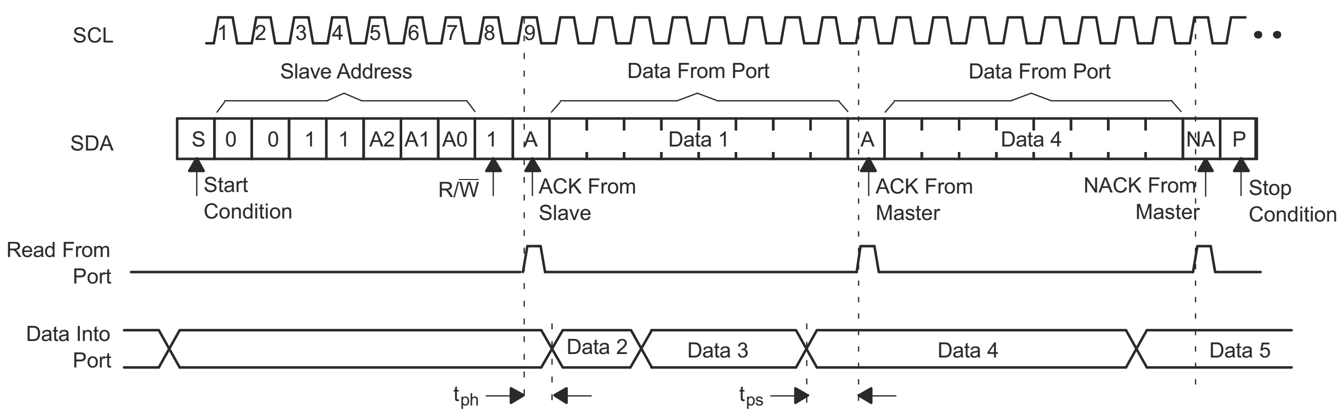


図 7-11. Read From Register



A. This figure assumes the command byte has been previously programmed with 00h.

B. Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see 図 7-11).

図 7-12. Read Input Port Register

8 Application and Implementation

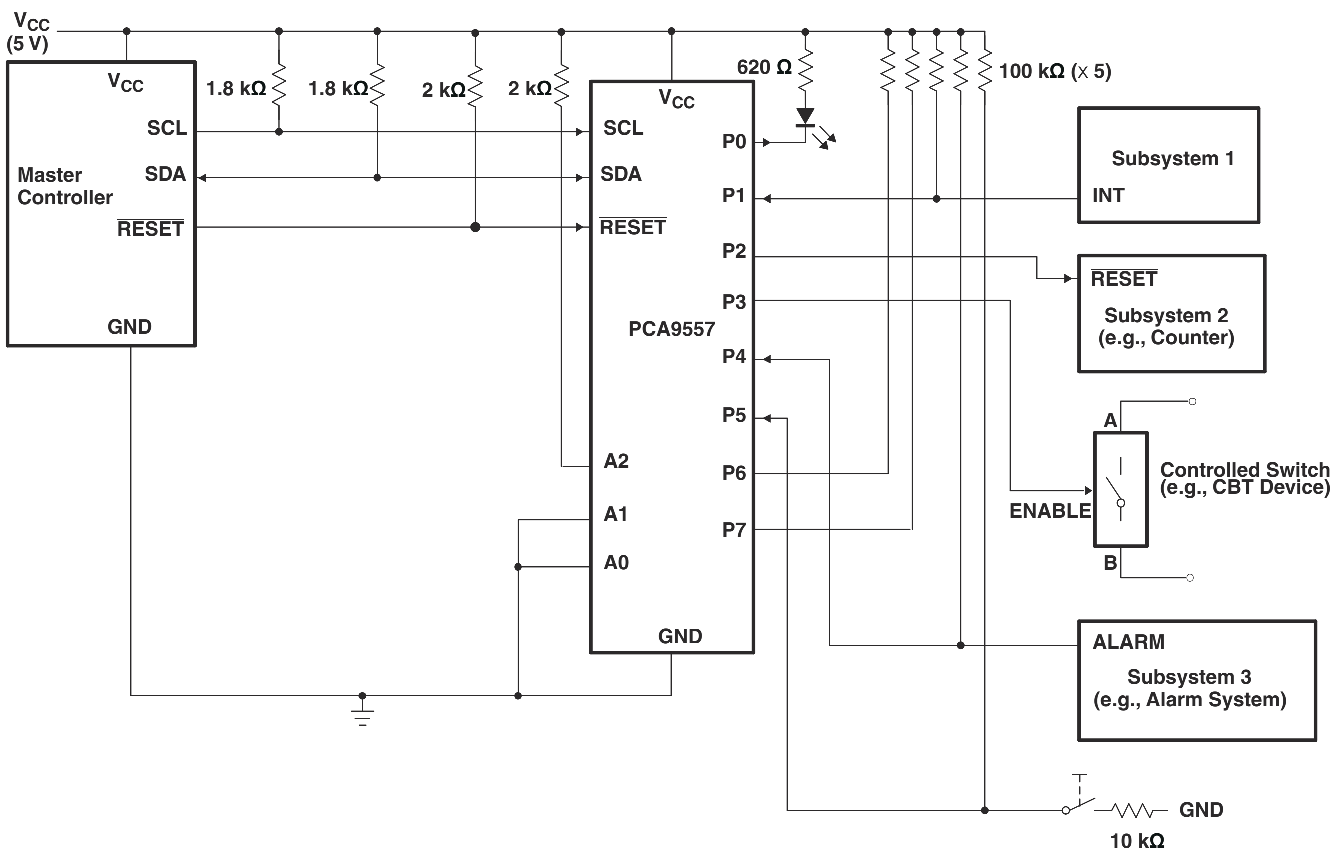
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

図 8-1 shows an application in which the PCA9557 can be used.

8.2 Typical Application



A. Device address is configured as 0011100 for this example.

B. P1, P4, and P5 are configured as inputs.

C. P0, P2, and P3 are configured as outputs.

D. P6 and P7 are not used and must be configured as outputs.

図 8-1. Typical Application

8.2.1 Detailed Design Procedure

8.2.1.1 Minimizing I_{CC} when I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in 図 8-1. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in the セクション 5.5 table shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

図 8-2 shows a high-value resistor in parallel with the LED. 図 8-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

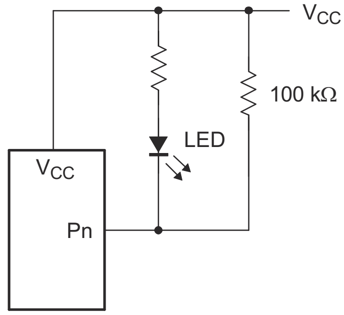


図 8-2. High-Value Resistor in Parallel with the LED

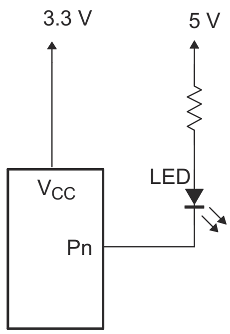


図 8-3. Device Supplied by a Low Voltage

8.3 Power Supply Recommendations

8.3.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed in 図 8-4.

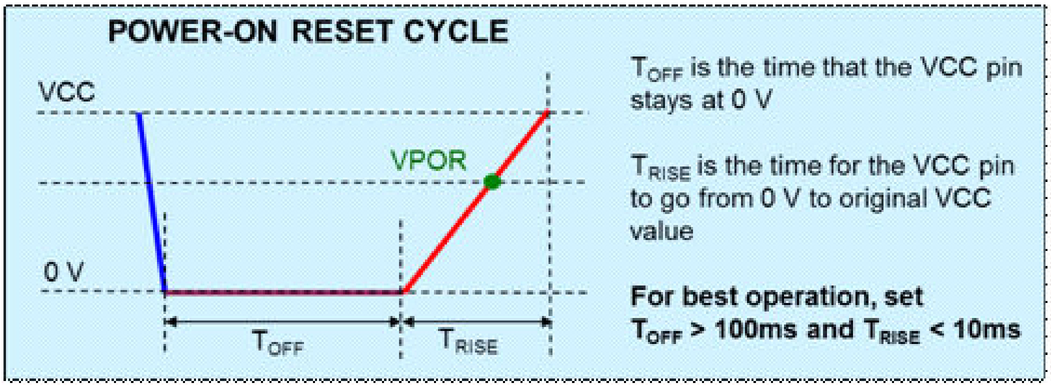


図 8-4. Power-On Reset

8.3.1.1 System Impact

As shown in the previous figure, if ramp conditions are outside timing allowance, then POR condition can be missed causing the device to lock up.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *I2C Bus Pull-Up Resistor Calculation*
- Texas Instruments, *Maximum Clock Frequency of I2C Bus Using Repeaters*
- Texas Instruments, *Introduction to Logic*
- Texas Instruments, *Understanding the I2C Bus*
- Texas Instruments, *Choosing the Correct I2C Device for New Designs*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

9.3 サポート・リソース

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9.5 静電気放電に関する注意事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (May 2014) to Revision K (December 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を変更 1
- Moved Storage Temperature Range row from *ESD Ratings* table to *Absolute Maximum Ratings* table 6
- Updated V_{IH} from 2.0V to 2.2V 6
- Add V_{IL} parameter for $\overline{\text{RESET}}$ 6
- Updated *Thermal Information* values for D, PW and RGV packages 7
- Updated *I^2C Timing Requirements* table 8
- Add t_W parameter for 2.5V voltage condition 9

Changes from Revision I (June 2008) to Revision J (May 2014) **Page**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9557D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	PCA9557
PCA9557DB	Active	Production	SSOP (DB) | 16	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DB.A	Active	Production	SSOP (DB) | 16	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9557
PCA9557DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9557
PCA9557PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD557
PCA9557RGVR	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557
PCA9557RGVR.A	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557
PCA9557RGVRG4	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557
PCA9557RGVRG4.A	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557
PCA9557RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557
PCA9557RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD557

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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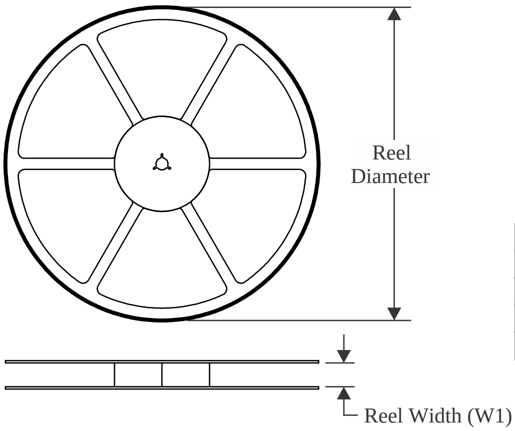
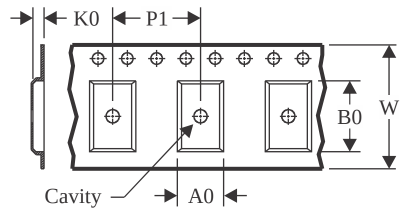
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

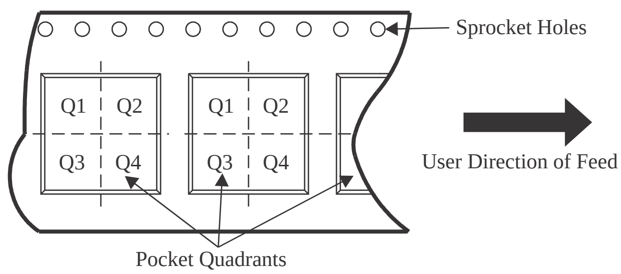


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

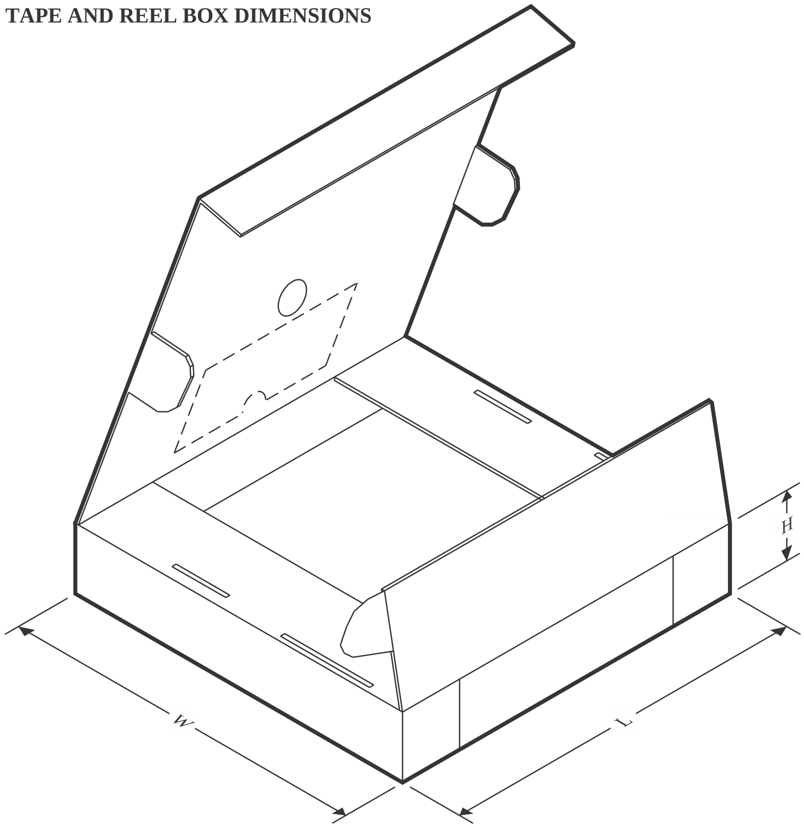
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9557DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
PCA9557DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9557DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
PCA9557DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
PCA9557PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9557PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9557RGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9557RGVRG4	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9557RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

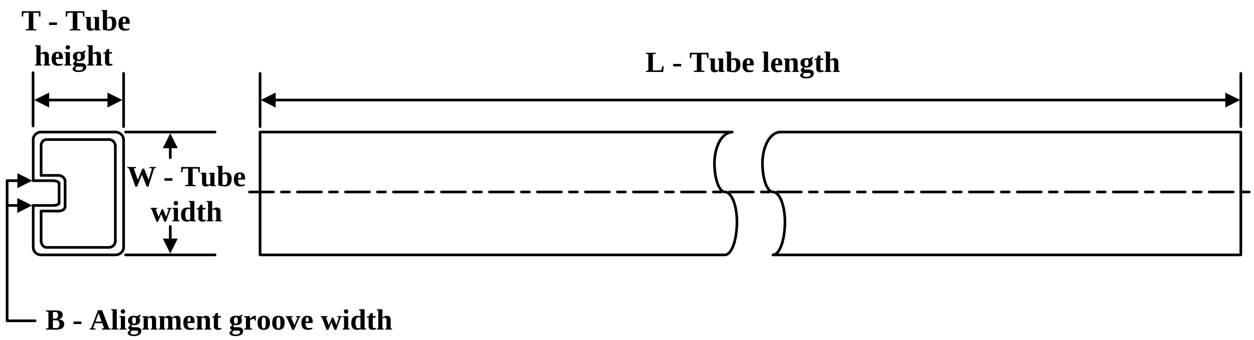
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9557DBR	SSOP	DB	16	2000	356.0	356.0	35.0
PCA9557DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
PCA9557DR	SOIC	D	16	2500	333.2	345.9	28.6
PCA9557DR	SOIC	D	16	2500	340.5	336.1	32.0
PCA9557PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9557PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9557RGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
PCA9557RGVRG4	VQFN	RGV	16	2500	356.0	356.0	35.0
PCA9557RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

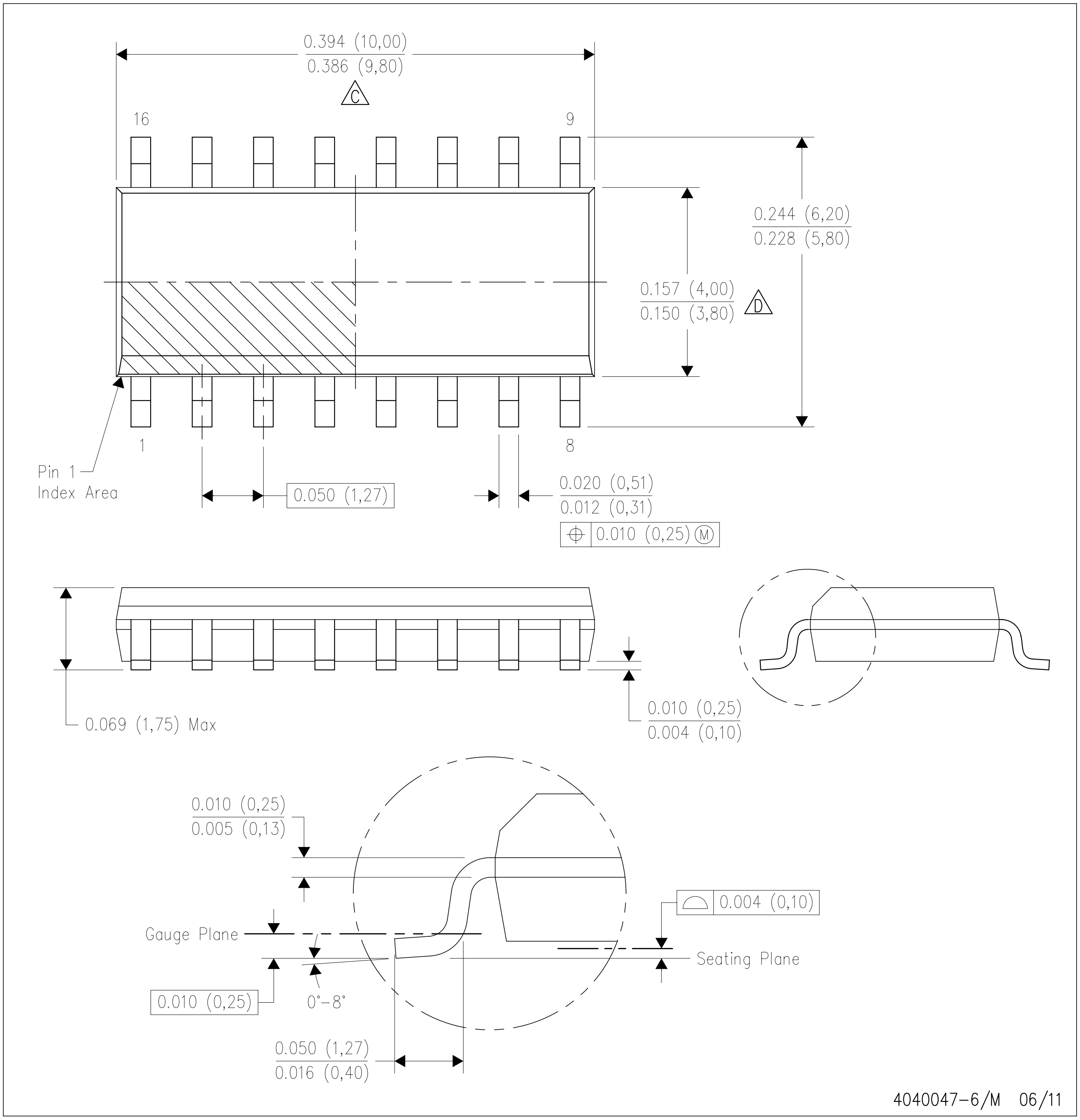
TUBE



*All dimensions are nominal

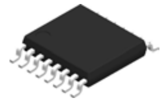
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9557DB	DB	SSOP	16	80	530	10.5	4000	4.1
PCA9557DB.A	DB	SSOP	16	80	530	10.5	4000	4.1

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



4040047-6/M 06/11

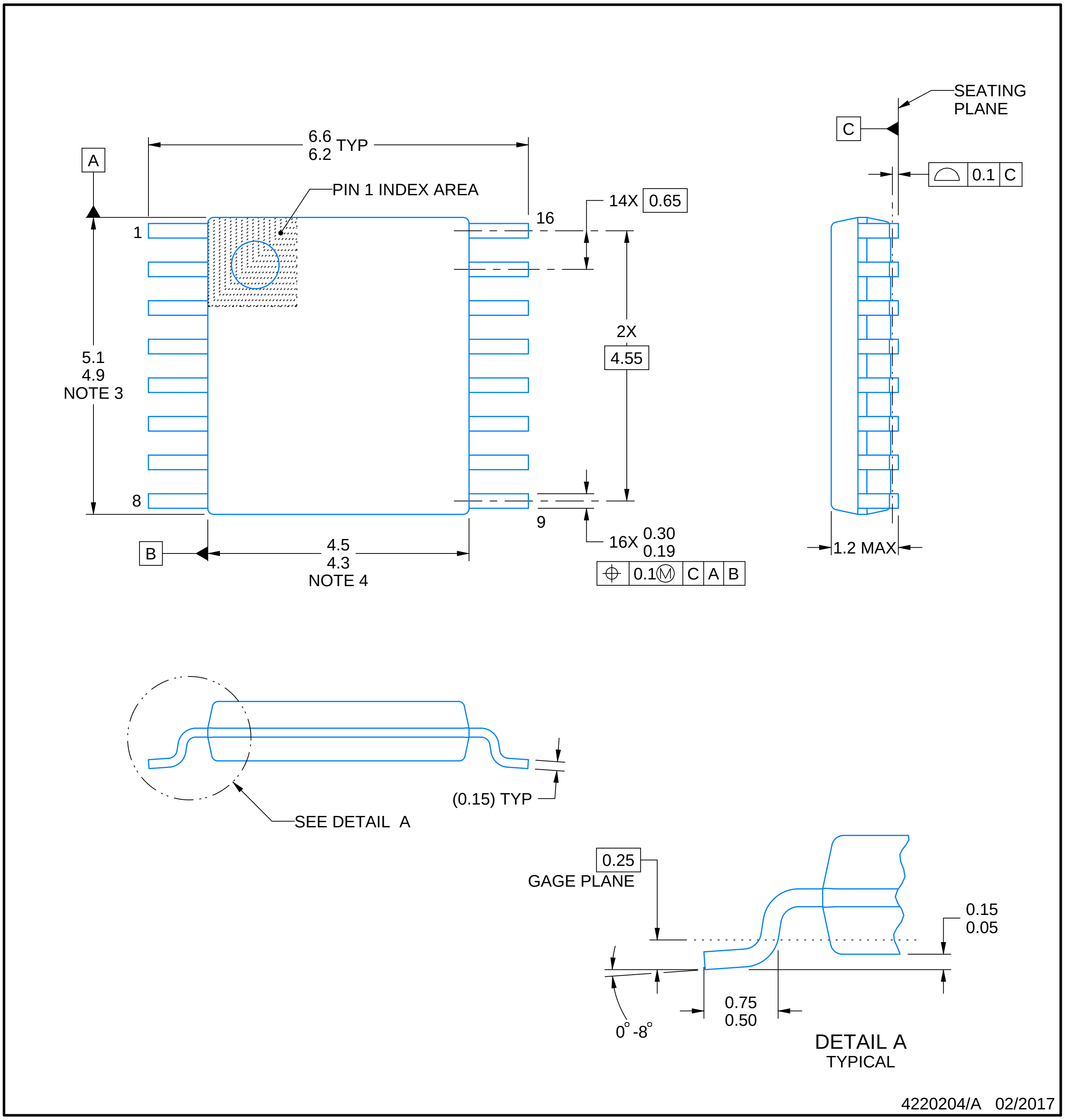
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



PACKAGE OUTLINE

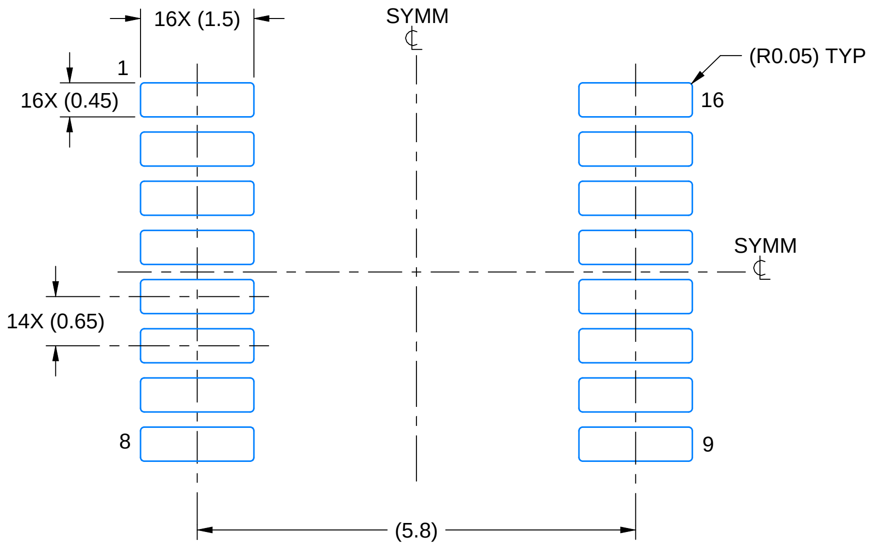
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



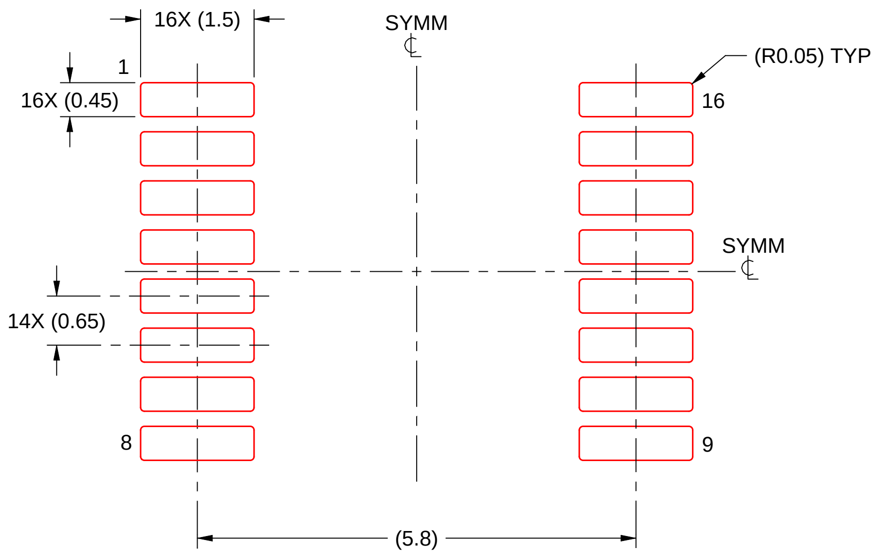
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

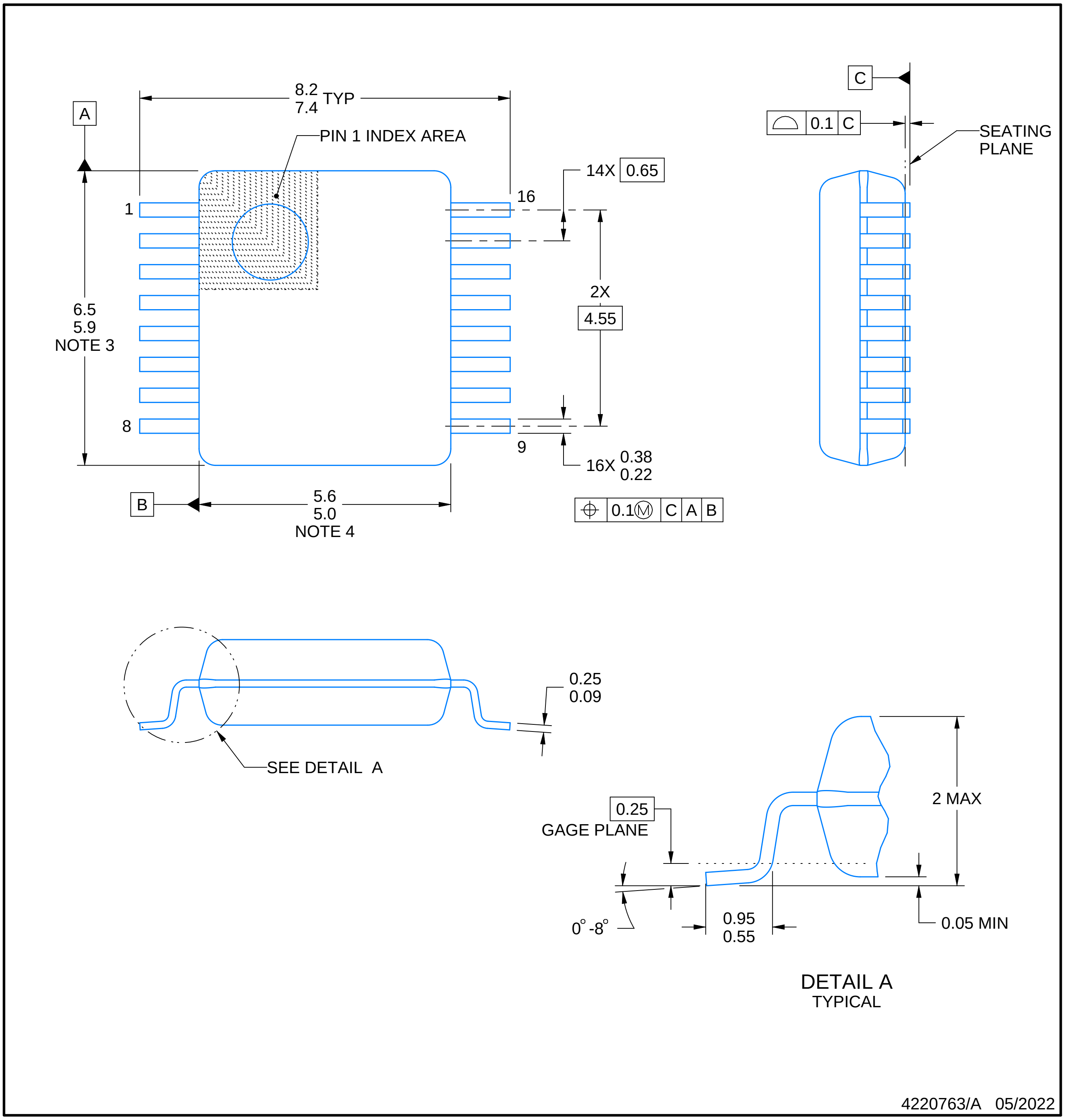
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

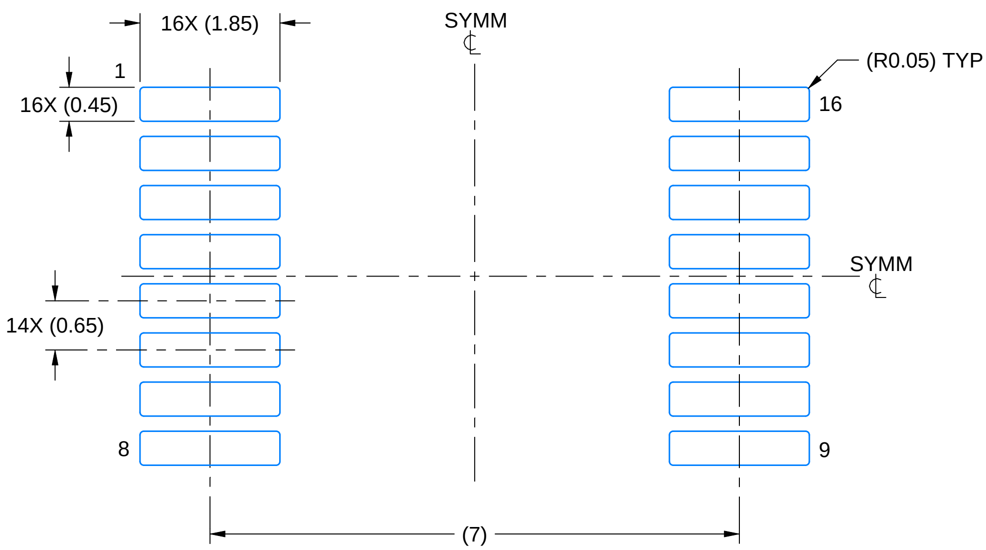
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

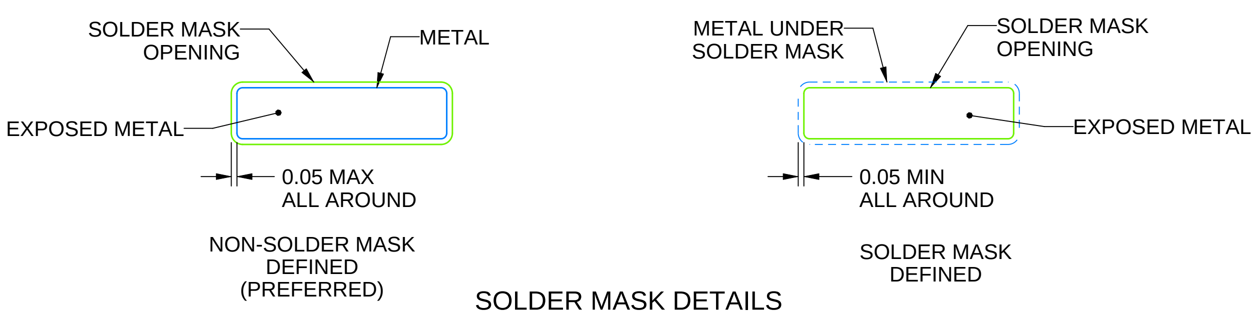


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

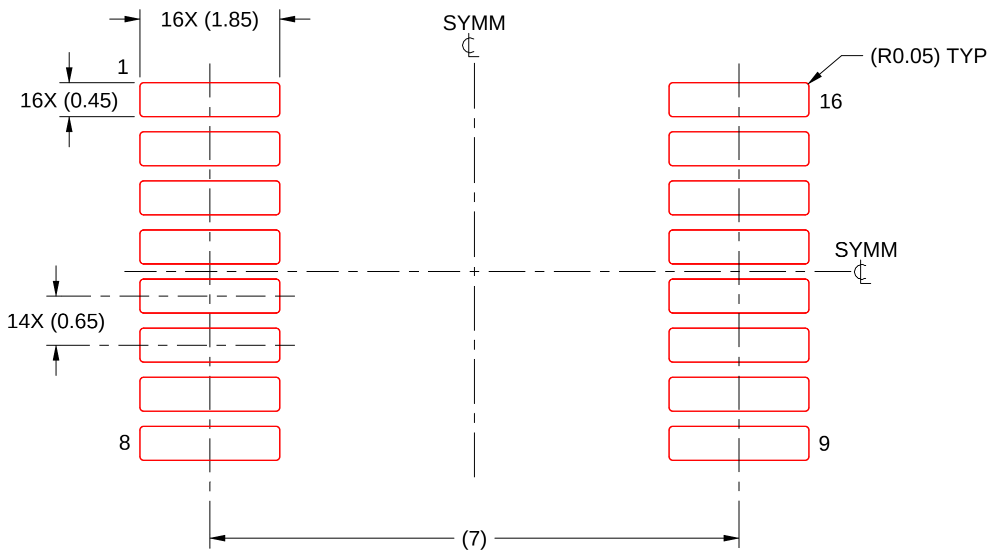


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



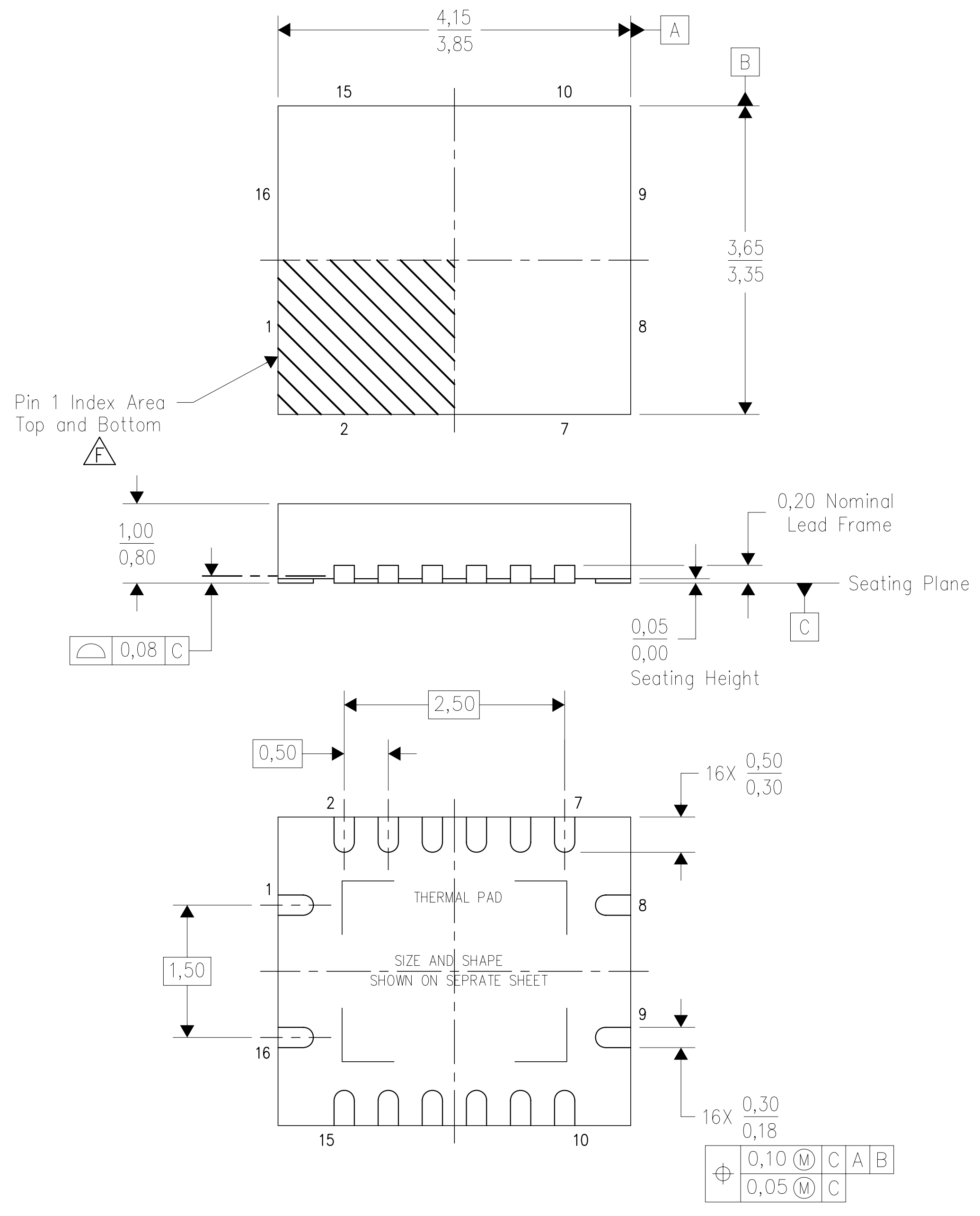
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4203539-3/I 06/2011

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO–241 variation BA.

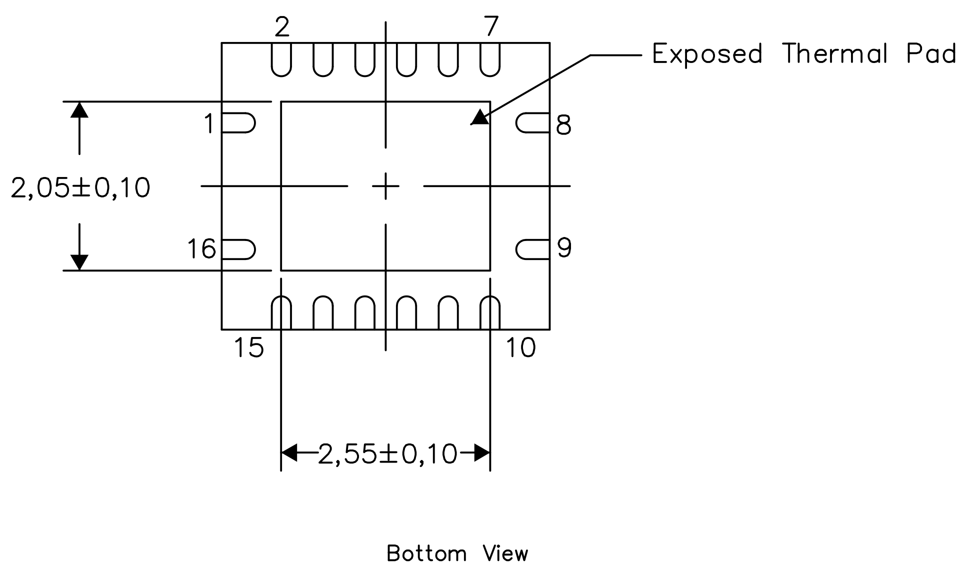
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

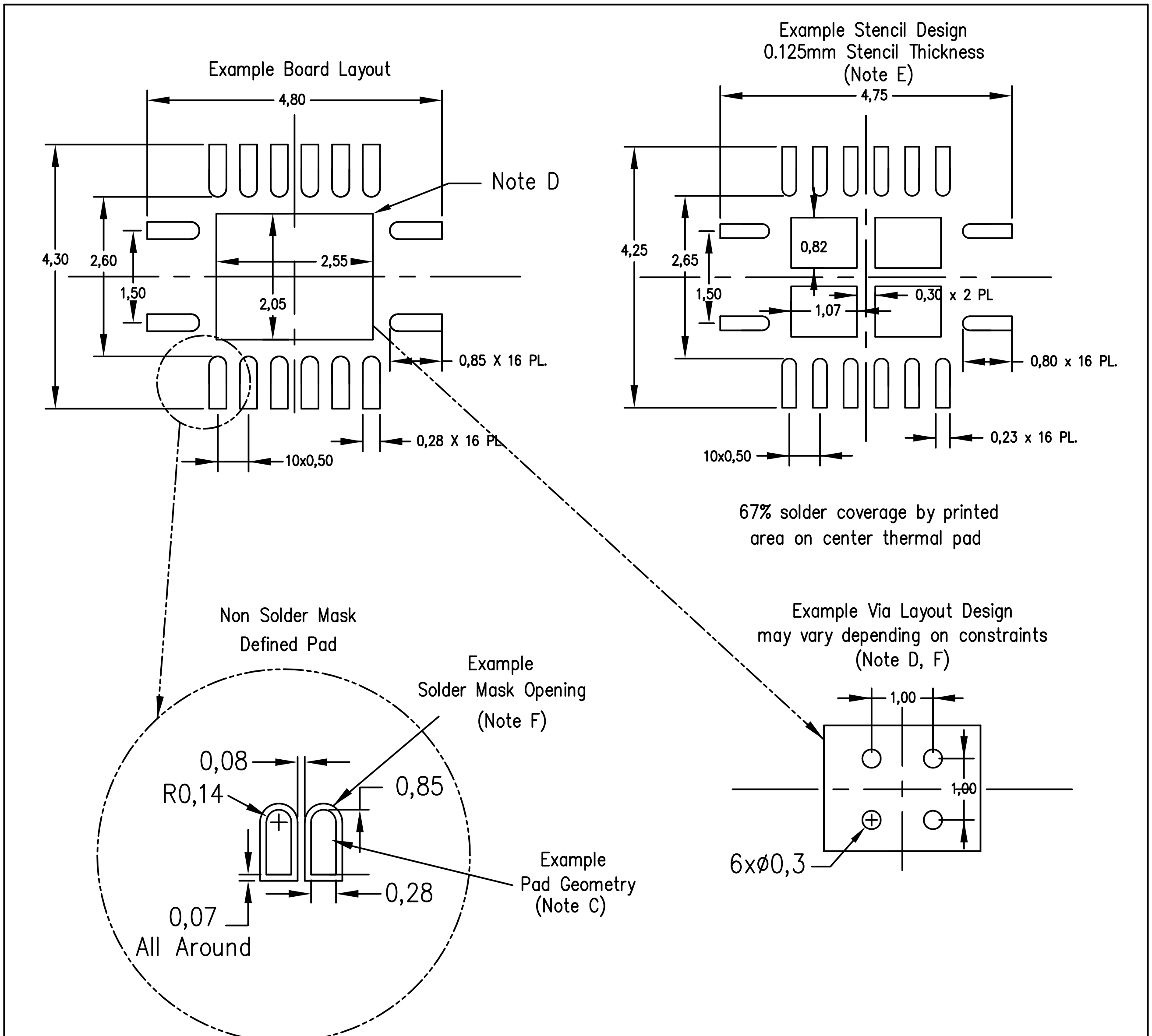


Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

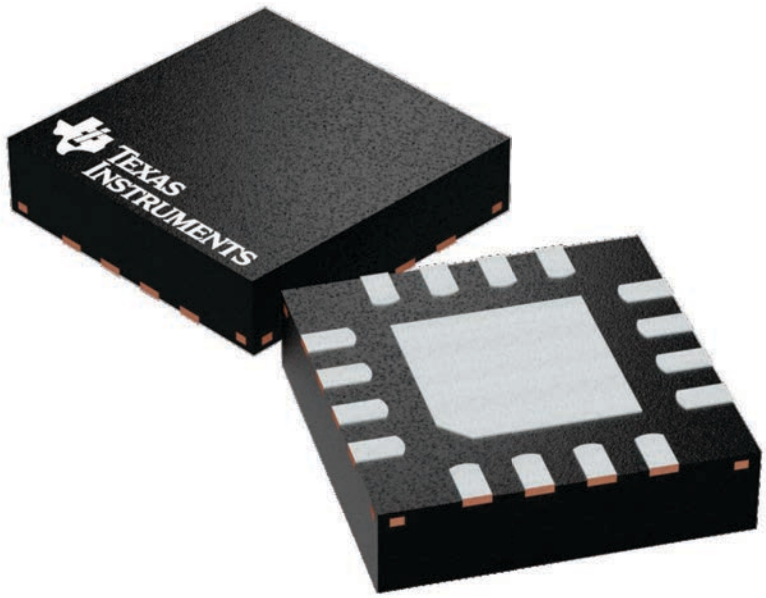
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

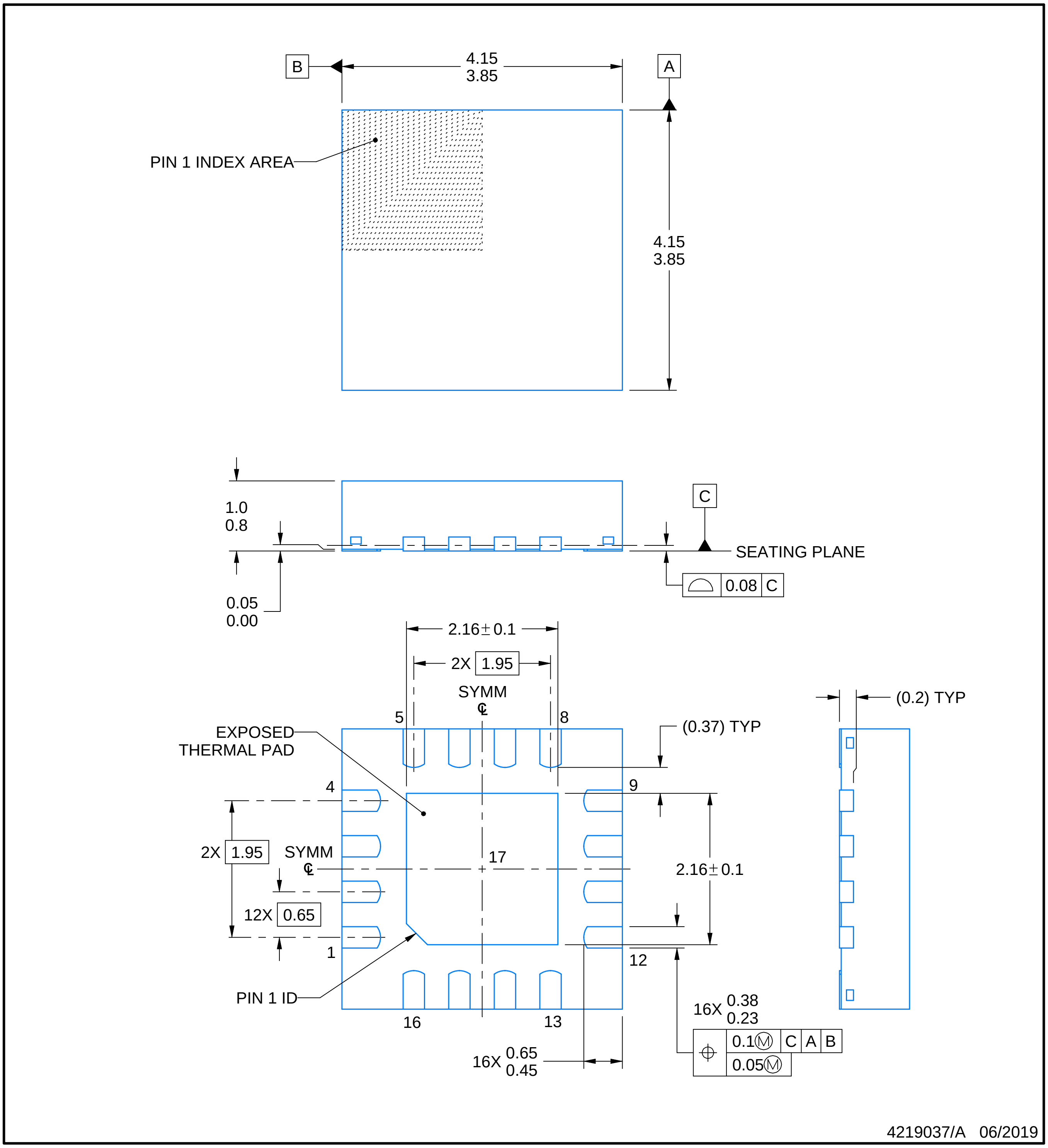
4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



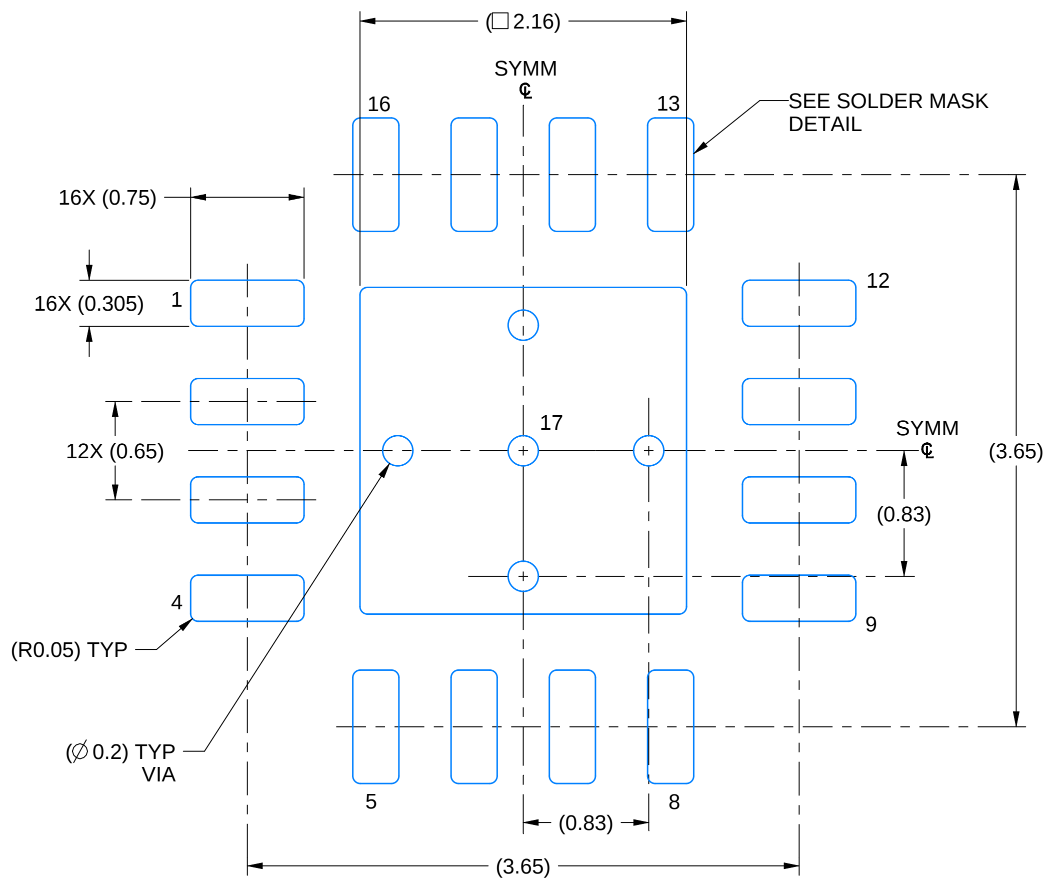
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

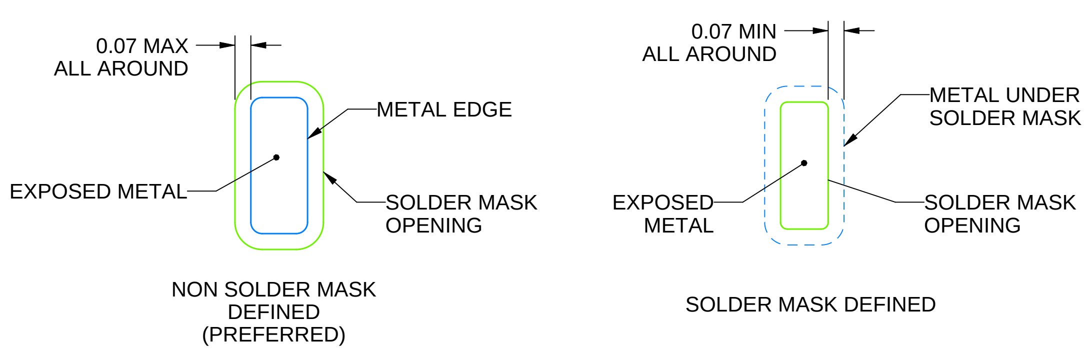


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

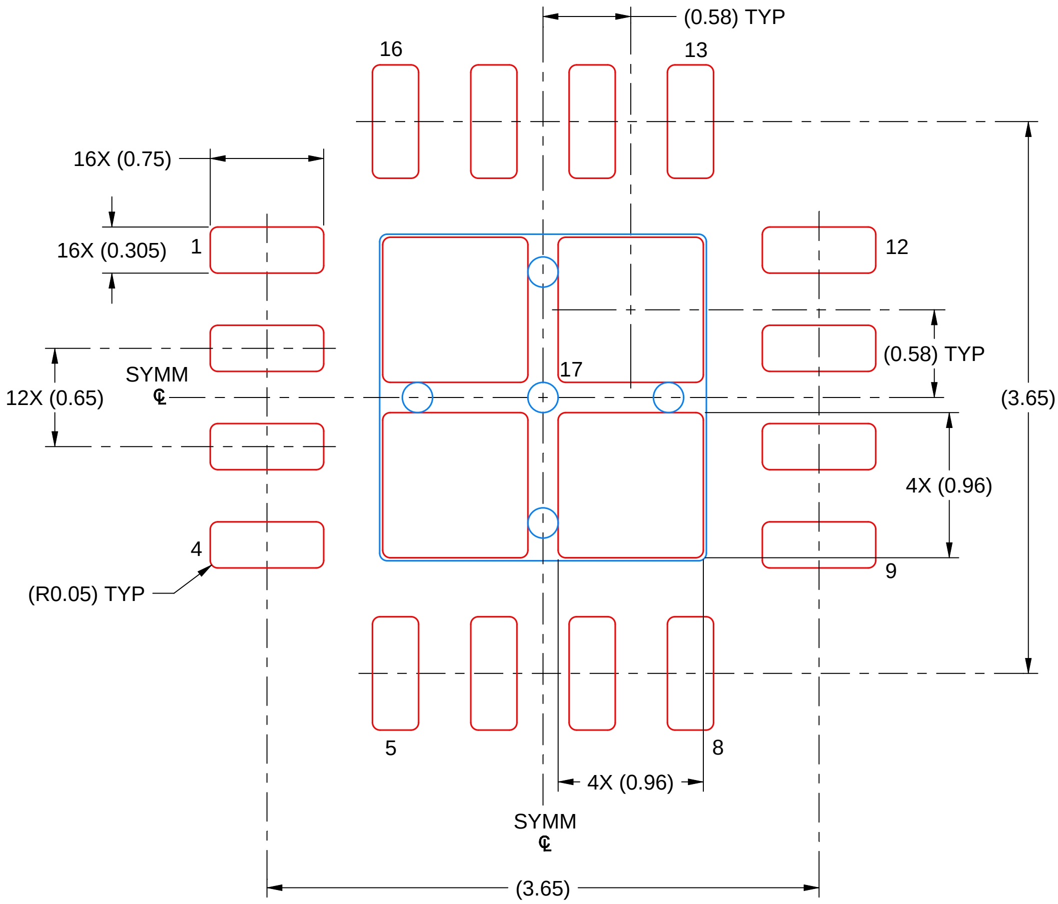


SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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