



RF430F5978 MSP430[™] System-in-Package With Sub-1-GHz Transceiver and 3D LF Wake-up and Transponder Interface

1 Device Overview

1.1 Features

- True System-In-Package Based On MSP430[™] Microcontroller With Sub-1-GHz Transceiver System-On-Chip (SoC) and Additional 3D LF Wake-up and Transponder Interface
- Wide Supply Voltage Range: 3.6 V Down To 1.8 V
- Ultra-Low Power Consumption
 - CPU Active Mode (AM): 160 µA/MHz
 - Standby Mode (LPM3 Real-Time Clock [RTC] Mode): 2.0 µA
 - Off Mode (LPM4 RAM Retention): 1.0 μA
 - Radio in Receive: 15 mA, 250 kbps, 915 MHz
- MSP430 System and Peripherals
 - 16-Bit RISC Architecture, Extended Memory, up to 20-MHz System Clock
 - Wake up From Standby Mode in Less Than 6
 µs
 - Flexible Power-Management System With SVS and Brownout
 - Unified Clock System With FLL
 - 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
 - 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
 - Hardware RTC
 - Two Universal Serial Communication Interfaces (USCIs)
 - USCI_A0 Supports UART, IrDA, SPI
 - USCI_B0 Supports I²C, SPI
 - 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan Features
 - Comparator
 - 128-Bit AES Security Encryption and Decryption Coprocessor
 - 32-Bit Hardware Multiplier
 - 3-Channel Internal DMA
 - Serial Onboard Programming, No External Programming Voltage Needed
 - Embedded Emulation Module (EEM)

- High-Performance Sub-1-GHz Radio Frequency (RF) Transceiver Core
 - Same as in CC1101
 - Wide Supply Voltage Range: 2 V to 3.6 V
 - Frequency Bands: 300 MHz to 348 MHz, 389 MHz to 464 MHz, and 779 MHz to 928 MHz
 - Programmable Data Rate From 0.6 kBaud to 500 kBaud
 - High Sensitivity (–117 dBm at 0.6 kBaud, –111 dBm at 1.2 kBaud, 315 MHz, 1% Packet Error Rate)
 - Excellent Receiver Selectivity and Blocking Performance
 - Programmable Output Power up to +12 dBm for All Supported Frequencies
 - 2-FSK, 2-GFSK, and MSK Supported as Well as OOK and Flexible ASK Shaping
 - Flexible Support for Packet-Oriented Systems: On-Chip Support for Sync Word Detection, Address Check, Flexible Packet Length, and Automatic CRC Handling
 - Support for Automatic Clear Channel Assessment (CCA) Before Transmitting (for Listen-Before-Talk Systems)
 - Digital RSSI Output
 - Suited for Systems Targeting Compliance With EN 300 220 (Europe) and FCC CFR Part 15 (US)
 - Suited for Systems Targeting Compliance With Wireless M-Bus Standard EN 13757-4:2005
 - Support for Asynchronous and Synchronous Serial Receive and Transmit Mode for Backward Compatibility With Existing Radio Communication Protocols





- High-Performance Low-Frequency (LF) Interface
 - 3D Wake-up Receiver
 - Low Standby Current Consumption: 4.4 µA
 - Regular Sensitivity Mode: 3.7 mVpp → Approximate 3-m Wake Range
 High Sensitivity Mode:
 - 0.5 mVpp \rightarrow Approximate 6-m Wake Range
 - Low Sensitivity Variation
 - Digital RSSI, 72 dB, 8-Bit Logarithmic
 - Two Independent Wake Patterns, 0-Bit to 24-Bit Length
 - Dedicated Sensitivity Levels for Both Wake
 Patterns
 - Integrated LF Bit Stream Data Decoding and Digital Data Output
 - AES-128 Hardware Encryption Coprocessor
 - Resonant Frequency: 134.2 kHz
 - Embedded Resonant Trimming for All Three Resonant Circuits

1.2 Applications

- Wireless Analog Sensor Systems
- Wireless Digital Sensor Systems
- Access Control

- 3D Transponder Interface
 - Transponder Read Range up to 4 in (10 cm), Power Received From LF RF Field
 - Half-Duplex (HDX) Communication Protocol
 - Selectable Challenge/Response Length: 32/32, 64/64, or 96/64 Bit
 - Mutual Authentication For All Commands With 32-Bit Reader Signature
 - Burst Read Mode
 - Anticollision Encryption
- EEPROM Memory Size of 2048 Bytes
 - Available User EEPROM is 1776 Bytes
 - Encryption Keys 4 x 128 Bits
 - Configurable Page Types for Selective Access Grant
 - All Pages Lockable (No Reprogramming Possible)
- Switch Interface With up to Eight Inputs
- Asset Tracking
- Smart Grid Wireless Networks

1.3 Description

The TI RF430F5978 system-in-package adds a 3D low-frequency (LF) wake-up and transponder interface to the CC430 ultra-low-power microcontroller system-on-chip (SoC) with integrated sub-1-GHz RF transceiver. This architecture allows activation and deactivation of the device in a dedicated and well-defined area "on-demand" to achieve extended battery life for the whole system. The embedded LF transponder interface is always functional even without battery supply and offers the highest level of security through its 128-bit AES encryption for challenge/response and mutual authentication. The embedded LF transponder interface also adds 2KB of programmable EEPROM memory to the system.

The CC430 ultra-low-power microcontroller system-on-chip (SoC) combines the CC1101 sub-1-GHz RF transceiver with the powerful MSP430 16-bit RISC CPU. Sixteen-bit registers and constant generators contribute to maximum code efficiency. The RF430F5978 device features the MSP430 CPUXV2, 32KB of in-system programmable flash memory, 4KB of RAM, two 16-bit timers, a high-performance 12-bit ADC with six external inputs plus internal temperature and battery sensors, a comparator, two USCIs, a 128-bit AES security accelerator, a hardware multiplier, DMA, and an RTC module with alarm capabilities.

The RF430F5978 provides a tight integration between the microcontroller core, its peripherals, software, and the integrated sub-1-GHz RF transceiver and 3D LF transceiver for wake-up and transponder interface, making these solutions easy to use while improving performance.

(4)

For complete module descriptions, see the RF430 Family User's Guide (SLAU378).

Device Information ⁽¹⁾								
PART NUMBER	PACKAGE	BODY SIZE ⁽²⁾						
RF430F5978IRGC	VQFN (64)	9 mm × 9 mm						

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com.

(2) The size shown here is an approximation. For the package dimensions with tolerances, see the *Mechanical Data* in Section 9.



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1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Chan	ges from February 12, 2013 to October 28, 2015	Page
•	Document organization and structure changes throughout, including addition of section numbering	<u>1</u> 2
٠	Added Device Information table	2
•	Moved functional block diagram to Section 1.4	3
•	Moved Table 3-1, Family Members, to Section 3, Device Characteristics	7
•	Added Section 5.2, ESD Ratings	. 12
•	Added note to the C _{VCORE} parameter in Section 5.3, Recommended Operating Conditions	. 12
•	Added Section 5.8, Thermal Resistance Characteristics	. 17
•	Corrected spelling of MRG bits in f _{MCLK,MRG} parameter symbol and description in Section 5.38, Flash Memory Changed the "RF crystal oscillator only" test conditions and added note in Section 5.42, Current Consumption,	. <u>38</u>
	Reduced-Power Modes	. <u>39</u>
•	Changed the TYP value of the "High-bit transmit frequency" parameter in Section 5.67, Resonant Circuits – LF Front End, from 134.2 to 124.2	. 54
•	Changed the limits for the trimming capacitor parameters CT _{max} , CT1, CT2, CT3, CT4, CT5, CT6, and CT7 in	· · ·
	Section 5.69, Resonant Circuit Capacitor – LF Front End	· <u>54</u>
•	Changed all instances of "bootstrap loader" to "bootloader"	• <u>64</u>
•	Corrected spelling of NMIIFG (added missing "I") in Table 6-10, System Module Interrupt Vector Registers	• <u>69</u>
•	Added Section 8, Device and Documentation Support	<u>102</u>
•	Added Section 9, Mechanical, Packaging, and Orderable Information	104



3 Device Characteristics

Table 3-1 summarizes the device characteristics.

Table 3-1. Family Members

					LF INTER	FACE	US	SCI				
DEVICE	PROGRAM (KB)	SRAM (KB)	EEPROM (Byte)	Timer_A ⁽¹⁾	TRANSPONDER CHANNELS	WAKE RECEIVER CHANNELS	CHANNEL A: UART, LIN, IrDA, SPI	CHANNEL B: SPI, I ² C	ADC12_A CHANNELS	Comp_B CHANNELS	I/O	PACKAGE
RF430F5978	32	4	1776	5, 3	3	3	1	1	8 ext, 4 int	8	27	64 RGC

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 5, 3 would represent two instantiations of Timer_A, the first instantiation having 5 and the second instantiation having 3 capture compare registers and PWM output generators, respectively.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout of the 64-pin RGC package.

			P2.1/A1	P2.2/A2	P2.4/A4	P2.5/A5	AVCC	P5.0/XOUT	P5.1/XIN	AGND	DGND	DVCC	RESET	TEST	PJ3/TCK	PJ2/TMS	PJ1/TDI	PJ0/TDO		
			64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49		
	(\bigcirc		Ē	Ū	Ū	П Ц U	110	5	U	00	0	Ц Ц	Ū	П U	0	U			
P2.0/A0	1	:0	Г														_	CII 4	8 RF_AVCC	
P1.7/UCA_CLK	2	:0																CII 4	7 RF_RBIAS	
P1.6/UCA_SIMO	3 = =	0	I															CII 4	6 RF_AVCC	
P1.5/UCA_SOMI	4	0																CII 4	5 RF_GND	
VCORE	5	0															 	CII 44	4 RF_N	
DVCC	6	: 2	i I															CII 43	3 RF_P	
P1.4/UCB_CLK	7	:0																CII 4:	2 RF_GND	
P1.3/UCB_SIMO	8	:0															 	<== 4	1 RF_AVCC	
P1.2/UCB_SOMI	9	50																CII 4	0 RF_GND	
P1.1/RF_GDO2	10 🗔	50																CII 3	9 RF_AVCC	
P1.0/RF_GD00	11 = 1	10																CII 3	8 RF_XOUT	
P3.7/PM SMCLK	12 = 1	10																CII 3	7 RF_XIN	
AFE_VCL	13 🗔	10																CII 3	6 SW7	
AFE RF1	14	:0																CII 3	5 SW6	
AFE RF2	15																	CII 34	4 SW5	
AFE RF3	16	10															-	CII 3	3 P4.0/RF_ATES	31
_ 1																		\cap		
			17 ጉ	18 ጉ	19 ጉ	20 ≻	21 ≻	22 ≻	23	24	25	26	27	28	29	30	31	32		
			VFE_GND	VFE_TEN	VFE_DAT	VFE_TCLK	VFE_ACTI	VFE_VCCS	/BAT	INDA	VAKE	ń	ŝWO	\$W1	3W2	\$W3	3W4	ົດ		
								š												

NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. This pinout shows the default mapping. See Table 6-8 for details.

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4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Terminal Functions

TERMINAL			DESCRIPTION				
NAME	NO.	1/0					
			General-purpose digital I/O with port interrupt and mappable secondary function				
			Default mapping: Comparator_B output				
P2.0/PM_CBOUT1/PM_TA1CLK/	1	I/O	Default mapping: Timer1_A3 clock input				
			Comparator input CB0				
			Analog input A0 – 12-bit ADC				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	2	I/O	Default mapping: USCI_A0 clock input/output				
			Default mapping: USCI_B0 SPI slave transmit enable				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	3	I/O	Default mapping: USCI_A0 UART transmit data				
			Default mapping: USCI A0 SPI slave in/master out				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	4	I/O	Default mapping: USCI_A0 UART receive data				
PM_UCAURXD/PM_UCAUSOMI			Default mapping: USCI_A0 SPI slave out/master in				
VCORE	5	S	Regulated core power supply				
DVCC	6	s	Digital power supply				
			General-purpose digital I/O with port interrupt and mappable secondary function				
P1.4/	7	I/O	Default mapping: USCI_B0 clock input/output				
FM_0CB0CER/FM_0CA0STE			Default mapping: USCI_A0 SPI slave transmit enable				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	8	I/O	Default mapping: USCI_B0 SPI slave in/master out				
			Default mapping: USCI B0 I ² C data				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	9	I/O	Default mapping: USCI_B0 SPI slave out/master in				
			Default mapping: UCSI B0 I ² C clock				
			General-purpose digital I/O with port interrupt and mappable secondary function				
P1.1/PM_RFGDO2	10	I/O	Default mapping: Radio GDO2 output				
			General-purpose digital I/O with port interrupt and mappable secondary function				
P1.0/PM_RFGDO0	11	I/O	Default mapping: Radio GDO0 output				
			General-purpose digital I/O with port interrupt and mappable secondary function				
P3.7/PM_SMCLK	12	1/0	Default mapping: SMCLK output				
AFE_VCL	13	А	Charge capacitor and supply voltage for immobilizer mode				
AFE_RF1	14	А	Connection for resonant circuit 1				
AFE_RF2	15	Α	Connection for resonant circuit 2				
AFE_RF3	16	Α	Connection for resonant circuit 3				
AFE_GND	17		Analog LF front end GND				
AFE_TEN	18		Test interface enable of analog LF front end				
AFE_TDAT	19	1/O	I est interface data of analog LF front end				
AFE_TCLK	20		I est interface clock of analog LF front end				
AFE_ACTI	21	A	lest interface output of analog front end				

(1) I = input, O = output, S = supply, G = ground

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TERMINAL			DESCRIPTION						
NAME	NO.	1/0(*)	DESCRIPTION						
AFE_VCCSW	22	А	Switched power supply buffer (external capacitor)						
VBAT	23	S	Supply voltage analog front end						
GNDA	24	G	Analog ground						
WAKE	25	0	Analog ground						
NC	26		Not connected						
SW0	27	I	Switch input with internal pullup resistor						
SW1	28	I	Switch input with internal pullup resistor						
SW2	29	I	Switch input with internal pullup resistor						
SW3	30	I	Switch input with internal pullup resistor						
SW4	31	I	Switch input with internal pullup resistor						
NC	32		Not connected						
P4.0	33	I/O	General-purpose digital I/O						
SW5	34	I	Switch input with internal pullup resistor						
SW6	35	I	Switch input with internal pullup resistor						
SW7	36	I	Switch input with internal pullup resistor						
RF_XIN	37	Ι	Input terminal for RF crystal oscillator or external clock input						
RF_XOUT	38	0	Output terminal for RF crystal oscillator						
RF_AVCC	39	S	Radio analog power supply						
RF_GND	40	G	Radio ground						
RF_AVCC	41	S	Radio analog power supply						
RF_GND	42	G	Radio ground						
		RF	Positive RF input to LNA in receive mode						
RF_P	43	I/O	Positive RF output from PA in transmit mode						
DE N	11	RF	Negative RF input to LNA in receive mode						
Kr_N	44	I/O	Negative RF output from PA in transmit mode						
RF_GND	45	G	Radio ground						
RF_AVCC	46	S	Radio analog power supply						
RF_RBIAS	47		External bias resistor for radio reference current						
RF_AVCC	48	I/O	Radio analog power supply						
PJ.0/TDO	49	I/O	General-purpose digital I/O or test data output port						
PJ.1/TDI/TCLK	50	I/O	General-purpose digital I/O or test data input or test clock input						
PJ.2/TMS	51	I/O	General-purpose digital I/O or test mode select						
PJ.3/TCK	52	I/O	General-purpose digital I/O or test clock						
TEST/SBWTCK	53	I	Test mode pin – select digital I/O on JTAG pins or Spy-Bi-Wire input clock						
			Reset input active low						
RST/NMI/SBWTDIO	54	I/O	Nonmaskable interrupt input						
			Spy-Bi-Wire data input/output						
DVCC	55	S	Digital power supply						
DGND	56	G	Digital ground supply						
AGND	57	G	Analog ground supply						
	50	1/0	General-purpose digital I/O						
P5.1/XUU1	58	1/0	Output terminal of crystal oscillator XT1						
			General-purpose digital I/O						
P5.0/XIN	59	I/O	Input terminal for crystal oscillator XT1						
AVCC	60	S	Analog power supply						

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TERMINAL			DESCRIPTION				
NAME	NO.	1/0 (/	DESCRIPTION				
			General-purpose digital I/O with port interrupt and mappable secondary function				
			Default mapping: SVM output				
P2.5/PM_SVMOUT/CB5/A5/	61	1/0	Comparator input CB5				
VREF+/VeREF+	01	1/0	Analog input A5 – ADC				
			Output of positive reference voltage				
			Input for an external positive reference voltage to the ADC				
			General-purpose digital I/O with port interrupt and mappable secondary function				
			Default mapping: RTCCLK output				
P2.4/PM_RTCCLK/CB4/A4/ VREF-	62	1/0	Comparator input CB4				
/VeREF-	02	1/0	Analog input A4 – ADC				
			Output of negative reference voltage				
			Input for an external negative reference voltage to the ADC				
			General-purpose digital I/O with port interrupt and mappable secondary function				
D2 2/DM TA1CCD1A/CD2/A2	62	1/0	Default mapping: TA1 CCR1 compare output/capture input				
	05	1/0	Comparator input CB2				
			Analog input A2 – ADC				
			General-purpose digital I/O with port interrupt and mappable secondary function				
	64	1/0	Default mapping: TA1 CCR0 compare output/capture input				
F2.1/FM_TATCCR0A/CB1/AT	04	1/0	Comparator input CB1				
			Analog input A1 – ADC				
			Ground supply				
Exposed die attach pad			The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.				

Table 4-1. Terminal Functions (continued)

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC/VBAT and AVCC pins to V_{SS}	-0.3	3.6	V
Voltage applied to any pin (excluding VCORE, RF_P, RF_N, and R_BIAS) ⁽²⁾	-0.3	V _{CC} + 0.3 4.1 V Max	V
Voltage applied to VCORE, RF_P, RF_N, and R_BIAS ⁽²⁾	-0.3	2	V
Input RF level at pins RF_P and RF_N		10	dBm
Diode current at any device terminal		±2	mA
Storage temperature ⁽³⁾ , T _{stg}	-55	125	°C
Maximum junction temperature, T _J		95	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}.

(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatia discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
Vec	Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾ during program execution and flash programming	PMMCOREVx = 0 (default after POR)	1.8		3.6	V	
	with PMM default settings. Radio is not operational with PMMCOREVx = 0, 1. ⁽²⁾⁽³⁾	PMMCOREVx = 1	2.0		3.6	3.6	
	Supply voltage range applied at all DVCC and AVCC	PMMCOREVx = 2	2.2		3.6		
V _{CC}	pins ⁽¹⁾ during program execution, flash programming, and radio operation with PMM default settings. ⁽²⁾⁽³⁾ Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾ during program execution, flash programming, and	PMMCOREVx = 3	2.4		3.6	V	
V _{CC}	Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾ during program execution, flash programming, and radio operation with PMMCOREVx = 2, high-side SVS level lowered (SVSHRVLx = SVSHRRRLx = 1) or high-side SVS disabled (SVSHE = 0). ⁽⁴⁾ (²⁾ (³⁾	PMMCOREVx = 2, SVSHRVLx = SVSHRRRLx = 1 or SVSHE = 0	2.0		3.6	V	
V _{SS}	Supply voltage applied at the exposed die attach VSS and A	VSS pin		0		V	
T _A	Operating free-air temperature		-40		85	°C	
TJ	Operating junction temperature		-40		85	°C	
C _{VCORE}	Recommended capacitor at VCORE ⁽⁵⁾		470		nF		
C _{DVCC} / C _{VCORE}	Capacitor ratio of capacitor at DVCC to capacitor at VCORE		10				

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.

(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.

(3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.19 threshold parameters for the exact values and further details.

(4) Lowering the high-side SVS level or disabling the high-side SVS might cause the LDO to operate out of regulation, but the core voltage stays within its limits and is still supervised by the low-side SVS to ensure reliable operation.

(5) A capacitor tolerance of $\pm 20\%$ or better is required.

12 Specifications



Recommended Operating Conditions (continued)

Typical values are specified at V_{CC} = 3.3 V and T_{A} = 25°C (unless otherwise noted)

			MIN	NOM MAX	UNIT	
fsystem		PMMCOREVx = 0 (default condition)	0	0 8		
	Processor (MCLK) frequency ⁽⁶⁾ (see Figure 5-1)	PMMCOREVx = 1	0	12	MHz	
		PMMCOREVx = 2	0	16		
		PMMCOREVx = 3	0	20		
PINT	Internal power dissipation		V _C	$V_{CC} \times I_{(DVCC)}$		
P _{IO}	I/O power dissipation of I/O pins powered by DVCC		(V _{CC} –	V _{IOH}) × I _{IOH} + ′ _{IOL} × I _{IOL}	W	
P _{MAX}	Maximum allowed power dissipation, P _{MAX} > P _{IO} + P _{INT}		(T _J -	– Τ _Α) / Rθ _{JA}	W	

(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Supply Voltage (V)

NOTE: The numbers (0, 1, 2, and 3) in the fields are the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{cc} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

PARAMETER									FRE		CY (f _{DC}	o = f _{MCI}	_{LK} = f _{SN}	ICLK)			
	EXECUTION	V _{cc}	V _{CC} PMMCOREVx	1 N	/Hz	8 N	/Hz	12 I	MHz	16 I	MHz	20 1	MHz	UNIT			
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX				
. (4)		Fleeb 2.V		0	0.23	0.26	1.35	1.60									
	Flash		Fleeh	Floop	2.1/	1	0.25	0.28	1.55		2.30	2.65					A
IAM, Flash` '			2	0.27	0.30	1.75		2.60		3.45	3.90			mA			
			3	0.28	0.32	1.85		2.75		3.65		4.55	5.10				
			0	0.18	0.20	0.95	1.10										
I (5)	DAM	2.1/	1	0.20	0.22	1.10		1.60	1.85					A			
IAM, RAM	RAM	3 V	2	0.21	0.24	1.20		1.80		2.40	2.70			mA			
			3	0.22	0.25	1.30		1.90		2.50		3.10	3.60				

(1)

All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load (2)capacitance are chosen to closely match the required 12.5 pF.

Characterized with program executing typical data processing. (3) $f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency. XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

(4) Active mode supply current when program executes in flash at a nominal supply voltage of 3 V.

Active mode supply current when program executes in RAM at a nominal supply voltage of 3 V. (5)

Typical Characteristics – Active Mode Supply Currents 5.5



Figure 5-2. Active Mode Supply Current vs MCLK Frequency

Low-Power Mode Supply Currents (Into V_{cc}) Excluding External Current 5.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

				TEMPERATURE (T _A)								
	PARAMETER	V _{cc}	PMMCOREVx	-40	°C	25	°C	60	°C	85	°C	UNIT
				ТҮР	MAX	ТҮР	MAX	TYP	MAX	TYP	MAX	
	Low nower mode $O^{(3)}(4)$	2.2 V	0	80	100	80	100	80	100	80	100	
LPM0,1MHz	Low-power mode 0 (1777)	3 V	3	90	110	90	110	90	110	90	110	μΑ
	Low power mode 2 ⁽⁵⁾ ⁽⁴⁾	2.2 V	0	6.5	11	6.5	11	6.5	11	6.5	11	
ILPM2 Low-power mode 2	Low-power mode 2010	3 V	3	7.5	12	7.5	12	7.5	12	7.5	12	μΑ
	Low-power mode 3, crystal mode ^{(6) (4)}		0	1.8		2.0	2.6	3.0	4.0	4.4	5.9	
I _{LPM3,XT1LF}		3 V	1	1.9		2.1		3.2		4.8		
			2	2.0		2.2		3.4		5.1		μΛ
			3	2.0		2.2	2.9	3.5	4.8	5.3	7.4	
			0	0.9		1.1	2.3	2.1	3.7	3.5	5.6	
	Low-power mode 3,	2.1/	1	1.0		1.2		2.3		3.9		
LPM3,VLO	VLO mode ⁽⁷⁾ (4)	3 V	2	1.1		1.3		2.5		4.2		μΑ
			3	1.1		1.3	2.6	2.6	4.5	4.4	7.1	
			0	0.8		1.0	2.2	2.0	3.6	3.4	5.5	
	Low nower mode $A^{(8)}$ (4)	2.1/	1	0.9		1.1		2.2		3.8		
ILPM4	Low-power mode 4 (*) (*)	зv	2	1.0		1.2		2.4		4.1		μΑ
			3	1.0		1.2	2.5	2.5	4.4	4.3	7.0	

 All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
 The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). (3)

 $\begin{array}{l} \mathsf{CPUOFF} = 1, \ \mathsf{SCG0} = 0, \ \mathsf{SCG1} = 0, \ \mathsf{OSCOFF} = 0 \ (\mathsf{LPM0}), \ f_{\mathsf{ACLK}} = 32768 \ \mathsf{Hz}, \ f_{\mathsf{MCLK}} = 0 \ \mathsf{MHz}, \ f_{\mathsf{SMCLK}} = f_{\mathsf{DCO}} = 1 \ \mathsf{MHz} \\ \mathsf{Current} \ \mathsf{for} \ \mathsf{brownout}, \ \mathsf{high} \ \mathsf{side} \ \mathsf{supervisor} \ (\mathsf{SVS}_{\mathsf{H}}) \ \mathsf{normal} \ \mathsf{mode} \ \mathsf{included}. \ \mathsf{Low-side} \ \mathsf{supervisor} \ (\mathsf{SVS}_{\mathsf{L}}) \ \mathsf{and} \ \mathsf{low-side} \ \mathsf{monitor} \ (\mathsf{SVM}_{\mathsf{L}}) \\ \end{array}$ (4)disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DC0} = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.

Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). (6) Content for watchdog timer and KTC clocked by ACLK included. ACLK = 10th requests stylear operation (KTC = 0) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(7)

- (8)



5.7 Typical Characteristics – Low-Power Mode Supply Currents



5.8 Thermal Resistance Characteristics

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
Rθ _{JA}	Junction-to-ambient thermal resistance, still air ⁽¹⁾		24.6	°C/W
R _{θJC(TOP)}	Junction-to-case (top) thermal resistance ⁽²⁾		8.8	°C/W
R _{θJC(BOT)}	Junction-to-case (bottom) thermal resistance ⁽³⁾		0.9	°C/W
Rθ _{JB}	Junction-to-board thermal resistance ⁽⁴⁾	VQFN-04 (KGC)	3.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		3.8	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.1	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(3) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.9 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
V	Desitive going input threaded valtage		1.8 V	0.80		1.40	V
VIT+	Positive-going input theshold voltage		3 V	1.50		2.10	v
V	Negative going input threshold veltage		1.8 V	0.45		1.00	V
VIT-	Negative-going input theshold voltage		3 V	0.75		1.65	v
V _{hys}	Input voltage hysteresis (V _{IT+} - V _{IT-})		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	V
R _{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
CI	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
I _{lkg(Px.y)}	High-impedance leakage current	(1) (2)	1.8 V, 3 V			±50	nA
t _(int)	External interrupt timing (external trigger pulse duration to set interrupt flag) $^{(3)}$	Ports with interrupt capability (see block diagram and terminal function descriptions).	1.8 V, 3 V	20			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.10 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	MAX	UNIT	
		$I_{(OHmax)} = -1 \text{ mA}, \text{ PxDS.y} = 0^{(2)}$	4.0.)/	V _{CC} - 0.25	V _{CC}		
V	High-level output voltage,	$I_{(OHmax)} = -3 \text{ mA}, \text{ PxDS.y} = 0^{(3)}$	1.8 V	$V_{CC} - 0.60$	V _{CC}	N	
VOH	reduced drive strength ⁽¹⁾	$I_{(OHmax)} = -2 \text{ mA}, \text{ PxDS.y} = 0^{(2)}$	0.)/	V _{CC} - 0.25	V _{CC}	v	
		$I_{(OHmax)} = -6 \text{ mA}, \text{ PxDS.y} = 0^{(3)}$	3 V	V _{CC} - 0.60	V _{CC}		
		$I_{(OLmax)} = 1 \text{ mA}, \text{ PxDS.y} = 0^{(2)}$	4.0.)/	V _{SS}	V _{SS} + 0.25		
V	Low-level output voltage,	$I_{(OLmax)} = 3 \text{ mA}, \text{ PxDS.y} = 0^{(3)}$	1.8 V	V _{SS}	V _{SS} + 0.60	V	
VOL	reduced drive strength ⁽¹⁾	$I_{(OLmax)} = 2 \text{ mA}, \text{ PxDS.y} = 0^{(2)}$	2.1/	V _{SS}	V _{SS} + 0.25		
		$I_{(OLmax)} = 6 \text{ mA}, \text{ PxDS.y} = 0^{(3)}$	3 V	V _{SS}	V _{SS} + 0.60		
		$I_{(OHmax)} = -3 \text{ mA}, \text{ PxDS.y} = 1^{(2)}$	4.0.)/	V _{CC} - 0.25	V _{CC}		
V	High-level output voltage,	$I_{(OHmax)} = -10 \text{ mA}, \text{ PxDS.y} = 1^{(3)}$	1.8 V	V _{CC} - 0.60	V _{CC}	N	
V _{OH}	full drive strength	$I_{(OHmax)} = -5 \text{ mA}, \text{ PxDS.y} = 1^{(2)}$	2.1/	V _{CC} - 0.25	V _{CC}	v	
		$I_{(OHmax)} = -15 \text{ mA}, \text{ PxDS.y} = 1^{(3)}$	3 V	$V_{CC} - 0.60$	V _{CC}		
		$I_{(OLmax)} = 3 \text{ mA}, \text{ PxDS.y} = 1^{(2)}$	1.0.)/	V _{SS}	V _{SS} + 0.25		
V	Low-level output voltage,	$I_{(OLmax)} = 10 \text{ mA}, \text{PxDS.y} = 1^{(3)}$	1.0 V	V _{SS}	$V_{SS} + 0.60$		
VOL	full drive strength	$I_{(OLmax)} = 5 \text{ mA}, \text{ PxDS.y} = 1^{(2)}$	2.1/	V _{SS}	V _{SS} + 0.25	v	
		$I_{(OLmax)} = 15 \text{ mA}, \text{PxDS.y} = 1^{(3)}$	3 V	V _{SS}	V _{SS} + 0.60		
f	Port output frequency	$C = 20 \text{ pc} \text{ B} \frac{(4)}{(5)}$	$V_{CC} = 1.8 V,$ PMMCOREVx = 0		16		
IPx.y	(with load)	$C_{L} = 20 \text{ pr}, R_{L} (7, 5)$	V _{CC} = 3 V, PMMCOREVx = 2		25		
4			$V_{CC} = 1.8 V,$ PMMCOREVx = 0		16	N 41 1-	
^I Port_CLK	Clock output frequency	Clock output frequency $C_L = 20 \text{ pF}^{(5)}$		$V_{CC} = 3 V,$ PMMCOREVx = 2		25	IVIHZ

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

(4) A resistive divider with 2 x R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω . For reduced drive strength, R1 = 1.6 k Ω . C_L = 20 pF is connected to the output to V_{SS}.

(5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.



5.11 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

5.12 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)



5.13 Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			0.075		
ΔI _{DVCC.LF}	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	$\label{eq:f_OSC} \begin{array}{l} f_{OSC} = 32768 \mbox{ Hz}, \mbox{ XTS} = 0, \\ \mbox{ XT1BYPASS} = 0, \mbox{ XT1DRIVEx} = 2, \\ \mbox{ T}_A = 25^{\circ}\mbox{C} \end{array}$	3 V		0.170		μA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C	_		0.290		
f _{XT1,LF0}	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
f _{XT1,LF,SW}	XT1 oscillator logic-level square- wave input frequency, LF mode	$XTS = 0, XT1BYPASS = 1^{(2)}$ (3)		10	32.768	50	kHz
OA _{LF}	Oscillation allowance for LF crystals ⁽⁴⁾	$\begin{array}{l} XTS = 0, \\ XT1BYPASS = 0, XT1DRIVEx = 0, \\ f_{XT1,LF} = 32768 \ \text{Hz}, \ C_{L,eff} = 6 \ \text{pF} \end{array}$			210		1-0
		$\begin{array}{l} XTS = 0, \\ XT1BYPASS = 0, XT1DRIVEx = 1, \\ f_{XT1,LF} = 32768 \mbox{ Hz}, C_{L,eff} = 12 pF \end{array}$			300		K12
		$XTS = 0, XCAPx = 0^{(6)}$			2		
C	Integrated effective load	XTS = 0, XCAPx = 1			5.5		ъĘ
CL,eff	capacitance, LF mode ⁽⁵⁾	XTS = 0, XCAPx = 2			8.5		рг
OA _{LF}		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768 Hz$		30%		70%	
f _{Fault,LF}	Oscillator fault frequency, LF mode ⁽⁷⁾	XTS = 0 ⁽⁸⁾		10		10000	Hz
t _{START,LF}	Start up time. LE mode		- 21/	1000		me	
	Start-up time, LF mode		5 v		500		1115

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.

Keep the trace between the device and the crystal as short as possible.

Design a good ground plane around the oscillator pins.

Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.

Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.

- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:

 - For XT1DRIVEx = 0, $C_{L,eff} \le 6 \text{ pF}$ For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le 9 \text{ pF}$ For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le 10 \text{ pF}$ For XT1DRIVEx = 3, $C_{L,eff} \ge 6 \text{ pF}$
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. (7)Frequencies in between might set the flag.
- Measured with logic-level input frequency but also applies to operation with crystals. (8)

5.14 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1)

Calculated using the box method: $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C)) Calculated using the box method: <math>(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$ (2)

5.15 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
I _{REFO}	REFO oscillator current consumption	$T_A = 25^{\circ}C$	1.8 V to 3.6 V		3		μA
f _{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		$T_A = 25^{\circ}C$	3 V			±1.5%	
df_{REFO}/d_{T}	REFO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t _{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		μs

Calculated using the box method: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C - (-40°C)) (1)

Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V) (2)

5.16 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{DCO(0,0)}	DCO frequency (0, 0) ⁽¹⁾	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
f _{DCO(0,31)}	DCO frequency (0, 31) ⁽¹⁾	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
f _{DCO(1,0)}	DCO frequency (1, 0) ⁽¹⁾	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
f _{DCO(1,31)}	DCO frequency (1, 31) ⁽¹⁾	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
f _{DCO(2,0)}	DCO frequency (2, 0) ⁽¹⁾	DCORSELx = 2, $DCOx = 0$, $MODx = 0$	0.32		0.75	MHz
f _{DCO(2,31)}	DCO frequency (2, 31) ⁽¹⁾	DCORSELx = 2, $DCOx = 31$, $MODx = 0$	3.17		7.38	MHz
f _{DCO(3,0)}	DCO frequency (3, 0) ⁽¹⁾	DCORSELx = 3, $DCOx = 0$, $MODx = 0$	0.64		1.51	MHz
f _{DCO(3,31)}	DCO frequency (3, 31) ⁽¹⁾	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
f _{DCO(4,0)}	DCO frequency (4, 0) ⁽¹⁾	DCORSELx = 4, $DCOx = 0$, $MODx = 0$	1.3		3.2	MHz
f _{DCO(4,31)}	DCO frequency (4, 31) ⁽¹⁾	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
f _{DCO(5,0)}	DCO frequency (5, 0) ⁽¹⁾	DCORSELx = 5, $DCOx = 0$, $MODx = 0$	2.5		6.0	MHz
f _{DCO(5,31)}	DCO frequency (5, 31) ⁽¹⁾	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
f _{DCO(6,0)}	DCO frequency (6, 0) ⁽¹⁾	DCORSELx = 6, $DCOx = 0$, $MODx = 0$	4.6		10.7	MHz
f _{DCO(6,31)}	DCO frequency (6, 31) ⁽¹⁾	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
f _{DCO(7,0)}	DCO frequency (7, 0) ⁽¹⁾	DCORSELx = 7, $DCOx = 0$, $MODx = 0$	8.5		19.6	MHz
f _{DCO(7,31)}	DCO frequency (7, 31) ⁽¹⁾	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
S _{DCORSEL}	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S _{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL, DCO+1)}/f_{DCO(DCORSEL, DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df _{DCO} /dT	DCO frequency temperature drift	f _{DCO} = 1 MHz		0.1		%/°C
df _{DCO} /dV _{CC}	DCO frequency voltage drift	f _{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n, 31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.



Figure 5-13. Typical DCO frequency

5.17 PMM, Brown-Out Reset (BOR)

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	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _(DVCC_BOR_IT-)	BOR_{H} on voltage, DV_{CC} falling level	$ dDV_{CC}/d_t < 3 V/s$			1.45	V
V _(DVCC_BOR_IT+)	BOR_{H} off voltage, DV_{CC} rising level	$ dDV_{CC}/d_t < 3 V/s$	0.80	1.30	1.50	V
V _(DVCC_BOR_hys)	BOR _H hysteresis		60		250	mV
t _{RESET}	Pulse duration required at RST/NMI pin to accept a reset		2			μs

5.18 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
V _{CORE3} (AM)	Core voltage, active mode, PMMCOREV = 3	$2.4 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.90	V
V _{CORE2} (AM)	Core voltage, active mode, PMMCOREV = 2	$2.2 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.80	V
V _{CORE1} (AM)	Core voltage, active mode, PMMCOREV = 1	$2 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.60	V
V _{CORE0} (AM)	Core voltage, active mode, PMMCOREV = 0	$1.8 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.40	V
V _{CORE3} (LPM)	Core voltage, low-current mode, PMMCOREV = 3	$2.4 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.94	V
V _{CORE2} (LPM)	Core voltage, low-current mode, PMMCOREV = 2	$2.2 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.84	V
V _{CORE1} (LPM)	Core voltage, low-current mode, PMMCOREV = 1	$2 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.64	V
V _{CORE0} (LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV _{CC} ≤ 3.6 V	1.44	V



5.19 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVSHE = 0, DV _{CC} = 3.6 V		0		~^
I _(SVSH)	SVS current consumption	SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		ΠA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		μA
		SVSHE = 1, SVSHRVL = 0	1.53	1.60	1.67	
V _(SVSH_IT-)	SVS on voltage level ⁽¹⁾	SVSHE = 1, SVSHRVL = 1	1.73	1.80	1.87	V
	SVS _H on voltage level	SVSHE = 1, SVSHRVL = 2	1.93	2.00	2.07	v
		SVSHE = 1, SVSHRVL = 3	2.03	2.10	2.17	
		SVSHE = 1, SVSMHRRL = 0	1.60	1.70	1.80	
	SVS _H off voltage level ⁽¹⁾	SVSHE = 1, SVSMHRRL = 1	1.80	1.90	2.00	V
		SVSHE = 1, SVSMHRRL = 2	2.00	2.10	2.20	
		SVSHE = 1, SVSMHRRL = 3	2.10	2.20	2.30	
V(SVSH_IT+)		SVSHE = 1, SVSMHRRL = 4	2.25	2.35	2.50	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.65	2.78	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
	SVS _H propagation delay	SVSHE = 1, dV _{DVCC} /dt = 10 mV/µs, SVSHFP = 1		2.5		
t _{pd} (SVSH)		SVSHE = 1, $dV_{DVCC}/dt = 1 \text{ mV}/\mu s$, SVSHFP = 0		20		μs
t _(SVSH)	SVS _H on or off delay time	SVSHE = 0 \rightarrow 1, dV _{DVCC} /dt = 10 mV/µs, SVSHFP = 1		12.5		
		SVSHE = 0 \rightarrow 1, dV _{DVCC} /dt = 1 mV/µs, SVSHFP = 0		100		μs
dV _{DVCC} /dt	DV _{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage* Supervisor chapter in the *RF430F5978 User's Guide* (SLAU378) on recommended settings and usage.

5.20 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVMHE = 0, DV _{CC} = 3.6 V		0		۳Å
I _(SVMH)	SVM _H current consumption	SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		ΠA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		μA
		SVMHE = 1, SVSMHRRL = 0	1.60	1.70	1.80	
V _(SVMH)		SVMHE = 1, SVSMHRRL = 1	1.80	1.90	2.00	
		SVMHE = 1, SVSMHRRL = 2	2.00	2.10	2.20	
	SVM _H on or off voltage level ⁽¹⁾	SVMHE = 1, SVSMHRRL = 3	2.10	2.20	2.30	
		SVMHE = 1, SVSMHRRL = 4	2.25	2.35	2.50	V
		SVMHE = 1, SVSMHRRL = 5	2.52	2.65	2.78	-
		SVMHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
		SVMHE = 1, SVMHOVPE = 1		3.75		
		SVMHE = 1, dV _{DVCC} /dt = 10 mV/µs, SVMHFP = 1		2.5		
t _{pd} (SVMH)	SVM _H propagation delay	SVMHE = 1, $dV_{DVCC}/dt = 1 \text{ mV/}\mu\text{s}$, SVMHFP = 0		20		μs
t _(SVMH)	SVM _H on or off delay time	SVMHE = 0 \rightarrow 1, dV _{DVCC} /dt = 10 mV/µs, SVMHFP = 1		12.5		
		SVMHE = 0 \rightarrow 1, dV _{DVCC} /dt = 1 mV/µs, SVMHFP = 0		100		μs

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *RF430F5978 User's Guide* (SLAU378) on recommended settings and usage.

5.21 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVSLE = 0, PMMCOREV = 2		0		~ ^
I _(SVSL)	SVS_L current consumption	SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		ΠA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		μA
t _{pd(SVSL)}	SVS_L propagation delay	SVSLE = 1, dV _{CORE} /dt = 10 mV/µs, SVSLFP = 1	2.5			
		SVSLE = 1, $dV_{CORE}/dt = 1 \text{ mV/}\mu\text{s}$, SVSLFP = 0		20		μs
t(SVSL)	SVS_L on or off delay time	SVSLE = 0 \rightarrow 1, dV _{CORE} /dt = 10 mV/µs, SVSLFP = 1	12.			
				100		μs

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5.22 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVMLE = 0, PMMCOREV = 2		0		۳Å
I _(SVML)	SVM_L current consumption	SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		ΠA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		μA
t _{pd(SVML)}	SVM_L propagation delay	SVMLE = 1, dV _{CORE} /dt = 10 mV/µs, SVMLFP = 1	2.5			
		SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu s$, SVMLFP = 0		20		μs
t _(SVML)	SVM_L on or off delay time	SVMLE = 0 \rightarrow 1, dV _{CORE} /dt = 10 mV/µs, SVMLFP = 1	12.5			
		SVMLE = 0 \rightarrow 1, dV _{CORE} /dt = 1 mV/µs, SVMLFP = 0		100		μs

5.23 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Wake-up time from LPM2,	PMMCOREV = SVSMLRRL = n	$f_{MCLK} \ge 4.0 \text{ MHz}$			5	
twake-up-fast	LPM3, or LPM4 to active mode ⁽¹⁾	(where n = 0, 1, 2, or 3), SVSLFP = 1	f _{MCLK} < 4.0 MHz	z		6	μs
t _{WAKE-UP-SLOW}	Wake-up time from LPM2, LPM3 or LPM4 to active mode ⁽²⁾	$\begin{array}{l} PMMCOREV = SVSMLRRL = n \\ (\text{where } n = 0, \ 1, \ 2, \ \text{or} \ 3), \\ SVSLFP = 0 \end{array}$			150	165	μs
t _{WAKE-UP-RESET}	Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽³⁾				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). Fastest wake-up times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *RF430F5978 User's Guide* (SLAU378).

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *RF430F5978 User's Guide* (SLAU378).

(3) This value represents the time from the wake-up event to the reset vector execution.

5.24 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN MAX	UNIT
f _{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10%	1.8 V, 3 V	25	MHz
t _{TA,cap}	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20	ns

5.25 USCI (UART Mode) Clock Frequency

	PARAMETER	CONDITIONS	MIN	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%		f _{SYSTEM}	MHz
f _{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

5.26 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	V _{cc}	MIN	TYP MAX	UNIT
	t _T UART receive deglitch time ⁽¹⁾		50	600	2
τ _τ			50	600	ns

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.27 USCI (SPI Master Mode) Clock Frequency

	PARAMETER	CONDITIONS	MIN	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ±10%		f _{SYSTEM}	MHz

5.28 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 5-14 and Figure 5-15)

II input data setup time		0	1.8 V 3 V	55 38		
II input data setup time		0	3 V	38		
ii input data setup time						
3 –	2	2.4 V	30		ns	
		3	3 V	25		
		0	1.8 V	0		
Il face of all the ballel floors		0	3 V	0		
			2.4 V	0		ns
		3	3 V	0		
		0	1.8 V		20	- ns
	UCLK edge to SIMO valid, $C_L = 20 \text{ pF}$		3 V		18	
D output data valid time			2.4 V		16	
		3	3 V		15	
		0	1.8 V	-10		
Southeast data hadd there (3)	0 00 - 5	0	3 V	-8		ns
D output data hold time (*)	$C_L = 20 \text{ pF}$		2.4 V	-10		
		3	3 V	-8		
	I input data hold time) output data valid time ⁽²⁾) output data hold time ⁽³⁾ 2t _{LO/HI} with t _{LO/HI} ≥ max(t _{VALID.MO}	I input data hold time) output data valid time ⁽²⁾ UCLK edge to SIMO valid, $C_L = 20 \text{ pF}$) output data hold time ⁽³⁾ $C_L = 20 \text{ pF}$ 2t _{LO/HI} with t _{LO/HI} ≥ max(t _{VALID MO(USCI}) + t _{SU,SI(Slave)} , t _{SU,MI(USCI}) +	I input data hold time 0 3 3 0 output data valid time ⁽²⁾ UCLK edge to SIMO valid, C _L = 20 pF 0 0 output data valid time ⁽³⁾ C _L = 20 pF 3 0 output data hold time ⁽³⁾ C _L = 20 pF 3 2t O/H with t ₁ O/H ≥ max(t _{VALID} MO(USC) + t _{SU} SI(Slave), t _{SU} MI(USC) + t _{VALID} SO(Slave)).	Linput data hold time $ \begin{array}{c} 0 & \frac{1.8 \vee}{3 \vee} \\ 2.4 \vee}{3 \vee} \\ 3 \vee \\ 3 \vee \\ 0 & \frac{1.8 \vee}{3 \vee} \\ 0 & 1.$	I input data hold time $ \begin{array}{c c} 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 3 \lor & 0 \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & 0}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & -10}{3 \lor & 0} \\ \hline 0 & \frac{1.8 \lor & -10}{3 \lor & -8} \\ \hline 0 & \frac{1.8 \lor & -10}{3 \lor & -8} \\ \hline 2.4 \lor & -10 \\ \hline 3 \lor & -8 \\ \hline 2.4 \lor & -$	I input data hold time0 $1.8 \lor 0$ 3 $3 \lor 0$ 3 $2.4 \lor 0$ 3 $3 \lor 0$ 3 ∪ 0 0 $1.8 \lor 20$ 3 ∨ 0 $C_L = 20 \text{ pF}$ 0 $1.8 \lor -10$ $3 \lor -8$ $2.4 \lor -10$ $3 \lor -8$

For the slave parameters $t_{SU,SI(Slave)}$ and $t_{ALID,SO(Slave)}$, see the SPI parameters of the attached slave. Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams (2) in Figure 5-14 and Figure 5-15.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-14 and Figure 5-15.

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EXAS

STRUMENTS





Figure 5-15. SPI Master Mode, CKPH = 1

5.29 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

(see Figure 5-16 and Figure 5-17)

	PARAMETER	TEST CONDITIONS	PMMCOREVx	Vcc	MIN	MAX	UNIT
				1.8 V	11		
			0	3 V	8		
t _{STE,LEAD}	STE lead time, STE low to clock		_	2.4 V	7		ns
			3	3 V	6		
				1.8 V	3		
	STE lag time. Last clock to STE		0	3 V	3		
t _{STE,LAG}	high			2.4 V	3		ns
			3	3 V	3		
			0	1.8 V		66	
	STE access time, STE low to SOMI		0	3 V		50	
^t STE,ACC	data out			2.4 V		36	ns
			3	3 V		30	
			0	1.8 V		30	ns
	STE disable time, STE high to		0	3 V		23	
^I STE,DIS	SOMI high impedance			2.4 V		16	
			3	3 V		13	
				1.8 V	5		ns
			0	3 V	5		
t _{SU,SI}	SIMO input data setup time			2.4 V	2		
			3	3 V	2		
				1.8 V	5		
			0	3 V	5		
t _{HD,SI}	SIMO input data hold time			2.4 V	5		ns
			3	3 V	5		
				1.8 V		76	
	(2)	UCLK edge to SOMI valid.	0	3 V		60	
t _{VALID,SO}	SOMI output data valid time ⁽²⁾	$C_L = 20 \text{ pF}$		2.4 V		44	ns
			3	3 V		40	
				1.8 V	18		ns
	$\mathbf{OOM} = (1, $	0 00	U	3 V	12		
^t HD,SO	SOMI output data hold time ⁽³⁾	C _L = 20 pF	3	2.4 V	10		
				3 V	8		

(1)

 $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \ge max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$. For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master. Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams (2) in Figure 5-16 and Figure 5-17.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-16 and Figure 5-17.







5.30 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-18)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%			f _{SYSTEM}	MHz
f _{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
	Light time (repeated) START	f _{SCL} ≤ 100 kHz	221/21/	4.0		
'HD,STA	Hold lime (repeated) START	f _{SCL} > 100 kHz	2.2 V, 3 V	0.6		μs
	Setup time for a repeated START	f _{SCL} ≤ 100 kHz	221/21/	4.7		
^I SU,STA		f _{SCL} > 100 kHz	2.2 V, 3 V	0.6		μs
t _{HD,DAT}	Data hold time		2.2 V, 3 V	0		ns
t _{SU,DAT}	Data setup time		2.2 V, 3 V	250		ns
	Catura times for CTOD	f _{SCL} ≤ 100 kHz	0.0.1/ 0.1/	4.0		
^I SU,STO	Setup time for STOP	f _{SCL} > 100 kHz	2.2 V, 3 V	0.6		μs
	Dulas duration of anilyse suppressed by input filter		2.2 V	50	600	ns
t _{SP}	Pulse duration of spikes suppressed by input filter		3 V	50	600	



Figure 5-18. I²C Mode Timing

5.31 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT
AV _{CC}	Analog supply voltage, Full performance	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0 V$		2.2		3.6	V
V _(Ax)	Analog input voltage range ⁽²⁾	All ADC12 analog input pins Ax		0		AV_{CC}	V
	Operating supply current into	$f_{ADC12CLK} = 5.0 \text{ MHz}, \text{ ADC12ON} = 1,$	2.2 V		125	155	
I _{ADC12_A} AVCC	AVCC terminal ⁽³⁾	REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	3 V		150	220	μΑ
CI	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
RI	Input MUX ON resistance	$0 V \le V_{Ax} \le AV_{CC}$		10	200	1900	Ω

The leakage current is specified by the digital I/O input leakage. (1)

(2)The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 5.35 and Section 5.36.

The internal reference supply current is not included in current consumption parameter IADC12 A. (3)

5.32 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
f _{ADC12CLK}		For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	4.8	5.4	MHz
f _{ADC12OSC}	Internal ADC12 oscillator ⁽¹⁾	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
^t CONVERT	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12OSC} = 4.2 \text{ MHz}$ to 5.4 MHz	2.2 V, 3 V	2.4		3.1	hs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL $\neq 0$			(2)		
t _{Sample}	Sampling time		2.2 V, 3 V	1000			ns

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.

13 × ADC12DIV × 1/f_{ADC12CLK} (2)

(3)

Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB: t_{Sample} = ln(2ⁿ⁺¹) x (R_S + R_I) x C_I + 800 ns, where n = ADC resolution = 12, R_S = external source resistance

5.33 12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
E	Integral	$1.4 \text{ V} \leq (\text{V}_{eREF+} - \text{V}_{REF-}/\text{V}_{eREF-}) \text{min} \leq 1.6 \text{ V}$	221/21/			±2	
Ξļ	linearity error (INL)	1.6 V < (V _{eREF+} – V _{REF} /V _{eREF})min \leq V _{AVCC}	2.2 V, 3 V			±1.7	LOD
ED	Differential linearity error (DNL)	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 20 \text{ pF}$	2.2 V, 3 V			±1.0	LSB
Eo	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-}),$ Internal impedance of source R _S < 100 Ω , C _{VREF+} = 20 pF	2.2 V, 3 V		±1.0	±2.0	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF_}/V_{eREF_})$ min $\leq (V_{eREF+} - V_{REF_}/V_{eREF_}), C_{VREF+} = 20 \text{ pF}$	2.2 V, 3 V		±1.0	±2.0	LSB
E _T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 20 \text{ pF}$	2.2 V, 3 V		±1.4	±3.5	LSB

5.34 12-Bit ADC, Temperature Sensor and Built-In V_{MID} ⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
V	$S_{222} \begin{pmatrix} 2 \\ 3 \end{pmatrix}$	ADC12ON = 1, INCH = 0Ah,	2.2 V		680		
VSENSOR	See	$T_A = 0^{\circ}C$	3 V		680		mv
то	See ⁽³⁾	ADC12ON = 1 INCH = 0.0h	2.2 V		2.25		m\//°C
I C _{SENSOR}	See	ADC12ON = 1, INCH = 0AI	3 V		2.25		mv/°C
t _{SENSOR(sample)}	Sample time required if channel 10 is selected ⁽⁴⁾	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤1 LSB	2.2 V	100			
			3 V	100			μs
	AV_{CC} divider at channel 11, V_{AVCC} factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V _{AVCC}
V _{MID}	A)/ divider et chennel 11		2.2 V	1.06	1.1	1.14	V
	AV _{CC} divider at channel 11	ADC12ON = 1, INCH = 0BIT	3 V	1.44	1.5	1.56	v
t _{VMID(sample)}	Sample time required if channel 11 is selected ⁽⁵⁾	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤1 LSB	2.2 V, 3 V	1000			ns

 The temperature sensor is provided by the REF module. See the REF module parametric, I_{REF+}, regarding the current consumption of the temperature sensor.

(2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.

(3) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as V_{SENSE} = TC_{SENSOR} * (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.

(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.

(5) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.



Figure 5-19. Typical Temperature Sensor Voltage

5.35 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
V _{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ ⁽²⁾		1.4		AV _{CC}	V
V _{REF-} /V _{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ ⁽³⁾		0		1.2	V
(V _{eREF+} – V _{REF-} /V _{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ ⁽⁴⁾		1.4		AV _{CC}	V
Iveref+ Ivref-/veref-	Static input current	$\begin{array}{l} 1.4 \ V \leq V_{eREF+} \leq V_{AVCC}, \\ V_{eREF-} = 0 \ V, \\ f_{ADC12CLK} = 5 \ MHz, \\ ADC12SHTx = 1h, \\ Conversion \ rate \ 200 ksps \end{array}$	2.2 V, 3 V		±8.5	±26	
		$\begin{array}{l} 1.4 \ V \leq V_{eREF+} \leq V_{AVCC}, \\ V_{eREF-} = 0 \ V \\ f_{ADC12CLK} = 5 \ MHz, \\ ADC12SHTx = 8h, \\ Conversion \ rate \ 20 \ ksps \end{array}$	2.2 V, 3 V			±1	μΑ
$C_{VREF\pm}$	Capacitance at VREF+ or VREF- terminal, external reference ⁽⁵⁾			10			μF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

(5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *RF430F5978 User's Guide* (SLAU378).

5.36 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
		$\begin{array}{l} REFVSEL = 2 \text{ for } 2.5 \text{ V}, \\ REFON = REFOUT = 1, \\ I_{VREF+} = 0 \text{ A} \end{array}$	3 V		2.41	±1.5%	
V _{REF+}	Positive built-in reference voltage output	$\begin{array}{l} REFVSEL = 1 \text{ for } 2 \text{ V}, \\ REFON = REFOUT = 1, \\ I_{VREF+} = 0 \text{ A} \end{array}$	3 V		1.93	±1.5%	V
		$\begin{aligned} &REFVSEL = 0 \text{ for } 1.5 \text{ V}, \\ &REFON = REFOUT = 1, \\ &I_{VREF+} = 0 \text{ A} \end{aligned}$	2.2 V, 3 V		1.45	±1.5%	
		REFVSEL = 0 for 1.5 V, reduced performance		1.8			
A)/	AVCC minimum voltage,	REFVSEL = 0 for 1.5 V		2.2			V
AVCC(min)	active	REFVSEL = 1 for 2 V		2.3			v
		REFVSEL = 2 for 2.5 V		2.8			
, Ope	Operating supply current into	REFON = 1, REFOUT = 0, REFBURST = 0	3 V		100	140	μA
IREF+	AVCC terminal ^{(2) (3)}	REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.9	1.5	mA
I _{L(VREF+)}	Load-current regulation, VREF+ terminal ⁽⁴⁾	$\label{eq:REFVSEL} \begin{array}{l} REFVSEL = (0,1,\text{or}2), \\ I_{VREF+} = +10\;\mu\text{A}/\!-\!1000\;\mu\text{A}, \\ AV_{CC} = AV_{CC}\;(\text{min}) \text{ for each reference level}, \\ REFVSEL = (0,1,\text{or}2), \\ REFON = REFOUT = 1 \end{array}$				2500	µV/mA
$C_{VREF\pm}$	Capacitance at VREF+ and VREF- terminals, internal reference	REFON = REFOUT = 1		20		100	pF
TC _{REF+}	Temperature coefficient of built-in reference ⁽⁵⁾	I _{VREF+} = 0 A, REFVSEL = (0, 1, or 2), REFON = 1, REFOUT = 0 or 1			30	50	ppm/ °C
PSRR_DC	Power supply rejection ratio (DC)				120	300	μV/V
PSRR_AC	Power supply rejection ratio (AC)				6.4		mV/V
	Settling time of reference voltage ⁽⁶⁾				75		
t _{SETTLE}					75		μs

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the V_{REF+} terminal. When REFOUT = 1, the reference is available at the V_{REF+} terminal, as well as, used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.

(2) The internal reference current is supplied through the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.

(3) The temperature sensor is provided by the REF module. Its current is supplied through the AVCC terminal and is equivalent to I_{REF+} with REFON = 1 and REFOUT = 0.

(4) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace, etc.

(5) Calculated using the box method: (MAX(-40° C to 85°C) – MIN(-40° C to 85°C)) / MIN(-40° C to 85°C)/(85°C – (-40° C)).

(6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.


5.37 Comparator B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage			1.8		3.6	V
			1.8 V			40	
	Comparator operating supply	CBPWRMD = 00	2.2 V		30	50	
I _{AVCC_COMP}	current into AVCC, Excludes		3 V		40	65	μA
	reference resistor ladder	CBPWRMD = 01	2.2 V, 3 V		10	30	
		CBPWRMD = 10	2.2 V, 3 V		0.1	0.5	
I _{AVCC_REF}	Quiescent current of local reference voltage amplifier into AVCC	CBREFACC = 1, CBREFLx = 01				22	μA
V _{IC}	Common mode input range			0		V _{CC} -1	V
M	Innut offect velteres	CBPWRMD = 00				±20	m)/
VOFFSET	Input onset voltage	CBPWRMD = 01, 10				±10	mv
C _{IN}	Input capacitance				5		pF
Р	Sorioo input registance	ON - switch closed			3	4	kΩ
R _{SIN}	Series input resistance	OFF - switch opened		30			MΩ
		CBPWRMD = 00, CBF = 0				450	20
t _{PD}	Propagation delay, response time	CBPWRMD = 01, CBF = 0				600	115
		CBPWRMD = 10, CBF = 0				50	μs
		$\begin{array}{l} CBPWRMD = 00, CBON = 1, \\ CBF = 1, CBFDLY = 00 \end{array}$		0.35	0.6	1.0	
	Propagation delay with filter	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
^t PD,filter	active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t _{EN_CMP}	Comparator enable time, settling time	CBON = 0 to CBON = 1, CBPWRMD = 00, 01, 10			1	2	μs
t _{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			0.3	1.5	μs
V _{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN ×	(n + 1)	/ 32	V

5.38 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TJ	MIN	TYP	MAX	UNIT
DV _{CC(PGM/ERASE)}	Program and erase supply voltage		1.8		3.6	V
I _{PGM}	Average supply current from DVCC during program			3	5	mA
I _{ERASE}	Average supply current from DVCC during erase			2	6.5	mA
I _{MERASE} , I _{BANK}	Average supply current from DVCC during mass erase or bank erase			2	6.5	mA
t _{CPT}	Cumulative program time ⁽¹⁾				16	ms
	Program and erase endurance		10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	25°C	100			years
t _{Word}	Word or byte program time ⁽²⁾		64		85	μs
t _{Block, 0}	Block program time for first byte or word ⁽²⁾		49		65	μs
t _{Block, 1-(N-1)}	Block program time for each additional byte or word, except for last byte or $\operatorname{word}^{(2)}$		37		49	μs
t _{Block, N}	Block program time for last byte or word ⁽²⁾		55		73	μs
t _{Erase}	Erase time for segment erase, mass erase, and bank erase when available $^{\left(2\right) }$		23		32	ms
f _{MCLK,MRG}	MCLK frequency in marginal read mode (FCTL4.MRG0 = 1 or FCTL4. MRG1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

5.39 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	V _{cc}	MIN	TYP	MAX	UNIT
f _{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	μs
t _{SBW, En}	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾	2.2 V, 3 V			1	μs
t _{SBW,Rst}	Spy-Bi-Wire return to normal operation time		15		100	μs
1	TOK is not for success to A using $ TAO(2) $	2.2 V	0		5	MHz
ITCK	TCK input frequency to 4-wire STAG	3 V	0		10	MHz
R _{internal}	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.40 RF1A CC1101 Radio Parameters

RUMENTS

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		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage range during radio operation	2.0		3.6	V
PMMCOREVx	Core voltage range, PMMCOREVx setting during radio operation	2		3	
		300		348	
RF frequency range		389 ⁽¹⁾		464	MHz
		779		928	
	2-FSK	0.6		500	
Data rate	2-GFSK, OOK, and ASK	0.6		250	kBaud
	(Shaped) MSK (also known as differential offset QPSK) ⁽²⁾	26		500	
RF crystal frequency		26	26	27	MHz
RF crystal tolerance	Total tolerance including initial tolerance, crystal loading, aging and temperature dependency. ⁽³⁾		±40		ppm
RF crystal load capacitance		10	13	20	pF
RF crystal effective series resistance				100	Ω

Table 5-1. Recommended Operating Conditions

(1) If using a 27-MHz crystal, the lower frequency limit for this band is 392 MHz.

(2) If using optional Manchester encoding, the data rate in kbps is half the baud rate.

(3) The acceptable crystal tolerance depends on frequency band, channel bandwidth, and spacing. Also see design note DN005 -- CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (SWRA122).

5.41 RF Crystal Oscillator, XT2

 $T_A = 25^{\circ}C, V_{CC} = 3 V \text{ (unless otherwise noted)}^{(1)}$

PARAMETER	MIN	TYP	MAX	UNIT
Start-up time ⁽²⁾		150	810	μs
Duty cycle	45%	50%	55%	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) The start-up time depends to a very large degree on the crystal that is used.

5.42 Current Consumption, Reduced-Power Modes

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current	RF crystal oscillator only ⁽²⁾		100		μA
consumption	IDLE state (including RF crystal oscillator)		1.7		mA
	FSTXON state (only the frequency synthesizer is running) ⁽³⁾		9.5		mA

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) To measure the current, follow this sequence:

• Enable XT2 with XOSC_FORCE_ON = 1.

• Set radio to sleep mode.

• Disable XT2 clock requests from any module.

(3) This current consumption is also representative of other intermediate states when going from IDLE to RX or TX, including the calibration state.

5.43 Current Consumption, Receive Mode

 T_{A} = 25°C, V_{CC} = 3 V (unless otherwise noted) $^{(1)\ (2)}$

PARAMETER	FREQ (MHz)	DATA RATE (kBaud)	TEST	CONDITIONS	MIN	ТҮР	МАХ	UNIT
		1.0		Input at –100 dBm (close to sensitivity limit)		17		
		1.2		Input at –40 dBm (well above sensitivity limit)		16		
	315	29.4	Register settings	Input at –100 dBm (close to sensitivity limit)		17		
		30.4	current	Input at -40 dBm (well above sensitivity limit)		16		
		250		Input at –100 dBm (close to sensitivity limit)		18		
		250		Input at –40 dBm (well above sensitivity limit)		16.5		
		1.0		Input at –100 dBm (close to sensitivity limit)				
	433 38.4	1.2		Input at -40 dBm (well above sensitivity limit)		17		
Current		20.4	Register settings	Input at –100 dBm (close to sensitivity limit)		18		~^
RX		433 <u>36.4</u> 0	current	Input at -40 dBm (well above sensitivity limit)		17		ΠA
		250		Input at –100 dBm (close to sensitivity limit)		18.5		
		250		Input at -40 dBm (well above sensitivity limit)		17		
		1.0		Input at –100 dBm (close to sensitivity limit)		16		
		1.2		Input at -40 dBm (well above sensitivity limit)		15		
	969 015	20.4	Register settings Input at –100 dBm (close sensitivity limit)			16		
	000, 915	30.4	current ⁽³⁾ Input at -40 dBm (well above sensitivity limit) 15					
	250			Input at –100 dBm (close to sensitivity limit)	16			
		200		Input at –40 dBm (well above sensitivity limit)		15		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.
 (3) For 868 or 915 MHz, see Figure 5-20 for current consumption with register settings optimized for sensitivity.



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Figure 5-20. Typical RX Current Consumption Over Temperature and Input Power Level, 868 MHz, Sensitivity-Optimized Setting

5.44 Current Consumption, Transmit Mode

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾ (2)

PARAMETER	FREQUENCY [MHz}	PATABLE SETTING	OUTPUT POWER (dBm)	ТҮР	UNIT
PARAMETER Current consumption, TX		0xC0	Maximum	26	
	215	0xC4	+10	25	
	315	0x51	0	15	
		0x29	-6	15	
		0xC0	Maximum	33	
	422	0xC6	+10	29	
	433	0x50	0	17	
Current concurrentian TV		0x2D	-6	17	A
		0xC0	Maximum	36	mA
	969	0xC3	+10	33	
	000	0x8D	0	18	
		-6	18		
		0xC0	Maximum	35	
	015	0xC3	+10	32	
	915	0x8D	0	18	
		0x2D	-6	18	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.

5.45 Typical TX Current Consumption, 315 MHz

	PATABLE	OUTPUT	Vcc	2 V	3 V	3.6 V		
PARAMETER	SETTING	POWER (dBm)	T _A	25°C	25°C	25°C	UNIT	
	0xC0	Maximum		27.5	26.4	28.1		
Current consumption,	0xC4	+10		25.1	25.2	25.3	~ ^	
TX	0x51	0		14.4	14.6	14.7	MA	
	0x29	-6		14.2	14.7	15.0		

5.46 Typical TX Current Consumption, 433 MHz

	PATABLE	OUTPUT	V _{cc}	2 V	3 V	3.6 V		
PARAMETER	SETTING	POWER (dBm)	T _A	25°C	25°C	25°C	UNIT	
	0xC0	Maximum		33.1	33.4	33.8		
Current consumption,	0xC6	+10		28.6	28.8	28.8		
тх	0x50	0		16.6	16.8	16.9	ma	
	0x2D	-6		16.8	17.5	17.8		

5.47 Typical TX Current Consumption, 868 MHz

PARAMETER	PATABLE SETTING	PATABLE	OUTPUT	Vcc		2 V			3 V			3.6 V		
		POWER (dBm)	TA	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT	
	0xC0	Maximum		36.7	35.2	34.2	38.5	35.5	34.9	37.1	35.7	34.7		
Current	0xC3	+10		34.0	32.8	32.0	34.2	33.0	32.5	34.3	33.1	32.2	~ ^	
consumption, TX	0x8D	0		18.0	17.6	17.5	18.3	17.8	18.1	18.4	18.0	17.7	mA	
	0x2D	-6		17.1	17.0	17.2	17.8	17.8	18.3	18.2	18.1	18.1		

5.48 Typical TX Current Consumption, 915 MHz

PARAMETER	PATABLE SETTING	PATABLE	OUTPUT	Vcc		2 V			3 V			3.6 V		
		POWER (dBm)	T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT	
	0xC0	Maximum		35.5	33.8	33.2	36.2	34.8	33.6	36.3	35.0	33.8		
Current	0xC3	+10		33.2	32.0	31.0	33.4	32.1	31.2	33.5	32.3	31.3	~ ^	
consumption, TX	0x8D	0		17.8	17.4	17.1	18.1	17.6	17.3	18.2	17.8	17.5	ШA	
	0x2D	-6		17.0	16.9	16.9	17.7	17.6	17.6	18.1	18.0	18.0		

5.49 RF Receive, Overall

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital channel filter bandwidth ⁽²⁾		58		812	kHz
Spurious emissions ⁽³⁾ ⁽⁴⁾	25 MHz to 1 GHz		-68	-57	dDm
	Above 1 GHz		-66	-47	автп
RX latency	Serial operation ⁽⁵⁾		9		bit

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0-MHz crystal).

(3) Typical radiated spurious emission is -49 dBm measured at the VCO frequency

(4) Maximum figure is the ETSI EN 300 220 limit

(5) Time from start of reception until data is available on the receiver data output pin is equal to 9 bit.

5.50 RF Receive, 315 MHz

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾

2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER	DATA RATE (kBaud)	TEST CONDITIONS	ТҮР	UNIT
	0.6	14.3-kHz deviation, 58-kHz digital channel filter bandwidth	-117	
Receiver sensitivity	1.2	5.2-kHz deviation, 58-kHz digital channel filter bandwidth ⁽²⁾	-111	
	38.4	20-kHz deviation, 100-kHz digital channel filter bandwidth ⁽³⁾	-103	dBm
	250	127-kHz deviation, 540-kHz digital channel filter bandwidth ⁽⁴⁾	-95	
	500	MSK, 812-kHz digital channel filter bandwidth ⁽⁴⁾	-86	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -109 dBm.

(3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -102 dBm.

(4) MDMCFG2.DEM_DCFILT_OFF = 1 can not be used for data rates \geq 250 kBaud.

5.51 RF Receive, 433 MHz

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾

2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER	DATA RATE (kBaud)	TEST CONDITIONS	MIN TYP M	ЛАХ	UNIT
	0.6	14.3-kHz deviation, 58-kHz digital channel filter bandwidth	-114		
Receiver sensitivity	1.2	5.2-kHz deviation, 58-kHz digital channel filter bandwidth ⁽²⁾	-111		
	38.4	20-kHz deviation, 100-kHz digital channel filter bandwidth ⁽³⁾	-104		dBm
	250	127-kHz deviation, 540-kHz digital channel filter bandwidth $^{(4)}$	-93		ubiii
	500	MSK, 812-kHz digital channel filter bandwidth ⁽⁴⁾	-85		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -109 dBm.

(3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -101 dBm.

(4) MDMCFG2.DEM_DCFILT_OFF = 1 can not be used for data rates ≥ 250 kBaud.

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5.52 RF Receive, 868 or 915 MHz

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾,

1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT			
0.6-kBaud data rate, 2-F	SK, 14.3-kHz deviation, 58-kHz digital channel filte	er bandwidth (unless other	wise note	ed)				
Receiver sensitivity				-115		dBm		
1.2-kBaud data rate, 2-F	SK, 5.2-kHz deviation, 58-kHz digital channel filter	bandwidth (unless otherw	ise noted	d)				
				-109				
Receiver sensitivity ⁽²⁾	2-GFSK modulation by setting MDMCFG2.MOD_FC Gaussian filter with BT = 0.5	DRMAT = 2,		-109		dBm		
Saturation	$FIFOTHR.CLOSE_IN_RX = 0^{(3)}$			-28		dBm		
Adjacent channel	Desired channel 3 dB above the sensitivity limit,	–100-kHz offset		39		dB		
rejection	100-kHz channel spacing ⁽⁴⁾	+100-kHz offset		39		uБ		
Image channel rejection	IF frequency 152 kHz, desired channel 3 dB above t	the sensitivity limit		29		dB		
Placking	Desired shapped 2 dB shows the constitutivity limit $^{(5)}$	±2-MHz offset		-48		dDm		
DIOCKING		±10-MHz offset		-40		UDIII		
38.4-kBaud data rate, 2-	FSK, 20-kHz deviation, 100-kHz digital channel filt	er bandwidth (unless othe	rwise not	ed)				
Receiver sensitivity ⁽⁶⁾								
	2-GFSK modulation by setting MDMCFG2.MOD_FC Gaussian filter with BT = 0.5	K modulation by setting MDMCFG2.MOD_FORMAT = 2, an filter with $BT = 0.5$						
Saturation	$FIFOTHR.CLOSE_IN_RX = 0^{(3)}$	THR.CLOSE_IN_RX = $0^{(3)}$						
Adjacent channel	Desired channel 3 dB above the sensitivity limit,	–200-kHz offset		20		dD		
rejection	200 kHz channel spacing ⁽⁵⁾	+200-kHz offset		25		aв		
Image channel rejection	IF frequency 152 kHz, Desired channel 3 dB above	the sensitivity limit		23		dB		
Blocking	Desired channel 3 dB above the sensitivity limit ⁽⁵⁾	±2-MHz offset		-48		alDura		
		±10-MHz offset		-40		aBm		
250-kBaud data rate, 2-l	FSK, 127-kHz deviation, 540-kHz digital channel file	ter bandwidth (unless othe	erwise no	ted)				
Receiver sensitivity (7)				-90				
	2-GFSK modulation by setting MDMCFG2.MOD_FC Gaussian filter with BT = 0.5	DRMAT = 2,		-90		dBm		
Saturation	$FIFOTHR.CLOSE_IN_RX = 0^{(3)}$			-19		dBm		
Adjacent channel	Desired channel 3 dB above the sensitivity limit,	–750-kHz offset		24				
rejection	750-kHz channel spacing ⁽⁶⁾	+750-kHz offset		30		uБ		
Image channel rejection	IF frequency 304 kHz, Desired channel 3 dB above	the sensitivity limit		18		dB		
Blocking	Desired channel 3 dB above the sensitivity limit ⁽⁸⁾	±2-MHz offset		-53		dDm		
		±10-MHz offset		-39		UDIII		
500-kBaud data rate, MS	SK, 812-kHz digital channel filter bandwidth (unles	s otherwise noted)						
Receiver sensitivity ⁽⁷⁾				-84		dBm		
Image channel rejection	IF frequency 355 kHz, Desired channel 3 dB above	the sensitivity limit		-2		dB		
Blocking	Desired channel 3 dB above the sensitivity $\overline{\rm limit^{(9)}}$	±2-MHz offset	-53			dBm		
		±10-MHz offset		-38		ubiii		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -107 dBm.

(3) See design note DN010 Close-in Reception with CC1101 (SWRA147).

(4) See Figure 5-21 for blocking performance at other offset frequencies.

(5) See Figure 5-22 for blocking performance at other offset frequencies.

(6) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF = 1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -100 dBm.

(7) MDMCFG2.DEM_DCFILT_OFF = 1 cannot be used for data rates ≥ 250 kBaud.

(8) See Figure 5-23 for blocking performance at other offset frequencies.

(9) See Figure 5-24 for blocking performance at other offset frequencies.



NOTE: 868.3 MHz, 2-FSK, 5.2-kHz deviation, IF frequency is 152.3 kHz, digital channel filter bandwidth is 58 kHz





Figure 5-22. Typical Selectivity at 38.4-kBaud Data Rate

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Figure 5-24. Typical Selectivity at 500-kBaud Data Rate

5.53 Typical Sensitivity, 315 MHz, Sensitivity-Optimized Setting

PARAMETER	DATA RATE (kBaud)	v_{cc}		2 V			3 V			3.6 V		
		TA	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
Sensitivity,	1.2		-112	-112	-110	-112	-111	-109	-112	-111	-108	
	38.4		-105	-105	-104	-105	-103	-102	-105	-104	-102	dBm
01010112	250		-95	-95	-92	-94	-95	-92	-95	-94	-91	

5.54 Typical Sensitivity, 433 MHz, Sensitivity-Optimized Setting

DADAMETED	DATA RATE (kBaud)	V _{cc}		2 V			3 V			3.6 V		LINUT
PARAMETER		T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
Sensitivity, 433MHz	1.2		-111	-110	-108	-111	-111	-108	-111	-110	-107	
	38.4		-104	-104	-101	-104	-104	-101	-104	-103	-101	dBm
	250		-93	-94	-91	-93	-93	-90	-93	-93	-90	1

5.55 Typical Sensitivity, 868 MHz, Sensitivity-Optimized Setting

PARAMETER	DATA RATE (kBaud)	V _{cc}		2 V			3 V			3.6 V		
		T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
	1.2		-109	-109	-107	-109	-109	-106	-109	-108	-106	
Sensitivity,	38.4		-102	-102	-100	-102	-102	-99	-102	-101	-99	alData
868MHz	250		-90	-90	-88	-89	-90	-87	-89	-90	-87	abm
	500		-84	-84	-81	-84	-84	-80	-84	-84	-80	

5.56 Typical Sensitivity, 915 MHz, Sensitivity-Optimized Setting

PARAMETER	DATA RATE (kBaud)	V _{cc}		2 V			3 V			3.6 V			
PARAMETER		T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT	
Sensitivity, 915MHz	1.2		-109	-109	-107	-109	-109	-106	-109	-108	-105		
	38.4		-102	-102	-100	-102	-102	-99	-103	-102	-99	dDate	
	250		-92	-92	-89	-92	-92	-88	-92	-92	-88	aBm	
	500		-87	-86	-81	-86	-86	-81	-86	-85	-80	1	

5.57 RF Transmit

 $T_A = 25^{\circ}C$, $V_{CC} = 3 \text{ V}$ (unless otherwise noted)⁽¹⁾, $P_{TX} = +10 \text{ dBm}$ (unless otherwise noted)

PARAMETER	FREQUENCY (MHz)	TEST CONDITIONS	S	MIN TY	P MAX	UNIT
	315			122 + j:	31	
Differential load	433			116 + j4	11	Ω
Impedance	868/915			86.5 + j4	13	
	315			+	12	
Output power, highest	433	Delivered to a 50- Ω single-ended load	d through the RF	+′	13	alDura
setting ⁽³⁾	868	matching network of the CC430 refere	ence design	+′	11	aBm
	915			+′		
Output power, lowest setting ⁽³⁾		Delivered to a 50- Ω single-ended load matching network of the CC430 references of the CC430 referen	d through the RF ence design		30	dBm
	100	Second harmonic			56	
	433	Third harmonic			57	
Harmonics,	000	Second harmonic			50	
radiated ⁽⁴⁾⁽⁵⁾⁽⁶⁾	868	Third harmonic			52	aBm
	045	Second harmonic		_{	50	
	915	Third harmonic		_{	54	
	245	Frequencies below 960 MHz		< -:	38	
	315	Frequencies above 960 MHz	+10 dBm Cvv	< -4	18	
	422	Frequencies below 1 GHz			15	
Hermonice, conducted	433	Frequencies above 1 GHz	+10 uBin Cw	< -4	18	dPm
Harmonics, conducted	969	Second harmonic			59	авті
	000	Other harmonics	+10 uBin Cw	<	71	
	015	Second harmonic	11 dPm CW(7)		53	
	915	Other harmonics		< -4	47	
	215	Frequencies below 960 MHz		<{	58	
	515	Frequencies above 960 MHz	+ TO UBILI CVV	<{	53	
		Frequencies below 1 GHz		< -{	54	
	433	Frequencies above 1 GHz	+10 dBm CW	<{	54	
Spurious emissions,		Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz		< -(63	dDm
not included ⁽⁸⁾		Frequencies below 1 GHz		< -4	16	авт
	868	Frequencies above 1 GHz	+10 dBm CW	< -{	59	
	000	Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz		< -{	56	
	045	Frequencies below 960 MHz		< -4	19	1
	915	Frequencies above 960 MHz		< -(63]
TX latency ⁽⁹⁾		Serial operation			8	bits

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

(2) Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna. Follow the CC430 reference designs available from the TI website.

(3) Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits. See also Application Note AN050 Using the CC1101 in the European 868MHz SRD Band (SWRA146) and design note DN013 Programming Output Power on CC1101 (SWRA168), which gives the output power and harmonics when using multi-layer inductors. The output power is then typically +10 dBm when operating at 868 or 915 MHz.

(4) The antennas used during the radiated measurements (SMAFF-433 from R.W.Badland and Nearson S331 868/915) play a part in attenuating the harmonics.

(5) Measured on EM430F6137RF900 with CW, maximum output power

(6) All harmonics are below –41.2 dBm when operating in the 902 through 928 MHz band.

(7) Requirement is -20 dBc under FCC 15.247

(8) All radiated spurious emissions are within the limits of ETSI. Also see design note DN017 CC11xx 868 or 915 MHz RF Matching (SWRA168).

(9) Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

5.58 Optimum PATABLE Settings for Various Output Power Levels and Frequency Bands

 $T_A = 25^{\circ}C, V_{CC} = 3 \text{ V} \text{ (unless otherwise noted)}^{(1)}$

		PATABLE SETTING										
OUTPUT POWER (dBill)	315 MHz	433 MHz	868 MHz	915 MHz								
-30	0x12	0x05	0x03	0x03								
-12	0x33	0x26	0x25	0x25								
-6	0x29	0x2D	0x2D	0x2D								
0	0x51	0x50	0x8D	0x8D								
10	0xC4	0xC4	0xC3	0xC3								
Maximum	0xC0	0xC0	0xC0	0xC0								

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

5.59 Typical Output Power, 315 MHz⁽¹⁾

DADAMETED	PATABLE SETTING	Vcc		2 V			3 V					
PARAMETER		Τ _Α	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
	0xC0 (max)		11.9			11.8			11.8			
	0xC4 (10 dBm)		10.3			10.3			10.3			
Output power, 315 MHz	0xC6 (default)						9.3					dBm
	0x51 (0 dBm)			0.7			0.6			0.7		
	0x29 (–6 dBm)			-6.8			-5.6			-5.3		

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

5.60 Typical Output Power, 433 MHz⁽¹⁾

DADAMETED	PATABLE SETTING	Vcc		2 V		3 V			3.6 V				
PARAMETER		TA	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT	
	0xC0 (max)			12.6			12.6			12.6			
	0xC4 (10 dBm)			10.3			10.2			10.2			
Output power, 433 MHz	0xC6 (default)						10.0					dBm	
400 WI 12	0x50 (0 dBm)			0.3			0.3			0.3			
	0x2D (6 dBm)			-6.4			-5.4			-5.1			

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

5.61 Typical Output Power, 868 MHz⁽¹⁾

DADAMETED	PATABLE SETTING	Vcc	2 V			3 V			3.6 V			
PARAMETER		T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
	0xC0 (max)		11.9	11.2	10.5	11.9	11.2	10.5	11.9	11.2	10.5	
	0xC3 (10 dBm)		10.8	10.1	9.4	10.8	10.1	9.4	10.7	10.1	9.4	
Output power, 868 MHz	0xC6 (default)						8.8					dBm
	0x8D (0 dBm)		1.0	0.3	-0.3	1.1	0.3	-0.3	1.1	0.3	-0.3	
	0x2D (-6 dBm)		-6.5	-6.8	-7.3	-5.3	-5.8	-6.3	-4.9	-5.4	-6.0	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

5.62 Typical Output Power, 915 MHz⁽¹⁾

DADAMETED	PATABLE SETTING	V _{cc}		2 V			3 V			3.6 V		LINUT
		T _A	–40°C	25°C	85°C	–40°C	25°C	85°C	–40°C	25°C	85°C	UNIT
	0xC0 (max)		12.2	11.4	10.6	12.1	11.4	10.7	12.1	11.4	10.7	
	0xC3 (10 dBm)		11.0	10.3	9.5	11.0	10.3	9.5	11.0	10.3	9.6	
Output power, 915 MHz	0xC6 (default)						8.8					dBm
	0x8D (0 dBm)		1.9	1.0	0.3	1.9	1.0	0.3	1.9	1.1	0.3	1
	0x2D (-6 dBm)		-5.5	-6.0	-6.5	-4.3	-4.8	-5.5	-3.9	-4.4	-5.1	

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.

5.63 Frequency Synthesizer Characteristics

 $T_A = 25^{\circ}C$, $V_{CC} = 3 V$ (unless otherwise noted)⁽¹⁾

MIN figures are given using a 27MHz crystal. TYP and MAX figures are given using a 26MHz crystal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Programmed frequency resolution ⁽²⁾	26- to 27-MHz crystal	397	f _{XOSC} /2 ¹⁶	412	Hz		
Synthesizer frequency tolerance ⁽³⁾			±40		ppm		
	50-kHz offset from carrier		-95				
	100-kHz offset from carrier		-94				
	200-kHz offset from carrier		-94				
	500-kHz offset from carrier		-98		dBc/Hz		
RF camer phase hoise	1-MHz offset from carrier		-107				
	2-MHz offset from carrier		-112				
	5-MHz offset from carrier		-118				
	10-MHz offset from carrier		-129		l		
PLL turnon or hop time ⁽⁴⁾	Crystal oscillator running	85.1	88.4	88.4	μs		
PLL RX-to-TX settling time ⁽⁵⁾		9.3	9.6	9.6	μs		
PLL TX-to-RX settling time ⁽⁶⁾		20.7	21.5	21.5	μs		
PLL calibration time ⁽⁷⁾		694	721	721	μs		

All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range. (1)

The resolution (in Hz) is equal for all frequency bands. (2)

(3) Depends on crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth and spacing.

Time from leaving the IDLE state until arriving in the RX, FSTXON, or TX state, when not performing calibration. (4)

Settling time for the 1-IF frequency step from RX to TX Settling time for the 1-IF frequency step from TX to RX (5)

(6)

Calibration can be initiated manually or automatically before entering or after leaving RX/TX. (7)

5.64 Typical RSSI_offset Values

 T_{A} = 25°C, V_{CC} = 3 V (unless otherwise noted)^{(1)}

	RSSI_OFFSET (dB)				
DATA RATE (RBaud)	433 MHz	868 MHz			
1.2	74	74			
38.4	74	74			
250	74	74			
500	74	74			

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range.



Figure 5-25. Typical RSSI Value vs Input Power Level for Different Data Rates at 868 MHz

5.65 3D LF Front-End Parameters

5.66 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{BAT}	Supply voltage range during LF operation	2.0		3.6	V
RF crystal load capacitance		10	13	20	pF
RF crystal effective series resistance				100	Ω

5.67 Resonant Circuits – LF Front End

The resonance circuit quality factor QOP can have a wide range between 10 and 120. The resonance frequency can be trimmed by the embedded trimming capacitor array.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{RES}	Resonant circuit frequency	25°C	133.2	134.2	135.2	
fL	Low hit tronomit from one	25°C, Q _{OP} = 10 to 120	133.2	134.2	135.2	
	Low-bit transmit frequency	-40° C to 85°C, Q _{OP} = 10 to 120	132.2	134.2	136.2	kHz
f _H	Lich hit transmit fraguency	25°C, Q _{OP} = 10 to 120	123.2	124.2	125.2	
	rign-bit transmit frequency	-40° C to 85°C, Q _{OP} = 10 to 120	122.2	124.2	126.2	

5.68 External Antenna Coil – LF Front End

The antenna coil LR, resonant capacitor CR and charge capacitor CL are external components with following recommended parameters

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L _{R1}	Equivalent inductance	25°C, f = 134.2 kHz	7.37	7.6	7.81	mH
L _{R2}	Equivalent inductance	25°C, f = 134.2 kHz	4.37	4.5	4.63	mH
dL _R /L _R dT	Temperature coefficient of LR	–40°C to 85°C			250	ppm/°C
Q _{LRT}	Quality factor of LR	–40°C to 85°C	10		150	

5.69 Resonant Circuit Capacitor – LF Front End

The input capacitance of the RF pins C_{RF} is the sum of parasitic capacitances of circuit blocks connected to the RF pin. The trimming capacitors are internal capacitances and can be programmed on or off. The resonance capacitor C_R is an external component and is not part of this IC.

-	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _R	Resonant circuit capacitor (option 1) (dCR = $\pm 2.0\%$)	LR = 7.6mH	147	150	153	pF
C _R	Resonant circuit capacitor (option 2) (dCR = $\pm 2.0\%$)	LR = 4.5mH	264.6	270	275.4	pF
	Dielectric of CR	dL _R /L _R dT ≤ 250 ppm		NPO		
$dC_R/C_R dT$	Temperature coefficient of CR (NP0)	dLR/LRdT ≤ 250 ppm		±30	73	ppm/°C
Q _{CR}	Quality factor		2000			
V _{RF}	Operating voltage		20	50		V _{PP}
C _{RF}	RF input capacitance	VCL = 5 V CT = off	21.3	24	26.6	pF
Q _{RF}	IC input quality factor (RF1, RF2, RF3)	VRF = 0.1 V, CT = max, CM = on or off	250	350		
	Capacitance voltage dependancy	VCL = 0 to 5 V, CT = on or off		-1		%/V
T _{step}	Trimming steps			128		
CT _{min}	Minimum trimming capacitor			0		pF
CT _{max}	Maximum trimming capacitor (CT = CT1 + CT2 + + CT7)	Calculated	70.8	74.7	78.8	pF
CT1	Trimming capacitor 1			0.6		pF
CT2	Trimming capacitor 2			1.2		pF

Resonant Circuit Capacitor – LF Front End (continued)

The input capacitance of the RF pins C_{RF} is the sum of parasitic capacitances of circuit blocks connected to the RF pin. The trimming capacitors are internal capacitances and can be programmed on or off. The resonance capacitor C_R is an external component and is not part of this IC.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CT3	Trimming capacitor 3			2.4		pF
CT4	Trimming capacitor 4			4.7		pF
CT5	Trimming capacitor 5			9.4		pF
CT6	Trimming capacitor 6			18.8		pF
CT7	Trimming capacitor 7			37.6		pF
dCT/dV	Voltage coefficient of CT				0.1	pF/V
dCT/dT	Temperature coefficient of CT				0.02	pF/K
CM1	Modulation capacitor 4.5 mH: CM1 + CM2 7.6 mH: CM1	Integrated capacitor	33.1	35.0	36.9	pF
CM2	Modulation capacitor	Integrated capacitor	17.0	18.0	19.0	pF
dCM/dV	Modulation capacitor voltage coefficient	25°C			0.1	%/V
dCM/dT	Modulation capacitor voltage coefficient				0.02	pF/K

5.70 Charge Capacitor – LF Front End

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
CL	Charge capacitor (dCL = $\pm 10\%$)	25°C, Q _{OP} = 134.2 kHz	198	220	242	nF
dCL(T)	Temperature coefficient of CL	–40°C to 85°C	-10%		10%	
	Dielectric of CL			XR7		
DCL(t)	Charge capacitor aging	100000 h	-10%		0%	

5.71 LF Wake Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{RES,PE}	Resonant circuit frequency	25°C	110		140	kHz
t _{WakeUp}	Wake-up time		500	560	1000	μs
I _{PESBWP}	Standby current	Wake pattern A active, wake pattern B off, regular sensitivity, VBAT = 3 V		4.4		μΑ
V _{WAKEA}	Sensitivity A (regular)	Configured to highest sensitivity	2.6	3.7	6.2	mV_{pp}
V _{WAKEA}	Sensitivity A (regular)	Configured to lowest sensitivity	9	13.5	23	mV _{pp}
V _{WAKEA}	Sensitivity A (high sensitivity mode)	Configured to highest sensitivity and high sensitivity mode	0.3	0.5	0.9	mV _{pp}
V _{WAKEB}	Sensitivity B	Configured to highest sensitivity	2.3	4.2	7.5	mV_{pp}
V _{WAKEB}	Sensitivity B	Configured to lowest sensitivity	50	110	200	mV_{pp}
VRF	Maximum RF input voltage				10	V _{pp}
S/N	Wake pattern detection error rate (S/N)			10		dB
t _{sA}	WDE settling time (wake A, low sensitivity)				500	μs
t _{sAh}	WDE settling time (wake A, high sensitivity)				600	μs
t _{s\B}	WDE settling time (wake B)				2000	μs
t _{resA}	WDE resettling time (strong burst recovery time)	Step VRF 2Vpp to 10mVpp			3000	μs

5.72 RSSI - LF Wake Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT
DR	Dynamic range		72		dB
VRF	Input voltage range	0.002		8	Vpp
A	RSSI linear coefficient		28		
В	RSSI constant coefficient		180		
#RSSI	Number of RSSI values		128		
Verr16mV	Absolute RSSI error at VRF = 16 mVpp	-1.28		1.28	mVpp
err16mV	Relative RSSI error VRF ≥ 16 mVpp	-8%		8%	
Verr2mV	Absolute RSSI error at VRF = 2 mVpp	-0.4		0.4	mVpp
err2mV	Relative RSSI error at VRF = 2 mVpp	-20%		20%	
Vmin	Resolution at VRF = 2 mVpp	0.14			mV
t	Measurement time (all three channels)			2	ms



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6 Detailed Description

6.1 3D LF Wake Receiver and 3D Transponder Interface

Figure 6-1 shows the LF interface block diagram.



Figure 6-1. LF Interface Block Diagram

The LF front end provides a SPI that is used for the communication with the CPU core. Data access, configuration, and status queries to the MSP430 core are executed with predefined commands over this interface, which is internally connected to IO ports (see Table 6-1).

MICROCONTROLLER PORT		LF FRONT-END MODULE PORT
P3.1	Input	SPI_SOMI
P3.2	Output	SPI_SIMO
P3.3	Output	SPI_CLK
P3.5	Input	CLK_OUT
P4.1	Input	EOB
P4.2	Input	SPI_BUSY

able 6-1. Intermodule	• Connections	for RF430F59xx
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6.1.1 3D LF Front End

The 3D LF front end provides two basic operation modes: transponder mode and wake receiver mode. The LF front end provides an external trigger to wake up the microcontroller on LF reception. Data received by the LF interface and status of the device can be read through SPI communication. Features of the LF front end include:

- Resonant frequency: 134.2 kHz
- Embedded resonant trimming for all three resonant circuits
- Quality factor range: 10 to 60
- Antenna Inductance 2.66 mH, 4.5 mH, or 7.6 mH
- AES-128 hardware-encryption coprocessor
- 3D wake receiver
 - Fixed downlink start pattern S10
 - Downlink data rate up to 4 kBps with bit-length coding
 - Two independent wake patterns WP A or WP B with 0-, 4-, 8-, 12-, 16-, 20-, or 24-bit length
 - Dedicated sensitivity levels for both WP
 - Digital RSSI 72 dB, 8-bit logarithmic
 - Accuracy ±8% in near distance (<16 mVpp)
 - Accuracy ±20% in far distance (>16 mVpp)
- 3D RFID transponder interface
 - Batteryless operation
 - Fixed downlink start pattern S01
 - Transponder read range up to 4 inches (10 cm)
 - Half-duplex communication protocol
 - Adaptive downlink data rate: up to 4 kbaud with ASK, bit-length coding
 - Uplink data rate: up to 8 kbaud with FSK
 - Selectable challenge/response length of 32/32, 64/64, or 96/64 bit
 - Mutual authentication for all commands with 32-bit reader signature
 - Selective addressing mode, 8 bit
 - Burst read mode
 - Anticollision encryption

6.1.2 EEPROM

The EEPROM can be accessed by SPI commands. Features of the EEPROM include:

- Total memory size: 2048 Bytes
- User memory size: 1776 Bytes
 - User memory has up to 4 banks
 - User memory is organized in 64 pages per bank of 8 bytes each
- EEPROM has one system memory bank organized in 64 pages of 4 bytes each.
 - System memory is organized in 64 pages of 4 bytes each
 - System memory is used for special information (configuration, four 128-bit encryption keys, counter values)
- The memory pages are configurable and provide different access modes
 - General-purpose memory (general read, program, and lock)
 - System only data (mutual only access)
 - Microcontroller only data (no access over LF interface)
 - Secured data (mutual program and lock, general read)
- All pages can be locked separately (no reprogramming possible)

Table 6-2 summarizes the EEPROM organization.

6.1.3 Switch Interface

The switch interface provides eight inputs. Features of the switch interface include:

- Internal pullups to minimize external components
- Embedded stuck button handling
- Embedded debouncing for each switch debounce time: 10, 20, 40, or 80 ms

Table 6-2. LF Front End EEPROM Memory Map

EEPROM (MEM)										
DANK	BYTE						PACE			
DAINK	7	6 5 4 3 2 1 0 P					FAC) C		
				Us	er Data				0	
					÷				:	
0				Us	er Data				7	
	<u> </u>						:			
	User Data						63			
				Us	er Data				0	
					÷				:	
1				Us	er Data				7	
									:	
				Us	er Data				63	,
				Us	ser Data				0	
_					-				:	
2		User Data						7		
		:								
				Us	ser Data				63	
	User Data							U :		
2					: or Doto					
3				08						
	Liser Data						29)		
						· · · · · · · · · · · · · · · · · · ·			1	0
									3	2
								5	4	
									7	6
		Configuration Data			Configuration Data			9	8	
									11	10
									13	12
7								15	14	
								17	16	
									19	18
									21	20
						E and the Kan			23	22
		Епстури	un reys			Encrypt	ion neys		25	24
								27	26	
									29	28
									31	30

6.2 Sub-1-GHz Radio

The sub-1-GHz radio module is based on the industry-leading CC1101 and requires very few external components. Figure 6-2 shows a high-level block diagram of the implemented radio.



Figure 6-2. Sub-1-GHz Radio Block Diagram

The radio features a low intermediate frequency (IF) receiver. The received RF signal is amplified by a low-noise amplifier (LNA) and down converted in quadrature to the IF. At the IF, the I/Q signals are digitized. Automatic gain control (AGC), fine channel filtering, and demodulation bit and packet synchronization are performed digitally.

The transmitter is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90-degree phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

The 26-MHz crystal oscillator generates the reference frequency for the synthesizer and the clocks for the ADC and the digital peripherals.

A memory-mapped register interface is used for data access, configuration, and status request by the CPU.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

For complete module descriptions, see the *RF430F5978 User's Guide* (SLAU378).



6.3 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-toregister operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.4 **Operating Modes**

The device has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following operating modes can be configured by software:

- Active mode (AM)
- All clocks are active
- Low-power mode 0 (LPM0)
- CPU is disabled
- ACLK and SMCLK remain active, MCLK is disabled
- FLL loop control remains active
- Low-power mode 1 (LPM1)
- CPU is disabled
- FLL loop control is disabled
- ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DC generator of the DCO remains enabled
 - ACLK remains active

- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - Crystal oscillator is stopped
 - Complete data retention

6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Time-out, Password Violation Flash Memory Password Violation	WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)}	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ^{(1) (3)}	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV) $^{(1)}$ $^{(3)}$	(Non)maskable	0FFFAh	61
Comparator_B	Comparator_B Interrupt Flags (CBIV) ⁽¹⁾	Maskable	0FFF8h	60
Watchdog Interval Timer Mode	WDTIFG	Maskable	0FFF6h	59
USCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) ⁽¹⁾	Maskable	0FFF4h	58
USCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG, I ² C Status Interrupt Flags (UCB0IV) ⁽¹⁾	Maskable	0FFF2h	57
ADC12_A	ADC12IFG0 ADC12IFG15 (ADC12IV) ⁽¹⁾	Maskable	0FFF0h	56
TAO	TA0CCR0 CCIFG0	Maskable	0FFEEh	55
TA0	TA0CCR1 CCIFG1 TA0CCR4 CCIFG4, TA0IFG (TA0IV) ⁽¹⁾	Maskable	0FFECh	54
RF1A CC1101-based Radio	Radio Interface Interrupt Flags (RF1AIFIV) Radio Core Interrupt Flags (RF1AIV)	Maskable	0FFEAh	53
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ⁽¹⁾	Maskable	0FFE8h	52
TA1	TA1CCR0 CCIFG0	Maskable	0FFE6h	51
TA1	TA1CCR1 CCIFG1 TA1CCR2 CCIFG2, TA1IFG (TA1IV) ⁽¹⁾	Maskable	0FFE4h	50
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾	Maskable	0FFE2h	49
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾	Maskable	0FFE0h	48
Reserved	Reserved ⁽⁴⁾		0FFDEh	47
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ⁽¹⁾	Maskable	0FFDCh	46
AES	AESRDYIFG	Maskable	0FFDAh	45
			0FFD8h	44
Reserved	Reserved ⁽⁴⁾		:	:
			0FF80h	0, lowest

Table 6-3. Interrupt Sources, Flags, and Vectors

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space.

(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.

(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.



6.6 Memory Organization

Table 6-4 summarizes the memory organization of the device.

		RF430F5978 ⁽¹⁾
Main Memory (flash)	Total Size	32KB
Main: Interrupt vector		00FFFFh to 00FF80h
Main: code memory	Bank 0	32KB 00FFFFh to 008000h
RAM	Total Size	4KB
	Sect 1	2KB 002BFFh to 002400h
	Sect 0	2KB 0023FFh to 001C00h
		128 B 001AFFh to 001A80h
Device descriptor		128 B 001A7Fh to 001A00h
	Info A	128 B 0019FFh to 001980h
Information memory	Info B	128 B 00197Fh to 001900h
(flash)	Info C	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h
	BSL 3	512 B 0017FFh to 001600h
Bootloader (BSL)	BSL 2	512 B 0015FFh to 001400h
memory (flash)	BSL 1	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h
Peripherals		4KB 000FFFh to 0h

Table 6-4. Memory Organization

(1) All memory regions not specified here are vacant memory, and any access to them causes a Vacant Memory Interrupt.

6.7 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory through the BSL is protected by an user-defined password. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming With the Bootloader User's Guide* (SLAU319). Table 6-5 lists the BSL in requirements.

DEVICE SIGNAL	BSL FUNCTION	
RST/NMI/SBWTDIO	Entry sequence signal	
TEST/SBWTCK	Entry sequence signal	
P1.6	Data transmit	
P1.5	Data receive	
VCC	Power supply	
VSS	Ground supply	

Table 6-5. UART BSL Pin Requirements and Functions

6.8 JTAG Operation

6.8.1 JTAG Standard Interface

The RF430F5978 supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin enables the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO pin is required to interface with MSP430 development tools and device programmers. Table 6-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the RF430F5978 supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply
VSS		Ground supply

6.9 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (Info A to Info D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments Info A to Info D can be erased individually, or as a group with the main memory segments. Segments Info A to Info D are also called *information memory*.
- Segment A can be locked separately.

6.10 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors of 2KB each.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the *RF430F5978 User's Guide* (SLAU378).

6.11.1 Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources that are available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.11.2 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitor (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.11.3 Digital I/O

Five I/O ports are implemented: ports P1 through P3 are 8 bit, P4 is 1 bit, and P5 is 2 bit.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P3) or word-wise in pairs (PA and PB).



6.11.4 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port pins of ports P1 through P3. Table 6-8 lists the available port mapping assignments, and Table 6-9 lists the default assignments.

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)	
0	PM_NONE	None	DVSS	
1 ⁽¹⁾	PM_CBOUT0	-	Comparator_B output (on TA0 clock input)	
	PM_TA0CLK	TA0 clock input	_	
2 ⁽¹⁾	PM_CBOUT1	-	Comparator_B output (on TA1 clock input)	
	PM_TA1CLK	TA1 clock input	_	
3	PM_ACLK	None	ACLK output	
4	PM_MCLK	None	MCLK output	
5	PM_SMCLK	None	SMCLK output	
6	PM_RTCCLK	None	RTCCLK output	
- (1)	PM_ADC12CLK	-	ADC12CLK output	
	PM_DMAE0	DMA external trigger input	_	
8	PM_SVMOUT	None	SVM output	
9	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0	
10	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1	
11	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2	
12	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3	
13	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4	
14	PM_TA1CCR0A	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0	
15	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1	
16	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2	
47(2)	PM_UCA0RXD	USCI_A0 UART RXD (direction	on controlled by USCI – input)	
17/	PM_UCA0SOMI	USCI_A0 SPI slave out/master	in (direction controlled by USCI)	
10(2)	PM_UCA0TXD	USCI_A0 UART TXD (direction	n controlled by USCI – output)	
10(-/	PM_UCA0SIMO	USCI_A0 SPI slave in/master o	ut (direction controlled by USCI)	
40(3)	PM_UCA0CLK	USCI_A0 clock input/output	(direction controlled by USCI)	
19(*)	PM_UCB0STE	USCI_B0 SPI slave transmit enable	(direction controlled by USCI – input)	
20 (4)	PM_UCB0SOMI	USCI_B0 SPI slave out/master	in (direction controlled by USCI)	
2017	PM_UCB0SCL	USCI_B0 I ² C clock (open drain and direction controlled by USCI)		
21 (4)	PM_UCB0SIMO	USCI_B0 SPI slave in/master out (direction controlled by USCI)		
2117	PM_UCB0SDA	USCI_B0 I ² C data (open drain and direction controlled by USCI)		
22 ⁽⁵⁾	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)		
22	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI – input)		
23	PM_RFGDO0	Radio GDO0 (direction controlled by radio)		
24	PM_RFGDO1	Radio GDO1 (direction controlled by radio)		
25	PM_RFGDO2	Radio GDO2 (direction controlled by Radio)		

Table 6-8. Port Mapping Mnemonics and Functions

(1) Input or output function is selected by the corresponding setting in the port direction register PxDIR.

(2) UART or SPI functionality is determined by the selected USCI mode.

(3) UCA0CLK function takes precedence over UCB0STE function. If the mapped pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode even if 4-wire mode is selected.

(4) SPI or I²C functionality is determined by the selected USCI mode. If I²C functionality is selected, the output of the mapped pin drives only the logical 0 to V_{SS} level.

(5) UCBOCLK function takes precedence over UCA0STE function. If the mapped pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire mode is selected.

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Table 6-8. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)
26	Reserved	None	DVSS
27	Reserved	None	DVSS
28	Reserved	None	DVSS
29	Reserved	None	DVSS
30	Reserved	None	DVSS
31 (0FFh) ⁽⁶⁾	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cros currents when applying analog signals.	

(6) The value of the PM_ANALOG mnemonic is FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION (PxDIR.y = 0)	OUTPUT PIN FUNCTION (PxDIR.y = 1)	
P1.0/P1MAP0	PM_RFGDO0	None	Radio GDO0	
P1.1/P1MAP1	PM_RFGDO2	None	Radio GDO2	
P1.2/P1MAP2	PM_UCB0SOMI/PM_UCB0SCL	USCI_B0 SPI slave out/master USCI_B0 I ² C clock (open drain a	in (direction controlled by USCI) and direction controlled by USCI)	
P1.3/P1MAP3	PM_UCB0SIMO/PM_UCB0SDA	USCI_B0 SPI slave in/master of USCI_B0 I ² C data (open drain a	ut (direction controlled by USCI) nd direction controlled by USCI)	
P1.4/P1MAP4	PM_UCB0CLK/PM_UCA0STE	USCI_B0 clock input/output (USCI_A0 SPI slave transmit enable	direction controlled by USCI) (direction controlled by USCI – input)	
P1.5/P1MAP5	PM_UCA0RXD/PM_UCA0SOMI	USCI_A0 UART RXD (direction USCI_A0 SPI slave out/master	on controlled by USCI – input) in (direction controlled by USCI)	
P1.6/P1MAP6	PM_UCA0TXD/PM_UCA0SIMO	USCI_A0 UART TXD (directio USCI_A0 SPI slave in/master or	n controlled by USCI – output) ut (direction controlled by USCI)	
P1.7/P1MAP7	PM_UCA0CLK/PM_UCB0STE	USCI_A0 clock input/output (direction controlled by USCI) USCI_B0 SPI slave transmit enable (direction controlled by USCI – input)		
P2.0/P2MAP0	PM_CBOUT1/PM_TA1CLK	TA1 clock input	Comparator_B output	
P2.1/P2MAP1	PM_TA1CCR0A	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0	
P2.2/P2MAP2	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1	
P2.3/P2MAP3	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2	
P2.4/P2MAP4	PM_RTCCLK	None	RTCCLK output	
P2.5/P2MAP5	PM_SVMOUT	None	SVM output	
P2.6/P2MAP6	PM_ACLK	None	ACLK output	
P2.7/P2MAP7	PM_ADC12CLK/PM_DMAE0	DMA external trigger input	ADC12CLK output	
P3.0/P3MAP0	PM_CBOUT0/PM_TA0CLK	TA0 clock input	Comparator_B output	
P3.1/P3MAP1	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0	
P3.2/P3MAP2	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1	
P3.3/P3MAP3	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2	
P3.4/P3MAP4	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3	
P3.5/P3MAP5	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4	
P3.6/P3MAP6	PM_RFGDO1	None	Radio GDO1	
P3.7/P3MAP7	PM_SMCLK	None	SMCLK output	

Table 6-9. Default Mapping



6.11.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These functions include poweron reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. Table 6-10 lists the interrupt vector registers supported by the SYS module.

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
		No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RST/NMI (POR)	04h	
		DoBOR (BOR)	06h	
		Reserved	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
	01055	SVML_OVP (POR)	10h	
STSKSTIV, System Reset	019En	SVMH_OVP (POR)	12h	
		DoPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		DLYLIFG	06h	
		DLYHIFG	08h	
SYSSNIV, System NMI		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		VLRLIFG	10h	
		VLRHIFG	12h	
		Reserved	14h to 1Eh	Lowest
		No interrupt pending	00h	
		NMIIFG	02h	Highest
SYSUNIV, User NMI	019Ah	OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h to 1Eh	Lowest

	Table 6-10.	System	Module	Interrupt	Vector	Registers
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6.11.6 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. Table 6-11 lists the available DMA trigger assignments.

TRICCER	CHANNEL				
IRIGGER	0	1	2		
0	DMAREQ	DMAREQ	DMAREQ		
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG		
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG		
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG		
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG		
5	Reserved	Reserved	Reserved		
6	Reserved	Reserved	Reserved		
7	Reserved	Reserved	Reserved		
8	Reserved	Reserved	Reserved		
9	Reserved	Reserved	Reserved		
10	Reserved	Reserved	Reserved		
11	Reserved	Reserved	Reserved		
12	Reserved	Reserved	Reserved		
13	Reserved	Reserved	Reserved		
14	Reserved	Reserved	Reserved		
15	Reserved	Reserved	Reserved		
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG		
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG		
18	UCB0RXIFG	UCB0RXIFG	UCBORXIFG		
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG		
20	Reserved	Reserved	Reserved		
21	Reserved	Reserved	Reserved		
22	Reserved	Reserved	Reserved		
23	Reserved	Reserved	Reserved		
24	ADC12IFGx	ADC12IFGx	ADC12IFGx		
25	Reserved	Reserved	Reserved		
26	Reserved	Reserved	Reserved		
27	Reserved	Reserved	Reserved		
28	Reserved	Reserved	Reserved		
29	MPY ready	MPY ready	MPY ready		
30	DMA2IFG	DMA0IFG	DMA1IFG		
31	DMAE0	DMAE0	DMAE0		

Table 6-11. DMA Trigger Assignments⁽¹⁾

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.



6.11.7 Watchdog Timer (WDT_A)

The primary function of the watchdog timer is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

6.11.8 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.11.9 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.11.10 AES128 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

6.11.11 Universal Serial Communication Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, and IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) and I²C.

A USCI_A0 and USCI_B0 module are implemented.

6.11.12 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers (see Table 6-12).

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
PM_TA0CLK	TACLK			
ACLK (internal)	ACLK	 .	NA	
SMCLK (internal)	SMCLK	Timer	NA	
RFCLK/192 ⁽¹⁾	INCLK			
PM_TA0CCR0A	CCI0A			PM_TA0CCR0A
DV _{SS}	CCI0B	CCDO	TAO	
DV _{SS}	GND	CCRU	TAU	
DV _{CC}	V _{CC}			
PM_TA0CCR1A	CCI1A			PM_TA0CCR1A
CBOUT (internal)	CCI1B	CCR1	TA1	ADC12 (internal) ADC12SHSx = {1}
DV _{SS}	GND			
DV _{CC}	V _{CC}			
PM_TA0CCR2A	CCI2A		TA2	PM_TA0CCR2A
ACLK (internal)	CCI2B	CCP2		
DV _{SS}	GND	CORZ		
DV _{CC}	V _{CC}			
PM_TA0CCR3A	CCI3A			PM_TA0CCR3A
GDO1 from Radio (internal)	CCI3B	CCR3	ТАЗ	
DV _{SS}	GND			
DV _{CC}	V _{CC}			
PM_TA0CCR4A	CCI4A			PM_TA0CCR4A
GDO2 from Radio (internal)	CCI4B	CCR4	TA4	
DV _{SS}	GND			
DV _{CC}	V _{CC}			

Table 6-12. TA0 Signal Connections

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.


6.11.13 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers (see Table 6-13).

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
				PZ
PM_TA1CLK	TACLK			
ACLK (internal)	ACLK	Timor	NIA	
SMCLK (internal)	SMCLK	Timer	INA	
RFCLK/192 ⁽¹⁾	INCLK			
PM_TA1CCR0A	CCI0A	CCR0		PM_TA1CCR0A
RF Async. Output (internal)	CCI0B		TAO	RF Async. Input (internal)
DV _{SS}	GND			
DV _{CC}	V _{CC}			
PM_TA1CCR1A	CCI1A			PM_TA1CCR1A
CBOUT (internal)	CCI1B	0004	T A4	
DV _{SS}	GND	CCRT	IAI	
DV _{CC}	V _{CC}			
PM_TA1CCR2A	CCI2A	CCR2		PM_TA1CCR2A
ACLK (internal)	CCI2B		TAO	
DV _{SS}	GND		I AZ	
DV _{CC}	V _{CC}			

Table 6-13. TA1 Signal Connections

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.

6.11.14 Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.11.15 REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC12_A, LCD_B, and COMP_B modules.

6.11.16 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.11.17 ADC12_A

The ADC12_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.11.18 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.11.19 Peripheral File Map

 Table 6-14 lists the register base address and offset range for each peripheral.
 Table 6-15 through

 Table 6-45 list the registers that are available in each peripheral.

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-15)	0100h	000h-01Fh
PMM (see Table 6-16)	0120h	000h-00Fh
Flash Control (see Table 6-17)	0140h	000h-00Fh
CRC16 (see Table 6-18)	0150h	000h-007h
RAM Control (see Table 6-19)	0158h	000h-001h
Watchdog (see Table 6-20)	015Ch	000h-001h
UCS (see Table 6-21)	0160h	000h-01Fh
SYS (see Table 6-22)	0180h	000h-01Fh
Shared Reference (see Table 6-23)	01B0h	000h-001h
Port Mapping Control (see Table 6-24)	01C0h	000h-007h
Port Mapping Port P1 (see Table 6-25)	01C8h	000h-007h
Port Mapping Port P2 (see Table 6-26)	01D0h	000h-007h
Port Mapping Port P3 (see Table 6-27)	01D8h	000h-007h
Port P1, P2 (see Table 6-28)	0200h	000h-01Fh
Port P3, P4 (see Table 6-29)	0220h	000h-01Fh
Port P5 (see Table 6-30)	0240h	000h-01Fh
Port PJ (see Table 6-31)	0320h	000h-01Fh
TA0 (see Table 6-32)	0340h	000h-03Fh
TA1 (see Table 6-33)	0380h	000h-03Fh
RTC_A (see Table 6-34)	04A0h	000h-01Fh
32-Bit Hardware Multiplier (see Table 6-35)	04C0h	000h-02Fh
DMA Module Control (see Table 6-36)	0500h	000h-00Fh
DMA Channel 0 (see Table 6-37)	0510h	000h-00Fh
DMA Channel 1 (see Table 6-38)	0520h	000h-00Fh
DMA Channel 2 (see Table 6-39)	0530h	000h-00Fh
USCI_A0 (see Table 6-40)	05C0h	000h-01Fh
USCI_B0 (see Table 6-41)	05E0h	000h-01Fh
ADC12 (see Table 6-42)	0700h	000h-03Fh
Comparator_B (see Table 6-43)	08C0h	000h-00Fh
AES Accelerator (see Table 6-44)	09C0h	000h-00Fh
Radio Interface (see Table 6-45)	0F00h	000h-03Fh

Table 6-14. Peripherals



REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-15. Special Function Registers (Base Address: 0100h)

Table 6-16. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-17. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-18. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-19. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-20. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h



REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 6-21. UCS Registers (Base Address: 0160h)

Table 6-22. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-23. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 6-24. Port Mapping Control Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key register	PMAPKEYID	00h
Port mapping control register	PMAPCTL	02h

Table 6-25. Port Mapping Port P1 Registers (Base Address: 01C8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1.0 mapping register	P1MAP0	00h
Port P1.1 mapping register	P1MAP1	01h
Port P1.2 mapping register	P1MAP2	02h
Port P1.3 mapping register	P1MAP3	03h
Port P1.4 mapping register	P1MAP4	04h
Port P1.5 mapping register	P1MAP5	05h
Port P1.6 mapping register	P1MAP6	06h
Port P1.7 mapping register	P1MAP7	07h

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REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2.0 mapping register	P2MAP0	00h
Port P2.1 mapping register	P2MAP2	01h
Port P2.2 mapping register	P2MAP2	02h
Port P2.3 mapping register	P2MAP3	03h
Port P2.4 mapping register	P2MAP4	04h
Port P2.5 mapping register	P2MAP5	05h
Port P2.6 mapping register	P2MAP6	06h
Port P2.7 mapping register	P2MAP7	07h

Table 6-26. Port Mapping Port P2 Registers (Base Address: 01D0h)

Table 6-27. Port Mapping Port P3 Registers (Base Address: 01D8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3.0 mapping register	P3MAP0	00h
Port P3.1 mapping register	P3MAP3	01h
Port P3.2 mapping register	P3MAP2	02h
Port P3.3 mapping register	P3MAP3	03h
Port P3.4 mapping register	P3MAP4	04h
Port P3.5 mapping register	P3MAP5	05h
Port P3.6 mapping register	P3MAP6	06h
Port P3.7 mapping register	P3MAP7	07h

Table 6-28. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup or pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup or pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-29. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup or pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah

Table 6-30. Port P5 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup or pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah

Table 6-31. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup or pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 6-32. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4 0Ah	
TA0 counter	TAOR	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TAOIV	2Eh

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Table 0-35. TAT Registers (Dase Address, 00001)	Tab	ole 6-33.	TA1	Registers	(Base	Address:	0380h)
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REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-34. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0 00	
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV 0Eh	
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 x 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 - signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 6-35. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)



REGISTER DESCRIPTION	REGISTER	OFFSET
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 6-36. DMA Module Control Registers (Base Address: 0500h)

Table 6-37. DMA Channel 0 Registers (Base Address: 0510h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah

Table 6-38. DMA Channel 1 Registers (Base Address: 0520h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah

Table 6-39. DMA Channel 2 Registers (Base Address: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah



Table 6-40. USCI_A0 Registers (Base Address: 05C0h)	
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REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-41. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCBORXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

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REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Table 6-42. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 6-43. Comparator_B Registers (Base Address: 08C0h)

Table 6-44. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET	
AES accelerator control register 0	AESACTL0	00h	
Reserved		02h	
AES accelerator status register	AESASTAT	04h	
AES accelerator key register	AESAKEY	06h	
AES accelerator data in register	AESADIN	008h	
AES accelerator data out register	AESADOUT	00Ah	

Table 6-45. Radio Interface Registers (Base Address: 0F00h)

	PEGISTEP	OFESET		
	RETAILCTLU	UUN		
Radio interface control 1	RF1AIFCTL1	02h		
Radio interface error flag	RF1AIFERR	06h		
Radio interface error vector word	RF1AIFERRV	0Ch		
Radio interface interrupt vector word	RF1AIFIV	0Eh		
Radio instruction word	RF1AINSTRW	10h		
Radio instruction word, 1-byte auto-read	RF1AINSTR1W	12h		
Radio instruction word, 2-byte auto-read	RF1AINSTR2W	14h		
Radio data in register	RF1ADINW	16h		
Radio status word	RF1ASTATW	20h		
Radio status word, 1-byte auto-read	RF1ASTAT1W	22h		
Radio status word, 2-byte auto-read	RF1AISTAT2W	24h		
Radio data out	RF1ADOUTW	28h		
Radio data out, 1-byte auto-read	RF1ADOUT1W	2Ah		
Radio data out, 2-byte auto-read	RF1ADOUT2W	2Ch		
Radio core signal input	RF1AIN	30h		
Radio core interrupt flag	RF1AIFG	32h		
Radio core interrupt edge select	RF1AIES	34h		
Radio core interrupt enable	RF1AIE	36h		
Radio core interrupt vector word	RF1AIV	38h		



6.12 Input/Output Schematics

6.12.1 Port P1, P1.0 to P1.4, Input/Output With Schmitt Trigger

Figure 6-3 shows the port schematic, and Table 6-46 summarizes selection of the pin function.



Figure 6-3. Port P1 (P1.0 to P1.4) Schematic

			CONTROL BITS OR SIGNALS ⁽¹⁾			
PIN NAME (P1.x)	x	FUNCTION	P1DIR.x	P1SEL.x	P1MAPx	LCDS19 to LCDS22
P1.0/P1MAP/S18	0	P1.0 (I/O)	I: 0; O: 1	0	Х	0
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0
		Output driver and input Schmitt trigger disabled	Х	1	= 31	0
		S18	х	Х	Х	1
P1.1/P1MAP1/S19	1	P1.1 (I/O)	I: 0; O: 1	0	Х	0
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0
		Output driver and input Schmitt trigger disabled	Х	1	= 31	0
		S19	Х	Х	Х	1
P1.2/P1MAP2/S20	2	P1.2 (I/O)	I: 0; O: 1	0	Х	0
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0
		Output driver and input Schmitt trigger disabled	Х	1	= 31	0
		S22	Х	Х	Х	1
P1.3/P1MAP3/S21	3	P1.3 (I/O)	I: 0; O: 1	0	Х	0
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0
		Output driver and input Schmitt trigger disabled	х	1	= 31	0
		S21	Х	Х	Х	1
P1.4/P1MAP4/S22	4	P1.4 (I/O)	I: 0; O: 1	0	Х	0
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0
		Output driver and input Schmitt trigger disabled	Х	1	= 31	0
		S22	Х	Х	Х	1

Table 6-46. Port P1 (P1.0 to P1.4) Pin Functions

(1) X = don't care

(2) According to mapped function - see Table 6-8.

6.12.2 Port P1, P1.5 to P1.7, Input/Output With Schmitt Trigger

Figure 6-4 shows the port schematic, and Table 6-47 summarizes selection of the pin function.



Figure 6-4. Port P1 (P1.5 to P1.7) Schematic

		FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾				
PIN NAME (PI.X)	X	FUNCTION	P1DIR.x	P1SEL.x	P1MAPx		
P1.5/P1MAP5/R23	5	P1.5 (I/O)	I: 0; O: 1	0	Х		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾		
		R23 ⁽³⁾	Х	1	= 31		
P1.6/P1MAP6/R13/		P1.6 (I/O)	I: 0; O: 1	0	Х		
LCDREF		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾		
		R13/LCDREF ⁽³⁾	Х	1	= 31		
P1.7/P1MAP7/R03	7	P1.7 (I/O)	I: 0; O: 1	0	Х		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾		
		R03 ⁽³⁾	Х	1	= 31		

Table 6-47. Port P1 (P1.5 to P1.7) Pin Functions

(1) X = don't care

According to mapped function - see Table 6-8.

(2) (3) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

6.12.3 Port P2, P2.0 to P2.2, Input/Output With Schmitt Trigger

Figure 6-5 shows the port schematic, and Table 6-48 summarizes selection of the pin function.





6.12.4 Port P2, P2.4 and P2.5, Input/Output With Schmitt Trigger

Figure 6-6 shows the port schematic, and Table 6-48 summarizes selection of the pin function.



Figure 6-6. Port P2 (P2.4 and P2.5) Schematic

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		FUNCTION	CC	CONTROL BITS OR SIGNALS ⁽¹⁾					
PIN NAME (P2.X)	x	FUNCTION	P2DIR.x	P2SEL.x	P2MAPx	CBPD.x			
P2.0/P2MAP0/CB0		P2.0 (I/O)	I: 0; O: 1	0	Х	0			
(/A0)		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0			
		A0 ⁽³⁾	Х	1	= 31	Х			
		CB0 ⁽⁴⁾	X	Х	Х	1			
P2.1/P2MAP1/CB1	1	P2.1 (I/O)	I: 0; O: 1	0	Х	0			
(/A1)		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	$\leq 30^{(2)}$	0			
		A1 ⁽³⁾	Х	1	= 31	Х			
		CB1 ⁽⁴⁾	Х	Х	Х	1			
P2.2/P2MAP2/CB2 (/A2)	2	P2.2 (I/O)	I: 0; O: 1	0	Х	0			
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0			
		A2 ⁽³⁾	Х	1	= 31	Х			
		CB2 ⁽⁴⁾	Х	Х	Х	1			
P2.4/P2MAP4/CB4	4	P2.4 (I/O)	I: 0; O: 1	0	Х	0			
(/A4/VREF-/VeREF-)		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	≤ 30 ⁽²⁾	0			
		A4/VREF-/VeREF- ⁽³⁾	Х	1	= 31	Х			
		CB4 ⁽⁴⁾	Х	Х	Х	1			
P2.5/P2MAP5/CB5	5	P2.5 (I/O)	I: 0; O: 1	0	Х	0			
(/A5/VREF+/VeREF+)		Mapped secondary digital function - see Table 6-8	0; 1 ⁽²⁾	1	$\leq 30^{(2)}$	0			
		A5/VREF+/VeREF+ ⁽³⁾	Х	1	= 31	Х			
		CB5 ⁽⁴⁾	Х	Х	Х	1			

Table 6-48. Port P2 (P2.0 to P2.2, P2.4, and P2.5) Pin Functions

(1) X = don't care

According to mapped function - see Table 6-8. Setting P2SEL.x bit together with P2MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger. Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog (2) (3) (4) signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

6.12.5 Port P3, P3.1 to P3.3, P3.5, and P3.7, Input/Output With Schmitt Trigger

Figure 6-7 shows the port schematic, and Table 6-49 summarizes selection of the pin function.



Figure 6-7. Port P3 (P3.1 to P3.3, P3.5, and P3.7) Schematic



			CC	NTROL BITS	OR SIGNAL	S ⁽¹⁾		
PIN NAME (P3.x)	x	FUNCTION	P3DIR.x	P3SEL.x	P3MAPx	LCDS10 to LCDS17		
P3.1/P3MAP1/S11 ⁽²⁾	1	P3.1 (I/O)	I: 0; O: 1	0	Х	0		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽³⁾	1	$\leq 30^{(3)}$	0		
		Output driver and input Schmitt trigger disabled	CONTROL BITS 0P3DIR.xP3SEL.xP)I: 0; 0: 10secondary digital function - see Table 6-80; 1 ⁽³⁾ 1river and input Schmitt trigger disabledX1XXXx)I: 0; 0: 10secondary digital function - see Table 6-80; 1 ⁽³⁾ 1river and input Schmitt trigger disabledX1river and input Schmitt trigger disabledX1xXX1xX1river and input Schmitt trigger disabledX1xXX1xX1<					
		S11	х	Х	Х	1		
P3.2/P3MAP7/S12 ⁽²⁾	2	P3.2 (I/O)	I: 0; O: 1	0	Х	0		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽³⁾	1	$\leq 30^{(3)}$	0		
		Output driver and input Schmitt trigger disabled	х	1	= 31	0		
		S12	х	Х	Х	1		
P3.3/P3MAP3/S13 ⁽²⁾	3	P3.3 (I/O)	I: 0; O: 1	0	Х	0		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽³⁾	1	$\leq 30^{(3)}$	0		
		Output driver and input Schmitt trigger disabled	х	1	= 31	0		
		S13	х	Х	Х	1		
P3.5/P3MAP5/S15 ⁽²⁾	5	P3.5 (I/O)	I: 0; O: 1	0	Х	0		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽³⁾	1	$\leq 30^{(3)}$	0		
		Output driver and input Schmitt trigger disabled	х	1	= 31	0		
		S15	х	Х	Х	1		
		S16	х	Х	Х	1		
P3.7/P3MAP7/S17	7	P3.7 (I/O)	I: 0; O: 1	0	Х	0		
		Mapped secondary digital function - see Table 6-8	0; 1 ⁽³⁾	1	$\leq 30^{(3)}$	0		
		Output driver and input Schmitt trigger disabled	Х	1	= 31	0		
		S17	Х	Х	Х	1		

Table 6-49. Port P3 (P3.1 to P3.3, P3.5, and P3.7) Pin Functions

(1) X = don't care

(2) (3) Internal connection to LF front end According to mapped function - see Table 6-8.

6.12.6 Port P4, P4.0 to P4.2, Input/Output With Schmitt Trigger

Figure 6-8 shows the port schematic, and Table 6-50 summarizes selection of the pin function.



Figure 6-8. Port P4 (P4.0 to P4.2) Schematic



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Table 6-50.	Port P4	(P4.0 to	P4.2) Pin	Functions
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			CONTROL BITS OR SIGNALS ⁽¹⁾				
PIN NAME (P4.x)	x	FUNCTION	P4DIR.x	P4SEL.x	LCDS2 to LCDS7		
P4.0/P4MAP0/S2	0	P4.0 (I/O)	I: 0; O: 1	0	0		
		N/A	0	1	0		
		DVSS	1	1	0		
		S2	Х	Х	1		
P4.1/P4MAP1/S3 ⁽²⁾	1	P4.1 (I/O)	I: 0; O: 1	0	0		
		N/A	0	1	0		
		DVSS	1	1	0		
		S3	Х	Х	1		
P4.2/P4MAP7/S4 ⁽²⁾	2	P4.2 (I/O)	I: 0; O: 1	0	0		
		N/A	0	1	0		
		DVSS	1	1	0		
		S4	Х	Х	1		

(1) X = don't care(2) Internal connect

(2) Internal connection to LF front end

6.12.7 Port P5, P5.0, Input/Output With Schmitt Trigger

Figure 6-9 shows the port schematic, and Table 6-51 summarizes selection of the pin function.



Figure 6-9. Port P5 (P5.0) Schematic

6.12.8 Port P5, P5.1, Input/Output With Schmitt Trigger

Figure 6-10 shows the port schematic, and Table 6-51 summarizes selection of the pin function.



Figure 6-10. Port P5 (P5.1) Schematic

PIN NAME (P5.x)		FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾						
		FUNCTION	P5DIR.x	P5SEL.0	P5SEL.1	XT1BYPASS X 0 1 X 0			
P5.0/XIN	0	P5.0 (I/O)	I: 0; O: 1	0	Х	Х			
		XIN crystal mode ⁽²⁾	Х	1	Х	0			
		XIN bypass mode ⁽²⁾	Х	1	Х	1			
P5.1/XOUT	1	P5.1 (I/O)	I: 0; O: 1	0	Х	Х			
		XOUT crystal mode ⁽³⁾	Х	1	Х	0			
		P5.1 (I/O) ⁽³⁾	Х	1	Х	1			

Table 6-51. Port P5 (P5.0 and P5.1) Pin Functions

(1) X = don't care

(2) Setting P5SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.0 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.1 can be used as general-purpose I/O.

6.12.9 Port J, J.0 JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-11 shows the port schematic, and Table 6-52 summarizes selection of the pin function.



Figure 6-11. Port PJ (PJ.0) Schematic

6.12.10 Port J, J.1 to J.3 JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-12 shows the port schematic, and Table 6-52 summarizes selection of the pin function.



Figure 6-12. Port PJ (PJ.1 to PJ.3) Schematic

Table 6-52	. Port PJ	(PJ.0 to	PJ.3)	Pin Functions
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PIN NAME (PJ.x)		FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1
		TDO ⁽³⁾	Х
PJ.1/TDI/TCLK	1	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1
		TDI/TCLK ^{(3) (4)}	Х
PJ.2/TMS	2	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1
		TMS ⁽³⁾ ⁽⁴⁾	Х
PJ.3/TCK	3	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1
		TCK ⁽³⁾ ⁽⁴⁾	Х

(1) X = don't care

(2) Default condition

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(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.13 Device Descriptor Structures

Table 6-53 lists the content of the device descriptor tag-length-value (TLV) structure.

		-		
DE	SCRIPTION	ADDRESS	SIZE (bytes)	VALUE RF430F5978
	Info length	01A00h	1	06h
	CRC length	01A01h	1	06h
	CRC value	01A02h	2	per unit
Info Block	Device ID	01A04h	1	61h
	Device ID	01A05h	1	37h
	Hardware revision	01A06h	1	per unit
	Firmware revision	01A07h	1	per unit
	Die record tag	01A08h	1	08h
	Die record length	01A09h	1	0Ah
	Lot/wafer ID	01A0Ah	4	per unit
Die Record	Die X position	01A0Eh	2	per unit
	Die Y position	01A10h	2	per unit
	Test results	01A12h	2	per unit
	ADC12 calibration tag	01A14h	1	11h
	ADC12 calibration length	01A15h	1	10h
	ADC gain factor	01A16h	2	per unit
	ADC offset	01A18h	2	per unit
	ADC 1.5-V reference Temperature sensor 30°C	01A1Ah	2	per unit
ADC12 Calibration	ADC 1.5-V reference Temperature sensor 85°C	01A1Ch	2	per unit
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	2	per unit
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	2	per unit
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	2	per unit
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	2	per unit
	REF calibration tag	01A26h	1	12h
	REF calibration length	01A27h	1	06h
REF Calibration	1.5-V reference factor	01A28h	2	per unit
	2.0-V reference factor	01A2Ah	2	per unit
	2.5-V reference factor	01A2Ch	2	per unit
Peripheral Descriptor (PD)	Peripheral descriptor tag	01A2Eh	1	02h
	Peripheral descriptor length	01A2Fh	1	57h
	Peripheral descriptors	01A30h	PD Length	

Table 6-53. Device Descriptor Table



7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Circuit



For a complete reference design including layout, see the Sub-1-GHz Transceiver, LF Wake Receiver/Transponder SoC Evaluation Kit (RF430F5978EVM) and the *MSP430 Hardware Tools User's Guide* (SLAU278).

Figure 7-1. Typical Application Circuit RF430F5978

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Getting Started and Next Steps

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio[™] Integrated Development Environment (IDE).

The following products support development of the RF430F5978 device applications:

Software Development Tools: Code Composer Studio Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools.

Hardware Development Tools: For a complete listing of development-support tools for the RF430F5978 platform, visit the TI website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all RF430 MCU devices and support tools. Each commercial family member has one of three prefixes: RF, P, or X (for example, RF430F5978). TI recommends two of three possible prefix designators for its support tools: RF and X. These prefixes represent evolutionary stages of product development from engineering prototypes (with X for devices and tools) through fully qualified production devices and tools (with RF for devices tools).

Device development evolutionary flow:

X – Experimental device that is not necessarily representative of the electrical specifications of the final device

P – Silicon die that conforms to the electrical specifications of the final device but has not completed quality and reliability verification

RF – Fully qualified production device

Support tool development evolutionary flow:

X – Development-support product that has not yet completed TI's internal qualification testing.

RF - Fully-qualified development-support product

X and P devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

RF devices and RF development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X and P) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGC) and temperature range (for example, I). Figure 8-1 provides a legend for reading the complete device name for any family member.





Figure 8-1. Device Nomenclature

8.2 Documentation Support

8.2.1 Related Documentation

The following documents describe the RF430F5978 SoC. Copies of these documents are available on the Internet at www.ti.com.

SLAU378 *RF430 Family User's Guide.* Detailed descriptions of all of the modules available in this device family.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from TI and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.4 Trademarks

MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	()	()			(-)	(4)	(5)		(-)
RF430F5978IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	RF430F5978
RF430F5978IRGCR.B	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	RF430F5978

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All	dimensions	are	nominal	

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RF430F5978IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

4-Jul-2017



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RF430F5978IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0

RGC 64

9 x 9, 0.5 mm pitch

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.


RGC0064A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



RGC0064A

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



RGC0064A

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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