SN74CB3Q3257 4 ビット、1:2 FET マルチプレクサ / デマルチプレクサ、2.5V/3.3V 低電圧高帯域バス スイッチ

1 特長

- 高帯域幅のデータ パス (最高最大 500MHz)
- デバイスの電源オン時とオフ時の両方で 5V 許容の I/O
- 動作範囲全体にわたって小さく平坦なオン抵抗 (r_{on}) 特性 (標準値 r_{on} = 4Ω)
- データ I/O ポートのレール ツー レール スイッチング
  - V_{CC} = 3.3V で 0～5V のスイッチング
  - V_{CC} = 2.5V で 0～3.3V のスイッチング
- 伝播遅延がゼロに近い双方向データ フロー
- 低い入力および出力容量により負荷および信号歪みが最小化 (標準値 $C_{io(OFF)}$ = 3.5pF)
- 高いスイッチング周波数 (最大値 $f_{\overline{OE}}$ = 20MHz)
- データおよび制御入力にアンダーシュート クランプ ダイオードを搭載
- 低消費電力 (I_{CC} = 0.7mA、標準値)
- 2.3V～3.6V の範囲の V_{CC} で動作
- データ I/O は 0～5V の信号レベルに対応 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
- 制御入力は、TTL または 5V および 3.3V CMOS 出力で駆動可能
- I_{off} により部分的パワーダウン モード動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- ESD 性能は JESD 22 に準拠しテスト済み
  - 人体モデルで 2000V (A114-B、クラス II)
  - 荷電デバイス モデルで 1000V (C101)
- デジタルとアナログの両方のアプリケーションに対応: USB インターフェイス、差動信号インターフェイス、バス絶縁、低歪み信号ゲーティング [1]

2 アプリケーション

- IP 電話: 有線および無線
- 光学モジュール
- 光ネットワーク: Video Over Fiber および EPON
- 構内交換機 (PBX)
- WiMAX およびワイヤレス インフラストラクチャ機器

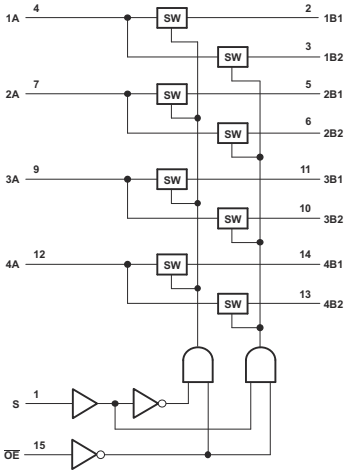
3 概要

SN74CB3Q3257 デバイスは高帯域の FET バス スイッチで、チャージ ポンプを使用してパス トランジスタのゲート電圧を上昇させ、低い平坦なオン抵抗 (r_{on}) を実現します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN74CB3Q3257	TVSOP (DGV) (16)	3.6mm × 6.4mm
	SSOP (DBQ) (16)	4.9mm × 6mm
	TSSOP (PW、16)	5mm × 6.4mm
	VQFN (RGV、16)	4mm × 3.5mm

(1) 詳細については、セクション 9 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

[1] CB3Q ファミリの性能特性の詳細については、TI のアプリケーション レポート『CBT-C、CB3T、および CB3Q シグナル スイッチ ファミリ』を参照してください。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 Recommended Operating Conditions ... 4
5.4 Thermal Information ... 5
5.5 Electrical Characteristics ... 5
5.6 Switching Characteristics, V_{CC} = 2.5V ... 6
5.7 Switching Characteristics, V_{CC} = 3.3V ... 6
5.8 Typical Characteristics ... 6
6 Detailed Description ... 8
6.1 Overview ... 8
6.2 Functional Block Diagram ... 9
6.3 Feature Description ... 9
6.4 Device Functional Modes ... 9
7 Device and Documentation Support ... 12
7.1 Documentation Support ... 12
7.2 Receiving Notification of Documentation Updates ... 12
7.3 サポート・リソース ... 12
7.4 Trademarks ... 12
7.5 静電気放電に関する注意事項 ... 12
7.6 用語集 ... 12
8 Revision History ... 12
9 Mechanical, Packaging, and Orderable Information ... 13

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

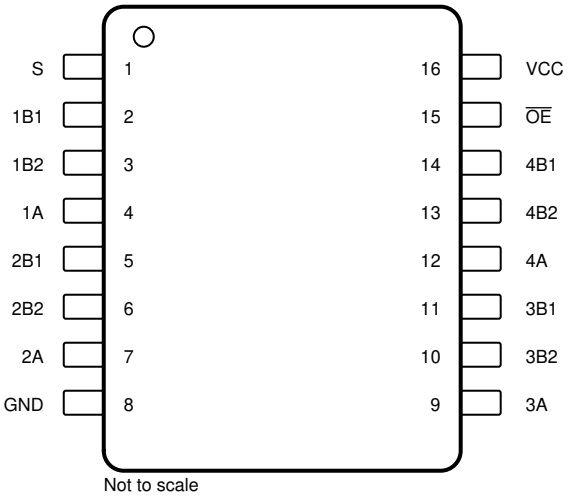


図 4-1. D, DB, DGV, DBQ, or PW Package 16-Pin SOIC, SSOP TVSOP, or TSSOP (Top View)

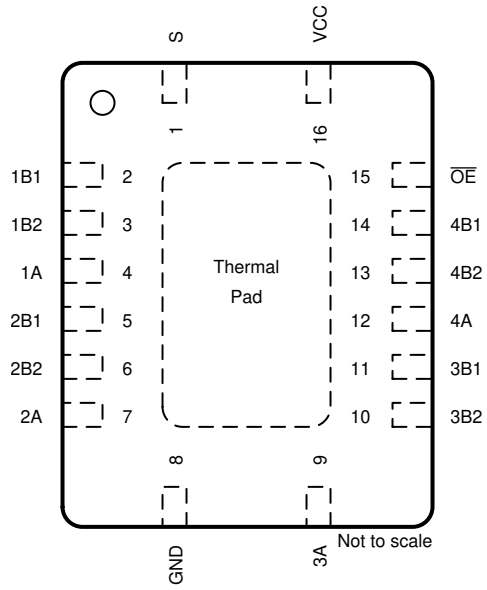


図 4-2. RGY Package, 16-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
S	1	I	Select Pin
1B1	2	I/O	Channel 1 I/O 1
1B2	3	I/O	Channel 1 I/O 2
1A	4	I/O	Channel 1 common
2B1	5	I/O	Channel 2 I/O 1
2B2	6	I/O	Channel 2 I/O 2
2A	7	I/O	Channel 2 common
GND	8	—	Ground
3A	9	I/O	Channel 3 common
3B2	10	I/O	Channel 3 I/O 2
3B1	11	I/O	Channel 3 I/O 1
4A	12	I/O	Channel 4 common
4B2	13	I/O	Channel 4 I/O 2
4B1	14	I/O	Channel 4 I/O 1
$\overline{OE}$	15	I	Output Enable (Active Low)
V_{CC}	16	—	Power

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
I_{IO}	ON-state switch current			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	105	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Copyright © 2024 Texas Instruments Incorporated

5.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3257				UNIT
		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.3	126.0	112.7	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.4	51.3	47.5	61.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	57.8	57.8	25.9	
ψ_{JT}	Junction-to-top characterization parameter	18.3	5.9	6.0	2.3	
ψ_{JB}	Junction-to-board characterization parameter	56.4	57.3	57.3	26.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	11.4	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

T_A = –40°C to 105°C. Typical values stated are over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V, I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF V_{IN} = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0				1	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND			0.7	1.5	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6 V, One input at 3 V, Other inputs at V_{CC} or GND				30	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle			0.3	0.35	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			5.5	7	pF
	B port	V_{CC} = 3.3 V, Switch OFF, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			3.5	5	pF
$C_{io(ON)}$	A port	V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 5.5 V, 3.3 V, or 0			10.5	13	pF
	B port				10.5	13	
r_{on} [6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0, I_O = 30 mA		4	8	Ω
			V_I = 1.7 V, I_O = –15 mA		4	9	
		V_{CC} = 3 V	V_I = 0, I_O = 30 mA		4	6	
			V_I = 2.4 V, I_O = –15 mA		4	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data terminals.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see 図 5-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Copyright © 2024 Texas Instruments Incorporated

5.6 Switching Characteristics, V_{CC} = 2.5V

Typical values stated are over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V			UNIT
			MIN	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10	10	MHz
t_{pd} (2)	A or B	B or A		0.12	0.21	ns
$t_{pd(s)}$	S	A	1.5	6.5	7.5	ns
t_{en}	S	B	1.5	6.5	7.5	ns
	$\overline{OE}$	A or B	1.5	6.5	7.5	
t_{dis}	S	B	1	6	7	ns
	$\overline{OE}$	A or B	1	6	7	

(1) Maximum switching frequency for control inputs ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

5.7 Switching Characteristics, V_{CC} = 3.3V

Typical values stated are over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3V ± 0.3V				UNIT
			MIN	TYP(1)	MAX (85°C)	MAX (105°C)	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B			20	20	MHz
t_{pd} (2)	A or B	B or A			0.2	0.32	ns
$t_{pd(s)}$	S	A	1.5	4.1	5.5	6.5	ns
t_{en}	S	B	1.5	4.6	5.5	6.5	ns
	$\overline{OE}$	A or B	1.5	4.7	5.5	6.5	
t_{dis}	S	B	1	3.3	6	7	ns
	$\overline{OE}$	A or B	1	3.1	6	7	

(1) TYP taken from average in 105°C

5.8 Typical Characteristics

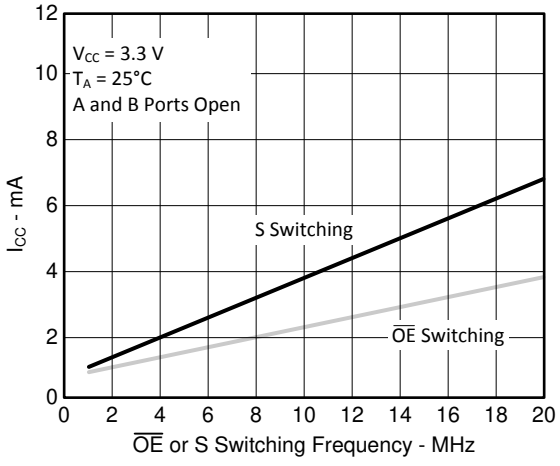


図 5-1. Typical r_{on} vs V_I

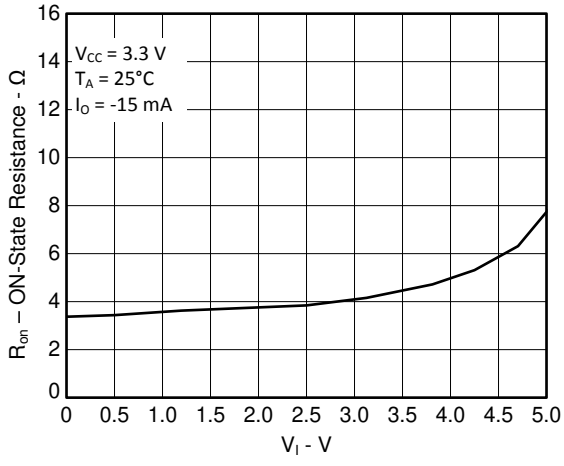
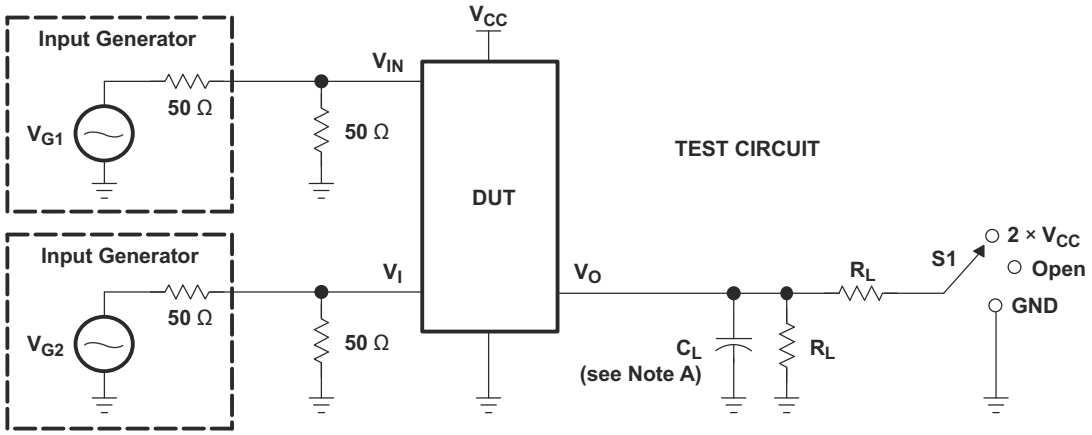


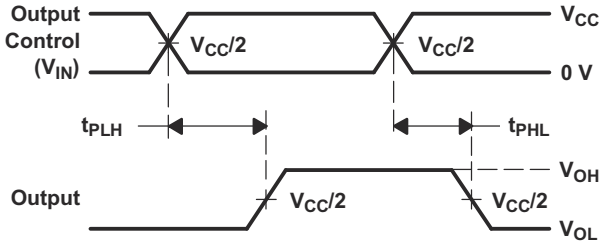
図 5-2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency

Copyright © 2024 Texas Instruments Incorporated

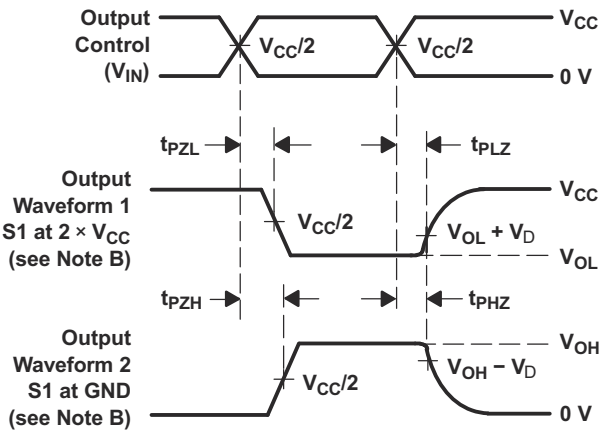
Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

Copyright © 2024 Texas Instruments Incorporated

6 Detailed Description

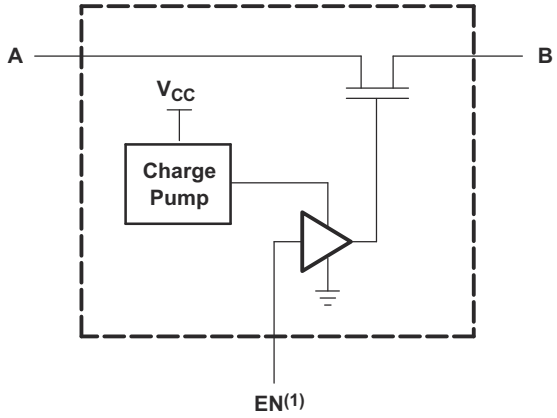
6.1 Overview

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable (1 $\overline{OE}$, 2 $\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

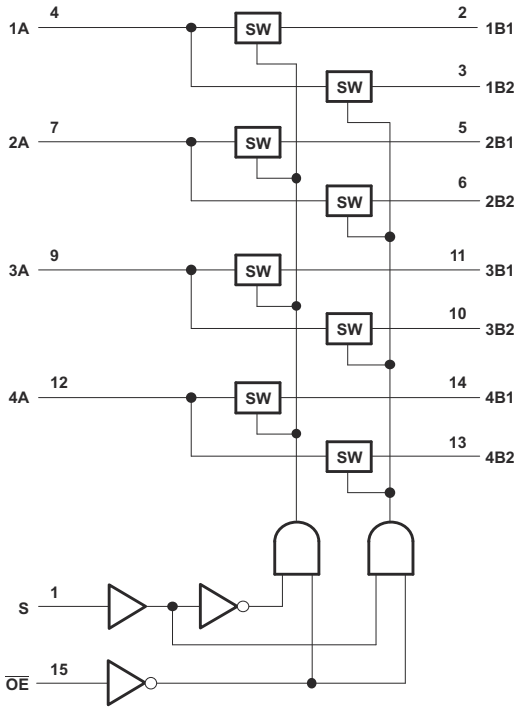


(1) EN is the internal enable signal applied to the switch.

図 6-1. Simplified Schematic, Each FET Switch (SW)

Copyright © 2024 Texas Instruments Incorporated

6.2 Functional Block Diagram



6.3 Feature Description

The SN74CB3Q3257 device has a high-bandwidth data path (up to 500 MHz) and has 5V tolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4Ω Typical).

This device also has rail-to-rail switching on data I/O ports for 0- to 5V switching with 3.3-V V_{CC} and 0- to 3.3V switching with 2.5V V_{CC} as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5pF Typical).

The SN74CB3Q3257 also provides a fast switching frequency ($f_{\overline{OE}}$ = 20MHz Max) with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC} = 0.6mA Typical).

The V_{CC} operating range is from 2.3V to 3.6V and the data I/Os support 0 to 5V signal levels of (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V).

The control inputs can be driven by TTL or 5V / 3.3V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation.

6.4 Device Functional Modes

表 6-1 lists the functional modes of the SN74CB3Q3257.

表 6-1. Function Table

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

Copyright © 2024 Texas Instruments Incorporated

Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The SN74CB3Q3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices. the $\overline{OE}$ and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

2 Typical Application

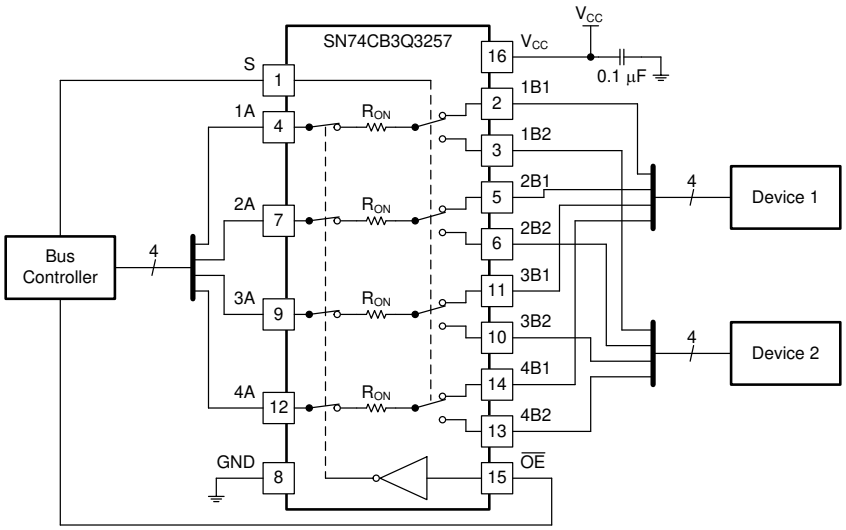


図 7-1. Typical Application of the SN74CB3Q3257

2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *セクション 5.3*.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed ±128mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 500MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in *セクション 7.3*.

2.2 Detailed Design Procedure

The 0.1µF capacitor should be place as close as possible to the device.

Copyright © 2024 Texas Instruments Incorporated

2.3 Application Curve

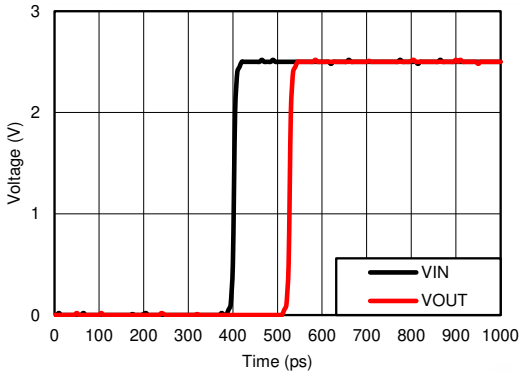


図 7-2. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5V.

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *セクション 5.1* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

3 Layout

3.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 7-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

3.2 Layout Example

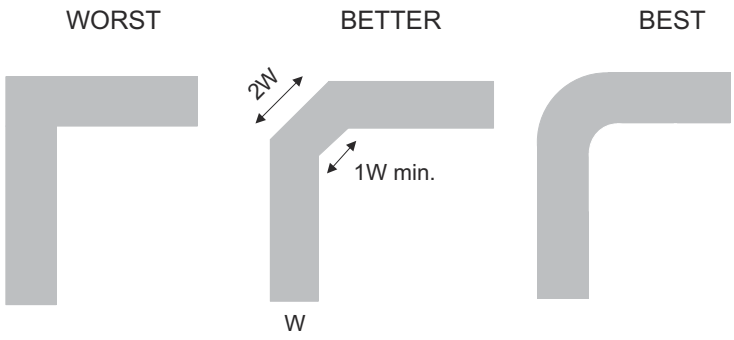


図 7-3. Trace Example

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch*

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

7.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

7.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

7.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

Changes from Revision D (July 2018) to Revision E (December 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• Changed the T_A MAX value from 85°C to 105°C in the *Recommended Operating Conditions*	4

Changes from Revision C (April 2017) to Revision D (July 2018)	Page
• Changed the pinout images appearance	3
• Added *Thermal Information* table values	5

Changes from Revision B (June 2015) to Revision C (April 2017)	Page
• Added MAX values for T_A = –40°C to 105°C to the *Electrical Characteristics* table	5
• Added MAX values for T_A = –40°C to 105°C to the *Switching Characteristics, V_{CC} = 2.5 V* table.	5

Copyright © 2024 Texas Instruments Incorporated

- Added separate *Switching Characteristics, V_{CC} = 3.3V* for V_{CC} = 3.3V ± 0.3V. Added TYP values and MAX values for T_A = –40°C to 105°C.....6

Changes from Revision A (November 2003) to Revision B (June 2015) **Page**

- 「注文情報」表を削除。 1
- 「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3Q3257DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	BU257
SN74CB3Q3257PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

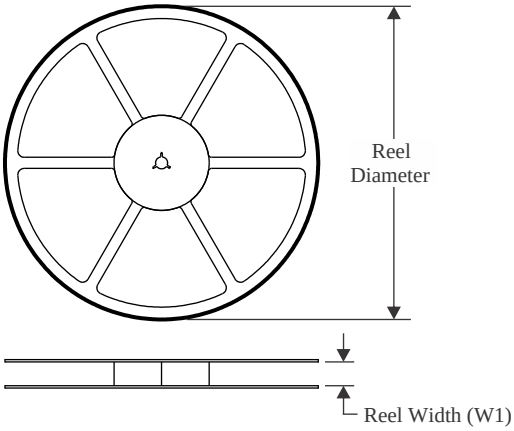
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

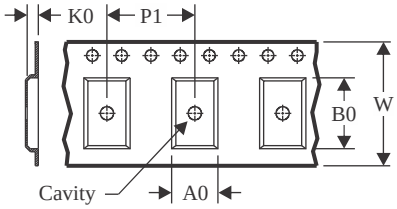
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

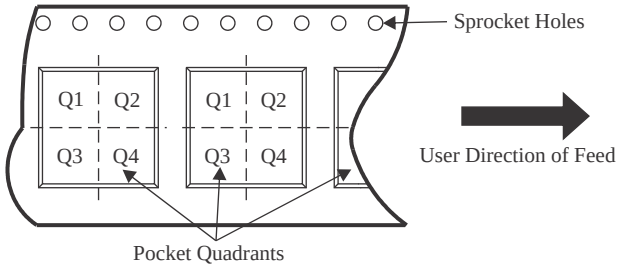


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

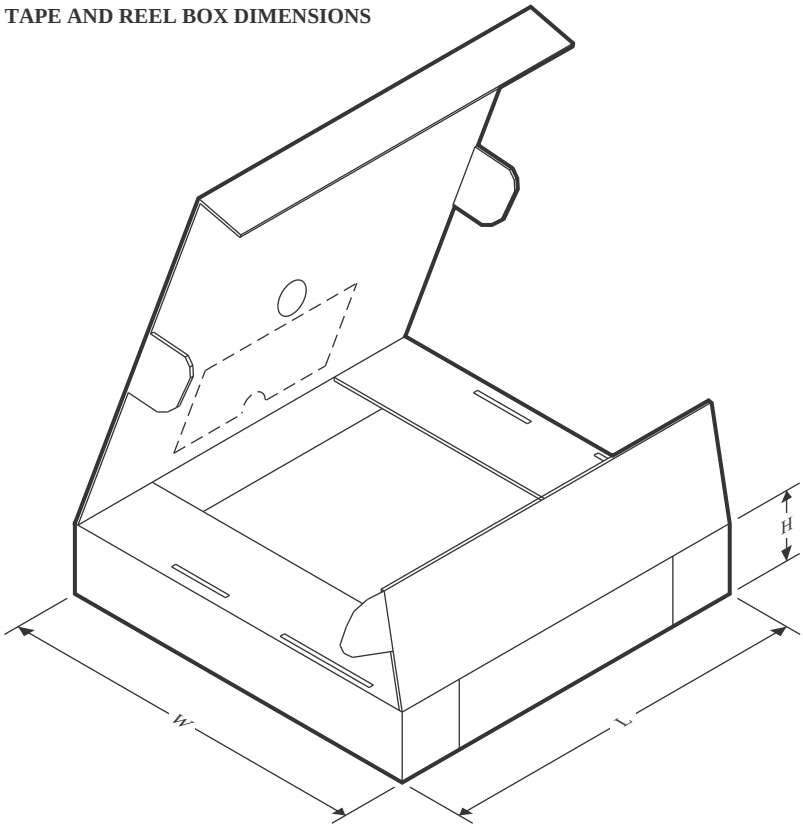
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

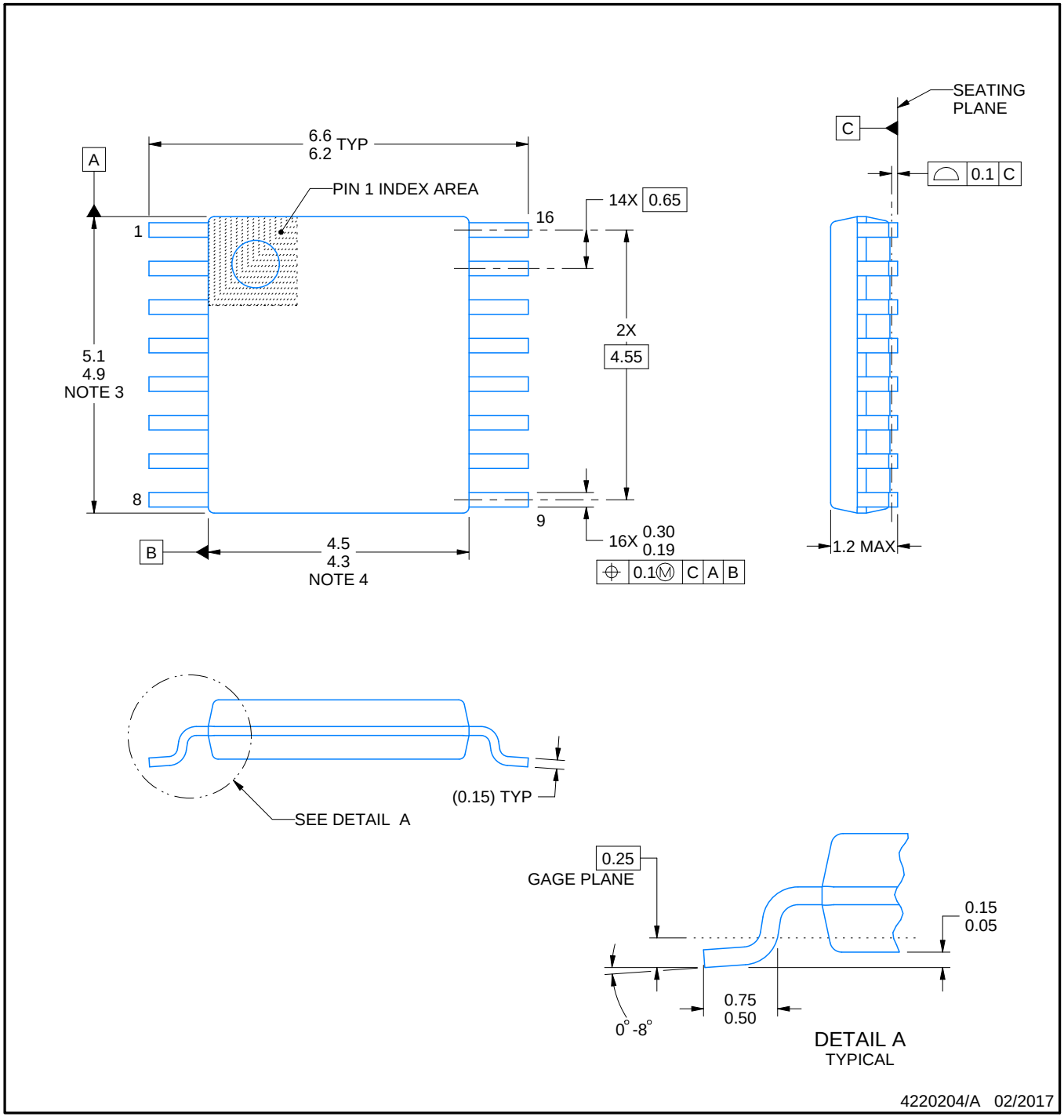
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

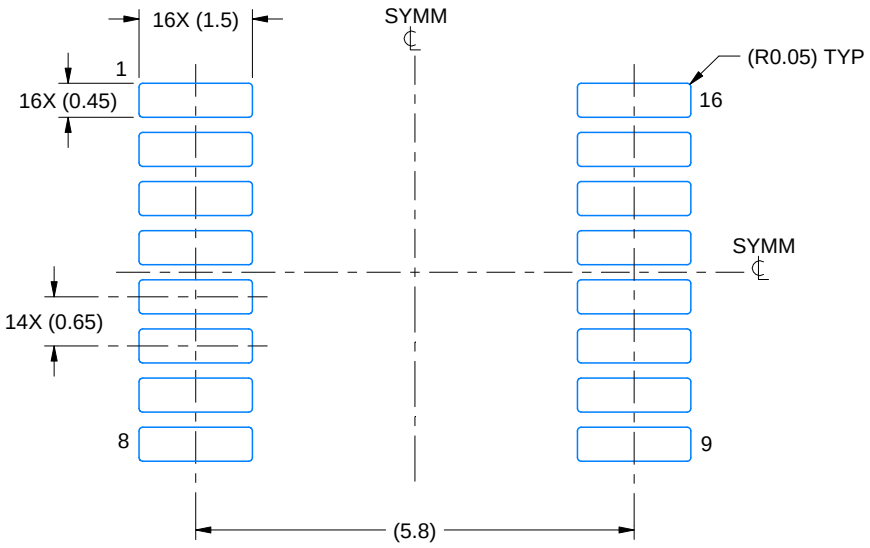
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



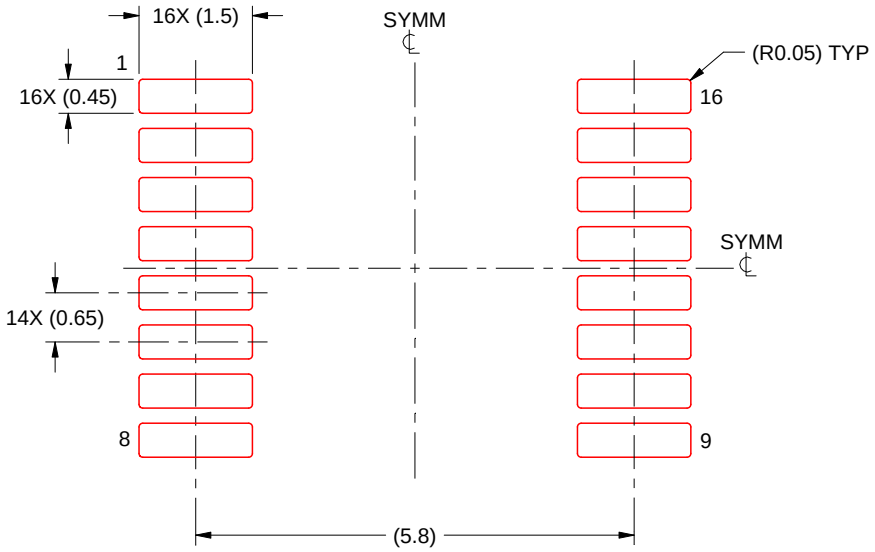
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

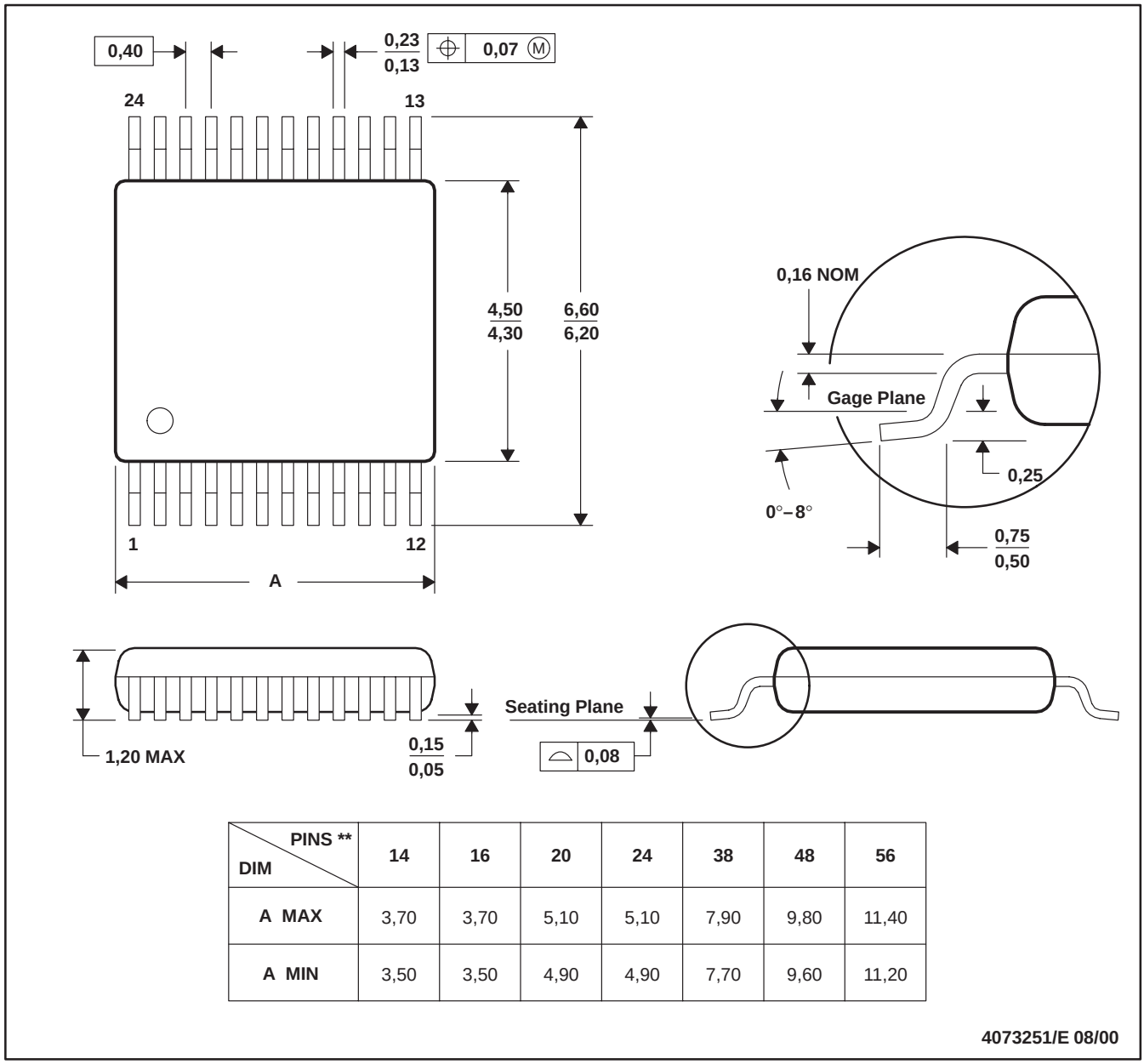
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

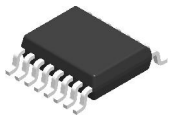
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

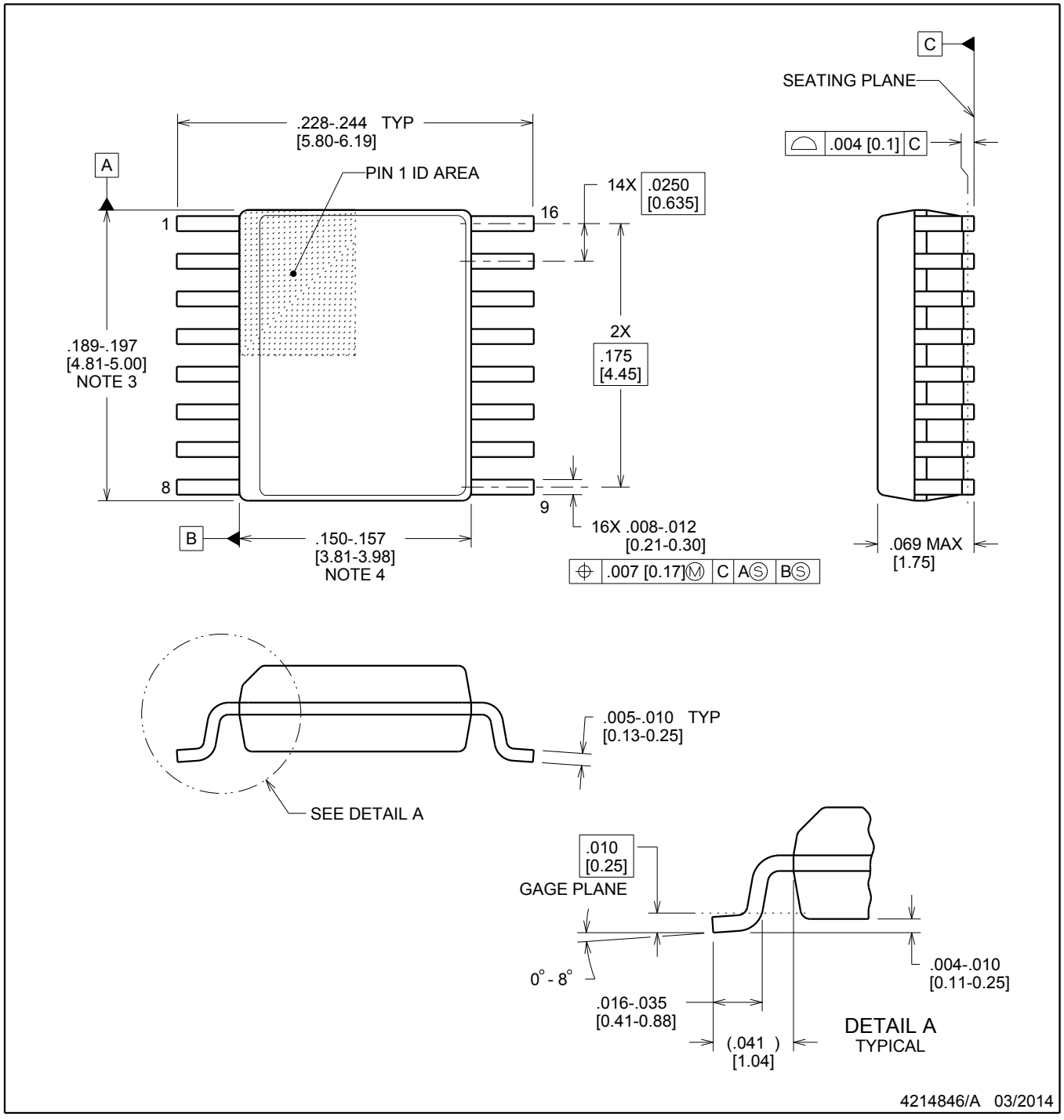


PACKAGE OUTLINE

DBQ0016A

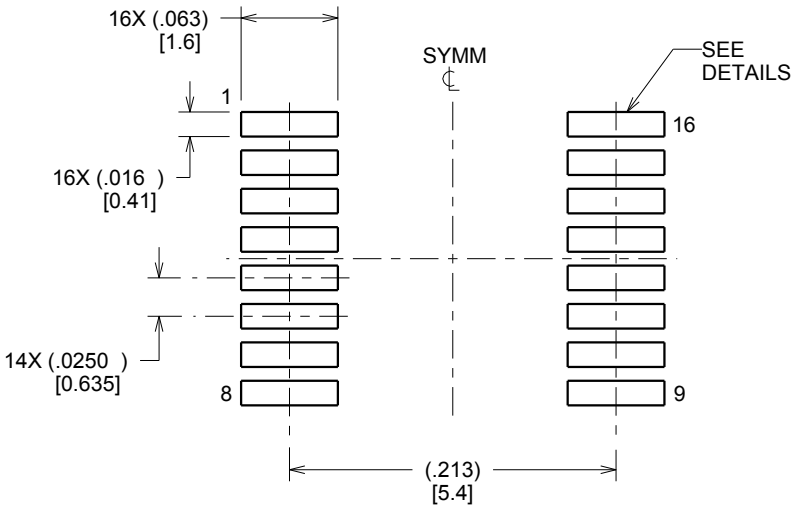
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

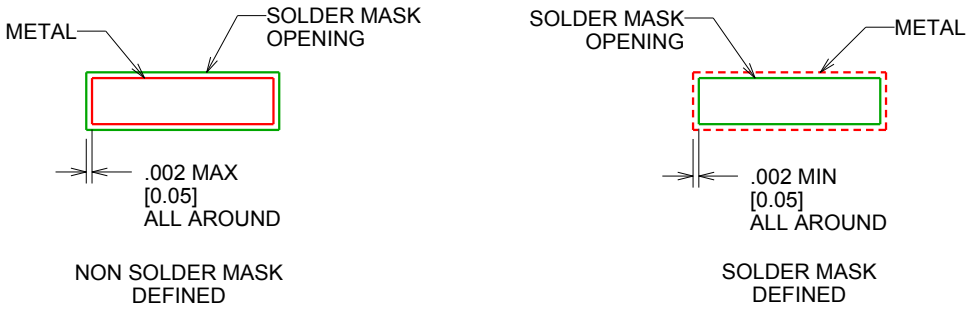


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

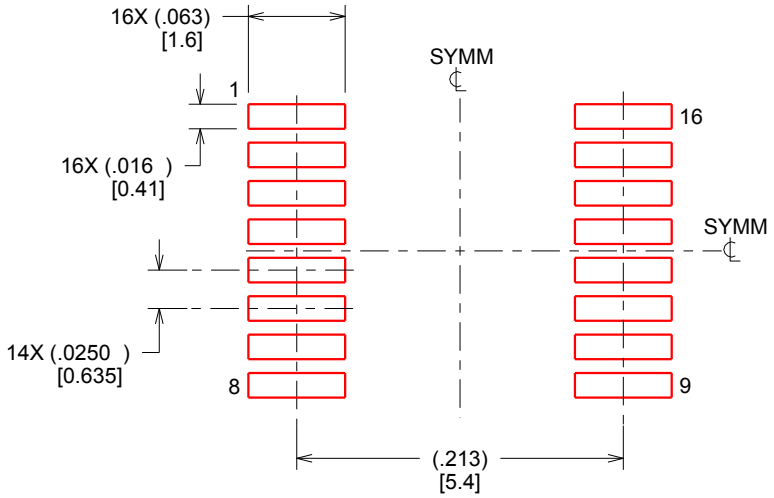
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



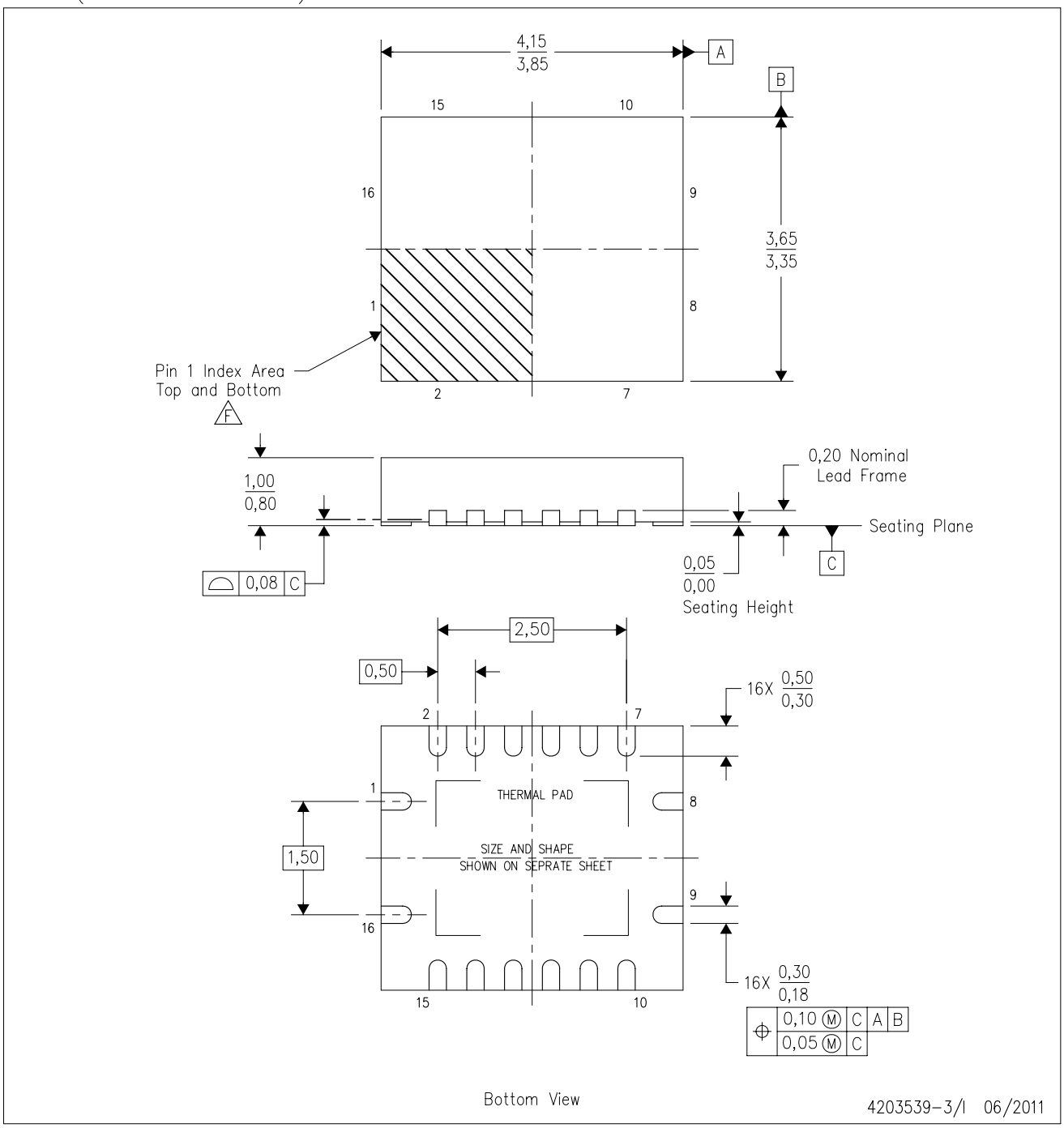
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

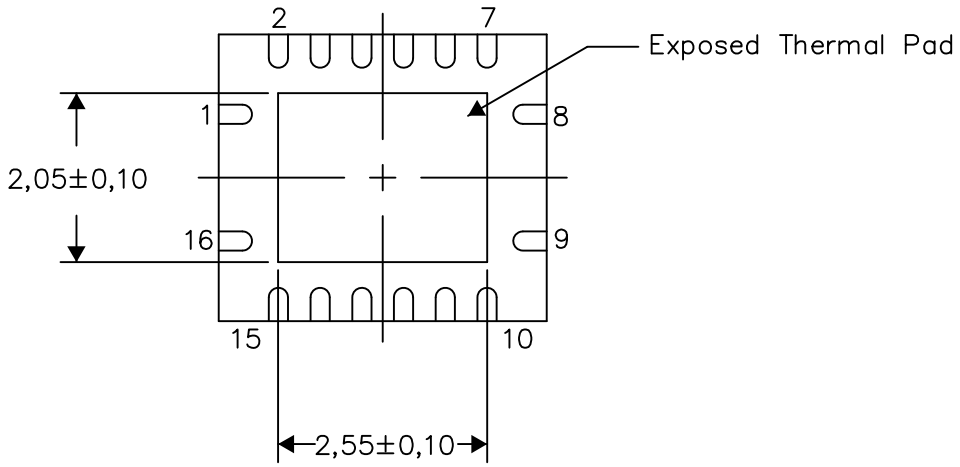
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



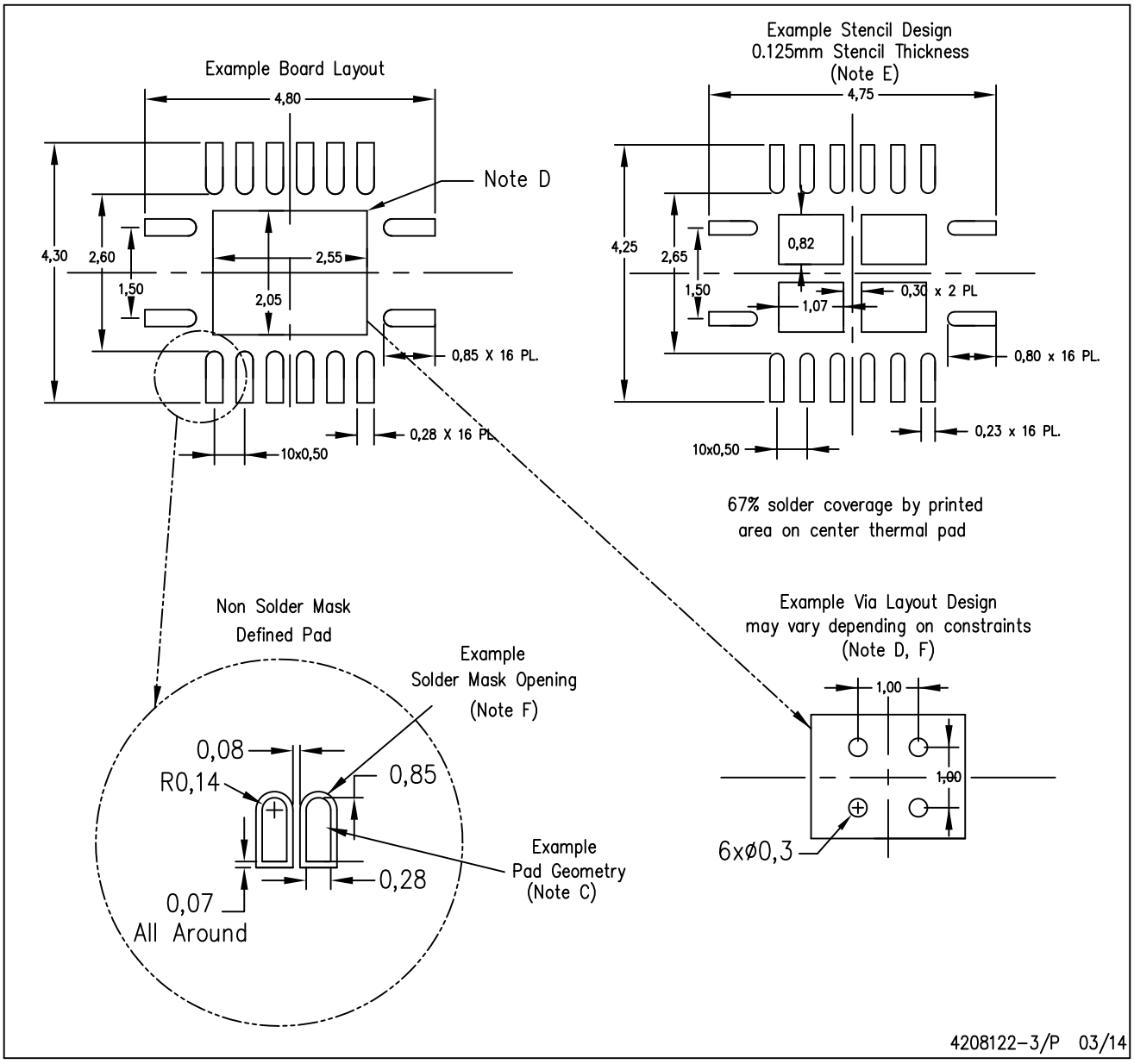
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated