TAS6424-Q1 75W、2MHzデジタル入力、4チャネル車載用Class-Dオーディオ・アンプ、負荷ダンプ保護およびI²C診断機能搭載

1 特長

- **高度な負荷診断**
  - 入力クロックなしで動作
  - AC診断による、インピーダンスおよびフェーズ応答を含むツイータ検出
- CISPR25-L5 EMC仕様へ簡単に適合
- **車載アプリケーションに認定済み**
- **オーディオ入力**
  - 4チャネルのI²Sまたは4/8チャネルのTDM入力
  - 入力サンプル・レート: 44.1kHz、48kHz、96kHz
  - 入力フォーマット: 16ビットから32ビットのI²SおよびTDM
- **オーディオ出力**
  - 4チャネルのBTL (Bridge-Tied Load)、並列BTL (PBTL)のオプションあり
  - 最大2.1MHzの出力スイッチング周波数
  - 75W、10% THD (4Ω、25V)
  - 45W、10% THD (2Ω、14.4V)
  - 150W、10% THD (2Ω、25V PBTL)
- **14.4V、4Ω負荷でのオーディオ性能**
  - 1WでTHD+N < 0.03%
  - 出力ノイズ: 42μV_{RMS}
  - クロストーク: –90dB
- **負荷診断**
  - 出力開路および負荷短絡
  - 出力からバッテリまたはグランドへの短絡
  - 最大6kΩのライン出力検出
  - ホストと独立の動作
  - プログラム可能なため柔軟な生産ラインのテストが可能
- **保護**
  - 出力電流制限
  - 出力短絡保護
  - 40Vの負荷ダンプ
  - グランド開路と電力許容
  - DCオフセット
  - 過熱
  - 低電圧および過電圧
- **一般的な動作**
  - 4.5V～26.4Vの電源電圧
  - 4つのアドレス・オプションを持つI²C制御
  - クリップ検出およびサーマル警告

2 アプリケーション

- **車載用ヘッド・ユニット**
- **車載用外部アンプ・モジュール**

3 概要

TAS6424-Q1デバイスは、4チャネルのデジタル入力、Class-Dオーディオ・アンプで、2.1MHzのPWMスイッチング周波数が実装されているため、非常に小さなサイズのPCBでコスト最適化されたソリューションを実現可能です。開始/停止イベントについて最低4.5Vで完全な動作を行い、最高40kHzのオーディオ帯域幅で非常に優れた音質を提供します。

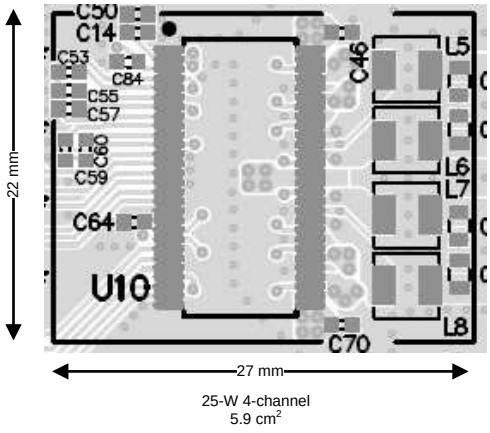
TAS6424-Q1 Class-Dオーディオ・アンプは、車載用ヘッドユニット、および外部アンプ・モジュールで使用するよう設計されています。このデバイスには4つのチャネルがあり、14.4V電源から4Ω負荷へ10% THD+Nで27Wを、2Ω負荷へ10% THD+Nで45Wを、25V電源から4Ω負荷へ10% THD+Nで75Wを供給できます。Class-Dトポロジにより、従来のリニア・アンプ・ソリューションと比較して劇的に効率が向上しています。出力スイッチング周波数をAMバンドよりも高く設定すると、AMバンドの干渉を排除し、出力フィルタのサイズとコストを削減できます。また、AMバンドよりも低く設定すれば、効率を最適化できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TAS6424-Q1	HSSOP (56)	18.41mm×7.49mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

PCB領域



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (October 2016) から Revision B に変更 **Page**

- プロダクト・フォルダが見やすくなるよう「*特長*」および「*概要*」セクションを 変更 ... 3

2016年9月発行のものから更新 **Page**

- データシートの完全版をリリース ... 3

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5 概要（続き）

ピン互換の2チャネルのアンプについては、TAS6422-Q1を参照してください。

このデバイスは、56ピンのHSSOP PowerPAD™パッケージで、サーマル・パッドが上面に露出した形態で供給されます。

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6 Device Comparison Table

PART NUMBER	INPUT TYPE	CHANNEL COUNT	POWER-SUPPLY VOLTAGE RANGE	OUTPUT CURRENT LIMIT	MAXIMUM PWM FREQUENCY
TAS6424-Q1	Digital	4	4.5 V to 26.4 V	6.5 A	2.1 MHz
TAS5414C-Q1	Analog, Single-Ended	4	5.6 V to 24 V	12.7 A	500 kHz
TAS5424C-Q1	Analog, Differential	4	5.6 v to 24 V	12.7 A	500 kHz

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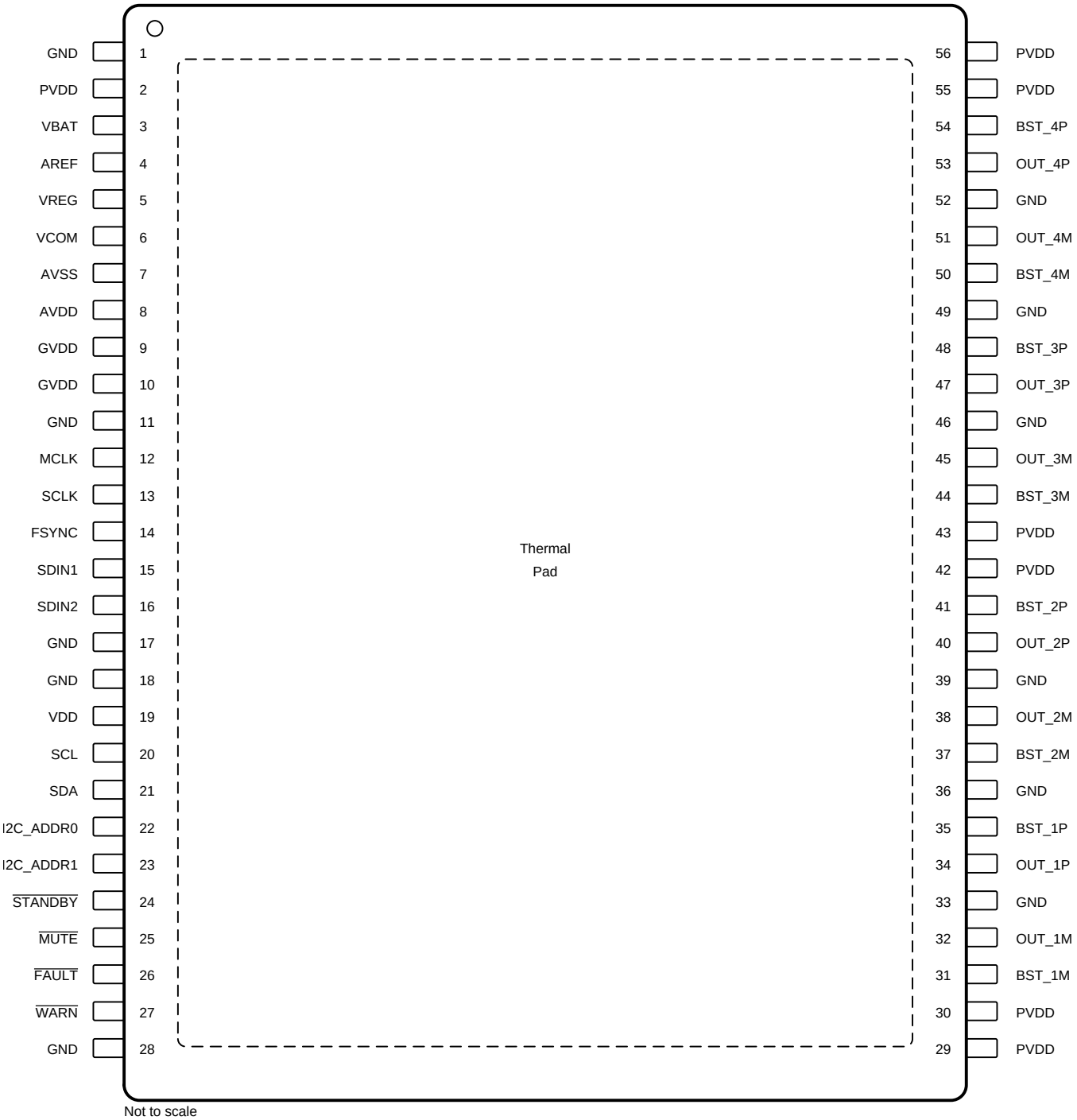
7 Pin Configuration and Functions

DKQ Package
56-Pin HSSOP With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AREF	4	PWR	VREG and VCOM bypass capacitor return
AVDD	8	PWR	Voltage regulator bypass
AVSS	7	PWR	AVDD bypass capacitor return
BST_1M	31	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_1P	35	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2M	37	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2P	41	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3M	44	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3P	48	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_4M	50	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_4P	54	PWR	Bootstrap capacitor connection pins for high-side gate driver
$\overline{\text{FAULT}}$	26	DO	Reports a fault (active low, open drain), 100-kΩ internal pullup resistor
FSYNC	14	DI	Audio frame clock input
GND	1	GND	Ground
	11		
	17		
	18		
	28		
	33		
	36		
	39		
	46		
	49		
	52		
GVDD	9	PWR	Gate drive voltage regulator for channel 3 and 4, derived from VBAT input pin.
	10		Gate drive voltage regulator for channel 1 and 2, derived from VBAT input pin.
I2C_ADDR0	22	DI	I^2C address pins
I2C_ADDR1	23		
MCLK	12	DI	Audio master clock input
$\overline{\text{MUTE}}$	25	DI	Mutes the device outputs (active low), 100-kΩ internal pulldown resistor
OUT_1M	32	NO	Negative output for the channel
OUT_1P	34	PO	Positive output for the channel
OUT_2M	38	NO	Negative output for the channel
OUT_2P	40	PO	Positive output for the channel
OUT_3M	45	NO	Negative output for the channel
OUT_3P	47	PO	Positive output for the channel
OUT_4M	51	NO	Negative output for the channel
OUT_4P	53	PO	Positive output for the channel
PVDD	2	PWR	PVDD voltage input (can be connected to battery)
	29		
	30		
	42		
	43		
	55		
	56		

(1) GND = ground, PWR = power, PO = positive output, NO = negative output, DI = digital input, DO = digital output, DI/O = digital input and output, NC = no connection

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SCL	20	DI	I^2C clock input
SCLK	13	DI	Audio bit and serial clock input
SDA	21	DI/O	I^2C data input and output
SDIN1	15	DI	TDM data input and audio I^2S data input for channels 1 and 2
SDIN2	16	DI	Audio I^2S data input for channels 3 and 4
$\overline{\text{STANDBY}}$	24	DI	Enables low power standby state (active Low), 100-kΩ internal pulldown resistor
VBAT	3	PWR	Battery voltage input
VCOM	6	PWR	Bias voltage
VDD	19	PWR	3.3-V external supply voltage
VREG	5	PWR	Voltage regulator bypass
$\overline{\text{WARN}}$	27	DO	Clip and overtemperature warning (active low, open drain), 100-kΩ internal pullup resistor
Thermal Pad	—	GND	Provides both electrical and thermal connection for the device. Heatsink must be connected to GND.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
PVDD, VBAT	DC supply voltage relative to GND		–0.3	30	V
V_{MAX}	Transient supply voltage: PVDD, VBAT	t ≤ 400 ms exposure	–1	40	V
V_{RAMP}	Supply-voltage ramp rate: PVDD, VBAT			75	V/ms
VDD	DC supply voltage relative to GND		–0.3	3.5	V
I_{MAX}	Maximum current per pin (PVDD, VBAT, OUT_xP, OUT_xM, GND)			8	A
I_{MAX_PULSED}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		12	A
V_{LOGIC}	Input voltage for logic pins (SCL, SDA, SDIN1, SDIN2, MCLK, BCLK, LRCLK, MUTE, $\overline{\text{STANDBY}}$, I2C_ADDRx)		–0.3	VDD + 0.5	V
V_{GND}	Maximum voltage between GND pins		–0.3	0.3	V
T_J	Maximum operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100–002(1)		±3000	V
		Charged-device model (CDM), per AEC Q100–011	All pins	±500	
			Corner pins (1, 28, 29 and 56)	±1000	

(1) AEC Q100–002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS–001 specification.

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8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
PVDD	Output FET supply voltage	Relative to GND	4.5		26.4	V
VBAT	Battery supply voltage input	Relative to GND	4.5	14.4	18	V
VDD	DC logic supply	Relative to GND	3.0	3.3	3.5	V
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature	An adequate thermal design is required	–40		150	°C
R_L	Nominal speaker load impedance	BTL Mode	2	4		Ω
		PBTL Mode	1	2		
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
C_{Bypass}	External capacitance on bypass pins	Pin 2, 3, 5, 6, 8, 9, 10, 19		1		µF
C_{OUT}	External capacitance to GND on OUT pins	Limit set by DC-diagnostic timing		1	3.3	µF
L_O	Output filter inductance	Minimum inductance at I_{SD} current levels	1			µH

8.4 Thermal Information

THERMAL METRIC(1)		TAS6424-Q1(2) DKQ (HSSOP) 56 PINS	TAS6424-Q1(3) DKQ (HSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) JEDEC Standard 4 Layer PCB.
(3) Measured using the TAS6424-Q1 EVM layout and heat sink. The device is not intended to be used without a heat sink.

8.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f = 1 kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings, see 図 79 and 図 82

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All channels playing, no audio input		75	90	mA
I_{VBAT_IDLE}	VBAT idle current	All channels playing, no audio input		90	100	mA
I_{PVDD_STBY}	PVDD standby current	$\overline{STANDBY}$ Active, VDD = 0 V		1	10	µA
I_{VBAT_STBY}	VBAT standby current	$\overline{STANDBY}$ Active, VDD = 0 V		4	10	µA
I_{VDD}	VDD supply current	All channels playing, –60-dB signal		15	18	mA
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	20	22		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	25	27		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	38	40		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	42	45		
		4 Ω, PVDD = 25 V, THD+N = 1%, T_C = 75°C	50	55		
		4 Ω, PVDD = 25 V, THD+N = 10%, T_C = 75°C	70	75		
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	35	40		W
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	45	50		
		1 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	72	80		
		1 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	80	90		
		2 Ω, PVDD = 25 V, THD+N = 1%, T_C = 75°C	98	120		
		2 Ω, PVDD = 25 V, THD+N = 10%, T_C = 75°C	138	150		

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Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f = 1 kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings, see 図 79 and 図 82

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EFF_P	Power efficiency	4 channels operating, 25-W output power/ch 4-Ω load, PVDD = 14.4 V, T_C = 25°C, including indcutor losses(1)		86%		
AUDIO PERFORMANCE						
V_n	Output noise voltage	Zero input, A-weighting, gain level 1, PVDD = 14.4 V		42		μV
		Zero input, A-weighting, gain level 2, PVDD = 14.4 V		55		
		Zero input, A-weighting, gain level 3, PVDD = 18 V		67		
		Zero input, A-weighting, gain level 4, PVDD = 25 V		85		
GAIN	Peak output voltage/dBFS	Gain level 1, Register 0x01, bit 1-0 = 00		7.5		V/FS
		Gain level 2, Register 0x01, bit 1-0 = 01		15		
		Gain level 3, Register 0x01, bit 1-0 = 10		21		
		Gain level 4, Register 0x01, bit 1-0 = 11		29		
Crosstalk	Channel crosstalk	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		–90	–75	dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		75		dB
THD+N	Total harmonic distortion + noise			0.02%	0.05 %	
G_{CH}	Channel-to-channel gain variation		–0.5	0	0.5	dB
LINE OUTPUT PERFORMANCE						
$V_{n_LINEOUT}$	LINE output noise voltage	Zero input, A-weighting, channel set to LINE MODE		42		μV
$V_{O_LINEOUT}$	LINE output voltage	0-dB input, channel set to LINE MODE		5.5		V_{RMS}
THD+N	Line output total harmonic distortion + noise	V_O = 2 V_{RMS} , channel set to LINE MODE		0.01%	0.03 %	
DIGITAL INPUT PINS						
V_{IH}	Input logic level high		70			%VDD
V_{IL}	Input logic level low				30	%VDD
I_{IH}	Input logic current, high	V_I = VDD			15	μA
I_{IL}	Input logic current, low	V_I = 0			–15	μA
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	Not including bond wire and package resistance		90		mΩ
OVERVOLTAGE (OV) PROTECTION						
V_{PVDD_OV}	PVDD overvoltage shutdown		27.0	27.8	28.8	V
$V_{PVDD_OV_HYS}$	PVDD overvoltage shutdown hysteresis			0.8		V
V_{VBAT_OV}	VBAT overvoltage shutdown		19.3	20	22	V
$V_{VBAT_OV_HYS}$	VBAT overvoltage shutdown hysteresis			0.6		V
UNDERVOLTAGE (UV) PROTECTION						
$VBAT_{UV}$	VBAT undervoltage shutdown			4	4.5	V
$VBAT_{UV_HYS}$	VBAT undervoltage shutdown hysteresis			0.2		V
$PVDD_{UV}$	PVDD undervoltage shutdown			4	4.5	V
$PVDD_{UV_HYS}$	PVDD undervoltage shutdown hysteresis			0.2		V
BYPASS VOLTAGES						
V_{GVDD}	Gate drive bypass pin voltage			7		V
V_{AVDD}	Analog bypass pin voltage			6		V
V_{VCOM}	Common bypass pin voltage			2.5		V
V_{VREG}	Regulator bypass pin voltage			5.5		V
POWER-ON RESET (POR)						
V_{POR}	VDD voltage for POR			2.1	2.7	V
V_{POR_HY}	VDD POR recovery hysteresis voltage			0.5		V
OVERTEMPERATURE (OT) PROTECTION						
OTW(i)	Channel overtemperature warning			150		°C

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Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f = 1 kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings, see 図 79 and 図 82

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTSD(i)	Channel overtemperature shutdown			175		°C
OTW	Global junction overtemperature warning	Set by register 0x01 bit 5-6, default value		130		°C
OTSD	Global junction overtemperature shutdown			160		°C
OT_{HYS}	Overtemperature hysteresis			15		°C
LOAD OVER CURRENT PROTECTION						
I_{LIM}	Overcurrent cycle-by-cycle limit	OC Level 1	4	4.8		A
		OC Level 2	6	6.5		
I_{SD}	Overcurrent shutdown	OC Level 1, Any short to supply, ground, or other channels		7		A
		OC Level 2, Any short to supply, ground, or other channels		9		
MUTE MODE						
G_{MUTE}	Output attenuation			100		dB
CLICK AND POP						
V_{CP}	Output click and pop voltage	ITU-R 2k filter, High-Z/MUTE to Play, Play to Mute/High-Z		7		mV
DC OFSET						
V_{OFFSET}	Output offset voltage			2	5	mV
DC DETECT						
DC_{FAULT}	Output DC fault protection			2	2.5	V
DIGITAL OUTPUT PINS						
V_{OH}	Output voltage for logic level high	I = ±2 mA	90			%VDD
V_{OL}	Output voltage for logic level low	I = ±2 mA			10	%VDD
$t_{DELAY_CLIPDET}$	Signal delay when output clipping detected				20	µs
LOAD DIAGNOSTICS						
S2P	Maximum resistance to detect a short from OUT pins to PVDD				500	Ω
S2G	Maximum resistance to detect a short from OUT pins to ground				200	Ω
SL	Shorted load detection tolerance	Other channels in Hi-Z			±0.5	Ω
OL	Open load	Other channels in Hi-Z	40	70		Ω
T_{DC_DIAG}	DC diagnostic time	All 4 Channels		230		ms
LO	Line output				6	kΩ
T_{LINE_DIAG}	Line output diagnostic time			40		ms
AC_{IMP}	AC impedance accuracy	Gain linearity, f = 19 kHz, R_L = 2 Ω to 16 Ω,			25%	
		Offset			±0.5	Ω
T_{AC_DIAG}	AC diagnostic time	All 4 Channels		520		ms
I2C_ADDR PINS						
t_{I2C_ADDR}	Time delay needed for I^2C address set-up			300		µs

(1) Tested with Output Inductor DFEG7030D-3R3M.

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8.6 Timing Requirements

Test conditions (unless otherwise noted): T_C = 25 °C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, P_O = 1 W/ch, f = 1 kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I²C settings, see 図 79 and 図 82

			MIN	TYP	MAX	UNIT
I²C CONTROL PORT (See 図 42)						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
t_{HOLD1}	Hold time, SCL to SDA		0			ns
t_{HOLD2}	Hold time, start condition to SCL		0.6			µs
t_{START}	I²C startup time after VDD power on reset				12	ms
t_{RISE}	Rise time, SCL and SDA				300	ns
t_{FALL}	Fall time, SCL and SDA				300	ns
t_{SU1}	Setup, SDA to SCL		100			ns
t_{SU2}	Setup, SCL to start condition		0.6			µs
t_{SU3}	Setup, SCL to stop condition		0.6			µs
$t_{W(H)}$	Required pulse duration SCL *High*		0.6			µs
$t_{W(L)}$	Required pulse duration SCL *Low*		1.3			µs
SERIAL AUDIO PORT (See 図 36)						
D_{MCLK}, D_{SCLK}	Allowable input clock duty cycle		45%	50%	55%	
f_{MCLK}	Supported MCLK frequencies: 128, 256, or 512		128		512	xFS
f_{MCLK_Max}	Maximum frequency				25	MHz
t_{SCY}	SCLK pulse cycle time		40			ns
t_{SCL}	SCLK pulse-with LOW		16			ns
t_{SCH}	SCLK pulse-with HIGH		16			ns
$t_{rise/fall}$	Rise and fall time		4			ns
t_{SF}	SCLK rising edge to FSYNC edge		8			ns
t_{FS}	FSYNC rising edge to SCLK edge		8			ns
t_{DS}	DATA set-up time		8			ns
t_{DH}	DATA hold time		8			ns
c_i	Input capacitance, pins MCLK, SCLK, FSYNC, SDIN1, SDIN2				10	pF
T_{LA}	Latency from input to output measured in FSYNC sample count	FSYNC = 44.1 kHz or 48 kHz			30	
		FSYNC = 96 kHz			12	

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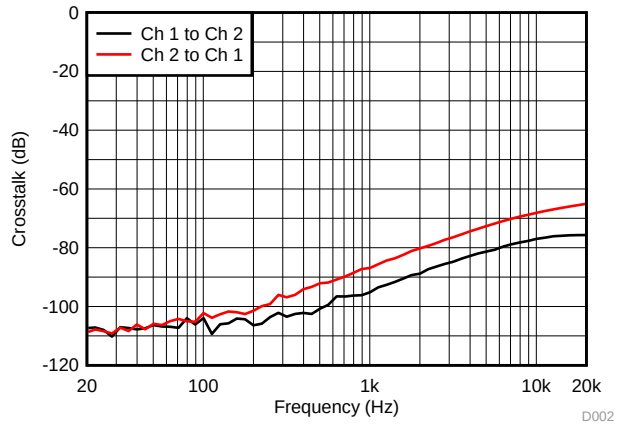
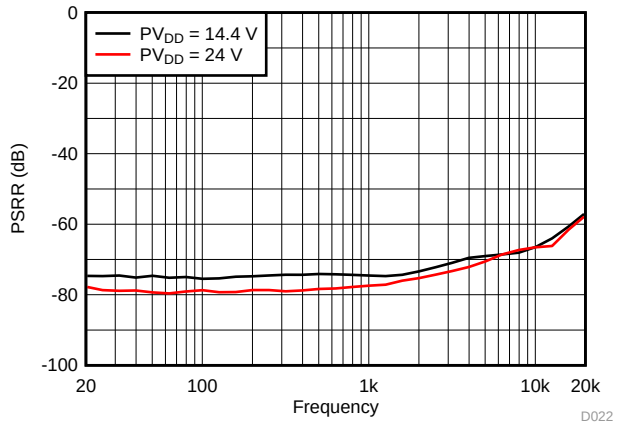
8.7 Typical Characteristics

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)



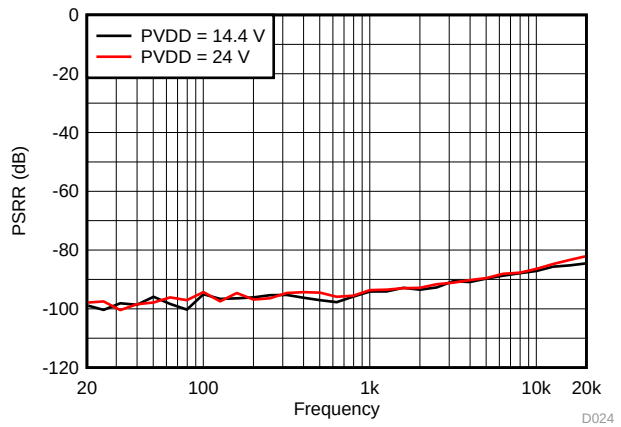
P_O = 1 W

図 1. Crosstalk vs Frequency



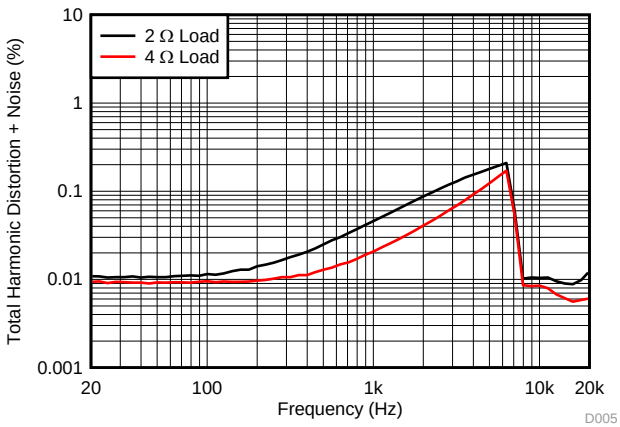
P_O = 1 W

図 2. PVDD PSRR vs Frequency



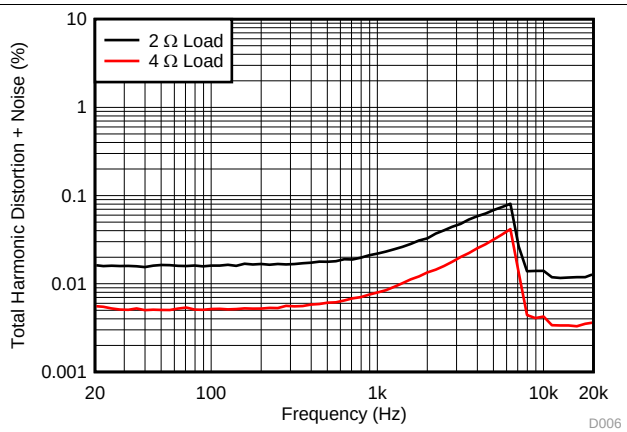
P_O = 1 W

図 3. VBAT PSRR vs Frequency



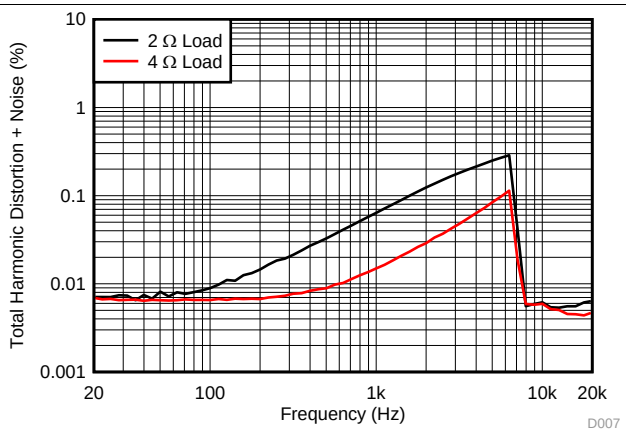
P_O = 1 W 384-kHz f_{SW}

図 4. THD+N vs Frequency



P_O = 1 W 2.11-MHz f_{SW}

図 5. THD+N vs Frequency



P_O = 1 W 24 V 384-kHz f_{SW}

図 6. THD+N vs Frequency

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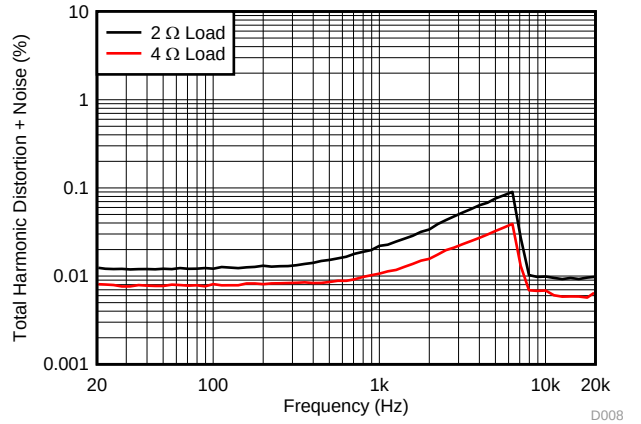
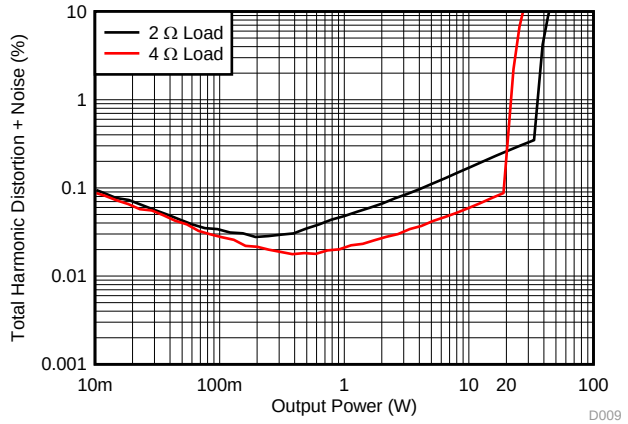
Typical Characteristics (continued)

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)



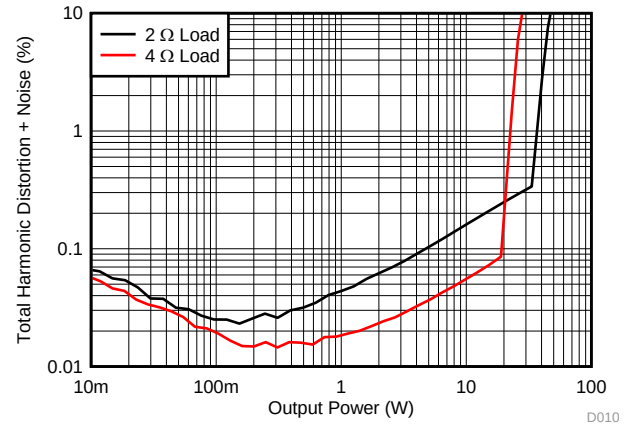
P_O = 1 W　　24 V　　2.11-MHz f_{SW}

図 7. THD+N vs Frequency



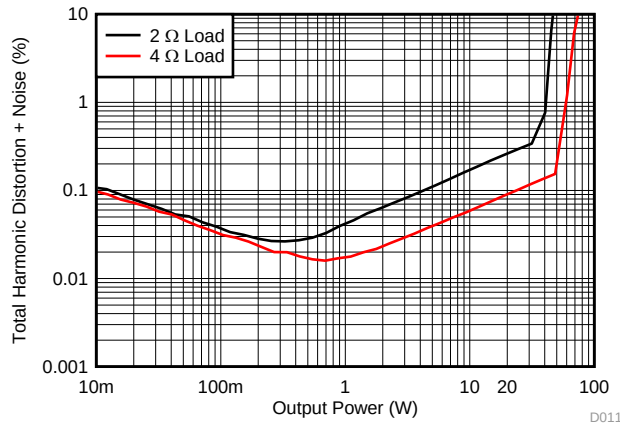
384-kHz f_{SW}

図 8. THD+N vs Power



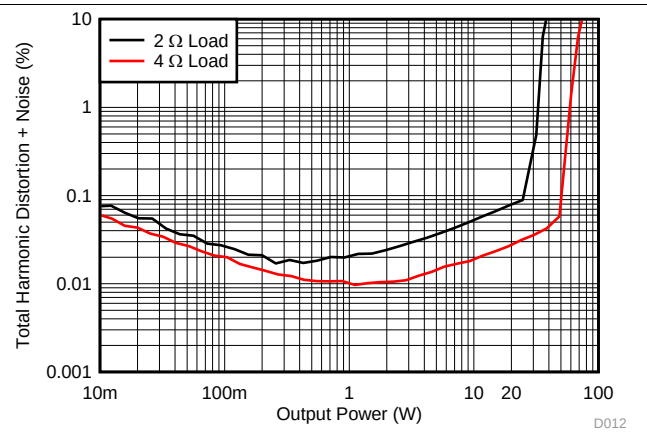
2.11-MHz f_{SW}

図 9. THD+N vs Power



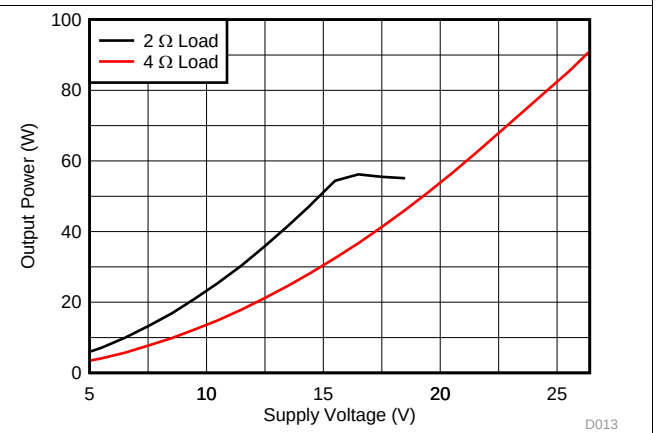
24 V　　384-kHz f_{SW}

図 10. THD+N vs Power



24 V　　2.11-MHz f_{SW}

図 11. THD+N vs Power

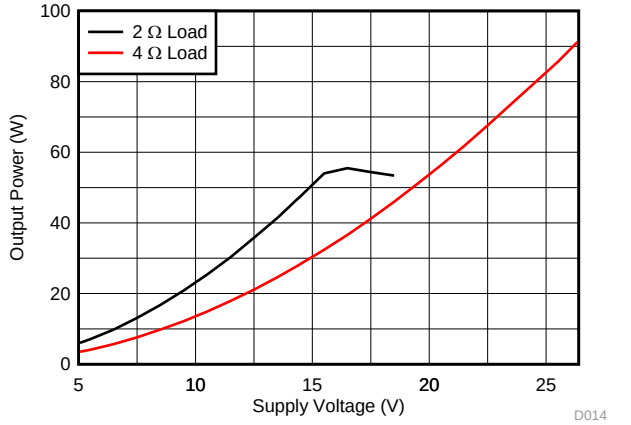


10% THD　　384-kHz f_{SW}

図 12. Output Power vs Supply Voltage

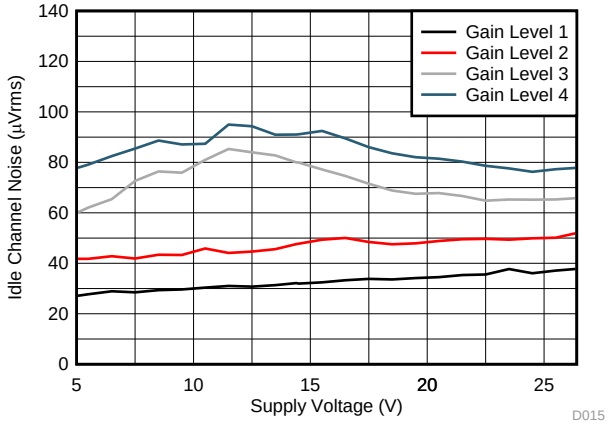
Typical Characteristics (continued)

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)



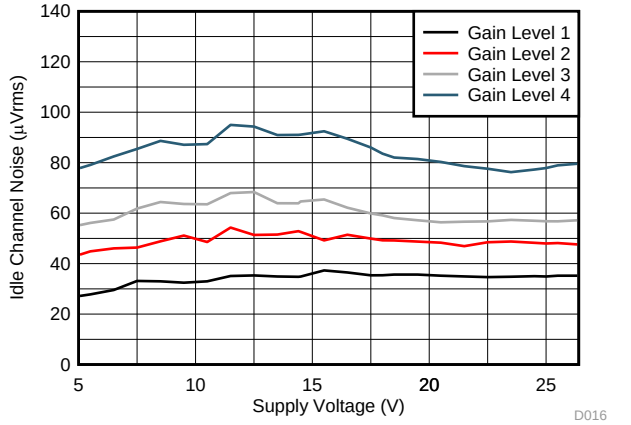
10% THD 2.11-MHz f_{SW}

図 13. Output Power vs Supply Voltage



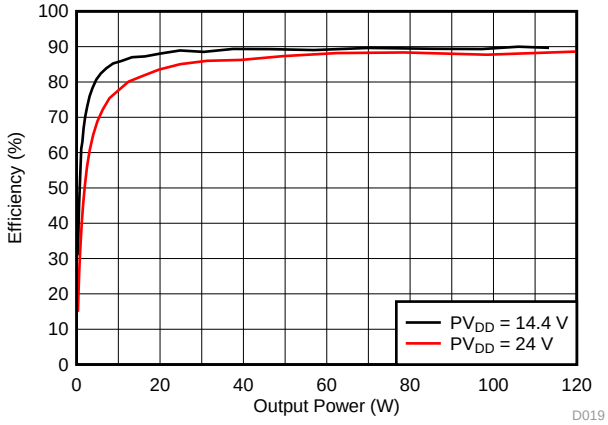
A-weighted Noise 384-kHz f_{SW}

図 14. Noise vs Supply Voltage



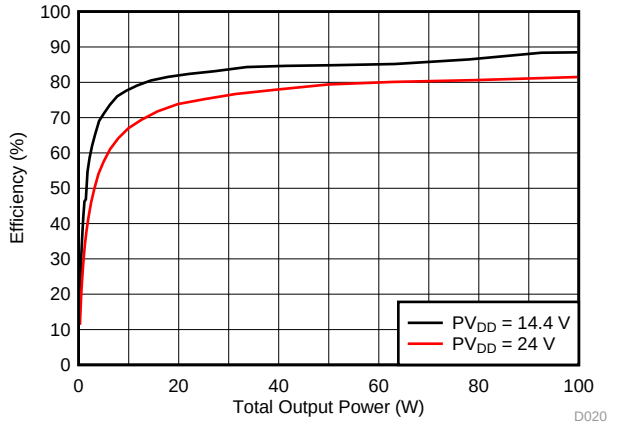
A-weighted Noise 2.11-MHz f_{SW}

図 15. Noise vs Supply voltage



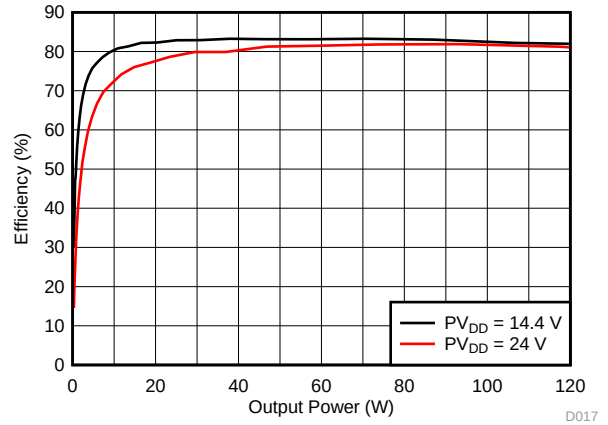
4 Ω 384-kHz f_{SW}

図 16. Power Efficiency vs Output Power



4 Ω 2.1-MHz f_{SW}

図 17. Power Efficiency vs Output Power



2 Ω 384-kHz f_{SW}

図 18. Power Efficiency vs Output Power

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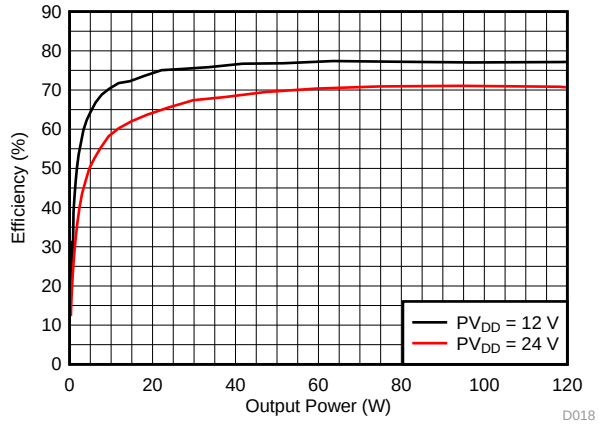
Typical Characteristics (continued)

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)



2 Ω 2.1-MHz f_{SW}

図 19. Power Efficiency vs Output Power

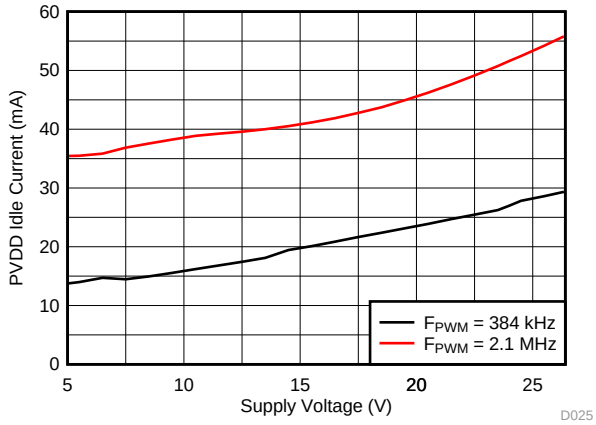


図 20. PVDD Current vs Voltage

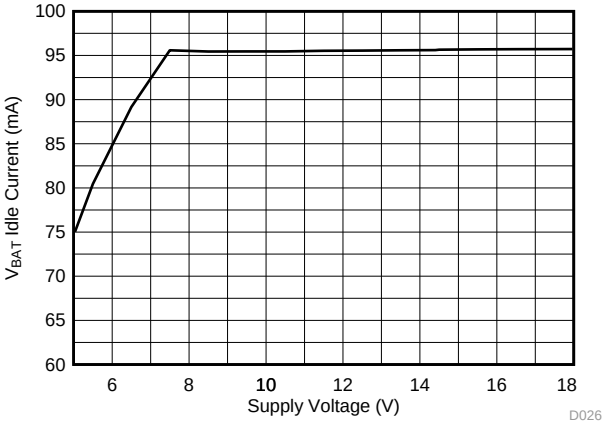


図 21. VBAT Current vs Voltage

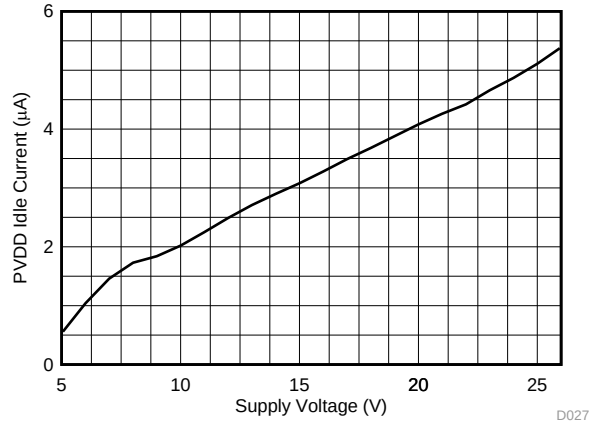
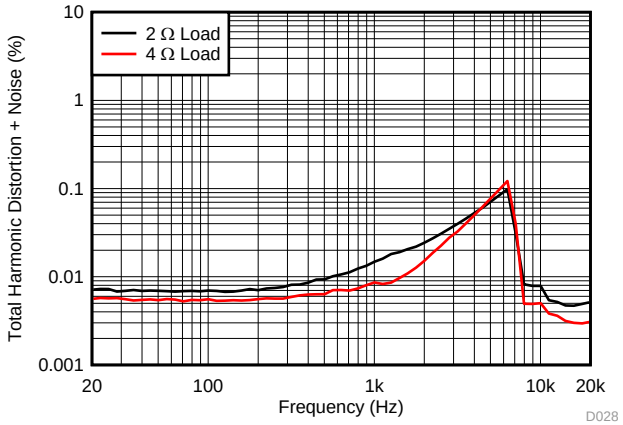
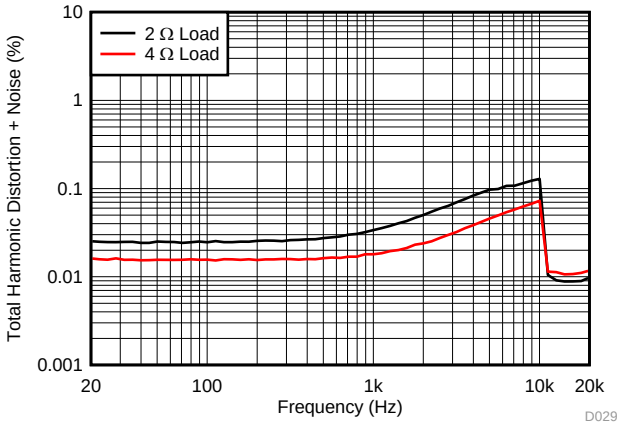


図 22. PVDD Standby Current vs Voltage



1 W 384-kHz f_{SW}

図 23. PBTL THD+N vs Frequency



P_O = 1 W 2.1-MHz f_{SW}

図 24. PBTL THD+N vs Frequency

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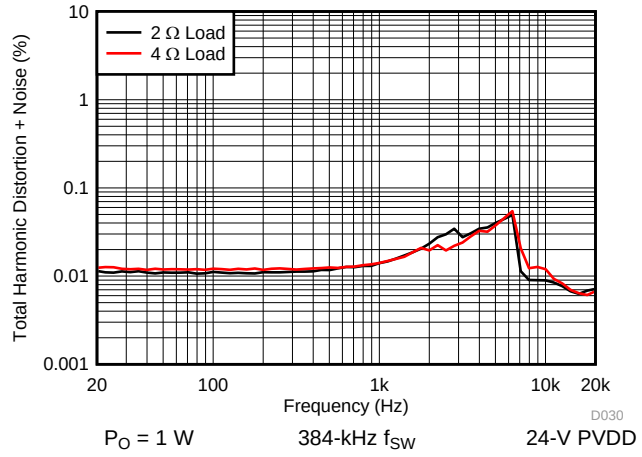
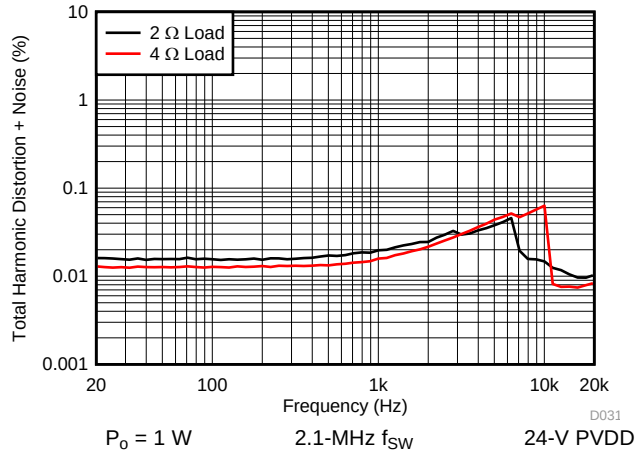
Typical Characteristics (continued)

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)



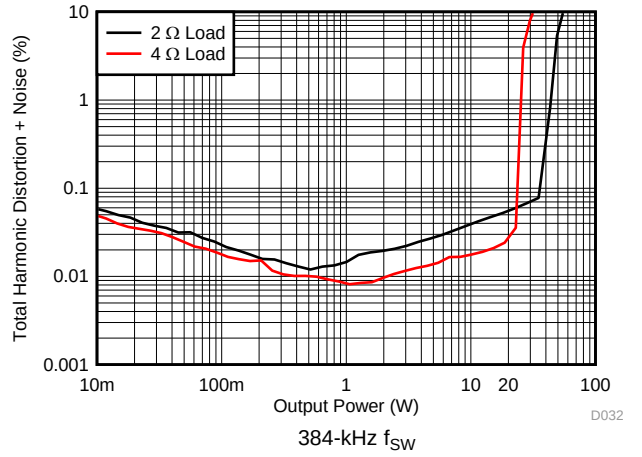
P_O = 1 W 384-kHz f_{SW} 24-V PVDD

図 25. PBTL THD+N vs Frequency



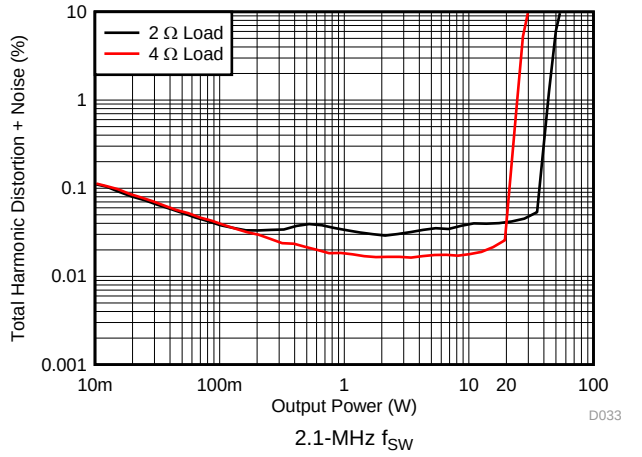
P_o = 1 W 2.1-MHz f_{SW} 24-V PVDD

図 26. PBTL THD+N vs Frequency



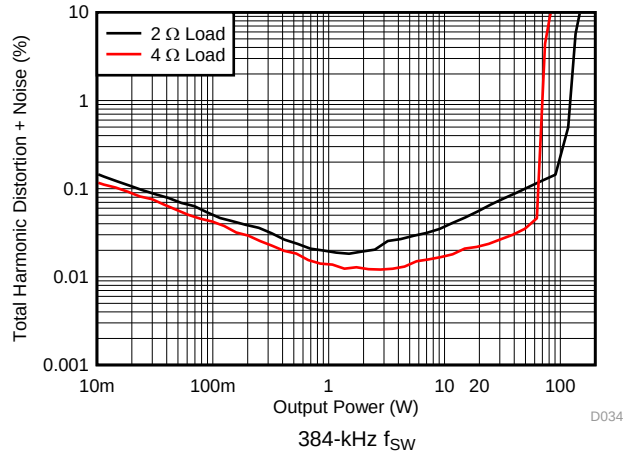
384-kHz f_{SW}

図 27. PBTL THD+N vs Power



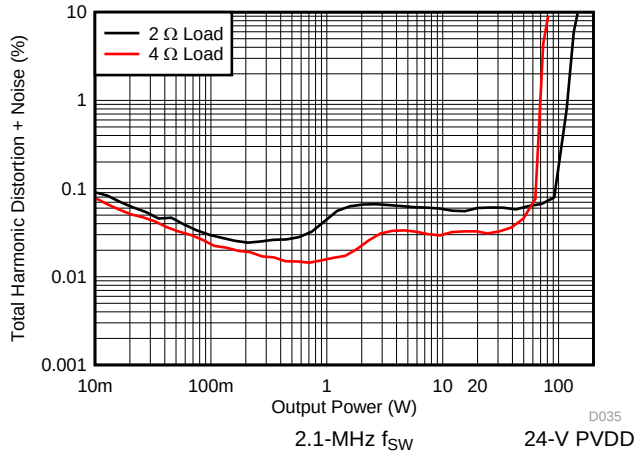
2.1-MHz f_{SW}

図 28. PBTL THD+N vs Power



384-kHz f_{SW}

図 29. PBTL THD+N vs Power



2.1-MHz f_{SW} 24-V PVDD

図 30. PBTL THD+N vs Power

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Typical Characteristics (continued)

T_A = 25 ºC, V_{VDD} = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, f_{SW} = 2.11 MHz, AES17 filter, default I^2C settings, see 図 79 and 図 82 (unless otherwise noted)

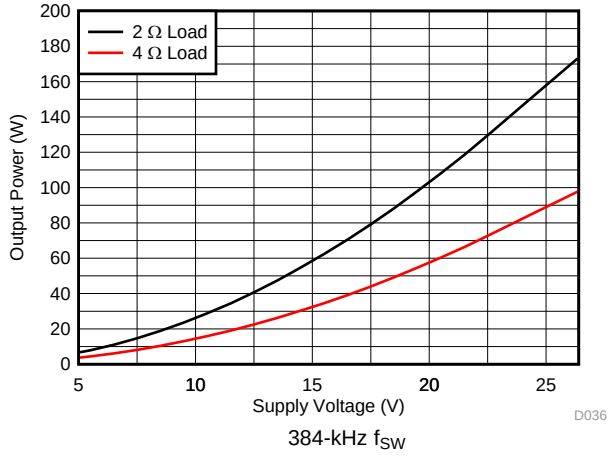

図 31. Output Power vs Voltage

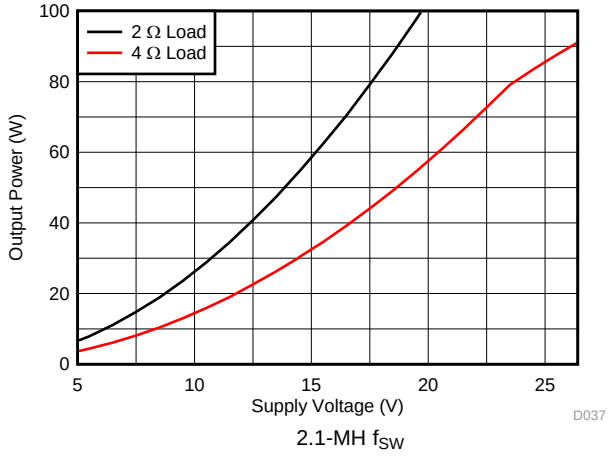

図 32. Output Power vs Voltage

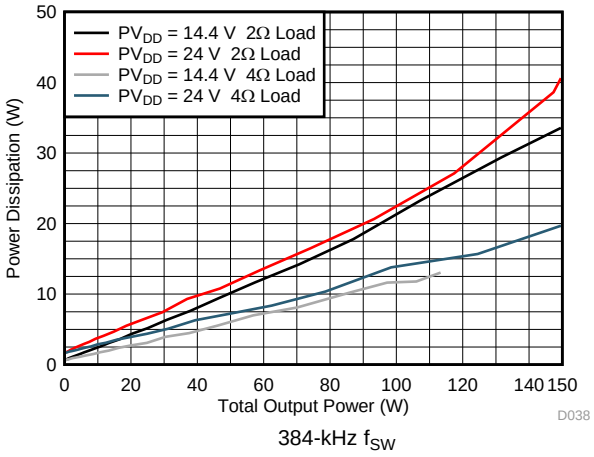

図 33. Power Dissipation vs Output Power

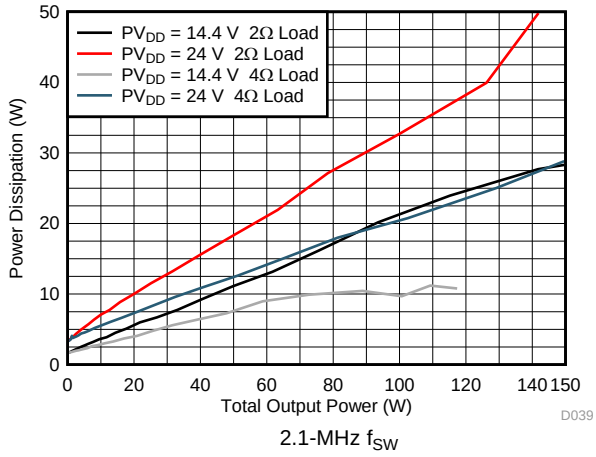

図 34. Power Dissipation vs Output Power

9 Parameter measurement Information

The parameters for the TAS6424-Q1 device were measured using the circuit in 図 79.

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10 Detailed description

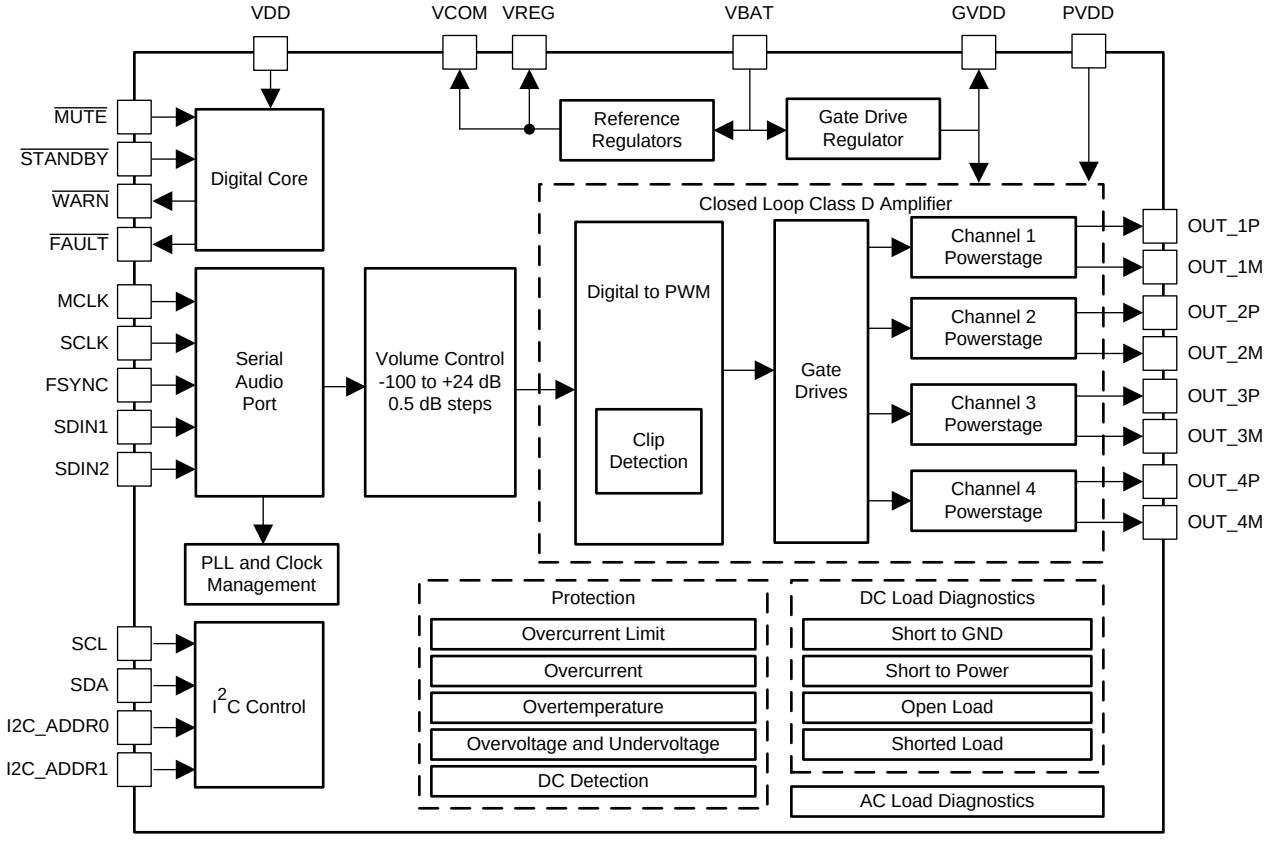
10.1 Overview

The TAS6424-Q1 device is a four-channel digital-input Class-D audio amplifier for use in the automotive environment. The device is designed for vehicle battery operation or boosted voltage systems. The design uses ultra-efficient class-D technology developed by Texas Instruments specifically tailored for the automotive industry. This technology allows for reduced power consumption, reduced PCB area, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound-system design with smaller size and lower weight than traditional class-AB solutions.

The core design blocks are as follows:

- Serial audio port
- Clock management
- High-pass filter and volume control
- Pulse width modulator (PWM) with output stage feedback
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

10.2 Functional Block Diagram



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10.3 Feature Description

10.3.1 Serial Audio Port

The serial audio port (SAP) receives audio in either I²S, left justified, right justified, or TDM formats.

Settings for the serial audio port are programmed in the SAP control register (address 0x03), see the *SAP Control (Serial Audio-Port Control) Register (address = 0x03) [default = 0x04]* section.

図 35 shows the digital audio data connections for I²S and TDM8 mode for an eight channel system.

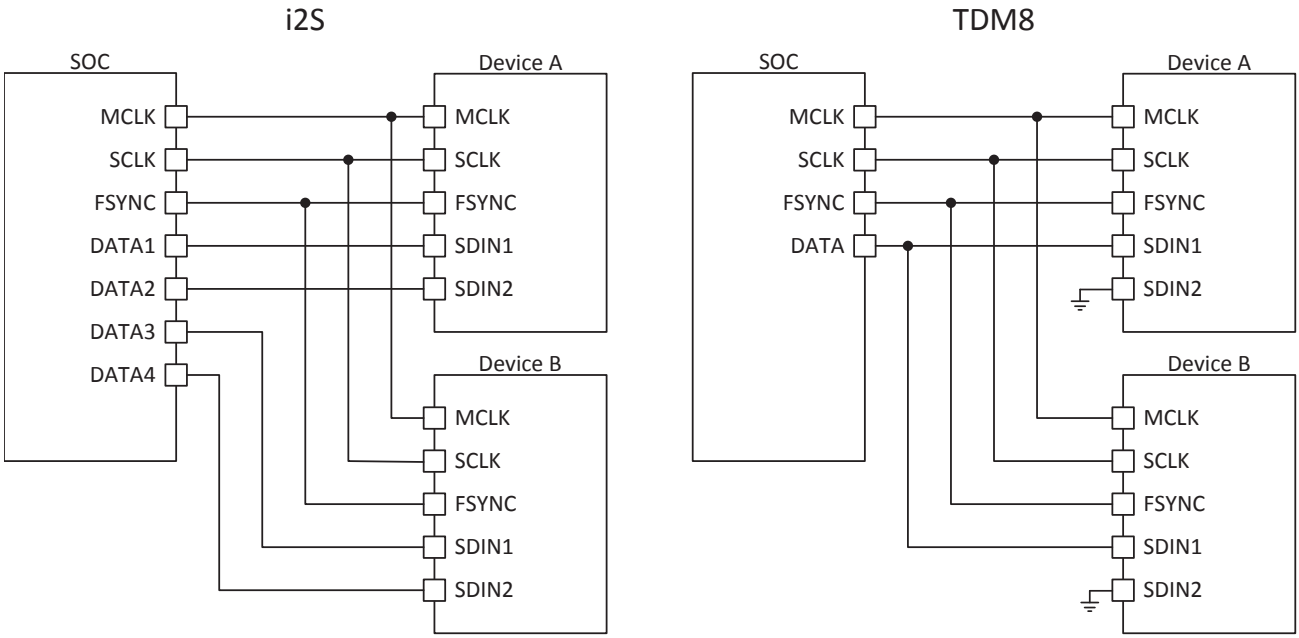

図 35. Digital-Audio Data Connection

10.3.1.1 I²S Mode

I²S timing uses the FSYNC pin to define when the data being transmitted is for the left channel and when it is for the right channel. The FSYNC pin is low for the left channel and high for the right channel. The bit clock, SCLK, runs at 32 or 64 × f_S and is used to clock in the data. A delay of one bit clock occurs from the time the FSYNC signal changes state to the first bit of data on the data lines. The data is presented in 2s-complement form (MSB-first). The data is valid on the rising edge of the bit clock and is used to clock in the data.

10.3.1.2 Left-Justified Timing

Left-justified (LJ) timing also uses the FSYNC pin to define when the data being transmitted is for the left channel and when it is for the right channel. The FSYNC pin is high for the left channel and low for the right channel. A bit clock running at 32 or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time FSYNC toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. Digital words can be 16-bits or 24-bits wide and pad any unused trailing data-bit positions in the left-right (L/R) frame with zeros.

10.3.1.3 Right-Justified Timing

Right-justified (RJ) timing also uses the FSYNC pin to define when the data being transmitted is for the left channel and when it is for the right channel. The FSYNC pin is high for the left channel and low for the right channel. A bit clock running at 32 or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8-bit clock periods (for 24-bit data) after the FSYNC pin toggles. In RJ mode the LSB of data is always clocked by the last bit clock before the FSYNC pin transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The device pads the unused leading data-bit positions in the L/R frame with zeros.

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Feature Description (continued)

10.3.1.4 TDM Mode

TDM mode supports 4 or 8 channels of audio data. The device can be configured through I^2C to use different stereo pairs in the TDM data stream. The TDM mode supports 16-bit, 24-bit, and 32-bit input data lengths.

In TDM mode, the SCLK pin must be 128 or 256, depending on the TDM slot size. In TDM mode SCLK and MCLK can be connected together

In TDM mode, the SDIN1 pin (pin 15) is used for digital audio data. TI recommends to connect the unused SDIN2 pin (pin 16) to ground. 表 1 lists register settings for the TDM channel selection.

表 1. TDM Channel Selection

REGISTER SETTING		TDM8 CHANNEL SLOT							
0x03 BIT 5	0x03 BIT 3	1	2	3	4	5	6	7	8
0	0	CH1	CH2	CH3	CH4	—	—	—	—
1	0	—	—	—	—	CH1	CH2	CH3	CH4
0	1	CH3	CH4	CH1	CH2	—	—	—	—
1	1	—	—	—	—	CH3	CH4	CH1	CH2

If PBTL mode is programmed for channel 1/2 or channel 3/4 the datasource can be set according to 表 2.

表 2. TDM Channel Selection in PBTL Mode

REGISTER SETTING			TDM8 CHANNEL SLOT							
0x03 BIT 5	0x03 BIT 3	0x21 BIT 6	1	2	3	4	5	6	7	8
0	0	0	PBTL CH1/2	—	PBTL CH3/4	—	—	—	—	—
1	0	0	—	—	—	—	PBTL CH1/2	—	PBTL CH3/4	—
0	0	1	—	PBTL CH1/2	—	PBTL CH3/4	—	—	—	—
1	0	1	—	—	—	—	—	PBTL CH1/2	—	PBTL CH3/4
0	1	0	PBTL CH3/4	—	PBTL CH1/2	—	—	—	—	—
1	1	0	—	—	—	—	PBTL CH3/4	—	PBTL CH1/2	—
0	1	1	—	PBTL CH3/4	—	PBTL CH1/2	—	—	—	—
1	1	1	—	—	—	—	—	PBTL CH3/4	—	PBTL CH1/2

10.3.1.5 Supported Clock Rates

The device supports MCLK rates of 128 × f_S, 256 × f_S, or 512 × f_S.

The device supports SCLK rates of 32 × f_S, 48 × f_S or 64 × f_S.

The device supports FSYNC rates of 44.1 kHz, 48 kHz, or 96 kHz.

The maximum clock frequency is 25 MHz. Therefore, for a 96-kHz FSYNC rate, the maximum MCLK rate is 256 × f_S.

The MCLK clock must not be in phase to sync to SCLK. Duty cycle of 50% is required for 128x FSYNC, for 256x and 512x 50% duty is not required.

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10.3.1.6 Audio-Clock Error Handling

When any kind of clock error, MCLK-FSYNC or SCLK-FSYNC ratio, or clock halt is detected, the device puts all channels into the Hi-Z state. When all audio clocks are within the expected range, the device automatically returns to the state it was in. See the *Timing Requirements* table for timing requirements.

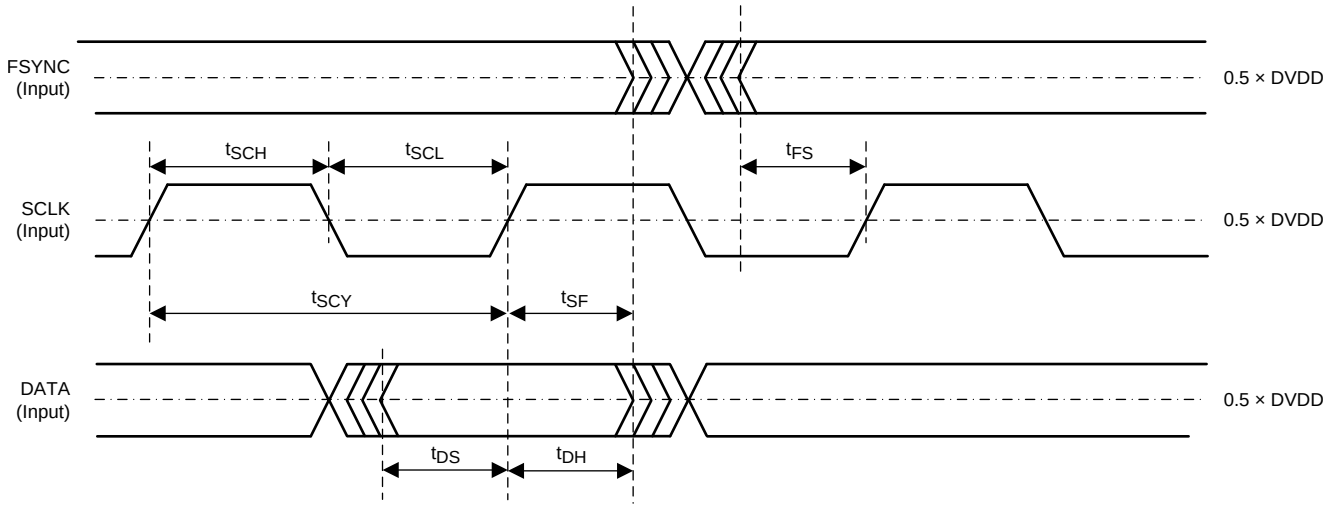

図 36. Serial Audio Timing

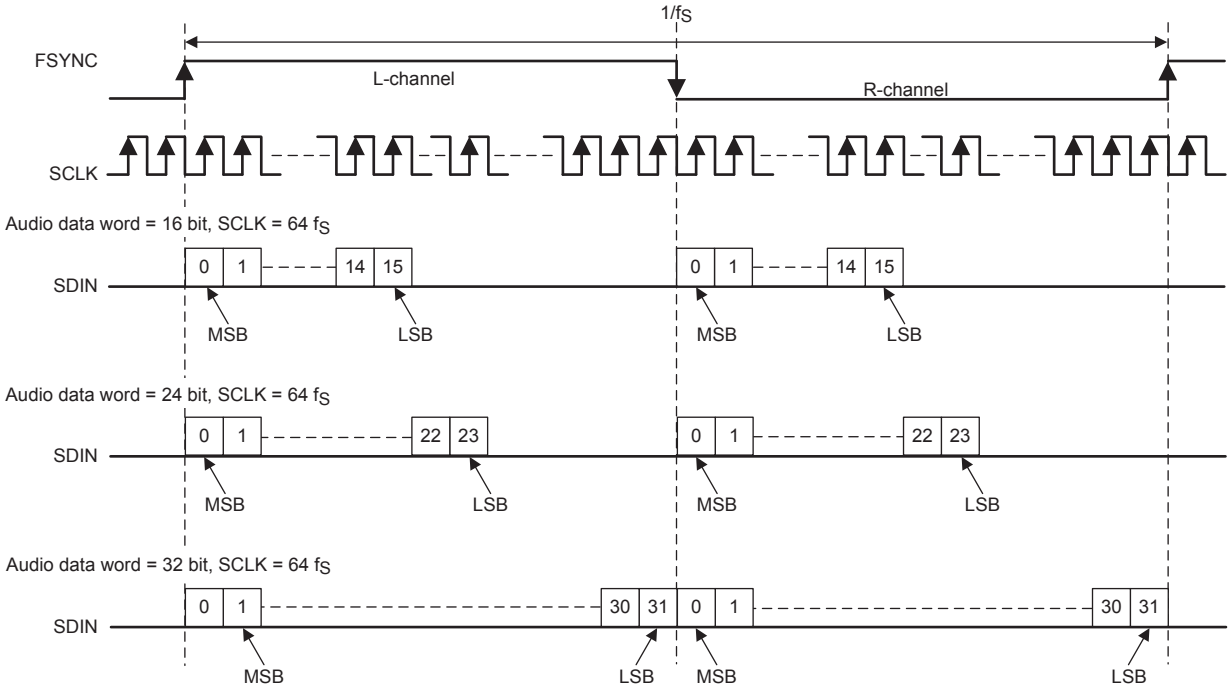

図 37. Left-Justified Audio Data Format

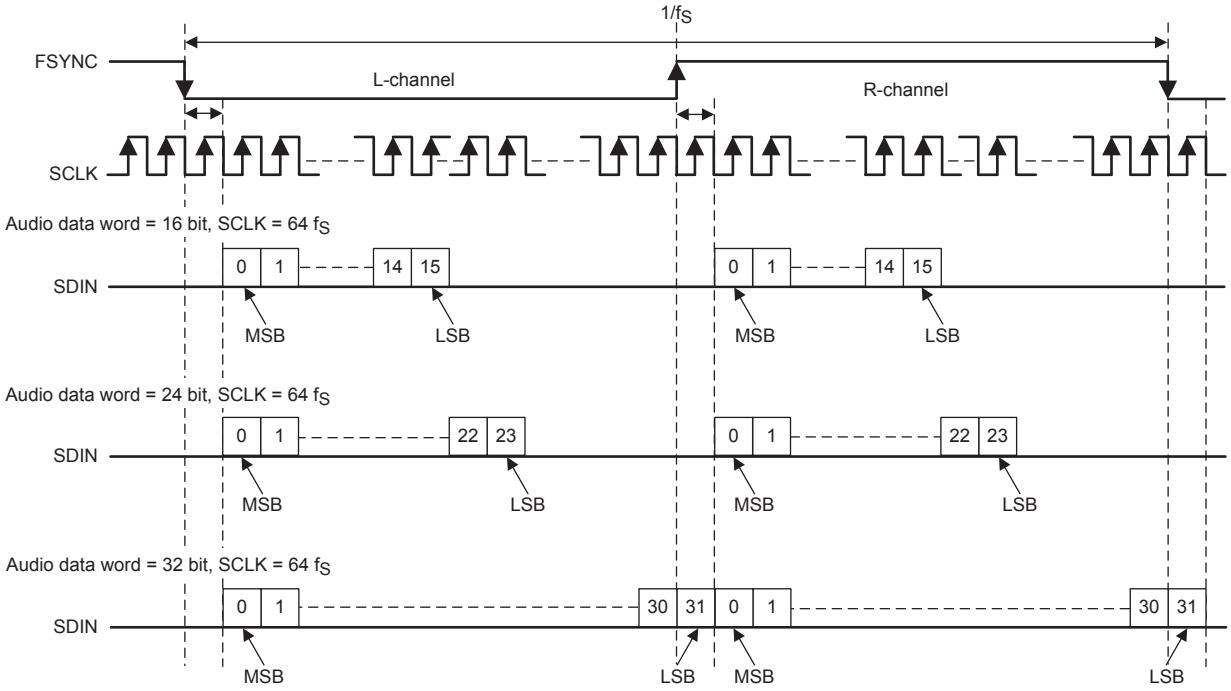

図 38. I²S Audio Data Format

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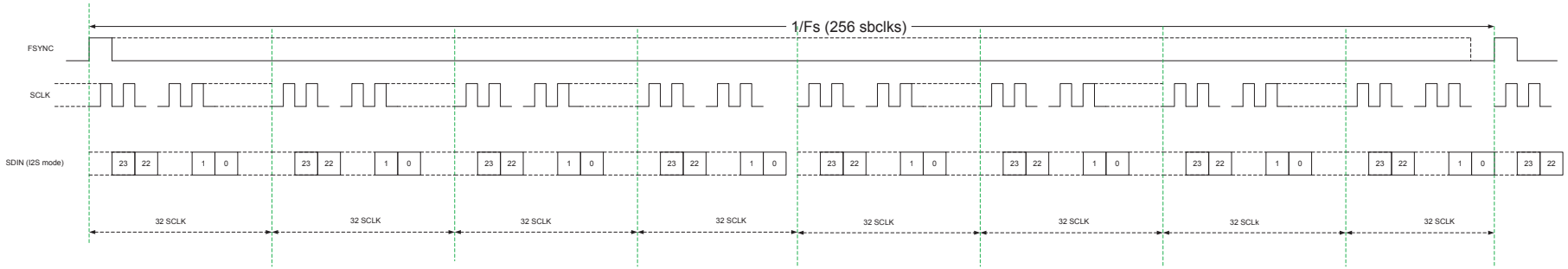

Audio Data Format: TDM8 mode

図 39. TDM Audio Data Format

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10.3.2 High-Pass Filter

Direct-current (DC) content in the audio signal can damage speakers. The data path has a high-pass filter to remove any DC from the input signal. The corner frequency is selectable from 4 Hz, 8 Hz, or 15 Hz to 30 Hz with bits 0 through 3 in register 0x26. The default value of –3 dB is approximately 4 Hz for 44.1 kHz or 48 kHz and approximately 8 Hz for 96-kHz sampling rates.

10.3.3 Volume Control and Gain

Each channel has a independent digital-volume control with a range from –100 dB to +24 dB with 0.5-dB steps. The volume control is set through I^2C. The gain-ramp rate is programmable through I^2C to take one step every 1, 2, 4, or 8 FSYNC cycles.

The peak output-voltage swing is also configurable in the gain control register through I^2C. The four gain settings are 7.5 V, 15 V, 21 V, and 29 V. TI recommends selecting the lowest possible for the expected PVDD operation to optimize output noise and dynamic range performance.

10.3.4 High-Frequency Pulse-Width Modulator (PWM)

The PWM converts the PCM input data into a switched signal of varying duty cycle. The PWM modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability. The output switching rate is synchronous to the serial audio-clock input and is programmed through I^2C to be between 8× and 48× the input-sample rate. The option to switch at high frequency allows the use of smaller and lower cost external filtering components. 表 3 lists the switch frequency options for bits 4 through 6 in the miscellaneous control 2 register (address 0x02).

表 3. Output Switch Frequency Option

INPUT SAMPLE RATE	BIT 6:4 SETTINGS					
	000	001	010 to 100	101	110	111
44.1 kHz	352.8 kHz	441 kHz	RESERVED	1.68 MHz	1.94 MHz	2.12 MHz
48 kHz	384 kHz	480 kHz	RESERVED	1.82 MHz	2.11 MHz	Not supported
96 kHz	384 kHz	480 kHz	RESERVED	1.82 MHz	2.11 MHz	Not supported

10.3.5 Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power-FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

The gate-driver power-supply voltage, GVDD, is internally generated and a decoupling capacitor is connected at pin 9 and pin 10.

The full H-bridge output stages use only NMOS transistors. Therefore, bootstrap capacitors are required for the proper operation of the high side NMOS transistors. A 1-µF ceramic capacitor of quality X7R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input (see the application circuit diagram in 図 79). The bootstrap capacitors connected between the BST pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high keeping the high-side MOSFETs turned on.

10.3.6 Power FETs

The BTL output for each channel comprises four N-channel 90-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle the fast switching frequency and large voltage transients during load dump.

10.3.7 Load Diagnostics

The device incorporates both DC-load and AC-load diagnostics which are used to determine the status of the load. The DC diagnostics are turned on by default but if a fast startup without diagnostics is required the DC diagnostics can be bypassed through I^2C. The DC diagnostics runs when any channel is directed to leave the Hi-Z state and enter the MUTE or PLAY state. The DC diagnostics can also be enabled manually to run on any or all channels even if the other channels are playing audio. DC Diagnostics can be started from any operating

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condition but if the channel is in play state then the time to complete the diagnostic is longer because the device must ramp down the audio signal of that channel before transitioning to the Hi-Z state. The DC diagnostics are available as soon as the device supplies are within the recommended operating range. The DC diagnostics do not rely on the audio input clocks to be available to function. DC Diagnostic results are reported for each channel separately through the I^2C registers.

10.3.7.1 DC Load Diagnostics

The DC load diagnostics are used to verify the load connected. The DC diagnostics consists of four tests: short-to-power (S2P), short-to-ground (S2G), open-load (OL), and shorted-load (SL). The S2P and S2G tests trigger if the impedance to GND or a power rail is below that specified in the *Specifications* section. The diagnostic detects a short to vehicle battery even when the supply is boosted. The SL test has an I^2C-configurable threshold depending on the expected load to be connected. Because the speakers connected to each channel might be different, each channel can be assigned a unique threshold value. The OL test reports if the select channel has a load impedance greater than the limits in the *Specifications* section.

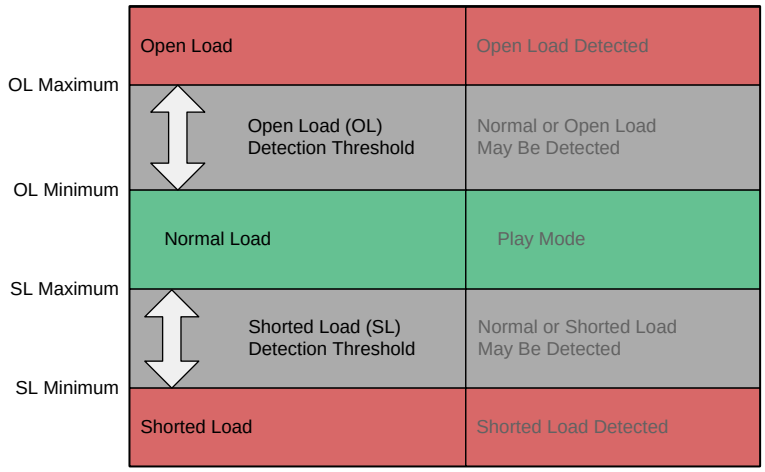

図 40. DC Load Diagnostic Reporting Thresholds

10.3.7.2 Line Output Diagnostics

The device also includes an optional test to detect a line-output load. A line-output load is a high-impedance load that is above the open-load (OL) threshold such that the DC-load diagnostics report an OL condition. After an OL condition is detected on a channel, if the line output detection bit is also set, the channel checks if a line-output load is present as well. This test is not pop free, so if an external amplifier is connected it should be muted.

10.3.7.3 AC Load Diagnostics

The AC load diagnostic is used to determine the proper connection of a capacitively coupled speaker or tweeter when used with a passive crossover. The AC load diagnostic is controlled through I^2C. The AC diagnostics requires an external input signal and reports the approximate load impedance and phase. The selected signal frequency should create current flow through the desired speaker for proper detection. If multiple channels must be tested, the diagnostics should be run in series. The AC load-diagnostic test procedure is as follows.

For load-impedance detection, use the following test procedure:

1. Set the channels to be tested into the Hi-Z state.
2. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 0.
3. Apply a full-scale input signal from the DSP for the tested channels with the desired frequency (recommended 10 kHz to 20 kHz).

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The device ramps the signal up and down automatically to prevent pops and clicks.

4. Set the device into the AC diagnostic mode (set bits 3:0 in register 0x15 to 1 for CH1 to CH4, set bit 3 in register 0x15 to 1, and set bit 1 in register 0x15 to 1 for PBTL12 and PBTL34).

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5. Read back the AC impedance (register 0x17 through register 0x1A).

   When the test is complete the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected impedance is stored in the appropriate I^2C register.

For loopback delay detection, use the following test procedure for either BTL mode or PBTL mode:

- BTL mode
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 1 to enable AC loopback mode.
  2. Apply a 0-dBFS 19K signal and enable AC load diagnostics. CH1 and CH2 reuse the AC sensing loop of CH1 (set bit 3 in register 0x15 to 1). CH3, CH4 reuse the AC sensing loop of CH3 (set bit 1 in register 0x15 to 1)
  3. Read back the AC_LDG_PHASE1 value (register 0x1B and register 0x1C).

     When the test is complete, the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected impedance is stored in the appropriate I^2C register.
- PBTL mode
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 1 to enable AC loopback mode.
  2. Set the PBTL CH12 and PBTL CH34 bits (bits 5 and 4 in register 0x00) to 0 without toggling SDz pin to enter BTL mode only for load diagnostics.
  3. Apply a 0-dBFS 19K signal and enable AC load diagnostics. For PBTL_12, enable the AC sensing loop of CH1 (set bit 3 in register 0x15 to 1). For PBTL_34, enable the AC sensing loop of CH3 (set bit 1 in register 0x15 to 1).
  4. Read back the AC_LDG_PHASE1 (register 0x1B and register 0x1C).
  5. Set the PBTL CH12 and PBTL CH34 bits (bits 5 and 4 in register 0x00) to 1 to go back to PBTL mode for load diagnostics.

表 4. AC Impedance Code to Magnitude

SETTING	GAIN AT 19 kHz	I(A)	MEASUREMENT RANGE (Ω)	MAPPING FROM CODE TO MAGNITUDE (Ω/Code)
Gain = 4, I = 10 mA (recommended)	4.28	0.01	12	0.05832
Gain = 4, I = 19 mA	4.28	0.019	6	0.0307
Gain = 1, I = 10 mA (recommended)	1	0.01	48	0.2496
Gain = 1, I = 19 mA	1	0.019	24	0.1314

10.3.8 Protection and Monitoring

10.3.8.1 Overcurrent Limit (I_{LIMIT})

The overcurrent limit terminates each PWM pulse to limit the output current flow when the current limit (I_{LIMIT}) is exceeded. Power is limited but operation continues without disruption and prevents undesired shutdown for transient music events. I_{LIMIT} is not reported as a fault condition to either registers or the $\overline{\text{FAULT}}$ pin. Each channel is independently monitored and limited. The two programable levels can be set by bit 4 in the miscellaneous control 1 register (address 0x01).

10.3.8.2 Overcurrent Shutdown (I_{SD})

If the output load current reaches I_{SD}, such as an output short to GND, then a peak current limit occurs which shuts down the channel. The time to shutdown the channel varies depending on the severity of the short condition. The affected channel is placed into the Hi-Z state, the fault is reported to the register, and the $\overline{\text{FAULT}}$ pin is asserted. If the diagnostics are enabled then the device automatically starts diagnostics on the channel and, if no load failure is found, the device restarts. If a load fault is found the device continues to rerun the diagnostics once per second. Because this hiccup mode is using the diagnostics, no high current is created. If the diagnostics are disabled the device sets the state for that channel to Hi-Z and requires the MCU to take the appropriate action.

There are two programable levels that can be set by bit 4 in the miscellaneous control 1 register (address 0x01).

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10.3.8.3 DC Detect

This circuit detects a DC offset continuously during normal operation at the output of the amplifier. If the DC offset exceeds the threshold, that channel is placed in the Hi-Z state, the fault is reported to the I^2C register, and the $\overline{\text{FAULT}}$ pin is asserted. A register bit can be used to mask reporting to the $\overline{\text{FAULT}}$ pin if needed.

10.3.8.4 Clip Detect

The clip detect is reported on the $\overline{\text{WARN}}$ pin if 100% duty-cycle PWM if reached for a minimum of 20 cycles. If any channel is clipping, the clipping is reported to the pin. The clip detect is latched and can be cleared by I^2C . Masking the clip reporting to the pin is possible through I^2C.

10.3.8.5 Global Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD)

Four overtemperature warning levels are available in the device that can be selected (see the *Register Maps* section for thresholds). When the junction temperature exceeds the warning level, the $\overline{\text{WARN}}$ pin is asserted unless the mask bit has been set to disable reporting. The device functions until the OTSD value is reached at which point all channels are placed in the Hi-Z state and the $\overline{\text{FAULT}}$ pin is asserted. When the junction temperature returns to normal levels, the device automatically recovers and places all channels into the state indicated by the register settings.

10.3.8.6 Channel Overtemperature Warning [OTW(i)] and Shutdown [OTSD(i)]

In addition to the global OTW, each channel also has an individual overtemperature warning and shutdown. If a channel exceeds the OTW(i) threshold, the warning register bit is set as the $\overline{\text{WARN}}$ pin is asserted unless the mask bit has been set to disable reporting. If the channel temperature exceeds the OTSD(i) threshold then that channel goes to the Hi-Z state until the temperature drops below the OTW(i) threshold at which point the channel goes to the state indicated by the state control register.

10.3.8.7 Undervoltage (UV) and Power-On-Reset (POR)

The undervoltage (UV) protection detects low voltages on the PVDD and VBAT pins. In the event of an UV condition, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. A power-on reset (POR) on the VDD pin causes the I^2C to goes to the high-impedance (Hi-Z) state and all registers are reset to default values. At power-on or after a POR event, the POR warning bit and $\overline{\text{WARN}}$ pin are asserted.

10.3.8.8 Overvoltage (OV) and Load Dump

The overvoltage (OV) protection detects high voltages on the PVDD pin. If the PVDD pin reaches the OV threshold, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. The device can withstand 40-V load-dump voltage spikes.

10.3.9 Power Supply

The device has three power supply inputs, VDD, PVDD, and VBAT, which are described as follows:

VDD This pin is a 3.3-V supply pin that provides power to the low voltage circuitry.

VBAT This pin is a higher voltage supply that can be connected to the vehicle battery or the regulated voltage rail in a boosted system within the recommended limits. For best performance, this rail should be 10 V or higher. See the *Recommended Operating Conditions* table for the maximum supply voltage. This supply rail is used for higher voltage analog circuits but not the output FETs.

PVDD This pin is a high-voltage supply that can either be connected to the vehicle battery or to another voltage rail in a boosted system. The PVDD pin supplies the power to the output FETs and can be within the recommended operating limits, even if that is below the VBAT supply, to allow for dynamic voltage systems.

Several on-chip regulators are included generating the voltages necessary for the internal circuitry. The external pins are provided only for bypass capacitors to filter the supply and should not be used to power other circuits.

The device can withstand fortuitous open ground and power conditions within the absolute maximum ratings for the device. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs.

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10.3.9.1 Vehicle-Battery Power-Supply Sequence

The device can accept any sequence of the VBAT, PVDD and VDD supply.

In a typical system, the VBAT and PVDD supplies are both connected to the vehicle battery and power up at the same time. The VDD supply should be applied after the VBAT and PVDD supplies are within the recommended operating range. When removing power from the device, TI recommends to deassert the VDD supply first then the VBAT, PVDD, or both supplies which provides the lowest click and pop performance.

10.3.9.2 Boosted Power-Supply Sequence

In this case, the VBAT and PVDD inputs are not connected to the same supply.

When powering up, apply the VBAT supply first, the VDD supply second, and the PVDD supply last.

When powering down, remove the PVDD supply first, the VDD supply second, and the VBAT supply last.

10.3.10 Hardware Control Pins

The device has four pins for control and device status: $\overline{\text{FAULT}}$, $\overline{\text{MUTE}}$, $\overline{\text{WARN}}$, and $\overline{\text{STANDBY}}$.

10.3.10.1 $\overline{\text{FAULT}}$

The $\overline{\text{FAULT}}$ pin reports faults and is active low under any of the following conditions:

- Any channel faults (overcurrent or DC detection)
- Overtemperature shutdown
- Overvoltage or undervoltage conditions on the VBAT or PVDD pins
- Clock errors

The $\overline{\text{FAULT}}$ pin is deactivated when none of the previously listed conditions exist.

Register bits are available to mask fault categories from reporting to the $\overline{\text{FAULT}}$ pin. These bits only mask the setting of the pin and do not affect the register reporting or protection of the device. By default all faults are reported to the pin. See the *Register Maps* section for a description of the mask settings.

This pin is an open-drain output with an internal 100-kΩ pullup resistor to VDD.

10.3.10.2 $\overline{\text{WARN}}$

This active-low output pin reports audio clipping, overtemperature warnings, and POR events.

Clipping is reported if any channel is at the maximum modulation for 20 consecutive PWM clocks which results in a 10-µs delay to report the onset of clipping. The warning bit is sticky and can be cleared by the CLEAR FAULT bit (bit 7) in register 0x21.

An overtemperature warning (OTW) is reported if the general temperature or any of the channel temperature warnings are set. The warning temperature can be set through bits 5 and 6 in register 0x01.

Register bits are available to mask either clipping or OTW reporting to the pin. These bits only mask the setting of the pin and do not affect the register reporting. By default both clipping and OTW are reported.

The $\overline{\text{WARN}}$ pin is latched and can be cleared by writing the CLEAR FAULT bit (bit 7) in register 0x21.

This pin is an open-drain output with an internal 100-kΩ pullup resistor to VDD.

10.3.10.3 $\overline{\text{MUTE}}$

This active-low input pin is used for hardware control of the mute and unmute function for all channels.

This pin has a 100-kΩ internal pulldown resistor.

10.3.10.4 $\overline{\text{STANDBY}}$

When this active-low input pin is asserted, the device goes into shutdown and current draw is limited. This pin can be used to shut down the device rapidly. The outputs are ramped down in less than 5 ms if the device is not already in the Hi-Z state. The I^2C bus goes into the high-impedance (Hi-Z) state when in $\overline{\text{STANDBY}}$.

This pin has a 100-kΩ internal pulldown resistor.

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10.4 Device Functional Modes

10.4.1 Operating Modes and Faults

The operating modes and faults are listed in the following tables.

表 5. Operating Modes

STATE NAME	OUTPUT FETS	OSCILLATOR	I^2C
STANDBY	Hi-Z	Stopped	Stopped
Hi-Z	Hi-Z	Active	Active
MUTE	Switching at 50%	Active	Active
PLAY	Switching with audio	Active	Active

表 6. Global Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION RESULT
POR	Voltage fault	All	I^2C + $\overline{WARN}$ pin	Standby
VBAT UV		Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin	Hi-Z
PVDD UV				
VBAT or PVDD OV				
OTW	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{WARN}$ pin	None
OTSD	Thermal shutdown	Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin	Hi-Z

表 7. Channel Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE
Clipping	Warning	Mute and play	$\overline{WARN}$ pin	None
Overcurrent limiting	Protection			Current limit
Overcurrent fault	Output channel fault		I^2C + $\overline{FAULT}$ pin	Hi-Z
DC detect				

10.5 Programming

10.5.1 I^2C Serial Communication Bus

The device communicates with the system processor through the I^2C serial communication bus as an I^2C slave-only device. The processor can poll the device through I^2C to determine the operating status, configure settings, or run diagnostics. For a complete list and description of all I^2C controls, see the *Register Maps* section.

The device includes two I^2C address pins, so up to four devices can be used together in a system with no additional bus switching hardware. The I^2C ADDRx pins set the slave address of the device as listed in 表 8.

表 8. I^2C Addresses

DESCRIPTION	I^2C ADDR1	I^2C ADDR0	I^2C Write	I^2C Read
Device 0	0	0	0xD4	0xD5
Device 1	0	1	0xD6	0xD7
Device 2	1	0	0xD8	0xD9
Device 3	1	1	0xDA	0xDB

10.5.2 I^2C Bus Protocol

The device has a bidirectional serial-control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 100-kbps and 400-kbps data transfer rates for random and sequential write and read operations. The TAS6424-Q1 device is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

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The I²C bus uses two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. The number of bytes that can be transmitted between start and stop conditions is unlimited. When the last word transfers, the master generates a stop condition to release the bus.

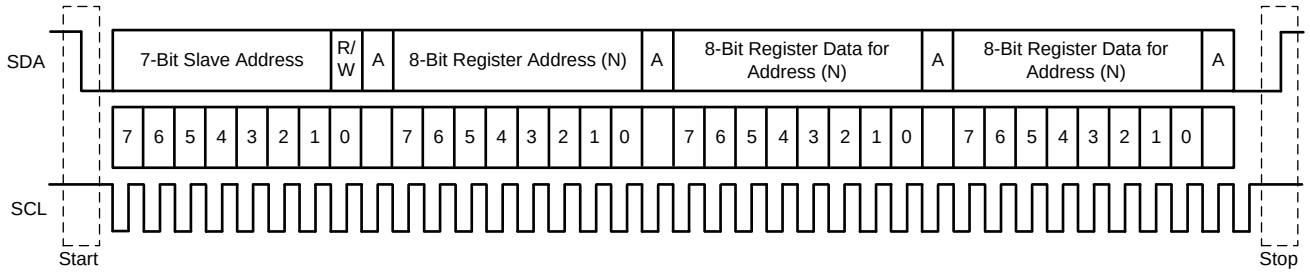

図 41. Typical I²C Sequence

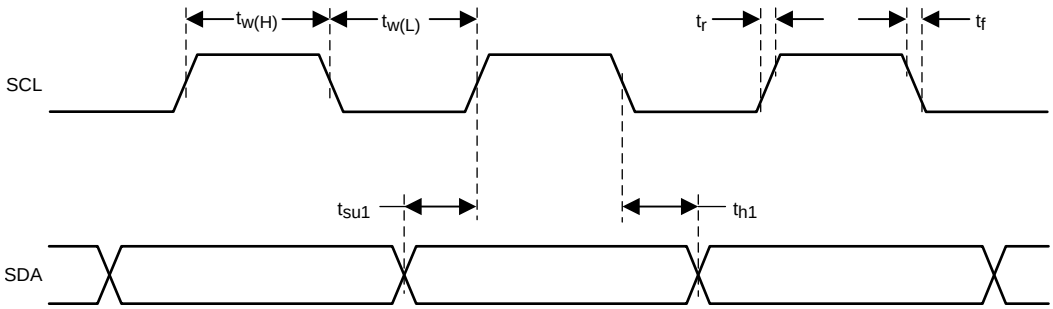

図 42. SCL and SDA Timing

Use the I²C ADDRx pins to program the device slave address. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

10.5.3 Random Write

As shown in 図 43, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. The R/W bit determines the direction of the data transfer. For a write data transfer, the R/W bit is a 0. After receiving the correct I²C device address and the R/W bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

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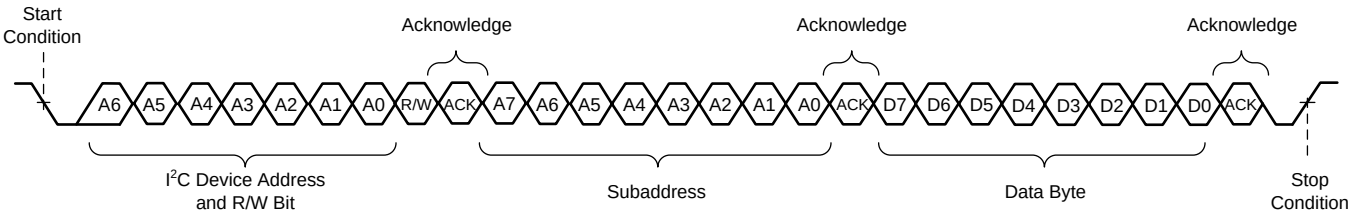

図 43. Random Write Transfer

10.5.4 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in 図 44. After receiving each data byte, the device responds with an acknowledge bit and the I^{2}C subaddress is automatically incremented by one.

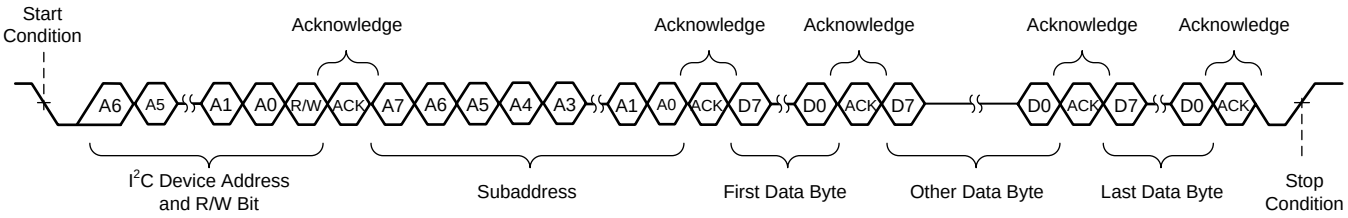

図 44. Sequential Write Transfer

10.5.5 Random Read

As shown in 図 45, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the R/W bit. For the data-read transfer, both a write followed by a read occur. Initially, a write occurs to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/W bit is a 0. After receiving the address and the R/W bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the address and the R/W bit again. This time the R/W bit is a 1, indicating a read transfer. After receiving the address and the R/W bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

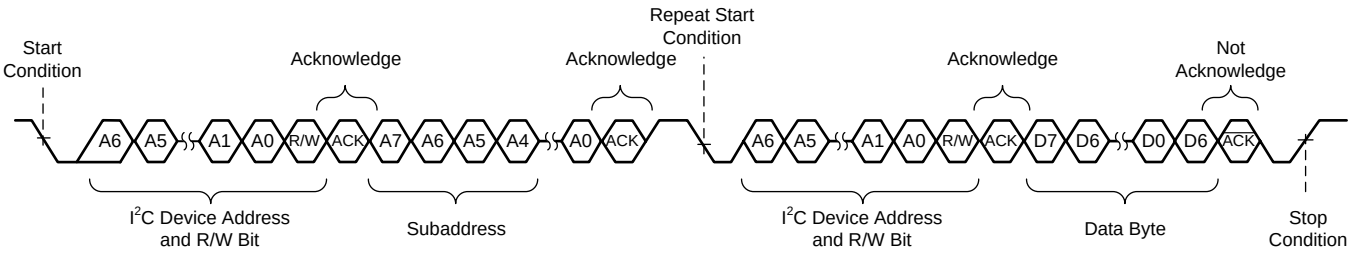

図 45. Random Read Transfer

10.5.6 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in 図 46. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^{2}C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge bit followed by a stop condition to complete the transfer.

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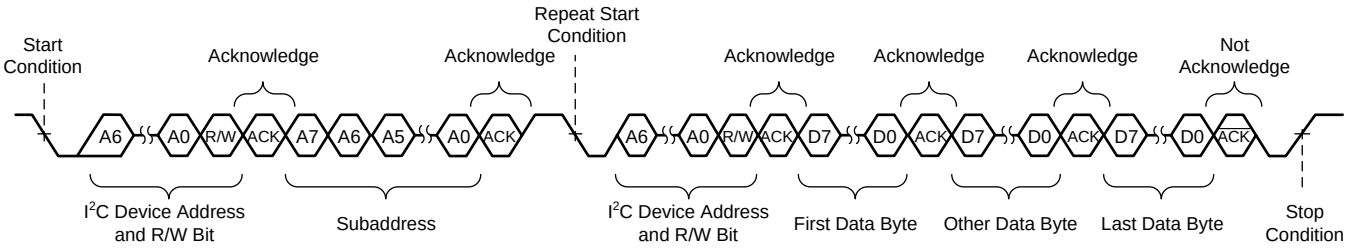

図 46. Sequential Read Transfer

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10.6 Register Maps

表 9. I²C Address Register Definitions

Address	Type	Register Description	Section
0x00	R/W	Mode control	Go
0x01	R/W	Miscellaneous control 1	Go
0x02	R/W	Miscellaneous control 2	Go
0x03	R/W	SAP control (serial audio-port control)	Go
0x04	R/W	Channel state control	Go
0x05	R/W	Channel 1 volume control	Go
0x06	R/W	Channel 2 volume control	Go
0x07	R/W	Channel 3 volume control	Go
0x08	R/W	Channel 4 volume control	Go
0x09	R/W	DC diagnostic control 1	Go
0x0A	R/W	DC diagnostic control 2	Go
0x0B	R/W	DC diagnostic control 3l	Go
0x0C	R	DC load diagnostic report 1 (channels 1 and 2)	Go
0x0D	R	DC load diagnostic report 2 (channels 3 and 4)	Go
0x0E	R	DC load diagnostic report 3—line output	Go
0x0F	R	Channel state reporting	Go
0x10	R	Channel faults (overcurrent, DC detection)	Go
0x11	R	Global faults 1	Go
0x12	R	Global faults 2	Go
0x13	R	Warnings	Go
0x14	R/W	Pin control	Go
0x15	R/W	AC load diagnostic control 1	Go
0x16	R/W	AC load diagnostic control 2	Go
0x17	R	AC load diagnostic report channel 1	Go
0x18	R	AC load diagnostic report channel 2	Go
0x19	R	AC load diagnostic report channels 3	Go
0x1A	R	AC load diagnostic report channels 4	Go
0x1B	R	AC load diagnostic phase report high	Go
0x1C	R	AC load diagnostic phase report low	Go
0x1D	R	AC load diagnostic STI report high	Go
0x1E	R	AC load diagnostic STI report low	Go
0x1F	R	RESERVED	
0x20	R	RESERVED	
0x21	R/W	Miscellaneous control 3	Go
0x22	R/W	Clip control	Go
0x23	R/W	Clip window	Go
0x24	R/W	Clip warning	Go
0x25	R/W	ILIMIT status	Go
0x26	R/W	Miscellaneous control 4	Go
0x27	R	RESERVED	
0x28	R/W	RESERVED	

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10.6.1 Mode Control Register (address = 0x00) [default = 0x00]

The Mode Control register is shown in 図 47 and described in 表 10.

図 47. Mode Control Register

7	6	5	4	3	2	1	0
RESET	RESERVED	PBTL CH34	PBTL CH12	CH1 LO MODE	CH2 LO MODE	CH3 LO MODE	CH4 LO MODE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 10. Mode Control Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0	**0: Normal operation** 1: Resets the device
6	RESERVED	R/W	0	RESERVED
5	PBTL CH34	R/W	0	**0: Channels 3 and 4 are in BTL mode** 1: Channels 3 and 4 are in parallel BTL mode
4	PBTL CH12	R/W	0	**0: Channels 1 and 2 are in BTL mode** 1: Channels 1 and 2 are in parallel BTL mode
3	CH1 LO MODE	R/W	0	**0: Channel 1 is in normal/speaker mode** 1: Channel 1 is in line output mode
2	CH2 LO MODE	R/W	0	**0: Channel 2 is in normal/speaker mode** 1: Channel 2 is in line output mode
1	CH3 LO MODE	R/W	0	**0: Channel 3 is in normal/speaker mode** 1: Channel 3 is in line output mode
0	CH4 LO MODE	R/W	0	**0: Channel 4 is in normal/speaker mode** 1: Channel 4 is in line output mode

10.6.2 Miscellaneous Control 1 Register (address = 0x01) [default = 0x32]

The Miscellaneous Control 1 register is shown in 図 48 and described in 表 11.

図 48. Miscellaneous Control 1 Register

7	6	5	4	3	2	1	0
HPF BYPASS	OTW CONTROL		OC CONTROL	VOLUME RATE		GAIN	
R/W-0	R/W-01		R/W-1	R/W-00		R/W-10	

表 11. Misc Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	HPF BYPASS	R/W	0	**0: High pass filter eneabled** 1: High pass filter disabled
6–5	OTW CONTROL	R/W	01	00: Global overtemperature warning set to 140°C **01: Global overtemperature warning set to 130C** 10: Global overtemperature warning set to 120°C 11: Global overtemperature warning set to 110°C
4	OC CONTROL	R/W	1	0: Overcurrent is level 1 **1: Overcurrent is level 2**
3–2	VOLUME RATE	R/W	00	**00: Volume update rate is 1 step / FSYNC** 01: Volume update rate is 1 step / 2 FSYNCs 10: Volume update rate is 1 step / 4 FSYNCs 11: Volume update rate is 1 step / 8 FSYNCs

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表 11. Misc Control 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1–0	GAIN	R/W	10	00: Gain level 1 = 7.6-V peak output voltage 01: Gain Level 2 = 15-V peak output voltage **10: Gain Level 3 = 21-V peak output voltage** 11: Gain Level 4 = 29-V peak output voltage

10.6.3 Miscellaneous Control 2 Register (address = 0x02) [default = 0x62]

The Miscellaneous Control 2 register is shown in 図 49 and described in 表 12.

図 49. Miscellaneous Control 2 Register

7	6	5	4	3	2	1	0
RESERVED	PWM FREQUENCY			RESERVED	SDM_OSR	OUTPUT PHASE	
R/W-110					R/W-0	R/W-10	

表 12. Misc Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED			**0**
6–4	PWM FREQUENCY	R/W	110	000: 8 × f_S (352.8 kHz / 384 kHz) 001: 10 × f_S (441 kHz / 480 kHz) 010: RESERVED 011: RESERVED 100: RESERVED 101: 38 × f_S (1.68 MHz / 1.82 MHz) **110: 44 × f_S (1.94 MHz / 2.11 MHz)** 111: 48 × f_S (2.12 MHz / not supported)
3	RESERVED		0	**0**
2	SDM_OSR	R/W	0	**0: 64x OSR** 1: 128x OSR
1–0	OUTPUT PHASE	R/W	10	00: 0 degrees output-phase switching offset 01: 30 degrees output-phase switching offset **10: 45 degrees output-phase switching offset** 11: 60 degrees output-phase switching offset

10.6.4 SAP Control (Serial Audio-Port Control) Register (address = 0x03) [default = 0x04]

The SAP Control (serial audio-port control) register is shown in 図 50 and described in 表 13.

図 50. SAP Control Register

7	6	5	4	3	2	1	0
INPUT SAMPLING RATE		8 Ch TDM SLOT SELECT	TDM SLOT SIZE	TDM SLOT SELECT 2	INPUT FORMAT		
R/W-00		R/W-0	R/W-0	R/W-0	R/W-100		

表 13. SAP Control Field Descriptions

Bit	Field	Type	Reset	Description
7–6	INPUT SAMPLING RATE	R/W	00	**00: 44.1 kHz** 01: 48 kHz 10: 96 kHz 11: RESERVED

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表 13. SAP Control Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	8 Ch TDM SLOT SELECT	R/W	0	**0: First four TDM slots** 1: Last four TDM slots
4	TDM SLOT SIZE	R/W	0	**0: TDM slot size is 24-bit or 32-bit** 1: TDM slot size is 16-bit
3	TDM SLOT SELECT 2	R/W	0	**0: Normal** 1: swap channel 1/2 with channel 3/4
2–0	INPUT FORMAT	R/W	100	000: 24-bit right justified 001: 20-bit right justified 010: 18-bit right justified 011: 16-bit right justified **100: I^2S (16-bit or 24-bit)** 101: Left justified (16-bit or 24-bit) 110: TDM mode (16-bit or 24-bit) 111: RESERVED

10.6.5 Channel State Control Register (address = 0x04) [default = 0x55]

The Channel State Control register is shown in 図 51 and described in 表 14.

図 51. Channel State Control Register

7	6	5	4	3	2	1	0
CH1 STATE CONTROL		CH2 STATE CONTROL		CH3 STATE CONTROL		CH4 STATE CONTROL	
R/W-01		R/W-01		R/W-01		R/W-01	

表 14. Channel State Control Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	CH3 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
1–0	CH4 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics

10.6.6 Channel 1 Through 4 Volume Control Registers (address = 0x05–0x088) [default = 0xCF]

The Channel 1 Through 4 Volume Control registers are shown in 図 52 and described in 表 15.

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図 52. Channel x Volume Control Register

7	6	5	4	3	2	1	0
CH x VOLUME							
R/W-CF							

表 15. Ch x Volume Control Field Descriptions

Bit	Field	Type	Reset	Description
7–0	CH x VOLUME	R/W	CF	8-Bit Volume Control for each channel, register address for Ch1 is 0x05, Ch2 is 0x06, Ch3 is 0x07 and Ch4 is 0x08, 0.5 dB/step: 0xFF: 24 dB **0xCF: 0 dB** 0x07: –100 dB < 0x07: MUTE

10.6.7 DC Load Diagnostic Control 1 Register (address = 0x09) [default = 0x00]

The DC Diagnostic Control 1 register is shown in 図 53 and described in 表 16.

図 53. DC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
DC LDG ABORT	2x_RAMP	2x_SETTLE	RESERVED			LDG LO ENABLE	LDG BYPASS
R/W-0	R/W-0	R/W-0				R/W-0	R/W-0

表 16. DC Load Diagnostics Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	DC LDG ABORT	R/W	0	**0: Default state, clear after abort** 1: Aborts the load diagnostics in progress
6	2x_RAMP	R/W	0	**0: Normal ramp time** 1: Double ramp time
5	2x_SETTLE	R/W	0	**0: Normal Settle time** 1: Double setling time
4–2	RESERVED		0	**0**
1	LDG LO ENABLE	R/W	0	**0: Line output diagnostics are disabled** 1: Line output diagnostics are enabled
0	LDG BYPASS	R/W	0	**0: Automatic diagnostics when leaving Hi-Z and after channel fault** 1: Diagnostics are not run automatically

10.6.8 DC Load Diagnostic Control 2 Register (address = 0x0A) [default = 0x11]

The DC Diagnostic Control 2 register is shown in 図 54 and described in 表 17.

図 54. DC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
CH1 DC LDG SL				CH2 DC LDG SL			
R/W-0001				R/W-0001			

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表 17. DC Load Diagnostics Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CH1 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3–0	CH2 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

10.6.9 DC Load Diagnostic Control 3 Register (address = 0x0B) [default = 0x11]

The DC Diagnostic Control 3 register is shown in 図 55 and described in 表 18.

図 55. DC Load Diagnostic Control 3 Register

7	6	5	4	3	2	1	0
CH3 DC LDG SL				CH4 DC LDG SL			
R/W-0001				R/W-0001			

表 18. DC Load Diagnostics Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CH3 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3–0	CH4 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

10.6.10 DC Load Diagnostic Report 1 Register (address = 0x0C) [default = 0x00]

DC Load Diagnostic Report 1 register is shown in 図 56 and described in 表 19.

図 56. DC Load Diagnostic Report 1 Register

7	6	5	4	3	2	1	0
CH1 S2G	CH1 S2P	CH1 OL	CH1 SL	CH2 S2G	CH2 S2P	CH2 OL	CH2 SL
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

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表 19. DC Load Diagnostics Report 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 S2G	R	0	**0: No short-to-GND detected** 1: Short-To-GND Detected
6	CH1 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
5	CH1 OL	R	0	**0: No open load detected** 1: Open load detected
4	CH1 SL	R	0	**0: No shorted load detected** 1: Shorted load detected
3	CH2 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
2	CH2 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
1	CH2 OL	R	0	**0: No open load detected** 1: Open load detected
0	CH2 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

10.6.11 DC Load Diagnostic Report 2 Register (address = 0x0D) [default = 0x00]

The DC Load Diagnostic Report 2 register is shown in 図 57 and described in 表 20.

図 57. DC Load Diagnostic Report 2 Register

7	6	5	4	3	2	1	0
CH3 S2G	CH3 S2P	CH3 OL	CH3 SL	CH4 S2G	CH4 S2P	CH4 OL	CH4 SL
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 20. DC Load Diagnostics Report 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
6	CH3 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
5	CH3 OL	R	0	**0: No open load detected** 1: Open load detected
4	CH3 SL	R	0	**0: No shorted load detected** 1: Shorted load detected
3	CH4 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
2	CH4 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
1	CH4 OL	R	0	**0: No open load detected** 1: Open load detected
0	CH4 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

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10.6.12 DC Load Diagnostics Report 3—Line Output—Register (address = 0x0E) [default = 0x00]

The DC Load Diagnostic Report, Line Output, register is shown in 図 58 and described in 表 21.

図 58. DC Load Diagnostics Report 3—Line Output—Register

7	6	5	4	3	2	1	0
RESERVED				CH1 LO LDG	CH2 LO LDG	CH3 LO LDG	CH4 LO LDG
				R-0	R-0	R-0	R-0

表 21. DC Load Diagnostics Report 3—Line Output—Field Descriptions

Bit	Field	Type	Reset	Description
7–4	RESERVED			**0**
3	CH1 LO LDG	R	0	**0: No line output detected on channel 1** 1: Line output detected on channel 1
2	CH2 LO LDG	R	0	**0: No line output detected on channel 2** 1: Line output detected on channel 2
1	CH3 LO LDG	R	0	**0: No line output detected on channel 3** 1: Line output detected on channel 3
0	CH4 LO LDG	R	0	**0: No line output detected on channel 4** 1: Line output detected on channel 3

10.6.13 Channel State Reporting Register (address = 0x0F) [default = 0x55]

The Channel State Reporting register is shown in 図 59 and described in 表 22.

図 59. Channel State-Reporting Register

7	6	5	4	3	2	1	0
CH1 STATE REPORT		CH2 STATE REPORT		CH3 STATE REPORT		CH3 STATE REPORT	
R-01		R-01		R-01		R-01	

表 22. State-Reporting Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	CH3 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
1–0	CH4 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics

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10.6.14 Channel Faults (Overcurrent, DC Detection) Register (address = 0x10) [default = 0x00]

The Channel Faults (overcurrent, DC detection) register is shown in 図 60 and described in 表 23.

図 60. Channel Faults Register

7	6	5	4	3	2	1	0
CH1 OC	CH2 OC	CH3 OC	CH4 OC	CH1 DC	CH2 DC	CH3 DC	CH4 DC
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

表 23. Channel Faults Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
6	CH2 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
5	CH3 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
4	CH4 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
3	CH1 DC	R	0	**0: No DC fault detected** 1: DC fault detected
2	CH2 DC	R	0	**0: No DC fault detected** 1: DC fault detected
1	CH3 DC	R	0	**0: No DC fault detected** 1: Overcurrent fault detected
0	CH4 DC	R	0	**0: No DC fault detected** 1: Overcurrent fault detected

10.6.15 Global Faults 1 Register (address = 0x11) [default = 0x00]

The Global Faults 1 register is shown in 図 61 and described in 表 24.

図 61. Global Faults 1 Register

7	6	5	4	3	2	1	0
RESERVED			INVALID CLOCK	PVDD OV	VBAT OV	PVDD UV	VBAT UV
			R-0	R-0	R-0	R-0	R-0

表 24. Global Faults 1 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED		0	**0**
4	INVALID CLOCK	R	0	**0: No clock fault detected** 1: Clock fault detected
3	PVDD OV	R	0	**0: No PVDD overvoltage fault detected** 1: PVDD overvoltage fault detected
2	VBAT OV	R	0	**0: No VBAT overvoltage fault detected** 1: VBAT overvoltage fault detected
1	PVDD UV	R	0	**0: No PVDD undervoltage fault detected** 1: PVDD undervoltage fault detected

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表 24. Global Faults 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VBAT UV	R	0	**0: No VBAT undervoltage fault detected** 1: VBAT undervoltage fault detected

10.6.16 Global Faults 2 Register (address = 0x12) [default = 0x00]

The Global Faults 2 register is shown in 図 62 and described in 表 25.

図 62. Global Faults 2 Register

7	6	5	4	3	2	1	0
RESERVED			OTSD	CH1 OTSD	CH2 OTSD	CH3 OTSD	CH4 OTSD
			R-0	R-0	R-0	R-0	R-0

表 25. Global Faults 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED			**0**
4	OTSD	R	0	**0: No global overtemperature shutdown** 1: Global overtemperature shutdown
3	CH1 OTSD	R	0	**0: No overtemperature shutdown on Ch1** 1: Overtemperature shutdown on Ch1
2	CH2 OTSD	R	0	**0: No overtemperature shutdown on Ch2** 1: Overtemperature shutdown on Ch2
1	CH3 OTSD	R	0	**0: No overtemperature shutdown on Ch4** 1: Overtemperature shutdown on Ch4
0	CH4 OTSD	R	0	**0: No overtemperature shutdown on Ch4** 1: Overtemperature shutdown on Ch4

10.6.17 Warnings Register (address = 0x13) [default = 0x20]

The Warnings register is shown in 図 63 and described in 表 26.

図 63. Warnings Register

7	6	5	4	3	2	1	0
RESERVED		VDD POR	OTW	OTW CH1	OTW CH2	OTW CH3	OTW CH4
		R-0	R-0	R-0	R-0	R-0	R-0

表 26. Warnings Field Descriptions

Bit	Field	Type	Reset	Description
7 -6	RESERVED		00	**0**
5	VDD POR	R	0	0: No VDD POR has occurred **1 VDD POR occurred**
4	OTW	R	0	**0: No global overtemperature warning** 1: Global overtemperature warning
3	OTW CH1	R	0	**0: No overtemperature warning on channel 1** 1: Overtemperature warning on channel 1
2	OTW CH2	R	0	**0: No overtemperature warning on channel 2** 1: Overtemperature warning on channel 2

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表 26. Warnings Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OTW CH4	R	0	**0: No overtemperature warning on channel 4** 1: Overtemperature warning on channel 4
0	OTW CH4	R	0	**0: No overtemperature warning on channel 4** 1: Overtemperature warning on channel 4

10.6.18 Pin Control Register (address = 0x14) [default = 0xFF]

The Pin Control register is shown in 図 64 and described in 表 27.

図 64. Pin Control Register

7	6	5	4	3	2	1	0
MASK OC	MASK OTSD	MASK UV	MASK OV	MASK DC	MASK ILIMIT	MASK CLIP	MASK OTW
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

表 27. Pin Control Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK OC	R/W	1	0: Do not report overcurrent faults on the $\overline{\text{FAULT}}$ pin **1: Report overcurrent faults on the $\overline{\text{FAULT}}$ Pin**
6	MASK OTSD	R/W	1	0: Do not report overtemperature faults on the $\overline{\text{FAULT}}$ pin **1: Report overtemperature faults on the $\overline{\text{FAULT}}$ pin**
5	MASK UV	R/W	1	0: Do not report overvoltage faults on the $\overline{\text{FAULT}}$ pin **1: Report overvoltage faults on the $\overline{\text{FAULT}}$ pin**
4	MASK OV	R/W	1	0: Do not report undervoltage faults on the $\overline{\text{FAULT}}$ pin **1: Report undervoltage faults on the $\overline{\text{FAULT}}$ pin**
3	MASK DC	R/W	1	0: Do not report DC faults on the $\overline{\text{FAULT}}$ pin **1: Report DC faults on the $\overline{\text{FAULT}}$ pin**
2	MASK ILIMIT	R/W	1	0: Do not report Ilimit on the $\overline{\text{FAULT}}$ pin **1: Report Ilimit on the $\overline{\text{FAULT}}$ pin**
1	MASK CLIP	R/W	1	0: Do not report clipping on the $\overline{\text{WARN}}$ pin **1: Report clipping on the $\overline{\text{WARN}}$ pin**
0	MASK OTW	R/W	1	0: Do not report overtemperature warnings on the $\overline{\text{WARN}}$ pin **1: Report overtemperature warnings on the $\overline{\text{WARN}}$ pin**

10.6.19 AC Load Diagnostic Control 1 Register (address = 0x15) [default = 0x00]

The AC Load Diagnostic Control 1 register is shown in 図 65 and described in 表 28.

図 65. AC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
CH1 GAIN	RESERVED	CH3 GAIN	RESERVED	CH1 ENABLE	CH2 ENABLE	CH3 ENABLE	CH4 ENABLE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 28. AC Load Diagnostic Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1, CH2, PBTL12: GAIN	R/W	0	**0: Gain 1** 1: Gain 4
6	RESERVED	R/W	0	0

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表 28. AC Load Diagnostic Control 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH3, CH4, PBTL34: GAIN	R/W	0	**0: Gain 1** 1: Gain 4
4	RESERVED	R/W	0	0
3	CH1 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
2	CH2 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
1	CH3 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
0	CH4 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics

10.6.20 AC Load Diagnostic Control 2 Register (address = 0x16) [default = 0x00]

The AC Load Diagnostic Control 1 register is shown in 図 65 and described in 表 28.

図 66. AC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
AC_DIAGS_LOOPBACK	RESERVED		AC TIMING	AC CURRENT		RESERVED	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 29. AC Load Diagnostic Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	AC_DIAGS_LOOPBACK	R/W	0	**0: disable AC Diag loopback** 1: Enable AC Diag loopback
6-5	RESERVED	R/W	00	**00**
4	AC TIMING	R/W	0	**0: 32 Cycles** 1: 64 Cycles
3-2	AC CURRENT	R/W	00	**00: 10mA** 01: 19 mA 10: RESERVED 11: RESERVED
1-0	RESERVED	R/W	00	**00**

10.6.21 AC Load Diagnostic Impedance Report Ch1 through CH4 Registers (address = 0x17–0x1A) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in 図 67 and described in 表 30.

図 67. AC Load Diagnostic Impedance Report Chx Register

7	6	5	4	3	2	1	0
CHx IMPEDANCE							
R-00							

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表 30. Chx AC LDG Impedance Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	CH x IMPEDANCE	R	00	8-bit AC-load diagnostic report for each channel with a step size of 0.2496 Ω/bit (control by register 0x15 and register 0x16) **0x00: 0 Ω** 0x01: 0.2496 Ω ... 0xFF: 63.65 Ω

10.6.22 AC Load Diagnostic Phase Report High Register (address = 0x1B) [default = 0x00]

The AC Load Diagnostic Phase High value registers are shown in 図 68 and described in 表 31.

図 68. AC Load Diagnostic (LDG) Phase High Report Register

7	6	5	4	3	2	1	0
AC Phase High							
R-00							

表 31. AC LDG Phase High Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC Phase High	R	00	Bit 15:8

10.6.23 AC Load Diagnostic Phase Report Low Register (address = 0x1C) [default = 0x00]

The AC Load Diagnostic Phase Low value registers are shown in 図 69 and described in 表 32.

図 69. AC Load Diagnostic (LDG) Phase Low Report Register

7	6	5	4	3	2	1	0
AC Phase Low							
R-00							

表 32. AC LDG Phase Low Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC Phase Low	R	00	Bit 7:0

10.6.24 AC Load Diagnostic STI Report High Register (address = 0x1D) [default = 0x00]

The AC Load Diagnostic STI High value registers are shown in 図 70 and described in 表 33.

図 70. AC Load Diagnostic (LDG) STI High Report Register

7	6	5	4	3	2	1	0
AC STI High							
R-00							

表 33. AC LDG STI High Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC STI High	R	00	Bit 15:8

10.6.25 AC Load Diagnostic STI Report Low Register (address = 0x1C) [default = 0x00]

The AC Load Diagnostic STI Low value registers are shown in 図 67 and described in 表 34.

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図 71. AC Load Diagnostic (LDG) STI Low Report Register

7	6	5	4	3	2	1	0
AC STI Low							
R-00							

表 34. Chx AC LDG STI Low Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC STI Low	R	00	Bit 7:0

10.6.26 Miscellaneous Control 3 Register (address = 0x21) [default = 0x00]

The Miscellaneous Control 3 register is shown in 図 73 and described in 表 35.

図 72. Miscellaneous Control 3 Register

7	6	5	4	3	2	1	0
CLEAR FAULT	PBTL_CH_SEL	MASK ILIMIT WARNING	RESERVED	OTSD AUTO RECOVERY	RESERVED		
R/W-0	R/W-0	R/W-0	R/W-1	R/W-0			

表 35. Misc Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	CLEAR FAULT	R/W	0	**0: Normal operation** 1: Clear fault
6	PBTL_CH_SEL	R/W	0	**0: PBTL normal signal source** 1: PBTL flip signal source
5	MASK ILIMIT WARNING	R/W	0	**0: Report ILIMIT on the $\overline{\text{WARN}}$ pin** 1: Do not report ILIMIT on the $\overline{\text{WARN}}$ pin
4	RESERVED	R/W	0	0
3	OTSD AUTO RECOVERY	R/W	0	**0: Report overtemperature faults on the $\overline{\text{FAULT}}$ pin** 0: Automatic temperature protection recovery. Do not report overtemperature faults on the $\overline{\text{FAULT}}$ pin
2–0	RESERVED		0	**0**

10.6.27 Clip Control Register (address = 0x22) [default = 0x01]

The Clip Detect register is shown in 図 73 and described in 表 36.

図 73. Clip Control Register

7	6	5	4	3	2	1	0
RESERVED							CLIPDET_EN
							R/W-1

表 36. Clip Control Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED			**0**
0	CLIPDET_EN	R/W	1	0: Clip detect disable **1: Clip Detect Enable**

10.6.28 Clip Window Register (address = 0x23) [default = 0x14]

The Clip Window register is shown in 図 74 and described in 表 37.

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図 74. Clip Window Register

7	6	5	4	3	2	1	0
CLIP_WINDOW_SEL[7:1]							
R/W-00001110							

表 37. Clip Window Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLIP_WINDOW_SEL[7:1]	R/W	00010100	00000000 00000001 00000010 00000011 00000100 00000101 00000110 00000111 00001000 00001001 00001010 00001110 00010100

10.6.29 Clip Warning Register (address = 0x24) [default = 0x00]

The Clip Window register is shown in 図 75 and described in 表 38.

図 75. Clip Warning Register

7	6	5	4	3	2	1	0
RESERVED				CH4_CLIP	CH4_CLIP	CH2_CLIP	CH1_CLIP
				R-0	R-0	R-0	R-0

表 38. Clip Warning Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED		0	**0**
3	CH4_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
2	CH3_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
1	CH2_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
0	CH1_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect

10.6.30 ILIMIT Status Register (address = 0x25) [default = 0x00]

The ILIMIT Status register is shown in 図 76 and described in 表 39.

図 76. ILIMIT Status Register

7	6	5	4	3	2	1	0
RESERVED				CH4_ILIMIT_WARN	CH3_ILIMIT_WARN	CH2_ILIMIT_WARN	CH1_ILIMIT_WARN
				R-0	R-0	R-0	R-0

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表 39. ILIMIT Status Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED		0	0
6	RESERVED		0	0
5	RESERVED		0	0
4	RESERVED		0	0
3	CH4_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning
2	CH3_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning
1	CH2_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning
0	CH1_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning

10.6.31 Miscellaneous Control 4 Register (address = 0x26) [default = 0x40]

The Miscellaneous Control 4 register is shown in 図 77 and described in 表 40.

図 77. Miscellaneous Control 4 Register

7	6	5	4	3	2	1	0
RESERVED					HPF_CORNER[2:0]		
R/W-00000					R/W-000		

表 40. Misc Control 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	01000	**01000: DEFAULT**
2-0	HPF_CORNER[2:0]	R/W	000	**000: 3.7 Hz** 001: 7.4 Hz 010: 15 Hz 011: 30 Hz 100: 59 Hz 101: 118 Hz 110: 235 Hz 111: 463 Hz

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11 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TAS6424-Q1 is a four-channel class-D digital-input audio-amplifier design for use in automotive head units and external amplifier modules. The TAS6424-Q1 incorporates the necessary functionality to perform in demanding OEM applications.

11.1.1 AM-Radio Band Avoidance

AM-radio frequency interference can be avoided by setting the switching frequency of the device above the AM band. The switching frequency options available are 38 f_s, 44 f_s, and 48 f_s. If the switch frequency cannot be set above the AM band, then use the two options of 8 f_s and 10 f_s. These options should be changed to avoid AM active channels.

11.1.2 Parallel BTL Operation (PBTL)

The device can drive more current-paralleling BTL channels on the load side of the LC output filter. For parallel operation, the parallel BTL mode, PBTL, must be used and the paralleled channels must have the same state in the state control register. If the two states are not aligned the device reports a fault condition.

To set the requested channels to PBTL mode the device must be in standby mode for the commands to take effect.

A load diagnostic is supported for PBTL channels. Paralleling on the device side of the LC output filter is not supported.

11.1.3 Demodulation Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. An LC demodulation filter is used to recover the audio signal. The filter attenuates the high-frequency components of the output signals that are out of the audio band. The design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, the selection of the inductors used in the output filter should be carefully considered.

11.1.4 Line Driver Applications

In many automotive audio applications, the same head unit must drive either a speaker (with several ohms of impedance) or an external amplifier input (with several kiloohms of impedance). The design is capable of supporting both applications and has special line-drive gain and diagnostics. Coupled with the high switching frequency, the device is well suited for this type of application. Set the desired channel in line driver mode through I^2C register 0x00, the externally connected amplifier must have a differential impedance from 600 Ω to 4.7 kΩ for the DC line diagnostic to detect the connected external amplifier. 図 78 shows the recommended external amplifier input configuration.

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Application Information (continued)

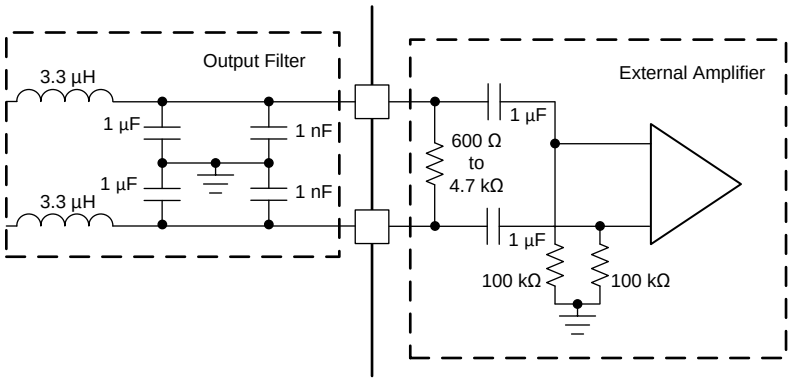

図 78. External Amplifier Input Configuration for Line Driver

11.2 Typical Applications

11.2.1 BTL Application

図 79 shows the schematic of a typical 4-channel solution for a head-unit application.

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Typical Applications (continued)

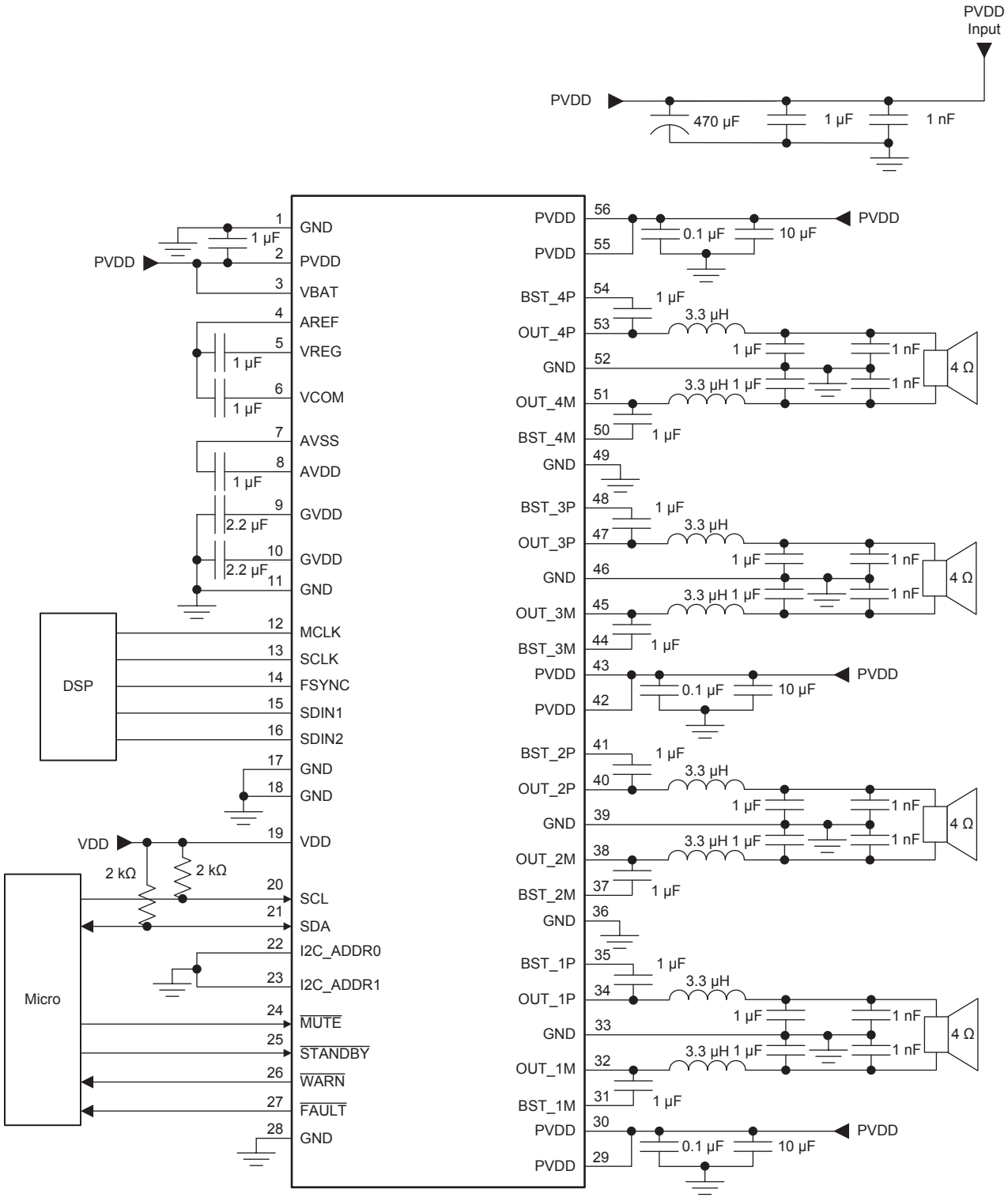

図 79. Typical 4-Channel BTL Application Schematic

Typical Applications (continued)

11.2.1.1 Design Requirements

Use the following requirements for this design:

- This head-unit example is focused on the smallest solution size for 4 × 50-W output power into 2 Ω with a battery supply of 14.4 V.
- The switching frequency is set above the AM-band with 44 times the input sample rate of 48 kHz which results in a frequency of 2.11 MHz.
- The selection of a 2.11-MHz switch frequency enables the use of a small output inductor value of 3.3 µH which leads to a very small solution size.

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11.2.1.2 Power Supplies

The TAS6424-Q1 requires three power supplies. The PVDD supply is the high-current supply in the recommended supply range. The VBAT supply is lower current supply that must be in the recommended supply range. The PVDD and VBAT pins can be connected to the same supply if the recommended supply range for VBAT is maintained. The VDD supply is the 3.3-Vdc logic supply and must be maintained in the tolerance as shown in the *Recommended Operating Conditions* table.

11.2.1.3 Communication

All communications to the TAS6424-Q1 are through the I^2C protocol. A system controller can communicate with the device through the SDA pins and SCL pins. The TAS6424-Q1 is an I^2C slave device and requires a master. The device cannot generate an I^2C clock or initiate a transaction. The maximum clock speed accepted by the device is 400 kHz. If multiple TAS6424-Q1 devices are on the same I^2C bus, the I^2C address must be different for each device. Up to four TAS6424-Q1 devices can be on the same I^2C bus.

The I^2C bus is shared internally.

> **注**
> Complete any internal operations, such as load diagnostics, before reading the registers for the results.

11.2.1.4 Detailed Design Procedure

11.2.1.4.1 Hardware Design

Use the following procedure for the hardware design:

- Determine the input format. The input format can be either I^2S or TDM mode. The mode determines the correct pin connections and the I^2C register settings.
- Determine the power output that is required into the load. The power requirement determines the required power-supply voltage and current. The output reconstruction-filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in 図 79 for the input connections.

11.2.1.4.2 Digital Input and the Serial Audio Port

The TAS6424-Q1 device supports four different digital input formats which are: I^2S, Right Justified, Left Justified, and TDM mode. Depending on the format, the device can support 16-, 18-, 20-, 24-, and 32-bit data. The supported frequencies are 96 kHz, 48 kHz, and 44.1 kHz. Please see 表 13 for the I^2C register, SAP Control, for the complete matrix to set up the serial audio port.

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Typical Applications (continued)

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Bits 3, 4, and 5 in this register are ignored in all input formats except for TDM. Setting up all the control registers to the system requirements should be done before the device is placed in Mute mode or Play mode. After the registers are setup, use bit 7 in register 0x21 to clear any faults. Then read the fault registers to make sure no faults are present. When no faults are present, use register 0x04 to place the device properly into play mode.

11.2.1.4.3 Bootstrap Capacitors

The bootstrap capacitors provide the gate-drive voltage of the upper N-channel FET. These capacitors must be sized appropriately for the system specification. A special condition can occur where the bootstrap may sag if the capacitor is not sized accordingly. The special condition is just below clipping where the PWM is slightly less than 100% duty cycle with sustained low-frequency signals. Changing the bootstrap capacitor value to 2.2 µF for driving subwoofers that require frequencies below 30 Hz may be necessary.

11.2.1.4.4 Output Reconstruction Filter

The output FETs drive the amplifier outputs in an H-Bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a reconstruction filter that comprises a series inductor and a capacitor to ground on each output, generally called an LC filter. The LC filter attenuates the PWM frequency and reduces electromagnetic emissions, allowing the reconstructed audio signal to pass to the speakers. refer to the *Class-D LC Filter Design*, (SLOA119) for a detailed description of proper component description and design of the LC filter based upon the specified load and frequency response. The recommended low-pass cutoff frequency of the LC filter is dependent on the selected switching frequency. The low-pass cutoff frequency can be as high as 100 kHz for a PWM frequency of 2.1 MHz. At a PWM frequency of 384 kHz the low-pass cutoff frequency should be less than 40 kHz. Certain specifications must be understood for a proper inductor. The inductance value is given at zero current, but the TAS6424-Q1 device will have current. Use the inductance versus current curve for the inductor to make sure the inductance does not drop below 2 µH (for f_{SW} = 2.1 MHz) at the maximum current provided by the system design. The DCR of the inductor directly affects the output power of the system design. The lower the DCR, the more power is provided to the speakers. The typical inductor DCR for a 4-Ω system is 40 to 50 mΩ and for a 2-Ω system is 20 to 25 mΩ.

11.2.1.5 Application Curves

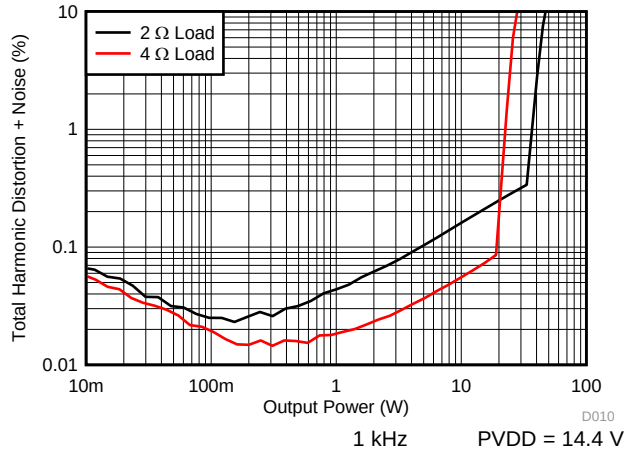

図 80. THD vs Output Power, 4R

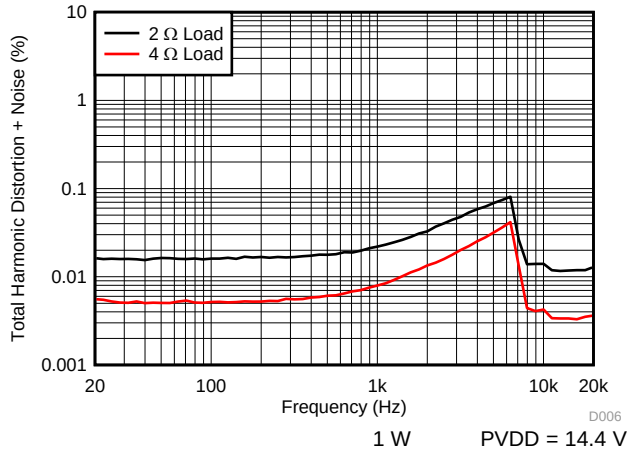

図 81. THD vs Frequency

11.2.2 PBTL Application

図 82 shows a schematic of a typical 2-channel solution for a head unit or external amplifier application where high power into 2 Ω is required.

Typical Applications (continued)

To operate in PBTL mode the output stage must be paralleled according to the schematic in 図 82. The device can operate in a mix of PBTL and BTL mode. This application can be set up for 3 channels, with one channel in PBTL mode and two channels in BTL mode. The device does not support a parallel configuration all four channels for a one-channel amplifier.

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Typical Applications (continued)

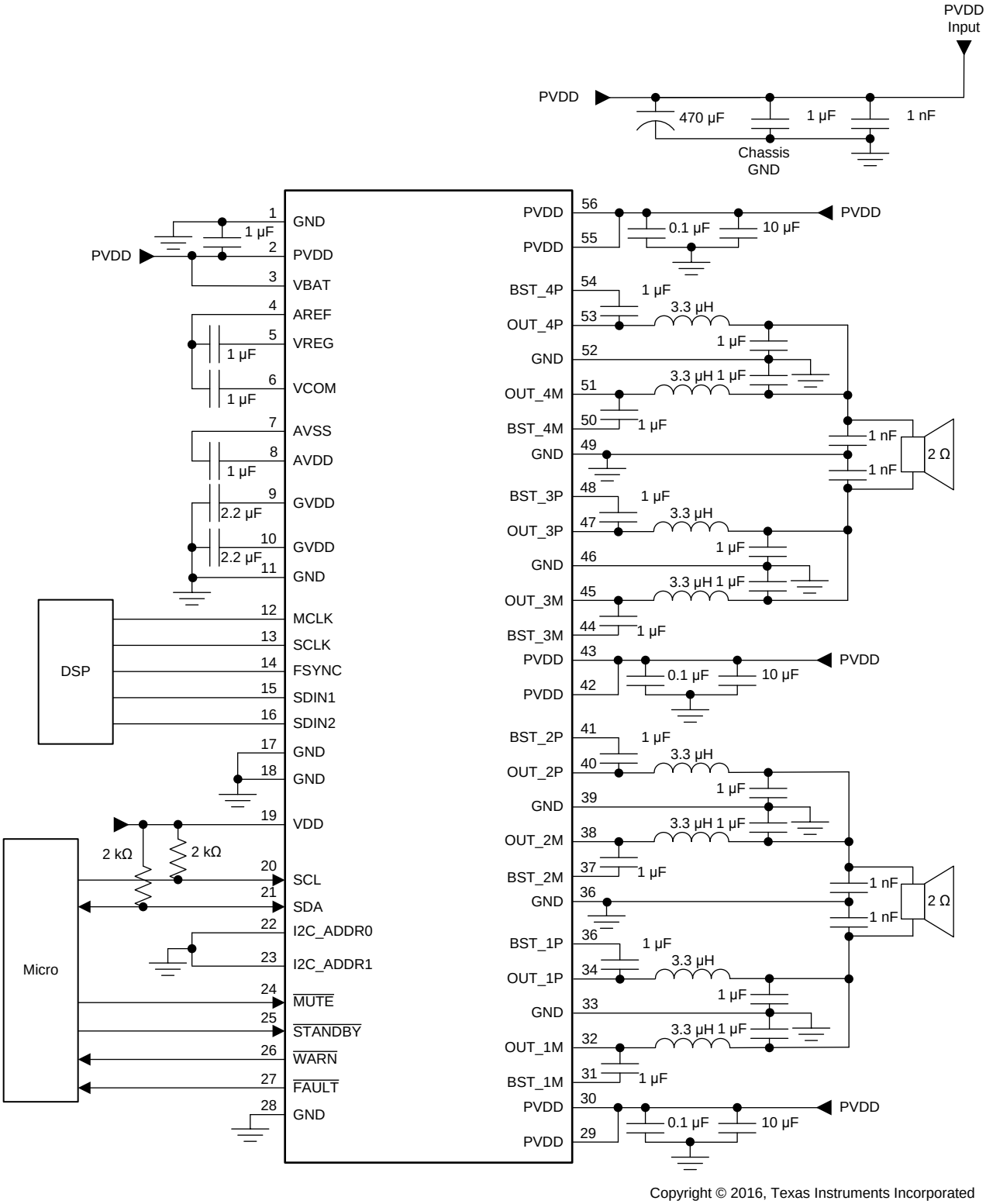

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図 82. 2-Channel PBTL Application Schematic

Typical Applications (continued)

11.2.2.1 Design Requirements

Use the following requirements for this design:

- This head-unit example is focused on the smallest solution size for 2 times 50-W output power into 2 Ω with a battery supply of 14.4 V
- The switching frequency is set above the AM-band with 44 times the input sample rate of 48 kHz which results in a frequency of 2.11 MHz.
- The selection of a 2.11-MHz switch frequency enables the use of a small output inductor value of 3.3 µH which leads to a very small solution size.

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11.2.2.1.1 Detailed Design Procedure

As a starting point, refer to the *Detailed Design Procedure* section for the BTL application. PBTL mode requires schematic changes in the output stage as shown in 図 82. The other required changes include setting up the I^2C registers correctly (see 表 13) and selecting which frame or channel to use on each output. Bit 6 in register 0x21 controls the frame selection.

11.2.2.2 Application Curves

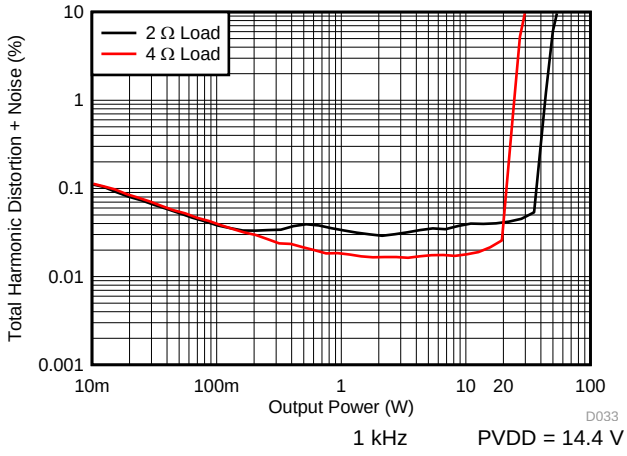

図 83. THD vs Output Power, 2R

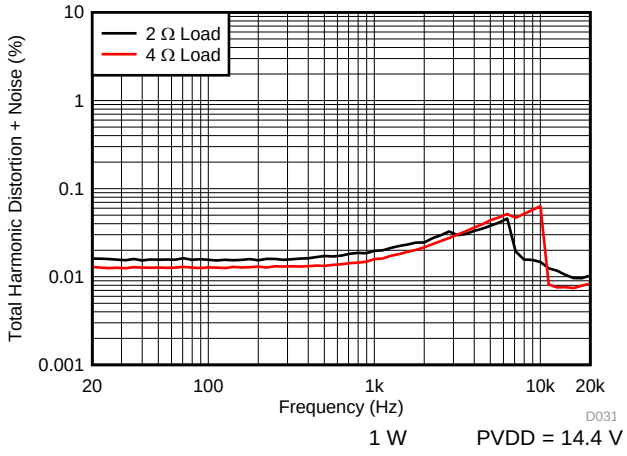

図 84. Frequency Response

12 Power Supply Recommendations

The TAS6424-Q1 requires three power supplies. The PVDD supply is the high-current supply in the recommended supply range. The VBAT supply is lower current supply that must be in the recommended supply range. The PVDD and VBAT pins can be connected to the same supply if the recommended supply range for VBAT is maintained. The VDD supply is the 3.3-Vdc logic supply and must be maintained in the tolerance as shown in the *Recommended Operating Conditions* table.

13 Layout

13.1 Layout Guidelines

The pinout of the TAS6424-Q1 was selected to provide flowthrough layout with all high-power connections on the right side, and all low-power signals and supply decoupling on the left side.

図 85 shows the area for the components in the application example (see the *Typical Applications* section).

The TAS6424-Q1 EVM uses a four-layer PCB. The copper thickness was selected as 70 µm to optimize power loss.

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Layout Guidelines (continued)

The small value of the output filter provides a small size and, in this case, the low height of the inductor enables double-sided mounting.

The EVM PCB shown in 図 85 is the basis for the layout guidelines.

13.1.1 Electrical Connection of Thermal pad and Heat Sink

For the DKQ package, the heat sink connected to the thermal pad of the device should be connected to GND. The heat slug must not be connected to any other electrical node.

13.1.2 EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design. The design has minimal parasitic inductances because of the short leads on the package which reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The design also incorporates circuitry that optimizes output transitions that cause EMI.

For optimizing the EMI a solid ground layer plane is recommended, for a PCB design the fulfills the CISPR25 level 5 requirements, see the TAS6424-Q1 EVM layout.

13.1.3 General Guidelines

The EVM layout is optimized for low noise and EMC performance.

The TAS6424-Q1 has an exposed thermal pad that is up, away from the PCB. The layout must consider an external heat sink.

Refer to 図 85 for the following guidelines:

- A ground plane, *A*, on the same side as the device pins helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current.
- The decoupling capacitors on PVDD, *B*, are very close to the device with the ground return close to the ground pins.
- The ground connections for the capacitors in the LC filter, *C*, have a direct path back to the device and also the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection.
- The traces from the output pins to the inductors, *D*, should have the shortest trace possible to allow for the smallest loop of large switching currents.
- Heat-sink mounting screws, *E*, should be close to the device to keep the loop short from the package to ground.
- Many vias, *F*, stitching together the ground planes can create a shield to isolate the amplifier and power supply.

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13.2 Layout Example

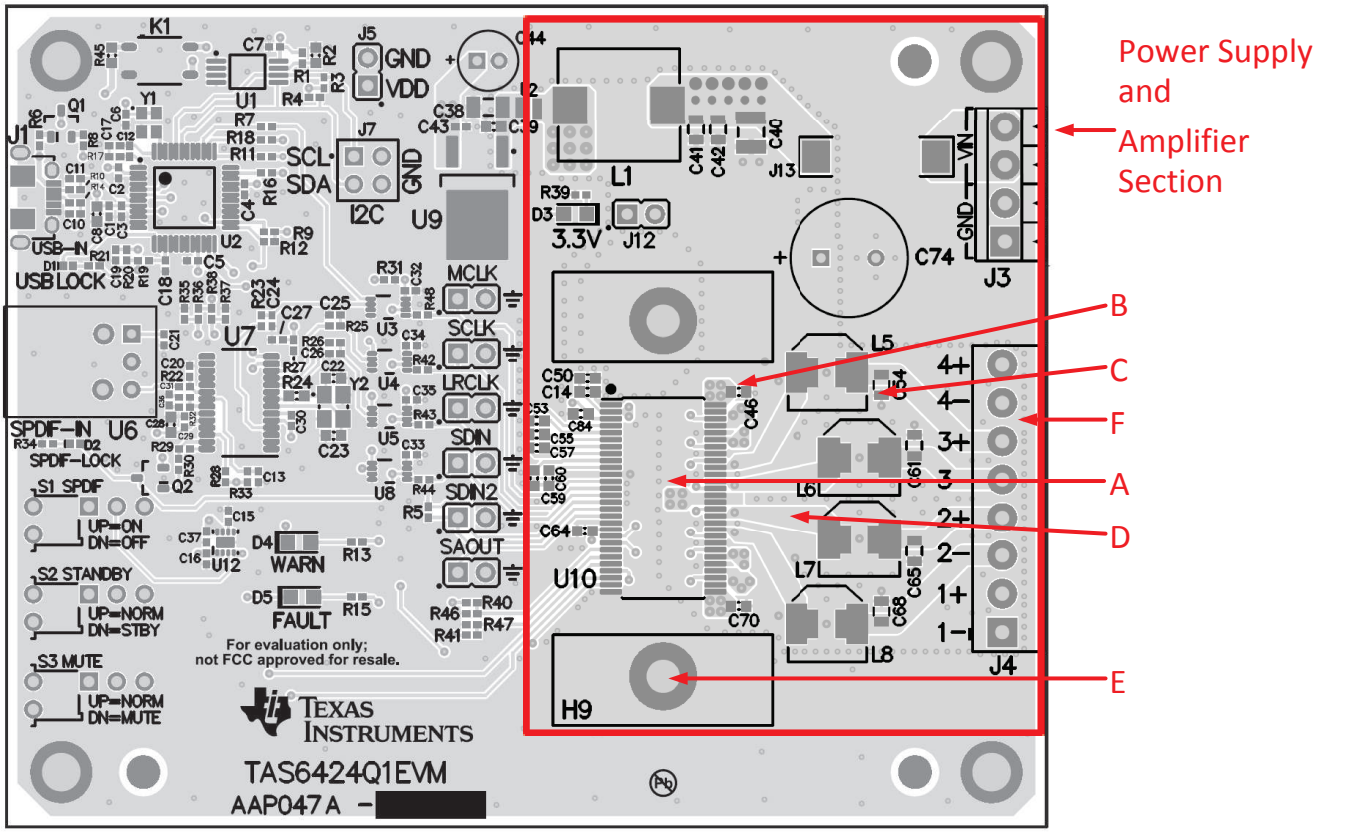

図 85. EVM Layout

13.3 Thermal Considerations

The thermally enhanced PowerPAD package has an exposed pad up for connection to a heat sink. The output power of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system, such as the ambient operating temperature. The heat sink absorbs heat from the TAS6424-Q1 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. Heat sinks can be smaller than that of classic linear amplifier design because of the excellent efficiency of class-D amplifiers. This device is intended for use with a heat sink, therefore, $R_{\theta JC}$ will be used as the thermal resistance from junction to the exposed metal package. This resistance will dominate the thermal management, so other thermal transfers will not be considered. The thermal resistance of $R_{\theta JA}$ (junction to ambient) is required to determine the full thermal solution. The thermal resistance is comprised of the following components:

- $R_{\theta JC}$ of the TAS6424-Q1
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

The thermal resistance of the thermal interface material can be determined from the manufacturer's value for the area thermal resistance (expressed in °C-mm^2/W) and the area of the exposed metal package. For example, a typical, white, thermal grease with a 0.0254-mm (0.001-inch) thick layer is approximately 4.52°C-mm^2/W. The TAS6424-Q1 in the DKQ package has an exposed area of 47.6 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the thermal grease. The thermal resistance of the thermal grease is 0.094°C/W

表 41 lists the modeling parameters for one device on a heat sink. The junction temperature is assumed to be 115°C while delivering and average power of 10 watts per channel into a 4-Ω load. The thermal-grease example previously described is used for the thermal interface material. Use 式 1 to design the thermal system.

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Thermal Considerations (continued)

$$R_{\theta JA} = R_{\theta JC} + \text{thermal interface resistance} + \text{heat sink resistance} \quad (1)$$

表 41. Thermal Modeling

Description	Value
Ambient Temperature	25°C
Average Power to load	40W (4x 10w)
Power dissipation	8W (4x 2w)
Junction Temperature	115°C
ΔT inside package	5.6°C (0.7°C/W × 8W)
ΔT through thermal interface material	0.75°C (0.094°C/W × 8W)
Required heat sink thermal resistance	10.45°C/W ([115°C – 25°C – 5.6°C – 0.75°C] / 8W)
System thermal resistance to ambient $R_{\theta JA}$	11.24°C/W

14 デバイスおよびドキュメントのサポート

14.1 ドキュメントのサポート

14.1.1 関連資料

関連資料については、以下を参照してください。

『PurePath™ Console 3ユーザー・マニュアル』(SLOU408)

『TAS6424-Q1 EVMユーザー・ガイド』(SLOU453)

14.2 ドキュメントの更新通知を受け取る方法

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14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS6424QDKQQ1.A	Active	Production	HSSOP (DKQ) | 56	20 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	TAS6424
TAS6424QDKQQ1.B	Active	Production	HSSOP (DKQ) | 56	20 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	TAS6424
TAS6424QDKQRQ1	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6424
TAS6424QDKQRQ1.A	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6424
TAS6424QDKQRQ1.B	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6424

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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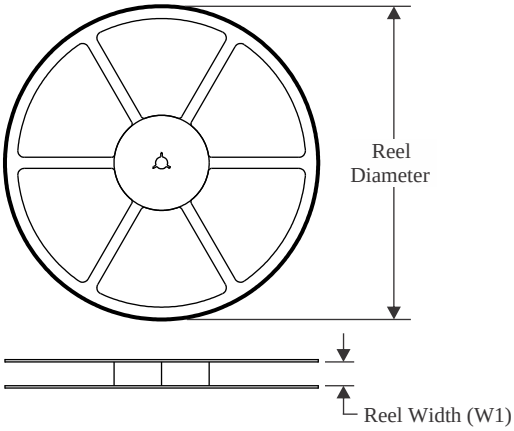
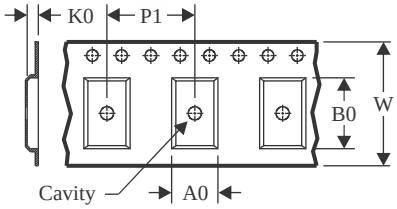
TAPE AND REEL INFORMATION

REEL DIMENSIONS

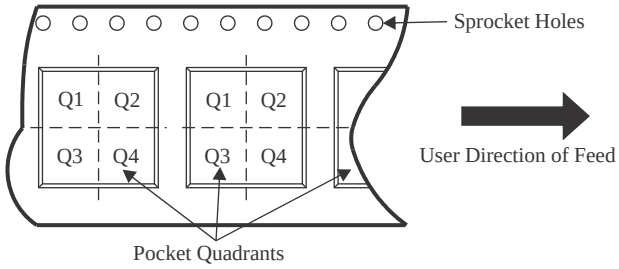


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

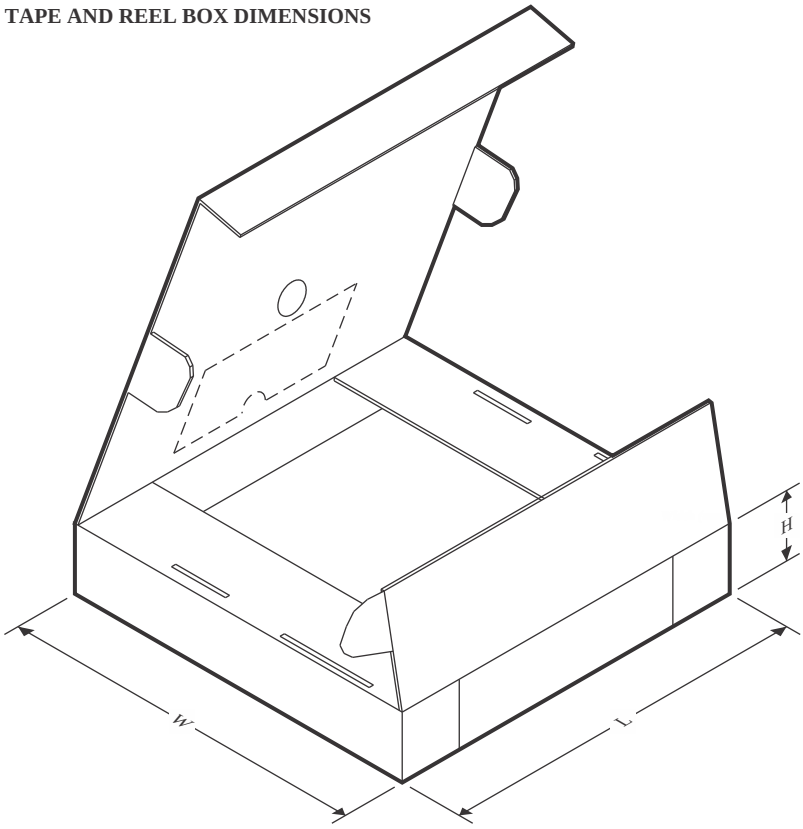
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6424QDKQRQ1	HSSOP	DKQ	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TAS6424QDKQRQ1	HSSOP	DKQ	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

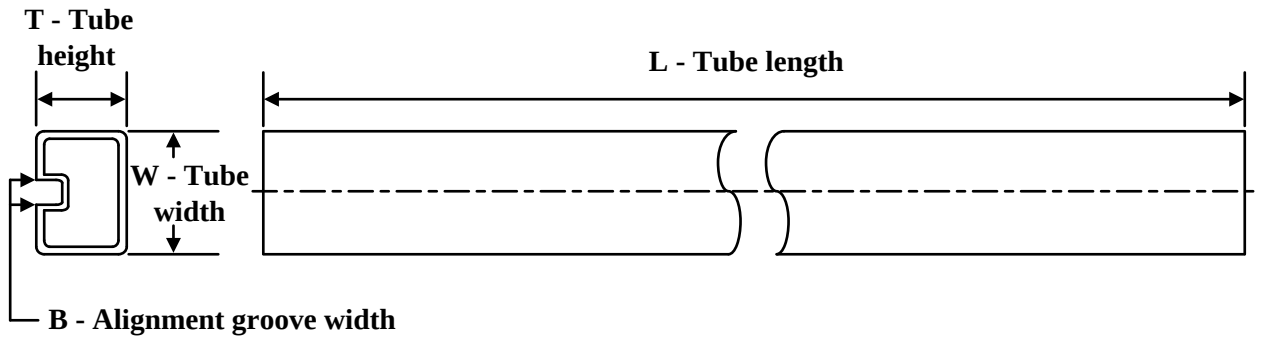
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6424QDKQRQ1	HSSOP	DKQ	56	1000	356.0	356.0	53.0
TAS6424QDKQRQ1	HSSOP	DKQ	56	1000	367.0	367.0	55.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS6424QDKQQ1.A	DKQ	HSSOP	56	20	473.7	14.24	5110	7.87
TAS6424QDKQQ1.B	DKQ	HSSOP	56	20	473.7	14.24	5110	7.87

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