THS3491 900MHz、500mA 高出力電流帰還アンプ

1 特長

- 帯域幅:
  - 900MHz (V_O = 2V_{PP}、A_V = 5V/V)
  - 320MHz (V_O = 10V_{PP}、A_V = 5V/V)
- スルーレート:8000V/µs (V_O = 20V_{PP})
- 入力電圧ノイズ:1.7nV/√Hz
- バイポーラ電源電圧範囲:±7V～±16V
- 単一電源電圧範囲:14V～32V
- 出力スイング:28V_{PP} (±16V 電源、100Ω 負荷)
- リニア出力電流:±420mA (標準値)
- 16.8mA の調整済み消費電流 (低温度係数)
- HD2 および HD3:–75dBc 未満 (50MHz、V_O = 10V_{PP}、100Ω 負荷)
- 立ち上がりおよび立ち下がり時間:1.3ns (10V ステップ)
- オーバーシュート:1.5% (10V ステップ、A_V = 5V/V)
- 電流制限およびサーマル・シャットダウン保護
- パワー・ダウン機能

2 アプリケーション

- 高電圧、任意波形発生器
- LCD テスタ用パターン発生器
- LCR メータ用出力ドライバ
- パワー FET ドライバ
- 高容量性負荷ピエゾ素子ドライバ
- VDSL ライン・ドライバ
- THS3095 へのピン互換アップグレード (DDA)

3 概要

THS3491 電流帰還アンプ (CFA) は、100Ω 負荷時に DC～100MHz 超の動作周波数により、高出力レベルで歪みを最小限に抑える必要があるアプリケーションにおいて、かつてないレベルの性能を実現します。仕様ではゲインは 5V/V ですが、この電流帰還設計により、広いゲイン範囲にわたって帯域幅と歪みがほぼ一定に維持されます。

8000V/µs のスルーレートにより、要求の厳しい負荷に 10V_{PP} の出力を提供し、100MHz まで歪みを小さく抑えることができます。900MHz の小信号帯域幅により、10V ステップで 1.5% 未満の低オーバーシュートと、1.3ns 未満の立ち上がり/立ち下がり時間を実現します。500mA を上回るピーク出力電流駆動により、高速信号で重い容量性負荷を駆動できます。

VQFN-16 (RGT) パッケージを使用した新規設計では、歪みを最小限に抑えることができる一方、8 ピンの HSOIC (DDA) パッケージ (PowerPAD™ 搭載) は既存の THS3091 設計または THS3095 設計をアップグレードします。THS3491 は出力ヘッドルームが小さく、THS3091 や THS3095 に比べて、同じ ±15V 電源でも出力振幅が大きくなります。

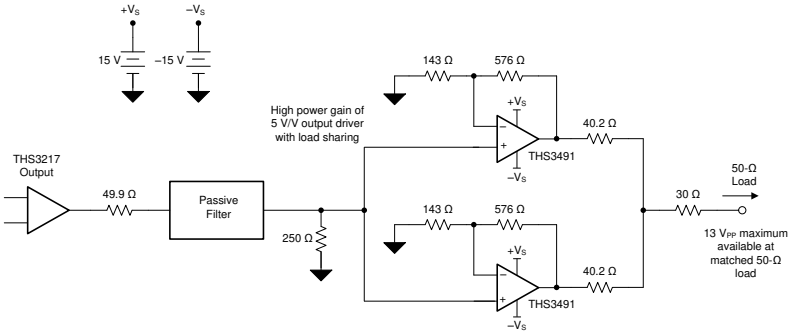
パッケージ情報(1)(2)

部品番号	パッケージ	本体サイズ (公称)
THS3491	RGT (VQFN、16)	3.00mm × 3.00mm
	DDA (HSOIC、8)	4.89mm × 3.90mm

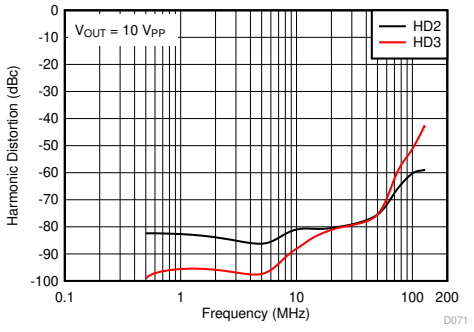
製品情報

部品番号	パッケージ	ダイ・サイズ (公称)
THS3491	ベア・ダイ	1.02mm × 1.06mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) デバイス比較表を参照してください。



標準的な任意波形発生器の出力駆動回路



高調波歪みと周波数との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2018) to Revision C (February 2023) **Page**

- データシートにベア・ダイ・パッケージの詳細情報を追加 1
- Removed *bipolar-supply operating range* and *single-supply operating range* specifications from *Electrical Characteristics: V_S = ±15 V* 8
- Added new test level *A2* that is clarifies what is tested for die sales 8

Changes from Revision A (March 2018) to Revision B (July 2018) **Page**

- 「標準的な任意波形発生器の出力駆動回路」の抵抗値 を 49.9Ω から 40.2Ω に変更 1
- 「標準的な任意波形発生器の出力駆動回路」の抵抗値 を 24.9Ω から 30Ω に変更 1
- Changed *T_A = 25°C* to *T_A ≅ 25°C* in *Electrical Characteristics: ±15 V* condition statement 8
- Changed *100% tested at 25°C* to *100% tested at ≅ 25°C* in the footnote of *Electrical Characteristics: ±15 V* 8
- Added *DDA package only* in Test Conditions column for *"V_{OS}"* specification 8
- Added new V_{OS} specifiction line for RGT package 8
- Added min/max values to *R_{FB_TRACE}* specification 8
- Changed units from: *pF || kΩ* to: *kΩ || pF* and changed typical spec accordingly 8
- Added min/max values to *T_{J_SENSE} 25℃ value* specification 8
- Changed *T_{J_SENSE} temperature coefficient* specification's typical value from 3 mV/℃ to 3.2 mV/℃ 8
- Added min/max values to *T_{J_SENSE} input impedance* specification 8
- Changed "T_A = 25°C" to "T_A ≅ 25°C" in *Electrical Characteristics: ±7.5 V* condition statement 11
- Changed "100% tested at 25°C" to "100% tested at ≅ 25°C" in the footnote of *Electrical Characteristics: ±7.5 V* 11
- Added "DDA package only" in Test Conditions column for "V_{OS}" specification 11
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- Added min/max values to "T_{J_SENSE} input impedance" specification 11
- Changed "T_A = 25°C" to "T_A ≅ 25°C" in *Typical Characteristics: ±15 V* condition statement 13
- Changed Z_{OL} low frequency value from 160 dB to 138 dB in *Open-Loop Transimpedance Gain and Phase vs Frequency* 13

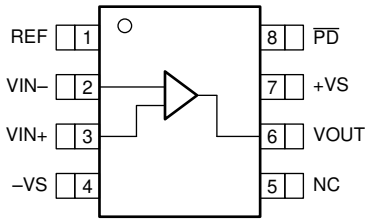
Changes from Revision * (August 2017) to Revision A (March 2018) **Page**

5 Device Comparison Table

DEVICE	SUPPLY, V_S (V)	SSBW, A_V = 5 (MHz)	MAXIMUM ICC AT 25°C (mA)	INPUT NOISE V_n (nV/√Hz)	HD2/3, 10 V_{PP} AT 50 MHz, G = 5 V/V (dBc)	SLEW RATE (V/µs)	LINEAR OUTPUT CURRENT (mA)
THS3491	±15	900	17.3	1.7	–76/–75	7100(1)	±420
THS3095	±15	190	9.5	1.6	–40/–42	1200(2)	±250
THS3001	±15	350	9	1.6	N/A	1400(3)	±120
THS3061	±15	260	8.3	2.6	N/A	1060(4)	±140

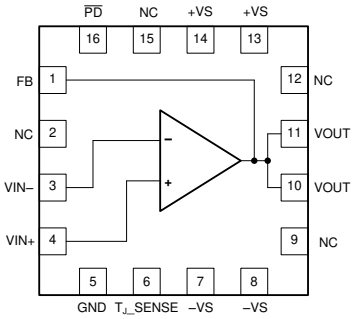
(1) Slew rate from FPBW of 320 MHz, 10 V_{PP}
(2) Slew rate from FPBW of 135 MHz, 4 V_{PP}
(3) Slew rate from FPBW of 32 MHz, 20 V_{PP}
(4) Slew rate from FPBW of 120 MHz, 4 V_{PP}

6 Pin Configuration and Functions



NC - no internal connection

図 6-1. DDA Package, 8-Pin HSOIC With PowerPAD (Top View)



NC - no internal connection

図 6-2. RGT Package, 16-Pin VQFN With Exposed Thermal Pad (Top View)

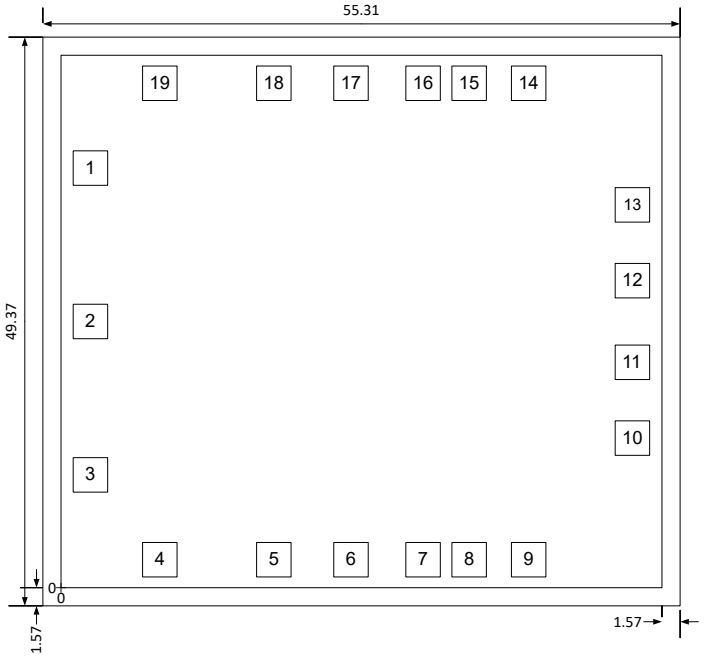
表 6-1. Pin Functions

PIN (1)			TYPE (2)	DESCRIPTION
NAME	HSOIC	VQFN		
FB	—	1	O	Input side feedback pin
GND	—	5	GND	Ground, $\overline{PD}$ logic reference on the VQFN-16 (RGT) package
NC	5	2, 9, 12, 15	—	No connect (there is no internal connection). Recommended connection to a heat spreading plane, typically GND.
$\overline{PD}$	8	16	I	Amplifier power down: low = amplifier disabled, high (default) = amplifier enabled
REF	1	—	I	$\overline{PD}$ logic reference on the SOIC-8 (DDA) package. Typically connected to GND.
T_{J_SENSE}	—	6	O	Voltage proportional to die temperature
VIN–	2	3	I	Inverting input
VIN+	3	4	I	Noninverting input
VOUT	6	10, 11	O	Amplifier output
–VS	4	7, 8	P	Negative power supply
+VS	7	13, 14	P	Positive power supply
Thermal pad			—	Thermal pad. Electrically isolated from the device. Recommended connection to a heat spreading plane, typically GND.

(1) Both packages include a backside thermal pad. The thermal pad can be connected to a heat spreading plane that can be at any voltage because the device die is electrically isolated from this metal plate. The thermal pad can also be unused (not connected to any heat spreading plane or voltage) giving higher thermal impedance.
(2) GND = ground, I = input, O = output, P = power

7 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS
15 mils (381 µm)	Silicon with backgrind	Wafer backside is electrically connected to -VS	Al	76.0 µm × 76.0 µm



Bond Pad Coordinates in Microns

NAME	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
FB	1	26.9	887	103	963
VIN-	2	26.9	549	103	625
VIN+	3	26.9	211	103	287
REF	4	180	23.7	256	99.7
DNC	5	431	23.7	507	99.7
T_{J_SENSE}	6	601	23.7	677	99.7
-VS	7	760	23.7	836	99.7
-VS	8	862	23.7	938	99.7
-VS	9	993	23.7	1069	99.7
-VS	10	1222	292	1298	368
VOUT	11	1222	459	1298	535
VOUT	12	1222	639	1298	715
+VS	13	1222	806	1298	882
+VS	14	993	1074	1069	1150
+VS	15	862	1074	938	1150
+VS	16	760	1074	836	1150
DNC	17	601	1074	677	1150
PD	18	431	1074	507	1150
REF	19	180	1074	256	1150

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, (+VS) – (–VS)			33	V
	Supply voltage turnon, turnoff maximum dV/dT (2)			1	V/µs
	Input/output voltage range		(–VS) – 0.5	(+VS) + 0.5	V
	Differential input voltage			±0.5	
Current	Continuous input current (3)			±10	mA
	Continuous output current (3)			±100	
Temperature	Junction temperature, T_J (4)	Maximum		150	°C
		Continuous operation, long-term reliability		125	
	Storage temperature, T_{stg} (5)		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stay below this dV/dT supply turnon and turnoff edge rate to make sure that the edge-triggered ESD absorption device across the supply pins remains open. Exceeding this supply edge rate may transiently show a short circuit across the supplies.
(3) Long-term continuous current for electro-migration limits.
(4) Thermal shutdown at approximately 160°C junction temperature and recovery at approximately 145°C.
(5) See the MSL or reflow rating information provided with the material or see https://www.ti.com for the latest information.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$(+V_S) – (–V_S)$	Supply voltage	Dual-supply	±7	±15	±16	V
		Single-supply	14	30	32	
T_A	Operating free-air temperature		–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)		THS3491		UNIT
		DDA (HSOIC)	RGT (VQFN)	
		8 PINS	8 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	44.5	49.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	66.8	55.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	19.2	23.1	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	6.4	1.8	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	19.5	23.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	7.8	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

8.5 Electrical Characteristics: V_S = ±15 V

at $+V_S$ = +15 V, $-V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 2 V_{PP}, < 0.5-dB peaking		900		MHz	C
LSBW	Large-signal bandwidth	V_O = 10 V_{PP}, < 1-dB peaking		320		MHz	C
	Bandwidth for 0.2-dB flatness	V_O = 2 V_{PP}		350		MHz	C
SR	Slew rate (20% – 80%)	V_O = 20 V_{PP}		8000		V/µs	C
	Overshoot and undershoot	V_O = 10-V step (input t_r/t_f = 1.0 ns)		1.5%			C
t_r/t_f	Rise and fall time	V_O = 10-V step (input t_r/t_f = 1.0 ns)		1.3		ns	C
t_s	Settling time to 0.1%	V_O = 10-V step (input t_r/t_f = 1.0 ns)		7		ns	C
HD2	Second-order harmonic distortion	f = 20 MHz, V_O = 10 V_{PP}		–78		dBc	C
		f = 50 MHz, V_O = 10 V_{PP}		–76			
		f = 70 MHz, V_O = 10 V_{PP}		–68			
		f = 100 MHz, V_O = 10 V_{PP}		–60			
		f = 20 MHz, V_O = 20 V_{PP}		–75			
		f = 50 MHz, V_O = 20 V_{PP}		–65			
		f = 70 MHz, V_O = 20 V_{PP}		–61			
		f = 100 MHz, V_O = 20 V_{PP}		–51			
HD3	Third-order harmonic distortion	f = 20 MHz, V_O = 10 V_{PP}		–81		dBc	C
		f = 50 MHz, V_O = 10 V_{PP}		–75			
		f = 70 MHz, V_O = 10 V_{PP}		–61			
		f = 100 MHz, V_O = 10 V_{PP}		–51			
		f = 20 MHz, V_O = 20 V_{PP}		–64			
		f = 50 MHz, V_O = 20 V_{PP}		–55			
		f = 70 MHz, V_O = 20 V_{PP}		–48			
		f = 100 MHz, V_O = 20 V_{PP}		–47			
IMD2	2nd-order two-tone intermodulation distortion	f = 20 MHz, V_O = 5 V_{PP} per tone, 100-kHz tone spacing		–79		dBc	C
IMD3	3rd-order two-tone intermodulation distortion	f = 20 MHz, V_O = 5 V_{PP} per tone, 100-kHz tone spacing		–68		dBc	C
e_n	Input-referred voltage noise	f ≥ 100 kHz		1.7		nV/√Hz	C
i_{np}	Noninverting, input-referred current noise	f ≥ 100 kHz		15		pA/√Hz	C
i_{nn}	Inverting, input-referred current noise	f ≥ 100 kHz		20		pA/√Hz	C
Z_{OUT}	Closed-loop output impedance	f = 50 MHz		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = ±10 V, R_{LOAD} = 500 Ω	5	8		MΩ	A1
V_{OS}	Input offset voltage	DDA package only	–2	1	2	mV	A1
		RGT package & DIE sales	–2.5	1	2.5	mV	A1
	Input offset voltage drift(2)	–40°C ≤ T_J ≤ +125°C		3		µV/°C	B
I_{B+}	Noninverting input bias current(3)		–7	–2	7	µA	A1
	Noninverting input bias current drift(2)	–40°C ≤ T_J ≤ +125°C		–8		nA/°C	B
I_{B-}	Inverting input bias current(3)		–20	–7	20	µA	A1
	Inverting input bias current drift(2)	–40°C ≤ T_J ≤ +125°C		–116		nA/°C	B

8.5 Electrical Characteristics: V_S = ±15 V (continued)

at +V_S = +15 V, –V_S = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(1)
R_{FB_TRACE}	Internal trace resistance to feedback pin	RGT only, pins 10 and 11 to pin 1	1.1	1.5	1.9	Ω	A2
CMRR	Common-mode rejection ratio	f = DC	69	75		dB	A1
INPUT							
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	A2
Z_{IN+}	Noninverting input impedance	Closed-loop measurement	50 || 1.2			kΩ || pF	C
Z_{IN-}	Inverting input impedance	Open-loop measurement	8	15	18	Ω	B
OUTPUT							
HR_{OUT}	Headroom to either supply		1.2	1.5	1.7	V	A1
$Iout_{MAX}$	Maximum current output	R_{LOAD} = 24 Ω, V_O = ±12.67 V, magnitude, both polarities	480	520	550	mA	A2
$Iout_{LINEAR}$	Linear output current	R_{LOAD} = 24 Ω, V_O = ±9.4 V, Z_{OL} > 1 MΩ, source and sink	380	420		mA	A2
$Iout_{PEAK}$	Peak output current in transition (transition peak at zero-crossing I_{OUT})	V_O = 0 V, R_O < 0.5 Ω, magnitude, both polarities	500	540		mA	B
I_{SC}	Output short-circuit current	V_S = ±9 V, V_O = ±6 V, magnitude, both polarities	550	620		mA	B
Z_{OUT}	DC output impedance	Closed-loop (±50 mA)		0.17		Ω	C
POWER SUPPLY							
I_Q	Quiescent current	V_S = ±15 V, No load	16.1	16.7	17.3	mA	A1
		V_S = ±16 V, No load	16.2	16.8	17.4	mA	A2
		V_S = ±7 V, No load	15.2	15.8	16.3	mA	A1
I_Q TC		V_S = ±15 V, T_J = –40°C to +125°C, No load		5		µA/°C	B
PSRR+	Positive power supply rejection ratio	+V_S ± 1.5 V, –V_S	78	82		dB	A1
PSRR–	Negative power supply rejection ratio	+V_S, –V_S ± 1.5 V	77	80		dB	A1
POWER DOWN							
REF_{RANGE}	REF pin voltage range	Do NOT float the REF pin.	–Vs	GND	+Vs – 5 V	V	A2
I_{REF_BIAS}	REF pin bias current	REF = 0 V, $\overline{PD}$ = REF + 3 V, positive out of the pin.	35	46	52	µA	A2
V_{IL}	Disable voltage threshold	REF = 0 V, guaranteed off below			0.8	V	A1
V_{IH}	Enable voltage threshold	REF = 0 V, guaranteed on above	1.5			V	A1
$\overline{PD}_{LOW\_BIAS}$	$\overline{PD}$ pin low input bias current	$\overline{PD}$ = REF = GND, positive out of the pin.	17	21	25	µA	A2
$\overline{PD}_{HIGH\_BIAS}$	$\overline{PD}$ pin high input bias current	$\overline{PD}$ = REF + 3 V, REF = GND, positive out of the pin.	–1	0	1	µA	A2
$I_{Q\_OFF\_+VS}$	+Vs disabled supply current		650	780	880	µA	A1
$I_{Q\_OFF\_-VS}$	–Vs disabled supply current		600	723	820	µA	A2
t_{ON}	Turnon time delay	DC output to 90% of final value		50		ns	C
t_{OFF}	Turnoff time delay	DC output to 10% of final value		4		µs	C
JUNCTION-TEMPERATURE SENSE, T_J_SENSE (QFN-16 ONLY, PIN 6)							
	T_{J_SENSE} 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A2
	T_{J_SENSE} temperature coefficient	T_J = 0°C to 125°C		3.2		mV/°C	B

8.5 Electrical Characteristics: V_S = ±15 V (continued)

at $+V_S$ = +15 V, $-V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(1)
	T_{J_SENSE} input impedance	Internally connected to REF pin	32.4	35	38	kΩ	A2

(1) Test levels (all values set by characterization and simulation): (A1) 100% tested at ≈ 25°C for all devices, overtemperature limits by characterization and simulation; (A2) 100% tested at ≈ 25°C for packaged devices, not tested in production for die sales (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information;
(2) Input offset voltage drift and input bias current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
(3) Current is considered positive out of the pin.

8.6 Electrical Characteristics: V_S = ±7.5 V

at $+V_S$ = +7.5 V, $-V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 2 V_{PP}, < 0.5-dB peaking		800		MHz	C
LSBW	Large-signal bandwidth	V_O = 5 V_{PP}, < 1-dB peaking		550		MHz	C
SR	Slew rate (20%-80%)	V_O = 10 V_{PP}		6000		V/µs	C
HD2	Second-order harmonic distortion	f = 20 MHz, V_O = 5 V_{PP}		–83		dBc	C
HD3	Third-order harmonic distortion	f = 20 MHz, V_O = 5 V_{PP}		–78		dBc	C
e_n	Input-referred voltage noise	f ≥ 100 kHz		1.7		nV/√Hz	C
i_{np}	Noninverting, input-referred current noise	f ≥ 100 kHz		15		pA/√Hz	C
i_{nn}	Inverting, input-referred current noise	f ≥= 100 kHz		20		pA/√Hz	C
Z_{OUT}	Closed-loop output impedance	f = 50 MHz		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = ±2.5 V, R_{LOAD} = 500 Ω	6	14		MΩ	A1
V_{OS}	Input offset voltage	DDA package limits	–2	1	2	mV	A1
		RGT package & die sales limits	–2.5	1	2.5	mV	A1
	Input offset-voltage drift(2)	–40°C ≤ T_J ≤ +125°C		3		µV/°C	B
I_{B+}	Noninverting input bias current(3)		–7	-2	7	µA	A1
	Noninverting input bias current drift(2)	–40°C ≤ T_J ≤ +125°C		–10		nA/°C	B
$I_{B–}$	Inverting input bias current(3)		–19	–6	19	µA	A1
	Inverting input bias current drift(2)	–40°C ≤ T_J ≤ +125°C		–112		nA/°C	B
INPUT							
Z_{IN+}	Noninverting input impedance	Closed-loop measurement	35 || 1.2			kΩ || pF	C
$Z_{IN–}$	Inverting input impedance	Open-loop measurement		15		Ω	C
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	B
OUTPUT							
HR_{OUT}	Headroom to either supply		1.2	1.5	1.7	V	A1
$Iout_{LINEAR}$	Linear output current	R_{LOAD} = 24 Ω, V_O = ±5 V, Z_{OL} > 1 MΩ, source and sink	200	230		mA	A2
POWER SUPPLY							
I_Q	Quiescent current	No load	15.2	15.8	16.4	mA	A1
POWER DOWN							
REF_{RANGE}	REF pin voltage range	Do NOT float the REF pin.	–Vs	GND	+Vs – 5 V	V	B
I_{REF_BIAS}	REF pin bias current	REF = 0 V, $\overline{PD}$ = REF + 3 V, positive out of the pin	35	37	52	µA	A2
V_{IL}	Disable voltage threshold	REF = 0 V, guaranteed off below			0.8	V	A1
V_{IH}	Enable voltage threshold	REF = 0 V, guaranteed on above	1.5			V	A1
$\overline{PD}_{LOW\_BIAS}$	$\overline{PD}$ pin low input bias current	$\overline{PD}$ = REF = GND, positive out of the pin.	17	21	25	µA	A2
$\overline{PD}_{HIGH\_BIAS}$	$\overline{PD}$ pin high input bias current	$\overline{PD}$ = REF + 3 V, REF = GND, positive out of the pin.	–1	0	1	µA	A2
$I_{Q\_OFF\_+VS}$	+Vs disabled supply current		600	700	850	µA	A1
$I_{Q\_OFF\_–VS}$	–Vs disabled supply current		550	642	770	µA	A2

8.6 Electrical Characteristics: V_S = ±7.5 V (continued)

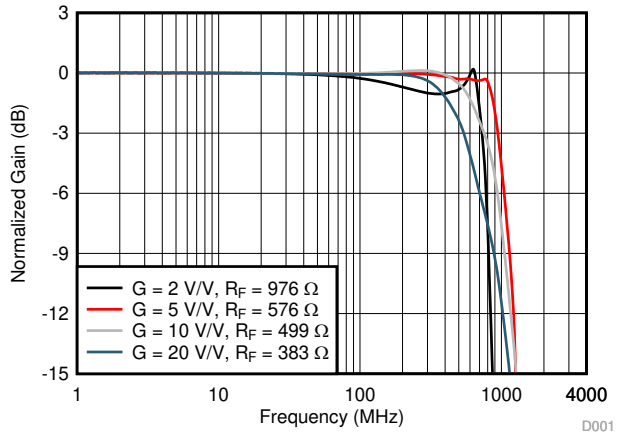
at $+V_S$ = +7.5 V, $–V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level(1)
JUNCTION-TEMPERATURE SENSE, T_J_SENSE (QFN-16 ONLY, PIN 6)							
	T_{J_SENSE} 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A2
	T_{J_SENSE} temperature coefficient	T_J = 0°C to 125°C		3.2		mV/°C	B
	T_{J_SENSE} input impedance	Internally connected to REF pin	32.4	35	38	kΩ	B

(1) Test levels (all values set by characterization and simulation): (A1) 100% tested at ≅ 25°C for all devices, overtemperature limits by characterization and simulation; (A2) 100% tested at ≅ 25°C for packaged devices, not tested in production for die sales (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information;
(2) Input offset voltage drift and input bias current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
(3) Current is considered positive out of the pin.

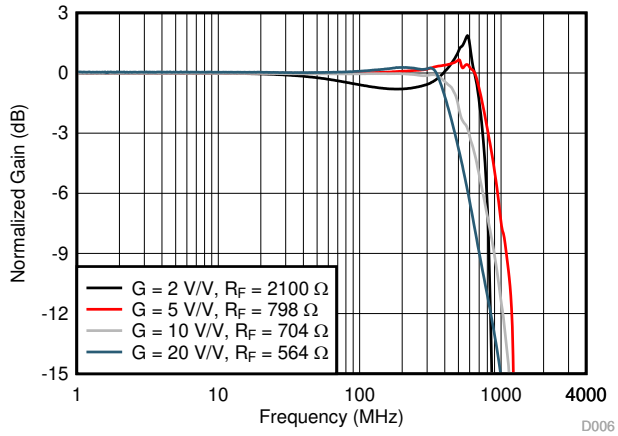
8.7 Typical Characteristics: ±15 V

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



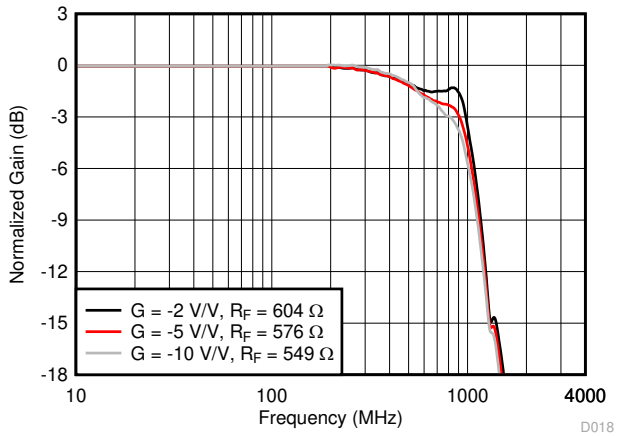
V_O = 2 V_{PP} RGT package

図 8-1. Noninverting Small-Signal Frequency Response



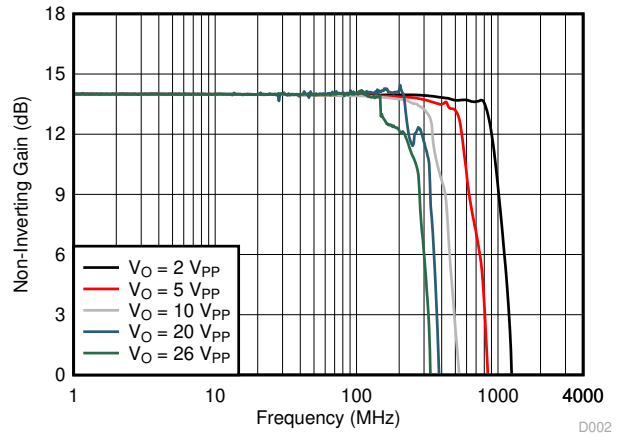
V_O = 2 V_{PP} DDA package

図 8-2. Noninverting Small-Signal Frequency Response



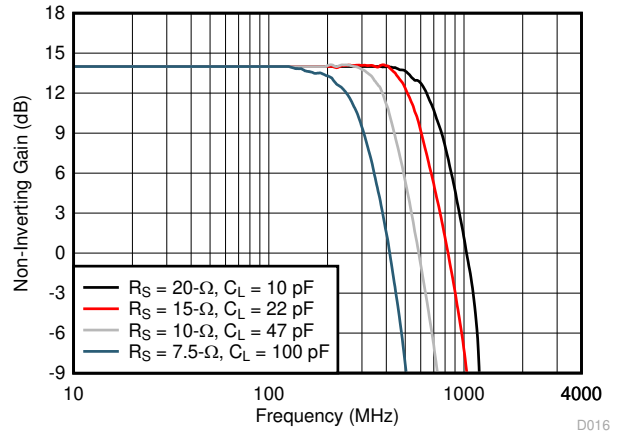
V_O = 2 V_{PP}

図 8-3. Inverting Small-Signal Frequency Response



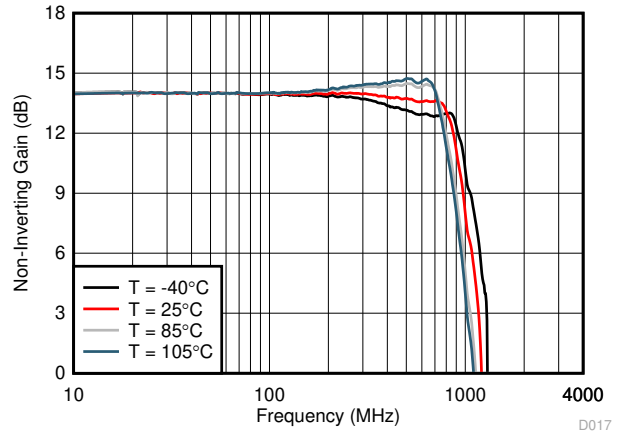
RGT package; see セクション 9.4.4 section for more details

図 8-4. Frequency Response vs Output Swing



RGT package; see 図 10-1 for setup information

図 8-5. Frequency Response vs C_{LOAD}

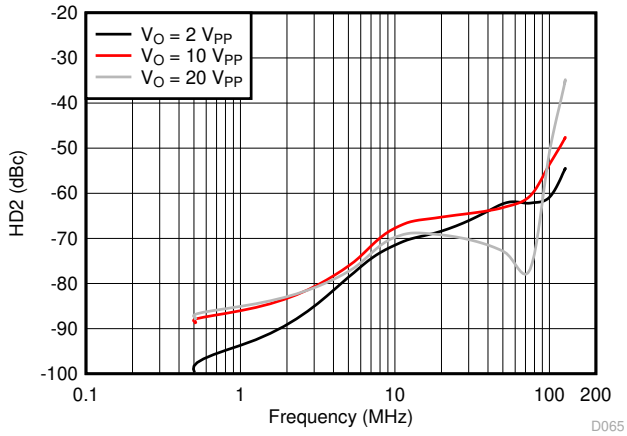


V_O = 2 V_{PP} RGT package

図 8-6. Frequency Response vs Temperature

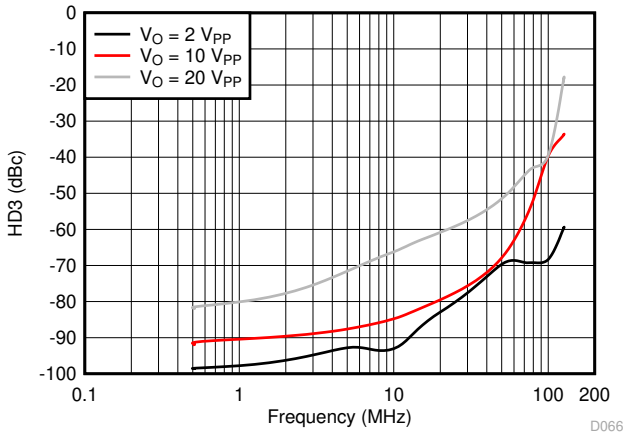
8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



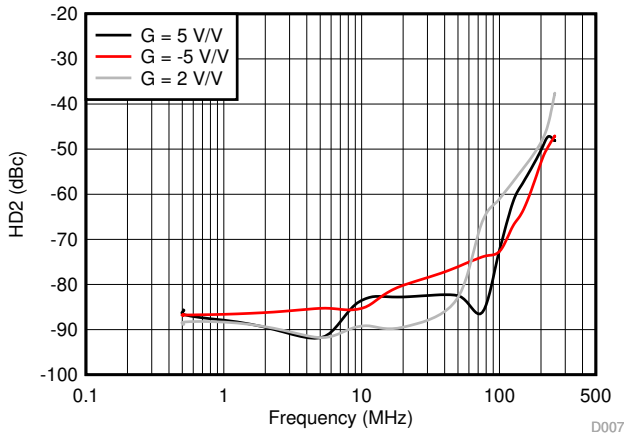
DDA package

図 8-7. HD2 vs Frequency



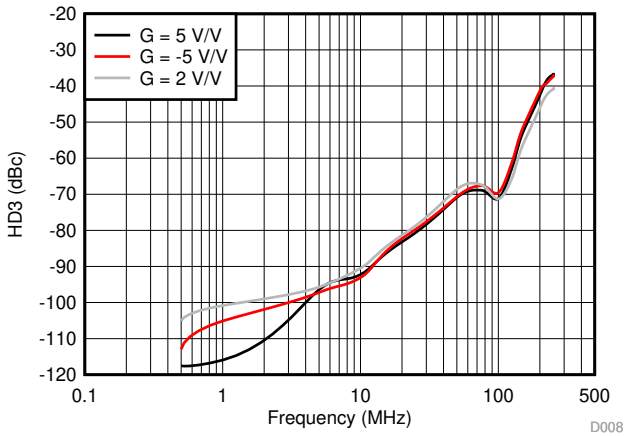
DDA package

図 8-8. HD3 vs Frequency



V_O = 2 V_{PP} RGT package

図 8-9. HD2 vs Frequency



V_O = 2 V_{PP} RGT package

図 8-10. HD3 vs Frequency

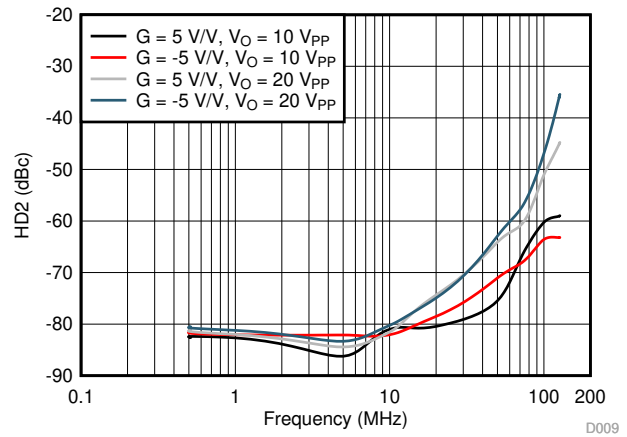


図 8-11. HD2 vs Frequency Across Output Swing

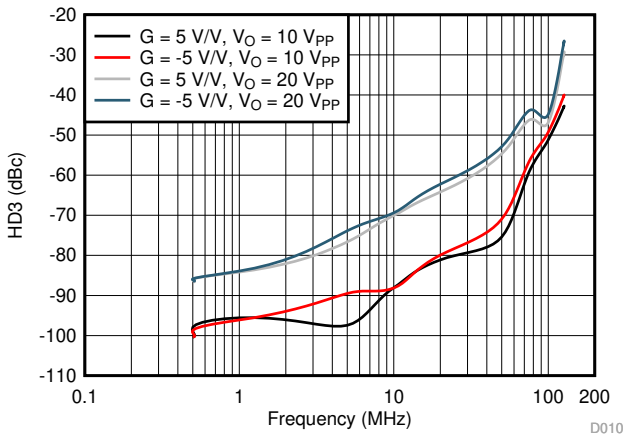


図 8-12. HD3 vs Frequency Across Output Swing

8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $-V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

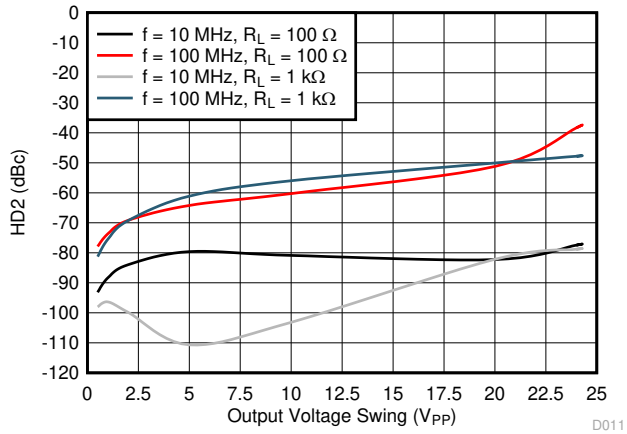


図 8-13. HD2 vs Output Swing

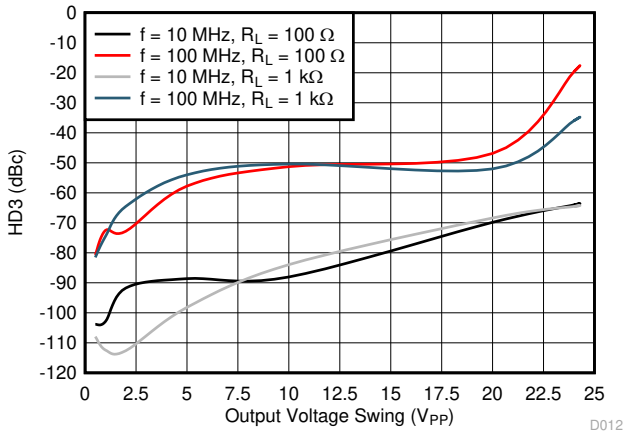
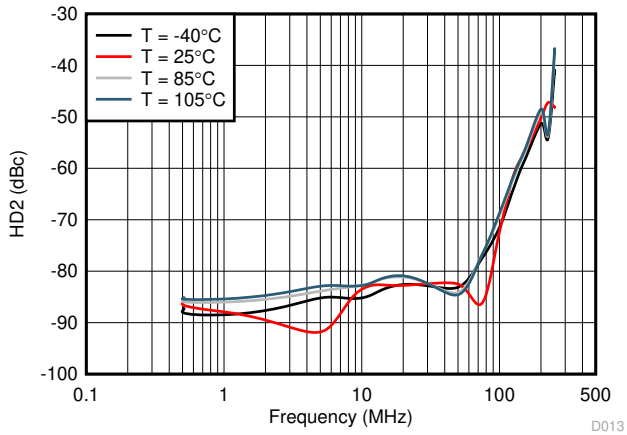
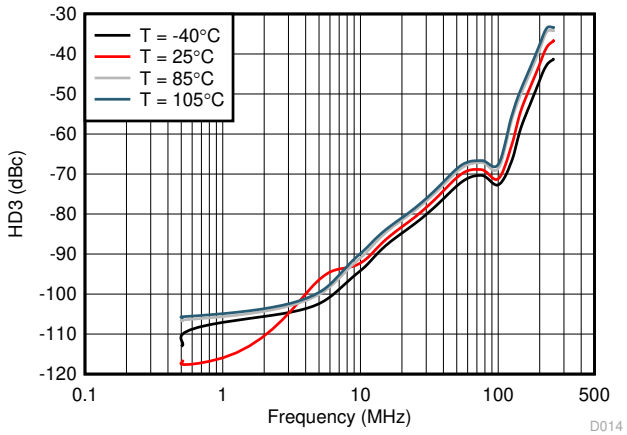


図 8-14. HD3 vs Output Swing



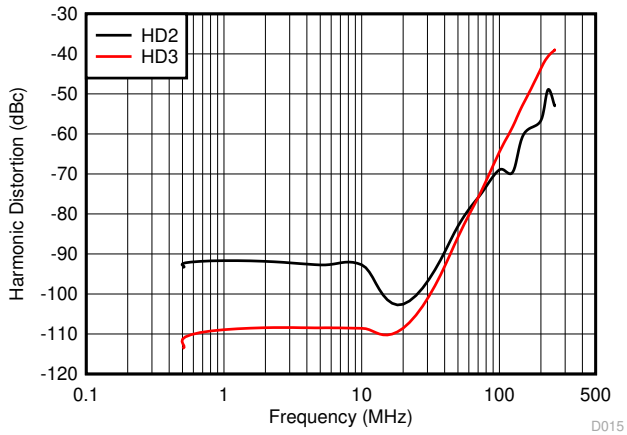
V_O = 2 V_{PP}

図 8-15. HD2 vs Frequency Across Temperature



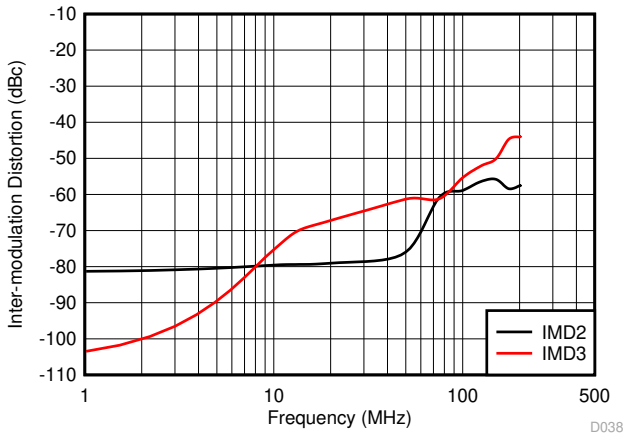
V_O = 2 V_{PP}

図 8-16. HD3 vs Frequency Across Temperature



V_O = 2 V_{PP} R_{Load} = 1 kΩ

図 8-17. Harmonic Distortion vs Frequency

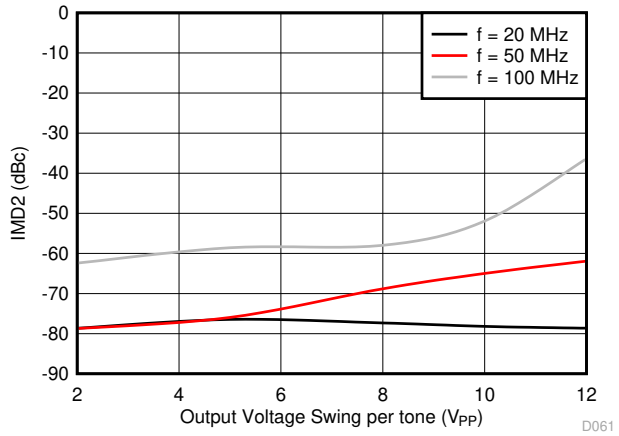


V_O = 5 V_{PP} per tone ±100-kHz frequency spacing

図 8-18. Intermodulation Distortion vs Frequency

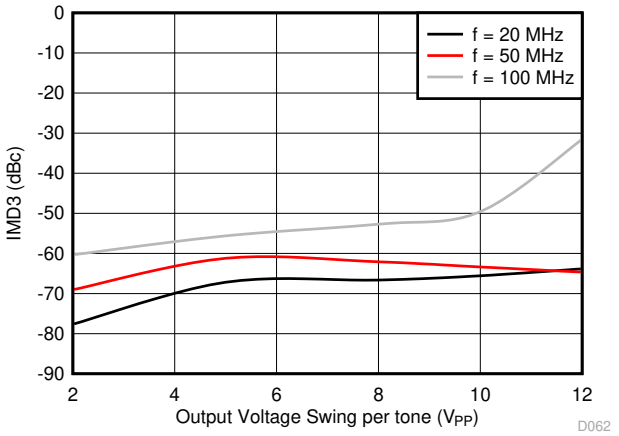
8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $-V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



±100-kHz frequency spacing

図 8-19. IMD2 vs Output Voltage Swing



±100-kHz frequency spacing

図 8-20. IMD3 vs Output Voltage Swing

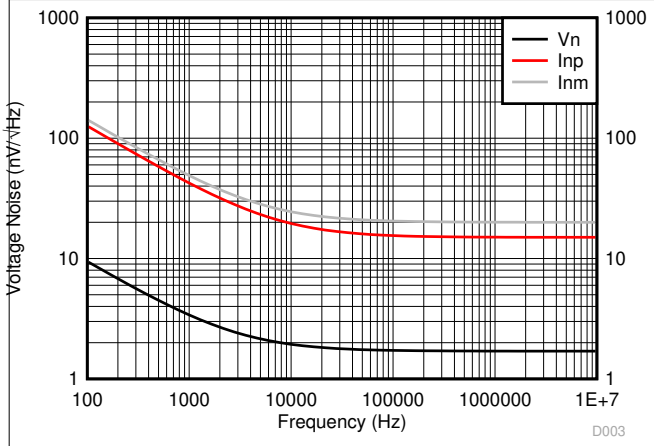
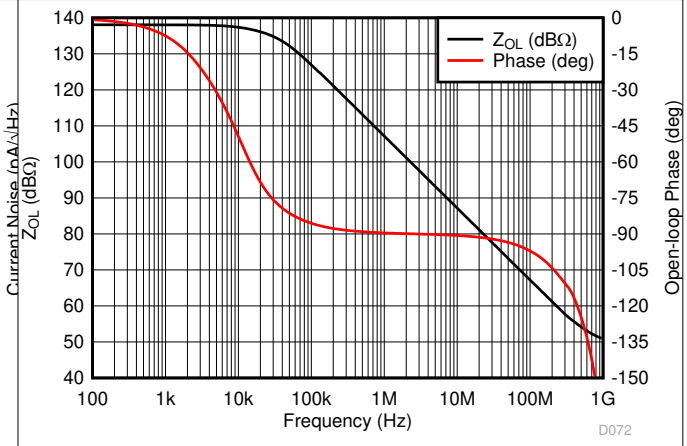
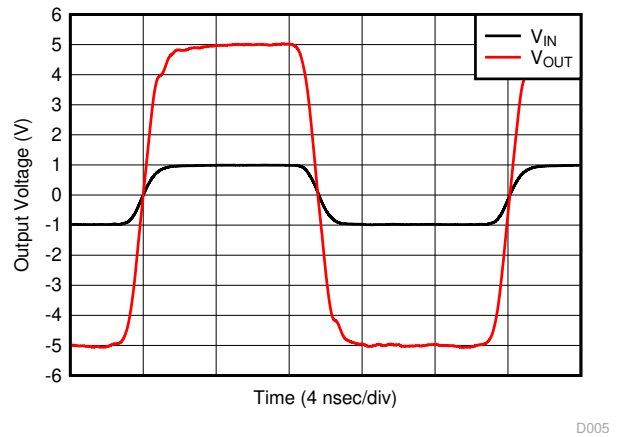


図 8-21. Spot Input Noise vs Frequency



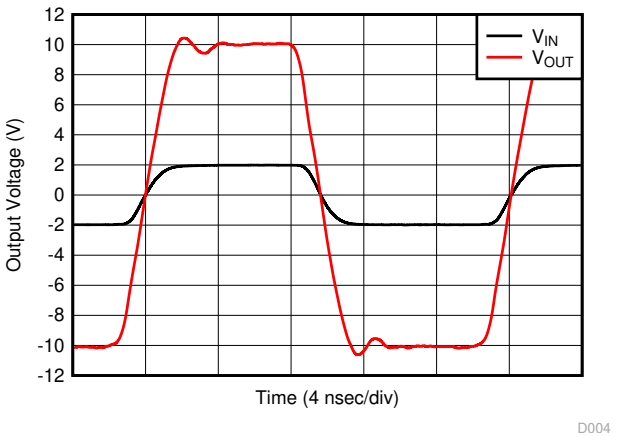
No load

図 8-22. Open-Loop Transimpedance Gain and Phase vs Frequency



V_O = 10 V_{PP}

図 8-23. G = 5 V/V Pulse Response

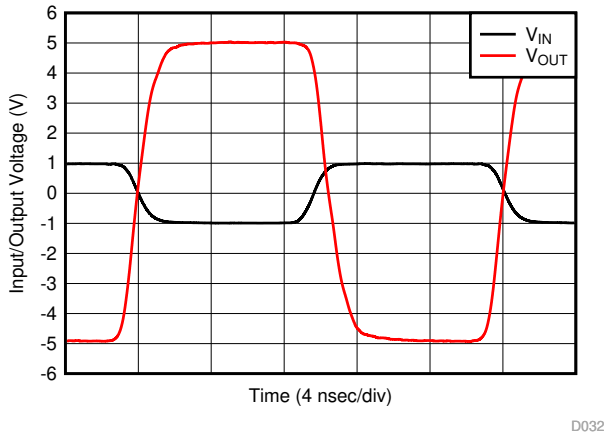


V_O = 20 V_{PP}

図 8-24. G = 5 V/V Pulse Response

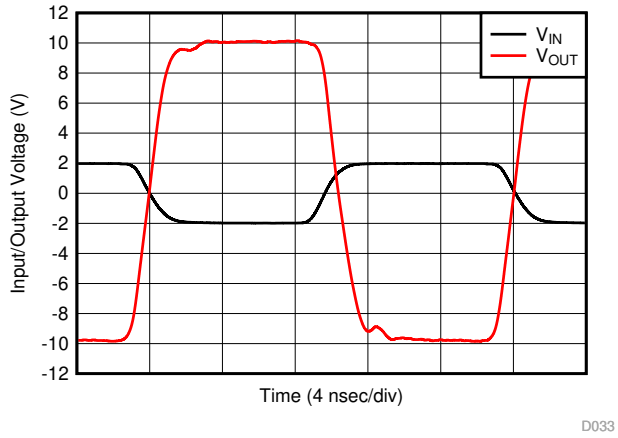
8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



V_O = 10 V_{PP}

図 8-25. G = –5 V/V Pulse Response



V_O = 20 V_{PP}

図 8-26. G = –5 V/V Pulse Response

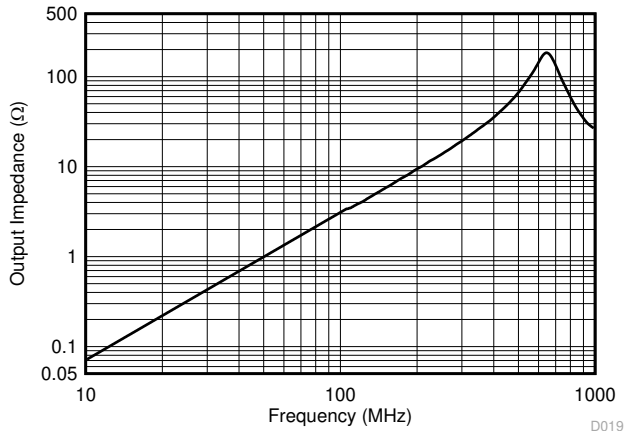


図 8-27. Output Impedance vs Frequency

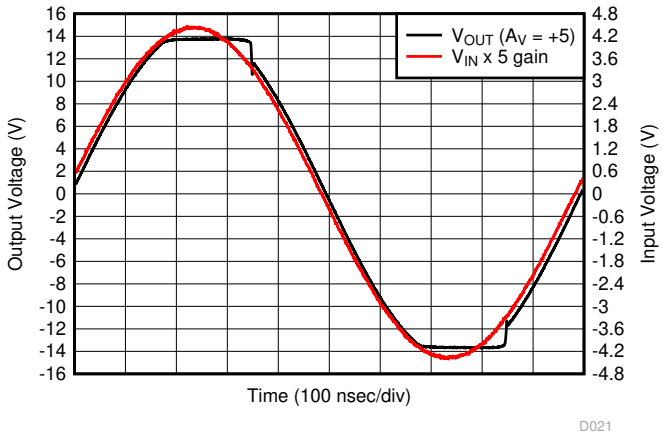
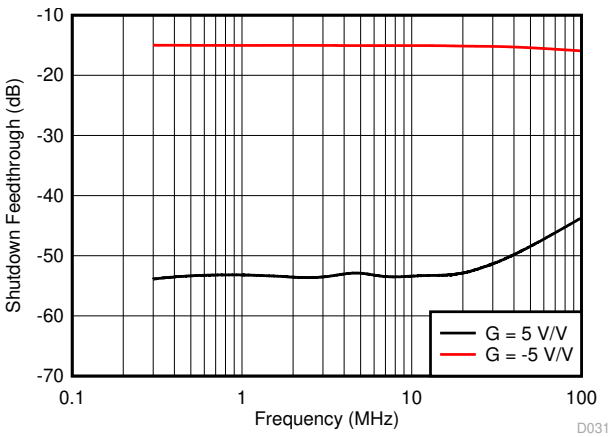


図 8-28. Overdrive Recovery Time



V_{IN} = 2 V_{PP}

図 8-29. Shutdown Feedthrough vs Frequency

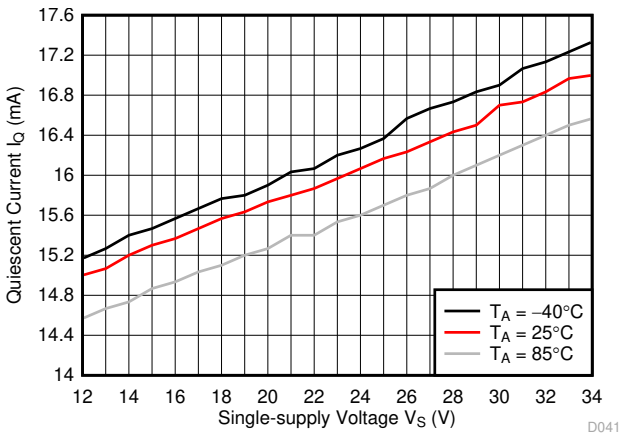
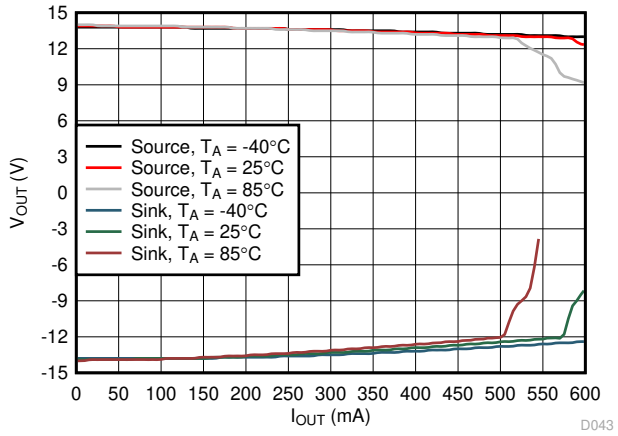


図 8-30. Quiescent Current vs Supply Voltage

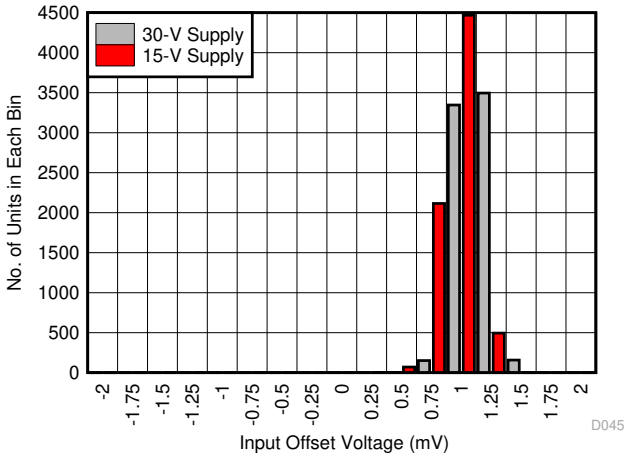
8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



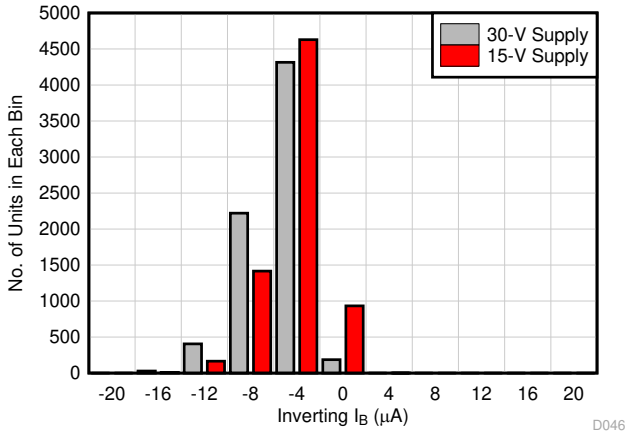
A. Measured with devices soldered on TI EVM. Devices not turned off at any read points but load applied for a few milliseconds to measure V_{OUT} and then removed.

図 8-31. Output Voltage Swing vs Output Current



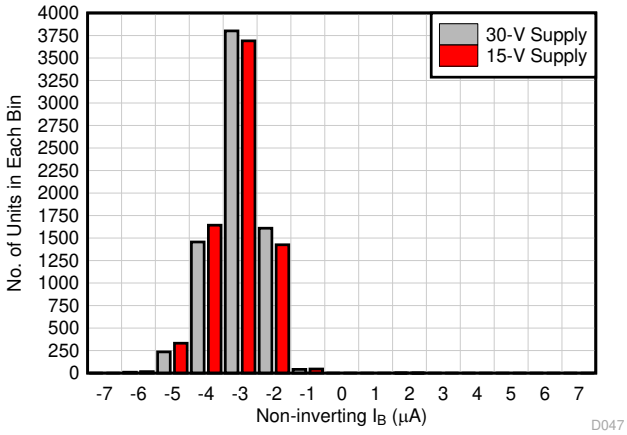
7100 units at each supply

図 8-32. Input Offset Voltage Distribution



7100 units at each supply

図 8-33. Inverting I_B Distribution

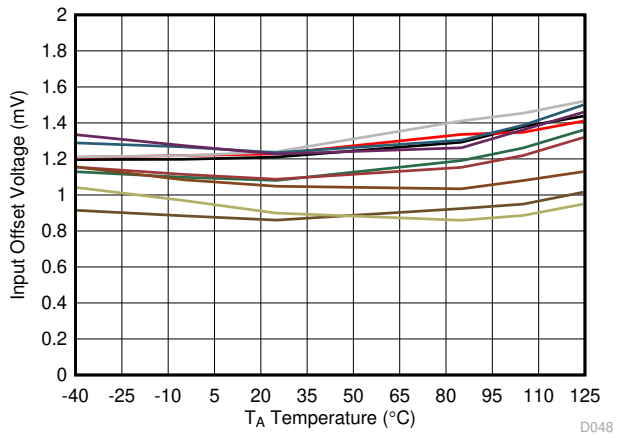


7100 units at each supply

図 8-34. Noninverting I_B Distribution

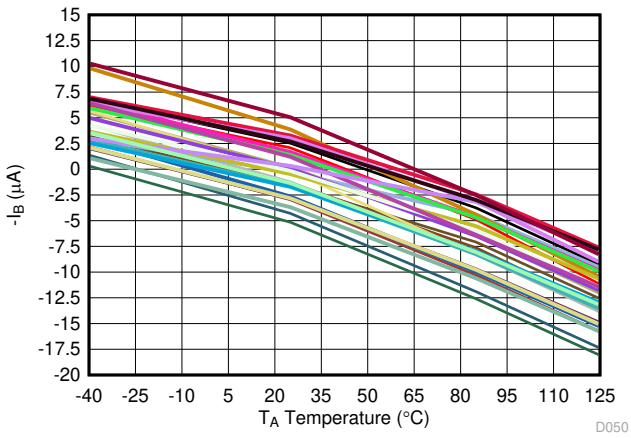
8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



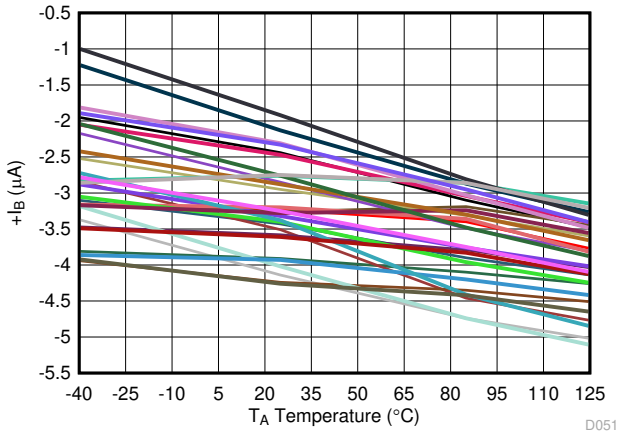
Flash tested to keep T_J as close to T_A as possible

図 8-35. Input Offset Voltage Over Temperature



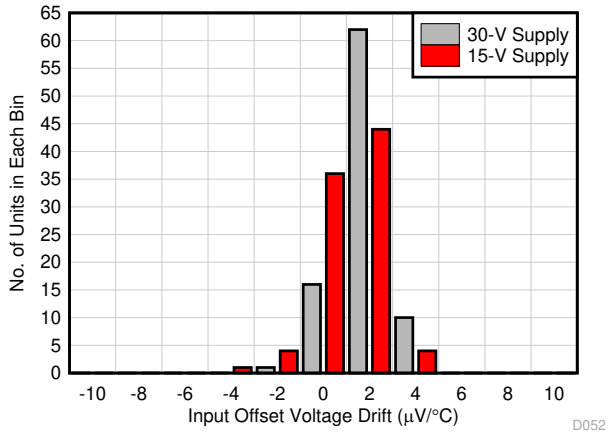
Flash tested to keep T_J as close to T_A as possible

図 8-36. Inverting I_B Over Temperature



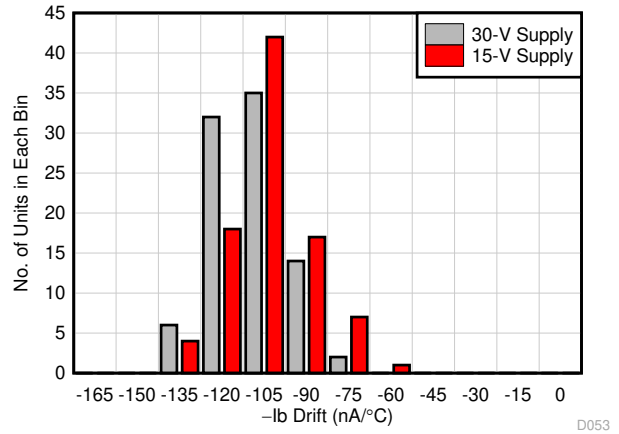
Flash tested to keep T_J as close to T_A as possible

図 8-37. Noninverting I_B Over Temperature



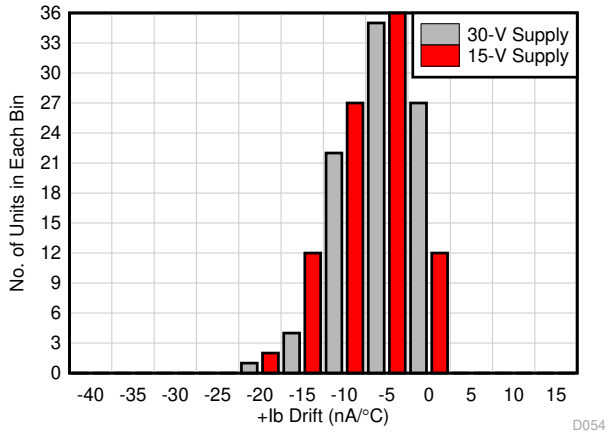
90 units at each supply

図 8-38. Input Offset Voltage Drift Histogram



90 units at each supply

図 8-39. Inverting I_B Drift Histogram

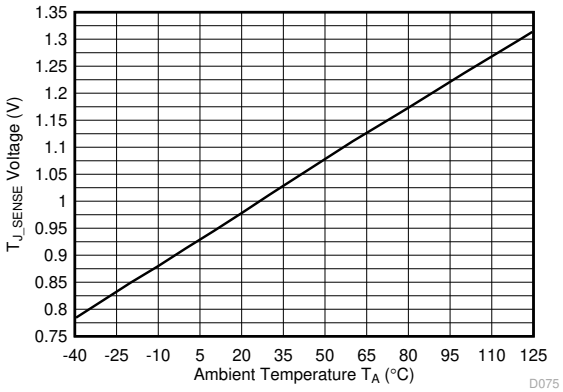


90 units at each supply

図 8-40. Noninverting I_B Drift Histogram

8.7 Typical Characteristics: ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V. RGT package : R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

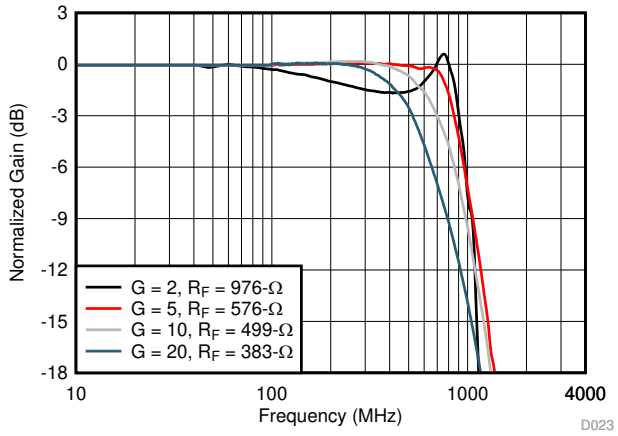


Device in shutdown mode to minimize self-heating, RGT package

図 8-41. T_{J_SENSE} Voltage vs Ambient Temperature

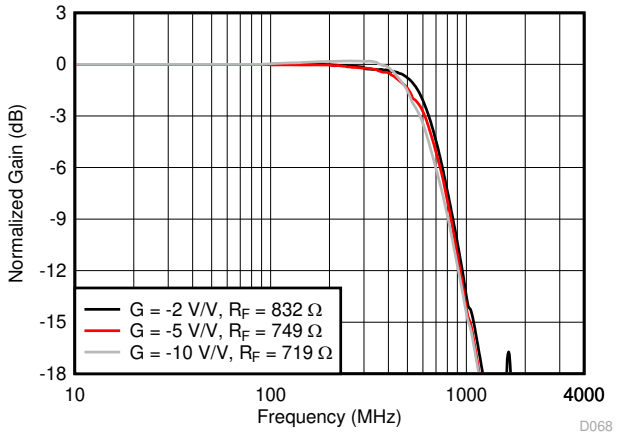
8.8 Typical Characteristics: ±7.5 V

at $+V_S$ = 7.5 V, $–V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



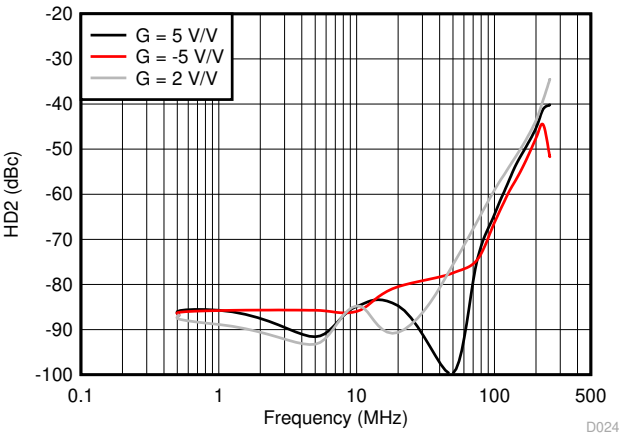
V_O = 2 V_{PP}

図 8-42. Noninverting Small-Signal Frequency Response



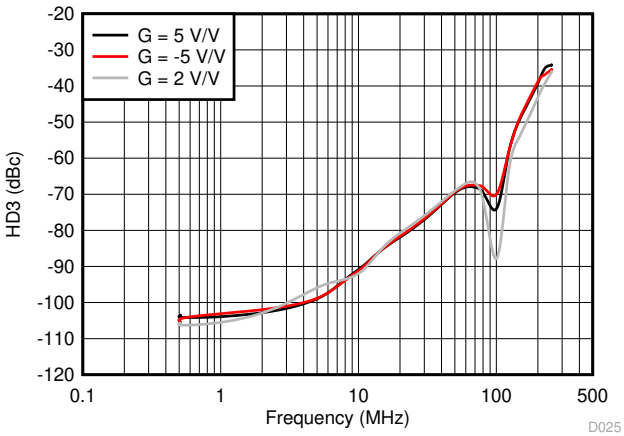
V_O = 2 V_{PP}

図 8-43. Inverting Small-Signal Frequency Response



V_O = 2 V_{PP}

図 8-44. HD2 vs Frequency



V_O = 2 V_{PP}

図 8-45. HD3 vs Frequency

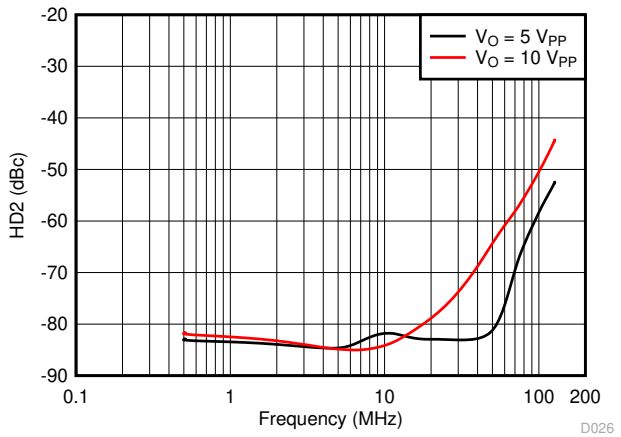


図 8-46. HD2 vs Frequency Across Output Swing

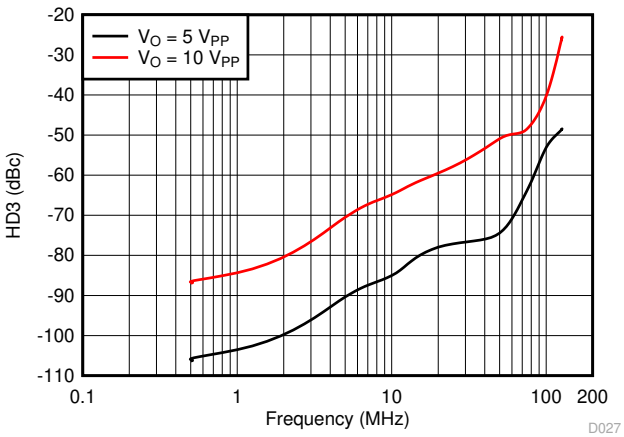


図 8-47. HD3 vs Frequency Across Output Swing

8.8 Typical Characteristics: ±7.5 V (continued)

at $+V_S$ = 7.5 V, $–V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

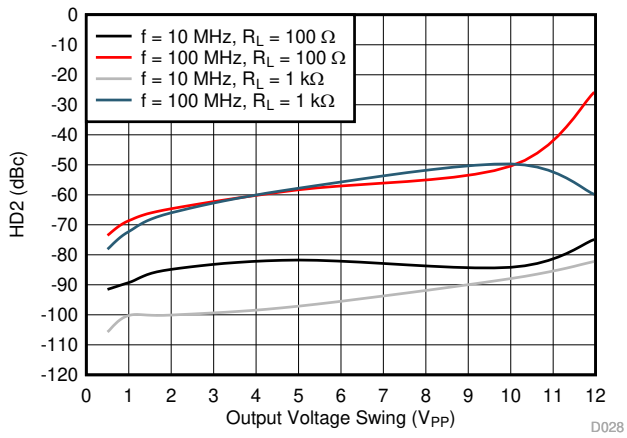


図 8-48. HD2 vs Output Swing

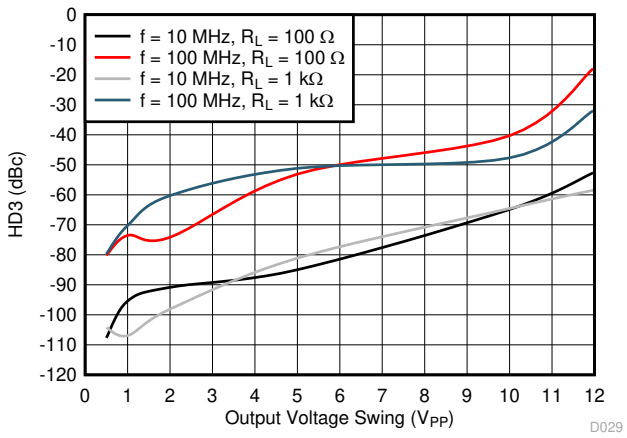
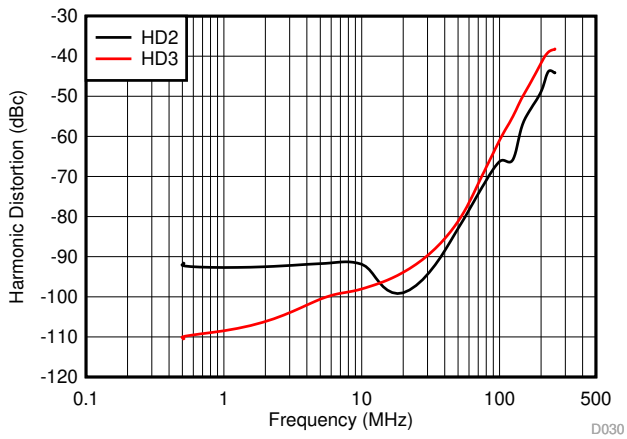
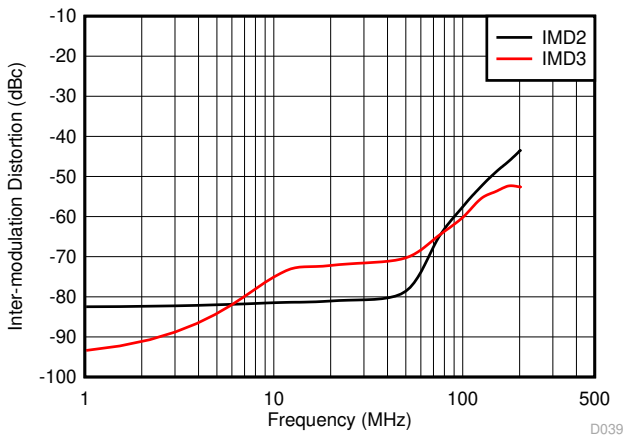


図 8-49. HD3 vs Output Swing



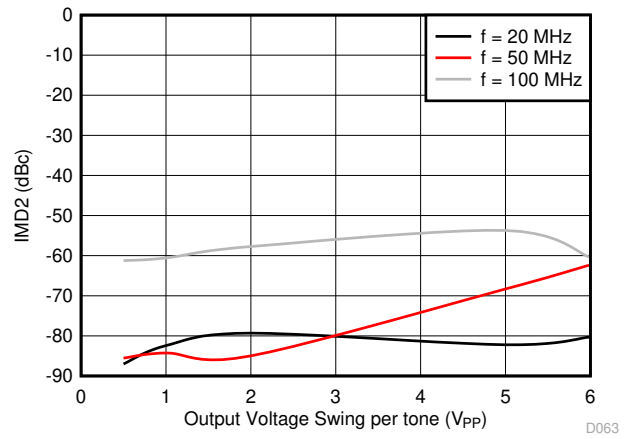
V_O = 2 V_{PP} R_{LOAD} = 1 kΩ

図 8-50. Harmonic Distortion vs Frequency



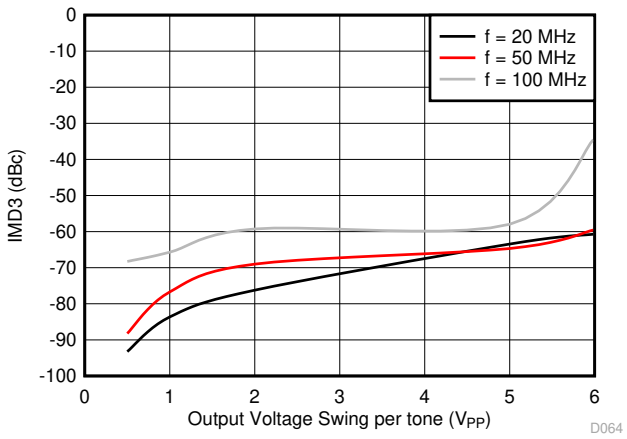
V_O = 2.5 V_{PP} per tone ±100-kHz frequency spacing

図 8-51. Intermodulation Distortion vs Frequency



±100-kHz frequency spacing

図 8-52. IMD2 vs Output Voltage Swing

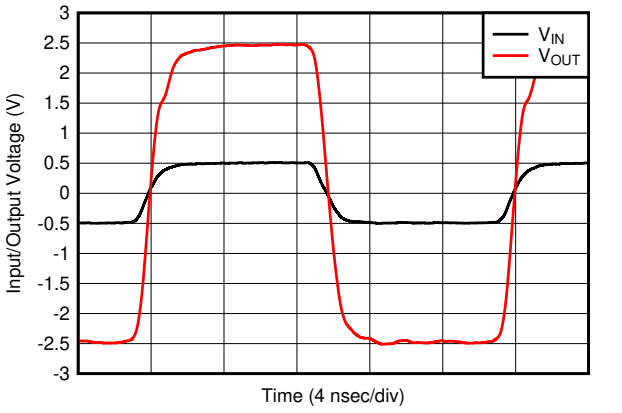


±100-kHz frequency spacing

図 8-53. IMD3 vs Output Voltage Swing

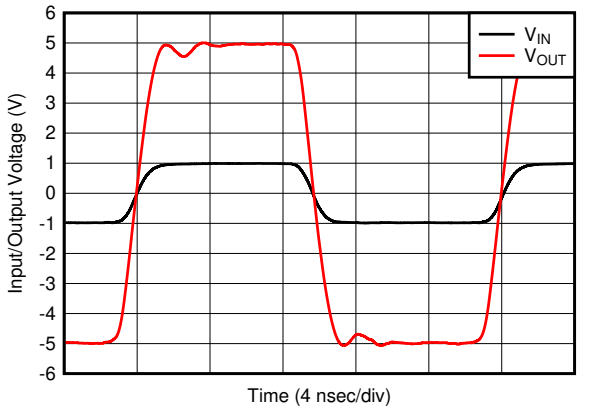
8.8 Typical Characteristics: ±7.5 V (continued)

at $+V_S$ = 7.5 V, $–V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



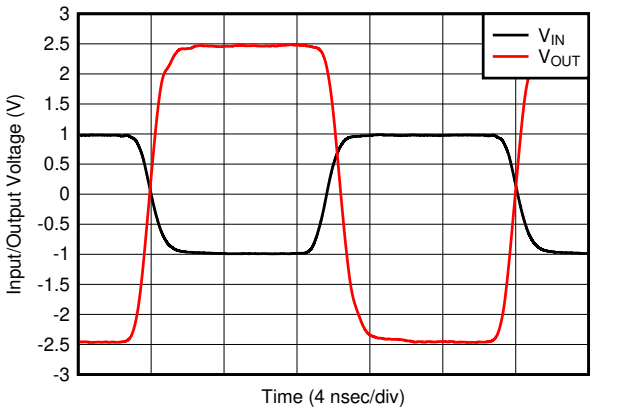
V_O = 5 V_{PP}

図 8-54. G = 5 V/V Pulse Response



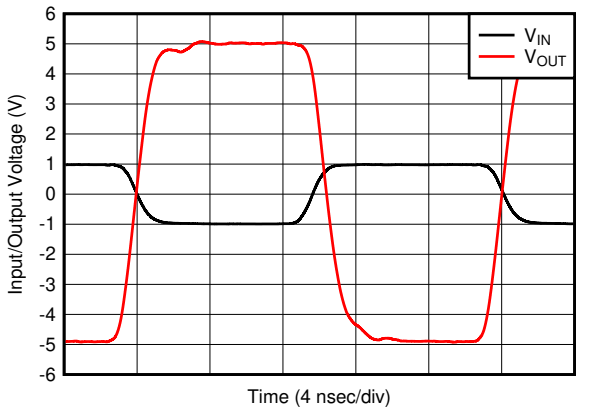
V_O = 10 V_{PP}

図 8-55. G = 5 V/V Pulse Response



V_O = 5 V_{PP}

図 8-56. G = –5 V/V Pulse Response



V_O = 10 V_{PP}

図 8-57. G = –5 V/V Pulse Response

8.8 Typical Characteristics: ±7.5 V (continued)

at $+V_S$ = 7.5 V, $–V_S$ = –7.5 V, T_A ≅ 25°C, R_{LOAD} = 100 Ω to midsupply, noninverting gain (G) = 5 V/V RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

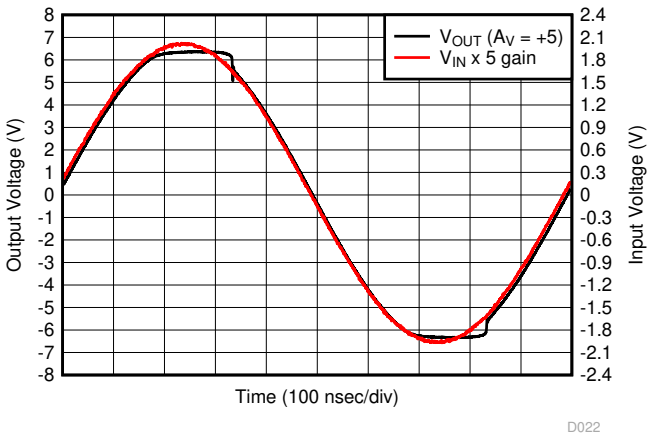
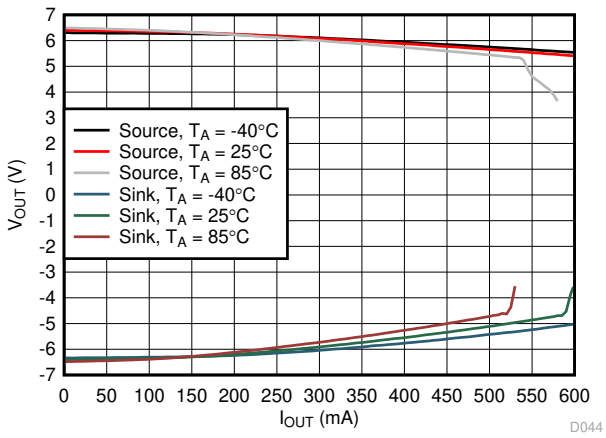
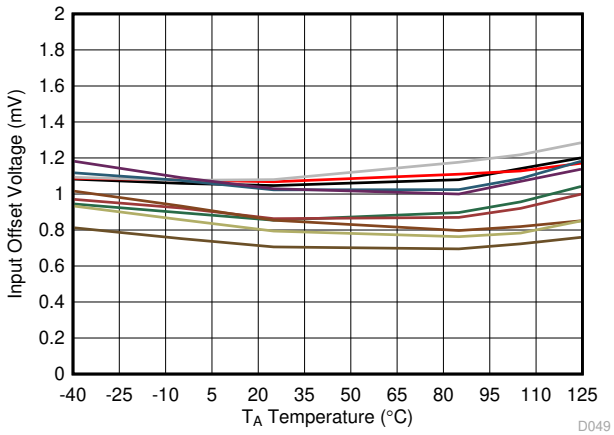


図 8-58. Overdrive Recovery Time



Measured with devices soldered on TI EVM. Devices not turned off at any read points but load applied for a few msec to measure V_{OUT} and then removed.

図 8-59. Output Voltage Swing vs Output Current



Flash tested to keep T_J as close to T_A as possible

図 8-60. Input Offset Voltage Over Temperature

9 Detailed Description

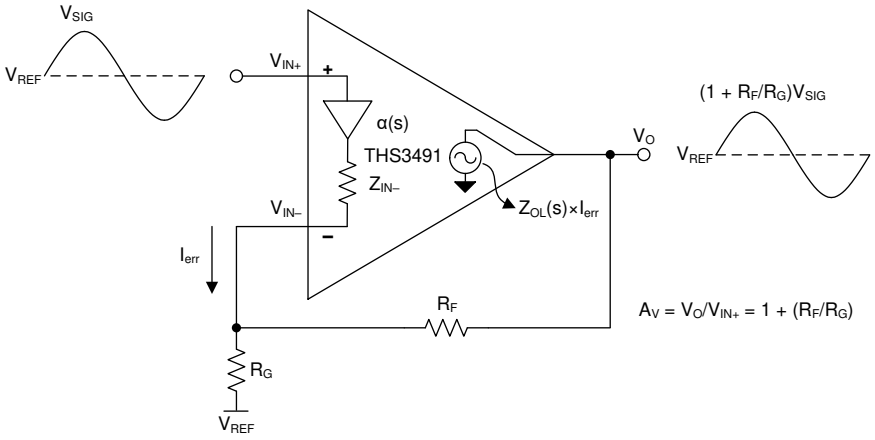
9.1 Overview

The THS3491 is a high-voltage, low-distortion, high-speed, current-feedback amplifier designed to operate over a wide supply range of ±7 V to ±16 V for applications requiring large, linear output swings such as arbitrary waveform generators.

The THS3491 features a power-down pin that puts the amplifier in low power standby mode and lowers the quiescent current from 16.7 mA to 750 µA.

The RGT package also features a feedback pin (pin 1). Internally on the die this pin is connected to the amplifier's output. This feedback pin arrangement minimizes the PCB trace lengths in the feedback path for the connection from the feedback resistor to the inverting input and output pins. This in turn minimizes the board parasitics in the feedback path, thus allowing to maximize bandwidth with minimal peaking.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Down ($\overline{PD}$) Pin

The THS3491 features a power-down ($\overline{PD}$) pin that lowers the quiescent current from 16.7 mA down to 750 µA, which is designed to reduce system power.

The power-down pin of the amplifier defaults to 2 V below the positive supply voltage in the absence of an externally applied voltage, which places the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be pulled low. The $\overline{PD}$ pin threshold voltages are specified with respect to the REF pin voltage. The threshold voltages for power on and power down are relative to the REF pin and are shown in the *セクション 8.5* and *セクション 8.6* tables. Above the enable threshold voltage, the device is on. Below the disable threshold voltage, the device is off. The behavior is not specified between these threshold voltages.

This power-down functionality helps the amplifier consume less power in power-down mode. Power-down mode is not intended to provide a high-impedance output. The power-down functionality is not intended for use as a tri-state bus driver. In power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device varies depending on the voltage applied to the outputs.

As with most current-feedback amplifiers, the internal architecture places limitations on the system in power-down mode. The most common limitation is that the amplifier turns on if there is a ±1 V or greater difference between the two input nodes (VIN+ and VIN–) of the amplifier. If this difference exceeds ±1 V, the amplifier creates an output voltage equal to approximately [(VIN+ – VIN–) –0.7 V] × gain. Conversely if a voltage is applied to the output while in power-down mode, the VIN– node voltage is equal to $V_{O(applied)} \times R_G / (R_F + R_G)$. For low-gain configurations and a large applied voltage at the output, the amplifier may turn on because of the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 10% or 90% of the final output voltage. The time delays are in nanoseconds during power on and microseconds during power off because the amplifier moves out of linear operating mode for power-off conditions.

9.3.2 Power-Down Reference (REF) Pin

In addition to the power-down pin, the DDA package features a reference pin (REF) that allows control over the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. This reference pin is explicitly pinned out on the DDA package as the REF pin. However, on the RGT package, the reference pin refers to pin 5 (GND), which must be connected to GND. In most split-supply applications, the reference pin is connected to ground. In either case, be aware of voltage-level thresholds that apply to the power-down pin. 表 9-1 provides examples and shows the relationship between the reference voltage and the power-down thresholds. In 表 9-1, the threshold levels are derived by the conditions that follow:

- $\overline{PD} \leq$ REF + 0.8 V (Disable)
- $\overline{PD} \geq$ REF + 1.5 V (Enable)

where the usable range at the REF pin is:

- $V_{S–} \leq V_{REF} \leq (V_{S+} – 5\ V)$

表 9-1. Example Power-Down Threshold Voltage Levels

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±15, ±7, 30	0	1.5	0.8
±15	2	3.5	2.8
±15	–2	–0.5	–1.2
±7	1	2.5	1.8
±7	–1	0.5	–0.2
30	15	16.5	15.8
14	7	8.5	7.8

The recommended operating mode is to tie the REF pin to ground for single and split-supply operations, which sets the enable and disable thresholds to 1.5 V and 0.8 V, respectively.

The REF pin must be tied to a valid potential within the recommended operating range of ($–V_S \leq V_{(REF)} \leq +V_S – 5$ V). Although the $\overline{PD}$ pin can be floated, TI does not recommend floating the $\overline{PD}$ pin in case stray signals couple into the pin and cause unintended turnon or turnoff device behavior. However, if the $\overline{PD}$ pin is left unterminated, the $\overline{PD}$ pin floats to 2 V below the positive rail and the device remains enabled. As a result, the THS3491 DDA package is a drop-in replacement for the THS3091 DDA pinout if the REF pin (pin 1) is tied to a valid potential. If balanced, split supplies are used ($\pm V_S$) and the REF and $\overline{PD}$ pins are grounded, the device is disabled.

9.3.3 Internal Junction Temperature Sense (T_{J_SENSE}) Pin

The RGT package includes an internal, junction-temperature sense pin (T_{J_SENSE}). This pin is a temperature-dependent current source from the positive supply into one side of the internal resistor, where the other side of the internal resistor is connected to pin 5 (GND), the $\overline{PD}$ logic reference pin on the die. For simplicity, and to keep the T_{J_SENSE} output ground referenced, tie pin 5 to ground (internally, the $\overline{PD}$ logic reference pin). If pin 5 is tied to a voltage in the same range as the REF pin voltage for the DDA package, the output of the T_{J_SENSE} voltage and input threshold voltages of the $\overline{PD}$ pin are level shifted.

9.4 Device Functional Modes

9.4.1 Wideband Noninverting Operation

The THS3491 is a 900-MHz current-feedback operational amplifier that is designed to operate from a power supply of ±7 V to ±16 V.

図 9-1 shows the THS3491 in a noninverting gain configuration of 5 V/V which is used to generate the majority of the performance curves. Most of the curves are characterized using signal sources with a 50-Ω source impedance and measurement equipment presenting a 50-Ω load impedance.

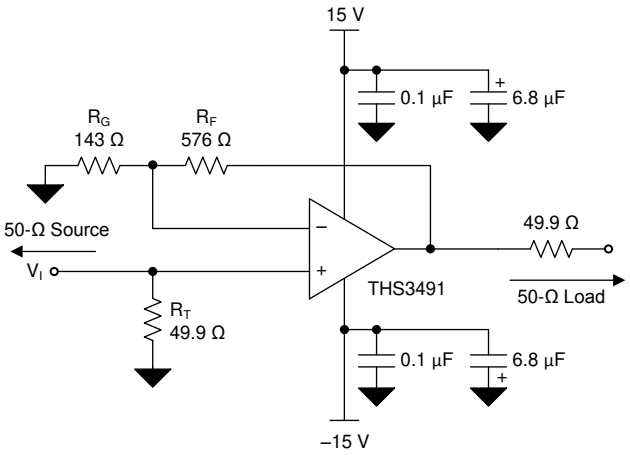


図 9-1. Wideband Noninverting Gain Configuration (5 V/V)

Current-feedback amplifiers are highly dependent on the R_F feedback resistor for maximum performance and stability. 表 9-2 provides the optimal resistor values for R_F and R_G at different gains to achieve maximum bandwidth with minimal peaking in the frequency response. Use lower R_F values for higher bandwidth. Note that this can cause additional peaking and a reduction in phase margin. Conversely, increasing R_F decreases the bandwidth but phase margin increases and stability improves. To gain further insight on the feedback and stability analysis of current-feedback amplifiers like the THS3491, see the Current-feedback Amplifiers section of TI Precision Labs.

表 9-2. Recommended Resistor Values for Minimum Peaking and Optimal Frequency Response With R_{LOAD} = 100 Ω

GAIN (V/V)	RGT PACKAGE		DDA PACKAGE	
	R_G (Ω)	R_F (Ω)	R_G (Ω)	R_F (Ω)
2	976	976	2.1k	2.1k
5	143	576	200	798
10	54.9	499	78.7	704
20	20	383	29.4	564

9.4.2 Wideband, Inverting Operation

図 9-2 shows the THS3491 in a typical inverting gain configuration where the input and output impedances and signal gain from 図 9-1 are retained in an inverting circuit configuration.

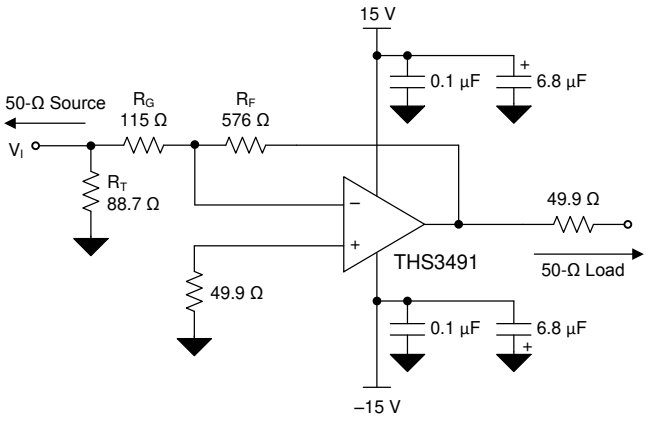


図 9-2. Wideband Inverting Gain Configuration (5 V/V)

9.4.3 Single-Supply Operation

The THS3491 operates from a single-supply voltage ranging from 14 V to 32 V. When operating from a single power supply, biasing the input and output at midsupply allows for the maximum output voltage swing. 図 9-3 shows circuits that display noninverting (a) and inverting (b) amplifiers that are configured for single-supply operation.

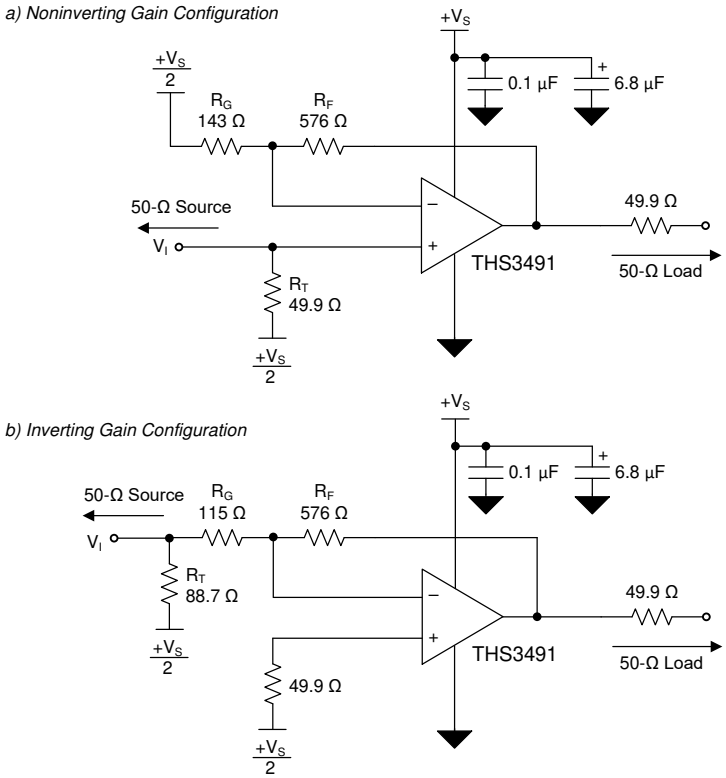


図 9-3. DC-Coupled, Single-Supply Operation

9.4.4 Maximum Recommended Output Voltage

The THS3491 is designed to produce better than 40 dB SFDR while driving a 100-MHz, 20-V_{pp} signal into a 100-Ω load. To accomplish this, the geometries of certain signal path transistors must be limited. As a result of this limitation, some internal devices begin to saturate when large signal levels are input at frequencies greater than 100 MHz. When these devices saturate, the loop opens and the amplifier is no longer in linear operation. This appears as a gain step-up in the frequency response curve. To avoid this phenomenon, applications must comply with the recommended linear operating region shown in 図 9-4. 図 9-4 shows the maximum output voltage vs frequency that is permitted to keep the amplifier in linear operation.

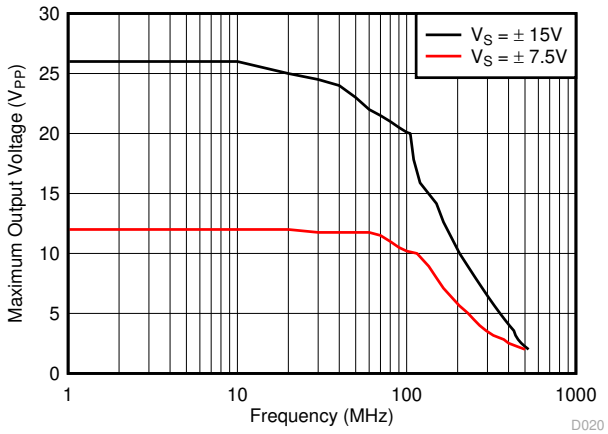


図 9-4. Maximum Recommended Output Voltage vs Frequency

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

10.1.1 Driving Capacitive Loads

Applications such as power JFET and MOSFET (power FET) drivers are highly capacitive and cause stability problems for high-speed amplifiers.

図 10-1 and 図 10-2 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier feedback path. The output impedance of the amplifier in conjunction with C_{LOAD} introduces a pole in the open-loop transimpedance gain response and if the pole is at a frequency lower than the non-dominant pole of the amplifier, then this results in a reduced loop gain and a reduced phase margin. The isolation resistor introduces a zero in the response, which counteracts the effect of the pole. The location of the zero is dependent on the values of R_{ISO} and C_{LOAD}. 図 8-5 shows examples of the recommended R_{ISO} values to achieve flat frequency response while driving certain capacitive loads. See *Effect of Parasitic Capacitance in Op Amp Circuits* for a detailed analysis of selecting isolation resistor values while driving capacitive loads.

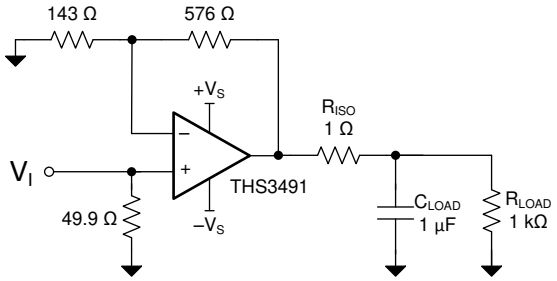


図 10-1. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

Placing a small series resistor (R_{ISO}) between the output of the amplifier and the capacitive load as 図 10-1 shows is a simple way to isolate the load capacitance.

図 10-2 shows two amplifiers in parallel to double the output drive current in order to drive larger capacitive loads. This technique is used when more output current is required to charge and discharge the load faster, such as driving large FET transistors.

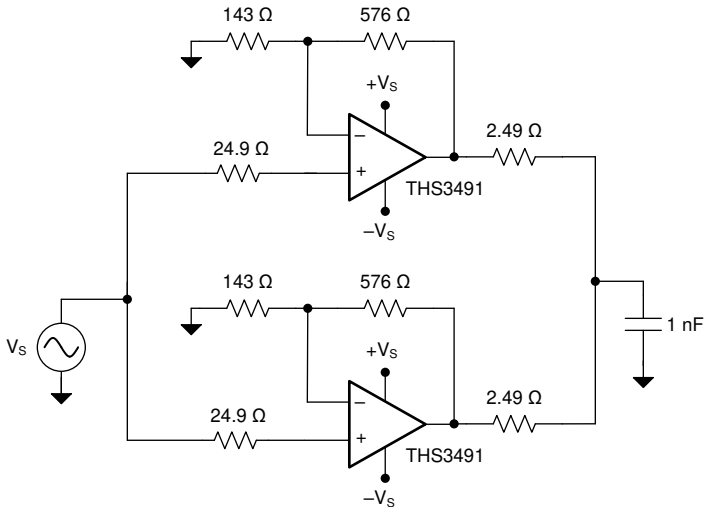


図 10-2. Driving a Large Capacitive Load Using Two Parallel Amplifier Channels

図 10-3 shows a push-pull FET driver circuit commonly used in ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

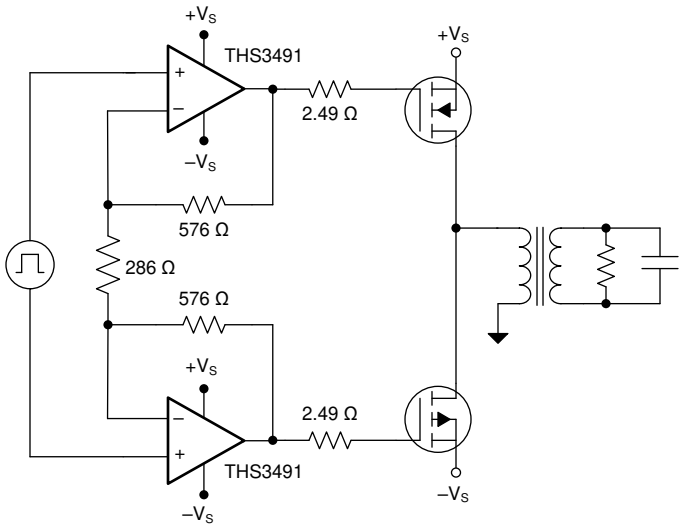


図 10-3. Power FET Drive Circuit

10.1.2 Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3491 meets the demands for video distribution by delivering video signals down multiple cables. For high signal quality with minimal degradation of performance, use a 0.1-dB gain flatness that is at least seven times the pass-band frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal and supports component video and RGB video signals that require fast transition and settling times for high signal quality.

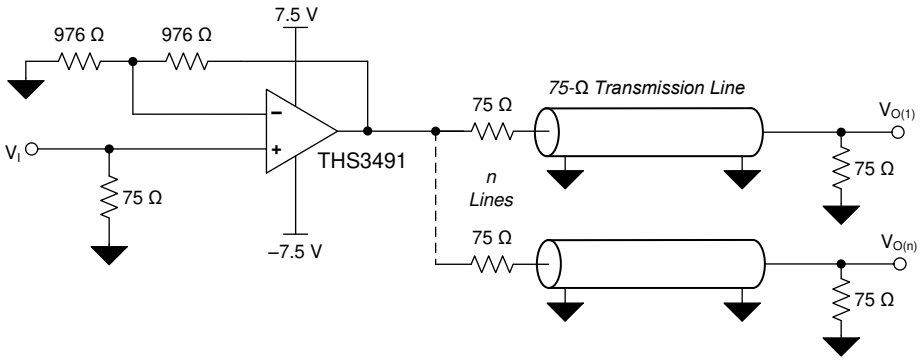


図 10-4. Video Distribution Amplifier Application

10.2 Typical Application

The fundamental concept of load sharing is to drive a load using two or more of the same operational amplifier. Each amplifier is driven by the same source. 図 10-5 shows two THS3491 amplifiers sharing the same load. This concept effectively reduces the current load of each amplifier by 1/N, where N is the number of amplifiers.

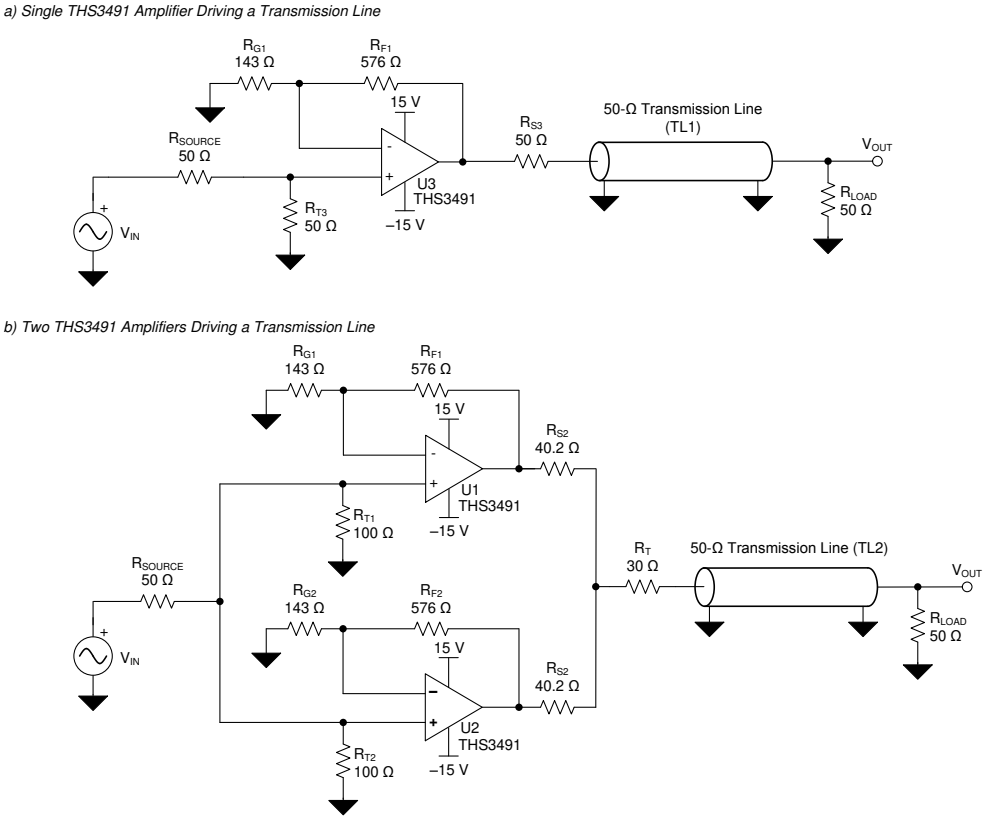


図 10-5. Load-Sharing Driver Application

10.2.1 Design Requirements

Use two THS3491 amplifiers in a parallel load-sharing circuit to improve distortion performance.

表 10-1. Design Parameters

DESIGN PARAMETER	VALUE
V_O (At amplifier output)	20 V_{PP}
R_{LOAD}	100 Ω
Gain flatness at 100 MHz	Less than 0.5 dB

10.2.2 Detailed Design Procedure

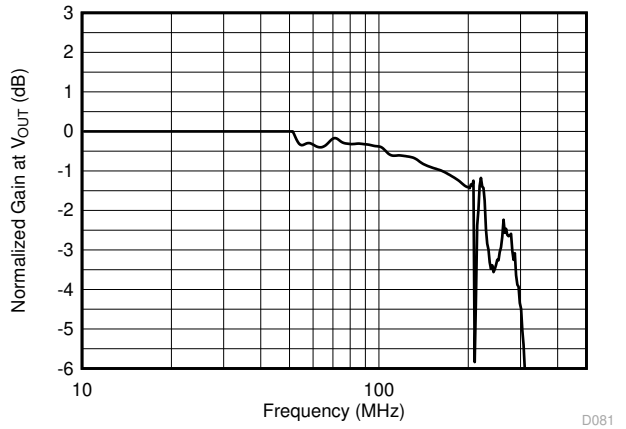
In addition to providing higher output current drive to the load, the load-sharing configuration provides improved distortion performance. In many cases, an operational amplifier shows greater distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor dominates the current load. In a load-sharing configuration of *N* amplifiers in parallel, the equivalent current load that each amplifier drives is 1/N times the total load current. For example, in a two amplifier load- sharing configuration with matching resistance (see 図 10-5) driving a resistive load (R_{LOAD}), the total series resistance (R_{TOT_SERIES}) at the output of the amplifiers is 2 x R_{LOAD} and each amplifier drives 2 x R_{LOAD}. The total series resistance in the two-amplifier configuration shown in 図 10-5 is the parallel combination of R_{S2} resistors in series with R_T resistor (R_{TOT_SERIES} = R_{S2} || R_{S2} + R_T). Such configuration of resistors at the output allows for fault detection if the load is shorted to GND and can be used for filtering the signal going to the load.

図 10-5 shows two circuits: one of a single THS3491 amplifier driving a double-terminated, 50-Ω cable and one of two THS3491 amplifiers in a load-sharing configuration. In the load-sharing configuration, the two 40.2-Ω series output resistors act in parallel and in conjunction with the 30-Ω terminating resistor provide 50-Ω back-matching to the 50-Ω cable.

図 10-6 shows the normalized frequency response for the two-amplifier load-sharing configuration. The total load, R_{TOT_LOAD}, for the configuration is the sum of R_{TOT_SERIES} and R_{LOAD} which is 100 Ω for the two-amplifier configuration in 図 10-5. 図 10-7 shows the distortion performance of the two-amplifier configuration.

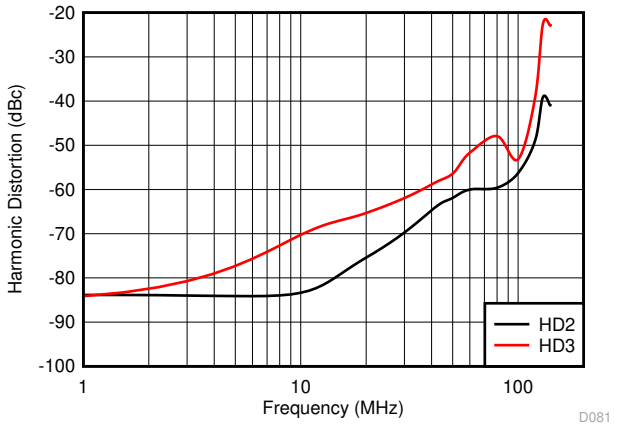
Benefit of the multiple amplifier's in load-sharing configuration becomes even more evident when the total load increases. 図 10-8 and 図 10-9 show the HD2 and HD3 performance, respectively, in two, three, and four amplifier configurations when the R_{TOT_LOAD} = 20 Ω. HD2 improves by almost 13 dB and 24 dB, respectively in the three and four amplifier configuration from the two-amplifier configuration, and HD3 shows an improvement of almost 15 and 19 dB in the three and four amplifier configurations, respectively.

10.2.3 Application Curves



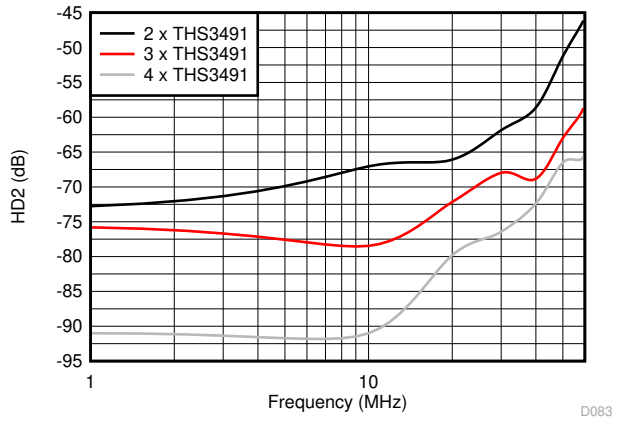
R_{TOT_LOAD} = 100 Ω V_O (amplifier output) = 20 V_{PP}

図 10-6. Frequency Response Of Two-Amplifier Configuration in 図 10-5 (Gain = 5 V/V, Measured At V_{OUT})



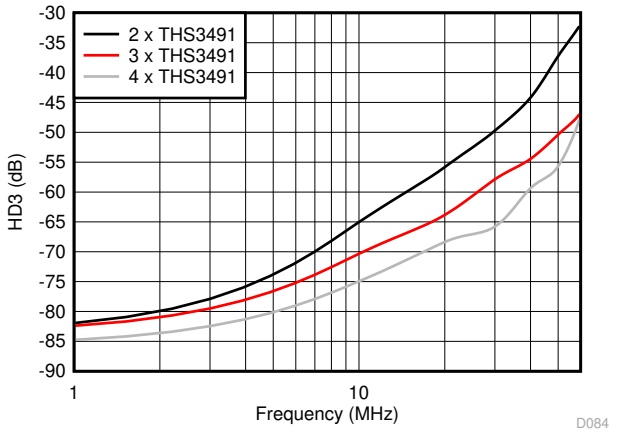
R_{TOT_LOAD} = 100 Ω V_O (amplifier output) = 20 V_{PP}

図 10-7. Distortion Of Two-Amplifier Configuration in 図 10-5 (Gain = 5 V/V, Measured At V_{OUT})



R_{TOT_LOAD} = 20 Ω V_O (amplifier output) = 20 V_{PP}

図 10-8. HD2 For Amplifier Load-Sharing Configuration (Gain = 5 V/V)



R_{TOT_LOAD} = 20 Ω V_O (amplifier output) = 20 V_{PP}

図 10-9. HD2 For Amplifier Load-Sharing Configuration (Gain = 5 V/V)

10.3 Power Supply Recommendations

The THS3491 operates from a single supply or with dual supplies if the input common-mode voltage range (CMIR) has the required headroom (4.3 V) to either supply rail. Supplies must be decoupled with low inductance (often ceramic) capacitors to ground less than 0.5 inches from the device pins. TI recommends using ground planes, and as in most high-speed devices, removing ground planes close to device sensitive pins such as input pins is advisable. An optional supply decoupling capacitor across the two power supplies (for split-supply operation) improves second harmonic distortion performance.

10.4 Layout

10.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS3491 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- Minimize the distance (< 0.25 of an inch [6.35 mm] from the power supply pins to high-frequency 0.1-µF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections must always be decoupled with these capacitors Use larger tantalum decoupling capacitors (with a value of 6.8 µF or more) that are effective at lower frequencies on the main supply pins. These can be placed further from the device and can be shared among several devices in the same area of the printed circuit board (PCB).
- Careful selection and placement of external components preserve the high-frequency performance of the THS3491. Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Keep leads and PCB trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close to the inverting input pins and output pins as possible, respectively. Place other network components such as input termination resistors close to the gain setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values create significant time **constants** constraints? that can degrade performance. Good axial metal film or surface-mount resistors feature approximately 0.2 pF capacitance in shunt with the resistor. For resistor values greater than 2 kΩ, this parasitic capacitance adds a pole or a zero that can effect circuit operation. Keep resistor values as low as possible and consistent with load-driving considerations.
- Make connections to other wideband devices on the board with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces of 0.05 inch to 0.1 inch (1.3 mm to 2.54 mm), preferably with open ground and power planes around the traces. Estimate the total capacitive load and determine if isolation resistors on the outputs are required. Low parasitic capacitive loads (less than 4 pF) may not require series resistance because the THS3491 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without a series resistance are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required and the 6-dB signal loss intrinsic to a twice-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).
- A 50-Ω environment is not required onboard, and a higher impedance environment improves distortion as shown in the distortion versus load plots; see 図 8-7 and 図 8-8. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3491 is used. A terminating shunt resistor at the input of the destination device is also used. The terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device. This total effective impedance must be set to match the trace impedance.
  If the 6-dB attenuation of a twice-terminated transmission line is unacceptable, a long trace can be series terminated at the source end only. Treat the trace as a capacitive load in this case. This termination does not preserve signal integrity as well as a twice-terminated line. If the input impedance of the destination device is low, there is some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.
- Do not socket a high-speed device like the THS3491. The socket introduces additional lead lengths and pin-to-pin capacitance, which can create a troublesome parasitic network. This can make it achieving a smooth,

stable frequency response impossible. Obtain better results by soldering the THS3491 devices directly onto the board.

10.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations (DDA Package Only)

The THS3491 is available in a thermally-enhanced PowerPAD integrated circuit package. These packages are constructed using a downset leadframe on which the die is mounted, as shown in the (a) and (b) sections of 図 10-10. This arrangement results in the lead frame that is exposed as a thermal pad on the underside of the package, a shown in 図 10-10(c). Because this thermal pad directly contacts the die, achieve efficient thermal performance by providing a good thermal path away from the thermal pad. Devices such as the THS3491 have no electrical connection between the PowerPAD and the die.

The PowerPAD integrated circuit package allows for assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are soldered), the thermal pad can be soldered to a copper area underneath the package. By using thermal paths within this copper area, heat is conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

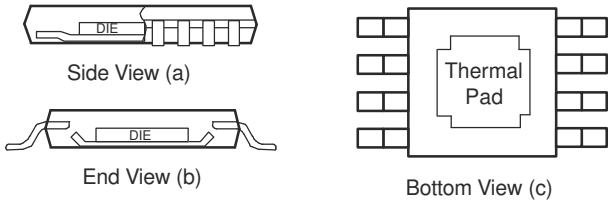


図 10-10. Views of Thermally Enhanced Package

Although there are many ways to properly heat sink the PowerPAD integrated circuit package, see セクション 10.4.1.1.1 for the recommended approach.

10.4.1.1.1 PowerPAD™ Integrated Circuit Package Layout Considerations

The DDA package top-side etch and via pattern is shown in 図 10-11.

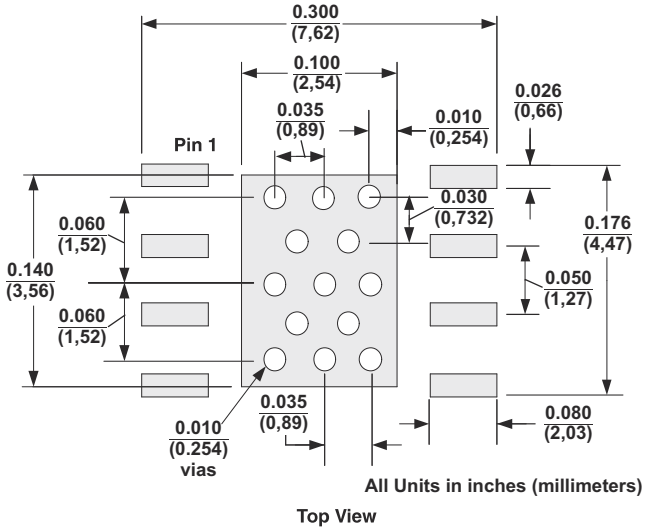


図 10-11. DDA PowerPAD™ Integrated Circuit Package PCB Etch and Via Pattern

1. Use etch for the leads and the thermal pad.
2. Place 13 vias in the thermal pad area. These vias must be 0.01 inch (0.254 mm) in diameter. Keep the vias small so that solder wicking through the vias is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area, and help dissipate the heat generated by the THS3491 device. These additional vias may be larger than the 0.01-inch (0.254 mm) diameter vias directly under the thermal pad because they are not in the area that requires soldering. As a result, wicking is not a problem.
4. Connect all vias to the internal ground plane. The PowerPAD integrated circuit package is electrically isolated from the silicon and all leads. Connecting the PowerPAD integrated circuit package to any potential voltage such as $-V_S$ is acceptable because there is no electrical connection to the silicon.
5. When connecting these vias to the ground plane, do not use the typical web or spoke through connection methodology. Web and spoke connections have a high thermal resistance that slows the heat transfer during soldering . Avoiding these connection methods makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the THS3491 PowerPAD integrated circuit package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the 13 vias exposed.
7. Apply solder paste to the exposed thermal pad area and all of the device pins.
8. With these preparatory steps in place, the device is placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a device that is properly installed.

10.4.1.1.2 Power Dissipation and Thermal Considerations

The THS3491 includes automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature decreases to approximately 145°C, the amplifier turns on again. However, for maximum performance and reliability, make sure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The package and the PCB dictate the thermal characteristics of the device. Maximum power dissipation for a particular package is calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \tag{1}$$

where

- PD_{max} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junction temperature (°C).
- T_A is the ambient temperature (°C).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

The thermal coefficient for the PowerPAD integrated circuit packages are substantially improved over the traditional SOIC package. The data for the PowerPAD packages assume a board layout that follows the PowerPAD package layout guidelines referenced above and detailed in *PowerPAD™ Thermally Enhanced Package*. Maximum power dissipation levels are shown in *Comparison of θ_{JA} for Various Packages*. If the PowerPAD integrated circuit package is not soldered to the PCB, the thermal impedance increases substantially and may cause serious heat and performance issues. Take care to always solder the PowerPAD integrated circuit package to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, make sure to consider not only quiescent power dissipation, but dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation provides visibility into a possible problem.

10.4.2 Layout Example

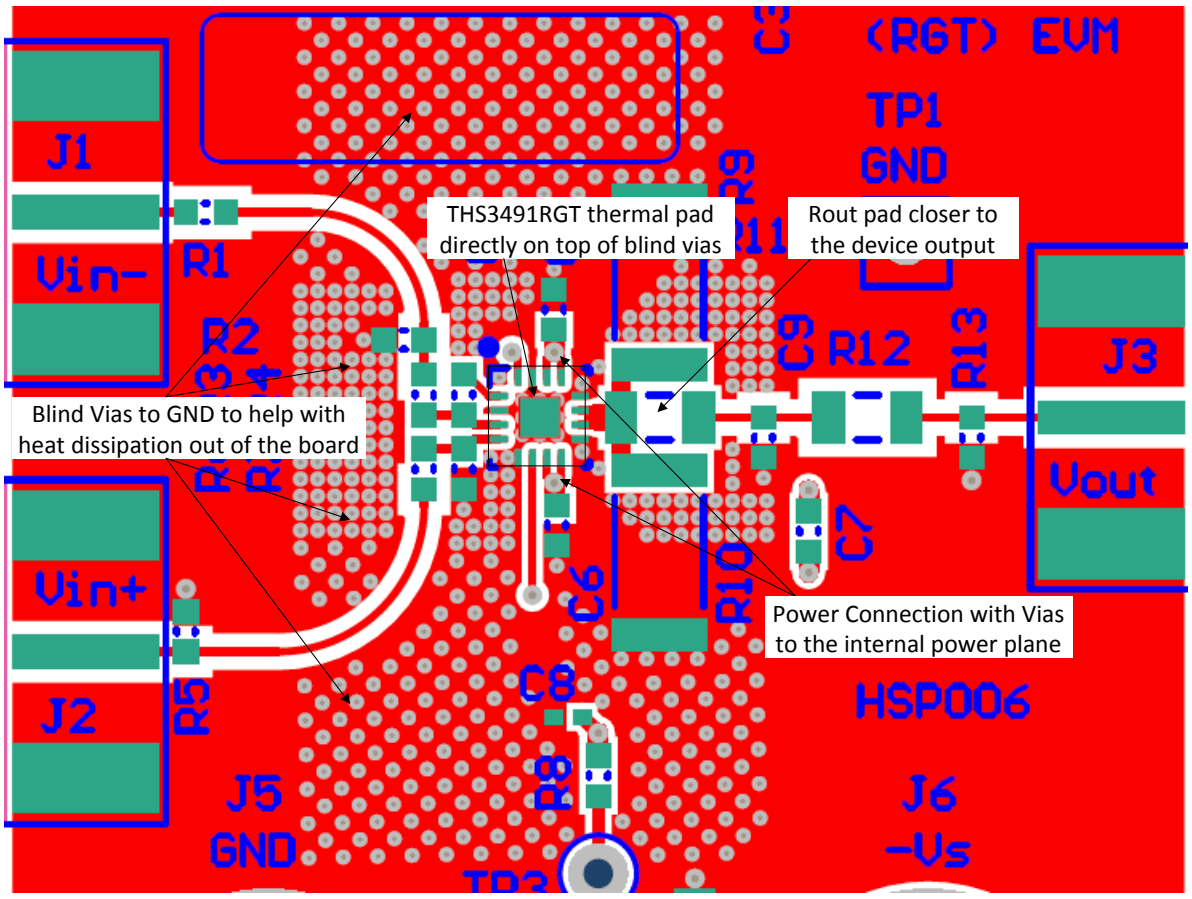


図 10-12. RGT Package Layout Example

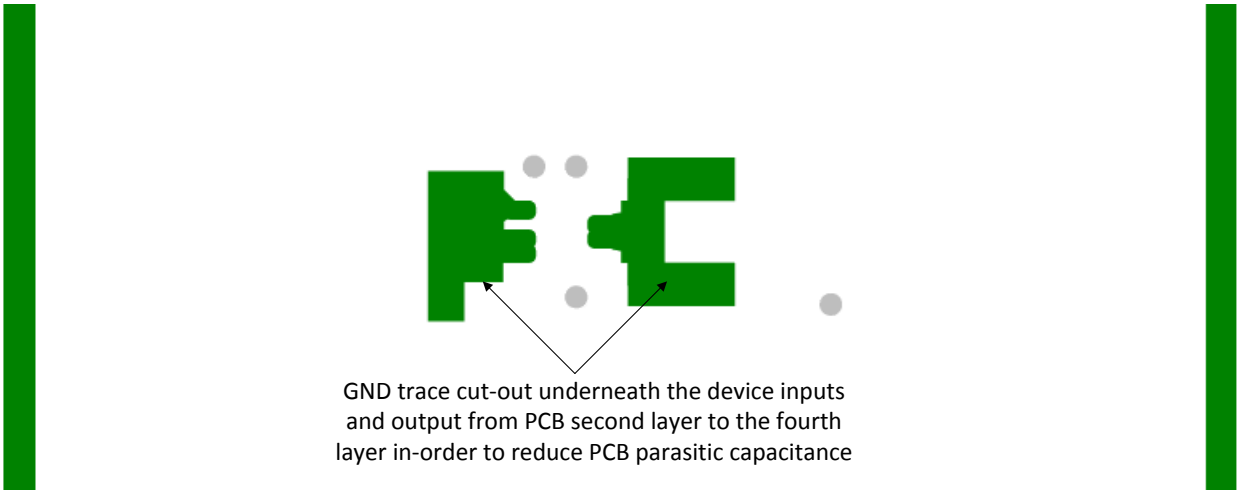


図 10-13. Ground Trace Cutout Beneath the Device Inputs and Output

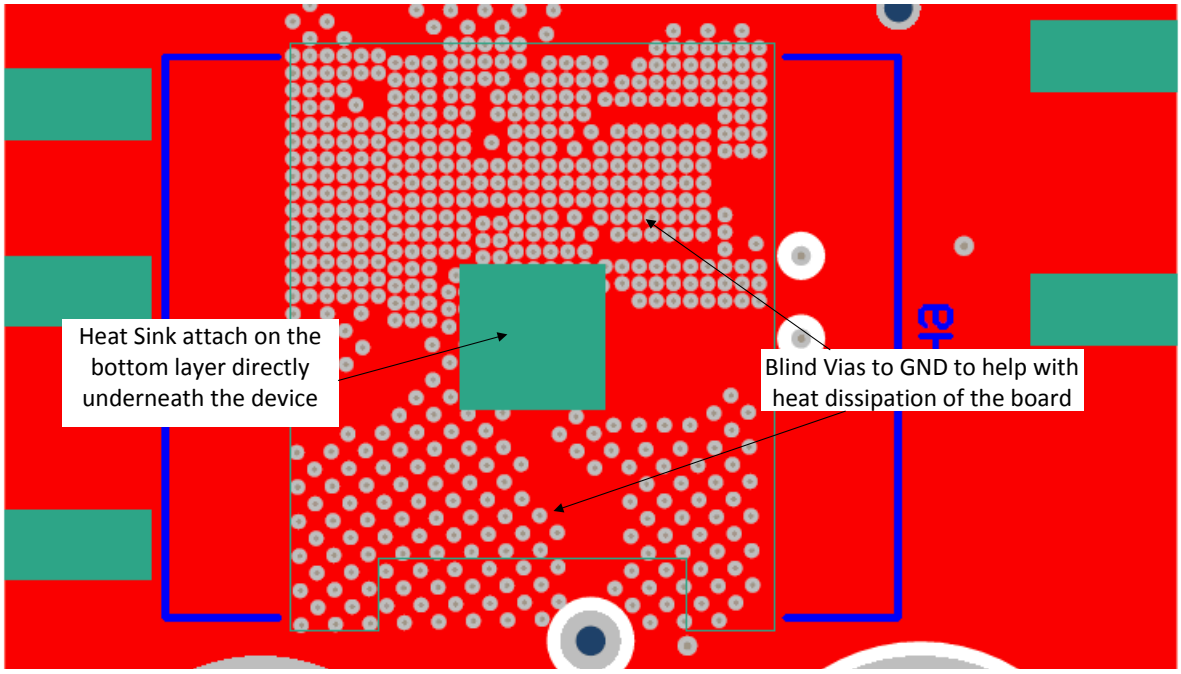


図 10-14. Heat Sink Attachment to Bottom Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD™ Made Easy*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
- Texas Instruments, *Voltage Feedback vs Current Feedback Op Amps*
- Texas Instruments, *Current Feedback Amplifier Analysis and Compensation*
- Texas Instruments, *Current Feedback Amplifiers: Review, Stability Analysis, and Applications*
- Texas Instruments, *Effect of Parasitic Capacitance in Op Amp Circuits*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
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11.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3491IDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAT	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAT.B	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IRGTR	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTR.B	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTRG4	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTRG4.B	Active	Production	VQFN (RGT) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491YR	Active	Production	DIESALE (Y) | 0	3000 | LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 85	
THS3491YR.B	Active	Production	DIESALE (Y) | 0	3000 | LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

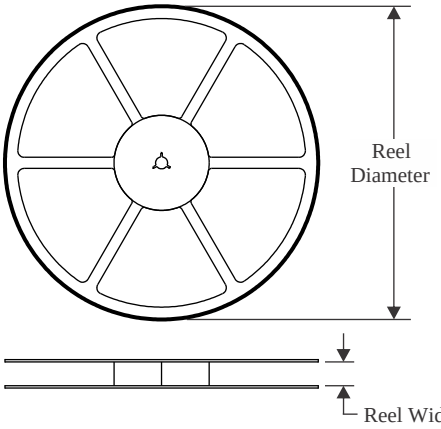
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

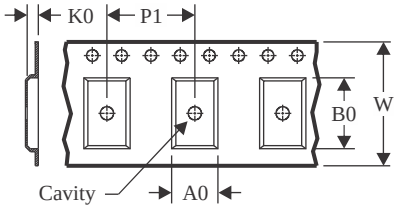
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

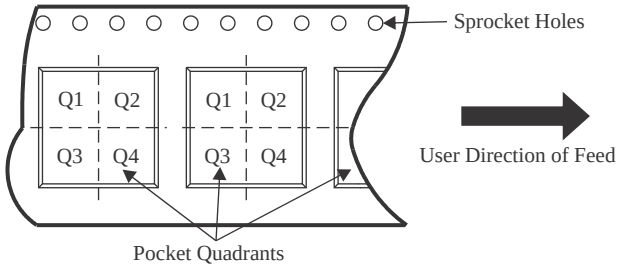


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

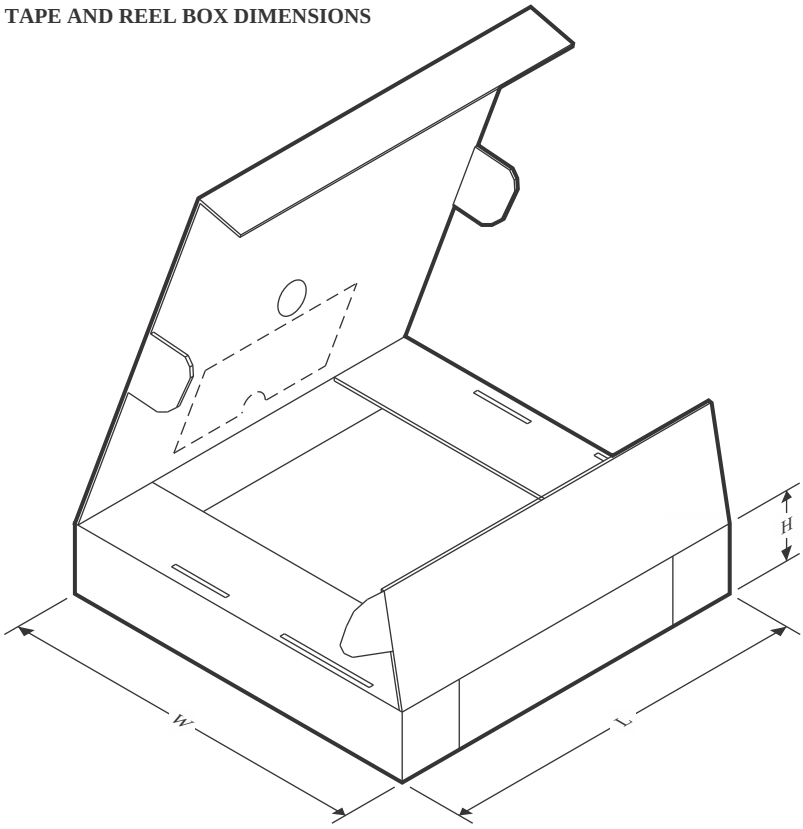
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3491IDDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
THS3491IDDAT	SO PowerPAD	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
THS3491IRGTR	VQFN	RGT	16	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS3491IRGTRG4	VQFN	RGT	16	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS3491IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

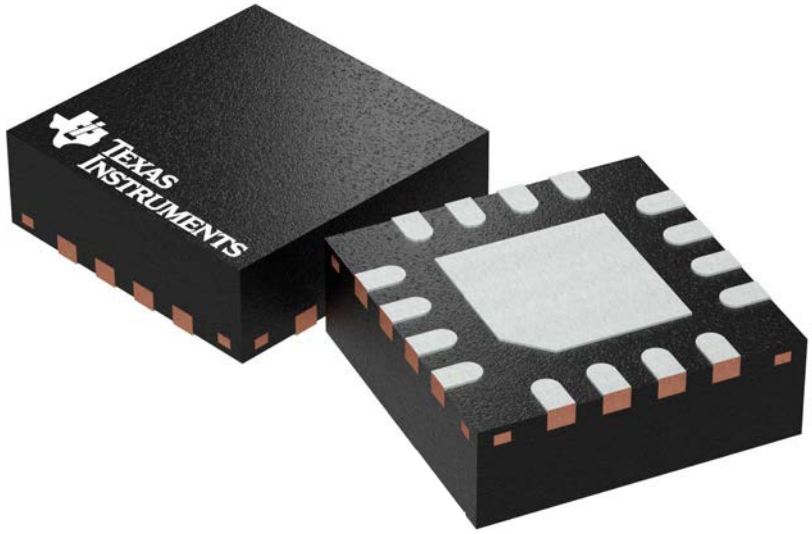


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3491IDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
THS3491IDDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0
THS3491IRGTR	VQFN	RGT	16	2500	346.0	346.0	33.0
THS3491IRGTRG4	VQFN	RGT	16	2500	346.0	346.0	33.0
THS3491IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



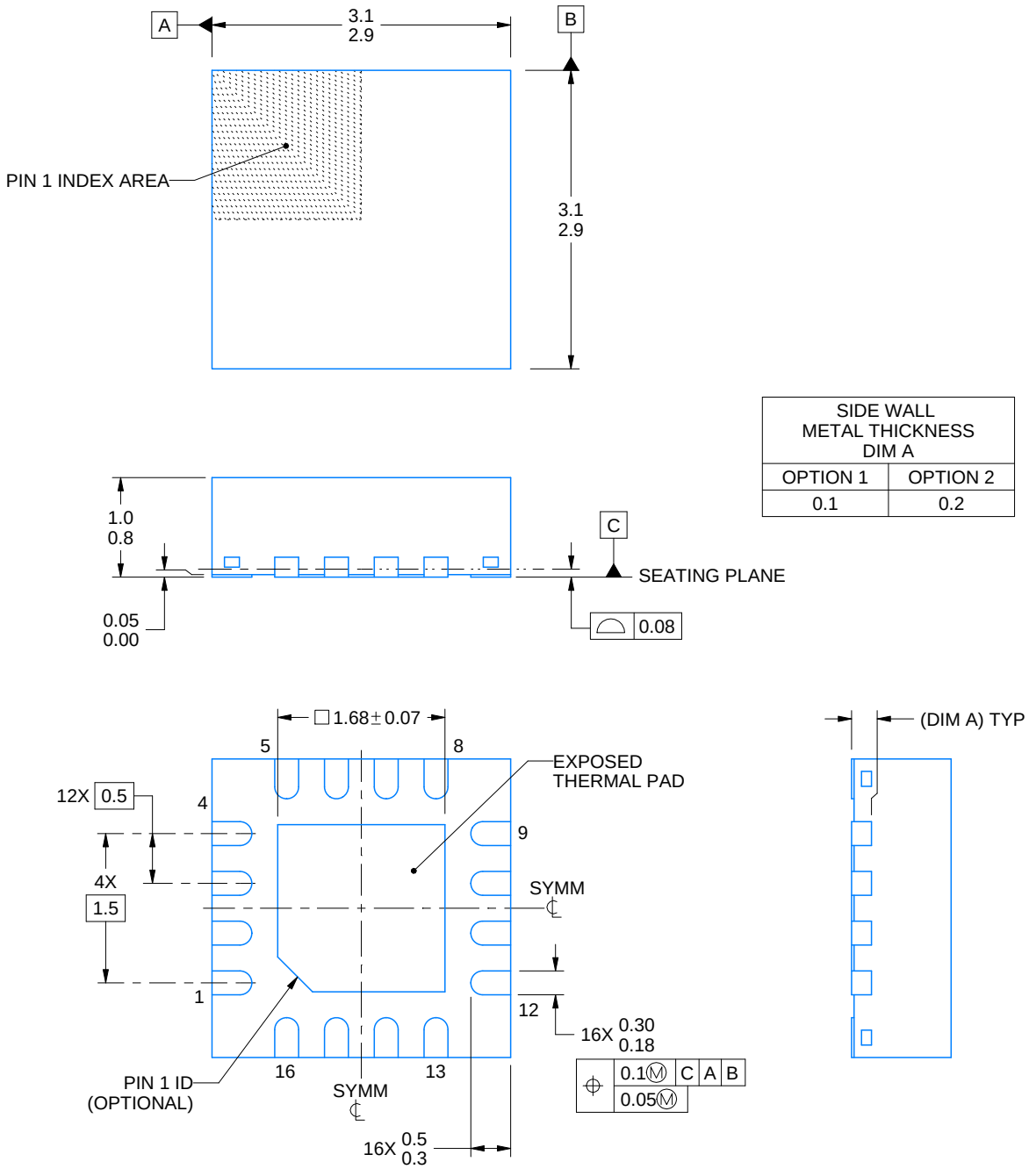
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

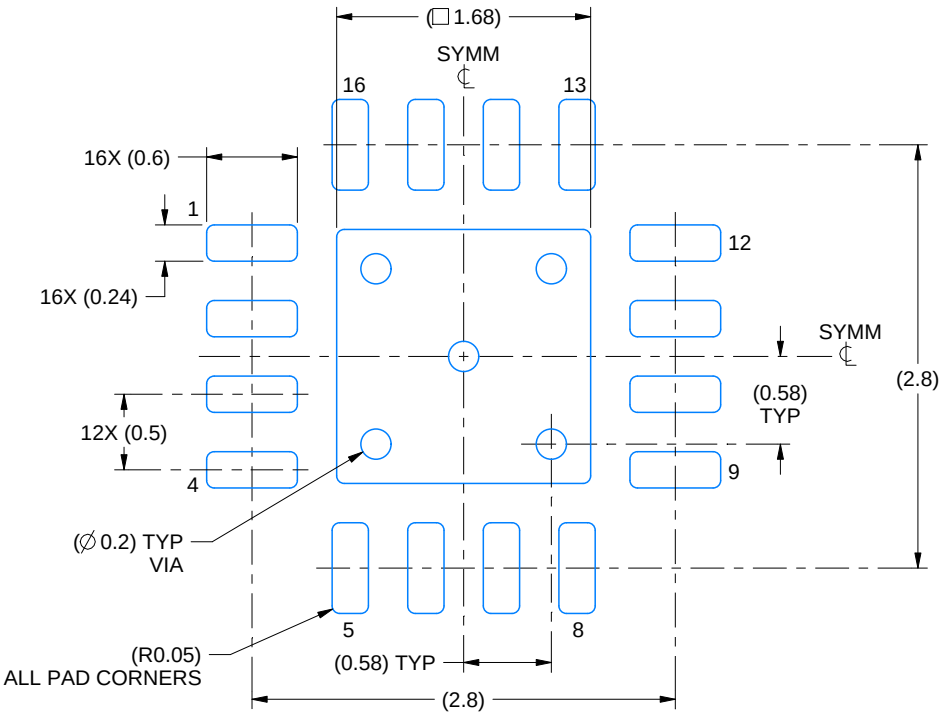
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

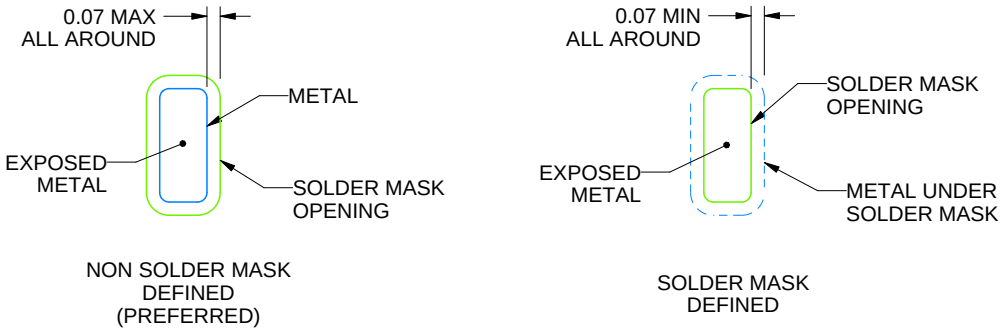


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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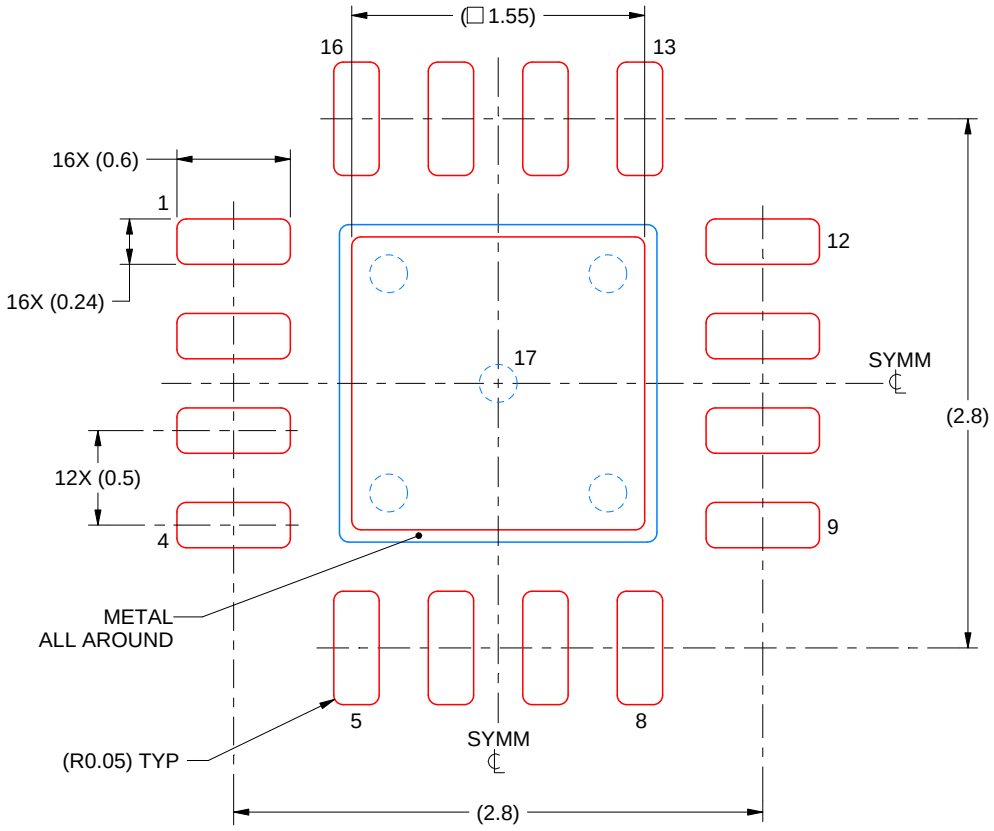
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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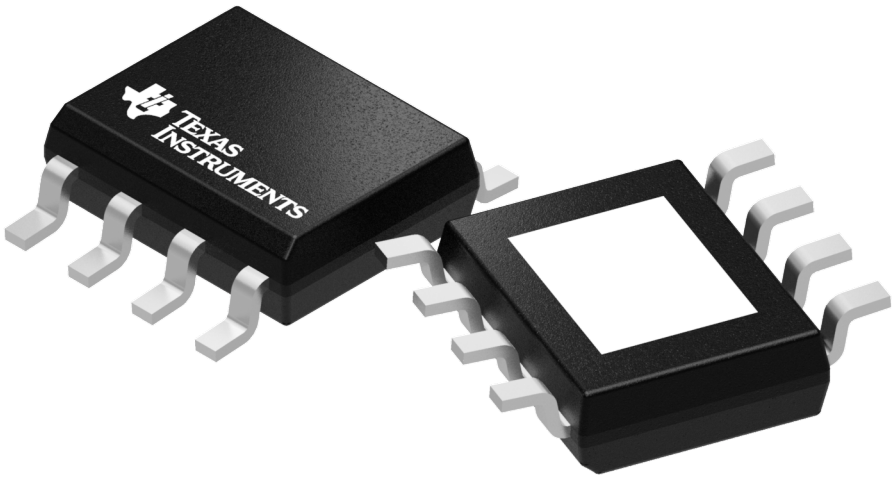
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

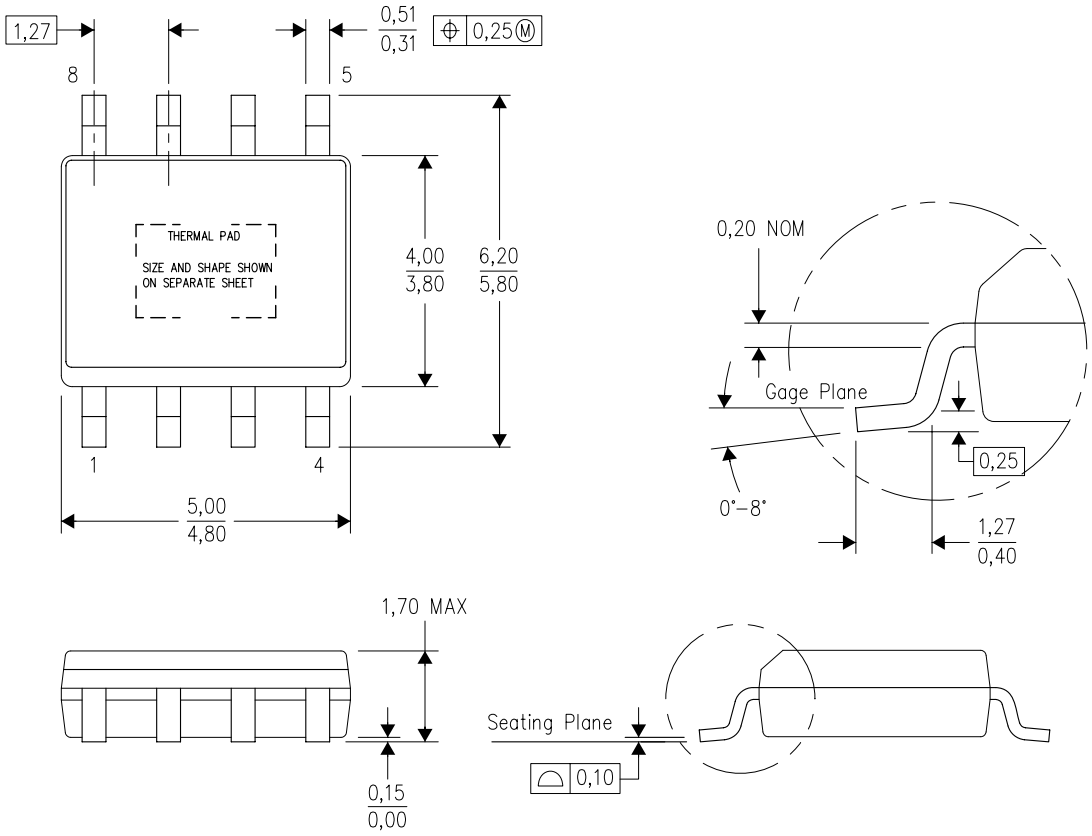
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

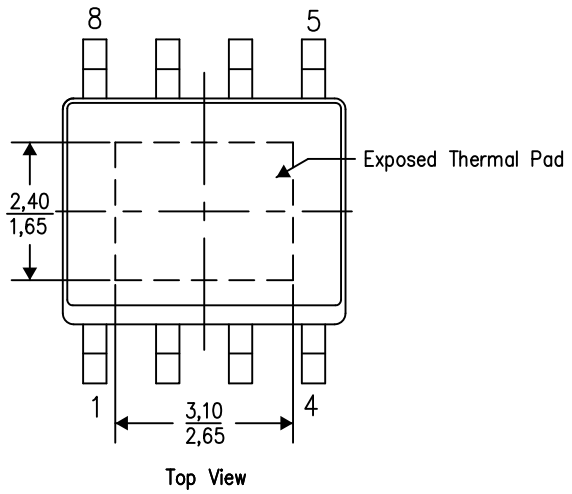
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



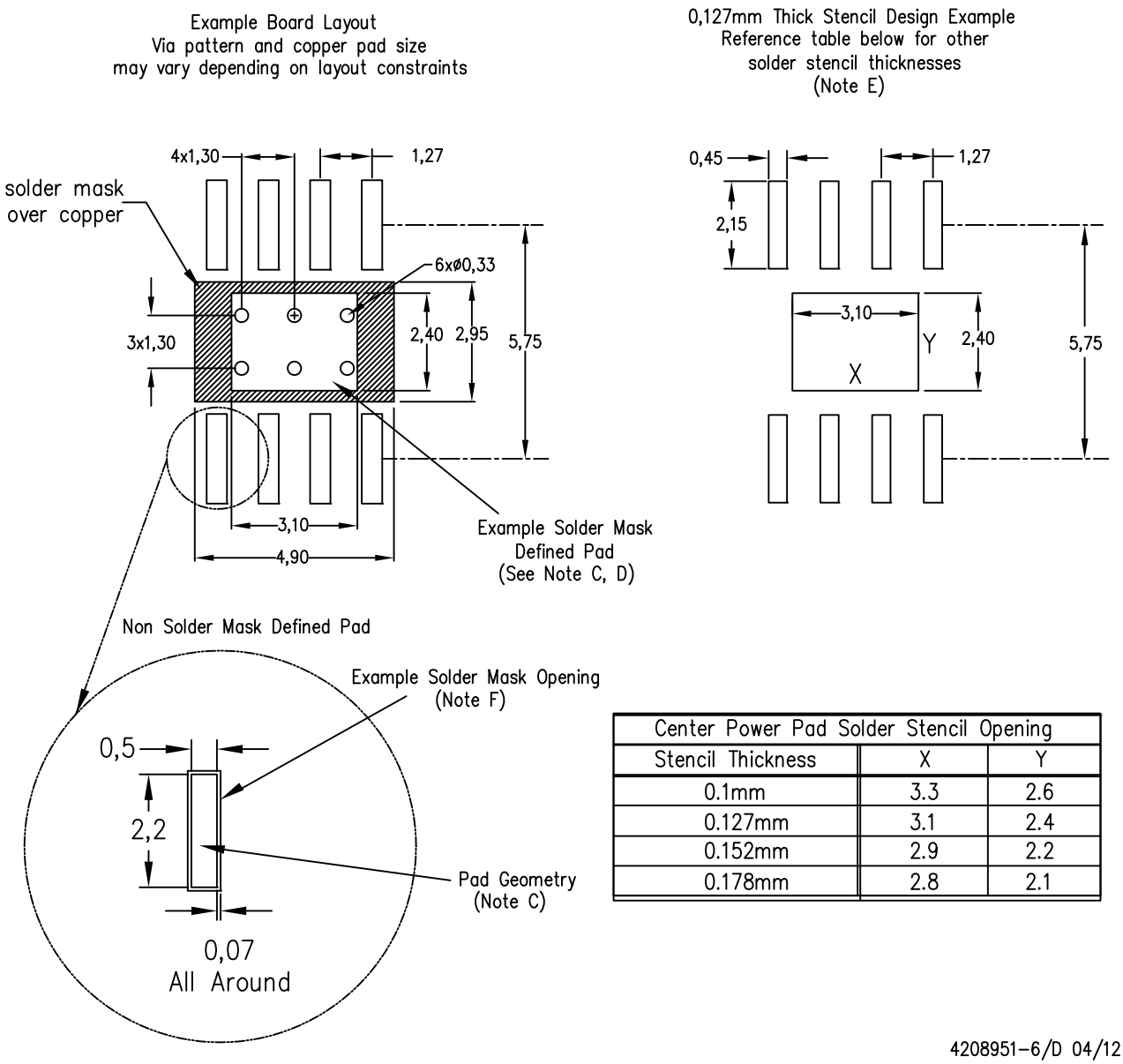
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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