THS4551
低ノイズ、高精度、150MHz 完全差動アンプ

1 特長

- 帯域幅:150MHz (G = 1V/V)
- 差動出力スルーレート:220V/µs
- ゲイン帯域幅積:135MHz
- 負のレール入力(NRI)、
  レール・ツー・レール出力(RRO)
- 広い出力同相制御範囲
- 単一電源動作範囲:2.7V～5.4V
- トリムされた電源電流:5V で 1 .37mA
- 25℃の入力オフセット:±175µV (最大値)
- 入力オフセット電圧ドリフト:±1.8µV/℃ (最大値)
- 差動入力電圧ノイズ:3.3nV/√Hz
- HD2:2V_{PP}、100kHz において -128dBc
- HD3:2V_{PP}、100kHz において -139dBc
- 50ns 未満のセトリング時間:4V ステップで 0.01% まで
- 18 ビットのセトリング時間:4V ステップで 500ns 未満

2 アプリケーション

- 24 ビットのデルタ-シグマ (ΔΣ) ADC ドライバ
- 16～20 ビットの差動高速 SAR ドライバ
- 差動アクティブ・フィルタ
- 差動トランスインピーダンス・アンプ
- THS4521 へのピン互換アップグレード (VSSOP-8 のみ)

3 概要

THS4551 完全差動アンプは、高精度 A/D コンバータ (ADC) に必要な、シングルエンドのソースから差動出力への簡単なインターフェイスとして機能します。このデバイスは、非常に優れた DC 精度、低ノイズ、堅牢な容量性負荷駆動を実現するよう設計されており、データ収集システムにおいて、高い精度が必要で、かつアンプと ADC の組み合わせによって最高の信号対雑音比 (SNR) やスプリアスフリー・ダイナミックレンジ (SFDR) が要求される場合に最適です。

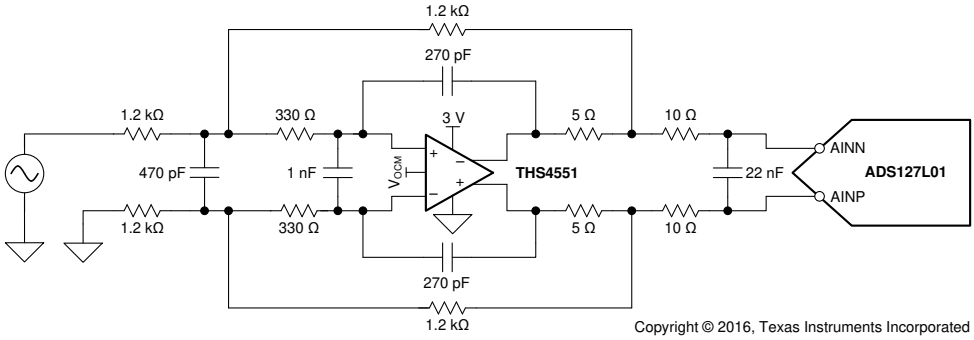
THS4551 には、DC 結合、グランド中心のソース信号と、単一電源の差動入力 ADC とを接続するために必要な、負のレール入力の機能があります。DC 誤差とドリフト係数が非常に低いため、最新の 16～20 ビットの逐次比較型レジスタ (SAR) の入力要件を満たすことができます。広い範囲の出力同相制御により、1.8V～5V の電源で動作する ADC をサポートし、ADC 同相入力要件は 0.7V から 3.0V 以上まで対応できます。

THS4551 デバイスは -40℃～+125℃の広い温度範囲にわたって動作が定義されており、8 ピンの VSSOP、16 ピンの VQFN および 10 ピンの WQFN パッケージで供給されます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
THS4551	VSSOP (8)	3.00mm × 3.00mm
	WQFN (10)	2.00mm × 2.00mm
	VQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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概略回路図：1V/V ゲイン、シングルエンド入力から差動出力、500kHz、ADS127L01 への複数のフィードバック・フィルタ・インターフェイス

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2017) to Revision D (April 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「*概要*」セクションに「*製品情報*」表を追加 ... 1
- Moved the *Low-Power ADCs Supported by the THS4551* table to the *Device Comparison* section ... 4
- Removed the I_{IB} input bias current (positive current out-of-node) minimum limits in the *Electrical Characteristics: $(V_{S+}) – (V_{S–})$ = 5 V* section ... 7
- Removed the I_{IB} input bias current (positive current out-of-node) minimum limits in the *Electrical Characteristics: $(V_{S+}) – (V_{S–})$ = 3 V* section ... 10

Changes from Revision B (November 2016) to Revision C (July 2017) — **Page**

- *セクション 7.6* の表で「47kΩ、1.3pF」を「150kΩ、7pF」に変更 ... 1

Changes from Revision A (August 2016) to Revision B (November 2016) — **Page**

- Added second row and footnote 2 to *Voltage* parameter of *Absolute Maximum Ratings* table ... 6
- Added package differences and footnote 3 to *ESD Ratings* table ... 6
- Changed footnotes 1 and 2 in *5-V Electrical Characteristics* table ... 7
- Added test conditions to A_{OL} parameter in *5-V Electrical Characteristics* table ... 7
- Changed *Input offset voltage drift* parameter ... 7
- Changed I_{IB} parameter minimum and maximum specifications in last three rows ... 7
- Changed *Input bias current drift* parameter test conditions and specifications ... 7
- Added *Input offset current drift* parameter test conditions, minimum and maximum specifications, and test level value to second row ... 7
- Changed test conditions of *Common-mode input, low* and *Common-mode input, high* parameters ... 7
- Changed test conditions of *Continuous output current* and *Linear output current* parameters ... 7

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- Changed test conditions of *Enable voltage threshold* and *Disable voltage threshold* parameters....7
- Changed specifications of *Power-down quiescent current* parameter 7
- Changed *Common-mode loop supply headroom to negative supply* parameter test conditions....7
- Changed test conditions and maximum specifications of *Common-mode loop supply headroom to positive supply* parameter....7
- Added test conditions to DC Performance, A_{OL} parameter....10
- Changed *Input offset voltage drift* parameter test conditions in first row, added second row....10
- Changed minimum and maximum specifications in last three rows of I_{IB} parameter....10
- Changed *Input bias current drift* parameter test conditions....10
- Added second row to *Input offset current drift* parameter 10
- Changed test conditions of *Common-mode input, low* and *Common-mode input, high* parameters....10
- Changed test conditions of *Continuous output current* and *Linear output current* parameters 10
- Changed test conditions of *Enable voltage threshold* and *Disable voltage threshold* parameters....10
- Changed $I_{Q(PD)}$ parameter specifications....10
- Changed *Common-mode loop supply headroom to negative supply* parameter test conditions....10
- Changed *Common-mode loop supply headroom to positive supply* parameter test conditions and maximum specifications 10
- Changed conditions of 図 7-49 to 図 7-54 19
- Changed *Single-Ended Source to a Differential Gain of a 1-V/V Test Circuit* figure....23
- Changed main *Device Functional Modes* section: changed value of $\overline{PD}$ pin voltage 38
- Changed the minimum value for single-supply operation in the *Operating the Power Shutdown Feature* section....45
- Added SBOS476, SBOC466, SBOC463, SBOC467, SBOS460, SBOC477, SBOC472, SLOC341, SBOC469, SBOC462, SBOC461, SBOC465, SBOC464, SBOC475, SBOC474, SBOC471, SBOC459, SBOC470, SBOC468, and SBOC473 to *Related Documentation* section 63

Changes from Revision * (April 2016) to Revision A (August 2016) **Page**

- 量産用にリリース....1

5 Companion Devices

Low-Power ADCs Supported by the THS4551

PART NUMBER	ADC TYPE	RESOLUTION, SPEED
ADS127L01	Delta sigma	24 bits, 0.512 MSPS
ADS8881	SAR	18 bits, 1 MSPS
ADS9110	SAR	18 bits, 2 MSPS
ADC3241	Pipeline	14 bits, 25 MSPS

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6 Pin Configuration and Functions

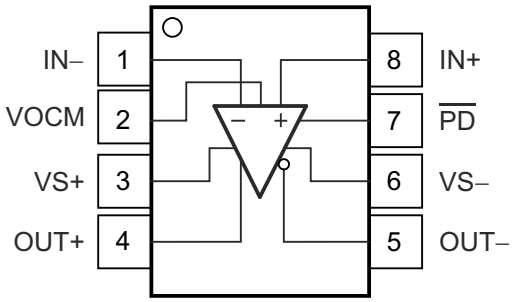

図 6-1. DGK Package 8-Pin VSSOP Top View

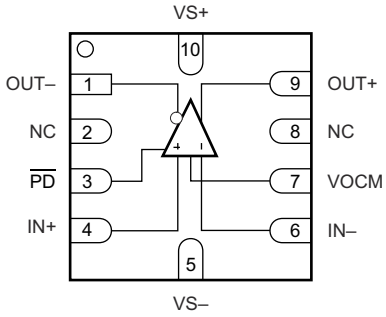

図 6-2. RUN Package 10-Pin WQFN Top View

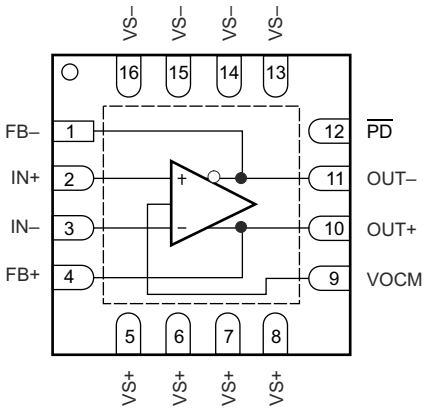

図 6-3. RGT Package 16-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	RGT(1)	RUN	DGK		
FB–	1	—	—	O	Inverting (negative) output feedback
FB+	4	—	—	O	Noninverting (positive) output feedback
IN–	3	6	1	I	Inverting (negative) amplifier input
IN+	2	4	8	I	Noninverting (positive) amplifier input
NC	—	2, 8	—	—	No internal connection
OUT–	11	1	5	O	Inverting (negative) amplifier output
OUT+	10	9	4	O	Noninverting (positive) amplifier output
$\overline{PD}$	12	3	7	I	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VOCM	9	7	2	I	Common-mode voltage input
VS–	13-16	5	6	I	Negative power-supply input
VS+	5, 6, 7, 8	10	3	I	Positive power-supply input

(1) Solder the exposed thermal pad (RGT package) to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but it must be connected to a power or ground plane and not floated.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, (V_{S+}) – ($V_{S–}$)		5.5	V
	Supply turn-on/off maximum dV/dT(2)		±1	V/µs
	Input/output voltage range	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
	Differential input voltage		±1	
Current	Continuous input current		±10	mA
	Continuous output current(3)		±20	
	Continuous power dissipation	See the *セクション 7.4* and *セクション 11.1* sections		
Temperature	Maximum junction		150	°C
	Operating free-air, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Staying below this ± supply turn-on edge rate ensures that the edge-triggered ESD absorption device across the supply pins remains off.
(3) Long-term continuous current for electro-migration limits.

7.2 ESD Ratings

			VALUE	UNIT
A. THS4551 in DGK, RUN Pacakges				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	
B. THS4551 in RGT Package				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (3)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) ESD limit of ±1000 V for any pin to thermal pad. Pin-to-pin HBM ESD specifications are rated at ±2500 V.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply positive voltage	2.7	5	5.4	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS4551 RGT(2) (VQFN) 16 PINS	THS4551 RUN (WQFN) 10 PINS	THS4551 DGK (VSSOP) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	54	142	185	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	72	78	76	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	28	97	106	°C/W

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THERMAL METRIC[1]		THS4551			UNIT
		RGT[2] (VQFN)	RUN (WQFN)	DGK (VSSOP)	
		16 PINS	10 PINS	8 PINS	
ψ_{JT}	Junction-to-top characterization parameter	3.2	9.7	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28	97	105	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal impedance for RGT reported with backside thermal pad soldered to heat spreading plane.

7.5 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[1]
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, peaking (< 1.0 dB)		150		MHz	C
		V_{OUT} = 20 mV_{PP}, G = 2		75			C
		V_{OUT} = 20 mV_{PP}, G = 10		15			C
GBP	Gain-bandwidth product	V_{OUT} = 20 mV_{PP}, G = 100		135		MHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		37		MHz	C
	Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 1		15		MHz	C
SR	Slew rate[2]	V_{OUT} = 4 V_{PP}, full-power bandwidth (FPBW), R_L = 1 kΩ		220		V/µs	C
t_R, t_F	Rise and fall time	V_{OUT} = 0.5-V step, G = 1, input t_R = 2 ns		6		ns	C
t_{SETTLE}	Settling time	To 0.1%, V_{OUT} = 0.5-V step, input t_R = 2 ns, G = 1		30		ns	C
		To 0.01%,V_{OUT} = 0.5-V step, input t_R = 2 ns, G = 1		50			C
	Overshoot and undershoot	V_{OUT} = 0.5-V step G = 1, input t_R = 2 ns		8%			C
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}, G = 1, R_L = 1 kΩ		–128		dBc	C
		f = 100 kHz, V_{OUT} = 8 V_{PP}, G = 1, R_L = 1 kΩ		–124			C
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}, G = 1, R_L = 1 kΩ		–139		dBc	C
		f = 100 kHz, V_{OUT} = 8 V_{PP}, G = 1, R_L = 1 kΩ		–131			C
	Input voltage noise	f > 500 Hz, 1/f < 150 Hz		3.3		nV/√Hz	C
	Input current noise	f > 20 kHz, 1/f <10 kHz		0.5		pA/√Hz	C
	Overdrive recovery time	G = 2, 2X output overdrive, dc coupled		50		ns	C
	Closed-loop output impedance	f = 100 kHz (differential), G = 1		0.02		Ω	C
DC PERFORMANCE[5]							
A_{OL}	Open-loop voltage gain	±3-V differential-to-differential, 1-kΩ load	105	125		dB	A
	Internal feedback trace resistance	T_A = 25°C, RGT only (pins 11-1, 10-4)	3.0	3.5	4.7	Ω	A
		T_A = –40°C to +125°C, temperature drift		10		mΩ/°C	B
	Internal feedback trace resistance mismatch	T_A = 25°C, RGT only (pins 11-1, 10-4)[6]	–1	0.05	1	Ω	A
		T_A = –40°C to +125°C, temperature drift		50		µΩ/°C	B
V_{IO}	Input-referred offset voltage	T_A = 25°C	–175	±50	175	µV	A
		T_A = 0°C to +70°C	–225		265		B
		T_A = –40°C to +85°C	–295		295		B
		T_A = –40°C to +125°C	–295		375		B
	Input offset voltage drift[3]	T_A = –40°C to +125°C (DGK package)	–2.0	±0.45	2.0	µV/°C	B
		T_A = –40°C to +125°C (RUN package)	–1.7	±0.4	1.7		B
		T_A = –40°C to +125°C (RGT package)	–1.8	±0.4	1.8		B

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7.5 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
I_{IB}	Input bias current (positive current out of node)	$T_A = 25°C$			1.0	1.5	μA	A
		$T_A = 0°C$ to $+70°C$				1.73		B
		$T_A = –40°C$ to $+85°C$				1.80		B
		$T_A = –40°C$ to $+125°C$				2.0		B
	Input bias current drift(3)	$T_A = –40°C$ to $+125°C$		2	3.3	5.0	nA/°C	B
I_{OS}	Input offset current	$T_A = 25°C$		–50	±10	50	nA	A
		$T_A = 0°C$ to $+70°C$		–57		63		B
		$T_A = –40°C$ to $+85°C$		–68		67		B
		$T_A = –40°C$ to $+125°C$		–68		78		B
	Input offset current drift(3)	$T_A = –40°C$ to $+125°C$ (DGK package)		–280	±70	280	pA/°C	B
		$T_A = –40°C$ to $+125°C$ (RGT and RUN package)		–120	±20	120		B
INPUT								
	Common-mode input, low	> 90-dB CMRR at input range limits	$T_A = 25°C$		$(V_{S–}) – 0.2$	$(V_{S–}) – 0.1$	V	A
			$T_A = –40°C$ to $+125°C$		$(V_{S–}) – 0.1$	$V_{S–}$		B
	Common-mode input, high	> 90-dB CMRR at input range limits	$T_A = 25°C$	$(V_{S+}) – 1.2$	$(V_{S+}) – 1.1$		V	A
			$T_A = –40°C$ to $+125°C$	$(V_{S+}) – 1.3$	$(V_{S+}) – 1.2$			B
CMRR	Common-mode rejection ratio	Input pins at $[(V_{S+}) – (V_{S–})] / 2$		93	110		dB	A
	Input impedance differential mode	Input pins at $[(V_{S+}) – (V_{S–})] / 2$			100 || 1.2		kΩ || pF	C
OUTPUT								
	Output voltage, low	$T_A = 25°C$			$(V_{S–}) + 0.2$	$(V_{S–}) + 0.23$	V	A
		$T_A = –40°C$ to $+125°C$			$(V_{S–}) + 0.2$	$(V_{S–}) + 0.22$		B
	Output voltage, high	$T_A = 25°C$		$(V_{S+}) – 0.23$	$(V_{S+}) – 0.2$		V	A
		$T_A = –40°C$ to $+125°C$		$(V_{S+}) – 0.22$	$(V_{S+}) – 0.2$			B
	Continuous output current	$T_A = 25°C$, ±2.5 V, $R_L = 40$ Ω, V_{OCM} offset < ±20 mV		±60	±65		mA	A
		$T_A = –40°C$ to $+125°C$, ±2.1 V, $R_L = 40$ Ω, V_{OCM} offset < ±20 mV		±50				B
	Linear output current	$T_A = 25°C$, ±2.1 V, $R_L = 50$ Ω, $A_{OL} > 80$ dB		±40	±45		mA	A
		$T_A = –40°C$ to $+125°C$, ±1.6 V, $R_L = 50$ Ω, $A_{OL} > 80$ dB		±30				B
POWER SUPPLY								
	Specified operating voltage			2.7	5	5.4	V	B
I_Q	Quiescent operating current	$T_A \approx 25°C$(7), $V_{S+} = 5$ V		1.28	1.37	1.44	mA	A
		$T_A = –40°C$ to $+125°C$, $V_{S+} = 5$ V		0.97		1.92		B
dI_Q/dT	Quiescent current temperature coefficient	$V_{S+} = 5$ V		2.4	3.9	5.4	μA/°C	B
±PSRR	Power-supply rejection ratio	Either supply pin to differential V_{OUT}		93	110		dB	A
POWER-DOWN								
	Enable voltage threshold	Specified on above $(V_{S–}) + 1.15$ V		$(V_{S–}) + 1.15$			V	A
	Disable voltage threshold	Specified off below $(V_{S–}) + 0.55$ V				$(V_{S–}) + 0.55$	V	A
	Disable pin bias current	$\overline{PD} = V_{S–} \rightarrow V_{S+}$		–100	±10	100	nA	B
	Power-down quiescent current			–2	1	5	μA	A
t_{ON}	Turn-on time delay	Time from $\overline{PD}$ = low to V_{OUT} = 90% of final value			700		ns	C
t_{OFF}	Turn-off time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of final value			100		ns	C

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7.5 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL(4) (See 図 8-5)									
SSBW	Small-signal bandwidth		V_{OCM} = 100 mV_{PP} at the control pin			40		MHz	C
LSBW	Large-signal bandwidth		V_{OCM} = 1 V_{PP} at the control pin			8		MHz	C
SR	Slew rate(2)		From 1-V_{PP} LSBW			18		V/µs	C
	Output common-mode noise (≥ 2 kHz)		VOCM pin driven from low impedance			15		nV/√Hz	C
	Gain		VOCM control pin input to output average voltage (see 図 8-5)		0.997	0.999	1.001	V/V	A
	Input bias current				–100	±10	100	nA	A
	DC output balance (differential mode to common-mode output)		V_{OUT} = ±1 V			85		dB	C
	Output balance	SSBW	V_{OUT} = 100 mV_{PP} (output balance drops –3 dB from the 85-dB dc level)			300		kHz	C
		LSBW	V_{OUT} = 2 V_{PP} (output balance drops –3 dB from the 85-dB dc level)			300			C
	Input impedance (VOCM pin input)					150 || 7		kΩ || pF	C
	Default voltage offset from $[(V_{S+}) – (V_{S–})] / 2$		VOCM pin open		–12	±2	12	mV	A
			VOCM pin open, T_A = –40°C to +125°C		15	35	55	µA/°C	B
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL (continued)									
CM V_{OS}	Common-mode offset voltage		VOCM pin driven to $[(V_{S+}) – (V_{S–})] / 2$	T_A = 25°C	–5.0	±1	5.0	mV	A
				T_A = 0°C to +70°C	–5.25		5.5		B
				T_A = –40°C to +85°C	–5.7		5.6		B
				T_A = –40°C to +125°C	–5.7		6.0		B
	Common-mode offset voltage drift(3)		T_A = –40°C to +125°C		–10	±2	10	µV/°C	B
	Common-mode loop supply headroom to negative supply		< ±15-mV shift from midsupply CM V_{OS}	T_A = 25°C			0.55	V	A
				T_A = 0°C to +70°C			0.6		B
				T_A = –40°C to +85°C			0.65		B
				T_A = –40°C to +125°C			0.7		B
	Common-mode loop supply headroom to positive supply		< ±15-mV shift from midsupply CM V_{OS}	T_A = 25°C			1.2	V	A
				T_A = 0°C to 70°C			1.25		B
				T_A = –40°C to +85°C			1.3		B
				T_A = –40°C to +125°C			1.3		B

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at $T_A \approx 25°C$. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the sinusoidal large-signal bandwidth as: $(V_P / \sqrt{2}) \times 2\pi \times f_{–3dB}$.
(3) Input offset voltage drift, input bias current drift, and input offset current drift are the mean ±1-sigma values calculated by taking measurements at the maximum-range ambient temperature end points, computing the difference, and dividing by the temperature range. Maximum drift specifications are set by mean ±4 σ on the device distributions tested over a –40℃ to +125℃ ambient temperature range. Drift is not specified by final ATE testing or QA sample test.
(4) Specifications are from the input VOCM pin to the differential output average voltage.
(5) Currents out of pin are treated as a positive polarity (with the exception of the power-supply pins).
(6) Trace mismatch measurement is dominated by the variation in contactor resistance. Internal mismatch is less than 0.1 Ω.
(7) T_A = 25°C and $I_{CC} \approx 1.37$ mA. The test limit is expanded for the ATE ambient range of 22°C to 32°C with a 4-µA/°C I_{CC} temperature coefficient considered; see 図 11-1.

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7.6 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, peaking (< 1.0 dB)		150		MHz	C
		V_{OUT} = 20 mV_{PP}, G = 2		80			C
		V_{OUT} = 20 mV_{PP}, G = 10		14			C
GPB	Gain-bandwidth product	V_{OUT} = 20 mV_{PP}, G = 100		130		MHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 1		45		MHz	C
	Bandwidth for 0.1-dB flatness	V_{OUT} = 1 V_{PP}, G = 1		14		MHz	C
SR	Slew rate(2)	V_{OUT} = 1 V_{PP}, FPBW, G = 1		110		V/µs	C
t_R, t_F	Rise and fall time	V_{OUT} = 0.5-V step, G = 1, input t_R = 4 ns		7.0		ns	C
t_{SETTLE}	Settling time	To 0.1%, V_{OUT} = 0.5-V step, input t_R = 4 ns, G = 1		35		ns	C
		To 0.01%, V_{OUT} = 0.5-V step, input t_R = 4 ns, G = 1		55			C
	Overshoot and undershoot	V_{OUT} = 0.5-V step, G = 1, input t_R = 4 ns		7%			C
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}, G = 1, R_L = 1 kΩ		–128		dBc	C
		f = 100 kHz, V_{OUT} = 4 V_{PP}, G = 1, R_L = 1 kΩ		–127			C
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}, G = 1, R_L = 1 kΩ		–139		dBc	C
		f = 100 kHz, V_{OUT} = 4 V_{PP}, G = 1, R_L = 1 kΩ		–125			C
	Input voltage noise	f > 500 Hz, 1/f < 150 Hz		3.4		nV/√Hz	C
	Input current noise	f > 20 kHz, 1/f < 10 kHz		0.5		pA/√Hz	C
	Overdrive recovery time	G = 2, 2X output overdrive, dc coupled		100		ns	C
	Closed-loop output impedance	f = 100 kHz (differential), G = 1		0.02		Ω	C
DC PERFORMANCE(5)							
A_{OL}	Open-loop voltage gain	±2-V differential to 1-kΩ differential load	100	120		dB	A
	Internal feedback trace resistance	T_A = 25°C, RGT only (pins 11-1, 10-4)	3.0	3.45	4.7	Ω	A
		T_A = –40°C to +125°C, temperature drift		50		mΩ/°C	B
	Internal feedback trace resistance mismatch	T_A = 25°C, RGT only (pins 11-1, 10-4)(6)	–1	0.05	1	Ω	A
		T_A = –40°C to +125°C, temperature drift		50		µΩ/°C	B
V_{IO}	Input-referred offset voltage	T_A = 25°C	–175	±40	175	µV	A
		T_A = 0°C to +70°C	–225		265		B
		T_A = –40°C to +85°C	–295		295		B
		T_A = –40°C to +125°C	–295		375		B
	Input offset voltage drift(3)	T_A = –40°C to +125°C (DGK package)	–2.0	±0.45	2.0	µV/°C	B
		T_A = –40°C to +125°C (RUN package)	–1.7	±0.4	1.7		B
		T_A = –40°C to +125°C (RGT package)	–1.8	±0.4	1.8		B
I_{IB}	Input bias current (positive current out of node)	T_A = 25°C		1.0	1.5	µA	A
		T_A = 0°C to +70°C			1.73		B
		T_A = –40°C to +85°C			1.80		B
		T_A = –40°C to +125°C			2.0		B
	Input bias current drift(3)	T_A = –40°C to +125°C	2	3.3	5.5	nA/°C	B
I_{OS}	Input offset current	T_A = 25°C	–50	±10	50	nA	A
		T_A = 0°C to +70°C	–57		63		B
		T_A = –40°C to +85°C	–68		67		B
		T_A = –40°C to +125°C	–68		78		B
	Input offset current drift(3)	T_A = –40°C to +125°C (DGK package)	–280	±70	280	pA/°C	B
		T_A = –40°C to +125°C (RGT and RUN package)	–120	±20	120		B

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7.6 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
INPUT								
	Common-mode input, low	> 87-dB CMRR at input range limits	$T_A = 25°C$		$(V_{S–}) – 0.2$	$(V_{S–}) – 0.1$	V	A
			$T_A = –40°C$ to +125°C		$(V_{S–}) – 0.1$	$V_{S–}$		B
	Common-mode input, high	> 87-dB CMRR at input range limits	$T_A = 25°C$	$(V_{S+}) – 1.2$	$(V_{S+}) –1.1$		V	A
			$T_A = –40°C$ to +125°C	$(V_{S+}) – 1.3$	$(V_{S+}) –1.2$			B
CMRR	Common-mode rejection ratio	Input pins at $[(V_{S+}) – (V_{S–})] / 2$		90	110		dB	A
	Input impedance differential mode	Input pins at $[(V_{S+}) – (V_{S–})] / 2$			100 || 1.2		kΩ || pF	C
OUTPUT								
V_{OL}	Output voltage, low	$T_A = 25°C$			$(V_{S–}) + 0.2$	$(V_{S–}) + 0.21$	V	A
		$T_A = –40°C$ to +125°C			$(V_{S–}) + 0.2$	$(V_{S–}) + 0.22$		B
V_{OH}	Output voltage, high	$T_A = 25°C$		$(V_{S+}) – 0.21$	$(V_{S+}) – 0.2$		V	A
		$T_A = –40°C$ to +125°C		$(V_{S+}) – 0.22$	$(V_{S+}) – 0.2$			B
	Continuous output current	±1.5 V, $R_L = 40$ Ω, V_{OCM} offset < ±20 mV	$T_A = 25°C$	±35	±40		mA	A
		±1.3 V, $R_L = 40$ Ω, V_{OCM} offset < ±20 mV	$T_A = –40°C$ to +125°C	±30				B
	Linear output current	±1.5 V, $R_L = 50$ Ω, $A_{OL} > 80$ dB	$T_A = 25°C$	±28	±35		mA	A
		±1.1 V, $R_L = 50$ Ω, $A_{OL} > 80$ dB	$T_A = –40°C$ to +125°C	±20				B
POWER SUPPLY								
	Specified operating voltage			2.7	3	5.4	V	B
I_Q	Quiescent operating current	$T_A \approx 25°C$(7), $V_{S+} = 3$ V		1.24	1.31	1.40	mA	A
		$T_A = –40°C$ to +125°C, $V_{S+} = 3$ V		0.96		1.84		B
dI_Q/dT	Quiescent current temperature coefficient	$V_{S+} = 3$ V		2.0	3.4	5.0	µA/°C	B
±PSRR	Power-supply rejection ratio	Either supply pin to differential V_{OUT}		90	105		dB	A
POWER-DOWN								
	Enable voltage threshold	Specified on above $(V_{S–}) + 1.15$ V		$(V_{S–}) + 1.15$			V	A
	Disable voltage threshold	Specified off below $(V_{S–}) + 0.55$ V				$(V_{S–}) + 0.55$	V	A
	Disable pin bias current	$\overline{PD} = V_{S–} \rightarrow V_{S+}$		–100	±10	100	nA	B
$I_{Q(PD)}$	Power-down quiescent current			–2	1	5	µA	A
t_{ON}	Turn-on time delay	Time from $\overline{PD}$ = low to V_{OUT} = 90% of final value			750		ns	C
t_{OFF}	Turn-off time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of final value			150		ns	C
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL(4) (See 図 8-5)								
SSBW	Small-signal bandwidth	$V_{OCM} = 100$ mV_{PP} at the control pin			40		MHz	C
LSBW	Large-signal bandwidth	$V_{OCM} = 1$ V_{PP} at the control pin			8		MHz	C
SR	Slew rate(2)	From 1-V_{PP} LSBW			12		V/µs	C
	Output common-mode noise	VOCM pin driven from low impedance, f ≥ 2 kHz			15		nV/√Hz	
	Gain	VOCM control pin input to output average voltage (see 図 8-5)		0.997	0.999	1.001	V/V	A
	DC output balance (differential mode to common-mode output)	$V_{OUT} = ±1$ V			85	dB		C

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7.6 Electrical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
	Output balance	SSBW	V_{OUT} = 100 mV_{PP} (output balance drops –3 dB from the 85-dB dc level)			300		kHz	C
		LSBW	V_{OUT} = 1 V_{PP} (output balance drops –3 dB from the 85-dB dc level)			300			C
	Input bias current				–100	±10	100	nA	A
	Input impedance					150 || 7		kΩ || pF	C
	Default voltage offset from $[(V_{S+}) – (V_{S–})] / 2$		VOCM pin open		–12	±2	12	mV	A
			VOCM pin open, T_A = –40°C to +125°C		15	35	55	µA/°C	B
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL (continued)									
CM V_{OS}	Common-mode offset voltage		V_{OCM} input driven to $[(V_{S+}) – (V_{S–})] / 2$	T_A = 25°C	–5.0	±1	5.0	mV	A
				T_A = 0°C to +70°C	–5.25		5.5		B
				T_A = –40°C to +85°C	–5.7		5.6		B
				T_A = –40°C to +125°C	–5.7		6.0		B
	Common-mode offset voltage drift(3)		V_{OCM} input driven to $[(V_{S+}) – (V_{S–})] / 2$		–10	±2	10	µV/°C	B
	Common-mode loop supply headroom to negative supply		< ±15-mV shift from midsupply CM V_{OS}	T_A = 25°C			0.55	V	A
				T_A = 0°C to +70°C			0.6		B
				T_A = –40°C to +85°C			0.65		B
				T_A = –40°C to +125°C			0.7		B
	Common-mode loop supply headroom to positive supply		< ±15-mV shift from midsupply CM V_{OS}	T_A = 25°C			1.2	V	A
				T_A = 0°C to +70°C			1.25		B
				T_A = –40°C to +85°C			1.3		B
				T_A = –40°C to +125°C			1.3		B

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at $T_A \approx 25°C$. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_{PP} / \sqrt{2}) \times 2\pi \times f_{-3dB}$.
(3) Input offset voltage drift, input bias current drift, and input offset current drift are the mean ±1-sigma values calculated by taking measurements at the maximum-range ambient temperature end points, computing the difference, and dividing by the temperature range. Maximum drift specifications are set by mean ±4 σ on the device distributions tested over a –40℃ to +125℃ ambient temperature range. Drift is not specified by final ATE testing or QA sample test.
(4) Specifications are from input VOCM pin to differential output average voltage.
(5) Currents out of pin are treated as a positive polarity (with exception of the power-supply pin currents).
(6) Trace mismatch measurement is dominated by the variation in contactor resistance. Internal mismatch is less than 0.1 Ω.
(7) T_A = 25°C and $I_{CC} \approx 1.31$ mA. The test limit is expanded for the ATE ambient range of 22°C to 32°C with a 4-µA/°C I_{CC} temperature coefficient considered; see 図 11-1.

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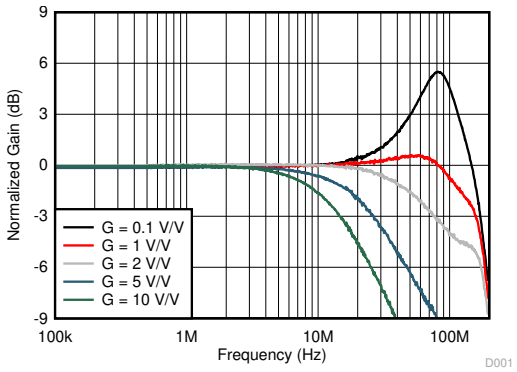
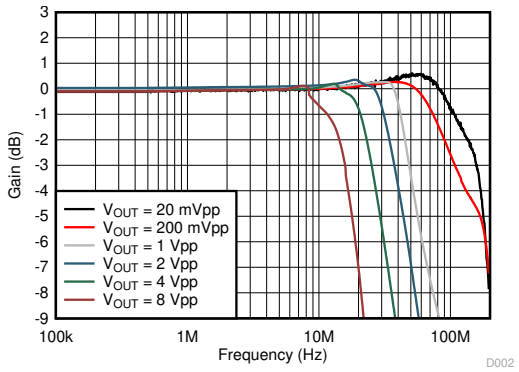
7.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



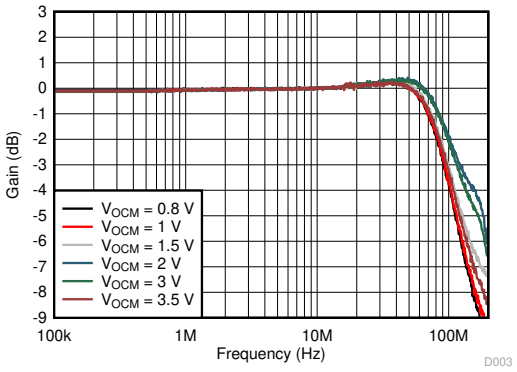
V_{OUT} = 20 mV_{PP}, see 図 8-1 and 表 9-1 for resistor values

図 7-1. Small-Signal Frequency Response vs Gain



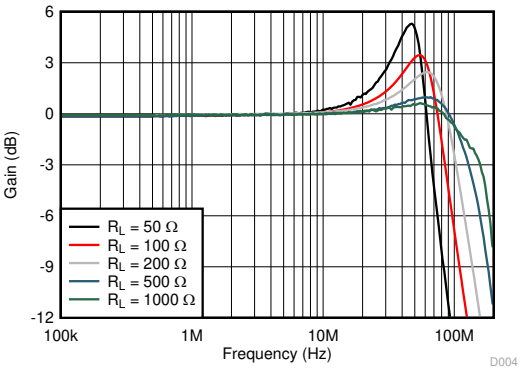
See 図 8-1

図 7-2. Frequency Response vs V_{OUT}



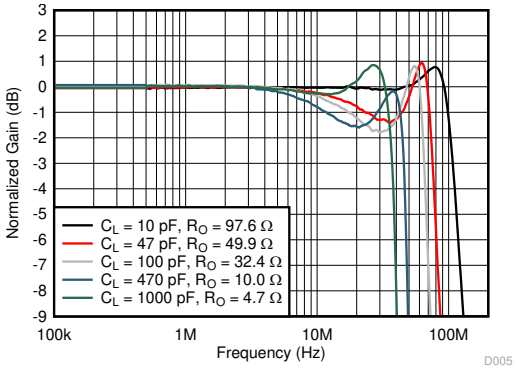
V_{OUT} = 20 mV_{PP} , see 図 8-1 with V_{OCM} adjusted

図 7-3. Small-Signal Frequency Response vs V_{OCM}



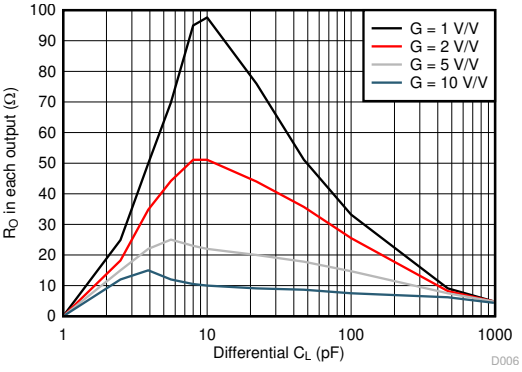
V_{OUT} = 20 mV_{PP}, see 図 8-1 with load resistance (R_L) adjusted

図 7-4. Small-Signal Frequency Response vs R_L



V_{OUT} = 20 mV_{PP} at load, G = 1, two series R_O added at output before capacitive load (C_L)

図 7-5. Small-Signal Frequency Response vs C_L



Output resistance (R_O) is two series output resistors to a differential C_L in parallel with a 1-kΩ load resistance

図 7-6. Recommended R_O vs C_L

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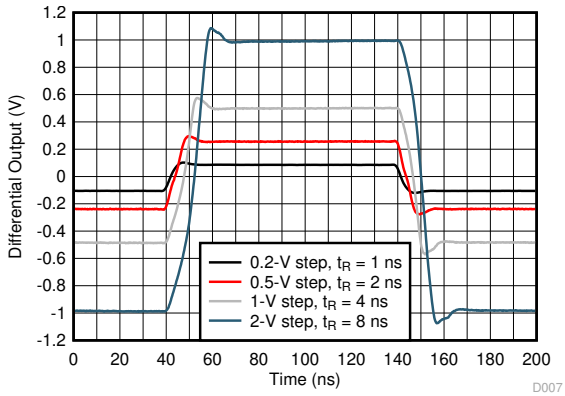
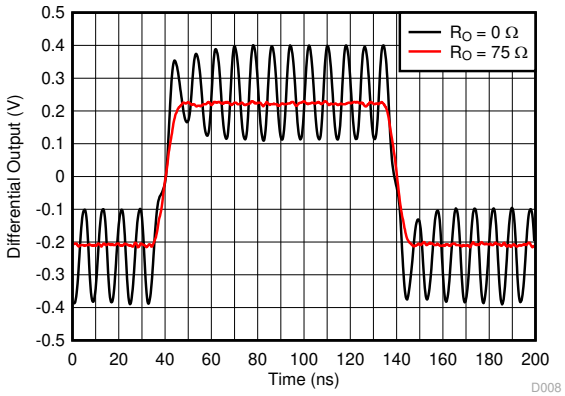
7.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



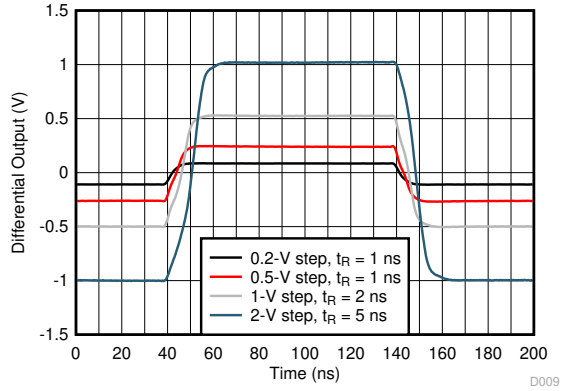
G = 1 V/V, 5-MHz input, single-ended to differential output

図 7-7. Small- and Large-Signal Step Response



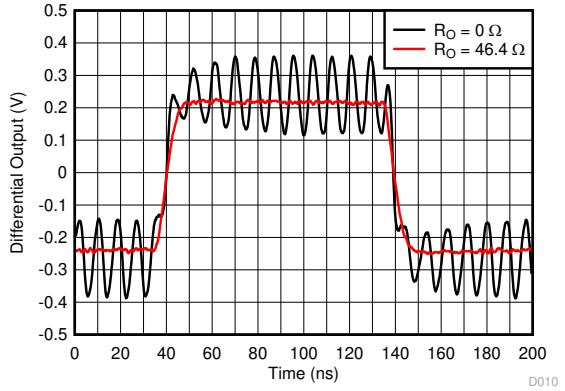
G = 1 V/V, V_{OUT} = 500-mV step into 22-pF C_L, see 図 8-4

図 7-8. Step Response Into Capacitive Load



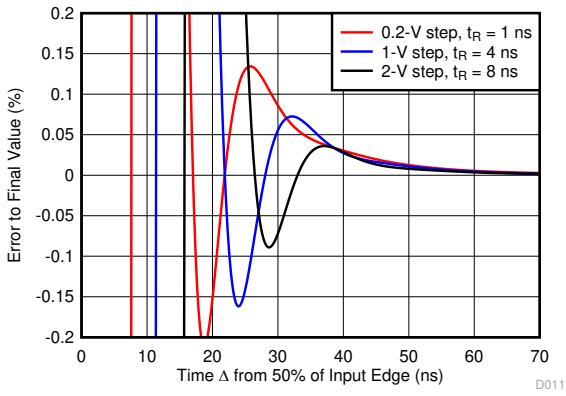
G = 2 V/V, 5-MHz input, single-ended input to differential output

図 7-9. Small- and Large-Signal Step Response



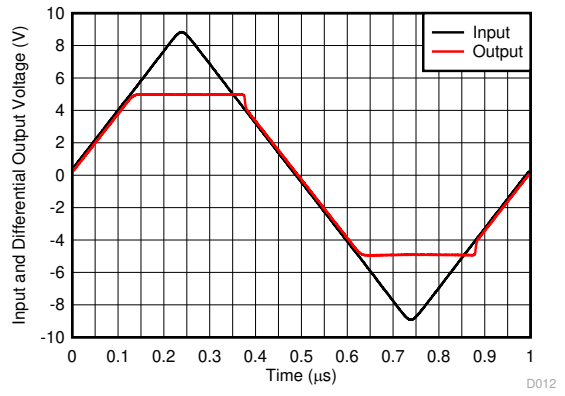
G = 2 V/V, V_{OUT} = 500-mV step into 22-pF C_L, see 図 8-4

図 7-10. Step Response Into Capacitive Load



Simulated with G = 1 V/V

図 7-11. Small- and Large-Signal Step Settling Time



Single-ended to differential gain of 2, 2X input overdrive

図 7-12. Overdrive Recovery Performance

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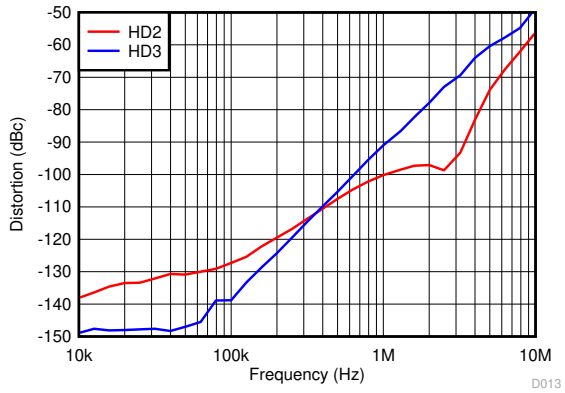
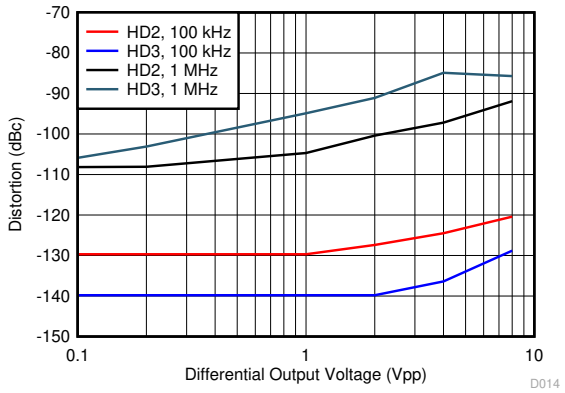
7.7 Typical Characteristics: (V_{S+}) – (V_{S-}) = 5 V (continued)

at T_A ≈ 25°C, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



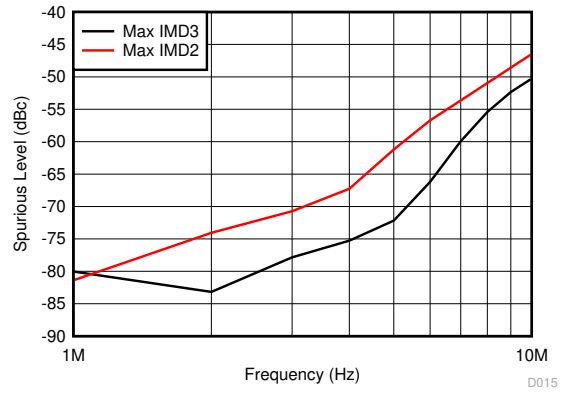
G = 1 V/V, V_{OUT} = 2 V_{PP}

図 7-13. Harmonic Distortion vs Frequency



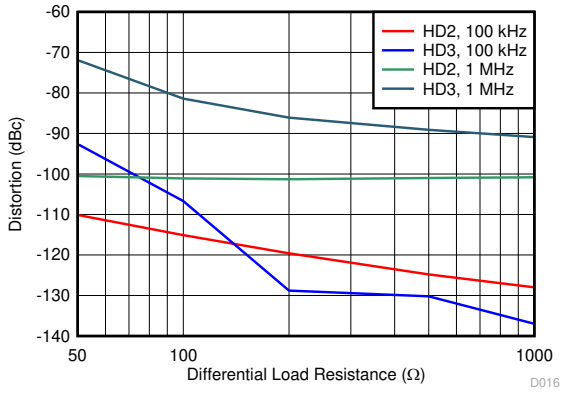
G = 1 V/V

図 7-14. Harmonic Distortion vs Output Swing



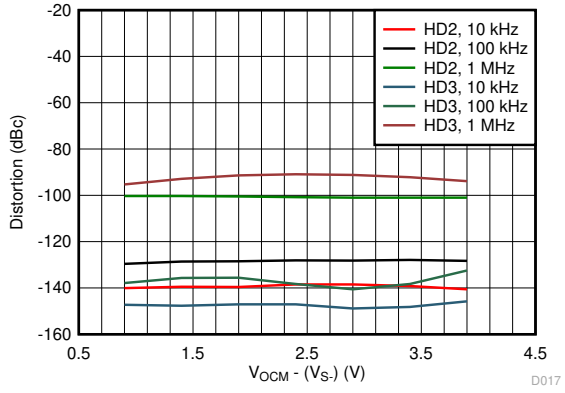
G = 1 V/V, V_{OUT} = 1 V_{PP} each tone

図 7-15. Intermodulation Distortion (IMD2 and IMD3) vs Frequency



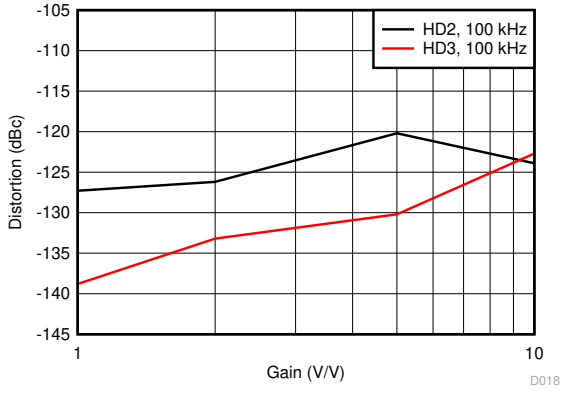
G = 1 V/V, V_{OUT} = 2 V_{PP}, with R_L adjusted

図 7-16. Harmonic Distortion vs R_L



G = 1 V/V, V_{OUT} = 2 V_{PP}, with V_{OCM} adjusted

図 7-17. Harmonic Distortion vs V_{OCM}



V_{OUT} = 2 V_{PP}, see 表 9-1 for gain setting

図 7-18. Harmonic Distortion vs Gain

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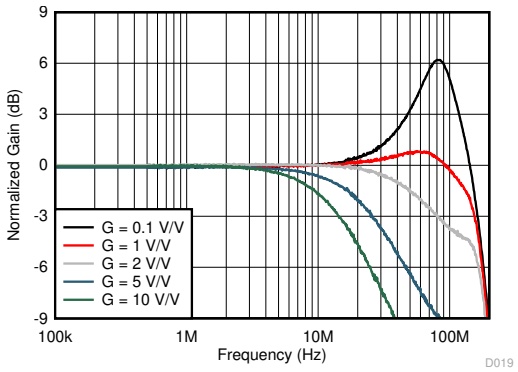
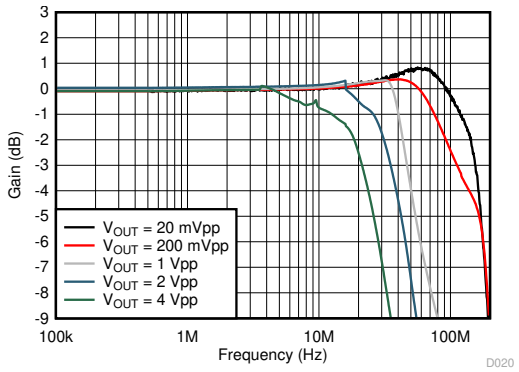
7.8 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



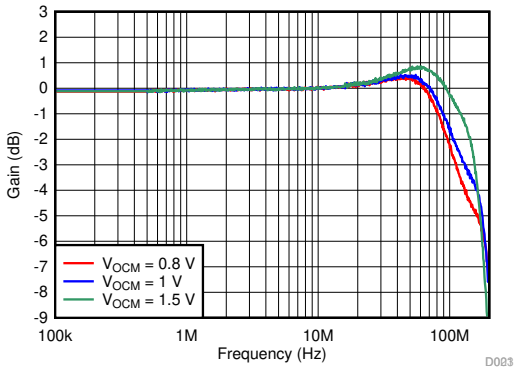
V_{OUT} = 20 mV_{PP}, see 図 8-1 and 表 9-1 for resistor values

図 7-19. Small-Signal Frequency Response vs Gain



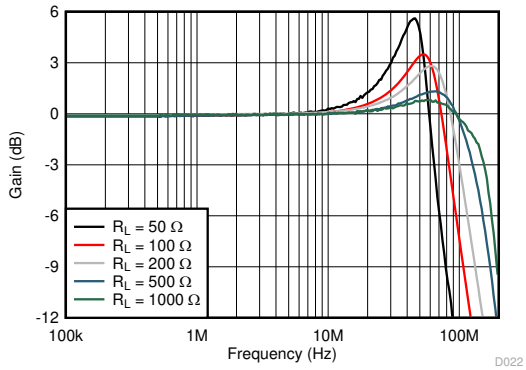
See 図 8-1

図 7-20. Frequency Response vs V_{OUT}



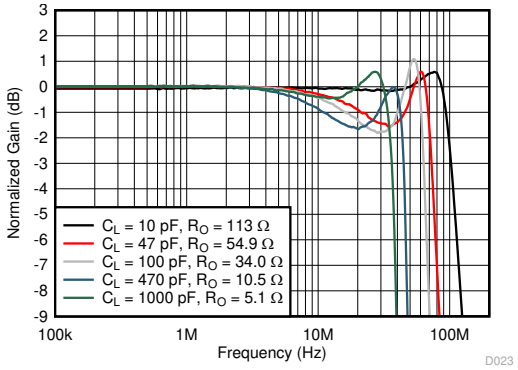
V_{OUT} = 20 mV_{PP}, see 図 8-1 with V_{OCM} adjusted

図 7-21. Small-Signal Frequency Response vs V_{OCM}



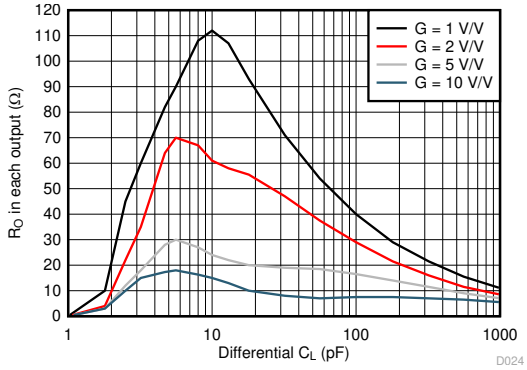
V_{OUT} = 20 mV_{PP}, see 図 8-1 with R_L adjusted

図 7-22. Small-Signal Frequency Response vs R_L



V_{OUT} = 20 mV_{PP}, G = 1 V/V, two series R_O added at output before C_L

図 7-23. Small-Signal Frequency Response vs C_L



Two R_O at output to differential C_L in parallel with a 1-kΩ load resistance

図 7-24. Recommended R_O vs C_L

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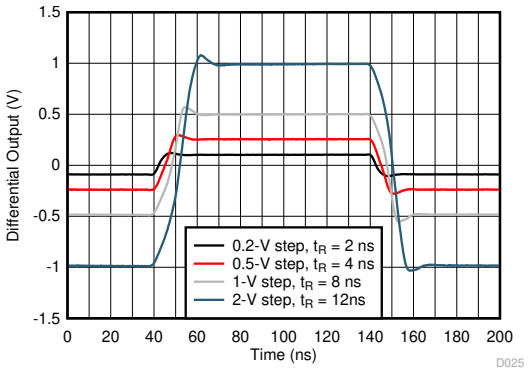
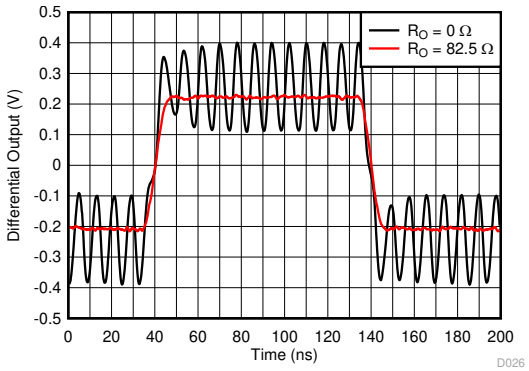
7.8 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 3$ V (continued)

at $T_A \approx 25°C$, VOCM pin = open, $R_F = 1$ kΩ, $R_L = 1$ kΩ, $V_{OUT} = 2$ V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



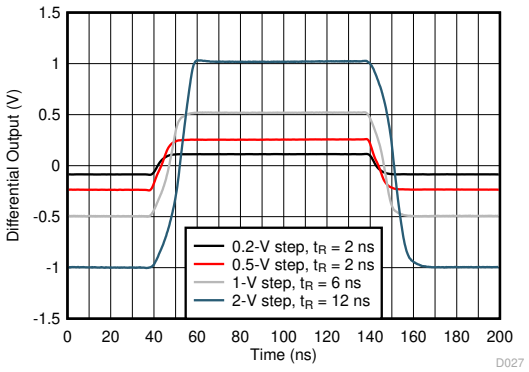
G = 1 V/V, 5-MHz input, single-ended input to differential output

図 7-25. Small- and Large-Signal Step Response



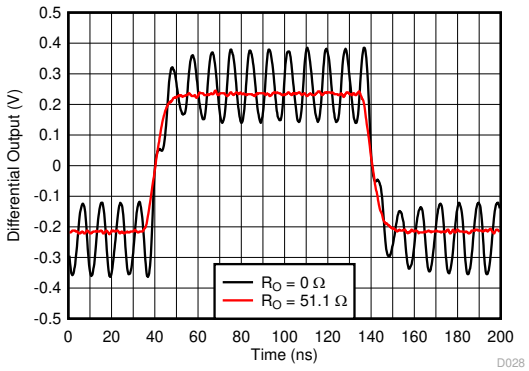
G = 1 V/V, V_{OUT} = 500-mV step into 22-pF C_L, see 図 8-4

図 7-26. Step Response Into Capacitive Load



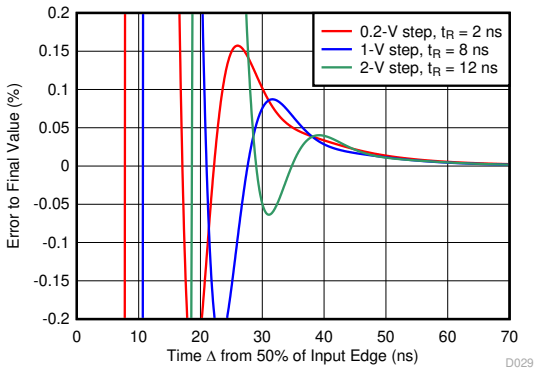
G = 2 V/V, 5-MHz input, single-ended input to differential output.

図 7-27. Small- and Large-Signal Step Response



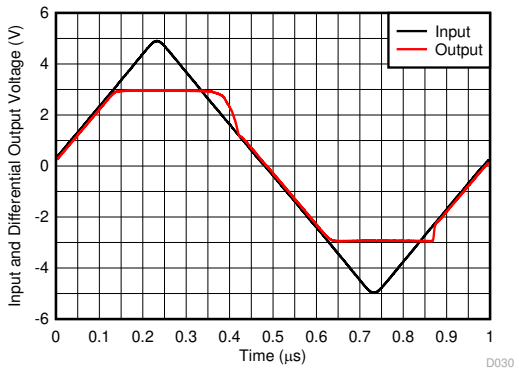
G = 2 V/V, V_{OUT} = 500-mV step into 22-pF C_L, see 図 8-4

図 7-28. Step Response Into Capacitive Load



Simulated with G = 1 V/V

図 7-29. Small- and Large-Signal Step Settling Time



Single-ended to differential gain of 2, 2X input overdrive

図 7-30. Overdrive Recovery Performance

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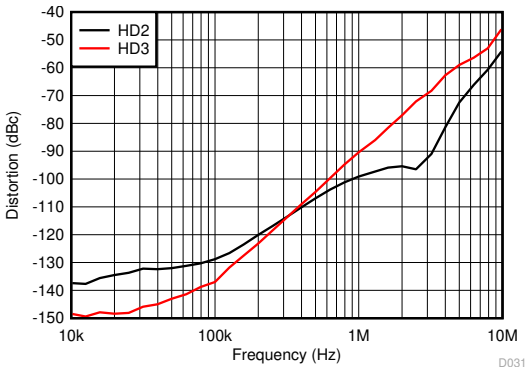
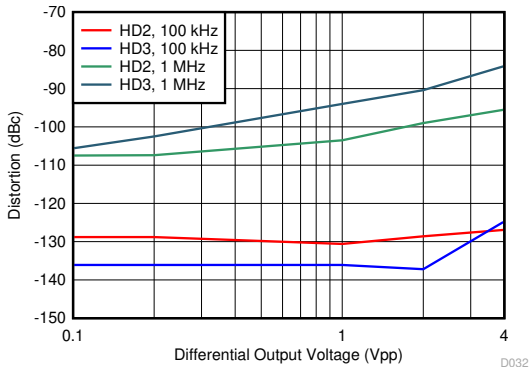
7.8 Typical Characteristics: $(V_{S+}) – (V_{S–})$ = 3 V (continued)

at T_A ≈ 25°C, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



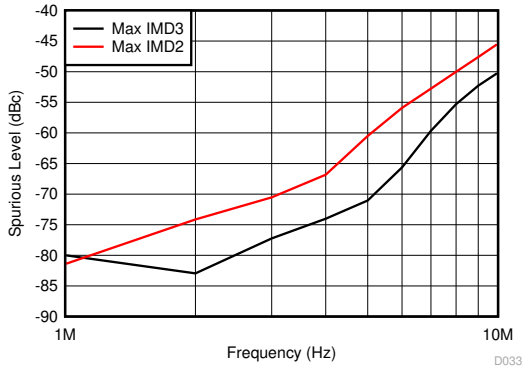
G = 1 V/V, V_{OUT} = 2 V_{PP}

図 7-31. Harmonic Distortion vs Frequency



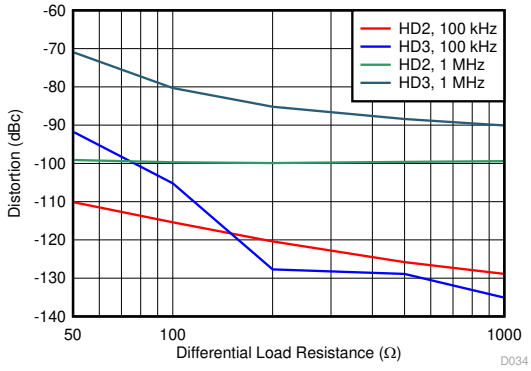
G = 1 V/V

図 7-32. Harmonic Distortion vs Output Swing



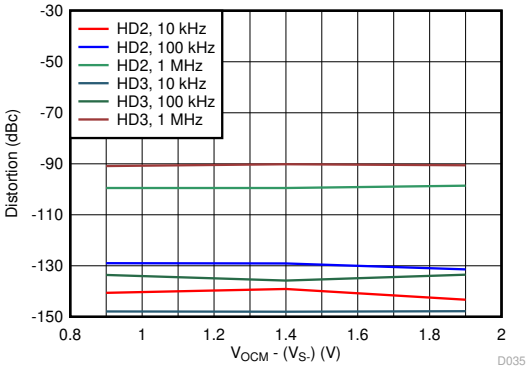
G = 1 V/V, 1 V_{PP} each tone

図 7-33. IMD2 and IMD3 vs Frequency



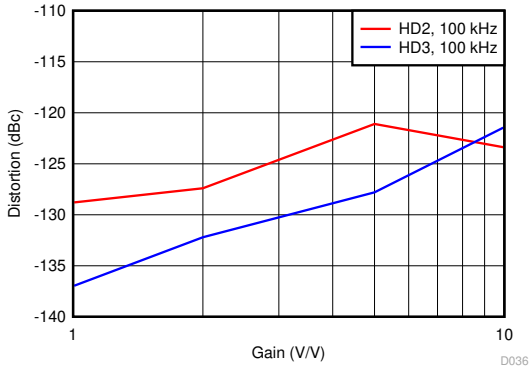
G = 1 V/V, V_{OUT} = 2-V_{PP} output, with R_L adjusted

図 7-34. Harmonic Distortion vs R_L



V_{OUT} = 2-V_{PP} output, with V_{OCM} adjusted

図 7-35. Harmonic Distortion vs V_{OCM}



V_{OUT} = 2-V_{PP} output, see 表 9-1 for gain setting

図 7-36. Harmonic Distortion vs Gain

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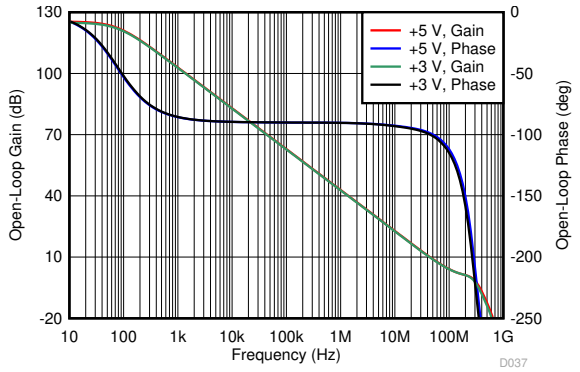
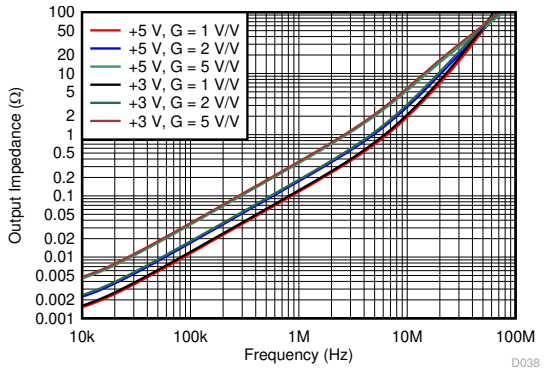
7.9 Typical Characteristics: 3-V to 5-V Supply Range

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



Simulated with a 1-kΩ differential load and 0.6-pF internal feedback capacitors removed

図 7-37. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Simulated closed-loop differential output impedance

図 7-38. Closed-Loop Output Impedance vs Frequency

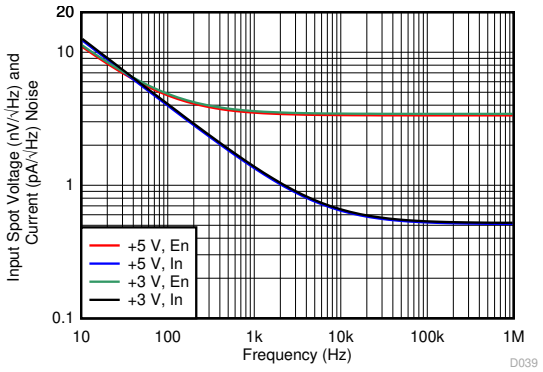
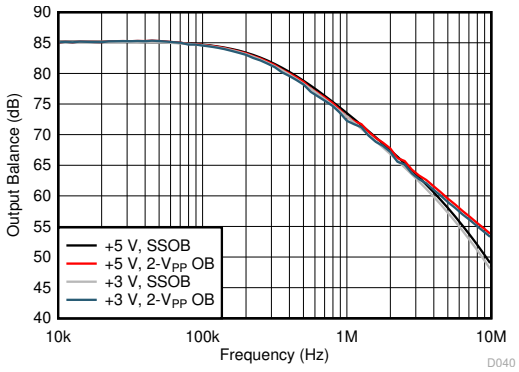
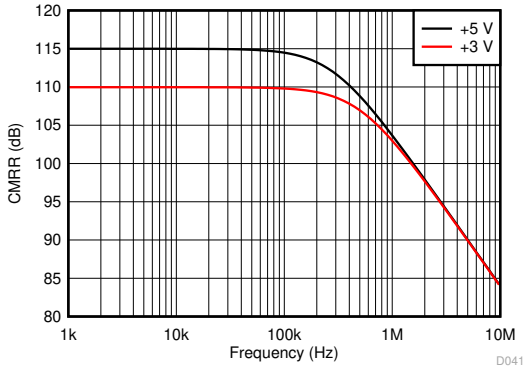


図 7-39. Input Spot Noise vs Frequency



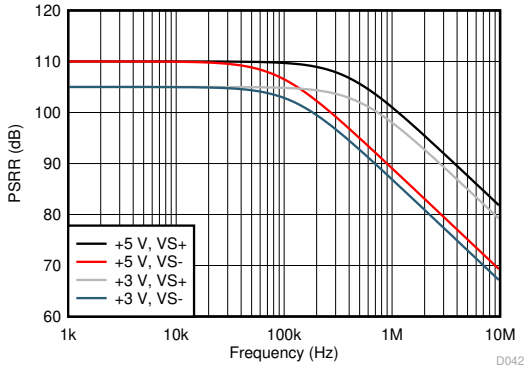
Differential mode output to common-mode output, simulated with G = 1 V/V

図 7-40. Output Balance vs Frequency



Common-mode input to differential output, simulated with G = 1 V/V

図 7-41. CMRR vs Frequency



Single-ended to differential gain of 1, PSRR simulated to differential output

図 7-42. Power-Supply Rejection Ratio vs Frequency

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7.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit

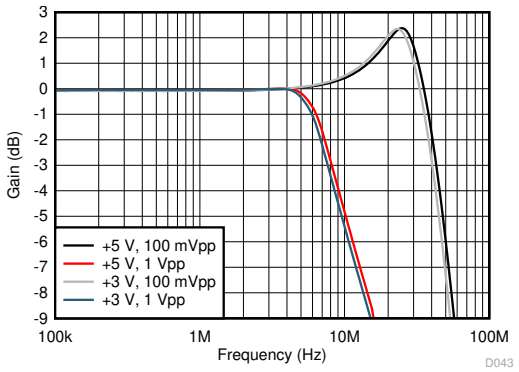


図 7-43. Common-Mode Voltage, Small- and Large-Signal Response (VOCM Pin Driven)

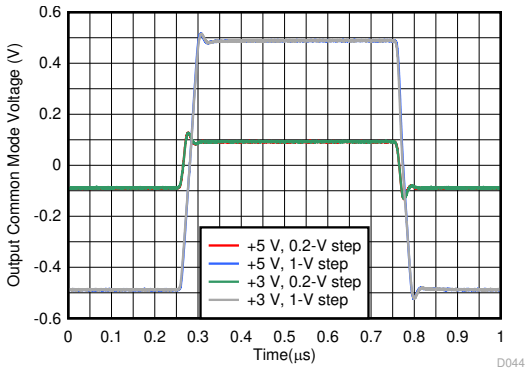
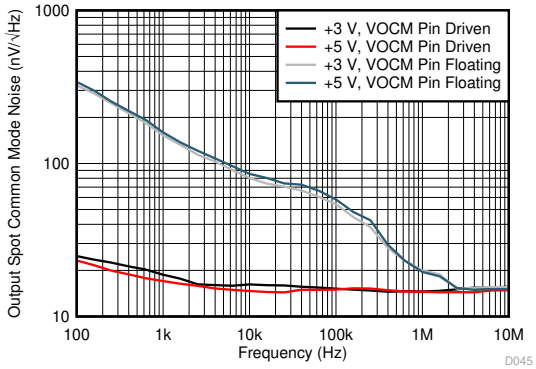
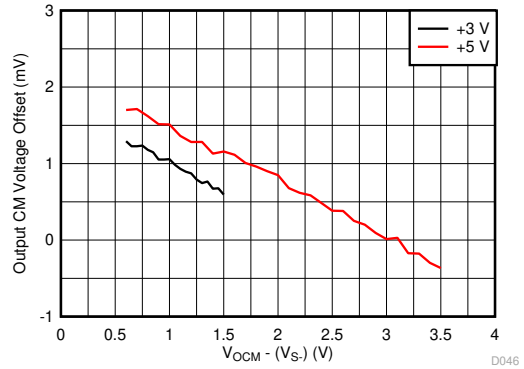


図 7-44. Common-Mode Voltage, Small- and Large-Step Response (VOCM Pin Driven)



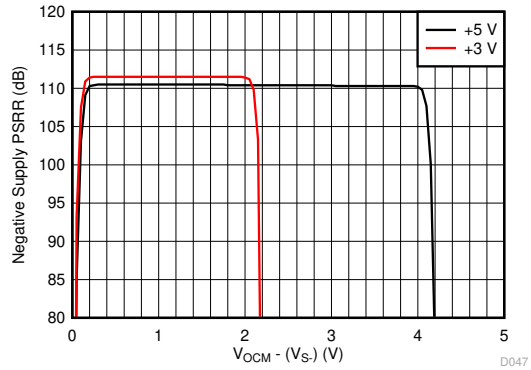
The VOCM pin is either driven to midsupply by low-impedance source or allowed to float and default to midsupply

図 7-45. Output Common-Mode Noise vs Frequency



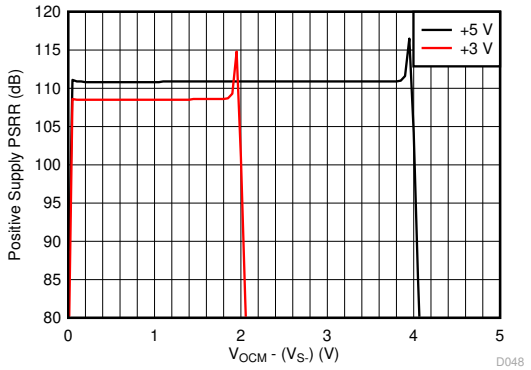
Average V_{OCM} output offset of 39 units, standard deviation < 2 mV

図 7-46. V_{OCM} Offset vs V_{OCM} Setting



Simulated with single-ended to differential gain of 1 , PSRR for negative supply to differential output

図 7-47. –PSRR vs V_{OCM} Approaching $V_{S–}$



Simulated with single-ended to differential gain of 1, PSRR for positive supply to differential output

図 7-48. +PSRR vs V_{OCM} Approaching V_{S+}

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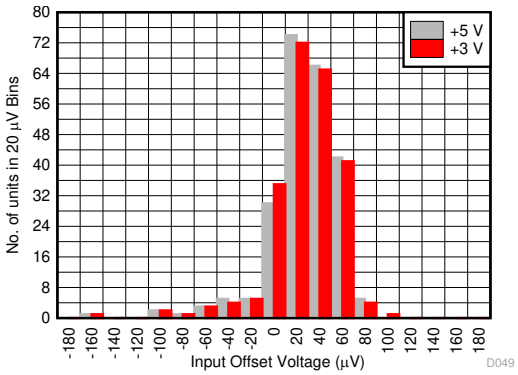
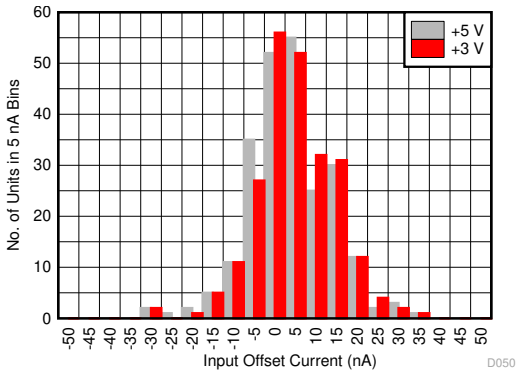
7.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD} = V_{S+}$, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



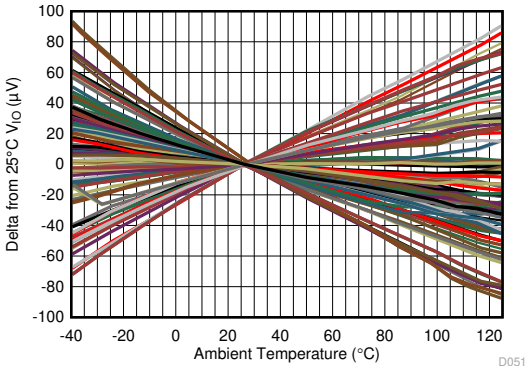
Total of 234 DGK units trimmed at a 5-V supply

図 7-49. Input Offset Voltage (V_{IO})



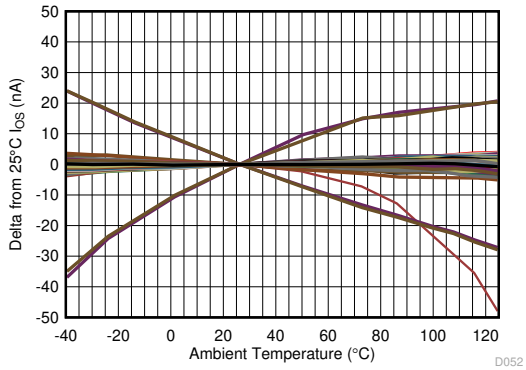
Total of 234 DGK units trimmed at a 5-V supply

図 7-50. Input Offset Current (I_{OS})



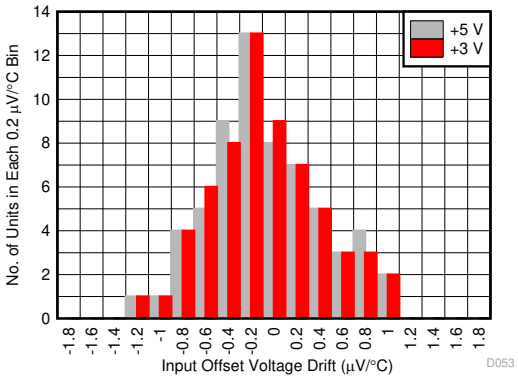
5-V and 3-V delta from 25°C V_{IO}, 50 DGK units

図 7-51. Input Offset Voltage vs Temperature



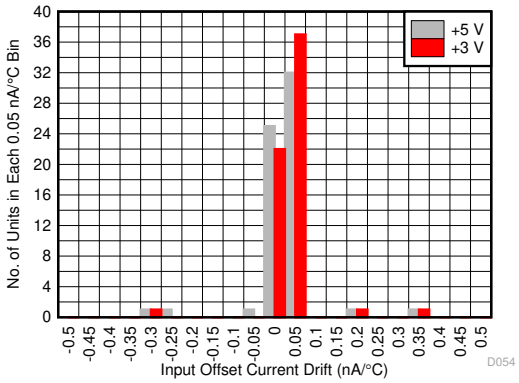
5-V and 3-V delta from 25°C I_{OS}, 50 DGK units

図 7-52. Input Offset Current vs Temperature



–40°C to +125°C endpoint drift, total of 62 DGK units

図 7-53. Input Offset Voltage Drift Histogram



–40°C to +125°C endpoint drift, total of 62 DGK units

図 7-54. Input Offset Current Drift Histogram

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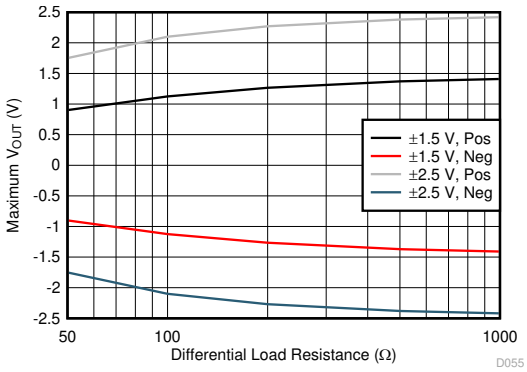
7.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at $T_A \approx 25°C$, VOCM pin = open, R_F = 1 kΩ, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}, 50-Ω input match, G = 1 V/V, $\overline{PD}$ = V_{S+}, single-ended input, differential output, and input and output referenced to default midsupply for ac-coupled tests (unless otherwise noted); see 図 8-1 for a gain of 1-V/V test circuit



Maximum differential output swing, V_{OCM} at midsupply

図 7-55. ±Maximum V_{OUT} vs Differential Load Resistance

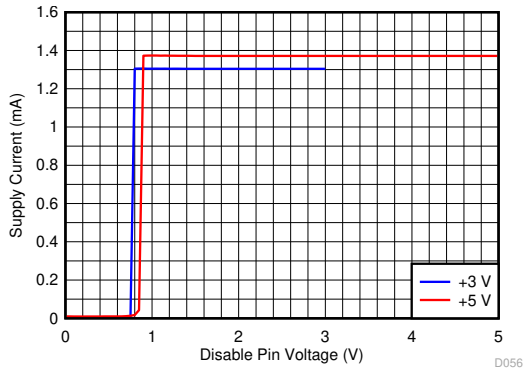
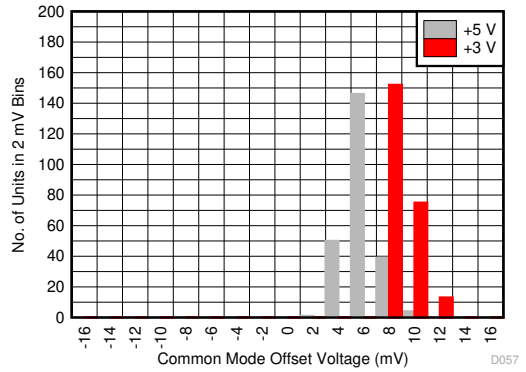
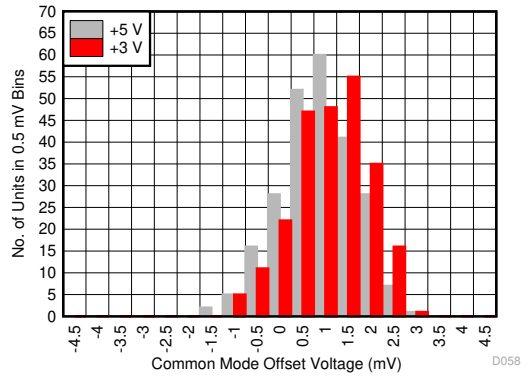


図 7-56. Supply Current vs $\overline{PD}$ Voltage



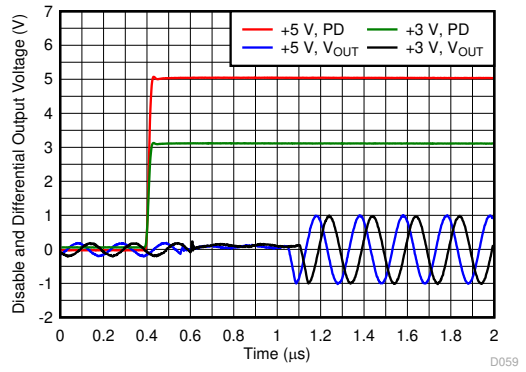
V_{OCM} input floating, total of 240 units

図 7-57. Common-Mode Output Offset from V_{S+} / 2 Default Value Histogram



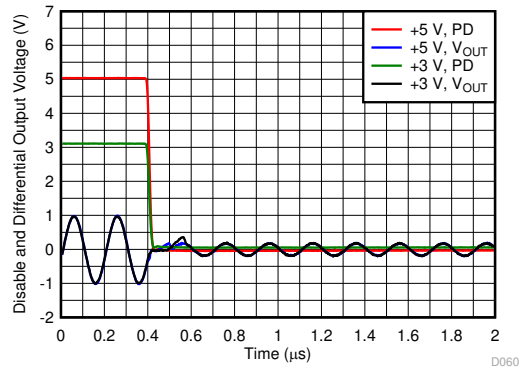
V_{OCM} Input driven to midsupply, total of 240 units

図 7-58. Common-Mode Output Offset from Driven V_{OCM} Histogram



5 MHz, 2-V_{PP} input, G = 1 V/V, see 図 8-1

図 7-59. $\overline{PD}$ Turn-On Waveform



5 MHz, 2-V_{PP} input, G = 1 V/V, see 図 8-1

図 7-60. $\overline{PD}$ Turn-Off Waveform

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8 Parameter Measurement Information

8.1 Example Characterization Circuits

The THS4551 offers the advantages of a fully differential amplifier (FDA) design with the trimmed input offset voltage and very low drift of a precision op amp. The FDA is an extremely flexible device where the main aim is to provide a purely differential output signal centered on a user-configurable common-mode voltage usually matched to the input common-mode voltage required by an analog-to-digital converter (ADC) following this stage. The primary options revolve around the choices of single-ended or differential inputs, ac-coupled or dc-coupled signal paths, gain targets, and resistor value selections. The characterizations described in this section focus on single-ended input to differential output designs as the more challenging application requirement. Differential sources can certainly be supported and are often simpler to both implement and analyze.

The characterization circuits are typically operated with a single-ended, matched, 50-Ω, input termination to a differential output at the FDA output pins because most lab equipment is single-ended. The FDA differential output is then translated back to single-ended through a variety of baluns (or transformers), depending on the test and frequency range. DC-coupled step response testing used two 50-Ω scope inputs with trace math. Single-supply operation is most common in end equipment designs. However, using split balanced supplies allows simple ground referenced testing without adding further blocking capacitors in the signal path beyond those capacitors already within the test equipment. The starting point for any single-ended input to differential output measurements (such as any of the frequency response curves) is shown in 図 8-1 (available as a TINA-TI ™ simulation file).

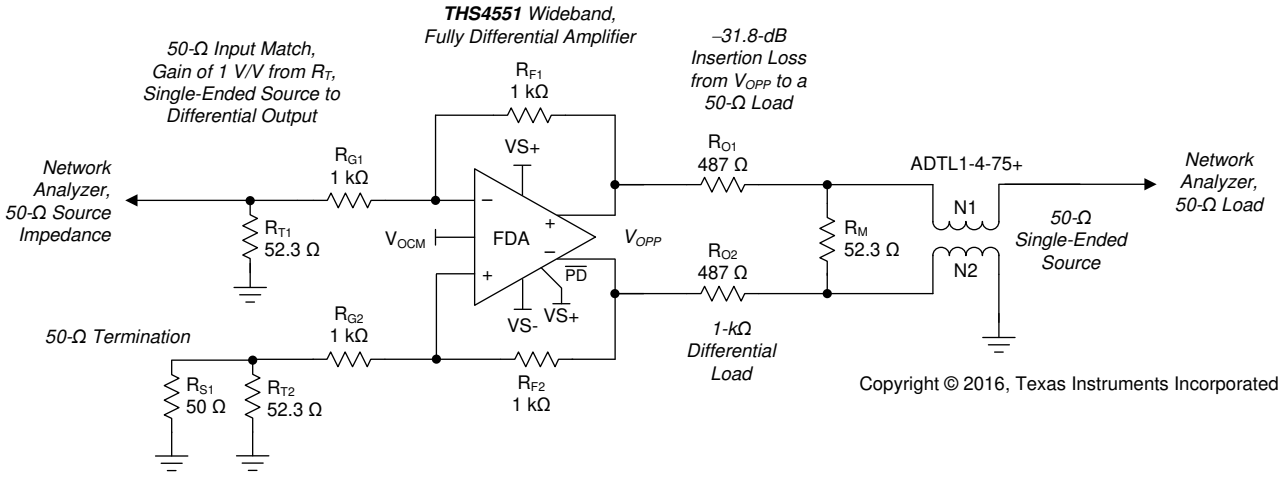

図 8-1. Single-Ended Source to a Differential Gain of a 1-V/V Test Circuit

Most characterization plots fix the R_F (R_{F1} = R_{F2}) value at 1 kΩ, as shown in 図 8-1. This element value is completely flexible in application, but 1 kΩ provides a good compromise for the parasitic issues linked to this value, specifically:

- Added output loading: the FDA functions similarly to an inverting op amp design with both feedback resistors appearing as an added load across the outputs (the approximate total differential load in 図 8-1 is 1 kΩ || 2 kΩ = 667 Ω). The 1-kΩ value also reduces the power dissipated in the feedback networks.
- Noise contributions resulting from resistor values: these contributions are both the $4kTR_F$ terms and the current noise times the R_F value to the output (see *セクション 10.1.1*).
- Parasitic feedback pole at the input summing nodes: this pole is created by the feedback resistor (R_F) value and the 1.2-pF differential input capacitance (as well as any board layout parasitic) and introduces a zero in the noise gain, thus decreasing the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot. Internal 0.6-pF feedback capacitors on each side combine with these external feedback resistors to introduce a zero in the noise gain, thereby reducing the effect of the feedback pole to the differential input capacitance.

The frequency domain characterization curves start with the selections of 図 8-1. Some of the features in this test circuit include:

- The elements on the non-signal input side exactly match the signal input resistors. This feature has the effect of more closely matching the divider networks on each side of the FDA. The three resistors on the non-signal input side can be replaced by a single resistor to ground using a standard E96 value of 1.02 kΩ with some loss in gain balancing between the two sides; see *セクション 9.3.4*).
- Translating from a 1-kΩ differential load to a 50-Ω environment introduces considerable insertion loss in the measurements (–31.8 dB in 図 8-1). The measurement path insertion loss is normalized out when reporting the frequency response curves to show the gain response to the FDA output pins.
- In the pass band for the output balun, the network analyzer 50-Ω load reflects to be in parallel with the 52.3-Ω shunt termination. These elements combine to show a differential 1-kΩ load at the output pins of the THS4551. The source impedance presented to the balun is a differential 50-Ω source. 図 8-2 and 図 8-3 show the TINA-TI™ model (available as a TINA-TI™ simulation file) and resulting response flatness for this relatively low-frequency balun providing 0.1-dB flatness through 100 MHz.

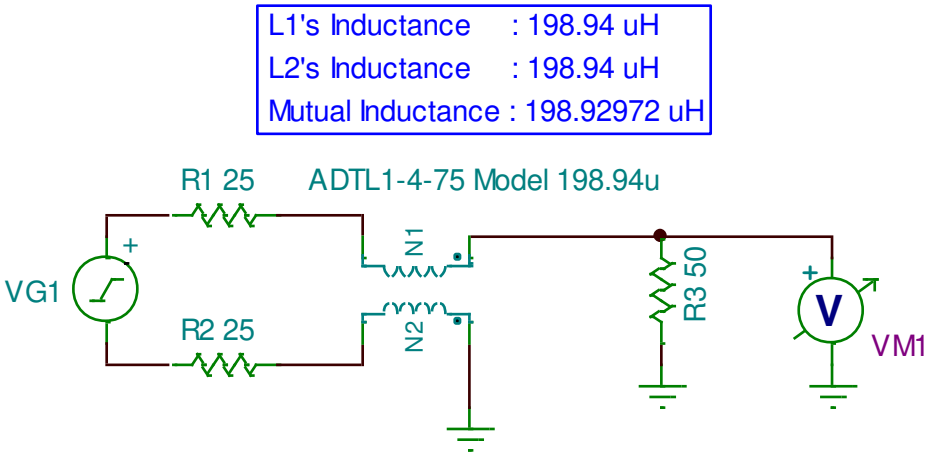

図 8-2. Output Measurement Balun Simulation Circuit in TINA-TI™

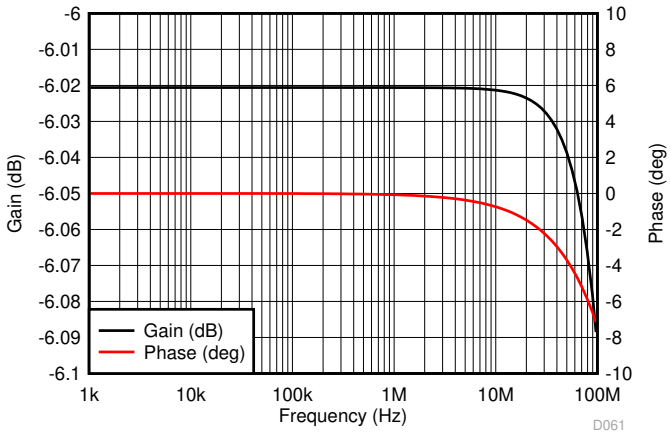

図 8-3. Output Measurement Balun Flatness Test

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Starting from the test circuit of 図 8-1, various elements are modified to show the effect of these elements over a range of design targets, specifically:

- The gain setting is changed by adjusting the R_T and the two R_G elements to provide a 50-Ω input match and setting the feedback resistors to 1 kΩ.
- Output loading of both resistive and capacitive load testing. Changing to lower resistive loads is accomplished by adding parallel resistors across the output pins in 図 8-1. Changing to capacitive loads adds series output resistors to a differential capacitance before the 1-kΩ sense path of 図 8-1.
- Power-supply settings. Most often, a single 5-V test uses a ±2.5-V supply and a 3-V test uses ±1.5-V supplies with the V_{OCM} input control at ground.
- The disable control pin ($\overline{PD}$) is tied to the positive supply (V_{S+}) for any active channel test.

8.2 Output Interface Circuit for DC-Coupled Differential Testing

The pulse response plots were taken using the output circuit of 図 8-4. The two sides of this circuit present a 500-Ω load to ground (for a differential 1-kΩ load) with a 50-Ω source to the two scope inputs. Trace math is used to combine the two sides into the pulse response plots of 図 7-7 to 図 7-10 and 図 7-25 to 図 7-28. Using balanced bipolar supplies for this test ensures that the THS4551 outputs deliver a ground-centered differential swing. This setup produces no dc load currents using the circuit of 図 8-4.

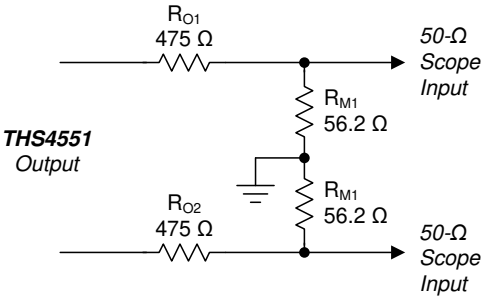

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図 8-4. Output Interface for DC-Coupled Differential Outputs

8.3 Output Common-Mode Measurements

The circuit of 図 8-5 is a typical setup for common-mode measurements.

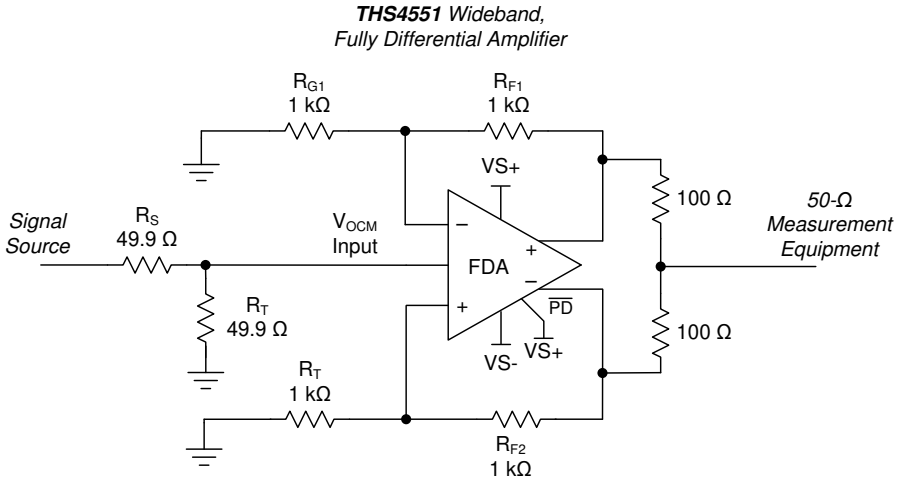

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図 8-5. Output Common-Mode Measurements

In 図 8-5, the differential path is simply terminated back to ground on the two 1-kΩ input resistors and the V_{OCM} control input is driven from a 50-Ω matched source for the frequency response and step response curves of 図 7-43 and 図 7-44. The outputs are summed to a center point (to obtain the average, or common-mode, output) through two 100-Ω resistors. These 100-Ω resistors form an equivalent 50-Ω source to the common-mode output for measurements. This common-mode test circuit is available as a TINA-TI™ simulation file. 図 7-45 illustrates the common-mode output noise measurements with either a ground on the VOCM input pin or with the VOCM input pin floating. The higher noise in 図 7-45 for a floated input can be reduced by including a capacitor to ground at the VOCM control input pin.

8.4 Differential Amplifier Noise Measurements

To extract out the input-referred noise terms from the total output noise, a measurement of the differential output noise is required under two external conditions to emphasize the different noise terms. A high-gain, low resistor value condition is used to emphasize the differential input voltage noise and a higher R_F at low gains is used to emphasize the two input current noise terms. The differential output noise must be converted to single-ended with added gain before being measured by a spectrum analyzer. At low frequencies, a zero 1/f noise, high-gain, differential to single-ended instrumentation amplifier (such as the INA188) is used. At higher frequencies, a differential to single-ended balun is used to drive into a high-gain, low-noise, op amp (such as the LMH6629). In this case, the THS4551 outputs drive 25-Ω resistors into a 1:1 balun where the balun output is terminated single-endedly at the LMH6629 input with 50 Ω. This termination provides a modest 6-dB insertion loss for the THS4551 differential output noise that is then followed by a 40-dB gain setting in the very wideband LMH6629.

8.5 Balanced Split-Supply Versus Single-Supply Characterization

Although most end applications use a single-supply implementation, most characterizations are done on a split balanced supply. Using a split balanced supply keeps the I/O common-mode inputs near midsupply and provides the most output swing with no dc bias currents for level shifting. These characterizations include the frequency response, harmonic distortion, and noise plots. The time domain plots are in some cases done via single-supply characterization to obtain the correct movement of the input common-mode voltage.

8.6 Simulated Characterization Curves

In some cases, a characteristic curve can only be generated through simulation. A good example of this scenario is the output balance plot of 図 7-40. This plot shows the best-case output balance (output differential signal versus output common-mode signal) using exact matching on the external resistors in simulation using a single-ended input to differential output configuration. The actual output balance is set by resistor mismatch at low frequencies but intersects and follows the high-frequency portion of 図 7-40.

The remaining simulated plots include:

- A_{OL} gain and phase, see 図 7-37.
- Large- and small-signal settling times, see 図 7-11 and 図 7-29.
- Closed-loop output impedance versus frequency, see 図 7-38.
- CMRR vs frequency, see 図 7-41.
- PSRR vs frequency and output common-mode voltage, see 図 7-42, 図 7-47, and 図 7-48.

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8.7 Terminology and Application Assumptions

Numerous common terms that are unique to this type of device exist. This section identifies and explains these terms.

- Fully differential amplifier (FDA). This term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not a high-impedance input) and includes a second internal control loop that sets the output average voltage (V_{OCM}) to a default or set point. This second common-mode control loop interacts with the differential loop in certain configurations.
- The desired output signal at the two output pins is a differential signal that swings symmetrically around a common-mode voltage, which is the average voltage for the two outputs.
- Single-ended to differential. The output must always be used differentially in an FDA; however, the source signal can be either a single-ended or a differential source with a variety of implementation details for either source. For an FDA operating in single-ended to differential, only one of the two input signals is applied to one of the input resistors.
- The common-mode control has limited bandwidth from the input VOCM pin to the common-mode output voltage. The internal loop bandwidth beyond the input V_{OCM} buffer is a much wider bandwidth than the reported V_{OCM} bandwidth, but is not directly discernable. A very wide bandwidth in the internal V_{OCM} loop is required to perform an effective and low-distortion single-ended to differential conversion.

Several features in the application of the THS4551 are not explicitly stated, but are necessary for correct operation. These features are:

- Good power-supply decoupling is required. Often a larger capacitor (2.2 µF, typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins (share this capacitor with the four supply pins in the RGT package). For single-supply operation, only the positive supply has these capacitors. Where a split supply is used, connect these capacitors to ground on both sides with the larger capacitor placed some distance from the package and shared among multiple channels of the THS4551, if used. A separate 0.1-µF capacitor must be provided to each device at the device power pins. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor to the local high-frequency decoupling capacitor is often useful.
- Although often not stated, the power disable pin ($\overline{PD}$) is tied to the positive supply when only an enabled channel is desired.
- Virtually all ac characterization equipment expects a 50-Ω termination from the 50-Ω source and a 50-Ω, single-ended source impedance from the device outputs to the 50-Ω sensing termination. This condition is achieved in all characterizations (often with some insertion loss) but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the THS4551, and to an ADC input do not require doubly-terminated lines or filter designs. The only exception is if the source requires a defined termination impedance for correct operation (for example, mixer outputs).
- The amplifier signal path is flexible for use as single- or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used as long as the total supply voltage across the TH4551 is less than 5.5 V and the required input, output, and common-mode pin headrooms to each supply are taken into account. When left open, the VOCM pin defaults to near midsupply for any combination of split or single supplies used. The disable pin ($\overline{PD}$) is referenced to the negative rail. Using a negative supply requires that $\overline{PD}$ be pulled down to within 0.55 V of the negative supply to disable the amplifier.
- External element values are normally assumed to be accurate and matched. In an FDA, this assumption translates to equal feedback resistor values and a matched impedance from each input summing junction to either a signal source or a dc bias reference on each side of the inputs. Unbalancing these values introduces non-idealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides creates a common-mode to differential conversion. Furthermore, mismatched R_F values and feedback ratios create additional differential output error terms from any common-mode dc or ac signal or noise terms. Using standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Modestly mismatched resistors or ratios do not by themselves degrade harmonic distortion. Where there is a meaningful common-mode noise or distortion coming in that gets converted to differential via an element or ratio mismatch. For the best dc precision, use 0.1% accuracy resistors that are readily available in E96 values (1% steps).

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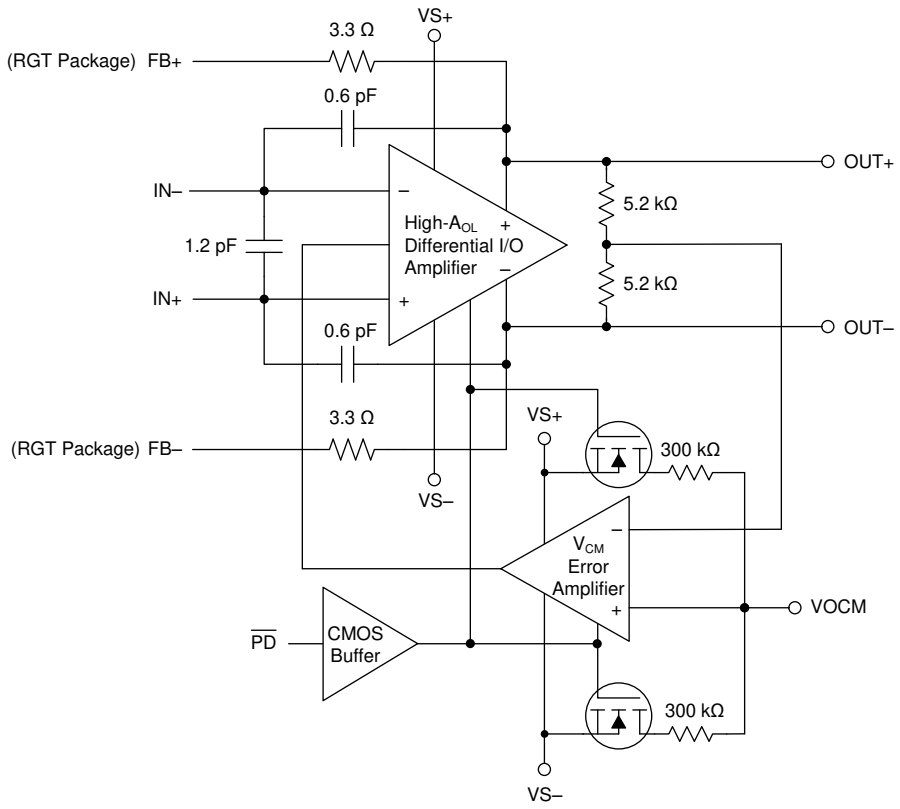
9 Detailed Description

9.1 Overview

In addition to the core differential I/O voltage feedback gain block, there are two 5.2-kΩ resistors internally across the outputs to sense the average voltage at the outputs. These resistors feed the average voltage back into a V_{CM} error amplifier where the voltage is compared to either a default voltage divider across the supplies or an externally set V_{OCM} target voltage. When the amplifier is disabled, the default midsupply bias string is disabled to save power.

To achieve the very-low noise at the low power provided by the THS4551, the input stage transistors are relatively large, thus resulting in a higher differential input capacitance (1.2 pF in the *セクション 9.2*). As a default compensation for the 1.2-pF differential input capacitance and the 1-kΩ feedback resistors used in characterization, internal 0.6-pF capacitors are placed between the two output and input pins. Adjust any desired external feedback capacitor value to account for these 0.6-pF internal elements. When using the 16-pin WQFN package and the internal feedback traces to the input side of the package, include the nominal trace impedance of 3.3 Ω in the design. These elements are not included in the TINA-TI™ model and must be added externally to a design intending to use the RGT package.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Differential Open-Loop Gain and Output Impedance

The most important elements to the closed-loop performance are the open-loop gain and open-loop output impedance. 図 9-1 and 図 9-2 show the simulated differential open-loop gain and phase from the differential inputs to the differential outputs with no load and with a 100-Ω load. Operating with no load removes any effect introduced by the open-loop output impedance to a finite load. This A_{OL} simulation removes the 0.6-pF internal feedback capacitors to isolate the forward path gain and phase (see 図 13-1). The 0.6-pF capacitance becomes part of the feedback network that sets the noise gain and phase combined with the external elements. The simulated differential open-loop output impedance is shown in 図 9-3.

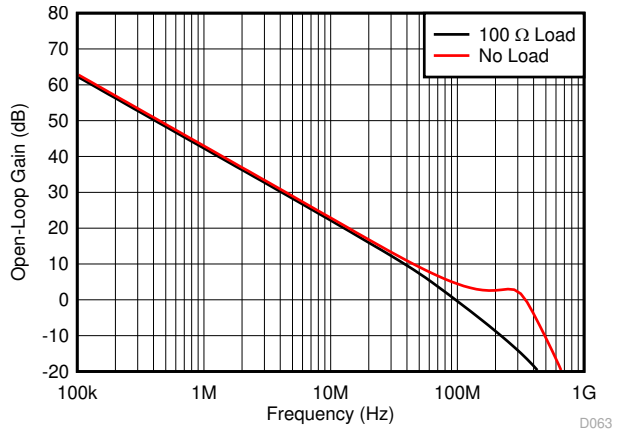

図 9-1. No-Load and 100-Ω Loaded A_{OL} Gain

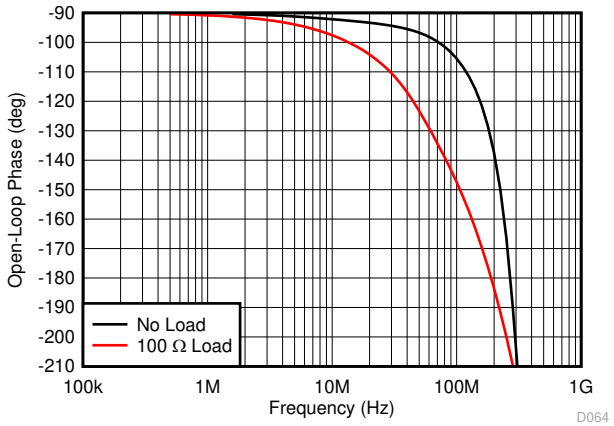

図 9-2. No-Load and 100-Ω A_{OL} Phase

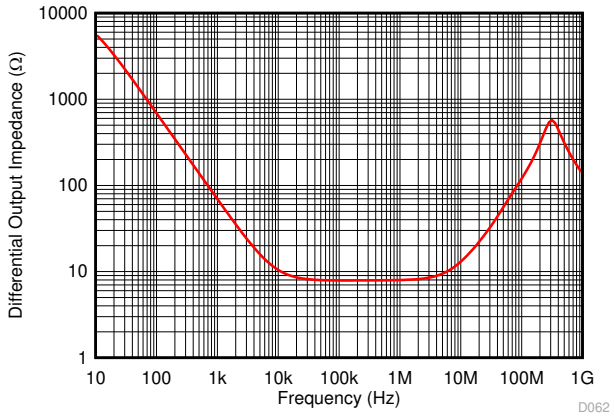

図 9-3. Differential Open-Loop Output Impedance

This impedance combines with the load to shift the apparent open-loop gain and phase to the output pins when the load changes. The rail-to-rail output stage shows a very high impedance at low frequencies that reduces with frequency to a lower midrange value and then peaks again at higher frequencies. The maximum value at low frequencies is set by the common-mode sensing resistors to be a 10.5-kΩ dc value (see *セクション 9.2*). This high impedance at a low frequency is significantly reduced in closed-loop operation by the loop gain, as shown in the closed-loop output impedance of 図 7-38. 図 9-1 compares the no load A_{OL} gain to the A_{OL} gain driving a 100-Ω load that shows the effect of the output impedance. The heavier loads pull the A_{OL} gain down faster to lower crossovers with more phase shift at the lower frequencies.

The much faster phase rolloff for the 100-Ω differential load explains the greater peaked response illustrated in 図 7-4 and 図 7-22 when the load decreases. This same effect happens for the RC loads common with converter interface designs. Use the TINA-TI™ model to verify loop phase margin in any design.

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9.3.2 Setting Resistor Values Versus Gain

The THS4551 offers considerable flexibility in the configuration and selection of resistor values. The design starts with the selection of the feedback resistor value. The 1-kΩ feedback resistor value used for the characterization curves is a good compromise between power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side) the input resistors are set to obtain the desired gain with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O.

For single-ended, matched, input impedance designs, 表 9-1 illustrates the suggested standard resistors set to approximately a 1-kΩ feedback. This table assumes a 50-Ω source and a 50-Ω input match and uses a single resistor on the non-signal input side for gain matching. Better matching is possible using the same three resistors on the non-signal input side as on the input side. 図 9-4 shows the element values and naming convention for the gain of 1-V/V configuration where the gain is defined from the matched input at R_T to the differential output.

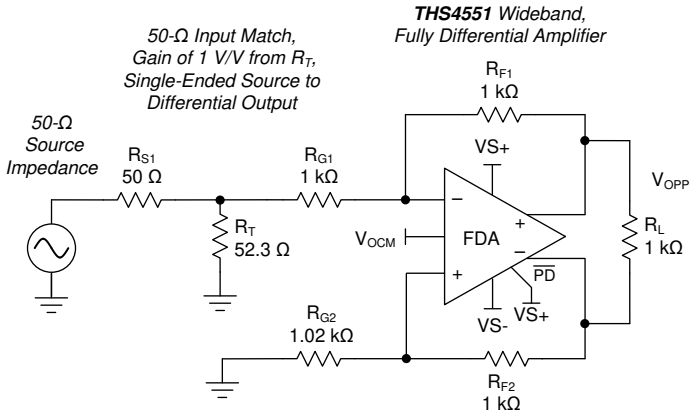

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図 9-4. Single-Ended to Differential Gain of 1 V/V with Input Matching Using Standard Resistor Values

Starting from a target feedback resistor value, the desired input matching impedance, and the target gain (A_V), the required input R_T value is given by solving the quadratic of 式 1.

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2+A_V) - R_S A_V(4+A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2+A_V) - R_S A_V(4+A_V)} = 0 \quad (1)$$

When this value is derived, the required input side gain resistor is given by 式 2 and then the single value for R_{G2} on the non-signal input side is given by 式 3:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \quad (2)$$

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \quad (3)$$

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Using these expressions to generate a swept gain table of values results in 表 9-1, where the best standard 1% resistor values are shown to minimize input impedance and gain error to target.

表 9-1. Swept Gain 50-Ω Input Match with R_F = 1-kΩ (±1 Standard Values)

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V
0.1	1000	10000	49.9	10000	49.66	0.09965
1	1000	976	51.1	1000	49.2	1.0096
2	1020	499	52.3	523	48.9	1.988
5	1000	187	59	215	50.2	5.057
10	1020	88.7	69.8	118	50.6	10.09

Where an input impedance match is not required, simply set the input resistor to obtain the desired gain without an additional resistor to ground (remove R_T in 図 9-4). This scenario is common when coming from the output of another single-ended op amp (such as the OPA192). This single-ended to differential stage shows a higher input impedance than the physical R_G as given by the expression for Z_A (active input impedance) shown as 式 4.

$$Z_A = R_{G1} \frac{\left(1 + \frac{R_{G1}}{R_{G2}}\right)\left(1 + \frac{R_F}{R_{G1}}\right)}{2 + \frac{R_F}{R_{G2}}} \tag{4}$$

Using 式 4 for the gain of 1 V/V with all resistors equal to 1-kΩ shows an input impedance of 1.33 kΩ. The increased input impedance comes from the common-mode input voltage at the amplifier pins moving in the same direction as the input signal. The common-mode input voltage must move to create the current in the non-signal input R_G resistor to produce the inverted output. The current flow into the signal-side input resistor is impeded because the common-mode input voltage moves with the input signal, thus increasing the apparent input impedance in the signal input path.

9.3.3 I/O Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage for the THS4551. For ac-coupled signal paths, this voltage is often the default midsupply voltage to retain the most available output swing around the voltage centered at the V_{OCM} voltage. For dc-coupled designs, set this voltage with consideration to the required minimum headroom to the supplies as described in the specifications of the *Electrical Characteristics* table for the V_{OCM} control. For precision ADC drivers, this output V_{OCM} becomes the input V_{CM} to the ADC. Often, V_{CM} is set to V_{REF} / 2 to center the differential input on the available input when precision ADCs are being driven.

From the target output V_{OCM}, the next step is to verify that the desired output differential peak-to-peak voltage (V_{OPP}) stays within the supplies. For any desired differential V_{OPP}, make sure that the absolute maximum voltage at the output pins swings with 式 5 and 式 6 and confirm that these expressions are within the supply rails minus the output headroom required for the RRO device.

$$V_{Omax} = V_{OCM} + \frac{V_{OPP}}{4} \tag{5}$$

$$V_{Omin} = V_{OCM} - \frac{V_{OPP}}{4} \tag{6}$$

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For instance, when the THS4551 drives the ADC3223 with a 0.95-V_{CM} control using a single 3.0-V supply, the negative-going signal sets the maximum output swing from 0.95 V_{CM} to 0.2 V above ground. This 0.75-V, single-sided swing becomes an available 4 × 0.75 V = 3-V_{PP} differential around the nominal 0.95-V_{CM} output common-mode voltage. On the high side, the maximum output is equal to 1.7 V (0.95 V + 0.75 V), which is well within the allowed maximum range of 2.8 V (3.0 V – 0.2 V). This available 3-V_{PP} maximum differential output is also well beyond the maximum value required for the 2-V_{PP} input ADS3223.

With the output headrooms confirmed, the input junctions must also stay within the operating range. The input range limitations only appear when approaching the positive supply where a maximum 1.3-V headroom is required over the full temperature range because the input range extends to the negative supply voltage over the full temperature range.

The input pins operate at voltages set by the external circuit design, the required output V_{OCM}, and the input signal characteristics. For differential-to-differential designs where there is no signal-related movement in the input V_{ICM} voltages, ac-coupled differential input designs have a V_{ICM} equal to the output V_{OCM}. Going towards the positive supply, the output common-mode can be set to within 1.2 V of the supply. AC-coupled input designs violate the required 1.3-V headroom on the input pins in this case. Going towards the negative supply on the V_{OCM} setting requires a minimum of 0.55 V above the supply. This extreme is always in range for the input pins that require a minimum 0-V headroom to the negative supply.

DC-coupled differential input designs must check the voltage divider from the source common-mode input voltage to the THS4551 V_{OCM} setting. This result must be equal to an input V_{ICM} within the specified range. If the source V_{CM} can vary over some voltage range, validate this result over that range before proceeding.

For single-ended input to differential output designs, the V_{ICM} is nominally at a voltage set by the external configuration with a small swing around the nominal value because of the common-mode loop. An ac-coupled, single-ended input to differential output design places an average input V_{ICM} equal to the output V_{OCM} for the FDA with an ac-coupled swing around the V_{OCM} voltage following the input voltage. A dc-coupled, single-ended input to differential design gets a nominal input V_{ICM} set by the source signal common-mode level and the V_{OCM} output voltage with a small signal-related swing around the nominal V_{ICM} voltage.

One approach to deriving the V_{ICM} voltage range for any single-ended input to differential output design is to observe the output voltage swing on the non-signal input side of the FDA outputs and simply take the voltage division on the input pin to ground or to the dc reference used on that side. An example analysis is shown in 図 9-5 using a Thevenized version of the gain of 2 values listed in 表 9-1 for a 50-Ω matched impedance, ac-coupled design.

In this example, a single 3.3-V supply is used with the V_{OCM} defaulted to midsupply or 1.65 V as a common-mode output voltage. This value is also the common-mode voltage on the input pins for the ac-coupled input to the FDA. Targeting a 4-V_{PP} differential output swing means each output pin swings ±1 V around this 1.65-V common-mode voltage. This output swing is in range because the full swing is 0.65 V to 2.65 V relative to ground, which is well within the 0.2-V output headroom requirements on a single 3.3-V supply.

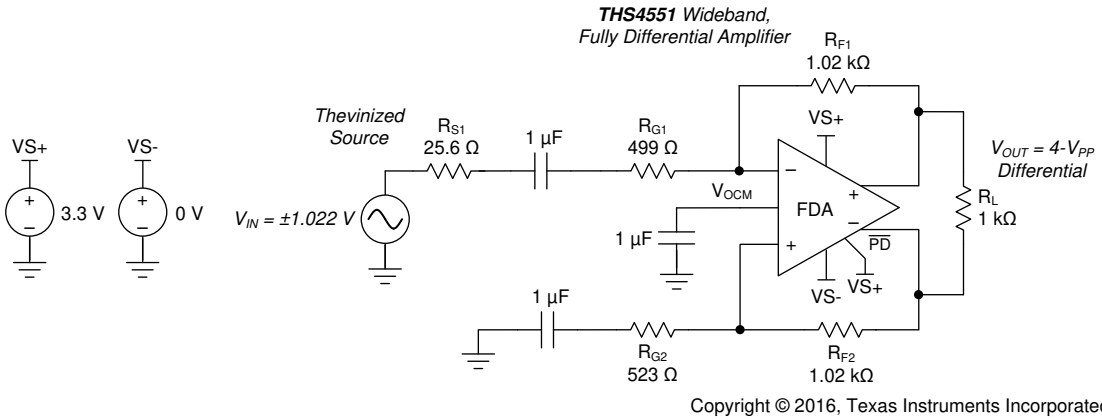

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図 9-5. Input Swing Analysis Circuit with AC-Coupled, Single-Ended to Differential Signal Path

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The output on the lower side of this design ranges from 0.65 V to 2.65 V. This 2-V_{PP} swing (on just one side, the other output is an inverted version and gives the 4-V_{PP} differential maximum) is divided back by the R_{F2} and R_{G2} divider to the input pins to form a common-mode input swing on top of the 1.65-V input common-mode voltage. This divider is 0.339 × 2 V_{PP} = 0.678 V_{PP} or ±0.34 V around the 1.65-V input common-mode voltage. The 1.31-V to 1.99-V common-mode input swing for this design is in range for the 0 V to 2.2 V available input range (the maximum headroom is 3.3 V – 1.1 V, which is equal to 2.2 V). These voltage swings can be directly observed using the SBOC460 TINA-TI™ simulation file. Shifting the V_{OCM} down slightly (if allowed by the design requirements) is a good way to improve the positive-swinging input headroom for this low-voltage design.

Taking a more complex example by using the THS4551 to attenuate a large bipolar input signal in a dc-coupled design for an ADC is shown in 図 9-6. To remove the peaking for this low-noise gain design, the two C_F elements and an input capacitor are added to shape the noise gain at high frequencies to a capacitive divider, as described in the *セクション 10.1.6*. In this example (including the 1.2-pF internal differential capacitor at the inputs and the 0.6-pF internal feedback capacitors), the high-frequency noise gain is 3 V/V and a flat frequency response with approximately 45 MHz of –3-dB BW is delivered.

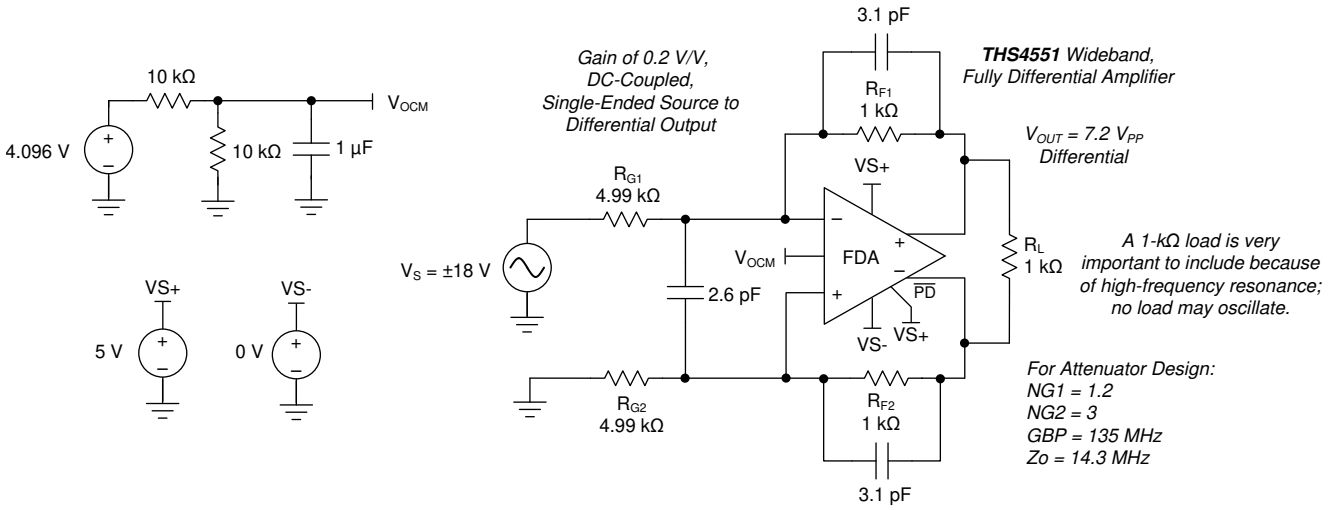

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図 9-6. DC-Coupled, Single-Ended to Differential Attenuator Design

In this example, the output V_{OCM} is 4.096 V / 2, which equals 2.048 V and the source signal V_{CM} is 0 V. These values set the nominal input pin V_{ICM} to 2.048 V × 4.99 kΩ / (4.99 kΩ + 1 kΩ) = 1.71 V. Applying a ±18-V input at the 4.99-kΩ input resistor produces a 7.2-V_{PP} differential output. That is, a ±1.8-V swing on the lower output side around the 2.048-V common-mode voltage. This 0.248-V to 3.84-V relative-to-ground swing at the output is well within the 0.2-V output headrooms to the 0-V to 5-V supplies used in the example in 図 9-6 (with the same swing inverted on the other output side). That output swing on the lower side produces an attenuated input common mode swing of (±1.8 V × (4.99 kΩ / (4.99 kΩ + 1 kΩ)) = ±1.5 V around the midscale input bias of 1.71 V. This 0.2-V to 3.2-V input common-mode swing is well within the available 0-V to 3.8-V input range. This ±18-V bipolar input signal is delivered to a SAR ADC with a 7.2-V_{PP} differential output with all I/O nodes operating in range using a single 5-V supply design. The source must sink the 2.048 V / 5.99 kΩ = 0.34-mA common-mode level-shifting current to take the input 0-V common-mode voltage up to the midscale 1.71-V V_{ICM} operating voltage. Using the single-ended input impedance of 式 4, the source must also drive an apparent input load of 5.44 kΩ.

Most designs do not run into an input range limit. However, using the approach shown in this section can allow a quick assessment of the input V_{ICM} range under the intended full-scale output condition. The TINA-TI™ simulation file for 図 9-6 can be used to plot the input voltages under the intended swings and application circuit to verify that there is no limiting from this effect. Driving the I/O nodes out of range in the TINA-TI™ model results in convergence problems. Increasing the positive and negative supplies slightly in simulation is an easy way to discover the simulated swings that might be going out of range.

As a third example of arriving at the input pin voltage swings, use the design of 図 10-17 (the ADC3241 design). Thevenize the source to just one input resistor to get an expression for the input V_{ICM} in terms of the input voltage to be derived. 図 9-7 shows the gain of 5 V/V, dc-coupled, matched input impedance, single-ended to differential circuit of 図 10-17 with both sides reduced to a single input resistor. In 図 10-17, the design operates on a single 3.3-V supply with an output V_{OCM} equal to 0.95 V to directly connect to TI's line of low-power ADC3xxx series of 12- and 14-bit ADCs. This family accepts a 2-V_{PP} maximum differential voltage, which (at the input-terminating resistor of 図 10-17) is a ±0.2-V swing. Going back to the source through the matching resistor is then a ±0.4-V source swing. Thevenizing that source with the R_T element provides the ±0.217 V shown in 図 9-7 and the total R2 as the sum of R_{G1} and 50 Ω || 59 Ω.

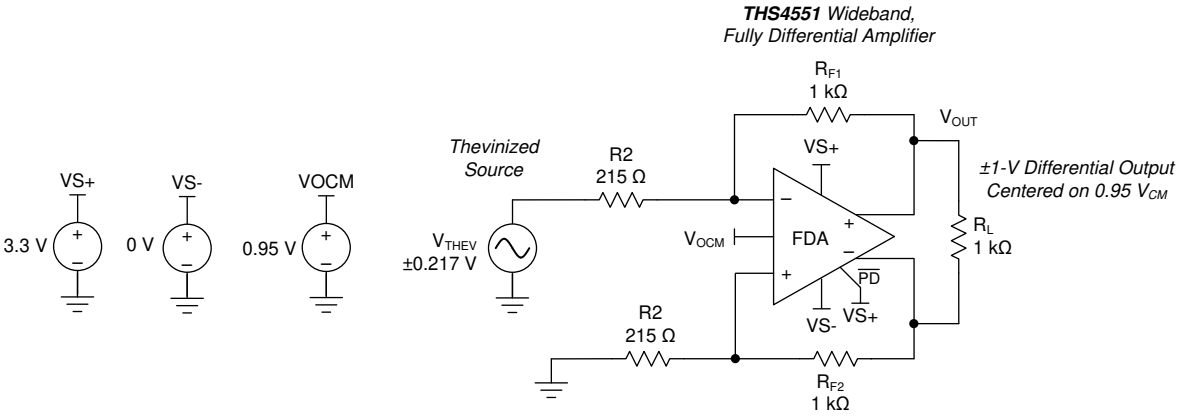

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図 9-7. Input V_{ICM} Analysis Circuit From the Design of 図 10-17

For an input signal (V_{THEV}) that swings around ground as ±V_{THEV}, the input pins are within a range given by 式 7, which is a superposition of the output V_{OCM} divided back to the input nodes and half of the input ±V_{THEV} signal.

$$V_{ICM} = V_{OCM}\frac{R_G}{R_G + R_F} \pm \frac{V_{THEV}}{2} \times \frac{R_F}{R_F + R_G} \tag{7}$$

Using the values from the design of 図 9-7, the computed input range for the THS4551 input pins is V_{ICM} = 0.168 V ± 0.89 mV or 0.079 V to 0.257 V at the input pins. These values are well within range for the negative rail input available in the THS4551.

A simpler approach to arriving at the input common mode range for this DC coupled single supply design would be to take the output voltage swing range on the lower side (non – signal input side) and simply divide it back through its resistor divider to ground on that side.

The output pin voltage swing is 0.95 V ± 0.5 V or 0.45 V to 1.45 V. This swing is divided back to the input V_{ICM} by a 215 / (215 + 1000) = 0.177 ratio. This ratio computes the input pin range as 79 mV to 0.256 V, matching the input source swing results in 式 7. The TINA-TI™ model for 図 9-7 (available as SBOC472) also provides these input swings as shown in the simplified circuit of 図 9-8. The large centered swing is the differential output voltage at the THS4551 output pins (which is actually the two outputs swinging ±0.5 V around a 0.95 V_{CM}), the small centered bipolar swing is the input swing for the thevenized source of 図 9-8, and the smallest V_{PP} swing on a dc offset is the input V_{ICM} voltage at the non-signal side input for the circuit of 図 9-8.

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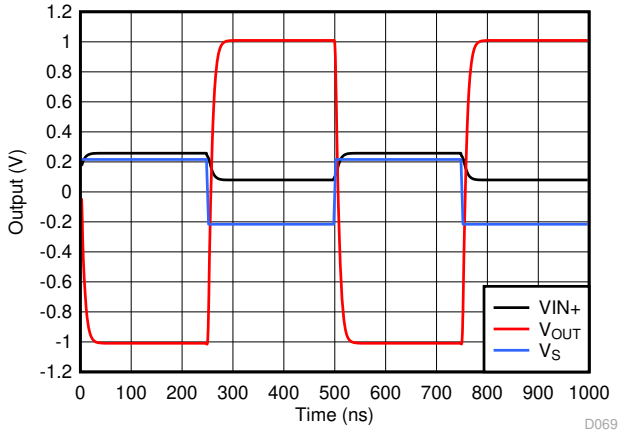

図 9-8. I/O Swing Simulation Using the TINA-TI™ Model

9.3.4 Output DC Error and Drift Calculations and the Effect of Resistor Imbalances

The THS4551 offers a trimmed input offset voltage and extremely low offset drift over the full –40°C to +125°C operating range. This offset voltage combines with several other error contribution terms to produce an initial 25°C output offset error band and then a drift over temperature. For each error term, a gain must be assigned to that term. For this analysis, only dc-coupled signal paths are considered. One new source of output error (versus the typical op amp analysis) arises from the effect mismatched resistor values and ratios can have on the two sides of the FDA. Any common-mode error or drift creates a differential output error through the slight mismatches arising from the external feedback and gain setting resistor tolerances or standard value constraints.

The error terms (25°C and drift), along with the gain to the output differential voltage, include input offset voltage and input offset current. Input offset voltage has a gain equal to the noise gain or $1 + R_F / R_G$, where R_G is the total dc impedance from the input pins back to the source or a dc reference (typically ground). Input offset current has a gain to the differential output through the average feedback resistor value.

The remaining terms arise from an assumed range on both the absolute feedback resistor mismatch and the mismatch in the divider ratio on each side of the FDA. The first of these resistor mismatch terms is the input bias current that creates a differential output offset via R_F mismatch. For simplicity, the upper R_F and R_G values are termed R_{F1} and R_{G1} with a ratio of $R_{F1} / R_{G1} \equiv G1$. The lower elements are defined as R_{F2} and R_{G2} with a ratio of $R_{F2} / R_{G2} \equiv G2$. To compute worst-case contributions, a maximum variation in the design resistor tolerance is used in the absolute and ratio mismatches.

For instance, ±1% tolerance resistors are assumed, giving a worst-case G1 that is 2% higher than nominal and a G2 that is 2% lower than nominal with a worst-case R_F value mismatch of 2% as well. Using a 0.1% precision resistor reduces the gain for the input bias current, but because these precision resistors are usually only available in 1% value steps, a gain mismatch term may still need to be considered. For matched impedance designs with R_T and R_{G1} on a single-ended to differential stage, the standard value constraint imposes a fixed mismatch in the initial feedback ratios with the tolerance of the resistors around the ratio if the non-signal input side uses a single resistor for R_{G2}.

Define the selected external resistor tolerance as ±T (so for 1% tolerance resistors, T = 0.01). Input bias current times the feedback resistor mismatch gain is $\pm 2 \times T \times R_{Fnom}$.

Anything that generates an output common-mode level or shift over temperature also generates an output differential error term if the two feedback ratios, G1 and G2, are not equal. An error trying to produce a shift in the output common-mode voltage is overridden by the common-mode control loop where the error becomes a balanced differential error around the output V_{OCM}.

The terms that create a differential error from a common-mode term and feedback ratio mismatch include the desired V_{OCM} voltage, any source common-mode voltage, any drift on the reference bias to the V_{OCM} control pin, any internal offset and drift in the V_{OCM} control path, and the input average bias current and drift.

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Considering just the output common-mode control and the source common-mode voltage, the conversion to output differential offsets is through 式 8.

$$V_{OD} = \frac{V_{OCM}(G1 - G2) - V_{ICM}(G1 - G2)}{1 + \frac{G1 + G2}{2}} \quad (8)$$

Neglecting any G1 and G2 mismatch because of standard values constraint, the conversion gain for these two terms can be recast in terms of the nominal R_F / R_G ≡ G and the tolerance T, as shown in 式 9. When G increases, this conversion gain approaches 4T.

$$\frac{V_{OD}}{V_{OCM}} = \frac{G}{(1 + G)} \bullet \frac{4T}{(1 - T^2)} \quad (9)$$

This conversion gain to differential output error is applied to two error terms: V_{OCM} and the input bias current and drift. (The source common-mode voltage is assumed to be 0 V. If not, apply this gain to the source common-mode voltage and any resulting shift in application.)

The output error is applied to V_{OCM}, assuming that the input control pin is driven and not floating. The input bias current and drift are multiplied by the average R_F value then by the conversion gain to differential output error to create an added output differential error.

As an example of using these terms to estimate the worst-case output 25°C error band and then the worst-case drift (by adding all error terms together independently), use the gain of 1-V/V configuration with R_F = 1 kΩ and assume a ±1% tolerance on the resistors with the standard values used in 図 9-9.

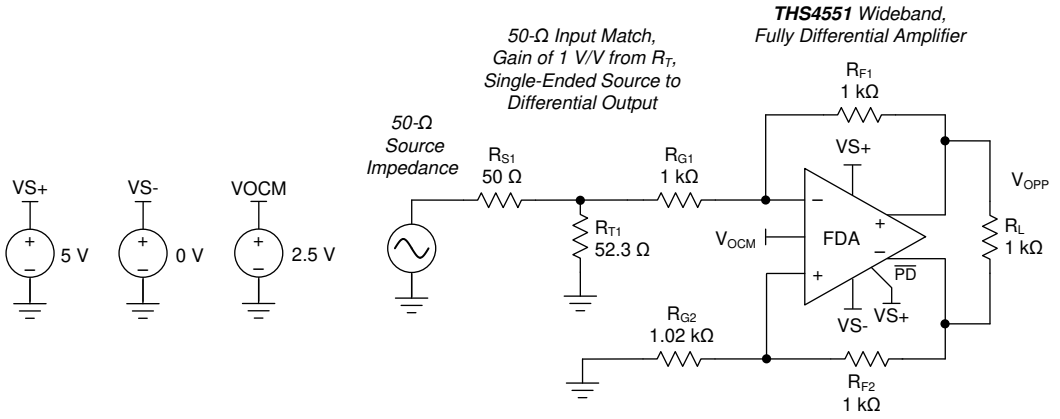

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図 9-9. DC-Coupled Gain of 1 with R_F = 1 kΩ and Single-to-Differential Matched Input 50-Ω Impedance

The standard value constraint on the non-signal input side actually produces more gain mismatch than the resistor tolerances. For 図 9-9, G2 = 1000 / 1020 = 0.9804 and G1 = 1000 / 1025.6 = 0.9751 nominally, then with a ±2% tolerance around the initial gain mismatch resulting from the standard values available if 1% resistors are used.

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Using the maximum 25°C error terms and nominal resistor values with an exact 2.5-V input to the VOCM control pin gives 表 9-2, gains to the output differential error (V_{OD}), and then the summed output error band at 25°C. The output error is clearly dominated by the V_{OCM} voltage and the effect of the nominal feedback dividers being slightly mismatched. This analysis does not include resistor tolerances but the approach is the same with the wider error bands on the gain terms. Using 1% tolerance on the resistors setting the gain matching dominates the output error band through the V_{OCM} input voltage. For the lowest output error, this analysis shows that an exact match on the feedback dividers with precision resistors is preferred. However, doing so would require duplicating the exact network on the non-signal input side and the signal input side. Where input impedance matching is not required, the two R_G resistors are simply single equal resistors and the gain mismatch is just from the tolerance of the resistors.

表 9-2. Worst-Case Output V_{OD} Error Band

ERROR TERM	25°C MAX VALUE	GAIN TO V_{OD}	OUTPUT ERROR (mV)	GAIN COMMENT
Input V_{IO}	±0.175 mV	1.9777	±0.346	Average noise gain
Input I_{OS}	±50 nA	1000	±0.05	Feedback resistor
Input I_{BCM}	1.5 µA	20 Ω	±0.03	Feedback resistor mismatch
Input I_{BCM}	1.5 µA	1 kΩ × 0.00268	±0.004	Converted to differential by gain mismatch
V_{OCM} input	2.5 V	0.00268	±6.7	V_{OCM} to differential by gain mismatch
		Total	±7.13	

The 0.00268 conversion gain for the gain ratio mismatch is the worst-case ratio starting from the initially lower G1 value resulting from the standard value constraint and using a ±1% tolerance on the R_F and R_G elements of the ratio. Adding in the resistor tolerances to the gain mismatch term greatly increases the contribution of those terms.

Normally, the expected drift in the output V_{OD} is of more interest than an initial error band. 表 9-3 shows these terms for the RGT package and the summed results by adding all terms independently to obtain a worst-case drift.

表 9-3. Worst-Case Output V_{OD} Drift Band

ERROR TERM	MAX VALUE	GAIN TO V_{OD}	OUTPUT ERROR (µV/°C)	GAIN COMMENT
Input V_{IO}	±1.8 µV/°C	1.9777	±3.56	Average noise gain
Input I_{OS}	±120 pA/°C	1000	±0.12	Feedback resistor
Input I_{BCM}	5.0 nA/°C	20 Ω	±0.10	Feedback resistor mismatch
Input I_{BCM}	5.0 nA/°C	1 kΩ × 0.00268	±0.013	Converted to differential by gain mismatch
V_{OCM} input	±10 µV/°C	0.00268	±0.027	V_{OCM} to differential by gain mismatch
		Total	±3.82	

In 表 9-3, the input offset voltage drift dominates the output drift. For the last term, the drift for the V_{OCM} path is just for the internal offset drift of the common-mode path with a driven input. Any added external drift on the source of the V_{OCM} input must also be considered. This type of calculation can be repeated for the exact application circuit considering each of these terms in the context of a specific design.

The absolute accuracy and drift for the THS4551 are exceptionally good. Mismatched resistor feedback ratios combined with a high drift in the V_{OCM} control input can actually dominate the output V_{OD} drift. Where the output differential precision is more important than the input matching accuracy, consider matching the networks on the two sides of the input to obtain improved nominal G1 to G2 match. The gains for the input bias current error terms are relatively low when using the 1-kΩ feedback values. Higher R_F values provide the input-current-related drift terms more gain.

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9.4 Device Functional Modes

The wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the $\overline{PD}$ pin asserted to a voltage greater than (V_{S-}) + 1.15 V, or turned off by asserting $\overline{PD}$ low (within 0.55 V of the negative supply). Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

Internal protection diodes remain present across the input pins in both operating and shutdown mode. Large input signals during disable can turn on the input differential protection diodes, thus producing a load current in the supply even in shutdown.

The VOCM control pin sets the output average voltage. Left open, VOCM defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor is recommended to be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias (see 図 7-45).

9.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. Although the output side is relatively straightforward, the device input pins move in a common-mode manner with the input signal. The common-mode voltage at the input pins, which moves with the input signal, increases the apparent input impedance to be greater than the R_G value. The input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as discussed in the *セクション 9.3.2*.

9.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversions

When the signal path can be ac-coupled, the dc biasing for the THS4551 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac-coupled and the output dc-coupled, or the output can be ac-coupled and the input dc-coupled, or both can be ac-coupled. One situation where the output can be dc-coupled (for an ac-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode voltage to the required ADC input common-mode voltage. In any case, the design starts by setting the desired V_{OCM}. When an ac-coupled path follows the output pins, the best linearity is achieved by operating VOCM at midsupply, which can be easily delivered by floating the VOCM pin. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.7 V greater than the negative supply and 1.3 V less than the positive supply for the full –40°C to +125°C operation). If the output path is also ac-coupled, simply letting the VOCM control pin float is usually preferred in order to obtain a midsupply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the VOCM control pin to ground.

After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} plus the positive and negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ (peak voltage) swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that $V_{OCM} \pm V_P$ does not exceed the absolute supply rails for the rail-to-rail output (RRO) device. Common-mode current does not flow from the common-mode output voltage set by the VOCM pin towards the device input pins side, because both the source and balancing resistor on the non-signal input side are dc blocked (see 図 9-5). The ac-coupled input path sets the input pin common-mode voltage equal to the output common-mode voltage.

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The input pin positive headroom requirement (1.2 V) is less than the V_{OCM} positive headroom (1.3 V). If the V_{OCM} is in range, the input pins are also in range for the ac-coupled input configuration. This headroom requirement functions similarly for when the output V_{OCM} voltage approaches the negative supply. The approximate minimum headroom of 0.6 V to the negative supply on the V_{OCM} voltage is greater than the input pin voltage headroom of approximately 0 V for the negative rail input design. The input common-mode voltage is also in range if the output common-mode voltage is in range and above 0.6 V from the negative supply because the input common-mode voltage follows the output V_{OCM} setting for ac-coupled input designs.

The input pin voltages move in a common-mode manner with the input signal, as described in *セクション 9.3.3*. Confirm that the V_{OCM} voltage plus the input V_{PP} common-mode swing also stays in range for the input pins.

9.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversions

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc-coupled when the output is ac coupled. A dc-coupled input with an ac-coupled output can have some advantages to move the input V_{ICM} down by adjusting the V_{OCM} down if the source is ground referenced. When the source is dc-coupled into the THS4551 (see 図 9-4), both sides of the input circuit must be dc-coupled to retain differential balance. Normally, the non-signal input side has an R_G element biased to whatever the source midrange is expected to be, provided that this midscale reference gives a balanced differential swing around V_{OCM} at the outputs. Often, R_{G2} is simply grounded for dc-coupled, bipolar-input applications. This configuration provides a balanced differential output if the source swings around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at VOCM (when the input is at ground) to one polarity of the swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around VOCM.

One significant consideration for a dc-coupled input is that VOCM sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_{IN} through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range. If the average source is at ground, the negative rail input stage for the THS4551 is in range for applications using a single positive supply and a positive output V_{OCM} setting because this dc common-mode current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA). TINA-TI™ simulations of the intended circuit offer a good check for input and output pin voltage swings (see 図 9-7).

9.4.2 Operation from a Differential Input to a Differential Output

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming that the two sides of the circuit are balanced with equal R_F and R_G elements, the differential input impedance is now just the sum of the two R_G elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal but must be dc biased in the design range for the input pins and must take into account the voltage headroom required to each supply. Slightly different considerations apply to ac- or dc-coupled differential input to differential output designs, as described in the following sections.

9.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

The most common way to use the THS4551 with an ac-coupled differential source is to simply couple the input into the R_G resistors through the blocking capacitors. 図 9-10 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (R_M) is included in this design. The R_M element allows the input R_G resistors to be scaled up and still delivers lower differential input impedance to the source. In this example, the R_G elements sum to show a 1-kΩ differential impedance and the R_M element combines in parallel to provide a net 500-Ω ac differential impedance to the source. Again, the design ideally proceeds by selecting the R_F element values, then the R_G to set the differential gain, and then an R_M element (if needed) to achieve a target input impedance. Alternatively, the R_M element can be eliminated, with the 2 × R_G elements set to the desired input impedance and R_F set to obtain the differential gain (equal to R_F / R_G).

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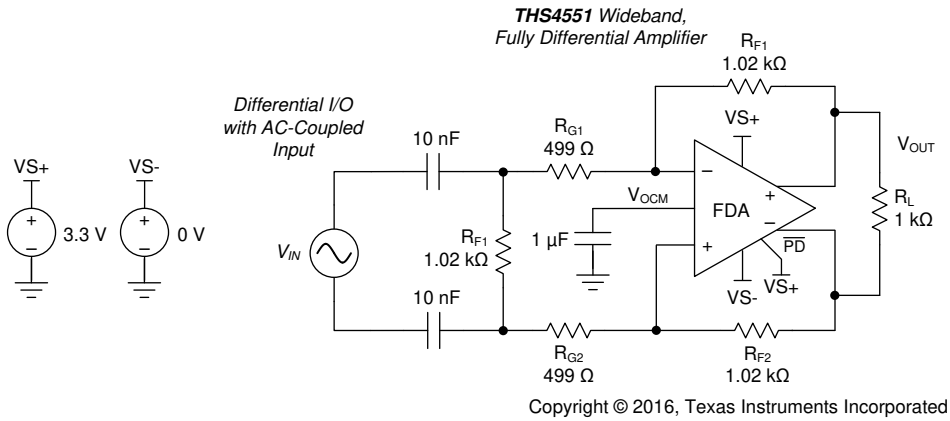

図 9-10. Example AC-Coupled Differential Input Design

The dc biasing for an ac-coupled differential input design is very simple. The output V_{OCM} is set by the input control voltage and, because there is no dc current path for the output common-mode voltage (as long as R_M is only differential and not split and connected to ground for instance), the dc bias also sets the common-mode operating points for the input pins. For a purely differential input, the voltages on the input pins remain fixed at the output V_{OCM} setting and do not move with the input signal (unlike the single-ended input configurations where the input pin common-mode voltages do move with the input signal). The SLOC341 TINA-TI™ simulation file is available for 図 9-10.

9.4.2.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the THS4551 with a dc-coupled differential input source is very simple and only requires that the input pins stay in range for the dc common-mode operating voltage. The example in 図 9-11 takes the output of a dual precision op amp (such as the OPA2192) where a high differential input signal is attenuated by the THS4551 down into the range of an 18-bit SAR ADC such as the 2-MSPS ADS9110. The input stage provides a differential gain of 21 V/V with a common-mode gain of 1 V/V. This example amplifies a small differential signal on top of a very-wide range common-mode voltage. The input common-mode voltage appears at the outputs of the OPA2192. The input common-mode voltage is level shifted by the FDA common-mode control to be at the required output common-mode voltage to drive the ADS9110 SAR ADC (with a 4.096-V reference, as shown in 図 9-11); the FDA output common-mode voltage must be at the 2.048 V shown in 図 9-11. This design offers a very high CMRR using the common-mode control loop of the FDA to reset the output common-mode voltage from that delivered to the inputs of the OPA2192. The actual CMRR from the OPA2192 inputs to the FDA outputs is dominated by the resistor mismatches in the FDA. The feedback and differential input capacitors are included to shape the noise gain as described in *セクション 10.1.6*. This full example circuit is available as a TINA-TI™ simulation file.

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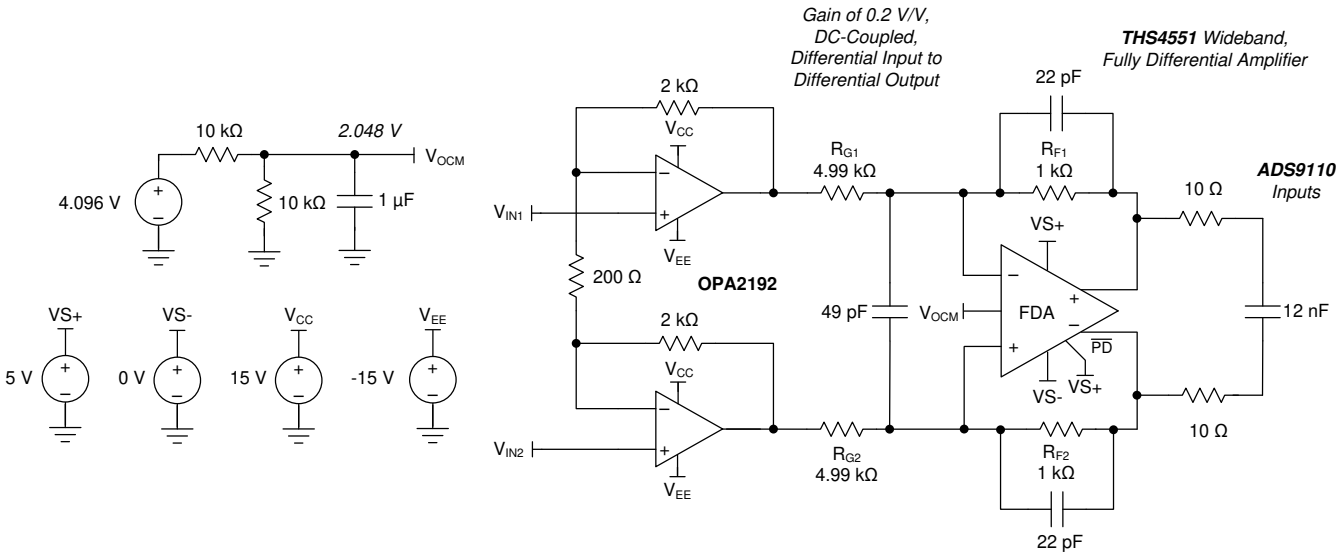

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図 9-11. Example DC-Coupled Differential I/O Design from a Precision Dual Op Amp to an 18-Bit SAR

9.4.3 Input Overdrive Performance

図 7-12 illustrates a 2X overdrive triangle waveform for the THS4551. The input resistor is driven with a ±9-V swing for the gain of 2-V/V configuration in the test circuit of 図 8-1 using a single 5-V supply. When the output maximum swing is reached at approximately the supply values, the increasing input voltage turns on the internal protection diodes across the two input pins. The internal protection diodes are two diodes in series in both polarities. This feature clamps the maximum differential voltage across the inputs to approximately 1.5 V when the output is limited at the supplies but the input exceeds the available range. The input resistors on both sides limit the current flow in the internal diodes under these conditions.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

Most applications for the THS4551 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier itself. The following sections detail some of the design issues with analysis and guidelines for improved performance.

10.1.1 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. 図 10-1 shows the simplest analysis circuit with the FDA and resistor noise terms to be considered.

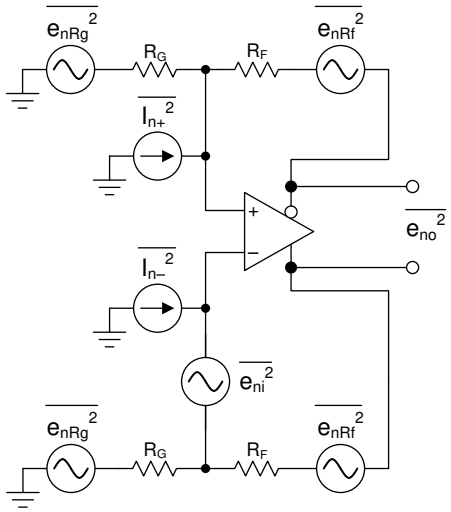

図 10-1. FDA Noise Analysis Circuit

The noise powers are shown in 図 10-1 for each term. When the R_F and R_G (or R_I) terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms. Using NG ≡ 1 + R_F / R_G, the total output noise is given by 式 10. Each resistor noise term is a 4kT × R power (4kT = 1.6E-20J at 290K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_F NG)} \tag{10}$$

The first term is simply the differential input spot noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together. Running a wide sweep of gains when holding R_F close to 1 kΩ and setting the input up for a 50-Ω match gives the standard values and resulting noise listed in 表 10-1.

Note that when the gain increases, the input-referred noise approaches only the gain of the FDA input voltage noise term at 3.3 nV/√ Hz.

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表 10-1. Swept Gain of the Output- and Input-Referred Spot Noise Calculations

GAIN (V/V)	R_F	R_{G1}	R_T	R_{G2}	Z_{IN}	A_V	E_O (nV/√Hz)	E_I (nV/√Hz)
0.1	1000	10000	49.9	10000	49.66	0.09965	7	70
1	1000	976	51.1	1000	49.2	1.0096	10.4	10.4
2	1020	499	52.3	523	48.9	1.988	13.9	6.95
5	1000	187	59	215	50.2	5.057	23	4.6
10	1020	88.7	69.8	118	50.6	10.09	36.4	3.64

10.1.2 Factors Influencing Harmonic Distortion

As illustrated in the swept frequency harmonic distortion plots (図 7-13 and 図 7-31), the THS4551 provides extremely low distortion at lower frequencies. In general, an FDA output harmonic distortion mainly relates to the open-loop linearity in the output stage corrected by the loop gain at the fundamental frequency. When the total load impedance decreases, including the effect of the feedback resistor elements in parallel for loading purposes, the output stage open-loop linearity degrades, thus increasing the harmonic distortion; see 図 7-16 and 図 7-34. When the output voltage swings increase, very fine scale open-loop output stage nonlinearities increase that also degrade the harmonic distortion; see 図 7-14 and 図 7-32. Conversely, decreasing the target output voltage swings drops the distortion terms rapidly. A nominal swing of 2 V_{PP} is used for harmonic distortion testing where 図 7-14 illustrates the effect of going up to an 8-V_{PP} differential input that is more common with SAR converters.

Increasing the noise gain functions to decrease the loop gain resulting in the increasing harmonic distortion terms; see 図 7-18 and 図 7-36. One advantage to the capacitive compensation for the attenuator designs is that the noise gain is shaped up with frequency to achieve a crossover at an acceptable phase margin at higher frequencies. This technique (see *セクション 10.1.6*) holds the loop gain high at frequencies lower than the noise gain zero, thus improving distortion at lower frequencies.

The THS4551 holds nearly constant distortion when the V_{OCM} operating point is moved in the allowed range; see 図 7-17 and 図 7-35. Clipping into the supplies with any combination of V_{OCM} and V_{OPP} rapidly degrades distortion performance.

The THS4551 does an exceptional job of converting from single-ended inputs to differential outputs with very low harmonic distortions. External resistors of 1% tolerance are used in characterization with good results. Unbalancing the feedback divider ratios does not degrade distortion directly. Imbalanced feedback ratios convert common-mode inputs to a differential mode at the outputs with the gain described in *セクション 9.3.4*.

10.1.3 Driving Capacitive Loads

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. Directly connecting a capacitive load to the output pins of a closed-loop amplifier such as the THS4551 can lead to an unstable response; see the step response plots into a capacitive load (図 7-8, 図 7-10, 図 7-26, and 図 7-28). One typical remedy to this instability is to add two small series resistors (R_O) at the outputs of the THS4551 before the capacitive load. 図 7-6 and 図 7-24 illustrate parametric plots of recommended R_O values versus differential capacitor load values and gains. Operating at higher noise gains requires lower R_O values to obtain a ±0.5-dB flat response for the same capacitive load. Some direct parasitic loading is acceptable without a series R_O that increases with gain setting (see 図 7-8, 図 7-10, 図 7-26, and 図 7-28 where the R_O value is 0 Ω). Even when these plots suggest that a series R_O is not required, good practice is to leave a place for the R_O elements in a board layout (a 0-Ω value initially) for later adjustment in case the response appears unacceptable.

The rail-to-rail output stage of the THS4551 has an inductive characteristic in the open-loop output impedance at higher frequencies; see 図 9-3. This inductive open-loop output impedance introduces added phase shift at the output pins for direct capacitive loads and feedback capacitors. Larger values of feedback capacitors (greater than 100 pF) can risk a low phase margin. Including a 10-Ω to 15-Ω series resistor with a feedback capacitor can be used to reduce this effect.

The TINA-TI™ simulation model does a good job of predicting these issues and illustrating the effect for different choices of capacitive load isolating resistors (R_O) and different feedback capacitor configurations.

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10.1.4 Interfacing to High-Performance Precision ADCs

The THS4551 provides a simple interface to a wide variety of precision SAR and delta-sigma (ΔΣ) ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than what is typically required in the signal path to the ADC inputs is provided by the THS4551. This wide amplifier bandwidth provides the low broadband, closed-loop output impedance to supply the sampling glitches and to recover quickly for the best SFDR. A particularly challenging task is to drive the high-frequency modulator sample rates for a precision ΔΣ converter where the modulator frequency can be far higher than the final output data rate. 図 10-2 shows a tested example circuit using the THS4551 in a 500-kHz, active multiple feedback (MFB) filter driving the 24-bit ADS127L01. This filter is designed for F_O = 500 kHz and Q = 0.63 to give a linear phase response with the –3-dB frequency at 443 kHz. This example circuit is available as a TINA-TI™ simulation file.

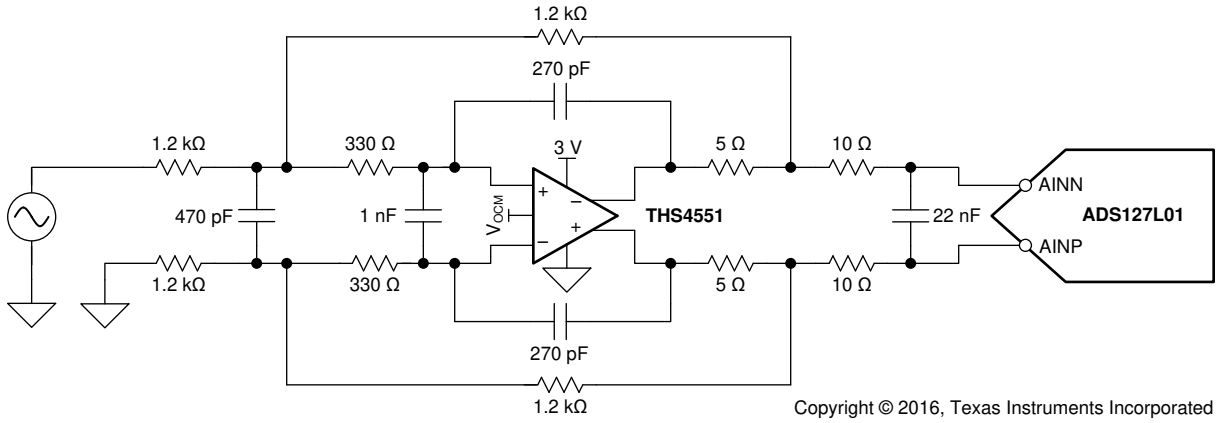

図 10-2. 500-kHz Low-Pass Active Filter

This 3-V supply example provides a low-power interface to the very low-power ADC. This circuit is available on the ADS127L01EVM board.

The 5-Ω resistors inside the loop at the output pins and the 1-nF differential capacitor across the FDA input pins are not part of the filter design. These elements function to improve the loop-phase margin with minimal interaction with the active filter operation To observe the loop gain and phase margin, use the SBOC461 TINA-TI ™ simulation file. Tested performance with the ADS127L01 at a 4-kHz input shows the exceptional THD and SNR of –114 dBc and 106 dB, respectively. 図 10-3 uses the ADS127L01 at a modulator frequency of 16 MHz.

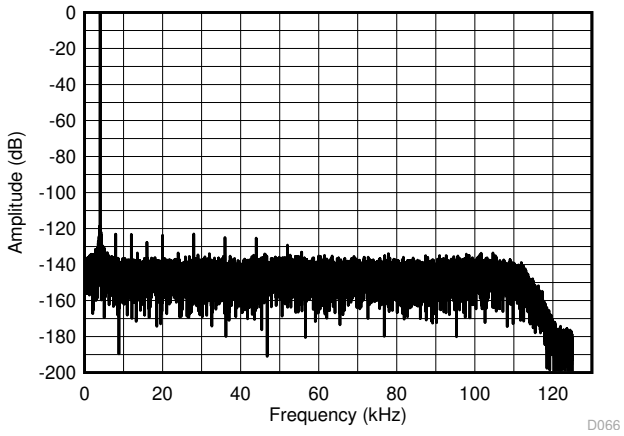

図 10-3. 4-kHz FFT Test for the Gain of 1 V/V Interface in 図 10-2

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10.1.5 Operating the Power Shutdown Feature

The CMOS input pin must be asserted to the desired voltage for operation. An internal pullup resistor is not provided on the $\overline{PD}$ pin so that off-state quiescent current can be minimized. For applications simply requiring the device to be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

The disable operation is referenced from the negative supply, normally ground. For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the THS4551 off. To assure an off state condition, the disable control pin must be below a voltage within 0.55 V of the negative supply.

For single-supply operation, a minimum of 1.15 V above the negative supply (ground in this case) is required to assure on operation. This logic threshold range allows direct operation from a 1.8-V supply logic when the THS4551 operates with a single positive supply and ground.

10.1.6 Designing Attenuators

Operating the THS4551 at a low-noise gain (or with higher feedback resistors) can cause a lower phase margin to exist, thus giving the response peaking illustrated in 図 7-1 for the gain of a 0.1 (a 1/10 attenuator) condition. Although operating the THS4551 as an attenuator is often useful, taking a large input range to a controlled output common-mode voltage with a purely differential signal around the V_{OCM} voltage, the response peaking illustrated in 図 7-1 is usually undesirable. Several approaches can be used to reduce or eliminate this peaking, usually at the cost of higher output noise. DC attenuation at the input usually increases the output noise broadband, whereas using an ac noise gain shaping technique that peaks the noise gain only at higher frequencies is more desirable. This peaking output noise can then be filtered off with the typical passive RC filters often used after this stage. 図 10-4 shows a simplified schematic for the gain of 0.1-V/V test from 図 7-1.

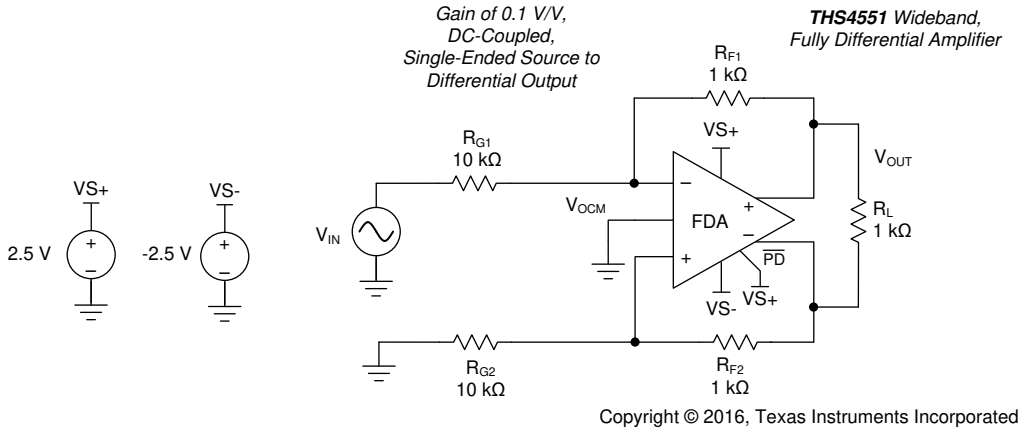

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図 10-4. Divide-by-10 Attenuator Application for the THS4551

A 5-dB peaked response (see 図 10-6) results from the configuration of 図 10-4, which results from a nominal 32° phase margin. This peaking can be eliminated by placing two feedback capacitors across the R_F elements and a differential input capacitor. Adding these capacitors provides a transition from a resistively set noise gain (NG1 = 1.1 in 図 10-4) to a capacitive divider at high frequency, and flattening out to a higher noise gain (NG2). The key for this approach is to target a Z_O where the noise gain begins to peak up. Using only the following terms, and targeting a closed-loop flat (Butterworth) response, gives this solution sequence (from 式 11 to 式 13) for Z_O and then the capacitor values. See the OPA847 data sheet (page 12) for a discussion of this inverting noise gain shaping technique.

- Gain bandwidth product in Hz (135 MHz for the THS4551)
- Low-frequency noise gain, NG1 (equal to 1.1 in the attenuator gain of a 0.1-V/V design)
- The target high-frequency noise gain is selected to be higher than NG1 (NG2 = 5 V/V) in this example
- Feedback resistor value, R_F (is assumed balanced for this differential design = 1 kΩ)

From these elements, for any voltage feedback op amp or FDA, solve for Z_O as shown in 式 11:

$$Z_O = \frac{GBP}{NG1^2}\left(1 - \frac{NG1}{NG2} - \sqrt{1 - 2\frac{NG1}{NG2}}\right) \quad (11)$$

From this target zero frequency in the noise gain, the feedback capacitors can be solved as 式 12:

$$C_F = \frac{1}{2\pi \bullet R_F \bullet Z_O \bullet NG2} \quad (12)$$

The next step is to resolve the input capacitance on the summing junction. 式 13 is for a single-ended op amp where the capacitor goes to ground. To use the capacitance (C_S) resulting from 式 13 for a voltage-feedback FDA, cut the target value in half and place the resulting C_S across the two inputs (reducing the external value by the specified internal differential capacitance).

$$C_S = (NG2 - 1)C_F \quad (13)$$

Using the computed capacitor values allows for an estimate of the resulting flat response bandwidth f_{-3dB} frequency, as shown in 式 14:

$$f_{-3dB} \approx \sqrt{GBP \bullet Z_O} \quad (14)$$

Running through these steps for the THS4551 in the attenuator circuit of 図 10-4 provides the proposed compensation of 図 10-5, where 式 14 estimates a bandwidth of 22 MHz (the Z_O target is 3.5 MHz). The solutions for C_F gives 9 pF, where this value is reduced to 8.4 pF to account for the internal 0.6-pF feedback. The single-ended solution for C_S gives 36 pF, which is reduced to 18 pF to be differential, and is then further reduced to 16.8 pF to account for the internal 1.2-pF differential input capacitance of the THS4551.

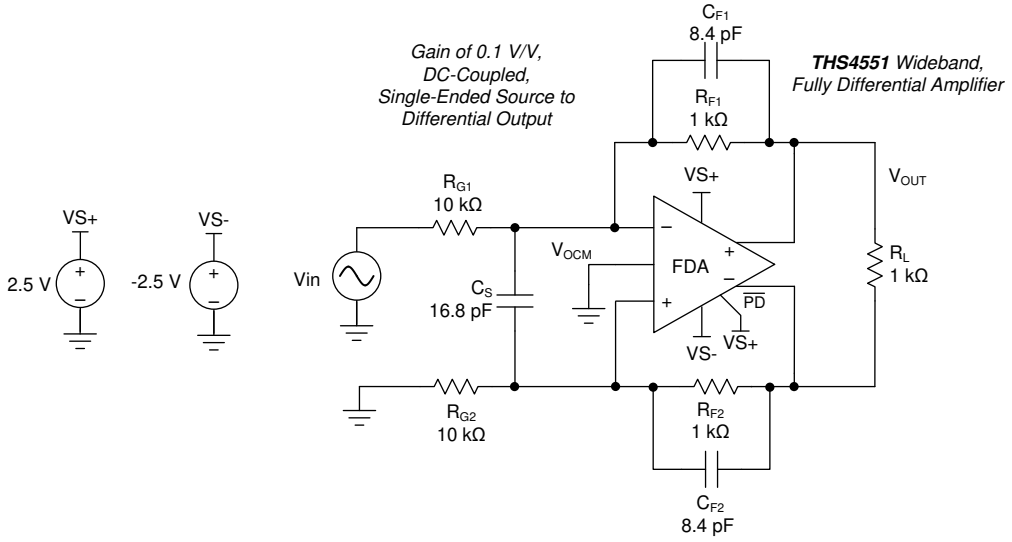

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図 10-5. Compensated Attenuator Circuit Using the THS4551

The 16.8 pF across the inputs is really a total of 36 pF for a single-ended design from 式 13 reduced by half and then the 1.2-pF internal capacitance is removed.

These two designs (with and without the compensation capacitors) were both bench tested and simulated using the THS4551 TINA-TI™ model, which resulted in 図 10-6. The TINA-TI™ simulation files used for 図 10-6 are available both without the compensation capacitors and with the capacitors in place.

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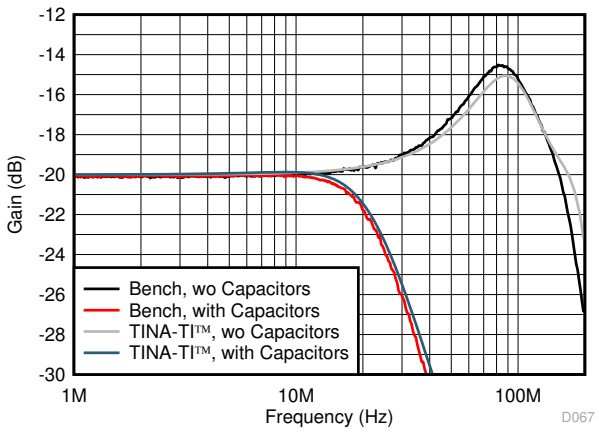

図 10-6. Attenuator Response Shapes With and Without External Capacitors

This approach does a good job of flattening the response for what starts out as a low phase margin attenuator application. The simulation model does a very good job of predicting the peaking and showing the same improvement with the external capacitors (both give a flat, approximately 24-MHz, closed-loop bandwidth for the gain of 0.1-V/V design). The output noise starts to peak up (because of the noise gain shaping of the capacitors) above 3.5 MHz in this example. These stages normally drive the RC filter at the input of a SAR ADC that filters off the noise peaking above 3.5 MHz.

10.1.7 The Effect of Adding a Feedback Capacitor

Adding a feedback capacitor to band-limit the signal path is very common in lower frequency designs. This approach is very effective for the signal path gain but does create the potential for high-frequency peaking and oscillation for a wideband device such as the THS4551. The feedback capacitor by itself takes the noise gain to 1 V/V at high frequencies. Depending on the frequency where the noise gain goes to 1V/V, and what added phase margin reduction may already be in place resulting from the load RC, the feedback capacitors can cause instability.

図 10-7 shows the starting point for a typical band-limited design. At lower frequencies, this example delivers a gain of 10 V/V with an intentional band limit in the feedback RC at 320 kHz. This single 5-V design targets a midsupply output common-mode voltage with only a noise reduction capacitor on the V_{OCM} input control.

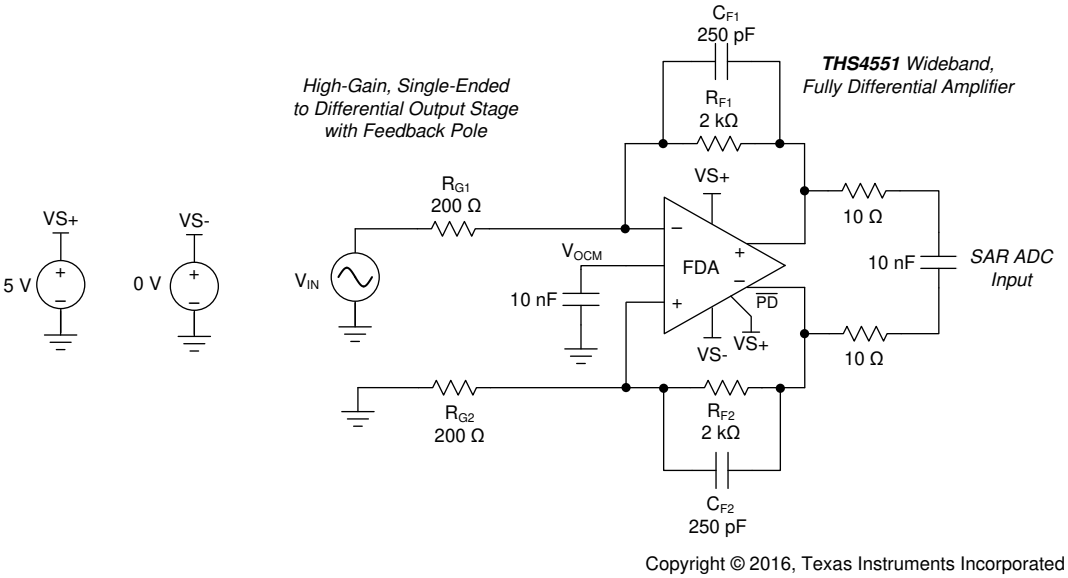

図 10-7. Single-Ended to Differential Stage with a Feedback Pole

The response shape must be probed at the FDA output pins before the added RC pole to the SAR input. Running a wideband sweep with the THS4551 TINA-TI™ model using the SBOC475 simulation file shows a resonance at 50 MHz in 図 10-8 resulting from the feedback capacitor.

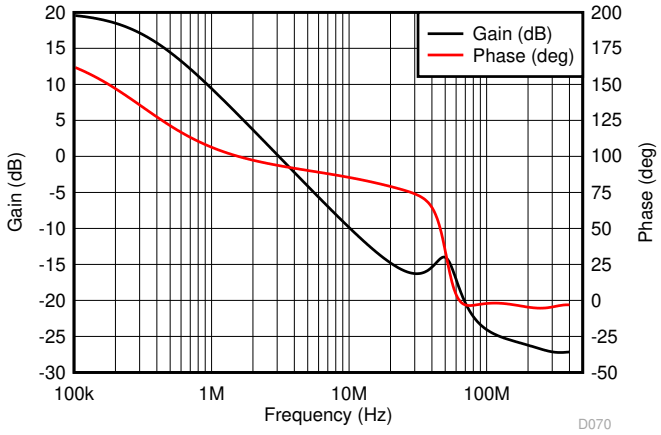

図 10-8. Gain and Phase Plot with a Feedback Pole

One approach to increasing the phase margin when there is a feedback capacitor is to include a differential input capacitor. This approach increases the noise gain at higher frequencies, thus creating a lower-frequency loop gain equal to a 0-dB crossover with more phase margin. 図 10-9 shows a differential input capacitor equal to the feedback capacitor in the test circuit. This approach increases the noise gain from 1 V/V at higher frequencies (with only a feedback capacitor) to a noise gain of 3 V/V at higher frequencies.

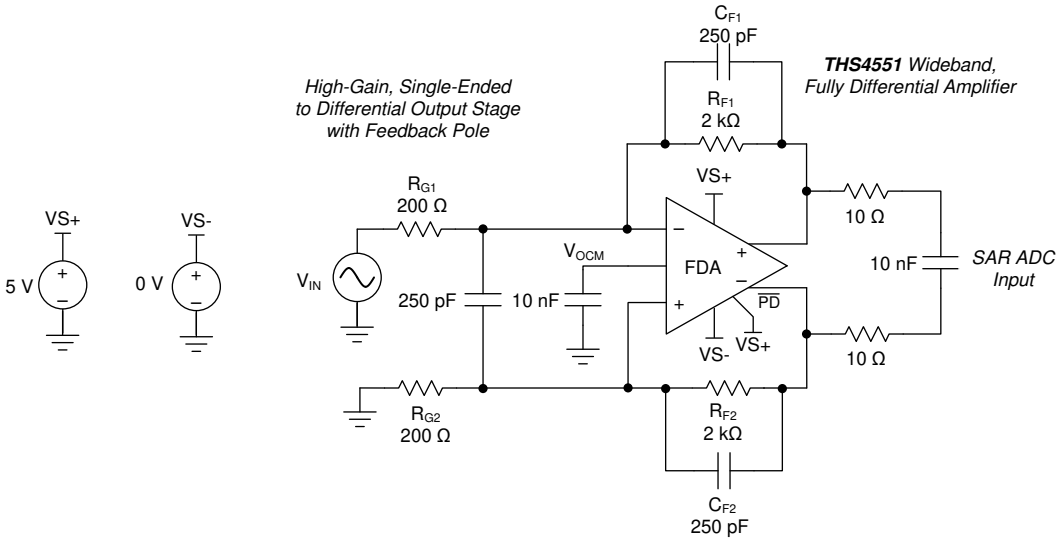

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図 10-9. Single-Ended to Differential Stage with a Feedback Pole and Differential Input Capacitor

Re-running the wideband response (using the SBOC474 TINA-TI™ simulation file) simulation illustrates in 図 10-10 that the resonance is greatly reduced with the higher noise gain at the loop gain equal to a 0-dB crossover at a lower frequency. Although this example is only modestly peaking, good design practice is to include a place for a differential input capacitor (even if not used) for any design using a feedback capacitor across the feedback resistors. This recommendation applies to this simple example and to multiple feedback active filter designs.

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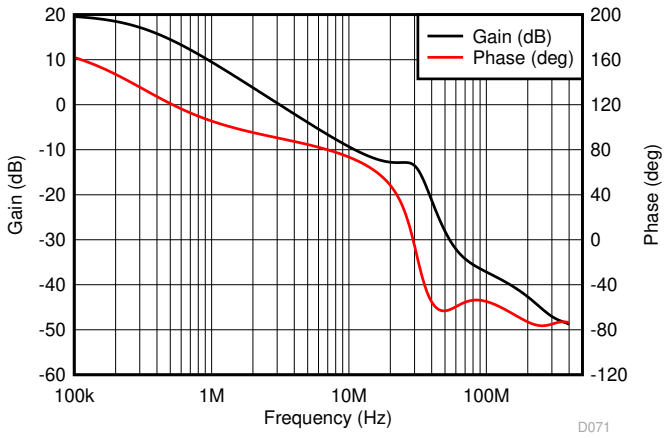

図 10-10. Gain and Phase Plot with a Differential Input Capacitor

10.2 Typical Applications

10.2.1 An MFB Filter Driving an ADC Application

One common application for the THS4551 is to take a single-ended, high V_{PP} voltage swing (from a high-voltage precision amplifier such as the OPA192) and deliver that swing to precision SAR ADC as a single-ended to differential conversion with output common-mode control and implement an active 2nd-order multiple feedback (MFB) filter design. Designing for a 40-V_{PP} maximum input down to an 8-V_{PP} differential swing requires a gain of 0.2 V/V. Targeting a 100-kHz Butterworth response with the RC elements tilted towards low noise gives the example design of 図 10-11. Note that the V_{CM} control is set to half of a 4.096-V reference, which is typical for 5-V differential SAR applications.

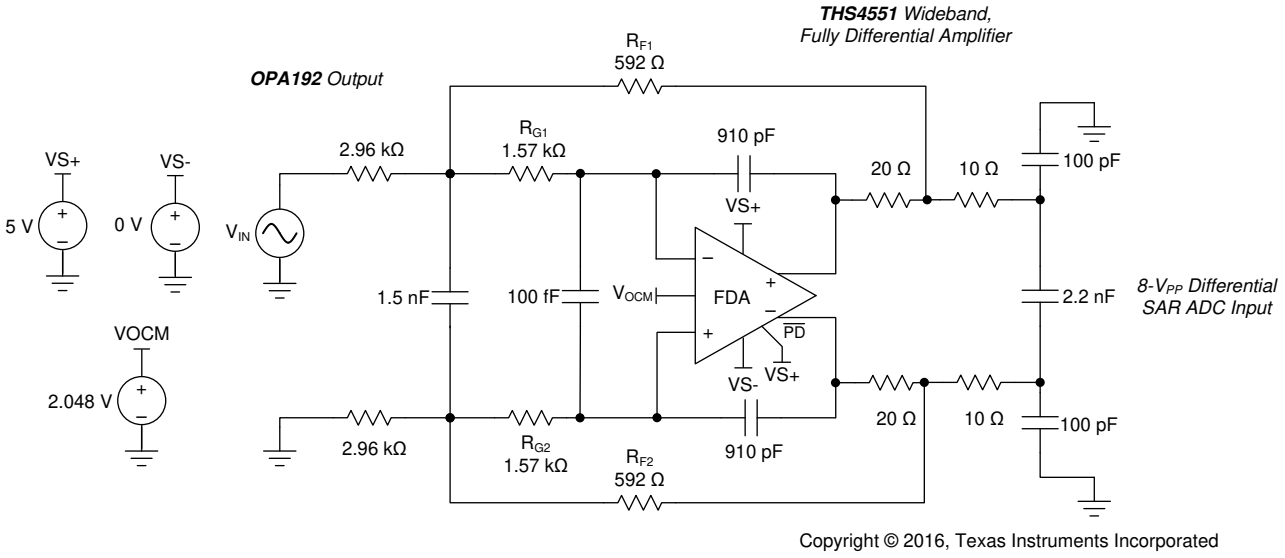

図 10-11. Example 100-kHz Butterworth Filter

10.2.1.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- Attenuation by 0.2-V/V gain
- Active filter set to a Butterworth, 100-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the THS4551 and noise peaking

10.2.1.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note (SBOA114). The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the THS4551 by itself
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design
- Set the output resistor to 10 Ω into a 2.2-nF differential capacitor
- Add 100-pF common-mode capacitors to the load capacitor to improve common noise filtering
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor
- Include a place for a differential input capacitor (illustrated as 100 fF in 図 10-11)

10.2.1.3 Application Curves

Probing the response to the output pins by using the THS4551 SBOC471 TINA-TI™ simulation model (before the RC filter to the SAR ADC) illustrates the expected response plus some peaking at higher frequencies. Any signal or noise peaking that appears at the output because of this peaking is rolled off by the RC filter between the FDA and SAR inputs. A place for a differential input capacitor is illustrated in 図 10-11 (as 0.1 pF) but is not used for this simulation. This slight peaking is a combination of low phase margin and feedthrough via the feedback capacitor to the increasing open-loop output impedance of 図 9-3. The loop gain and phase response are available as a TINA-TI™ simulation file.

Obtaining the SNR to the ADC input pins, and assuming an 8-V_{PP} full scale (2.83 V_{RMS}), gives the result of 図 10-13. The 113-dB SNR shown in 図 10-13 does not limit the performance for any SAR application.

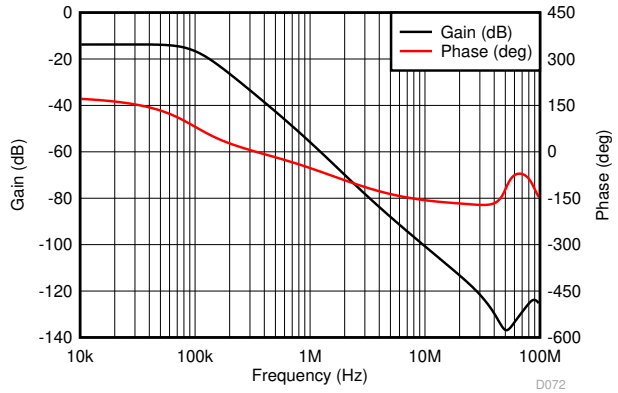

図 10-12. Gain and Phase Plot for a 100-kHz Butterworth Filter

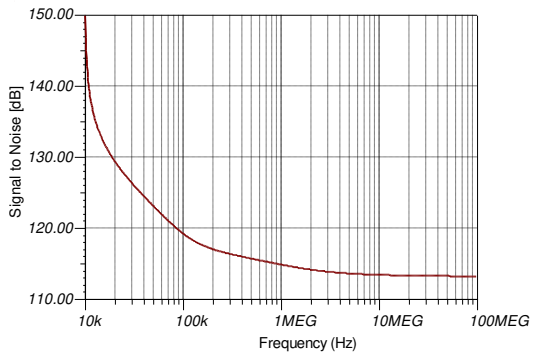

図 10-13. Signal-to-Noise Ratio Plot

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10.2.2 Differential Transimpedance Output to a High-Grade Audio PCM DAC Application

The highest-grade audio digital-to-analog converters (DACs) are a differential current-mode output. These devices normally suggest a two-amplifier transimpedance stage to hold the DAC output voltages fixed when the amplifiers produce a differential voltage swing at the outputs. Often, the differential voltage swing is then converted to single-ended in a differencing amplifier stage to drive headphone loads (see Figure 35 in the OPA1611). The emerging high-power class D audio amplifiers often require differential inputs. Applying the THS4551 as a differential transimpedance stage offers a simple solution for very low-distortion, differential-output audio channels.

Starting with the output specifications for a very high-performance PCM1792A audio DAC, the requirements for the THS4551 interface can be extracted. The DAC is a current-sourcing device that requires its outputs to be held at ground when using a transimpedance amplifier. Using the DAC 3.3-V supply and the LM27762 low-noise, low-dropout (LDO) regulator and inverter provides a ±2.5-V supply to the THS4551. Operating the THS4551 on ±2.5-V supplies places all nodes in range for an input V_{CM} equal to GND (and the DAC output voltages as well) and an FDA output V_{OCM} also equal to GND.

The center current in 表 10-2 is a fixed 6.2-mA dc current coming out of the DAC outputs regardless of the DAC code. This dc common-mode current can be absorbed by the –2.5-V supply at the input pins to hold the DAC compliance voltage and FDA input pins at ground. The FDA controls the output common-mode voltage, set to ground in this case, whereas the input pin voltage (which does not move with the DAC output differential current) is controlled with a resistor to the negative supply.

表 10-2. PCM1792A Analog Output Specification

ANALOG OUTPUT	TEST CONDITION	MIN	TYP	MAX	UNIT
Gain error		–6	±2	6	% of FSR
Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
Bipolar zero (BPZ) error	At BPZ	–2	±0.5	2	% of FSR
Output current	Full-scale (0 dB)		7.8		mA_{PP}
Center current	At BPZ		–6.2		mA

This bias is provided by the 402-Ω resistors to –2.5 V, as illustrated in 図 10-14. This design takes the differential 7.8 mA_{PP} from the DAC and produces a ±1.46-V swing on each output of the THS4551. This configuration gives a full-scale differential 5.85 V_{PP} available on the ±2.5-V supply design centered at ground at both the inputs and outputs. Although the LM27762 provides a very-low noise, –2.5-V supply, using 0.1% resistors in the current sink path to the –2.5-V supply as well as the feedback resistors limits any common-mode noise on the –2.5-V supply to differential mode conversion at the FDA outputs.

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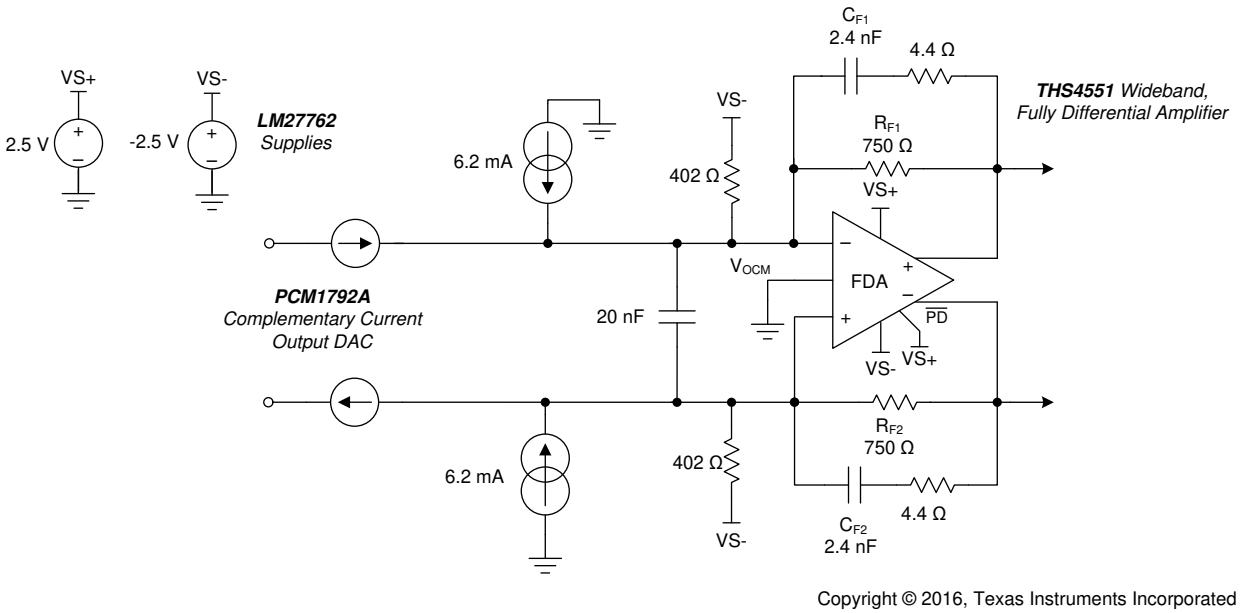

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図 10-14. PCM1792A DAC Output Driver

10.2.2.1 Design Requirements

To implement a differential transimpedance output interface to the PCM1792A DAC, the following requirements must be met:

- The center current of the DAC must be considered to hold the DAC output voltage at ground. Using an FDA controls the output side common-mode voltage, but the input common-mode voltage must also be controlled to ground.
- A direct means of sinking the center current is to add a pulldown resistor at the DAC outputs to a negative supply. Generating a ±2.5-V supply for this current sink requirement and the THS4551 is accomplished with the LM27762.
- The transimpedance gain can be set using the feedback resistors of the THS4551 FDA. These resistors are very flexible, but when set, the bandwidth in this stage is set to 88 kHz using a feedback capacitor in parallel with the resistive gain element.
- When the feedback capacitor is set, a differential input capacitor is added to increase the high-frequency noise gain for the overall loop gain stability.
- These frequency response control capacitors interact with the inductive open-loop output impedance to form a high-frequency resonance. Adding a small series resistor to the feedback capacitor paths reduces this effect.

10.2.2.2 Detailed Design Procedure

Proceed with this design using the techniques described in the *Design for Wideband Differential Transimpedance DAC Output* application note (SBAA150):

- Generate the bipolar balanced supplies using the LM27662.
- Set the THS4551 output common-mode voltage at midsupply by grounding the VOCM pin.
- Control the input pin operating voltage by sinking the center current out of the DAC to the –2.5-V supply with precision 402-Ω resistors.
- Set the gain for the complementary current output signal from the DAC by selecting the feedback resistor to be 750 Ω. Set this resistor to keep the resulting output swing to be less than the available 9-V_{PP} differential swing.
- Control the bandwidth in this differential transimpedance stage to 88 kHz using the 2.4-nF feedback capacitor on each side.
- Increase the high-frequency noise gain to 17.7 V/V by adding a differential input capacitor of 20 nF.
- Isolate these feedback capacitors with a series 4.4-Ω resistor in series with the feedback capacitors.

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10.2.2.3 Application Curves

The bandwidth is controlled to 88 kHz by using the 2.4-nF feedback capacitors. Amplifier stability is controlled by the 20-nF differential capacitor across the DAC outputs. The added 4.4 Ω in series with the feedback 2.2-nF capacitor isolates this capacitance from the inductive open-loop output impedance. To observe the effect of adding these small resistors in series with the feedback capacitors, use the TINA-TI™ loop gain simulation circuit. Include the DAC source capacitance in any final design analysis. Running the frequency response for this circuit (available as a TINA-TI™ simulation file) provides this result. The 63.5-dBΩ gain is the 1.5-kΩ transimpedance gain provided in this design.

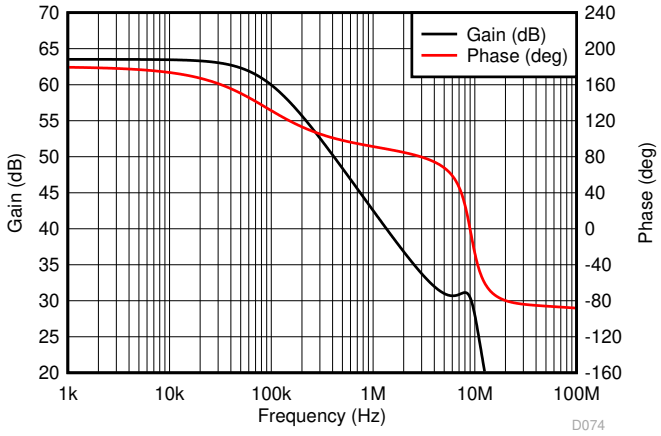

図 10-15. Gain and Phase Plot of DAC Output Driver

Running a full-scale sine wave at 1 kHz with ±1.95 mA on each output from the DAC at 180° out of phase, and probing each THS4551 output pin separately results in the expected ±1.46 V on each output pin, as shown in 図 10-16. More output swing is available for the RRO device using the ±2.5-V supplies provided by the LM27762 by simply increasing the feedback resistor values.

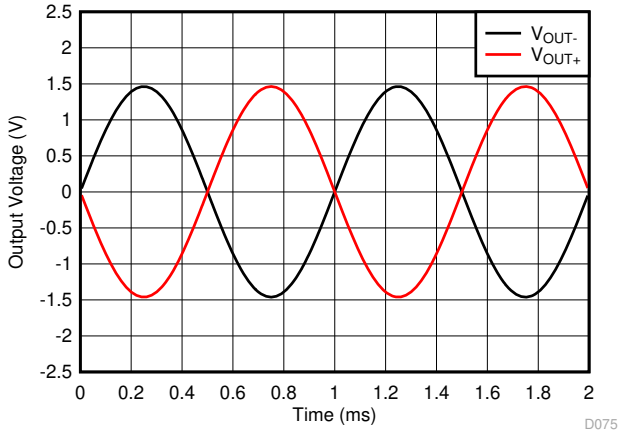

図 10-16. Output Waveform of the DAC Output Driver

Although this example is on the audio signal generation side, the THS4551 can also be used to convert a single-ended line input to a differential driver into an audio ADC.

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10.2.3 ADC3k Driver with a 2nd-Order RLC Interstage Filter Application

The THS4551 is well suited to low-power, dc-coupled requirements driving low-power pipeline ADCs (such as the ADC3241 25-MSPS, 14-bit, dual device). 図 10-17 shows an example design taking a bipolar input to a –1-dBFS swing at the ADC input of 1.8 V_{PP}. In this case, a 50-Ω source and input matching is assumed with a gain of 5 V/V to the output pins with a 2nd-order interstage filter adding a –1-dB insertion loss. Full-scale voltage at the input of R_T and R_{G1} is then ±0.2 V. The 0.95-V output common-mode voltage is provided by the ADC. The output filter provides a noise-power bandwidth limit with a low overshoot step response with no common-mode level shift from the 0.95-V voltage provided by the ADC.

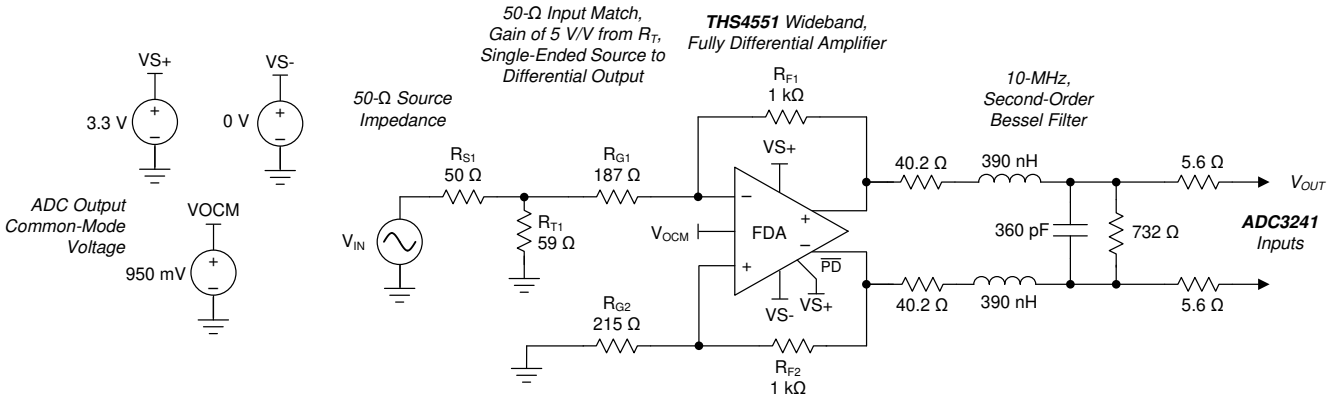

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図 10-17. ADC3k Driver with a 2nd-Order RLC Interstage Filter

10.2.3.1 Design Requirements

For this design example, the requirements include:

- Provide a wideband, 50-Ω input impedance match for a single-ended source centered on ground.
- From the input termination, provide a gain of 5 V/V to the FDA output pins as a differential signal.
- Set the output common-mode operating point using the ADC common-mode output voltage as the VOCM input to the THS4551 FDA.
- Implement a low-overshoot, noise-band-limiting filter between the FDA and the ADC. Use only differential shunt elements in the filter to pass the FDA output common-mode voltage to the ADC with no level shifting.
- Design the filter as a –1-dB insertion loss filter with a low series resistor to limit the common-mode level shift resulting from the ADC input sample-rate-dependent common-mode current.

10.2.3.2 Detailed Design Procedure

The design proceeds as follows:

- Select the feedback resistor to be 1 kΩ and use the values from 表 9-1 at a gain of 5 V/V to implement a 50-Ω input match with a gain of 5 V/V.
- Use a 3.3-V power supply and apply the ADC output common-mode voltage to the VOCM input pin of the THS4551.
- Design a –1-dB insertion loss, 2nd-order RLC filter using the approach described in the *RLC Filter Design for ADC Interface Applications* application note (SBAA108).
- Adjust the total resistive load target in the filter design to hit the standard value for the filter inductors.
- Convert the filter design to differential with only differential shunt elements. These elements must not be split and connected to a center-point ground. This technique passes the output common-mode voltage from the FDA to the ADC with no level shift error.
- Add a small series resistor at the ADC inputs. This resistor is not part of the filter design but spreads out the sampling glitch energy to provide improved SFDR.
- Check the common-mode level shift from the FDA outputs to the ADC resulting from the clock-rate-dependent common-mode current. This common-mode current into the ADC shifts the common-mode voltage slightly, but can easily stay in range with a low series resistor in the filter design.

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10.2.3.3 Application Curve

Driving a 2-MHz ±0.2-V square wave into this circuit (using a TINA-TI™ simulation file for the circuit of 図 10-17) gives the response shown in 図 10-18 at the ADC. The red trace is a –1-dBFS, 1.8-V_{PP} square wave at the ADC input pins. The gray trace is the input signal at the R_T termination resistor. The black trace is the common-mode voltage at the FDA input pins. Note that the input pin voltage swing stays above ground and in range for this bipolar input, single, 3.3-V supply design.

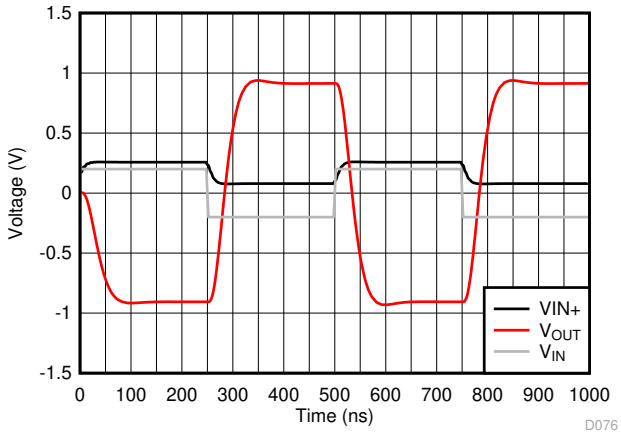

図 10-18. Time-Domain Waveform

Unbuffered pipeline ADCs draw a clock-rate-dependent input common-mode current. For the ADC3241, this input current is specified as 1.5 µA per MSPS. Operating at 25 MSPS, the common-mode current drops the common-mode voltage from 0.95 V at the THS4551 outputs by 37.5 µA × 45.8 Ω = 1.7 mV to 0.9483 V. This value is well within the allowed ±25-mV common-mode deviation from the ADC V_{CM} output. Consider this effect carefully when using higher resistor values in the interface at the ADC.

11 Power Supply Recommendations

The THS4551 is principally intended to operate with a nominal single-supply voltage of 3 V to 5 V. Supply voltage tolerances are supported with the specified operating range of 2.7 V (10% low on a 3-V nominal supply) and 5.4 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in *セクション 8.7*. Split (or bipolar) supplies can be used with the THS4551, as long as the total value across the device remains less than 5.5 V (absolute maximum). The thermal pad on the RGT package is electrically isolated form the die; connect the thermal pad (RGT package only) to any power or ground plane for reduced thermal impedance to the junction temperature. This pad must be connected to some power or ground plane and not floated.

For the best input offset voltage drift, the THS4551 uses a proportional to absolute temperature (PTAT) quiescent current biasing scheme. This approach gives a positive over temperature variation in supply current. 図 11-1 shows the 5-V supply current over a wide T_J range for a number of tested units. The *Electrical Characteristics* tables report the typical and range on this supply current temperature coefficient for both 5-V and 3-V supply operation.

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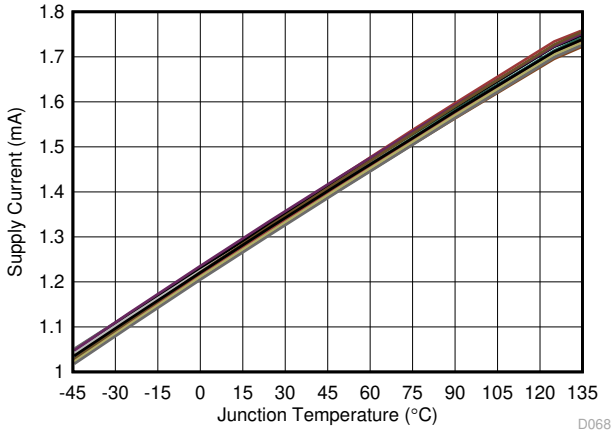

図 11-1. Linear Temperature Coefficient for Supply Current

Using a negative supply to deliver a true swing to ground output when driving SAR ADCs can be desired. Although the THS4551 quotes a rail-to-rail output, linear operation requires approximately 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed, negative-supply generator can accept the 3-V to 5-V positive supply input used by the THS4551 and provides a fixed –230-mV supply for the negative power supply. Using the LM7705 provides an effective solution, as discussed in the *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* TI design (TIDU187)

11.1 Thermal Analysis

The very low internal quiescent power dissipation for the THS4551, combined with the excellent thermal impedance of the 16-pin VQFN package (RGT), limits the possibility of excessively high internal junction temperatures. A more detailed analysis may be warranted because the 10-pin WQFN (RUN) package has a much higher junction-to-ambient thermal impedance (θ_{JA} = 163°C/W).

To estimate the internal T_J, an estimate of the maximum internal power dissipation is first required. There are two pieces to the internal power dissipation: quiescent current power and the power used in the output stage to deliver load current. To simplify the latter, the worst-case output stage power drives a dc differential voltage across a load using half the total supply voltage. Also assume a maximum ambient temperature of 125°C, giving the maximum quiescent current as shown in 図 11-1. As an example:

- Assume a maximum operating supply voltage of 5.4 V. This 5.4-V supply with a maximum I_{CC} of 1.75 mA gives a quiescent power term of 9.45 mW.
- Assume a 200-Ω differential load with a static 2.7-V differential voltage established across the load. The 1.35 mA of dc load current generates a maximum output stage power of (5.4 V – 2.7 V) × 1.35 mA = 3.65 mW.
- From the worst-case total internal P_D of 13.1 mW, multiplying the internal P_D with a 163°C/W thermal impedance times the 163°C/W thermal impedance for the very small 10-pin WQFN package results in a 2.1°C rise from ambient.

Even for this extreme condition and the maximum-rated ambient of 125°C, the junction temperature is a maximum of 127°C, which is less than the rated absolute maximum of 150°C. Follow this same calculation sequence for the exact application and package selected to predict the maximum T_J.

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12 Layout

12.1 Layout Guidelines

12.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. The *THS4551DGKEVM* user guide (SLOU447) shows a good example of high-frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that may not apply to some applications. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1 µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- Higher-speed FDAs such as the THS4551 include a duplicate of the output pins on the input feedback side of the larger 16-pin VQFN (RGT) package. This feature is intended to allow the external feedback resistors to be connected with virtually no trace length on the input side of the package. This internal feedback trace also provides a second feedback path for connecting a feedback capacitor on the input pin sides for band-limited or multiple feedback filter designs. This internal trace shows an approximate 3.3-Ω series resistance that must be considered in any design using that path. The TINA-TI™ model does not include that element (to be generally applicable to all package styles) and must be added externally if the RGT package is used. Use this layout approach without extra trace length on the critical feedback path. The smaller 10-pin WQFN package lines up the outputs and the required inputs on the same side of the package where the feedback R_F resistors must be placed immediately adjacent to the package with minimal trace length.
- The input summing junctions are very sensitive to parasitic capacitance. Any R_G elements must connect into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the R_G elements can have more trace length if needed to the source or to GND.

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12.2 Layout Example

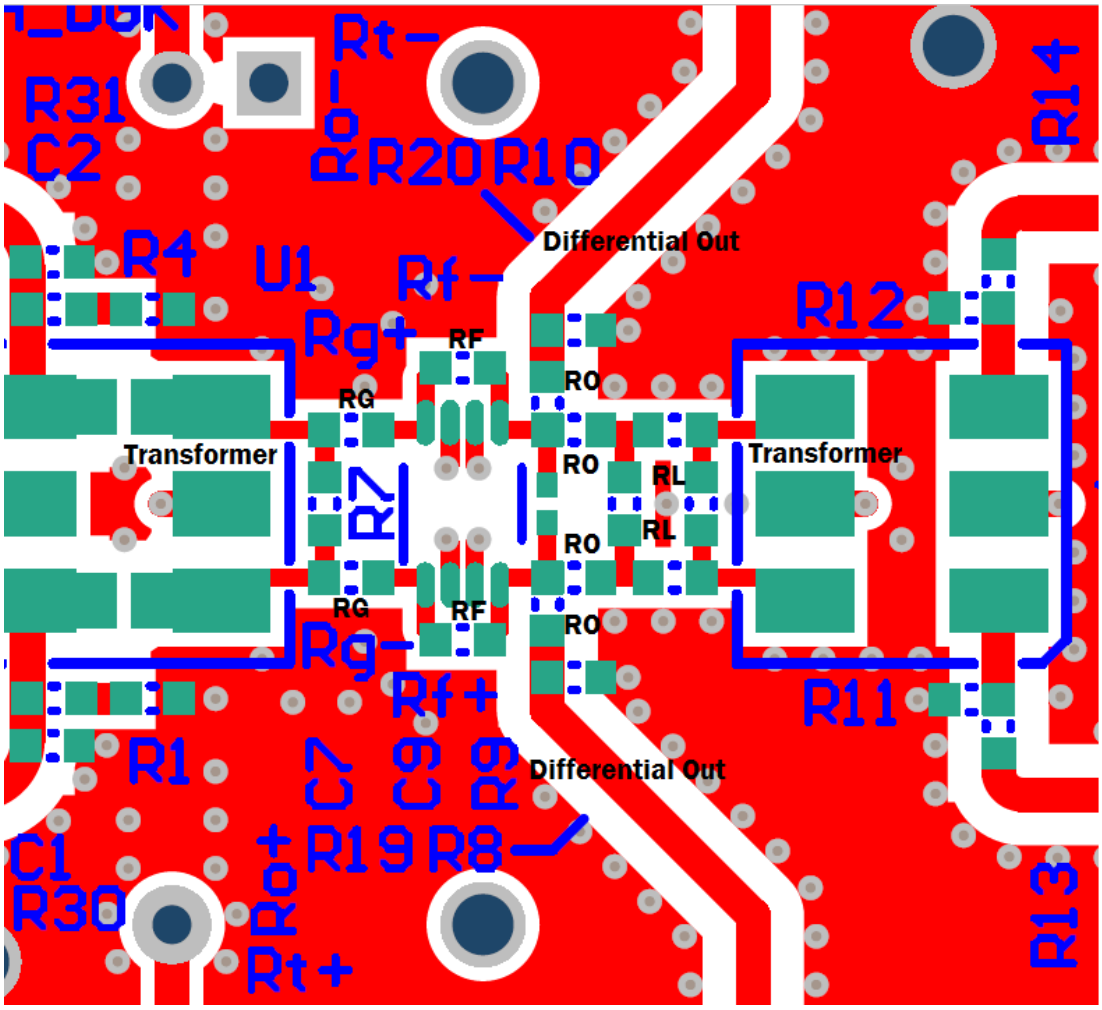

図 12-1. Example Layout

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12.3 EVM Board

図 12-2 and 図 12-3 show the layout of the top and bottom layers of the THS4551DGKEVM evaluation module, respectively.

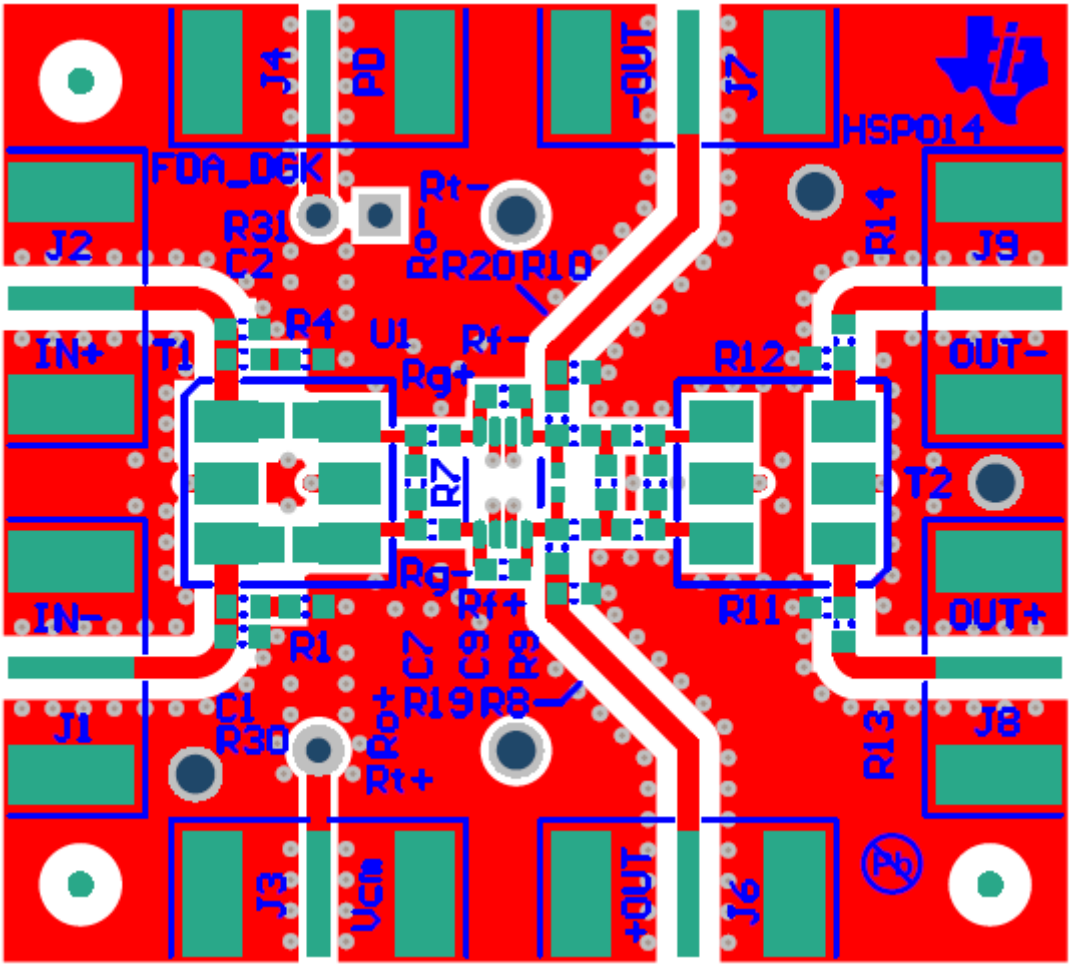

図 12-2. THS4551DGKEVM Top Layer

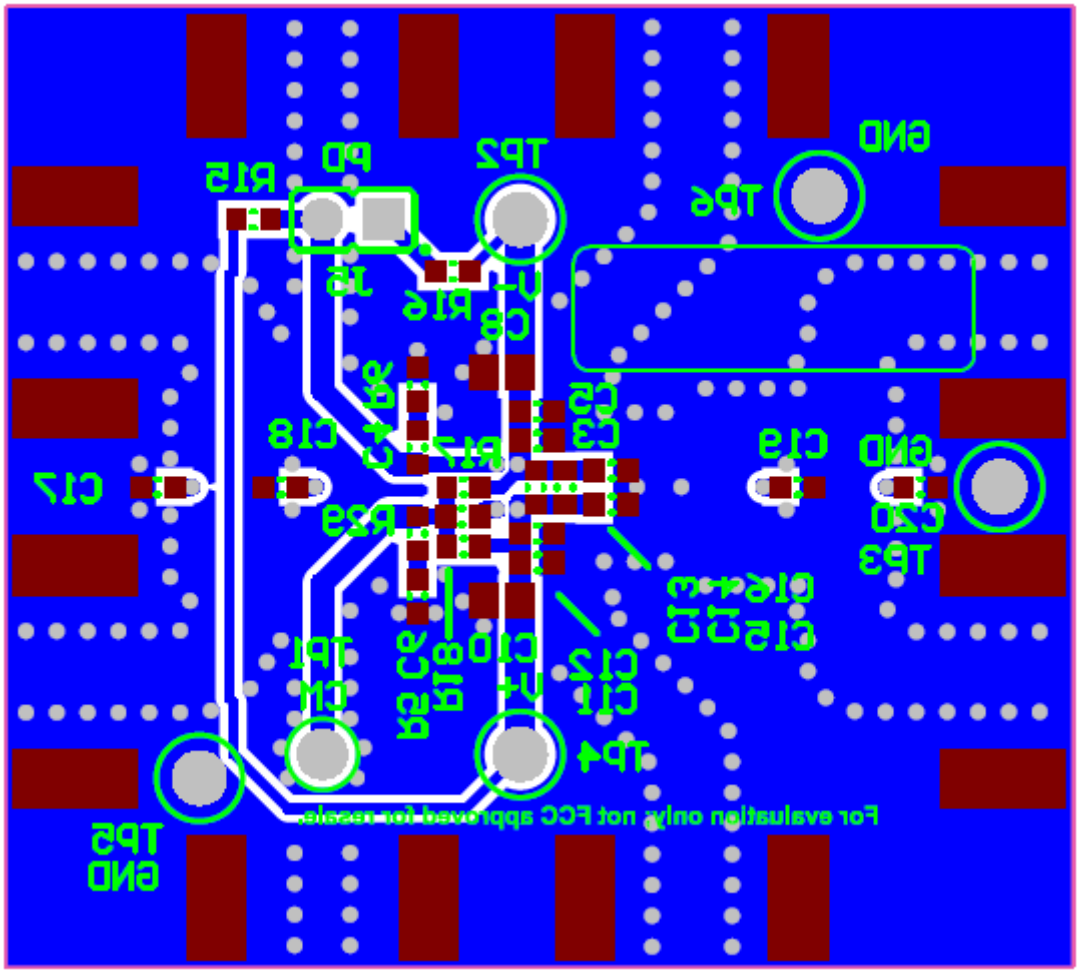

図 12-3. THS4551DGKEVM Bottom Layer

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13 Device and Documentation Support

13.1 Device Support

13.1.1 TINA-TI™ Simulation Model Features

The device model is available on the product folder under www.ti.com in a typical application circuit file. The model includes numerous features intended to speed designer progress over a wide range of application requirements. The following list shows the performance parameters included in the model:

- For the small-signal response shape with any external circuit:
  - Differential open-loop gain and phase
  - Parasitic input capacitance
  - Open-loop differential output impedance
- For noise simulations:
  - Input differential spot voltage noise and a 100-Hz 1/f corner
  - Input current noise on each input with a 6-kHz 1/f corner
- For time-domain, step-response simulations:
  - Differential slew rate
  - I/O headroom models to predict clipping
  - Input stage diodes to predict overdrive limiting
- Fine-scale, dc precision terms:
  - PSRR
  - CMRR

The *セクション 7.9* provides more detail than the macromodels can provide; some of the unmodeled features include:

- Harmonic distortion
- Temperature drift in dc error terms (V_{IO} and I_{OS})
- Overdrive recovery time
- Turn-on and turn-off times using the power-down feature

Some unique simulation considerations come with the THS4551 TINA-TI™ model. This device (and model) include 0.6-pF internal feedback capacitors. These capacitors are intended to improve phase margin when using higher external feedback resistor values. Higher feedback resistors generate an in-band pole in the feedback signal with the differential input capacitance, and the internal 0.6 pF capacitors add a zero to the feedback response shape to shape the noise gain flat at the loop-gain crossover.

In order to generate an accurate open-loop gain and phase simulation, these components must be removed because they are feedback elements, not forward path elements. 図 13-1 illustrates a typical A_{OL} gain and phase simulation (available as a TINA-TI™ software file) where external –0.6-pF capacitors cancel out the internal capacitors in the model (TINA-TI™ supports negative value elements). The inductors inside the loop close the loop for the dc operating point and open the loop immediately for an ac sweep. The input-coupling capacitors are open at dc, then couple in the differential input immediately on an ac sweep. The somewhat odd values help reduce numerical chatter in the simulation. When using the internal feedback traces from the outputs to the inputs on the RGT package, be sure to add the 3.3-Ω trace impedance to any simulation. This impedance is not included in the core model.

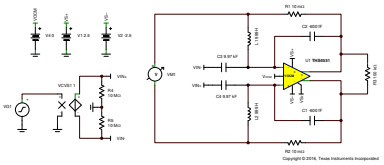

図 13-1. Open-Loop Gain and Phase TINA-TI™ Simulation Setup

This test is set up with a very light load to isolate the no load A_{OL} curve. Adding a load brings in the open-loop Z_{OL} response to the overall response of the output pins. Running this simulation gives the gain and phase of 図 13-2 that closely matches the plot of 図 7-37.

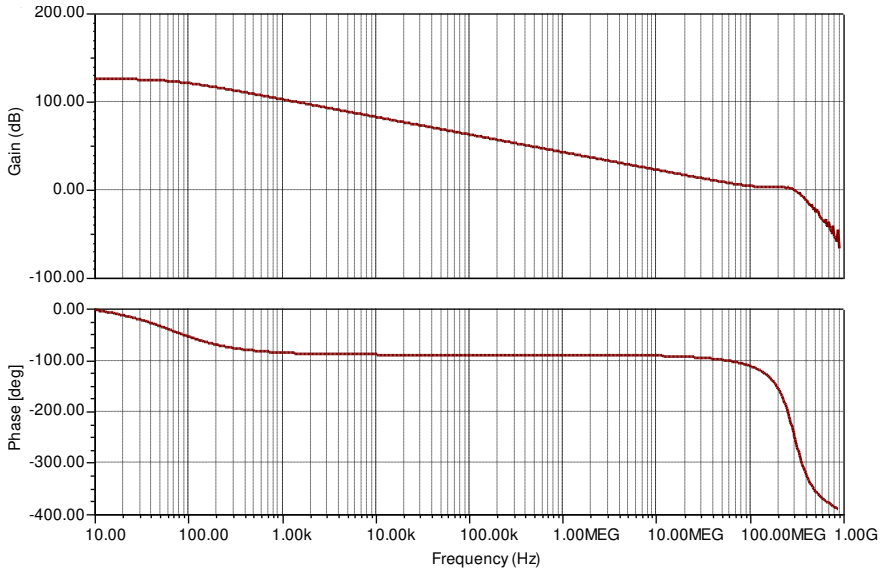

図 13-2. Open-Loop Gain and Phase Simulation Result

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, THS4551 TINA-TI™ model
- Texas Instruments, *THS4551DGKEVM User Guide*
- Texas Instruments, *THS452x Very Low Power, Negative Rail Input, Rail-To-Rail Output, Fully Differential Amplifier*
- Texas Instruments *LMH6629 Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown*
- Texas Instruments *OPA847 Wideband, Ultra-Low Noise, Voltage-Feedback Operational Amplifier with Shutdown*
- Texas Instruments, *INA188 Precision, Zero-Drift, Rail-to-Rail Out, High-Voltage Instrumentation Amplifier*
- Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™*
- Texas Instruments, *OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers*
- Texas Instruments, *ADC322x Dual-Channel, 12-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters*
- Texas Instruments, *ADC324x Dual-Channel, 14-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters*
- Texas Instruments, *ADS127L01 24-Bit, High-Speed, Wide-Bandwidth Analog-to-Digital Converter*
- Texas Instruments, *ADS127L01EVM User's Guide*
- Texas Instruments, *ADS9110 18-Bit, 2-MSPS, 15-mW, SAR ADC with multiSPI™ Interface*
- Texas Instruments, *REF6025EVM-PDK User's Guide* (SBAU258)
- Texas Instruments, *24-Bit, 192-kHz Sampling, Advanced Segment, Audio Stereo Digital-to-Analog Converter*
- Texas Instruments, *LM27762 Low-Noise Regulated Switched-Capacitor Voltage Inverter*
- Texas Instruments, *LM7705 Low-Noise Negative Bias Generator*
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts*
- Texas Isntruments, *Design Methodology for MFB Filters in ADC Interface Applications*
- Texas Instruments, *Design for Wideband Differential Transimpedance DAC Output*
- Texas Instruments, *RLC Filter Design for ADC Interface Applications*
- Texas Instruments, *TINA-TI Open Loop No Load Response*
- Texas Instruments, *TINA-TI Basic Gain of 1 Test Circuit*
- Texas Instruments, *TINA-TI ADTL1-4-75 Model Test*
- Texas Instruments, *TINA-TI Common Mode Test CKT*
- Texas Instruments, *TINA-TI AC Coupled Single to Differentiate Gain of 2*
- Texas Instruments, *TINA-TI Single to Differential Attenuator*
- Texas Instruments, *TINA-TI Gain of 5 Single to Different Simplified*
- Texas Instruments, *TINA-TI AC coupled different IO*
- Texas Instruments, *TINA-TI Differential IO with OPA2192 to FDA to SAR*
- Texas Instruments, *TINA-TI ADS127L01 MFB Driver*
- Texas Instruments, *TINA-TI ADS127L01 MFB Driver LG Test*
- Texas Instruments, *TINA-TI Attenuator With No Caps Gain of 0.1*
- Texas Instruments, *TINA-TI Attenuator With a Caps Gain of 0.1*
- Texas Instruments, *TINA-TI High Gain Single to Different with Feedback Pole*
- Texas Instruments, *TINA-TI High Gain Single to Different with Feedback Pole and Input C*
- Texas Instruments, *TINA-TI Gain of 0.2 100kHz Butterworth MFB Filter*
- Texas Instruments, *TINA-TI 100kHz MFB filter LG test*
- Texas Instruments, *TINA-TI Differential Transimpedance LG Sim*
- Texas Instruments, *TINA-TI Differential Audio DAC ZT Design*
- Texas Instruments, *TINA-TI Gain of 5 Single to Different with 10Mhz Bessel*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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13.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

13.5 Trademarks

TINA-TI™ are trademarks of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4551IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HS4551
THS4551IRGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HS4551
THS4551IRGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HS4551
THS4551IRGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HS4551
THS4551IRUNR	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IRUNR.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IRUNT	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4551
THS4551IRUNT.B	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4551

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

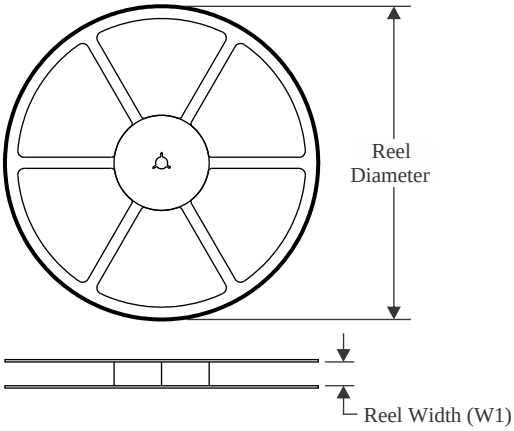
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

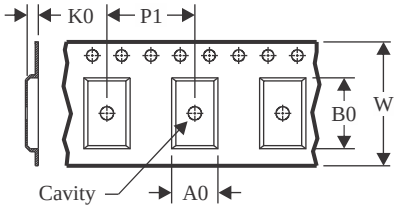
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

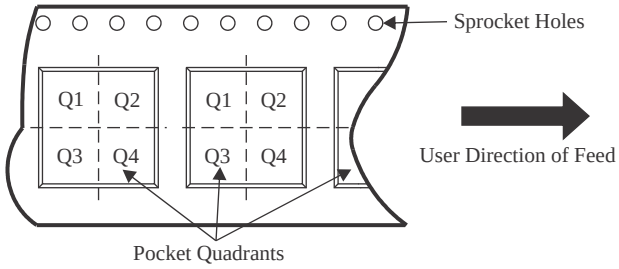


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

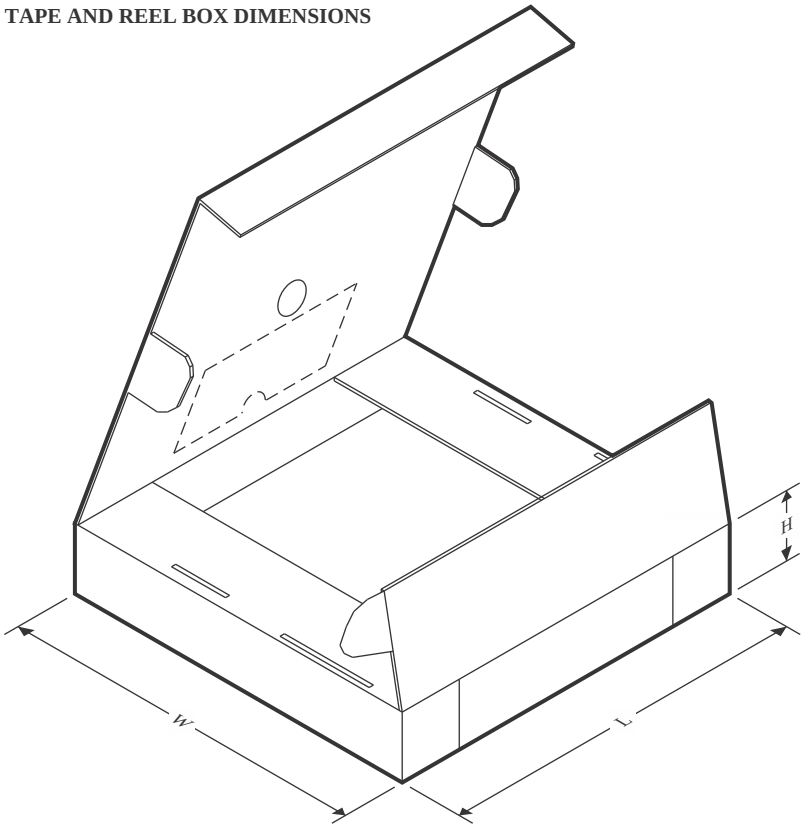
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4551IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4551IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4551IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4551IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4551IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
THS4551IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4551IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4551IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
THS4551IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
THS4551IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0
THS4551IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
THS4551IRUNT	QFN	RUN	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

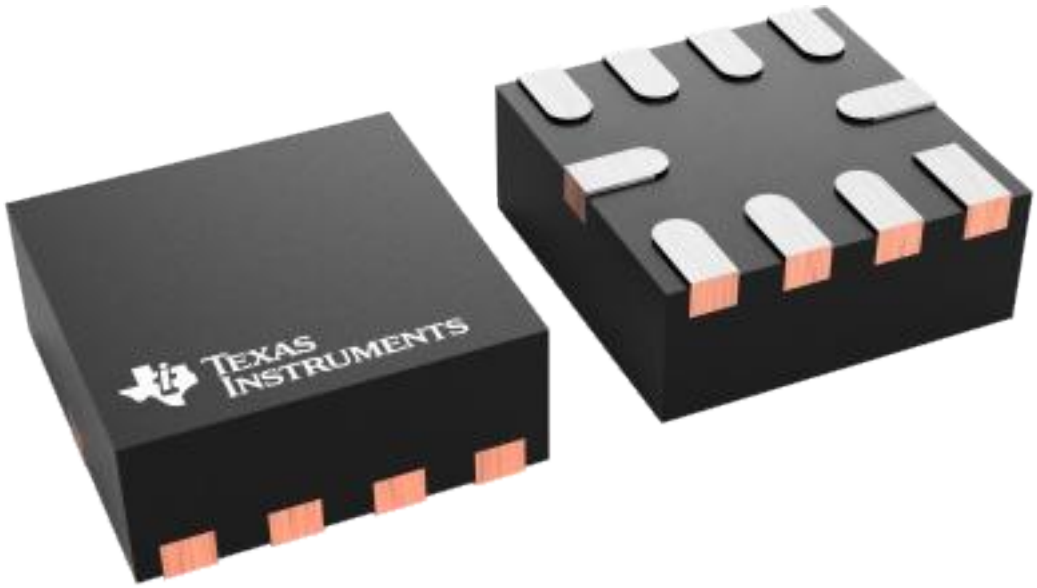
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



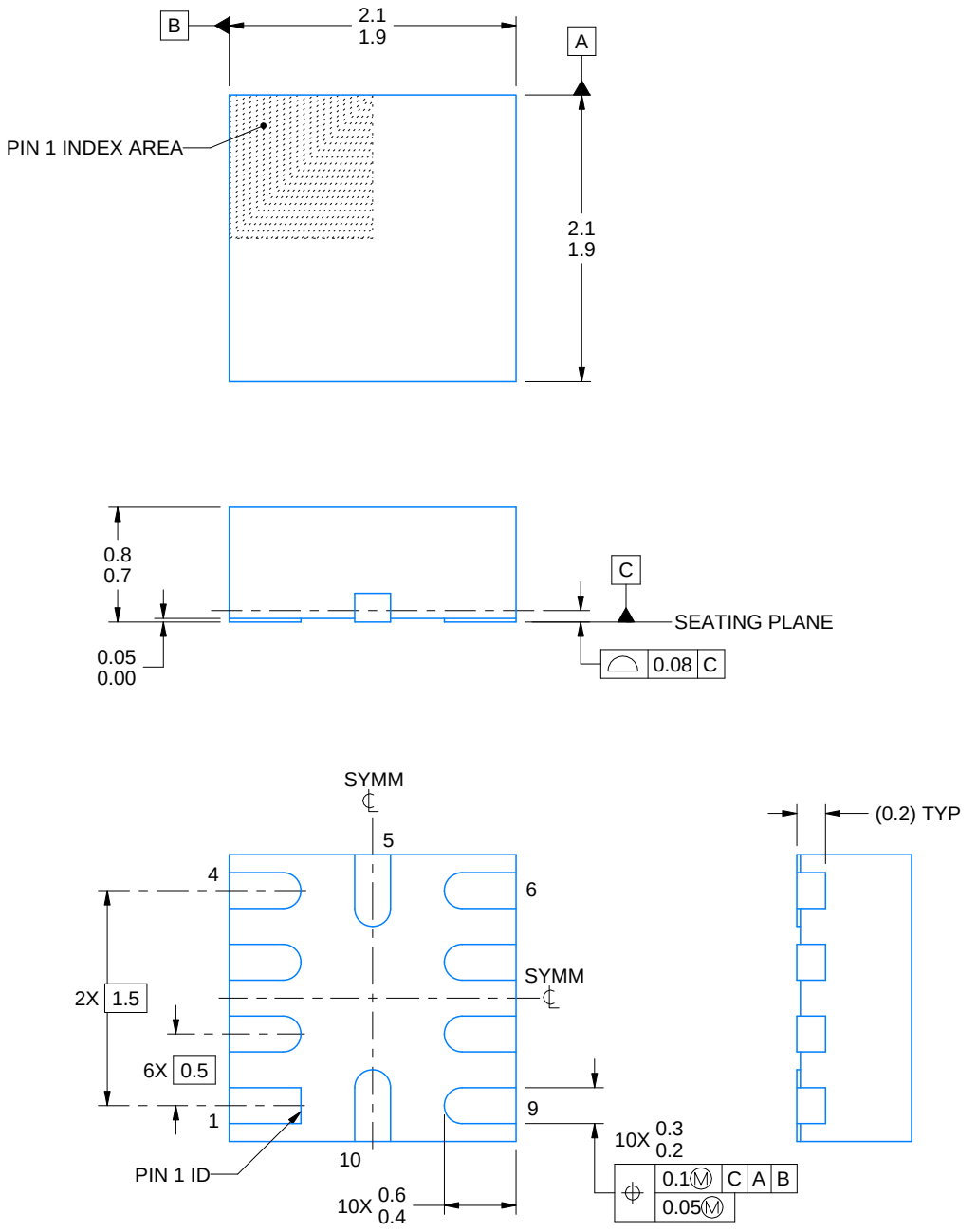
4228249/A

RUN0010A

PACKAGE OUTLINE

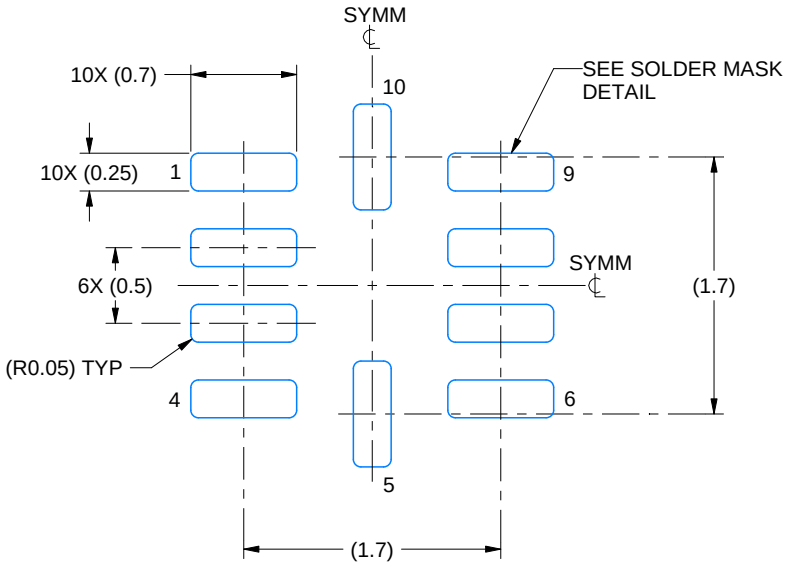
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

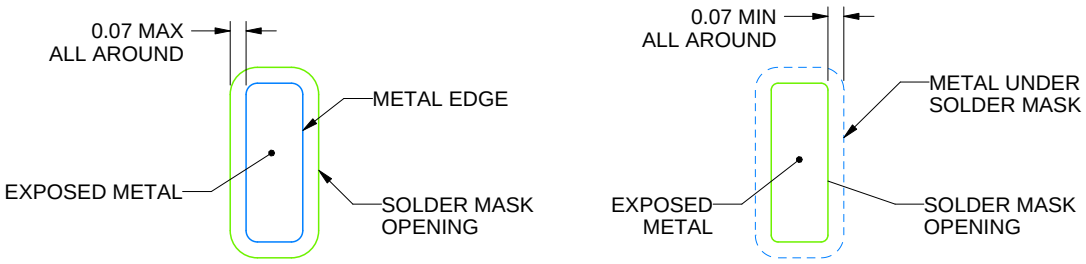


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

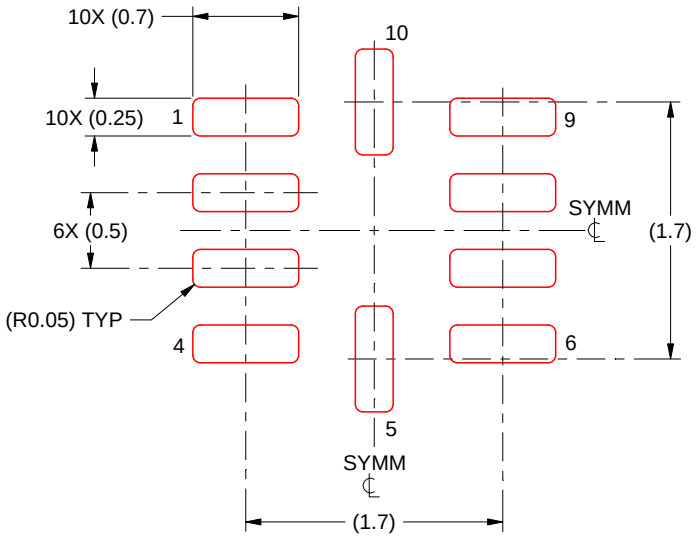
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

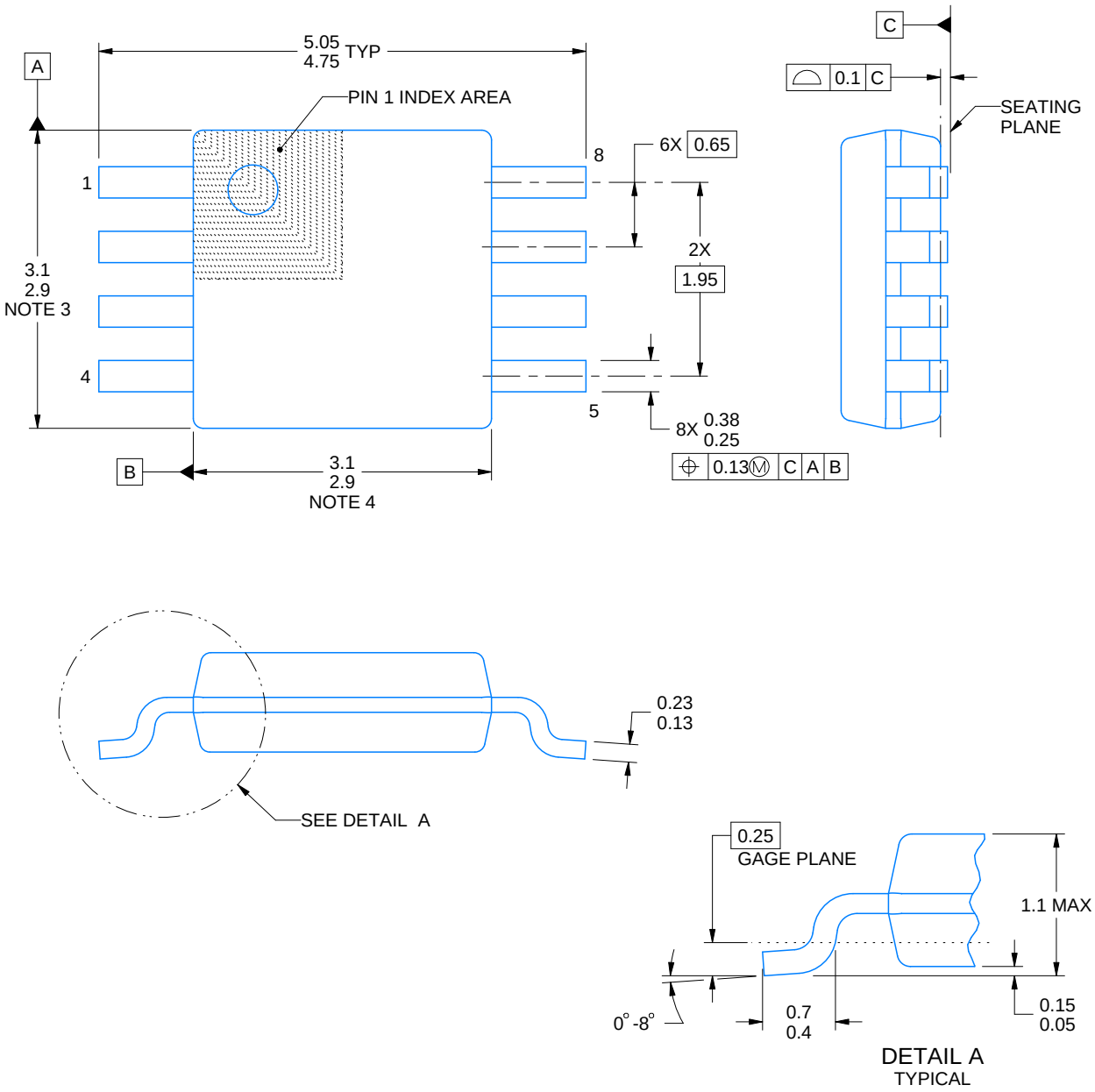
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

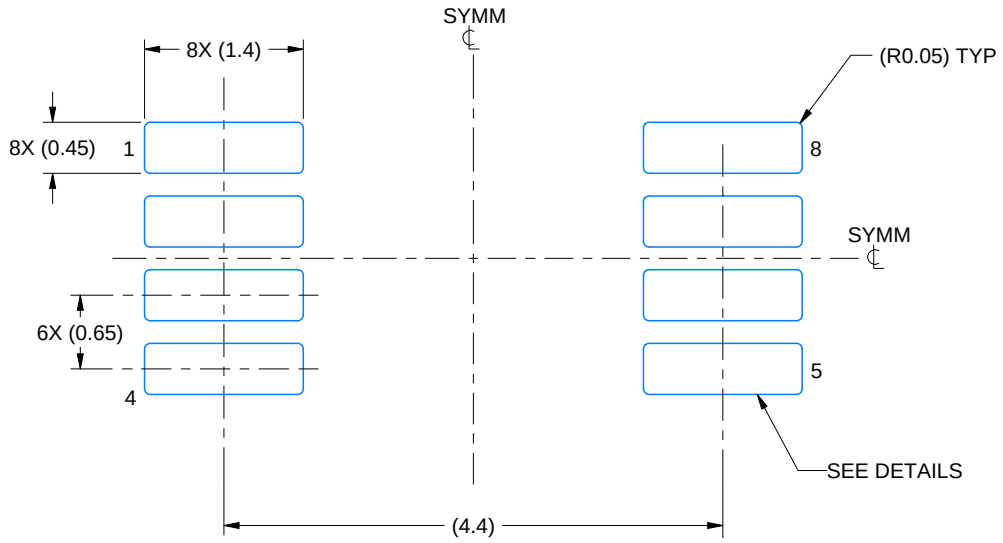
SMALL OUTLINE PACKAGE



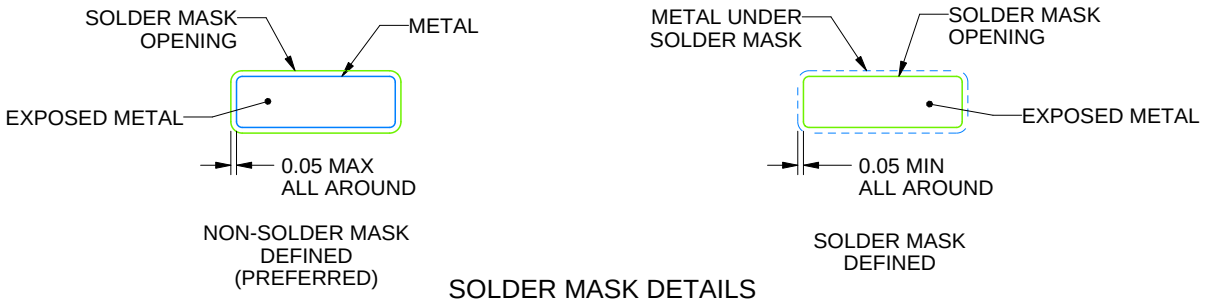
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

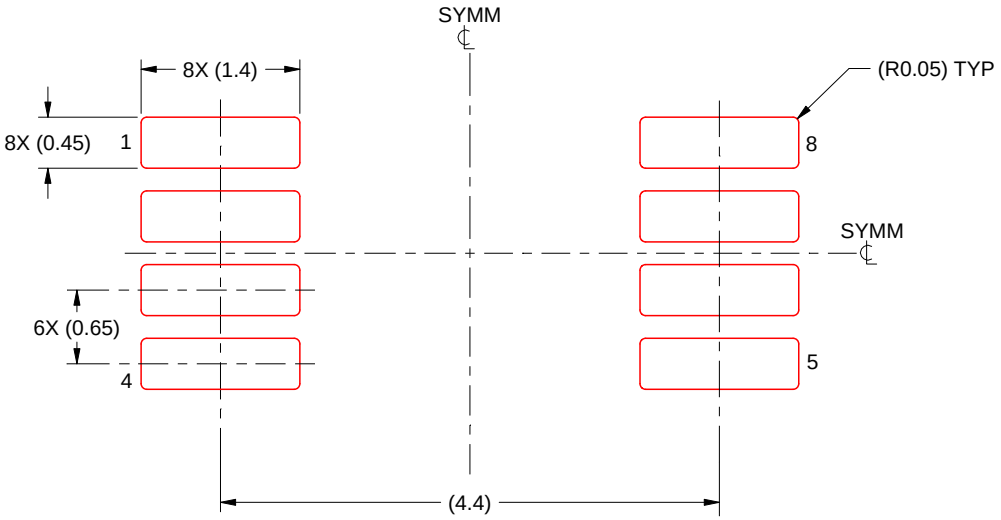


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

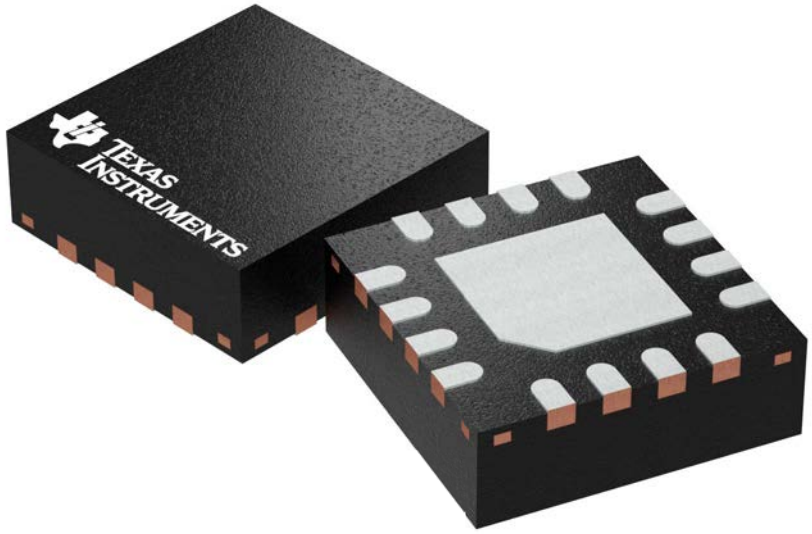
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

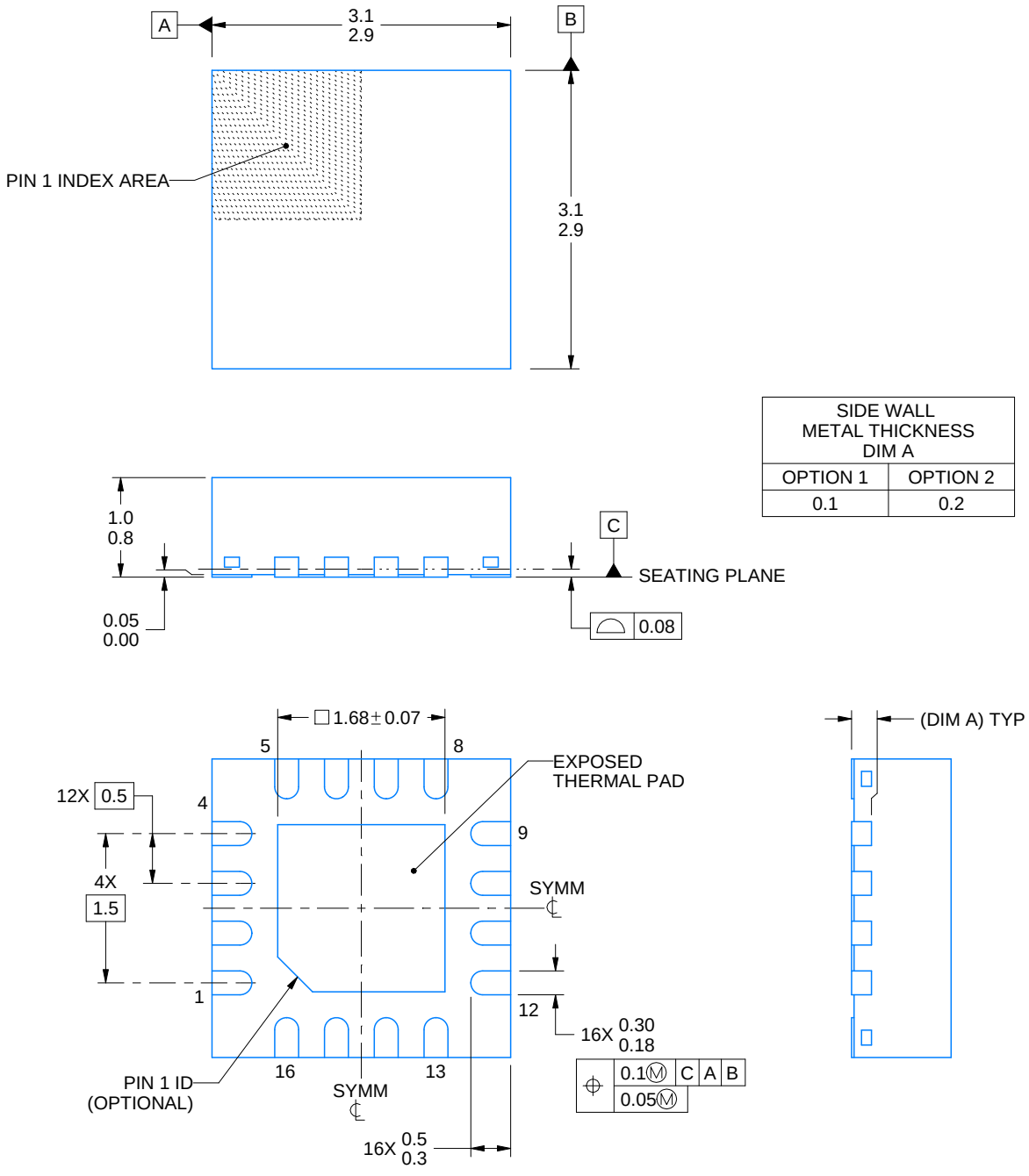
4203495/I

RGT0016C

PACKAGE OUTLINE

VQFN - 1 mm max height

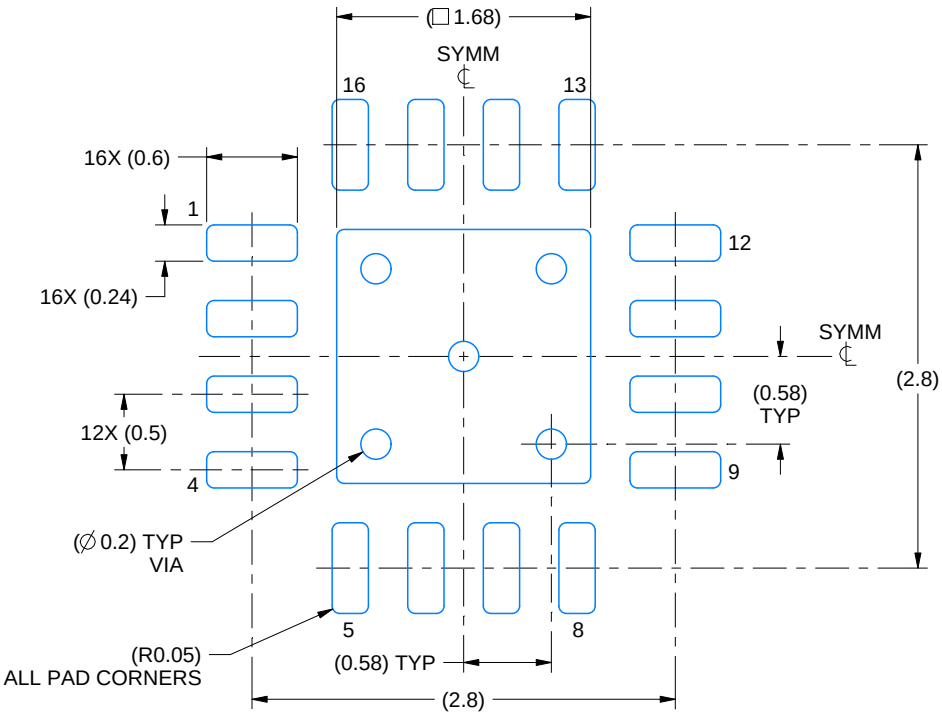
PLASTIC QUAD FLATPACK - NO LEAD



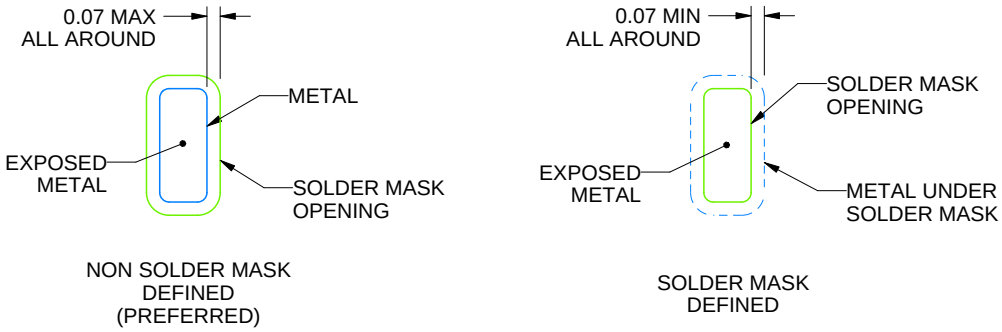
4222419/D 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

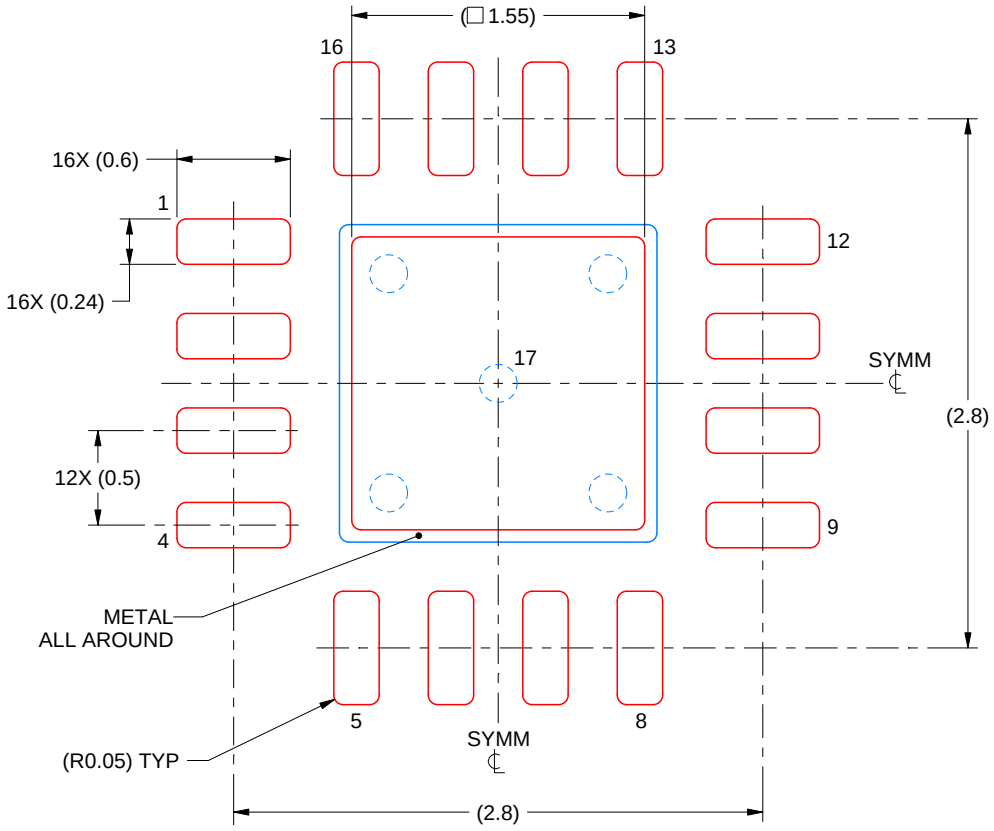


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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