THS4631 High-Voltage, High-Slew-Rate, Wideband FET-Input Operational Amplifier

1 Features

- High bandwidth:
  - 325MHz in unity gain
  - 210MHz gain bandwidth product
- High slew rate:
  - 900V/µs (G = 2)
  - 1000V/µs (G = 5)
- Low distortion of –76dB, SFDR at 5MHz
- Maximum input bias current: 100pA
- Input voltage noise: $7nV/\sqrt{Hz}$
- Maximum input offset voltage: 500µV at 25°C
- Low offset drift: 2.5µV/°C
- Input impedance: 10^9 || 3.9pF
- Wide supply range: ± 5V to ± 15V
- High output current: 95mA

2 Applications

- Wideband photodiode amplifier
- High-speed transimpedance gain stage
- Test and measurement systems
- Current DAC output buffer
- Active filtering
- High-speed signal integrator
- High-impedance buffer

3 Description

The THS4631 is a high-speed, FET-input op amp designed for applications requiring wideband operation, high-input impedance, and high-power supply voltages. By providing a 210MHz gain bandwidth product, ±15V supply operation, and 100pA input bias current, the THS4631 is capable of simultaneous wideband transimpedance gain and large output signal swing. The fast 1000V/µs slew rate allows for fast settling times and good harmonic distortion at high frequencies. Low current and voltage noise allow amplification of extremely low-level input signals while still maintaining a large signal-to-noise ratio.

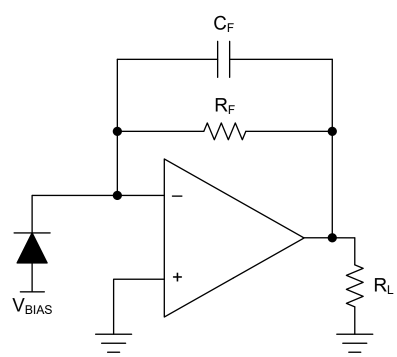
These high-performance characteristics make the THS4631 an excellent choice for use as a wideband photodiode amplifier. Photodiode output current is a prime candidate for transimpedance amplification. Other potential applications include test and measurement systems requiring high-input impedance, ADC and DAC buffering, high-speed integration, and active filtering.

The THS4631 is offered in a 8-pin SOIC (D) package, and 8-pin HSOIC (DDA) and HVSSOP (DGN) with PowerPAD™ integrated-circuit packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THS4631	D (SOIC, 8)	4.9mm × 6mm
	DDA (HSOIC, 8)	4.9mm × 6mm
	DGN (HVSSOP, 8)	3mm × 4.9mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Photodiode Circuit

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4 Related Products

DEVICE	V_S (V)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM GAIN
OPA656	±5	230	400	6	1
OPA657	±5	1600	700	4.8	7
OPA627	±15	16	55	4.5	1
THS4601	±15	180	100	5.4	1

5 Pin Configuration Functions

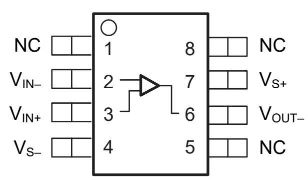


Figure 5-1. D Package, 8-Pin SOIC DDA Package, 8-pin HSOIC and DGN Package, 8-Pin HVSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1	—	No internal connection
NC	5	—	No internal connection
NC	8	—	No internal connection
V_{IN-}	2	Input	Inverting input
V_{IN+}	3	Input	Noninverting input
V_{OUT-}	6	Output	Amplifier output
V_{S-}	4	Input	Negative power-supply connection
V_{S+}	7	Input	Positive power-supply connection
Thermal Pad	Thermal Pad	—	For DDA and DGN packages only. The thermal pad is internally connected to V–. The thermal pad must be soldered to a printed-circuit board (PCB) connected to V–, even with applications that have low power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNITS
V_S	Supply voltage, V_{S-} to V_{S+}		33	V
V_I	Input voltage	$-V_S$	$+V_S$	V
I_O	Output current		150	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Junction temperature[2]		150	°C
T_A	Operating free-air temperature, continues operation, long-term reliability[2]		125	°C
T_{stg}	Storage temperature	−65	150	°C

(1) The *Absolute Maximum Ratings* under any condition is limited by the constraints of the silicon process. Stresses above these ratings can cause permanent damage. Exposure to absolute maximum conditions for extended periods can degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature can result in reduced reliability, lifetime of the device, or both.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	
		Machine-model (MM)	±100	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNITS
V_S	Supply Voltage	Dual supply	±5	±15	V
		Single supply	10	30	V
T_A	Operating free-air temperature		−40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		THS4631			UNIT
		D (SOIC)	DDA (HSOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95	45.8	58.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	9.2	4.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	N/A	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, and T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth, –3dB	G = 1, R_F = 0Ω, V_O = 200mV_{PP}			325		MHz
	G = 2, R_F = 499Ω, V_O = 200mV_{PP}			105		
	G = 5, R_F = 499Ω, V_O = 200mV_{PP}			55		
	G = 10, R_F = 499Ω, V_O = 200mV_{PP}			25		
Gain bandwidth product	G >= 20			210		MHz
0.1dB bandwidth flatness	G = 2, R_F = 499Ω, C_F = 8.2pF			6		MHz
	G = 2, R_F = 499Ω			20		
Large-signal bandwidth	G = 2, R_F = 499Ω, V_O = 2V_{PP}			105		MHz
Slew rate	G = 2, R_F = 499Ω, V_O = 2V step			550		V/µs
	G = 2, R_F = 499Ω, V_O = 10V step			900		
	G = 5, R_F = 499Ω, V_O = 10V step			1000		
Rise and fall time	2V step			5		ns
Settling time	0.1%, G = −1, V_O = 2V step, C_F = 4.7pF			40		ns
	0.01%, G = −1, V_O = 2V step, C_F = 4.7pF			190		
Second harmonic distortion	G = 2, V_O = 2V_{PP}, f = 5MHz	R_L = 100Ω		–65		dBc
		R_L = 1kΩ		–76		
Third harmonic distortion	G = 2, V_O = 2V_{PP}, f = 5MHz	R_L = 100Ω		–62		dBc
		R_L = 1kΩ		–94		
HARMONIC DISTORTION						
Input voltage noise	f > 10kHz			7		$nV/\sqrt{Hz}$
Input current noise	f > 10kHz			20		$fA/\sqrt{Hz}$
DC PERFORMANCE						
Open-loop gain	R_L = 1kΩ		70	80		dB
		T_A = −40°C to +85°C	65			
Input offset voltage(1)	V_{CM} = 0V			±260	±500	µV
		T_A = −40°C to +85°C			±2000	
Average offset voltage drift(1)	V_{CM} = 0V, T_A = −40°C to +85°C			±2.5	±12	µV/°C
Input bias current	V_{CM} = 0V			±50	±100	pA
		T_A = −40°C to +85°C			±2000	
Input offset current	V_{CM} = 0V			±25	±100	pA
		T_A = −40°C to +85°C			±1000	
INPUT CHARACTERISTICS						
Common-mode input voltage, high			11.5	12		V
	T_A = −40°C to +85°C		11			
Common-mode input voltage, low				–13	–12.5	V
	T_A = −40°C to +85°C				–9	
Common-mode rejection ratio	V_{CM} = ±10V		86	95		dB
		T_A = −40°C to +85°C	80			
Differential input impedance				10^9 || 3.9		Ω || pF
Common-mode input impedance				10^9 || 3.9		Ω || pF

6.5 Electrical Characteristics (continued)

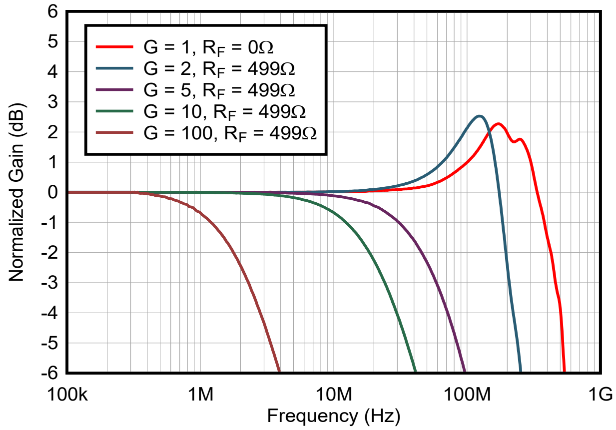
at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, and T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
Output voltage swing	R_L = 100Ω		±10	±11		V
		T_A = −40°C to +85°C	±9.5			
	R_L = 1kΩ		±13	±13.5		
		T_A = −40°C to +85°C	±12.8			
Static output current (sourcing)	R_L = 20Ω		120	180		mA
		T_A = −40°C to +85°C	90			
Static output current (sinking)	R_L = 20Ω			–180	–120	mA
		T_A = −40°C to +85°C			–90	
Closed loop output impedance	G = 1, f = 1MHz			0.1		Ω
POWER SUPPLY						
Specified operating voltage			±4	±15	±16.5	V
		T_A = −40°C to +85°C	±4		±16.5	V
Quiescent current			10	12.5	14.5	mA
		T_A = −40°C to +85°C	9		15	
Power supply rejection (PSRR +)	V_{S+} = 15.5V to 14.5V, V_{S-} = 15V		85	95		dB
		T_A = −40°C to +85°C	80			
Power supply rejection (PSRR –)	V_{S+} = 15V, V_{S-} = −15.5V to −14.5V		85	95		dB
		T_A = −40°C to +85°C	80			

(1) Input offset voltage is 100% tested at 25°C and is specified by characterization and simulation over the listed temperature range.

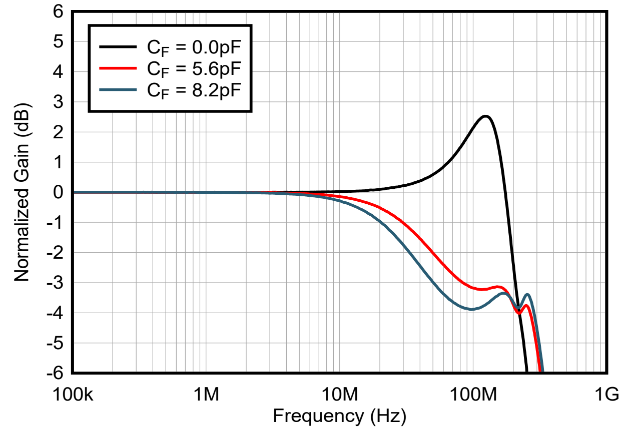
6.6 Typical Characteristics

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, C_F = 0pF, and T_A = 25°C (unless otherwise noted)



G = 100, R_F = 11.3kΩ, R_G = 115Ω, V_{OUT} = 200mV_{PP}

Figure 6-1. Small-Signal Frequency Response



G = 2, R_F = 499Ω, R_G = 499Ω, V_{OUT} = 200mV_{PP}

Figure 6-2. Small-Signal Frequency Response

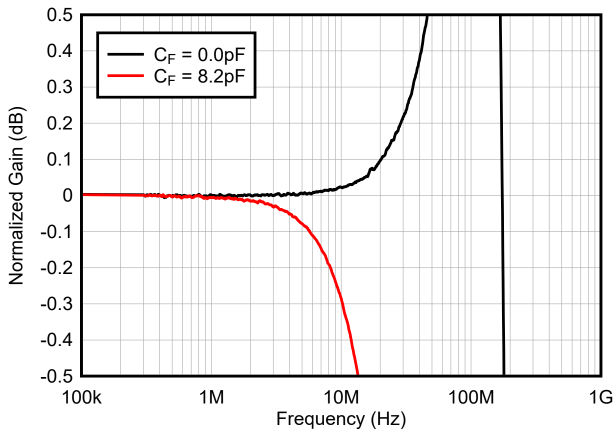
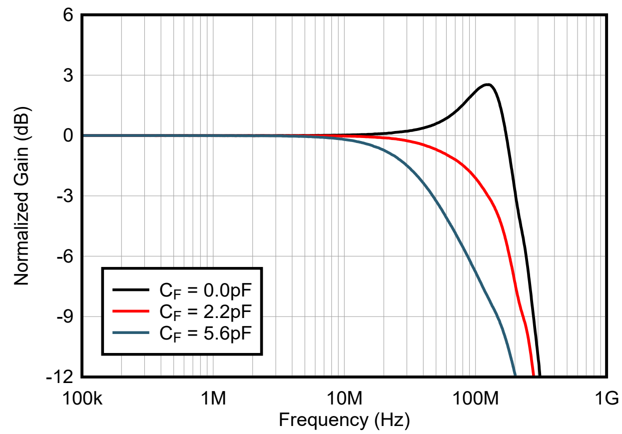


Figure 6-3. 0.1dB Flatness



G = –1, R_F = 499Ω, R_G = 499Ω, V_{OUT} = 200mV_{PP}

Figure 6-4. Small-Signal Frequency Response

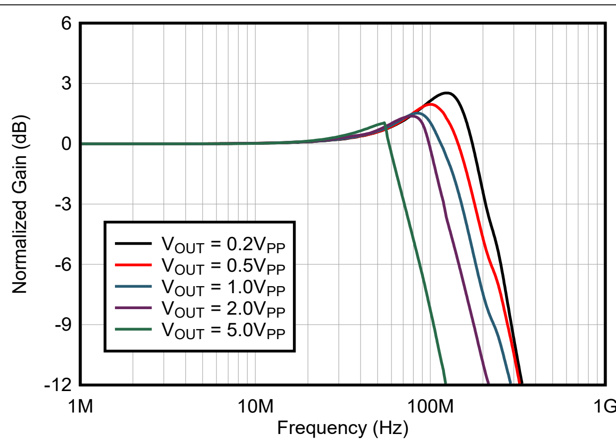
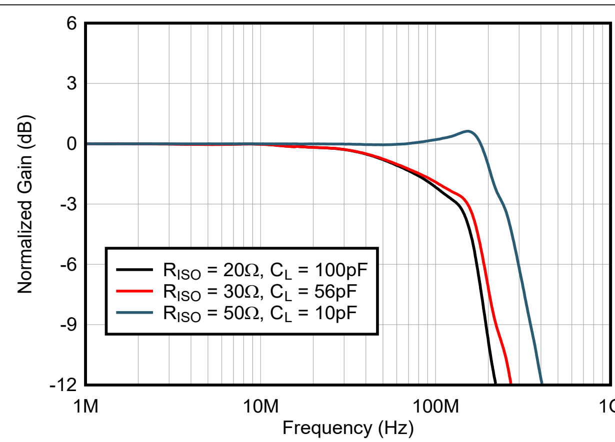


Figure 6-5. Large-Signal Frequency Response



G = 1, R_F = 0Ω

Figure 6-6. Frequency Response vs Capacitive Load

6.6 Typical Characteristics (continued)

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, C_F = 0pF, and T_A = 25°C (unless otherwise noted)

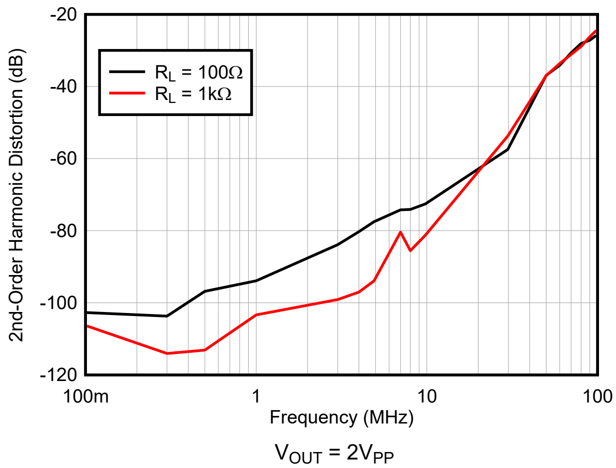


Figure 6-7. Second-Order Harmonic Distortion vs Frequency

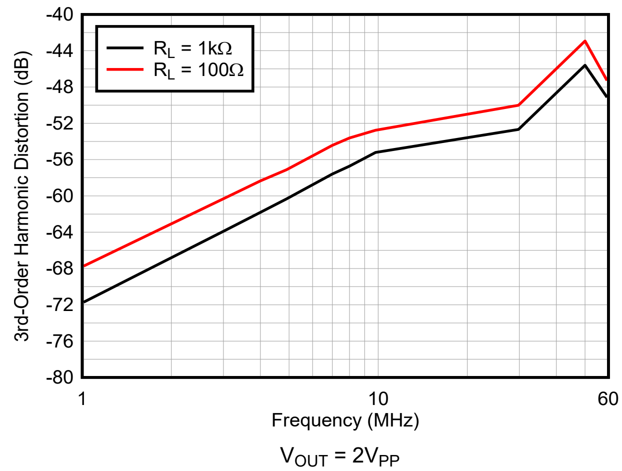


Figure 6-8. Third-Order Harmonic Distortion vs Frequency

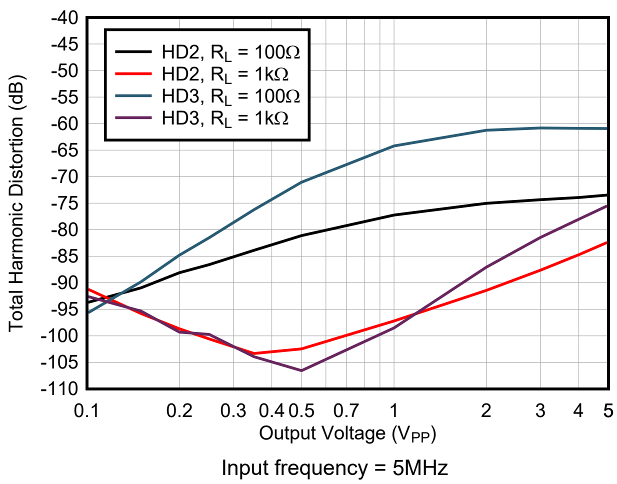


Figure 6-9. Harmonic Distortion vs Output-Voltage Swing

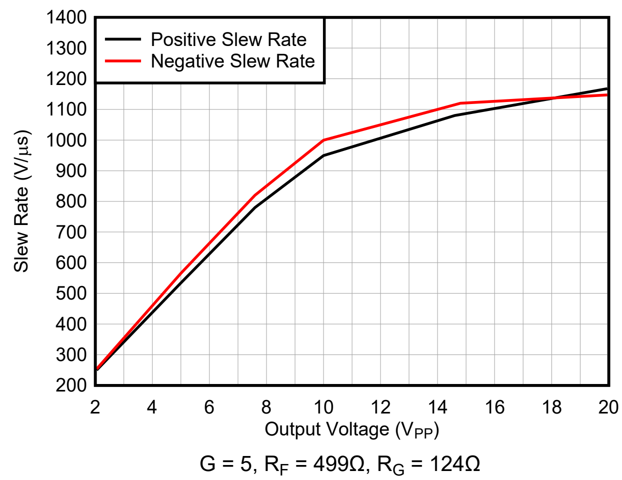


Figure 6-10. Slew Rate vs Output Voltage

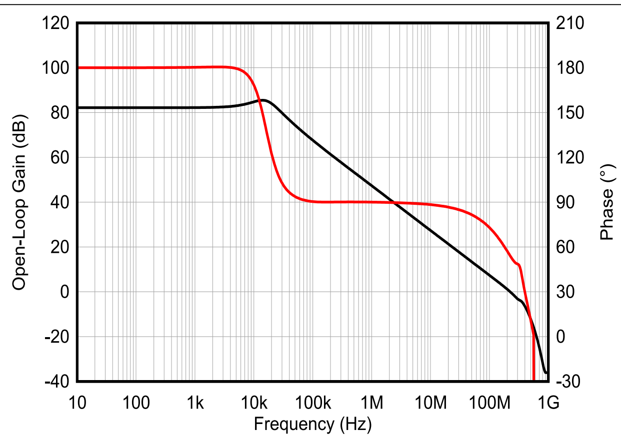


Figure 6-11. Open-Loop Gain and Phase vs Frequency

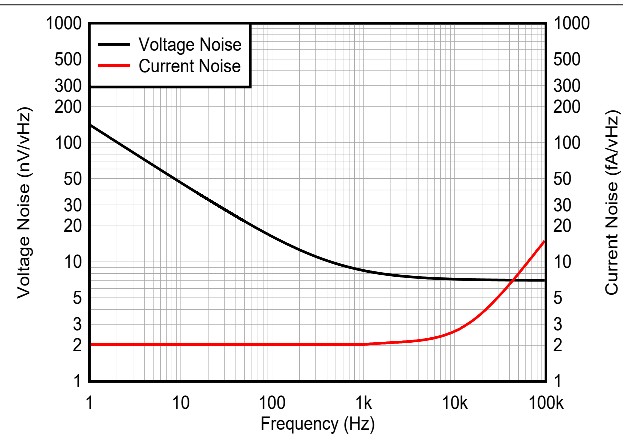


Figure 6-12. Input Voltage and Current Noise vs Frequency

6.6 Typical Characteristics (continued)

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, C_F = 0pF, and T_A = 25°C (unless otherwise noted)

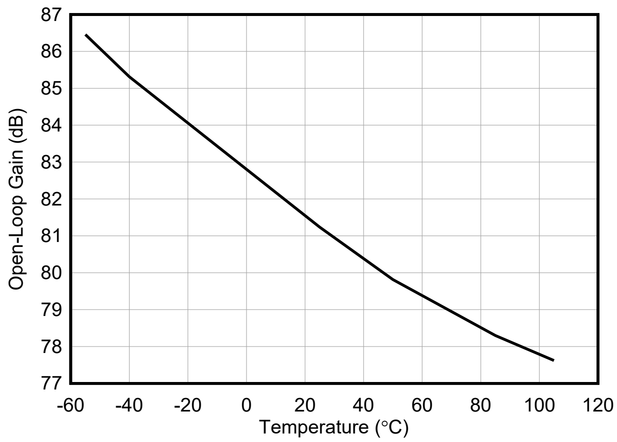


Figure 6-13. Open-Loop Gain vs Temperature

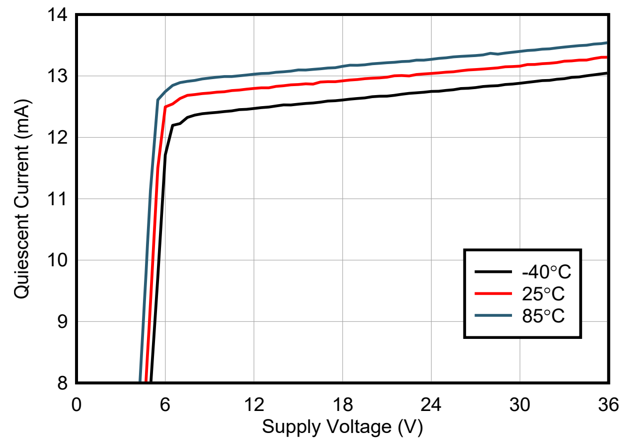


Figure 6-14. Quiescent Current vs Supply Voltage

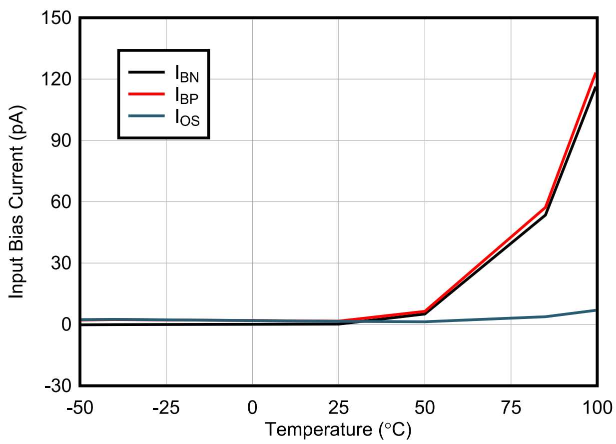


Figure 6-15. Input Bias Current vs Temperature

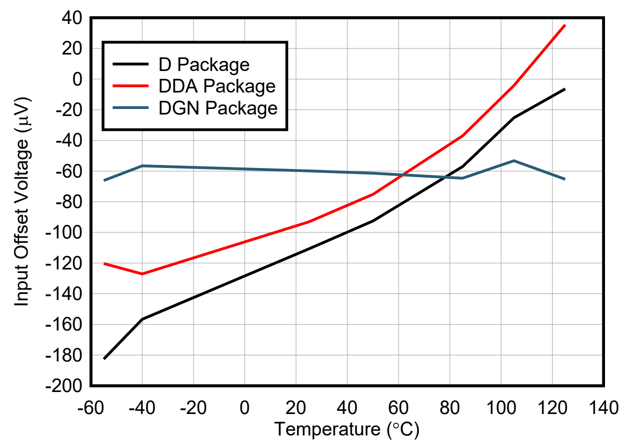


Figure 6-16. Input Offset Voltage vs Temperature

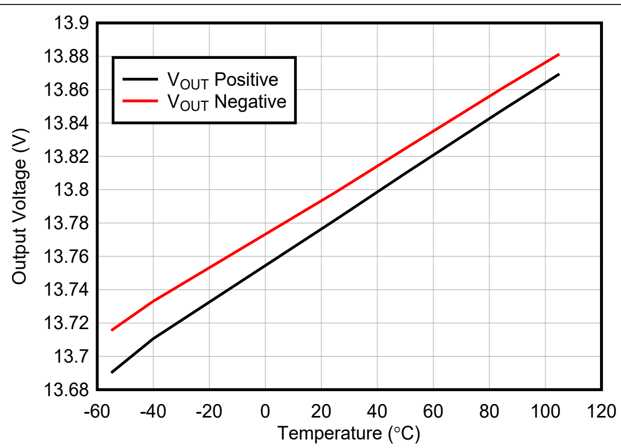


Figure 6-17. Output Voltage vs Temperature

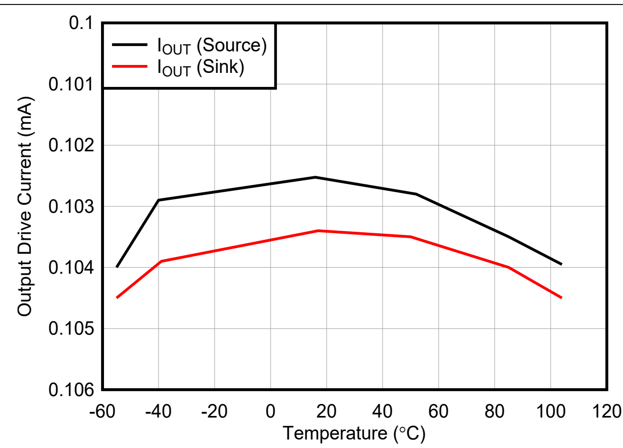
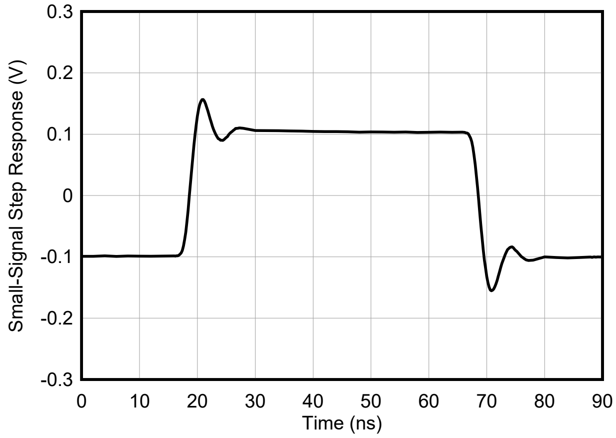


Figure 6-18. Static Output-Drive Current vs Temperature

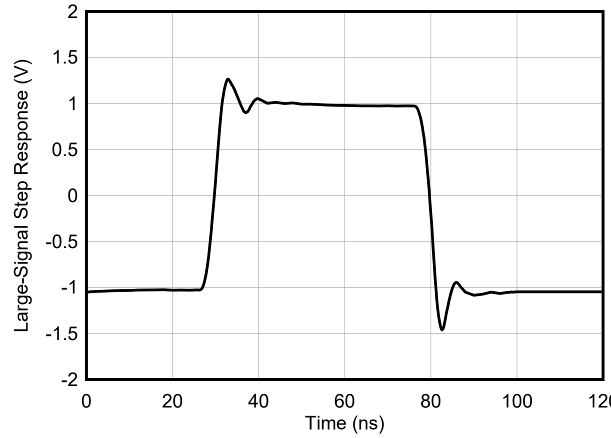
6.6 Typical Characteristics (continued)

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, C_F = 0pF, and T_A = 25°C (unless otherwise noted)



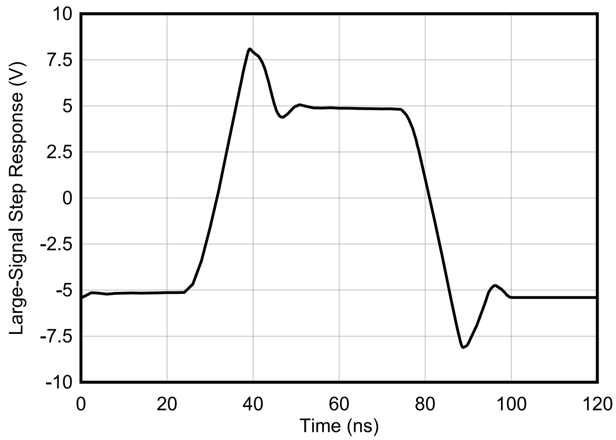
V_{IN} = 100mV_{PP}

Figure 6-19. Small-Signal Transient Response



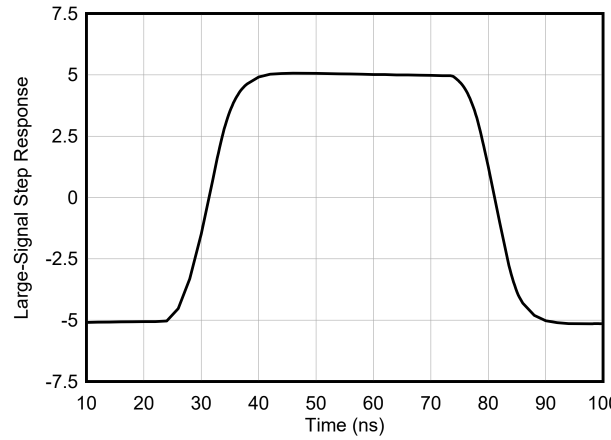
V_{IN} = 1V_{PP}

Figure 6-20. Large-Signal Transient Response



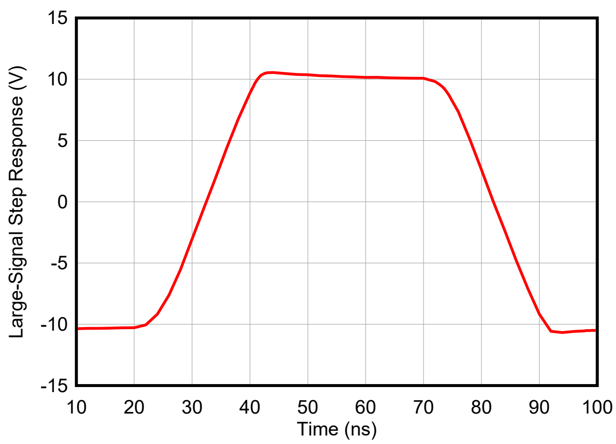
V_{IN} = 5V_{PP}

Figure 6-21. Large-Signal Transient Response



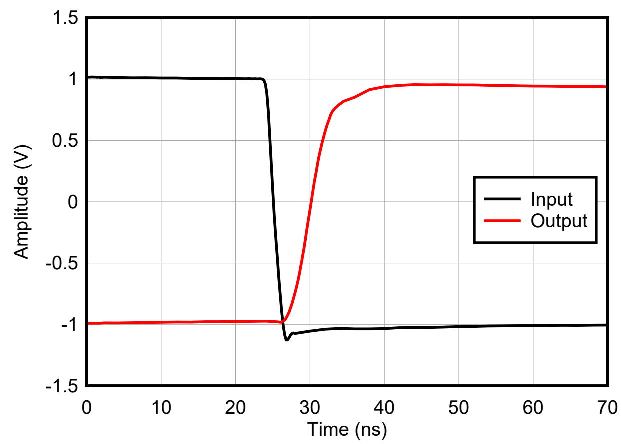
G = 5, R_F = 499Ω, R_G = 124Ω, V_{IN} = 2V_{PP}

Figure 6-22. Large-Signal Transient Response



G = 5, R_F = 499Ω, R_G = 124Ω, V_{IN} = 4V_{PP}

Figure 6-23. Large-Signal Transient Response

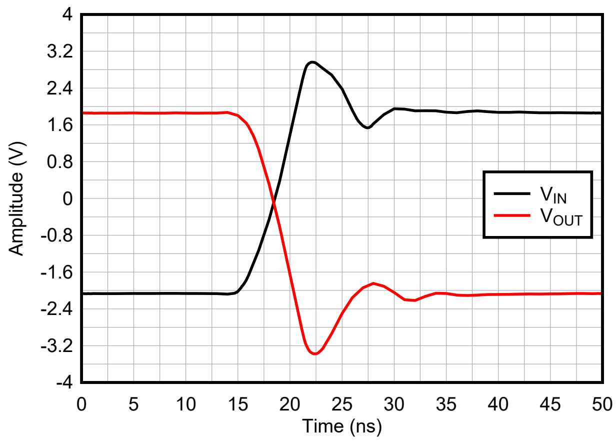


G = –1, C_F = 4.7pF

Figure 6-24. Settling Time

6.6 Typical Characteristics (continued)

at V_S = ±15V, R_F = 499Ω, R_L = 1kΩ, G = 2, C_F = 0pF, and T_A = 25°C (unless otherwise noted)



G = –1, C_F = 4.7pF

Figure 6-25. Settling Time

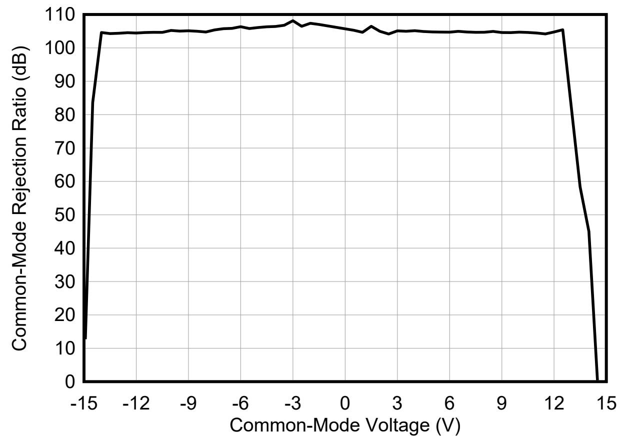
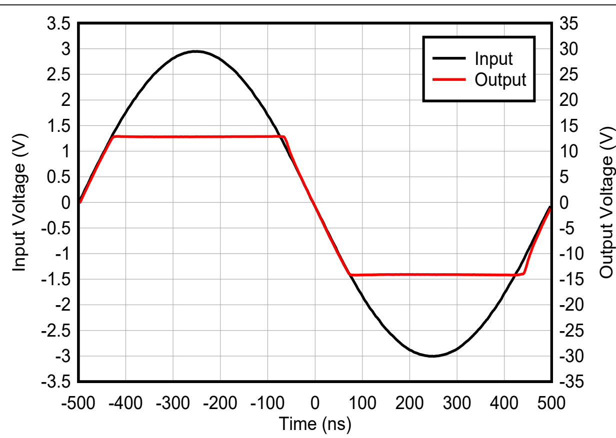
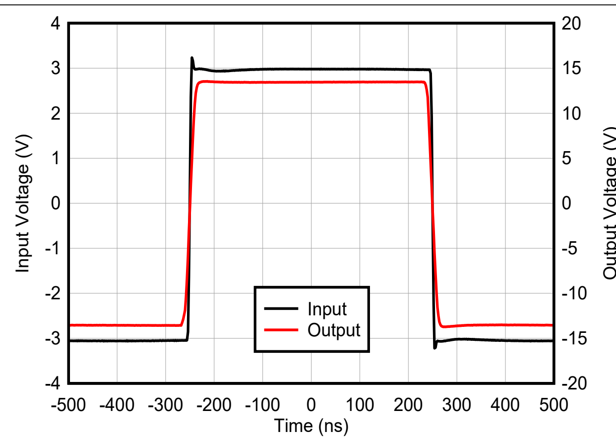


Figure 6-26. Common-Mode Rejection Ratio vs Input Common-Mode Range



G = 5, R_F = 499Ω, R_G = 124Ω, V_S = 30V, input frequency = 1MHz

Figure 6-27. Overdrive Recovery



G = 5, R_F = 499Ω, R_G = 124Ω, V_S = 30V, input frequency = 1MHz

Figure 6-28. Overdrive Recovery

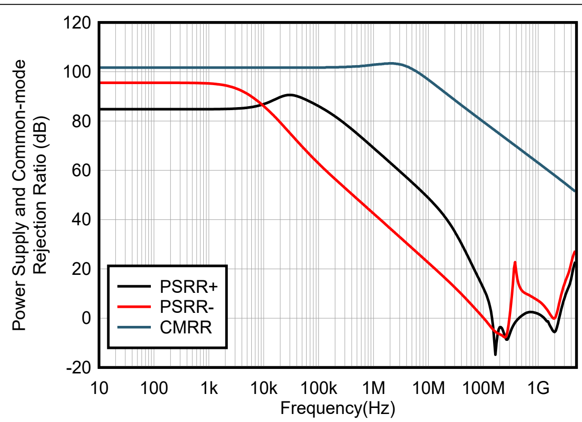


Figure 6-29. Rejection Ratio vs Frequency

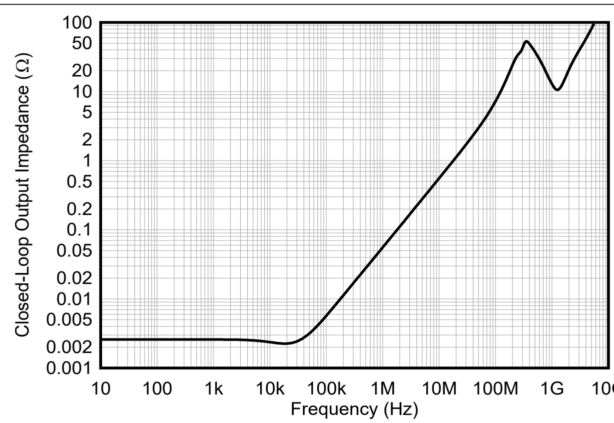


Figure 6-30. Output Impedance vs Frequency

7 Parameter Measurement Information

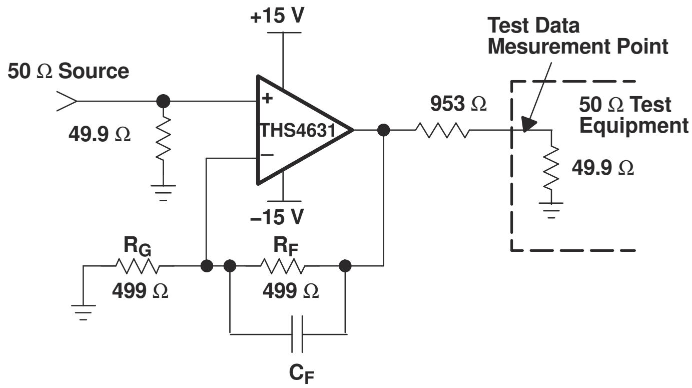


Figure 7-1. AC Measurement Configuration

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The THS4631 is a high-speed, FET-input operational amplifier. The combination of high gain bandwidth product of 210MHz, high slew rate of 1000V/µs, and trimmed dc precision makes this device an excellent design option. This device is a great choice for a wide variety of applications, including test and measurement, optical monitoring, transimpedance gain circuits, and high-impedance buffers. The applications section of the data sheet discusses these particular applications, in addition to general information about the device and device specific features.

8.1.1 Transimpedance Fundamentals

FET-input amplifiers are often used in transimpedance applications because of the amplifiers extremely high input impedance. A transimpedance block accepts a current as an input and converts this current to a voltage at the output. The high-input impedance associated with FET-input amplifiers minimizes errors in this process caused by the input bias currents, IIB, of the amplifier.

8.1.2 Noise Analysis

High slew rate, unity gain stable, voltage-feedback operational amplifiers usually achieve high slew rate at the expense of a higher-input noise voltage. However, the 7nV/√Hz input voltage noise for the THS4631 is much lower than comparable amplifiers while achieving high slew rates. The input-referred voltage noise and the input-referred current noise term combine to give low output noise under a wide variety of operating conditions. Figure 8-1 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or fA/√Hz.

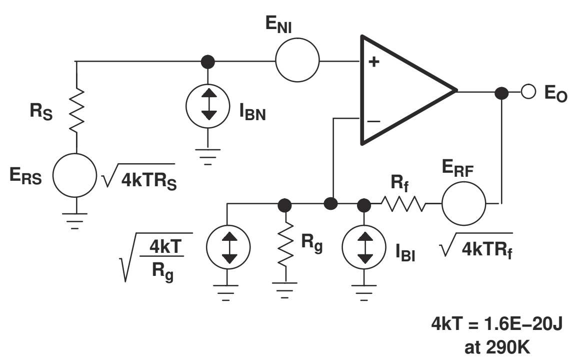


Figure 8-1. Noise Analysis Model

The total output noise voltage is computed as the square root of all square output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 8-1.

$$E_O = \sqrt{\left(E_{NI}{}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_fNG} \quad (1)$$

Equation 2 shows that dividing this expression by the noise gain [NG = (1+ R_f/R_g)] gives the equivalent input-referred spot noise voltage at the noninverting input.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \qquad (2)$$

High resistor values can dominate the total equivalent input-referred noise. Use a 3kΩ source-resistance (R_S) value to add a voltage noise term of approximately 7nV/√Hz. This noise term is equivalent to the amplifier voltage noise term. Higher resistor values dominate the noise of the system. Although the THS4631 JFET input stage is advantageous for high-source impedance because of the low-bias currents, the system noise and bandwidth is limited by a high-source (R_S) impedance.

8.2 Typical Applications

8.2.1 Wideband Photodiode Transimpedance Amplifier

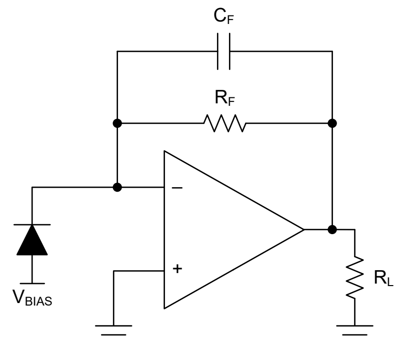


Figure 8-2. Wideband Photodiode Transimpedance Amplifier

8.2.1.1 Detailed Design Procedure

8.2.1.1.1 Designing the Transimpedance Circuit

Typically, design of a transimpedance circuit is driven by the characteristics of the current source that provides the input to the gain block. A photodiode is the most common example of a capacitive current source that interfaces with a transimpedance gain block. Continuing with the photodiode example, the system designer traditionally chooses a photodiode based on two opposing criteria: speed and sensitivity. Faster photodiodes cause a need for faster gain stages, and more sensitive photodiodes require higher gains to develop appreciable signal levels at the output of the gain stage.

These parameters affect the design of the transimpedance circuit in a few ways. First, the speed of the photodiode signal determines the required bandwidth of the gain circuit. Second, the required gain, based on the sensitivity of the photodiode, limits the bandwidth of the circuit. Third, the larger capacitance associated with a more sensitive signal source also detracts from the achievable speed of the gain block. The dynamic range of the input signal also places requirements on the amplifier dynamic range. Knowledge of the source output current levels, coupled with a desired voltage swing on the output, dictates the value of the feedback resistor, R_F. The transfer function from input to output is $V_{OUT} = I_{IN}R_F$.

The large gain-bandwidth product of the THS4631 provides the capability for simultaneously achieving both high transimpedance gain, wide bandwidth, high slew rate, and low noise. In addition, the high-power supply rails provide the potential for a very wide dynamic range at the output, allowing for the use of input sources which possess wide dynamic range. The combination of these characteristics makes the THS4631 an excellent design option for systems that require transimpedance amplification of wideband, low-level input signals. Figure 8-2 shows a standard transimpedance circuit.

As indicated, the current source typically sets the requirements for gain, speed, and dynamic range of the amplifier. For a given amplifier and source combination, achievable performance is dictated by the following parameters: amplifier gain-bandwidth product, amplifier input capacitance, source capacitance, transimpedance gain, amplifier slew rate, and amplifier output swing. From this information, the best case performance of a transimpedance circuit using a given amplifier is determined. Best case is defined here as providing the required transimpedance gain with a maximized flat frequency response.

For the circuit shown in Figure 8-2, all but one of the design parameters is known; the feedback capacitor (C_F) must still be determined. Proper selection of the feedback capacitor prevents an unstable design, controls pulse response characteristics, provides maximized flat transimpedance bandwidth, and limits broadband integrated noise. The maximized flat frequency response results with C_F calculated as shown in Equation 3:

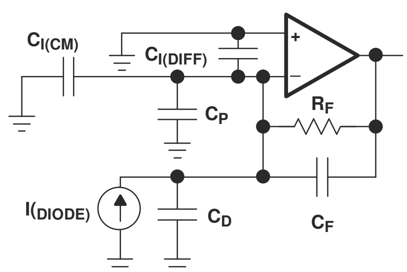
$$C_F = \frac{\frac{1}{\pi R_F GBP} + \sqrt{\left(\frac{1}{\pi R_F GBP}\right)^2 + \frac{4C_S}{\pi R_F GBP}}}{2} \tag{3}$$

where

- C_F is the feedback capacitor
- R_F is the feedback resistor
- C_F is the feedback capacitor
- R_F is the feedback resistor
- C_S is the total source capacitance (including amplifier input capacitance and parasitic capacitance at the inverting node)
- GBP is the gain-bandwidth product of the amplifier in hertz

After the feedback capacitor has been selected, the transimpedance bandwidth is calculated with Equation 4.

$$F_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F \left(C_S + C_F\right)}} \tag{4}$$



$C_S = C_{I(CM)} + C_{I(DIFF)} + C_P + C_D$

Note: The total source capacitance is the sum of several distinct capacitances.

Figure 8-3. Transimpedance Analysis Circuit

where

- $C_{I(CM)}$ is the common-mode input capacitance
- $C_{I(DIFF)}$ is the differential input capacitance
- C_D is the diode capacitance
- C_P is the parasitic capacitance at the inverting node

The feedback capacitor provides a pole in the noise gain of the circuit, counteracting the zero in the noise gain caused by the source capacitance. The pole is set such that the noise gain achieves a 20dB-per-decade rate of closure with the open-loop gain response of the amplifier, resulting in a stable circuit. As indicated, Equation 3 provides the feedback capacitance for maximized flat bandwidth. Reduction in the value of the feedback capacitor can increase the signal bandwidth, but the signal bandwidth increase occurs at the expense of peaking in the ac response.

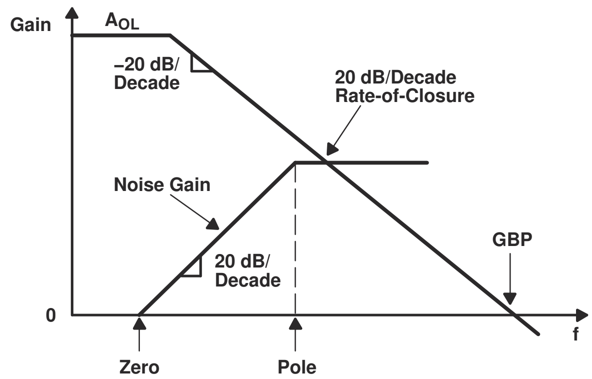


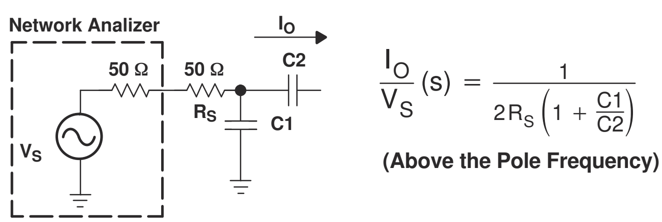
Figure 8-4. Transimpedance Circuit Bode Plot

The performance of the THS4631 has been measured for a variety of transimpedance gains with a variety of source capacitances. The achievable bandwidths of the various circuit configurations are summarized numerically in Table 8-1. Figure 8-6, Figure 8-7, and Figure 8-8 present the frequency responses.

Be aware the feedback capacitances do not correspond exactly with the values predicted by the equation. The capacitances have been tuned to account for the parasitic capacitance of the feedback resistor (typically 0.2pF for 0805 surface mount devices) as well as the additional capacitance associated with the printed circuit board (PCB). Use this equation as a starting point for the design, with final values for C_F optimized in the laboratory.

8.2.1.1.2 Measuring Transimpedance Bandwidth

While there is no substitute for measuring the performance of a particular circuit under the exact conditions that are used in the application, the complete system environment often makes measuring harder. Measuring the frequency response of a transimpedance circuit is difficult with traditional laboratory equipment because the circuit requires a current as an input rather than a voltage. Also, the capacitance of the current source has a direct effect on the frequency response. A simple interface circuit can be used to emulate a capacitive current source with a network analyzer. With this circuit, transimpedance bandwidth measurements are simplified, making amplifier evaluation easier and faster.



Note: The interface network creates a capacitive, constant current source from a network analyzer and properly terminates the network analyzer at high frequencies.

Figure 8-5. Emulating a Capacitive Current Source With a Network Analyzer

The transconductance transfer function of the interface circuit is:

$$\frac{I_O}{V_S}(s) = \frac{\dfrac{s}{2R_S\left(1+\dfrac{C1}{C2}\right)}}{s + \dfrac{1}{2R_S(C1+C2)}} \tag{5}$$

The transfer function contains a zero at dc and a pole at $\frac{1}{2R_S(C1 + C2)}$.

The transconductance is constant for signal source frequencies greater than the pole frequency, $\frac{1}{2R_S\left(1+\frac{C1}{C2}\right)}$, providing a controllable ac current source. This circuit also properly terminates the network analyzer with 50Ω at high frequencies. The second requirement for this current source is to provide the desired output impedance, emulating the output impedance of a photodiode or other current source. The output impedance of this circuit is given by:

$$Z_O(s) = \frac{C1 + C2}{C1 \times C2}\left[\frac{s + \frac{1}{2R_S(C1+C2)}}{s\left(s + \frac{1}{2R_S C1}\right)}\right] \tag{6}$$

Assuming C1 >> C2, the equation reduces to: $Z_O \approx \frac{1}{sC2}$, giving the appearance of a capacitive source at a higher frequency.

When selecting capacitor values, the designer must consider two requirements. First, C2 represents the anticipated capacitance of the true source. Second, C1 is chosen so that the corner frequency of the transconductance network is much less than the transimpedance bandwidth of the circuit. Choosing this corner frequency properly leads to more accurate measurements of the transimpedance bandwidth. If the interface-circuit corner frequency is too close to the bandwidth of the circuit, determining the power level in the flat band is difficult. A decade or more of flat bandwidth provides a good basis for determining the proper transimpedance bandwidth.

8.2.1.1.3 Summary of Key Decisions in Transimpedance Design

The following is a simplified process for basic transimpedance circuit design. This process gives a start to the design process, though the process does ignore some aspects that can be critical to the circuit.

- **STEP 1:** Determine the capacitance of the source.
- **STEP 2:** Calculate the total source capacitance, including the amplifier input capacitance, $C_{I(CM)}$ and $C_{I(DIFF)}$.
- **STEP 3:** Determine the magnitude of the possible current output from the source, including the minimum signal current anticipated and maximum signal current anticipated.
- **STEP 4:** Choose a feedback resistor value such that the input current levels create the desired output signal voltages, and verify that the output voltages can accommodate the dynamic range of the input signal.
- **STEP 5:** Calculate the optimum feedback capacitance using Equation 3.
- **STEP 6:** Calculate the bandwidth given the resulting component values.
- **STEP 7:** Evaluate the circuit to determine if all design goals are satisfied.

8.2.1.1.4 Selection of Feedback Resistors

Feedback-resistor selection can have a significant effect on the performance of the THS4631 in a given application, especially in configurations with low closed-loop gain. If the amplifier is configured for unity gain, connect the output directly to the inverting input. Any resistance between these two points interacts with the input capacitance of the amplifier and causes an additional pole in the frequency response. For non-unity gain configurations, low resistances are desirable for a flat frequency response. However, do not load the amplifier too heavily with the feedback network if large output signals are expected. In most cases, a tradeoff is made between the frequency response characteristics and the loading of the amplifier. For a gain of 2, a 499Ω feedback resistor is the recommended operating point from both perspectives. Resistor values that are too large subject the THS4631 to oscillation problems. For example, an inverting amplifier configuration with a 5kΩ gain resistor and a 5kΩ feedback resistor develops an oscillation due to the interaction of the large resistors with the input capacitance. In low-gain configurations, avoid feedback resistors that are too large or anticipate using an external compensation scheme to stabilize the circuit. Using a simple capacitor in parallel with the feedback resistor makes the amplifier more stable (see also the *Typical Characteristics* graphs).

Table 8-1. Transimpedance Performance Summary for Various Configurations

SOURCE CAPACITANCE (PF)	TRANSIMPEDANCE GAIN (Ω)	FEEDBACK CAPACITANCE (PF)	–3dB FREQUENCY (MHZ)
18	10k	2	15.8
18	100k	0.5	3
18	1M	0	1.2
47	10k	2.2	8.4
47	100k	0.7	2.1
47	1M	0.2	0.52
100	10k	3	5.5
100	100k	1	1.4
100	1M	0.2	0.37

8.2.1.2 Application Curves

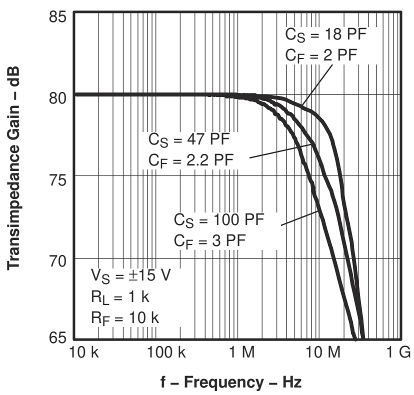


Figure 8-6. 10kΩ Transimpedance Responses

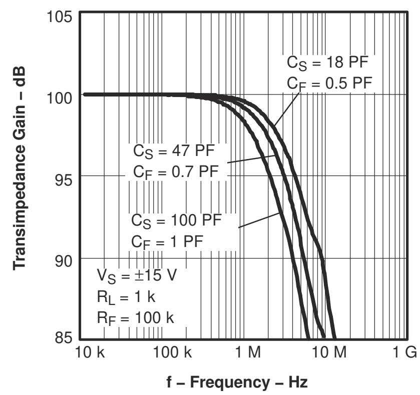


Figure 8-7. 100kΩ Transimpedance Responses

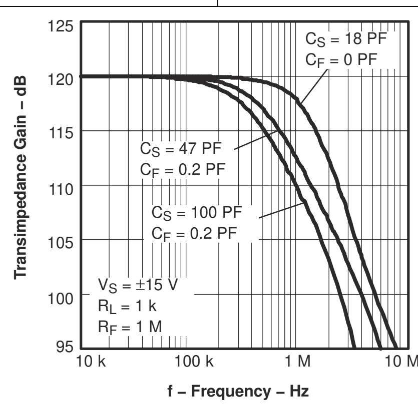
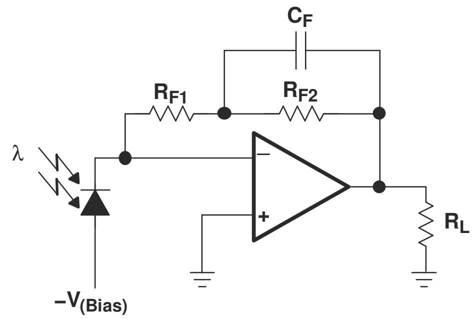


Figure 8-8. 1MΩ Transimpedance Responses

8.2.2 Alternative Transimpedance Configurations

Other transimpedance configurations are possible. The following three possibilities are shown.

The first configuration is a slight modification of the basic transimpedance circuit. By splitting the feedback resistor, the feedback capacitor value becomes more manageable and easier to control. This type of compensation scheme is useful when the feedback capacitor required in the basic configuration becomes so small that the parasitic effects of the board and components begin to dominate the total feedback capacitance. By reducing the resistance across the capacitor, the capacitor value can be increased. This compensation scheme mitigates the dominance of the parasitic effects.

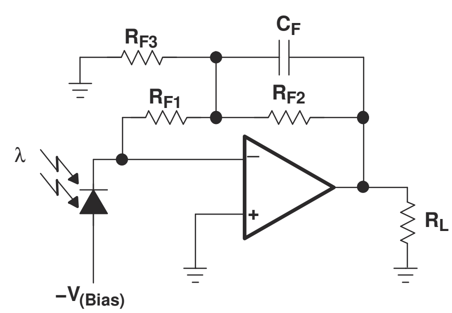


Note: Splitting the feedback resistor enables use of a larger, more manageable feedback capacitor.

Figure 8-9. Alternative Transimpedance Configuration 1

The second configuration uses a resistive T-network to achieve high transimpedance gains using relatively small resistor values. This topology is useful when the desired transimpedance gain exceeds the value of available resistors. The transimpedance gain is given by Equation 7.

$$R_{EQ} = R_{F1}\left(1 + \frac{R_{F2}}{R_{F3}}\right) \tag{7}$$

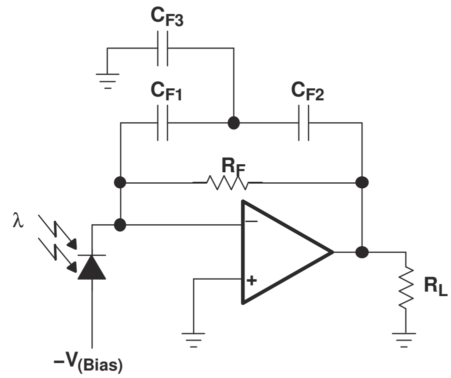


Note: A resistive T-network enables high transimpedance gain with reasonable resistor values.

Figure 8-10. Alternative Transimpedance Configuration 2

The third configuration uses a capacitive T-network to achieve fine control of the compensation capacitance. The capacitor CF3 can be used to tune the total effective feedback capacitance to a fine degree. This circuit behaves the same as the basic transimpedance configuration, with the effective CF given by Equation 8.

$$\frac{1}{C_{FEQ}} = \frac{1}{C_{F1}}\left(1 + \frac{C_{F3}}{C_{F2}}\right) \tag{8}$$



Note: A capacitive T-network enables fine control of the effective feedback capacitance using relatively large capacitor values.

Figure 8-11. Alternative Transimpedance Configuration 3

8.3 Power Supply Recommendations

8.3.1 Slew-Rate Performance With Varying Input-Step Amplitude and Rise-and-Fall Time

Some FET input amplifiers exhibit the peculiar behavior of having a larger slew rate when presented with smaller input voltage steps and slower edge rates due to a change in bias conditions in the input stage of the amplifier under these circumstances. This phenomena is most commonly seen when FET input amplifiers are used as voltage followers. This behavior is typically undesirable, and the THS4631 has been designed to avoid these issues. Larger amplitudes lead to higher slew rates, as anticipated, and fast edges do not degrade the slew rate of the device. The high slew rate of the THS4631 allows for improved SFDR and THD performance, especially noticeable at frequencies greater than 5MHz.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Printed-Circuit Board (PCB) Layout Techniques for High Performance

Achieving optimized performance with high-frequency amplifier-like devices in the THS4631 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins can be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes can be unbroken elsewhere on the board.
- Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1µF and 100pF decoupling capacitors. At the device pins, avoid routing ground and power planes in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Decouple the power supply connections with these capacitors. Use larger (6.8µF or more) tantalum decoupling capacitors, effective at lower frequency, on the main supply pins. Place these decoupling capacitors somewhat farther from the device and share the capacitors among several devices in the same area of the PCB.
- Careful selection and placement of external components preserve the high-frequency performance of the THS4631. Use very low reactance type resistors. Surface-mount resistors work best and allow a tighter overall layout. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. The output pin and inverting input pins are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Place other network components, such as input termination resistors, close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 2.0kΩ, this parasitic capacitance can add a pole, a zero that can effect circuit operation, or both. Keep resistor values as low as possible, consistent with load driving considerations.
- Make connections to other wideband devices on the board with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4pF) do not typically need an RS because the THS4631 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an RS are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion (see also the distortion versus load plots). With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4631 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: set this total effective impedance to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. Source-end-only termination does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Do not socket a high-speed part such as the THS4631. The additional lead length and pin-to-pin capacitance introduced by the socket creates a troublesome parasitic network that makes a stable and smooth frequency response almost impossible to achieve. Best results are obtained by soldering the THS4631 part directly onto the board.

8.4.1.2 PowerPAD Design Considerations

The THS4631 is available in a thermally-enhanced PowerPAD integrated circuit family of packages. These packages are constructed using a downset leadframe upon which the die is mounted; see also Figure 8-12 (a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see also Figure 8-12 (c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the mechanical methods of dissipating heat.

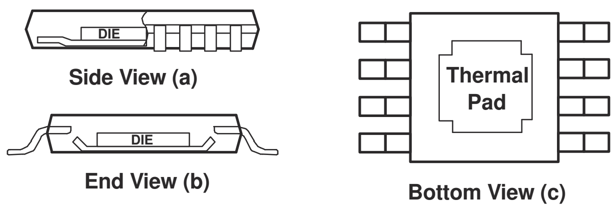


Figure 8-12. Views of Thermally Enhanced Package

8.4.1.3 PowerPAD PCB Layout Considerations

1. Figure 8-14 and Figure 8-15 show the PCB with a top-side etch pattern. There must be etch for the leads and for the thermal pad.
2. Place the recommended number of vias in the area of the thermal pad. These vias must be 10 mils in diameter. Keep the vias small so that solder wicking through the vias is not a problem during reflow.
3. Place additional vias anywhere along the thermal plane outside of the thermal pad area. Additional vias help dissipate the heat generated by the THS4631. These additional vias can be larger than the 10-mil diameter vias directly under the thermal pad because the vias are not in the thermal pad area to be soldered; therefore, wicking is not a problem.
4. Connect all thermal pad vias to the internal ground plane. Although the PowerPAD is electrically isolated from all pins and the active circuitry, connection to the ground plane is recommended to improve thermal performance. Ground planes are typically the largest copper area on the PCB and help to move heat across the PCB. After the heat spreads across the PCB, airflow can move across a larger surface area to remove heat from the system.
5. When connecting these vias to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing heat transfer, which makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the THS4631 PowerPAD package must make a connection to the internal ground plane with a complete connection around the entire circumference of the via.
6. For the top-side solder mask, leave the terminals of the package and the thermal pad area with via holes exposed. The bottom-side solder mask must cover the via holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the device terminals.
8. With these preparatory steps in place, the device is simply placed in position and run through the solder reflow operation as any standard surface-mount component.

Following these steps results in a device that is properly installed.

8.4.1.4 Power Dissipation and Thermal Considerations

To maintain maximum output capabilities, the THS4631 does not incorporate automatic thermal shutoff protection. The designer must take care that the design does not violate the absolute maximum junction temperature of the device. Failure can result if the absolute maximum junction temperature of 150°C is exceeded. For best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade. The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package is calculated using Equation 9.

$$P_{D\,max} = \frac{T_{max} - T_A}{\theta_{JA}} \tag{9}$$

where:

- P_{Dmax} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junction temperature (°C).
- T_A is the ambient temperature (°C).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

Note

For systems where heat dissipation is more critical, the THS4631 is offered in an 8-pin HVSSOP with PowerPAD package and an 8-pin HSOIC with PowerPAD package with better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in Figure 8-13 for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced previously, and detailed in the *PowerPAD™ Thermally Enhanced Package* application note. Figure 8-13 also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially, which can cause serious heat and performance issues. Always solder the PowerPAD to the PCB for optimized performance.

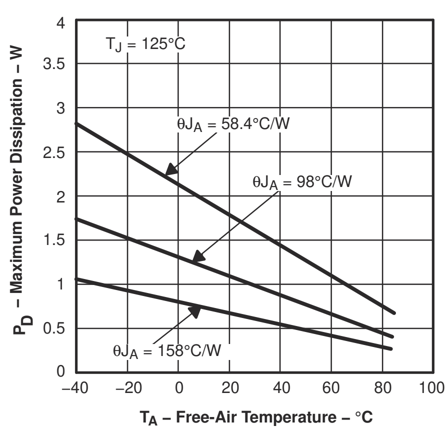


Figure 8-13. Maximum Power Dissipation vs Ambient Temperature

Results are with no air flow and PCB size = 3" × 3".

- θ_{JA} = 58.4°C/W for the 8-pin HVSSOP with PowerPAD (DGN).
- θ_{JA} = 98°C/W for the 8-pin SOIC high-K test PCB (D).
- θ_{JA} = 158°C/W for the 8-pin HVSSOP with PowerPAD, without solder.

When determining whether or not the device satisfies the maximum power dissipation requirement, consider not only quiescent power dissipation, but also dynamic power dissipation. Often, this dynamic dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

8.4.2 Layout Example

Although there are many ways to properly dissipate heat in the PowerPAD integrated circuit package, the following steps illustrate the recommended approach.

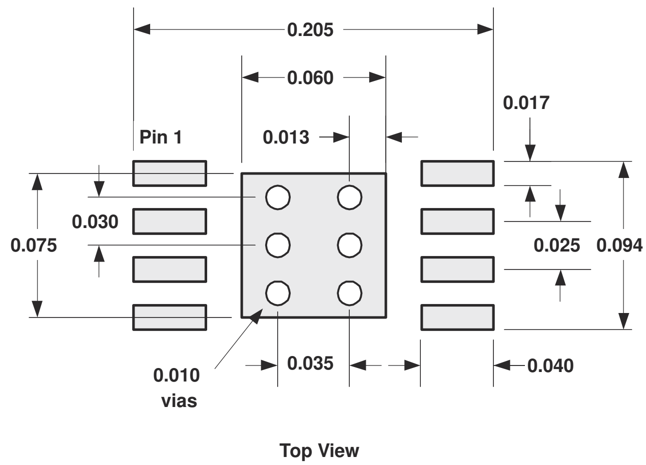


Figure 8-14. DGN PowerPAD™ Integrated Circuit Package PCB Etch and Via Pattern

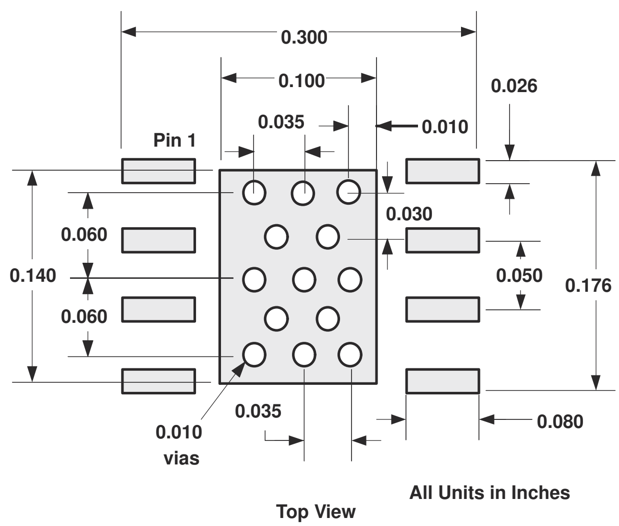


Figure 8-15. DDA PowerPAD™ Integrated Circuit Package PCB Etch and Via Pattern

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Design Tools Evaluation Fixture, Spice Models, and Applications Support

Texas Instruments is committed to providing customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS4631 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. The board layers are provided in Figure 9-1, Figure 9-2, and Figure 9-3. The bill of materials for the evaluation board is provided in Table 9-1.

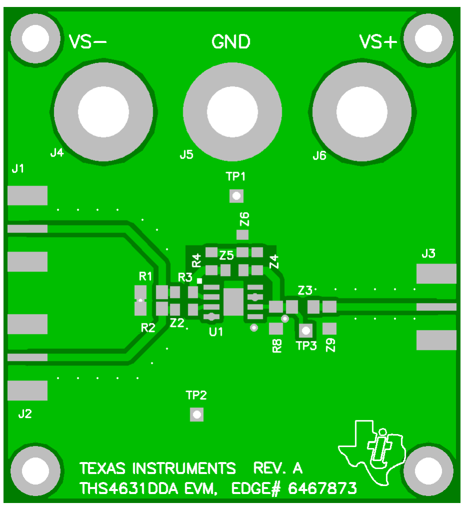


Figure 9-1. EVM Top Layer

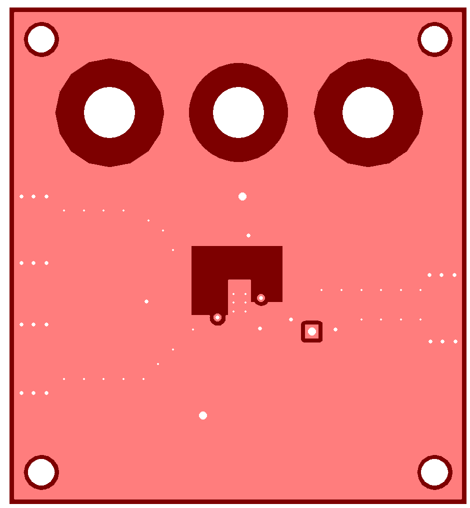


Figure 9-2. EVM Layers 2 and 3 Ground

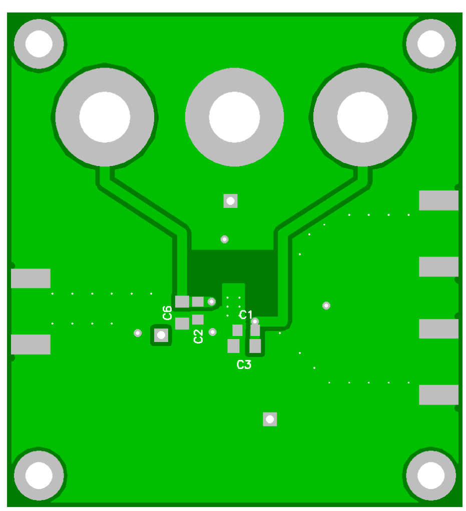


Figure 9-3. EVM Bottom Layer

9.1.1.1 Bill of Materials

Table 9-1. THS4631DDA EVM Bill of Materials (BOM)

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER PART NUMBER(1)
1	CAP, 2.2µF, CERAMIC, X5R, 25V	1206	C3, C6	2	(AVX) 12063D225KAT2A
4	CAP, 0.1µF, CERAMIC, X7R, 50V	0805	C1, C2	2	(AVX) 08055C104KAT2A
	OPEN	0805	R4, Z4, Z6	3	
6	RESISTOR, 0 OHM, 1/8 W	0805	Z2	1	(KOA) RK73Z2ATTD
7	RESISTOR, 499 OHM, 1/8 W, 1%	0805	R3, Z5	2	(KOA) RK73H2ATTD4990F
8	OPEN	1206	R8, Z9	2	
9	RESISTOR, 0 OHM, 1/4 W	1206	R1	1	(KOA) RK73Z2BLTD
10	RESISTOR, 49.9 OHM, 1/4 W, 1%	1206	R2	1	(KOA) RK73H2BLTD49R9F
11	RESISTOR, 953 OHM, 1/4 W, 1%	1206	Z3	1	(KOA) RK73H2BLTD9530F
13	CONNECTOR, SMA PCB JACK		J1, J2, J3	3	(JOHNSON) 142-0701-801
14	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J4, J5, J6	3	(SPC) 813
15	TEST POINT, BLACK		TP1, TP2	2	(KEYSTONE) 5001
	TEST POINT, RED		TP3	1	(KEYSTONE) 5000
16	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808
17	SCREW, PHILLIPS, 4-40, .250"			4	SHR-0440-016-SN
18	IC, THS4631		U1	1	(TI) THS4631DDA
19	BOARD, PRINTED CIRCUIT			1	(TI) EDGE # 6467873 Rev.A

(1) The manufacturer's part numbers are used for test purposes only.

9.1.1.2 EVM

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. SPICE is particularly helpful for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4631 is available through the Texas Instruments web site (www.ti.com). SPICE models help predict small-signal ac and transient performance under a wide variety of operating conditions. The models are not intended to model the distortion characteristics of the amplifier, nor do the models attempt to distinguish between the package types regarding small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file.

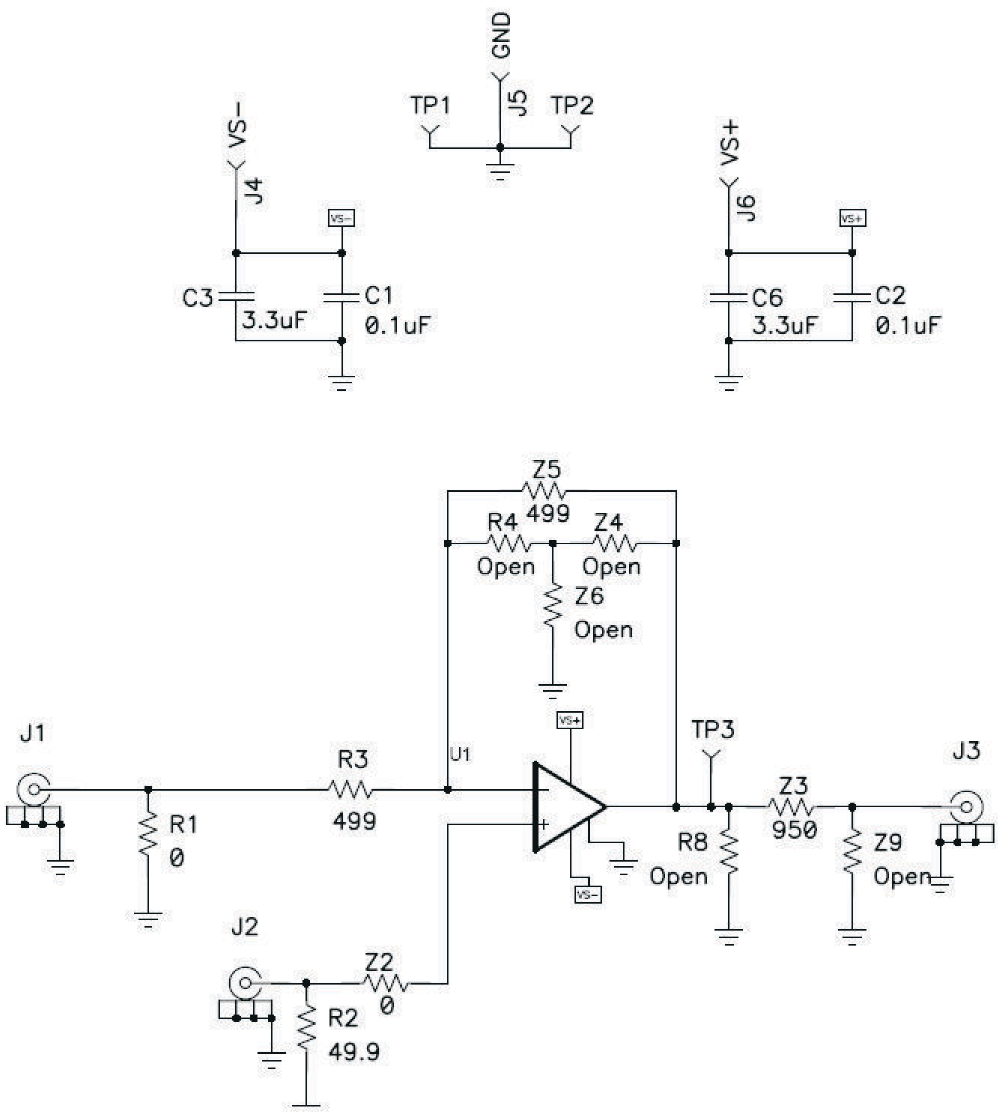


Figure 9-4. THS4631 EVM Schematic

9.1.1.3 EVM Warnings and Restrictions

This EVM must be operated within the input and output voltage ranges as specified in the following table.

Table 9-2. Input and Output Voltage Ranges

INPUT RANGE, V_{S+} TO V_{S-}	10V TO 30V
Input range, V_I	10V to 30V NOT TO EXCEED VS+ or VS–
Output range, V_O	10V to 30V NOT TO EXCEED VS+ or VS–

CAUTION

Exceeding the specified input range can cause unexpected operation, irreversible damage to the EVM, or both. If there are questions concerning the input range, contact a TI field representative before connecting the input power.

Applying loads outside of the specified output range can result in unintended operation, possible permanent damage to the EVM, or both. Consult the product data sheet or EVM user's guide (if available) before connecting any load to the EVM output. If there is uncertainty as to the load specification, contact a TI field representative.

During normal operation, some circuit components can have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, be aware that these devices can be very warm to the touch.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD Made Easy* application brief
- Texas Instruments, *PowerPAD Thermally Enhanced Package* technical brief
- Texas Instruments, *Noise Analysis of FET Transimpedance Amplifiers* application bulletin
- Texas Instruments, *Tame Photodiodes With Op Amp Bootstrap* application bulletin
- Texas Instruments, *Designing Photodiode Amplifier Circuits With OPA128*application bulletin
- Texas Instruments, *Photodiode Monitoring With Op Amps* application bulletin
- Texas Instruments, *Comparison of Noise Performance Between a FET Transimpedance Amplifier and a Switched Integrator* application bulletin

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2011) to Revision C (March 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................ 1
- Added *Device Information* table.. 1
- Changed OPA656 Voltage Noise from 7nV/√Hz to 6nV/√Hz and Slew Rate from 290V/µs to 400V/µs in *Related FET-Input-Amplifier Products* 2
- Added *Pin Functions* table..2
- Moved ESD ratings from *Absolute Maximum Ratings* to new *ESD Ratings*... 3
- Deleted 0°C to 70°C specifications from *Electrical Characteristics*...4
- Changed 0.1dB bandwidth flatness, with 8.2pF feedback capacitor, from 38MHz to 6MHz (Typ)....................4
- Added 0.1dB bandwidth flatness, with no 8.2pF feedback capacitor, with a value of 20MHz (Typ)..................4
- Changed Static output current (sourcing) from 80mA to 90mA (Min, –40°C to +125°C), 90mA to 120mA (Min, 25°C), 98mA to 180mA (Typ, 25°C)... 4
- Changed Static output current (sinking) from –80mA to –90mA (Max, –40°C to +125°C), –85mA to –120mA (Max, 25°C), –95mA to –180mA (Typ, 25°C).. 4
- Changed Quiescent current from 13mA to 14.5mA (Max, 25°C) and 14mA to 15mA (Max, –40°C to +125°C) 4
- Updated graphs with new silicon data to the latest standard.. 6
- Changed *Input Voltage vs Frequency* to *Input Voltage and Current Noise vs Frequency* 6
- Added current noise data to *Input Voltage and Current Noise vs Frequency* 6
- Deleted *Input Offset Current vs Temperature* 6
- Updated *Input Bias Current vs Temperature* to include input offset current..6
- Added typical C_F = 0pF to *Typical Characteristics* operating conditions... 6

Changes from Revision A (March 2005) to Revision B (August 2011) **Page**

- Changed the Tstg value in the *Absolute Maximum Ratings* table From: 65°C to 150°C To: –65°C to 150°C....3

Changes from Revision * (December 2004) to Revision A (March 2005) **Page**

- Changed the *Related FET Input Amplifier Products* table..1
- Changed the Differential input resistance value From: 109 || 6.5 To: 109 || 3.9..4
- Changed the Common-mode input resistance value From: 109 || 6.5 To: 109 || 3.9.. 4
- Changed Figure 8, *Third Order Harmonic Distortion vs Frequency* - From: R_L = 499Ω To R_F = 499Ω.............6
- Changed Figure 9, *Harmonic Distortion vs Output Voltage Swing* - From: R_L = 499Ω To R_F = 499Ω............... 6
- Added Figure 23, *Large Signal Transient Response* 6
- Added Figure 24, *Large Signal Transient Response* 6
- Added Figure 8-17, *THS4631 EVM Schematic* 26

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4631D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	4631
THS4631DDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	4631
THS4631DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	ADK
THS4631DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADK
THS4631DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4631

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

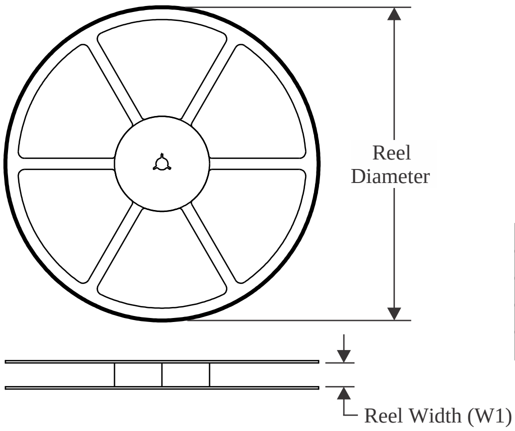
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

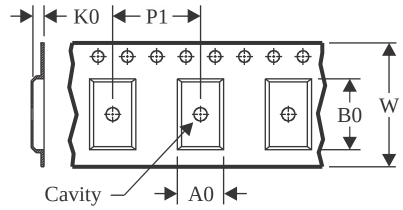
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

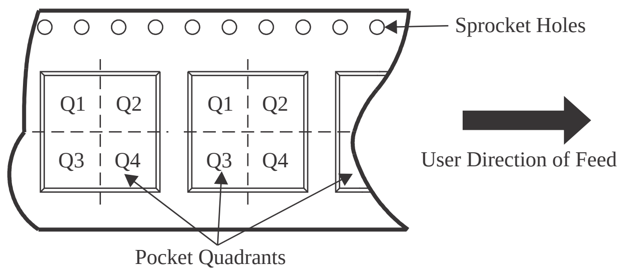


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

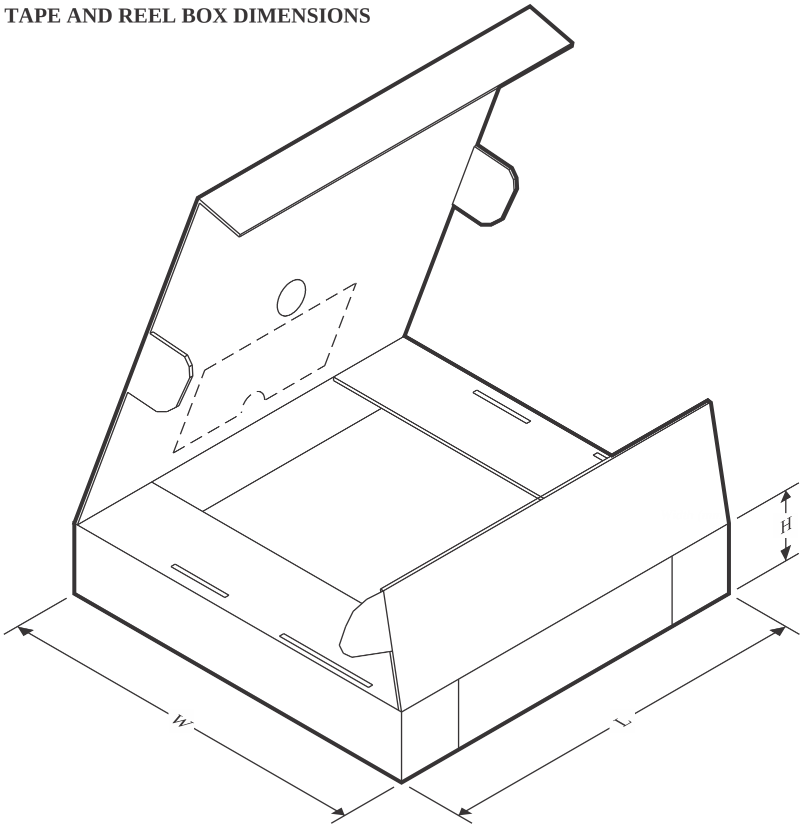
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4631DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4631DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4631DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

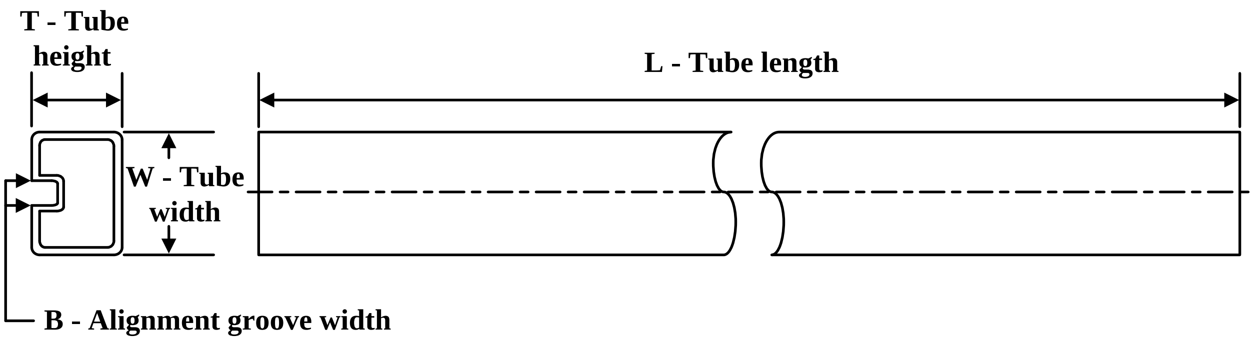
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4631DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4631DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4631DR	SOIC	D	8	2500	350.0	350.0	43.0

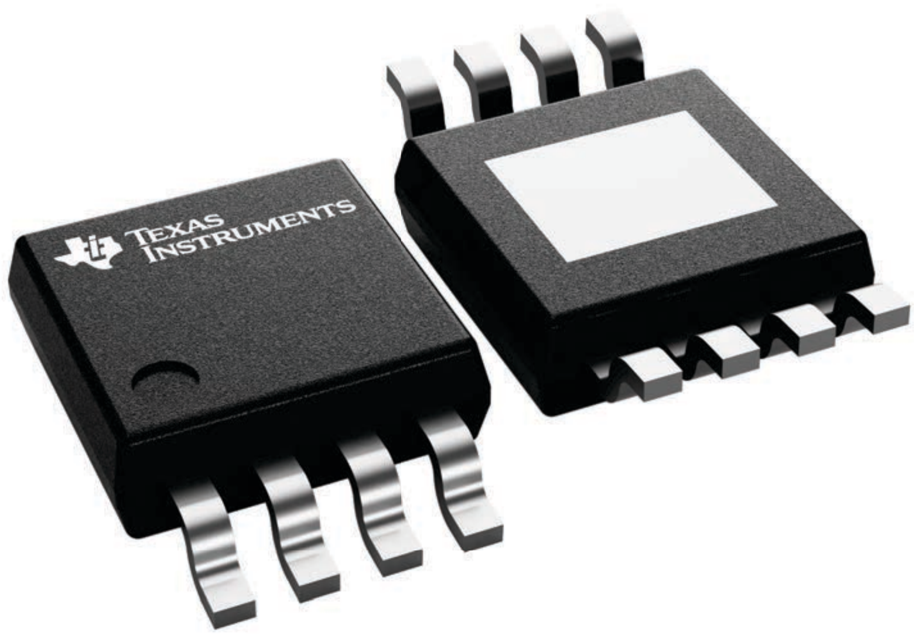
TUBE

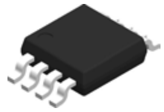


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4631DDA	DDA	HSOIC	8	75	505.46	6.76	3810	4

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

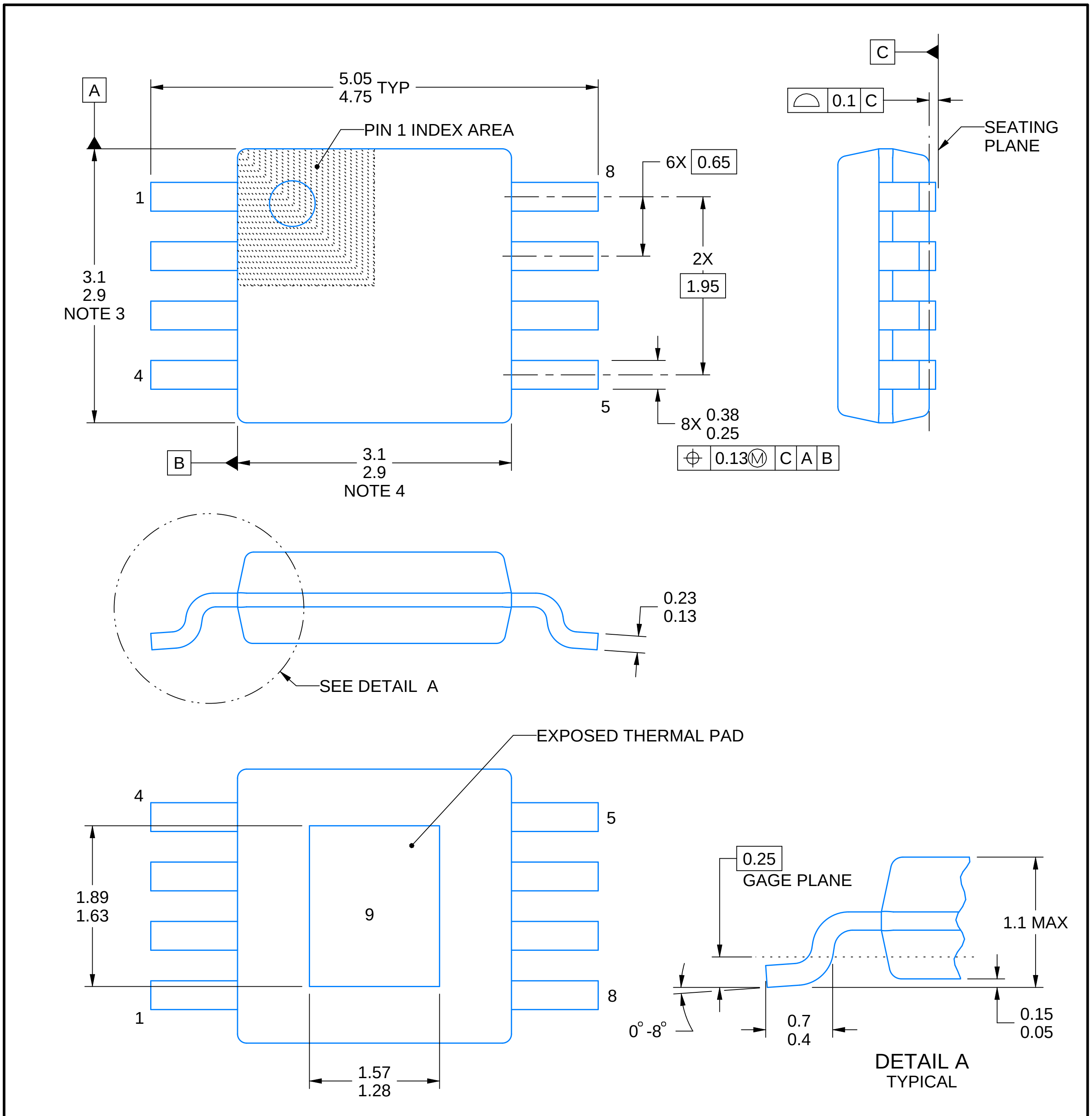




PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

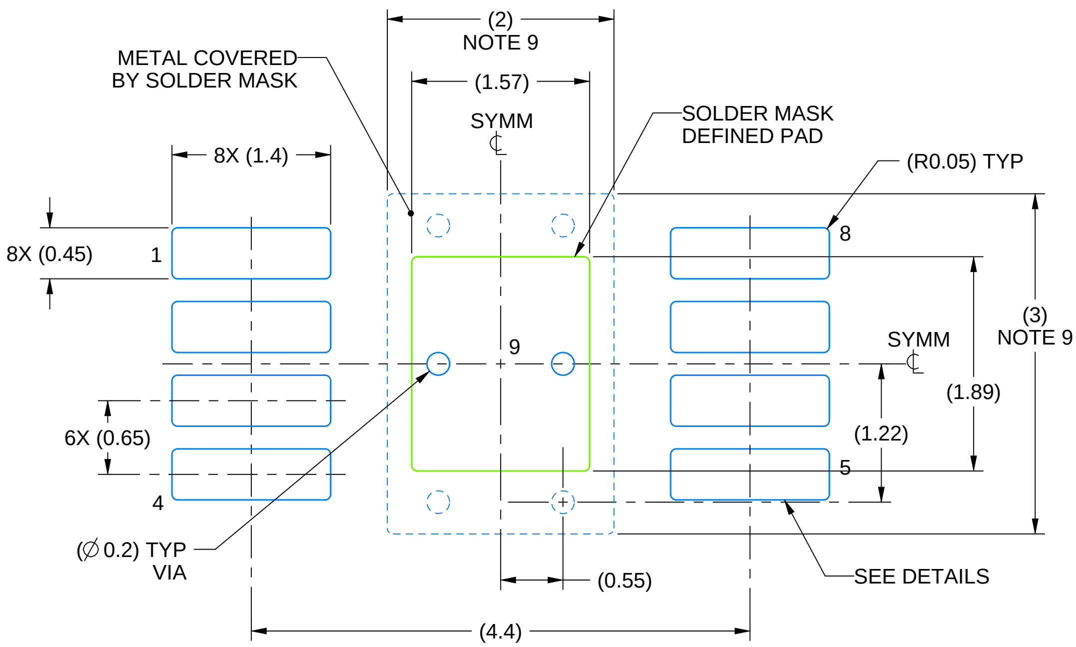


4225481/A 11/2019

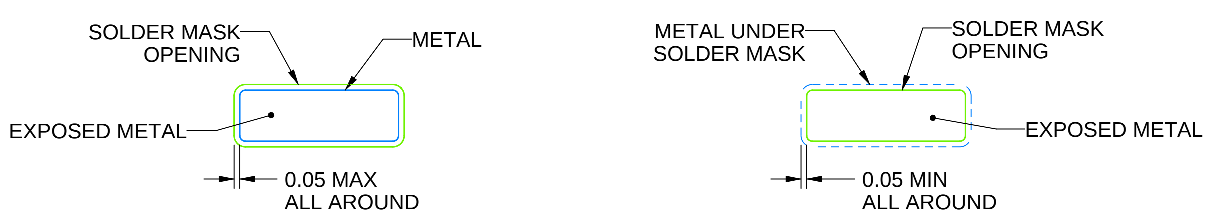
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

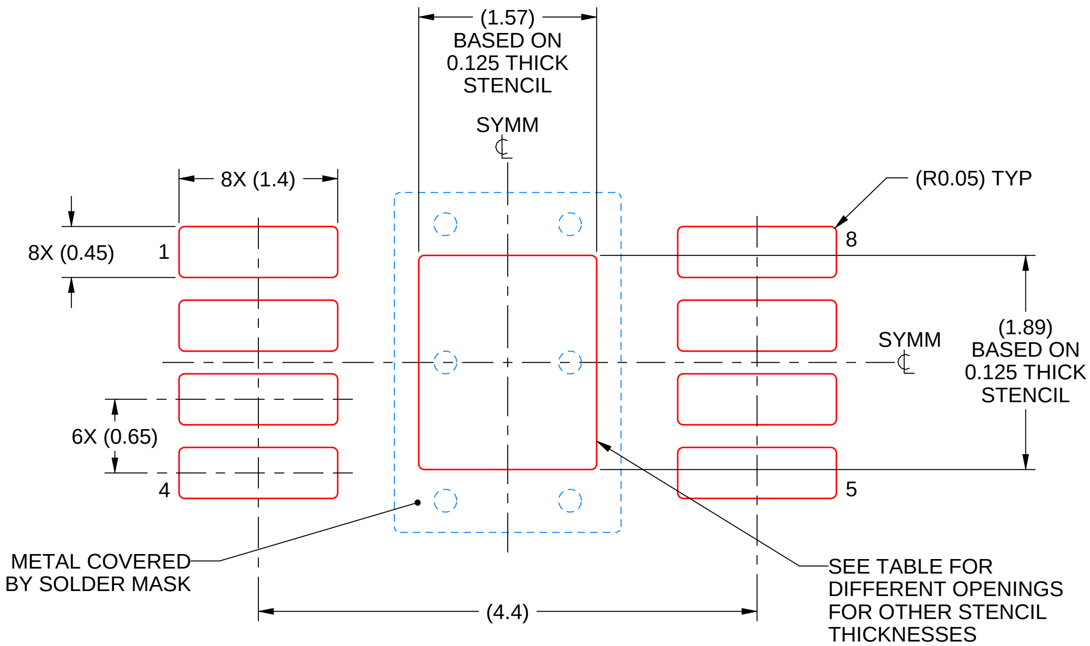
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



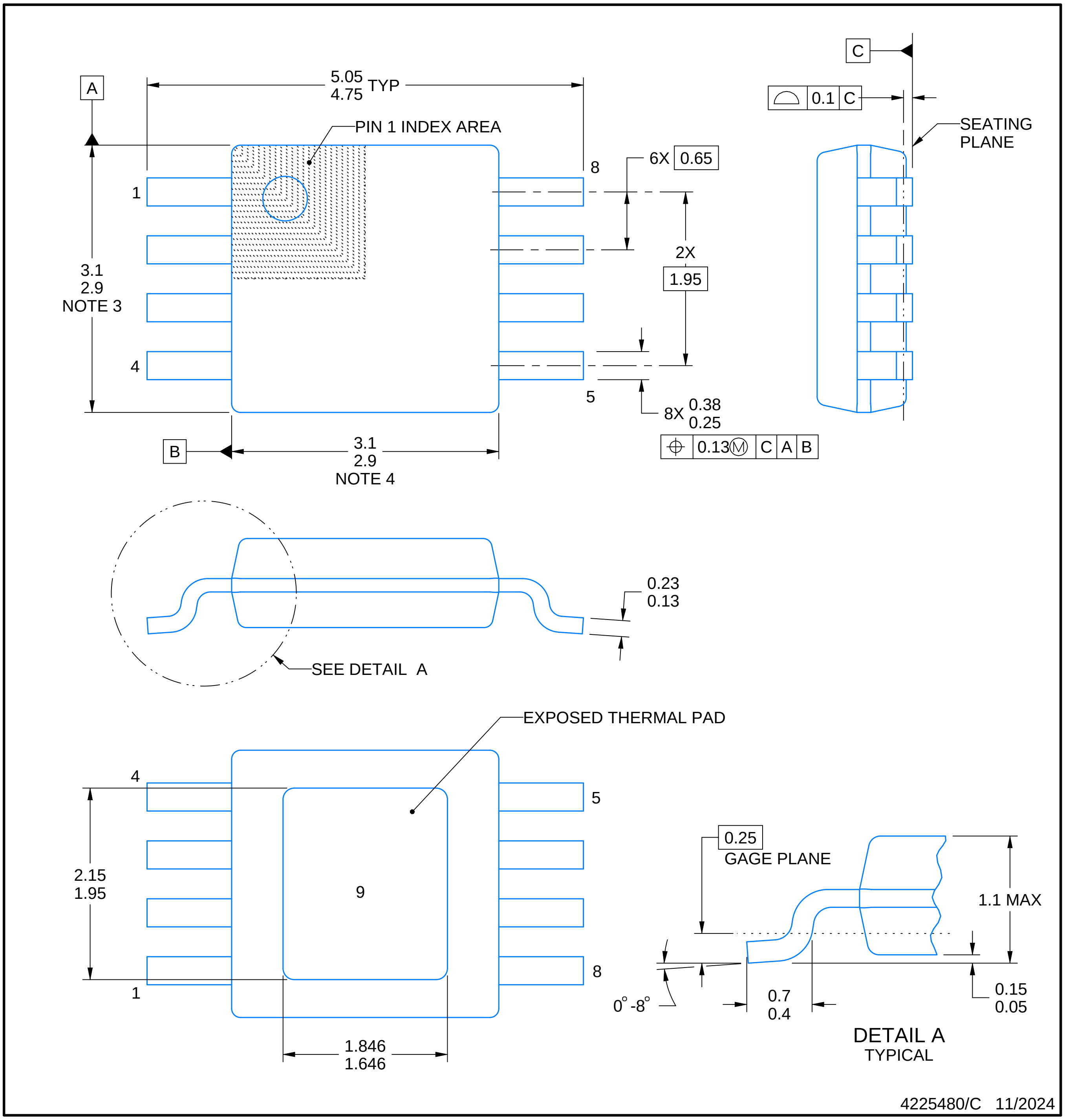
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

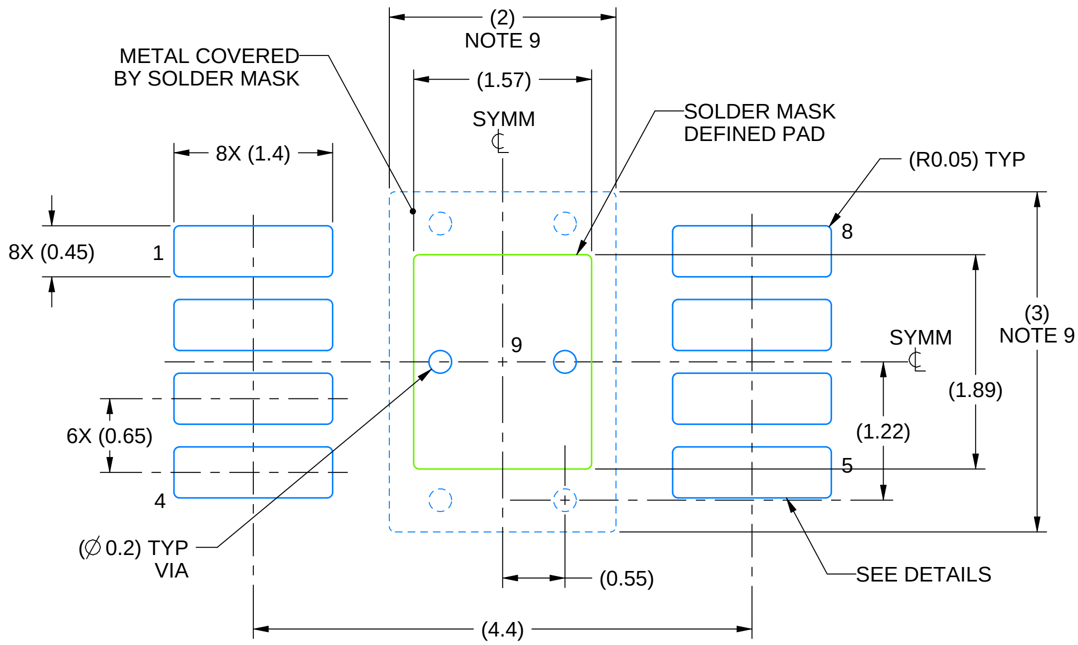


4225480/C 11/2024

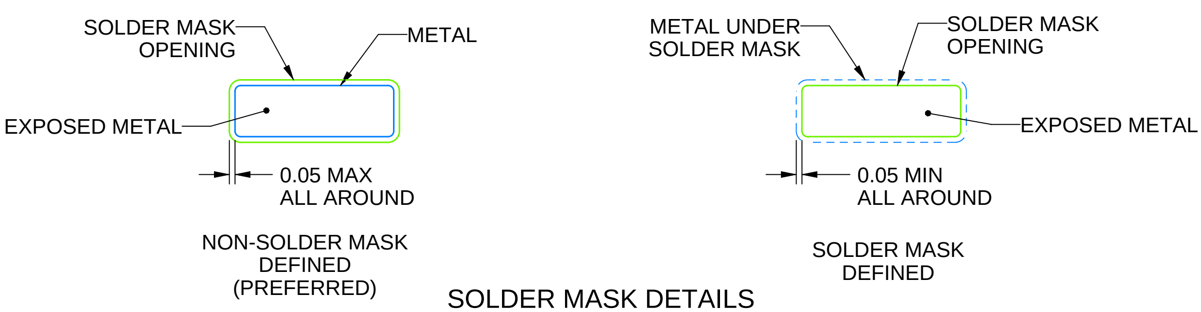
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

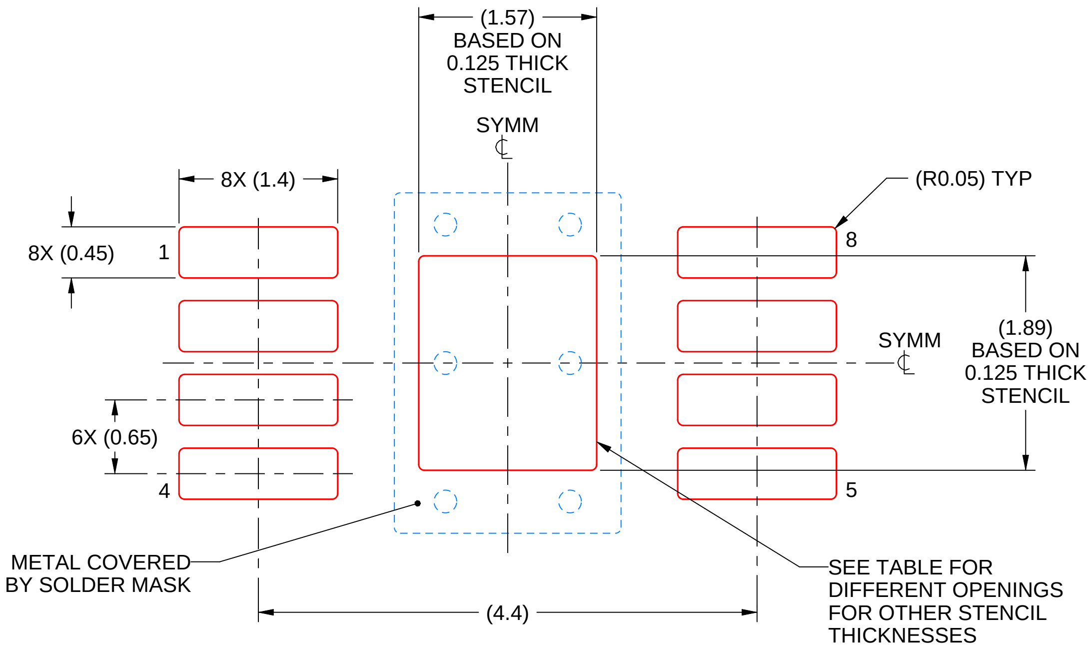


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



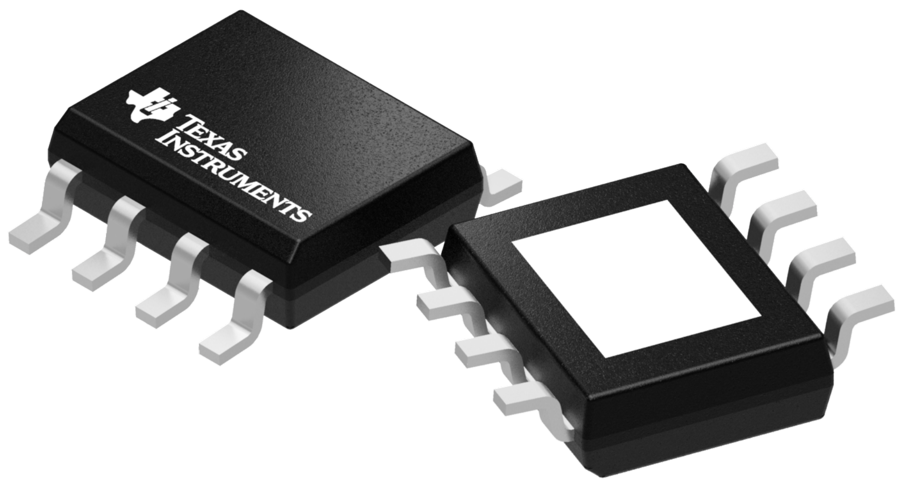
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

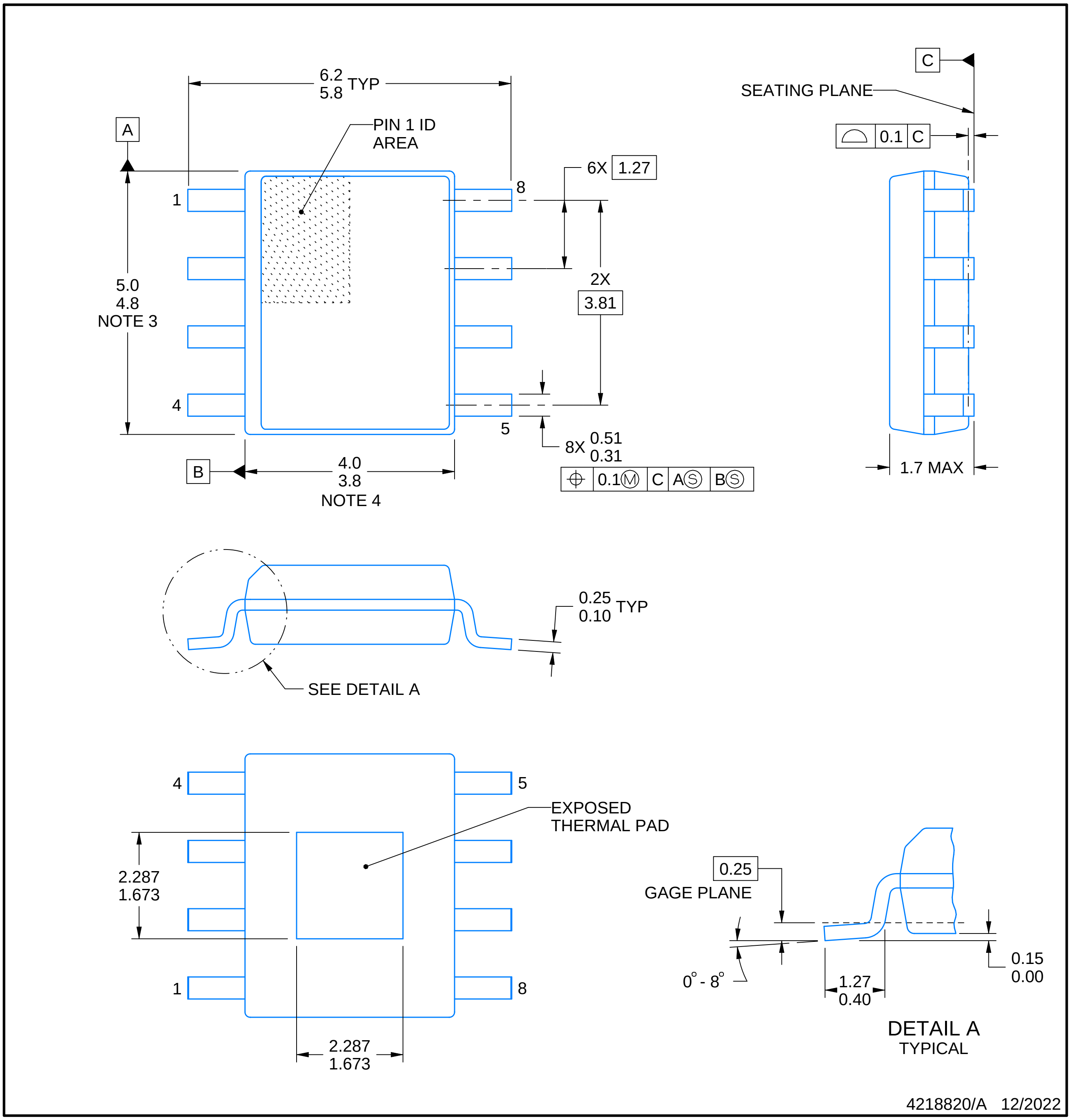
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

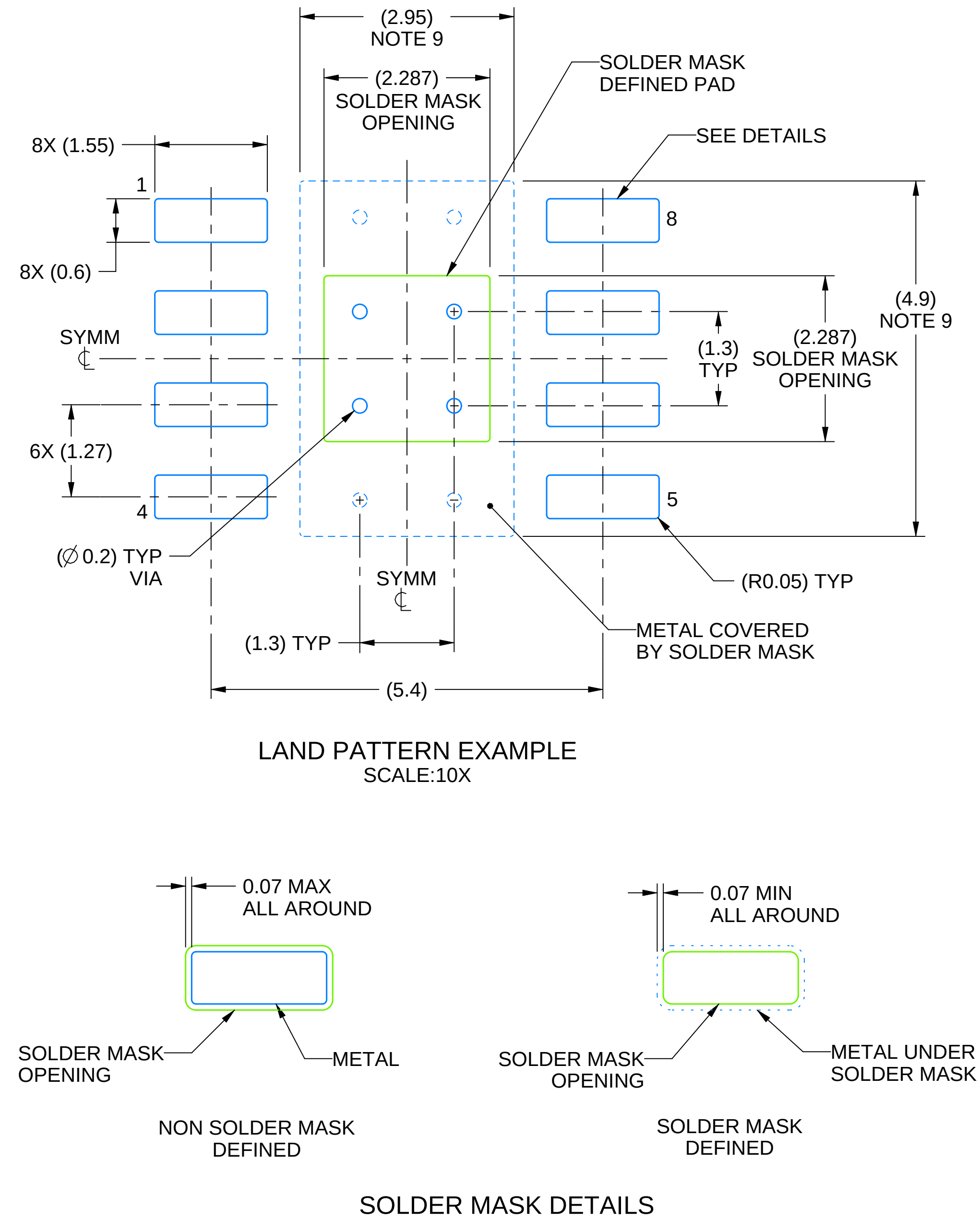
4202561/G



PowerPAD is a trademark of Texas Instruments.

NOTES:

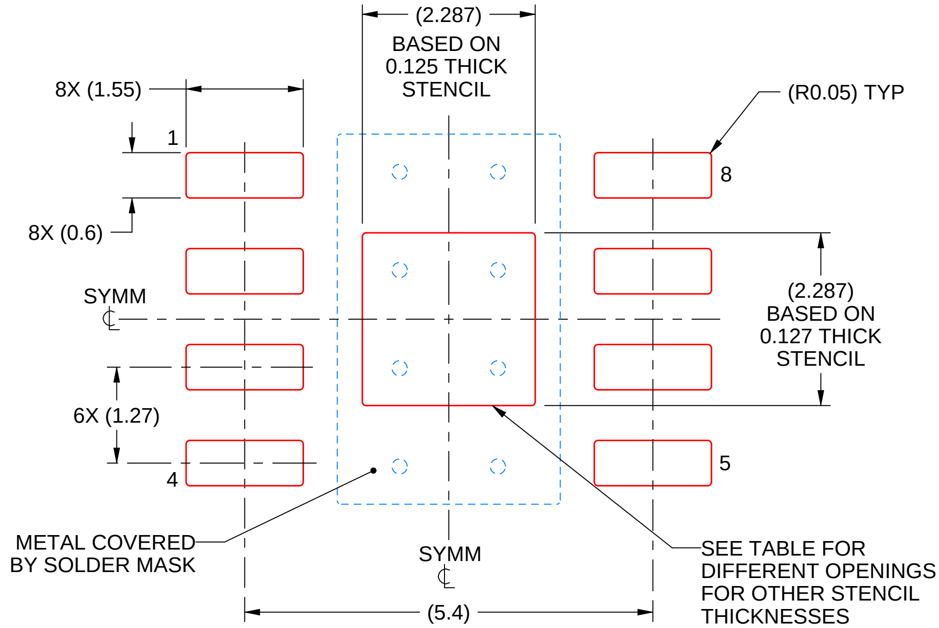
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

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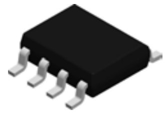
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

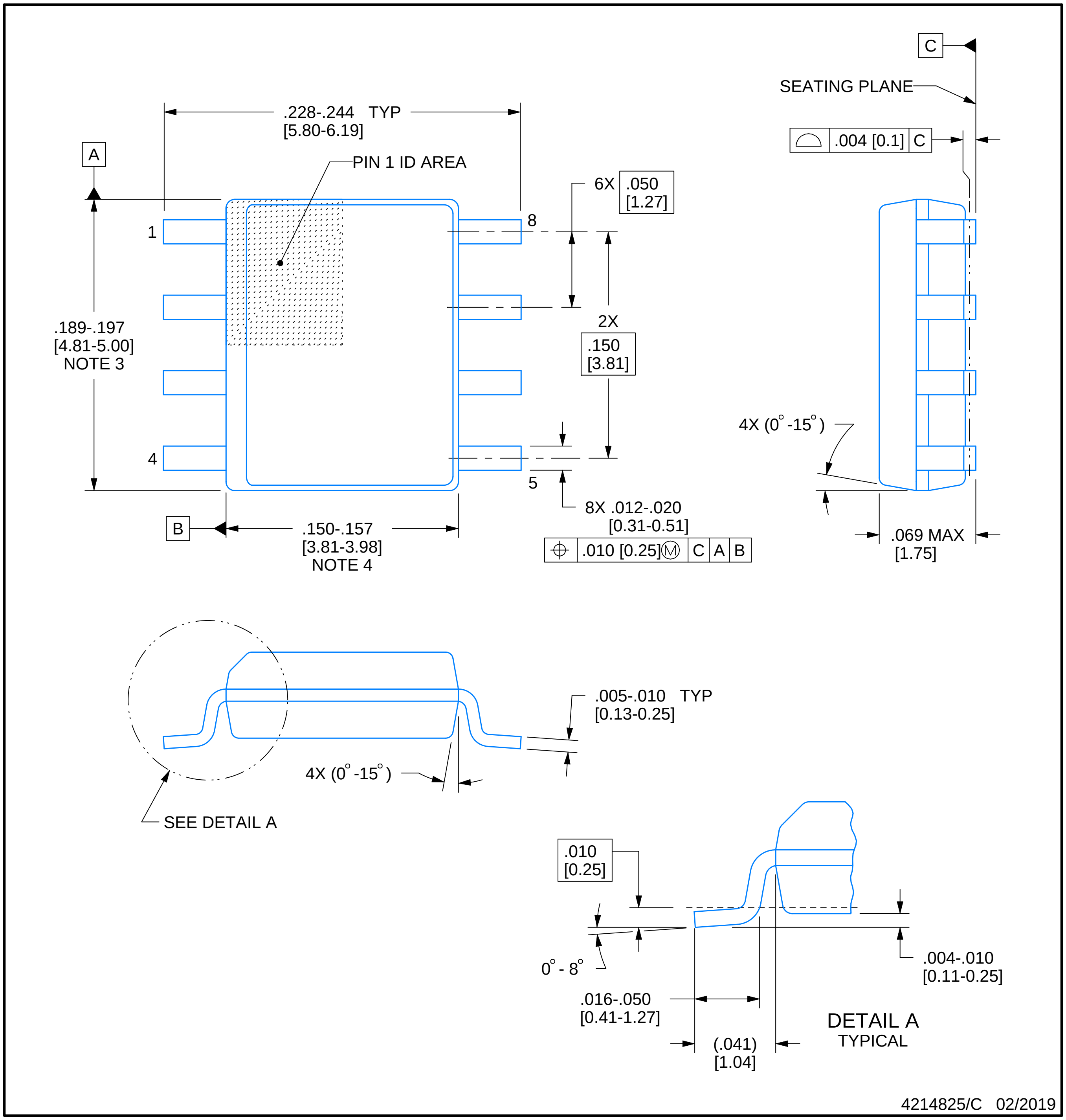


PACKAGE OUTLINE

D0008A

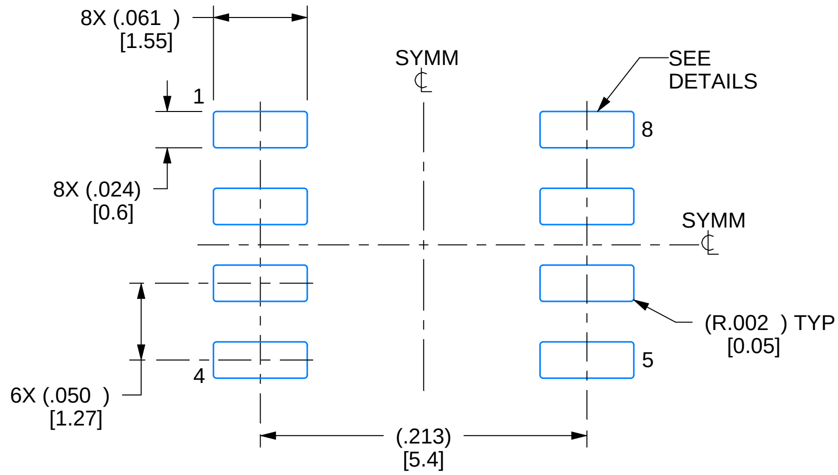
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

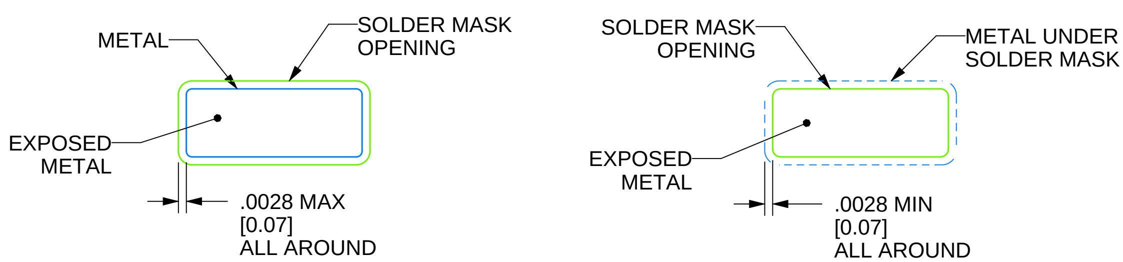


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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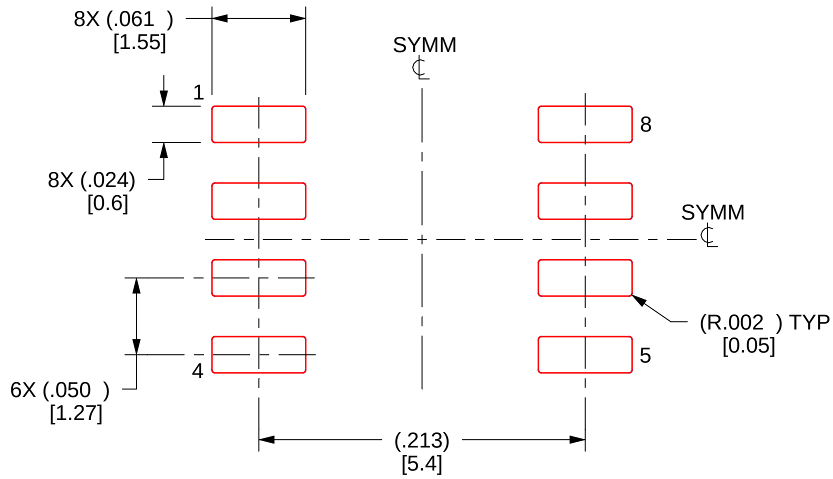
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265