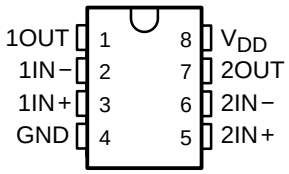
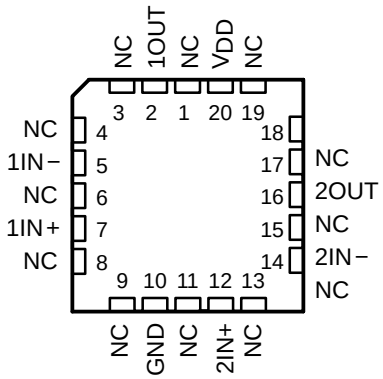
- **Very Low Power . . . 110 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  - **TLC393C . . . 3 V to 16 V**
  - **TLC393I . . . 3 V to 16 V**
  - **TLC393Q . . . 4 V to 16 V**
  - **TLC393M . . . 4 V to 16 V**
  - **TLC193M . . . 4 V to 16 V**
- **On-Chip ESD Protection**

D, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



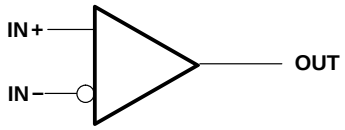
NC − No internal connection

description

The TLC193 and TLC393 consist of dual independent micropower voltage comparators designed to operate from a single supply. They are functionally similar to the LM393 but uses one-twentieth the power for similar response times. The open-drain MOS output stage interfaces to a variety of loads and supplies. For a similar device with a push-pull output configuration (see the TLC3702 data sheet).

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



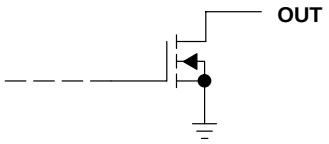
The TLC393C is characterized for operation over the commercial temperature range of T_A = 0°C to 70°C. The TLC393I is characterized for operation over the extended industrial temperature range of T_A = −40°C to 85°C. The TLC393Q is characterized for operation over the full automotive temperature range of T_A = −40°C to 125°C. The TLC193M and TLC393M are characterized for operation over the full military temperature range of T_A = −55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGES				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	5 mV	TLC393CD	—	—	TLC393CP	TLC393CPWLE
− 40°C to 85°C	5 mV	TLC393ID	—	—	TLC393IP	TLC393IPWLE
− 40°C to 125°C	5 mV	TLC393QD	—	—	—	—
− 55°C to 125°C	5 mV	TLC393MD	TLC193MFK	TLC193MJG	TLC393MP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC393CDR).

schematic



OPEN-DRAIN CMOS OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . − 0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage range, V_I . . . . . − 0.3 V to V_{DD}
Output voltage range, V_O . . . . . − 0.3 V to 16 V
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . 20 mA
Total supply current into V_{DD} . . . . . 40 mA
Total current out of GND . . . . . 40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC393C . . . . . 0°C to 70°C
TLC393I . . . . . − 40°C to 85°C
TLC393Q . . . . . − 40°C to 125°C
TLC393M . . . . . − 55°C to 125°C
TLC193M . . . . . − 55°C to 125°C
Storage temperature range . . . . . − 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW	525 mW	4.2 mW/°C	336 mW	273 mW	—

recommended operating conditions

	TLC393C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			0°C to 70°C	0 to V_{DD} − 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	μA
			0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC393I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	− 0.2		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	− 40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 85°C	0 to V_{DD} − 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			− 40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			− 40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	µA
			−40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC393Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393Q			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			−40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 125°C	0 to V_{DD} − 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			−40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	µA
			−40°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kΩ load to V_{DD}).

recommended operating conditions

	TLC193M, TLC393M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC193M, TLC393M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−55°C to 125°C	0 to V_{DD} − 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	μA
			−55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kΩ load to V_{DD}).

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

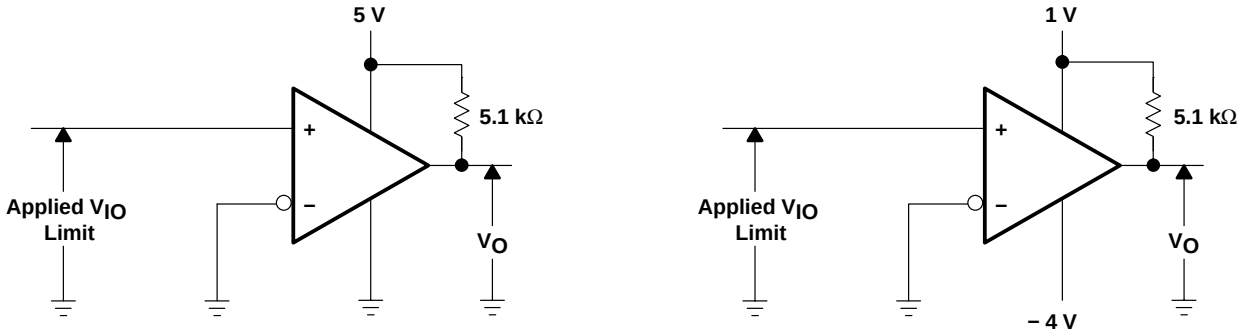
PARAMETER		TEST CONDITIONS		TLC393C, TLC393I TLC393Q, TLC193M, TLC393M			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.1		
t_{PHL}	Propagation delay time, high-to-low-level output	V_I = 1.4-V step at IN+			1.1		µs
		f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4-V step at IN+			0.10		
t_f	Fall time, output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		22		ns

PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection ratio, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

The voltage divider formed by R9 and R10 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

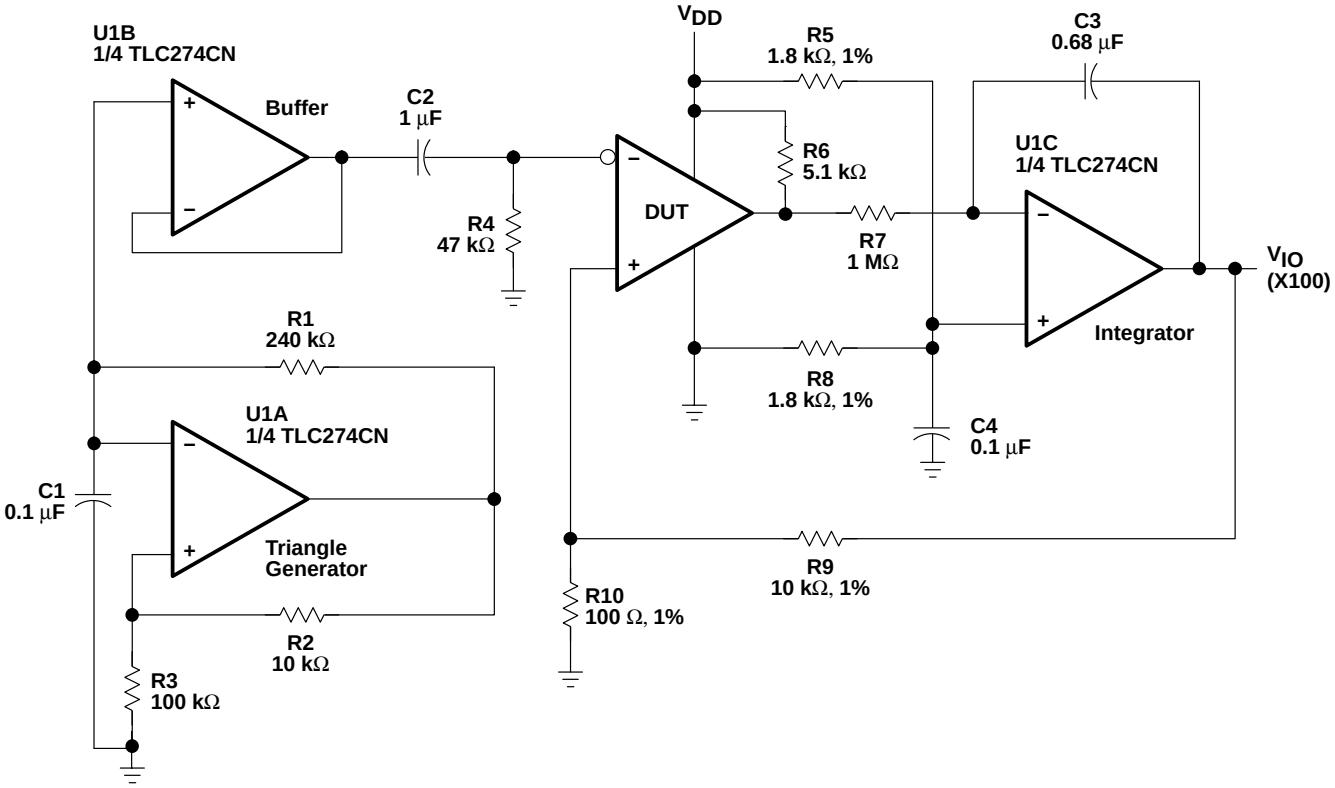
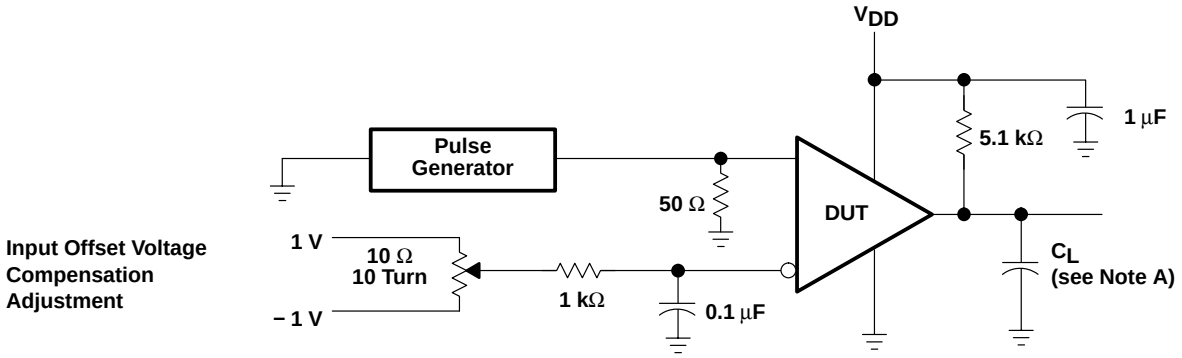


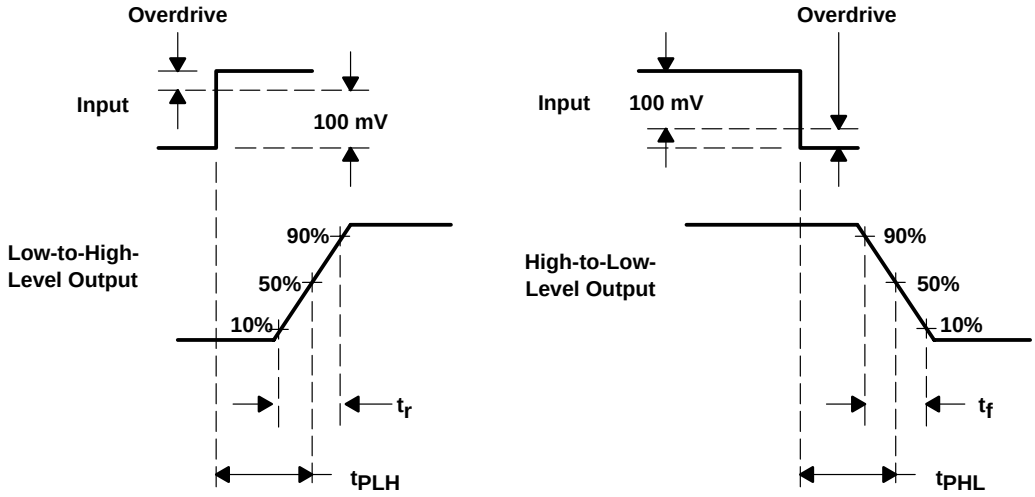
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105 mV or 5 mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise Time, and Fall Time Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	7
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	8 9
I_{OH}	Low-level output current	vs High-level output voltage vs Free-air temperature	10 11
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	12 13
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	14
t_{PHL}	High-to-low level output propagation delay time	vs Supply voltage	15
	Low-to-high-level output response	Low-to-high level output propagation delay time	16
	High-to-low level output response	High-to-low level output propagation delay time	17
t_f	Fall time	vs Supply voltage	18

DISTRIBUTION OF INPUT OFFSET VOLTAGE†

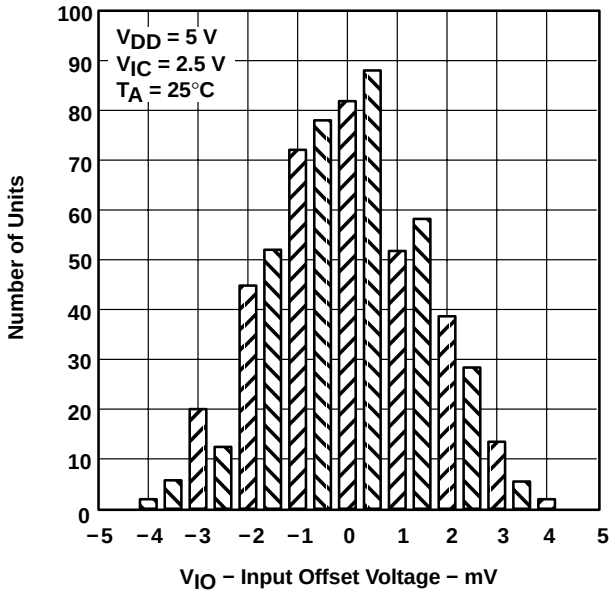


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE†

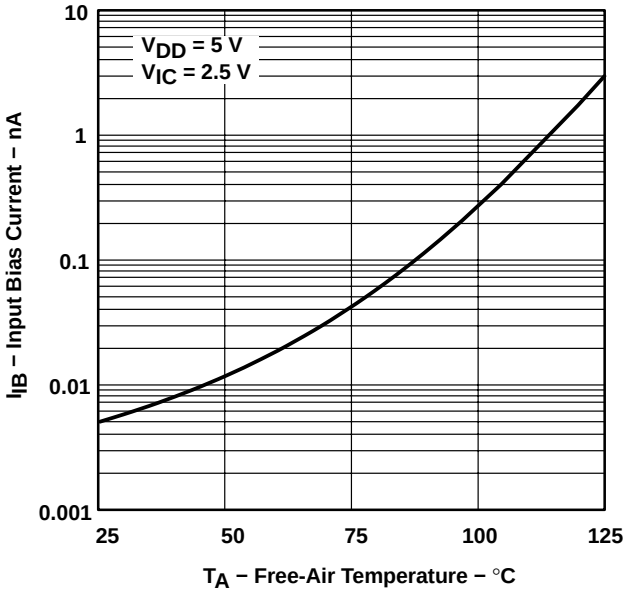


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

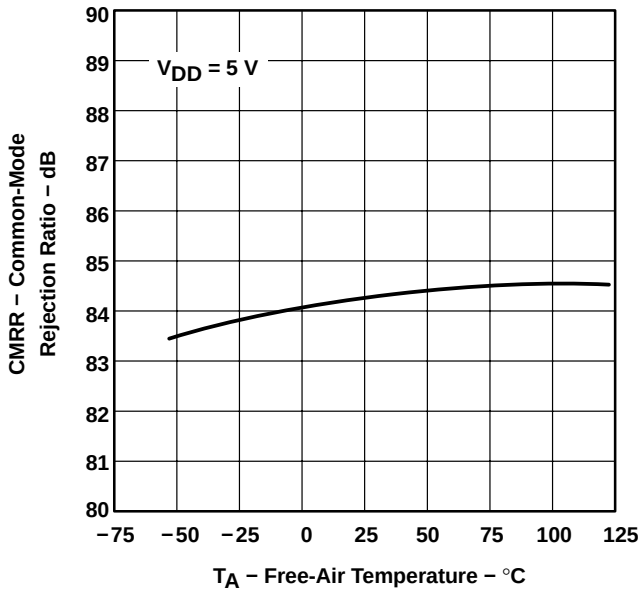


Figure 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

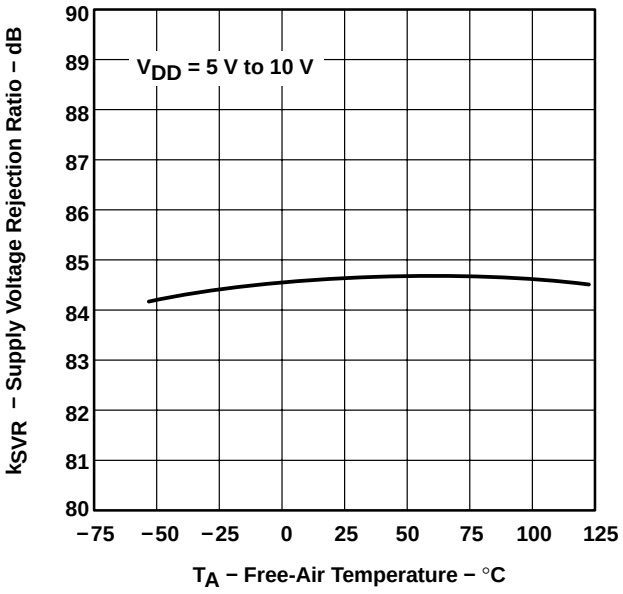


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

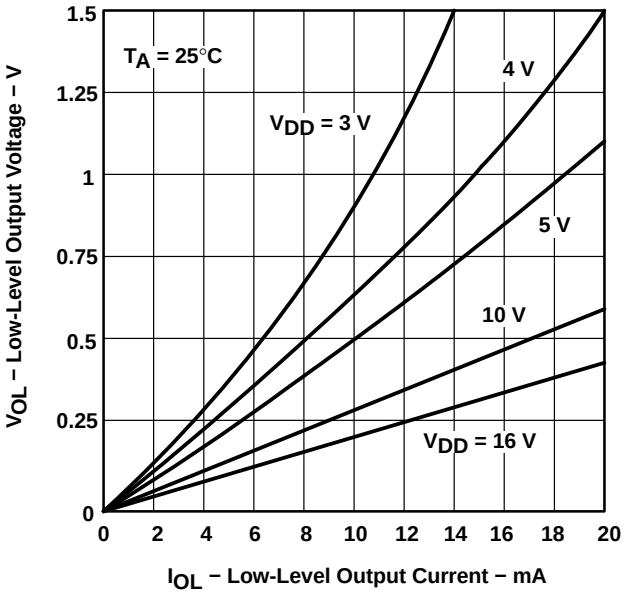


Figure 8

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

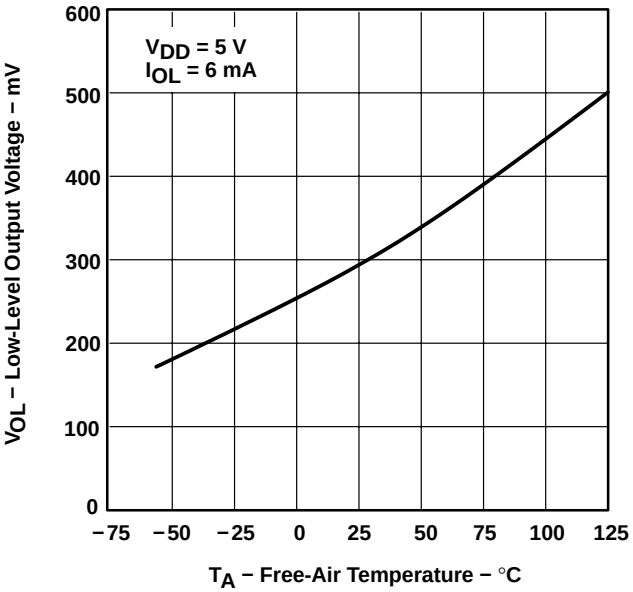


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

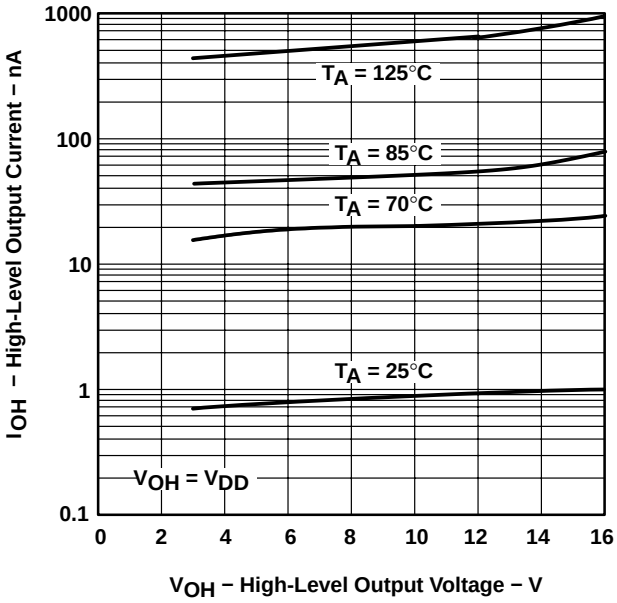


Figure 10

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

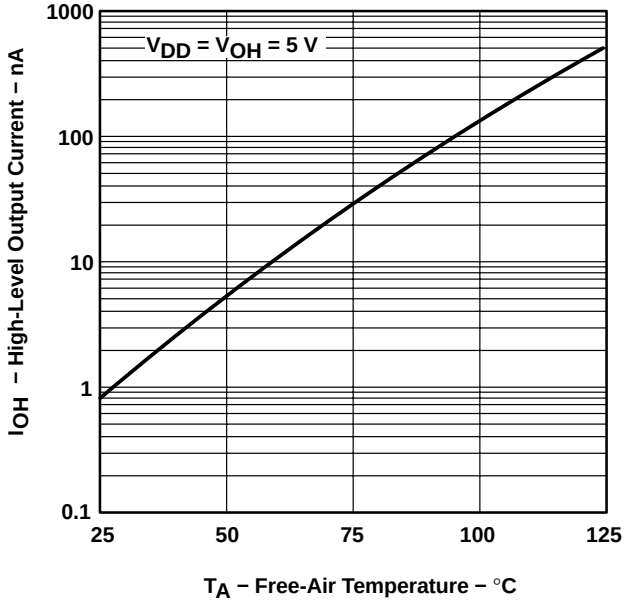


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

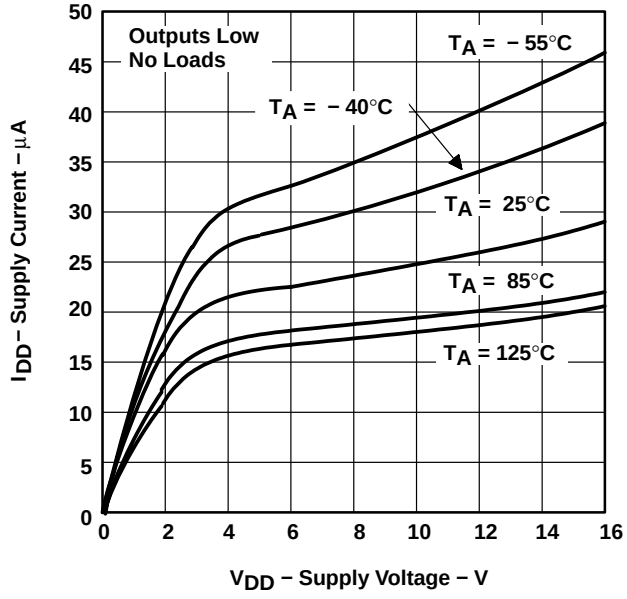


Figure 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

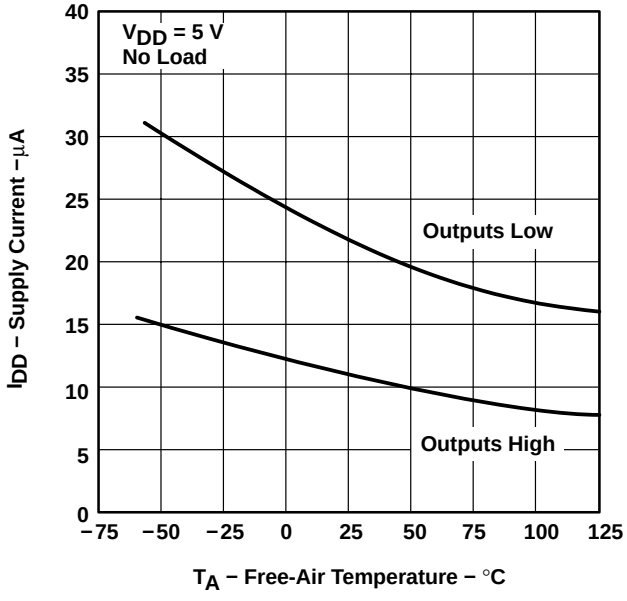


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE TIME vs SUPPLY VOLTAGE

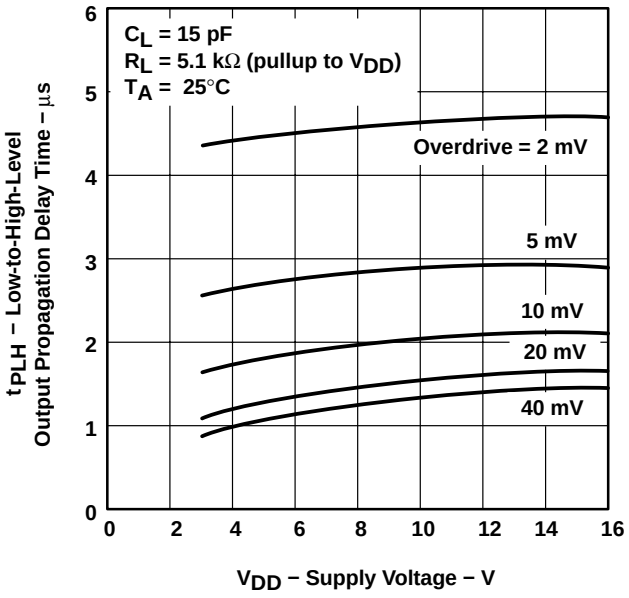


Figure 14

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE TIME vs SUPPLY VOLTAGE

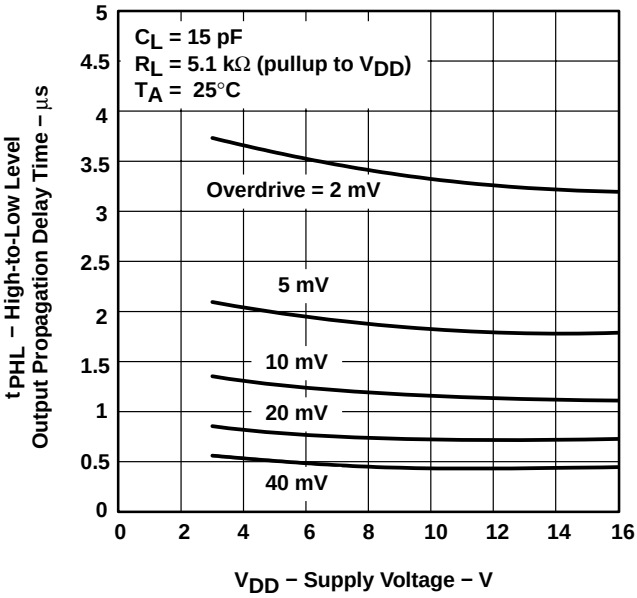


Figure 15

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS INPUT OVERDRIVES

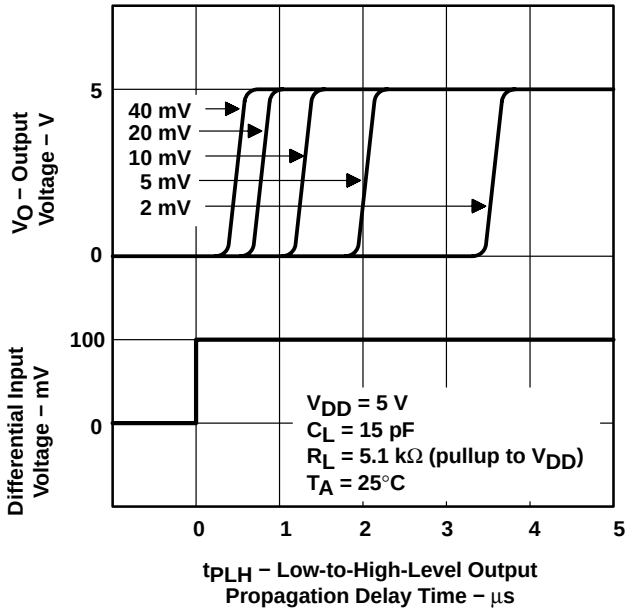


Figure 16

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS INPUT OVERDRIVES

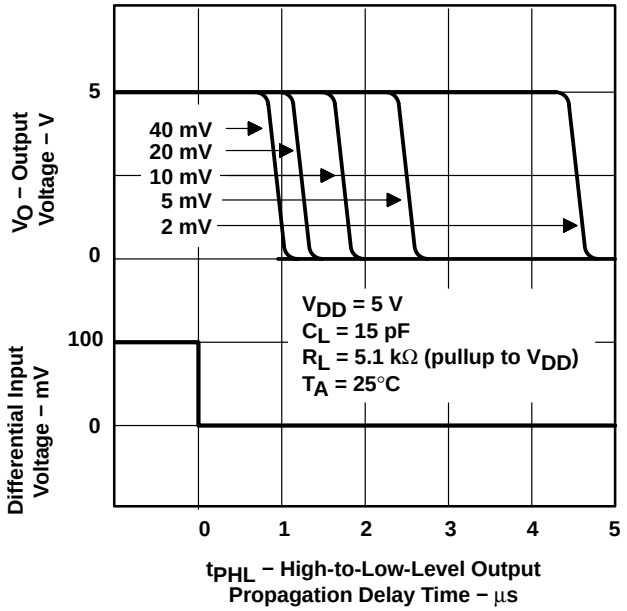


Figure 17

TYPICAL CHARACTERISTICS

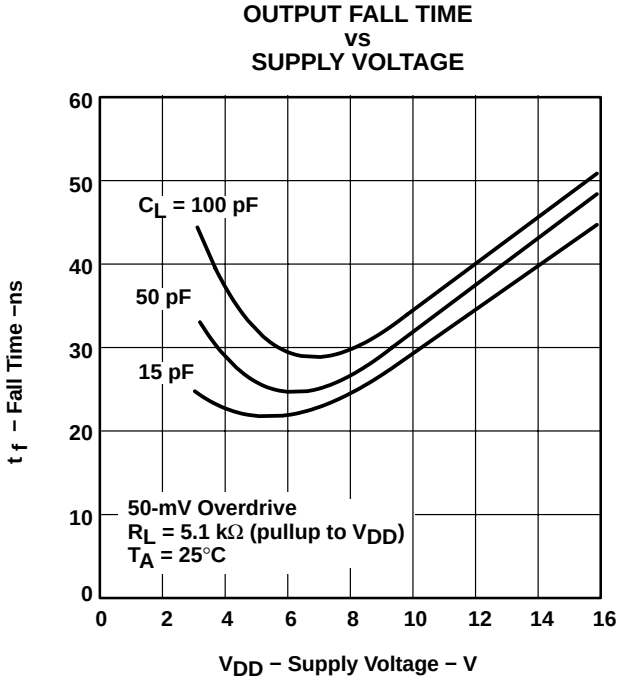


Figure 18

APPLICATION INFORMATION

The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to assure proper device operation.

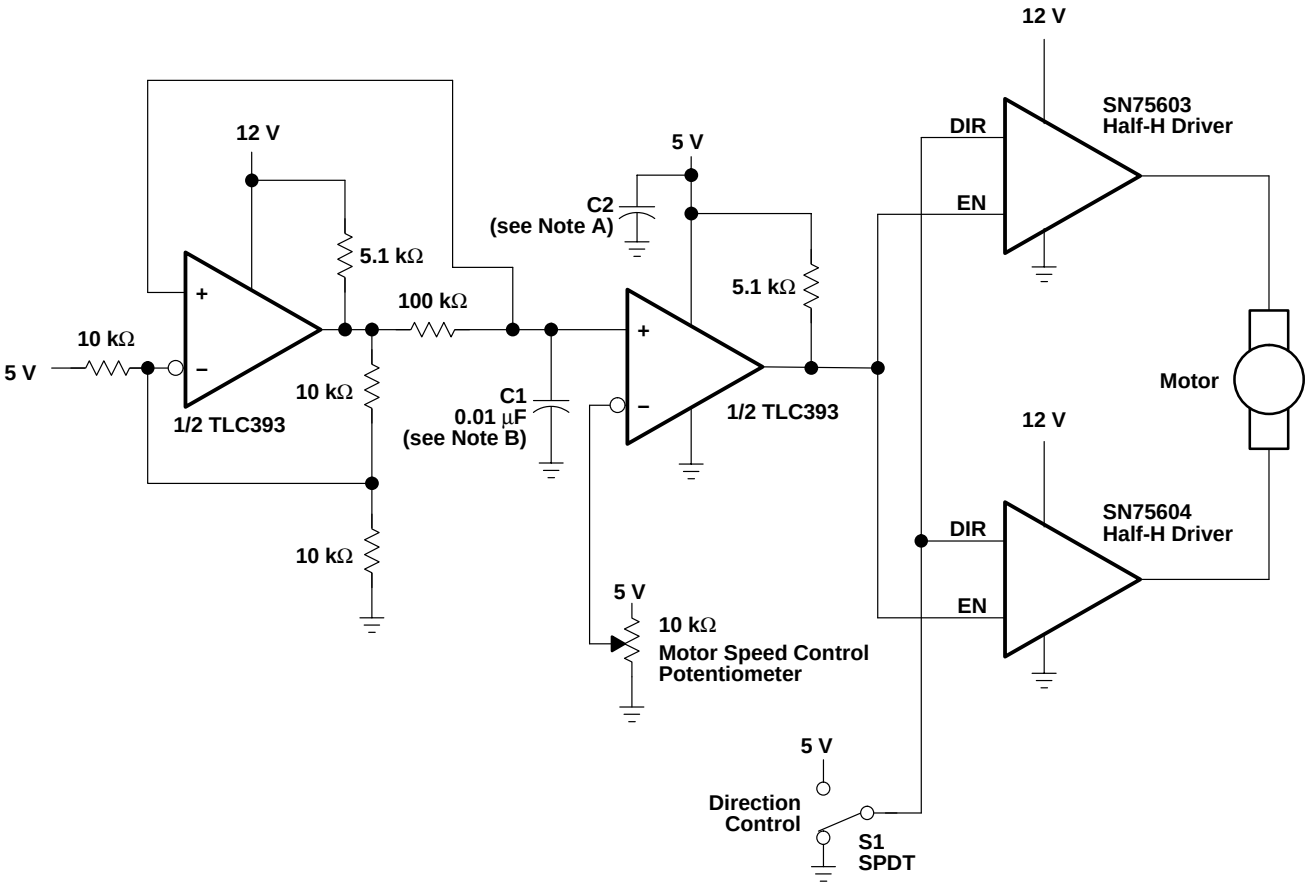
To assure reliable operation, the supply should be decoupled with a capacitor (0.1-μF) positioned as close to the device as possible.

The TLC393 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21
Micropower switching regulator	28

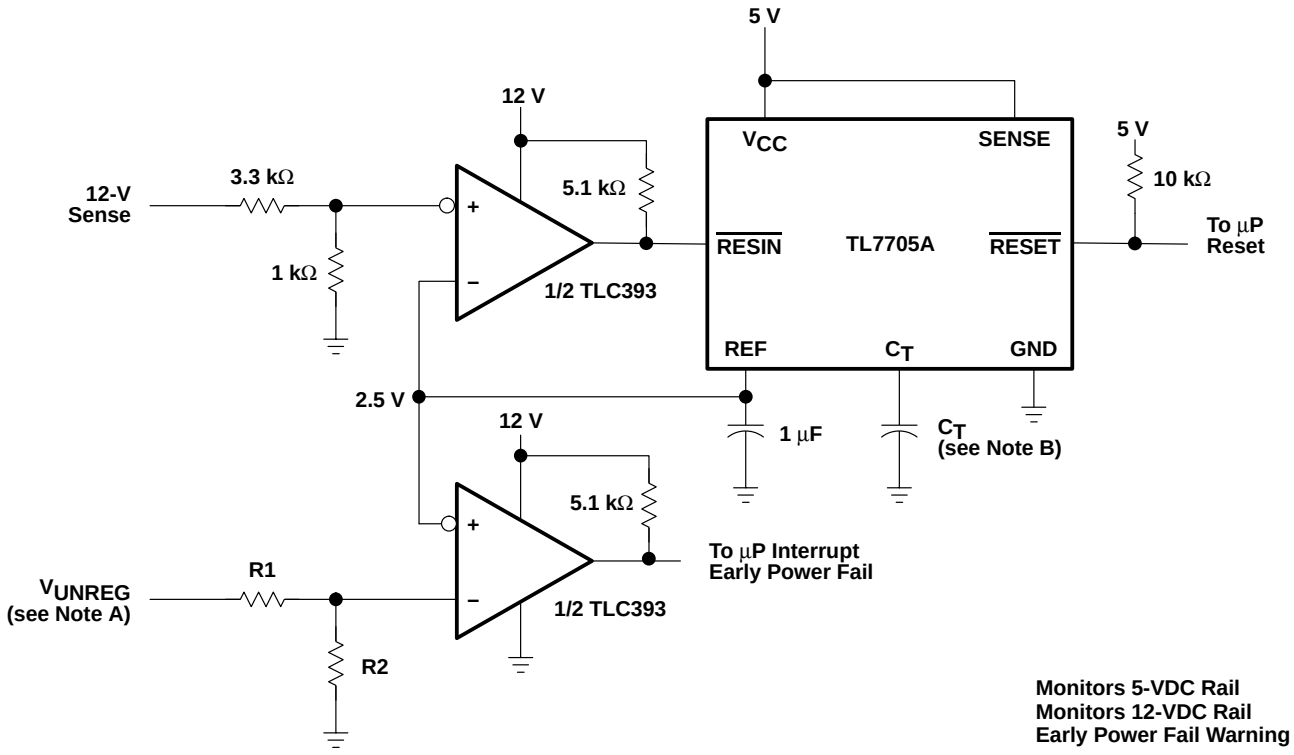
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

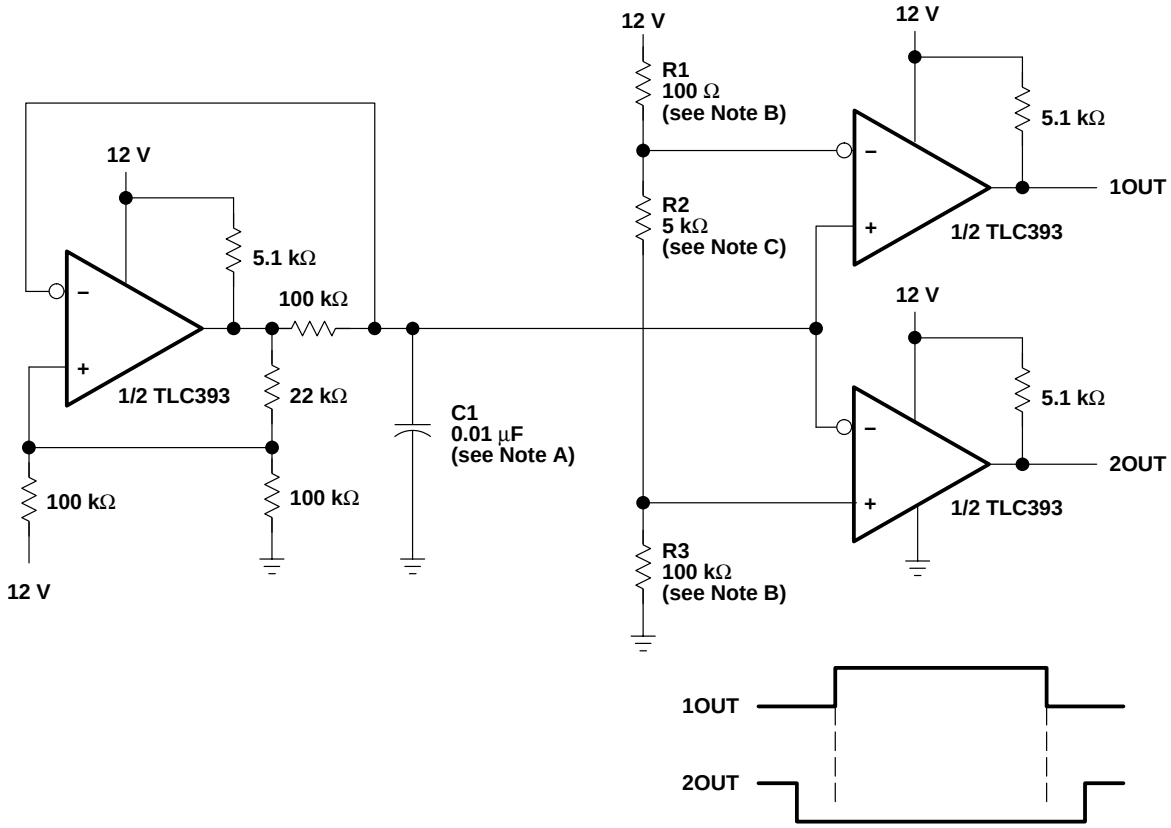


NOTES: A. $V_{UNREG} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor

APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 21. Two-Phase Nonoverlapping Clock Generator

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9555101NXDR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-	Q193M
5962-9555101QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555101QPA TLC193M
TLC193MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-	9555101QPA TLC193M
TLC193MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9555101QPA TLC193M
TLC393CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	C393C
TLC393CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	C393C
TLC393CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	C393C
TLC393CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393C
TLC393CDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393C
TLC393CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC393CP
TLC393CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC393CP
TLC393CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P393
TLC393ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	C393I
TLC393IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C393I
TLC393IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C393I
TLC393IDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393I
TLC393IDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393I
TLC393IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC393IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC393IP
TLC393IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC393IP
TLC393IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC393IP
TLC393IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	Y393

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC393IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y393
TLC393IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y393
TLC393IPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC393QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393Q
TLC393QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLC393 :

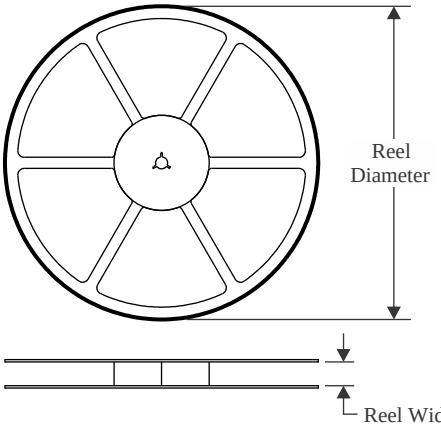
- Automotive : TLC393-Q1

NOTE: Qualified Version Definitions:

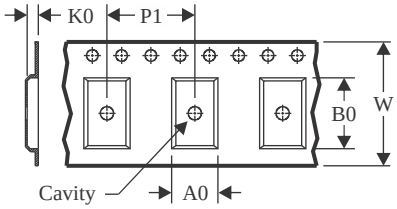
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

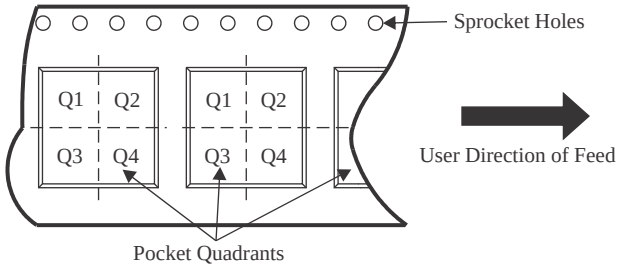


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

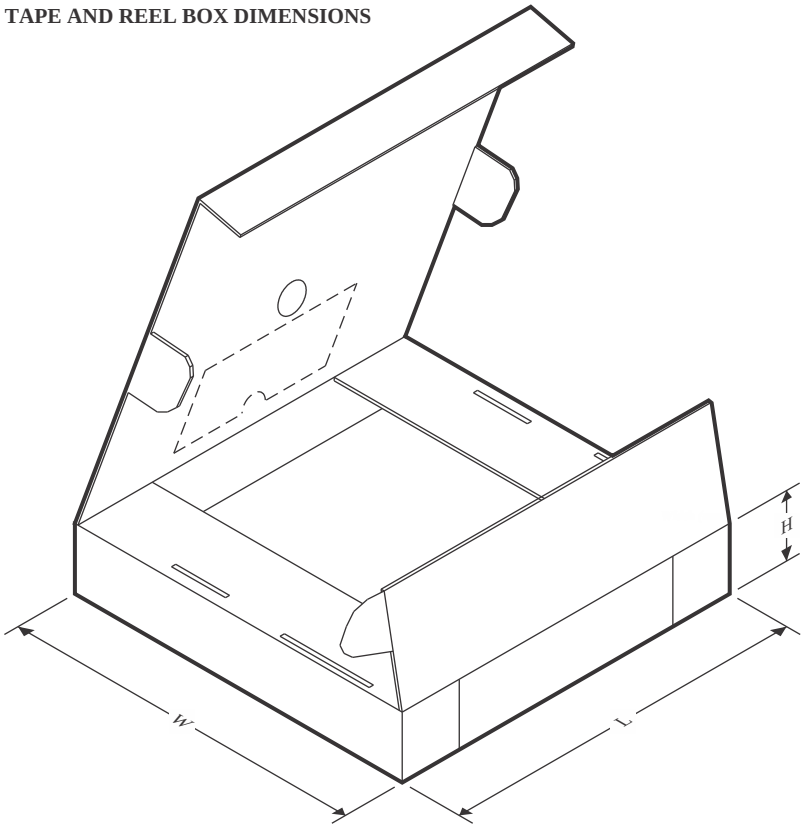
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC393CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC393CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC393CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TLC393CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC393CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC393IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC393IDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC393QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

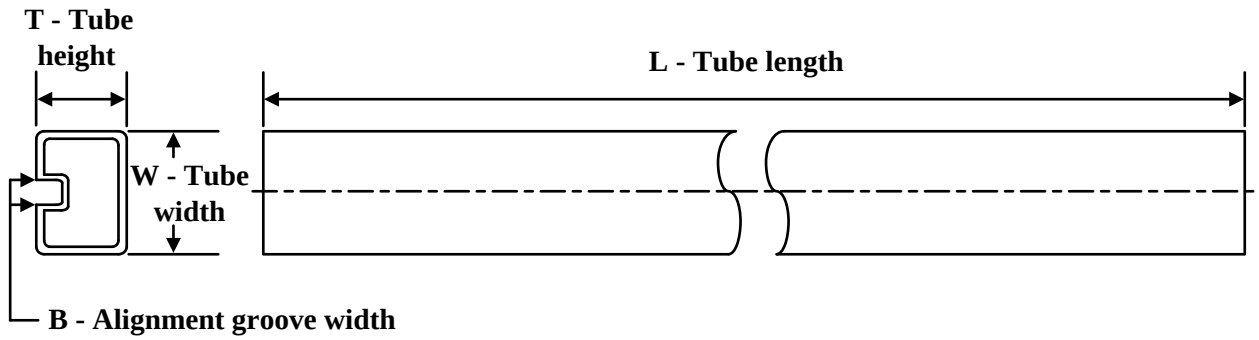
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

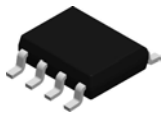
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC393CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC393CDRG4	SOIC	D	8	2500	356.0	356.0	35.0
TLC393CPSR	SO	PS	8	2000	356.0	356.0	35.0
TLC393CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC393CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC393IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLC393IDR1G4	SOIC	D	8	2500	356.0	356.0	35.0
TLC393IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC393IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLC393QDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC393CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC393CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC393CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC393CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC393IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC393IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC393IPE4	P	PDIP	8	50	506	13.97	11230	4.32

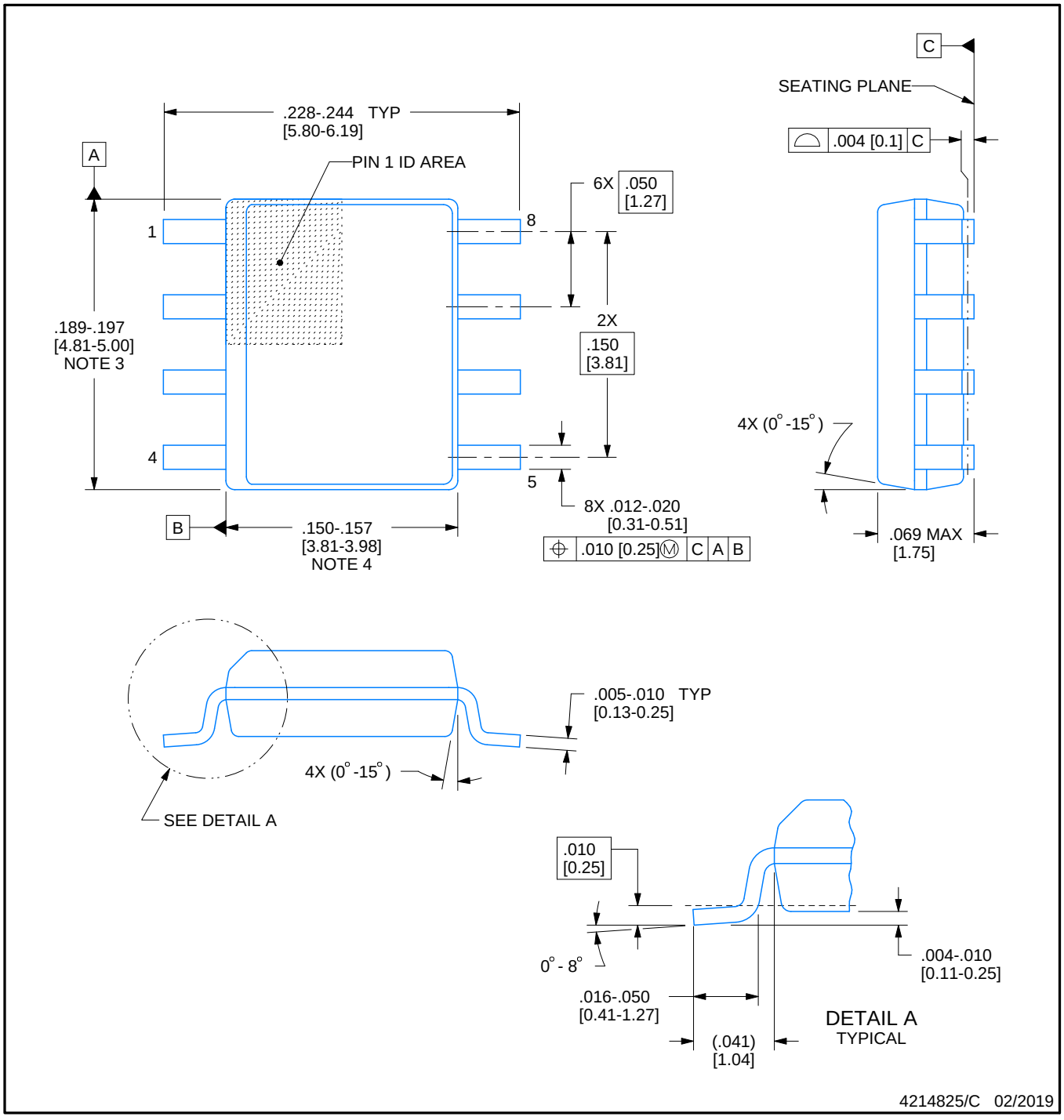


PACKAGE OUTLINE

D0008A

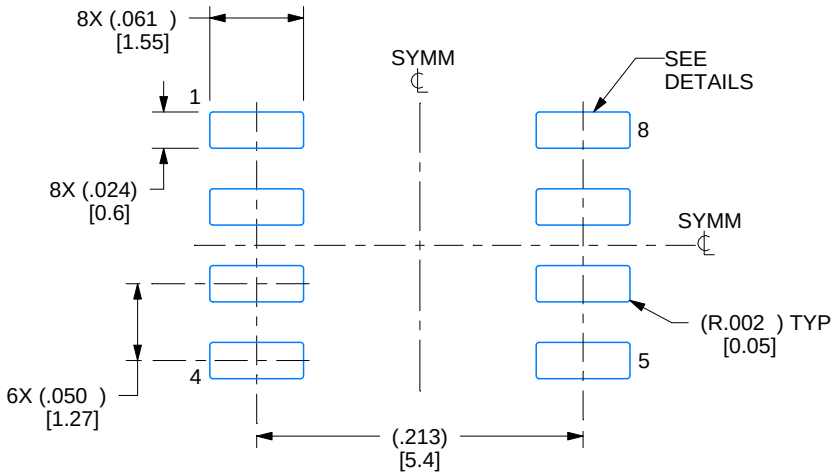
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

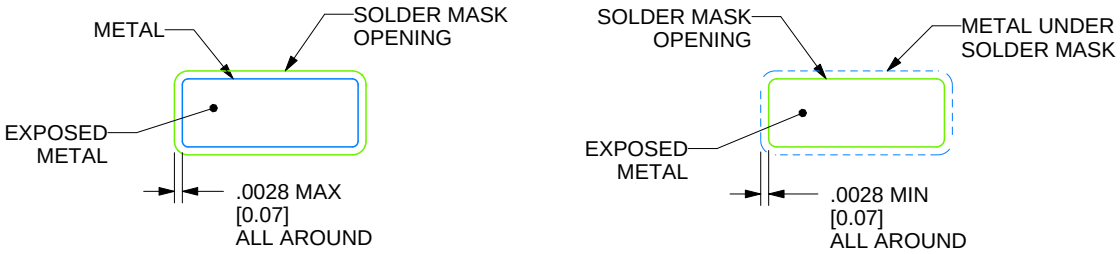


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

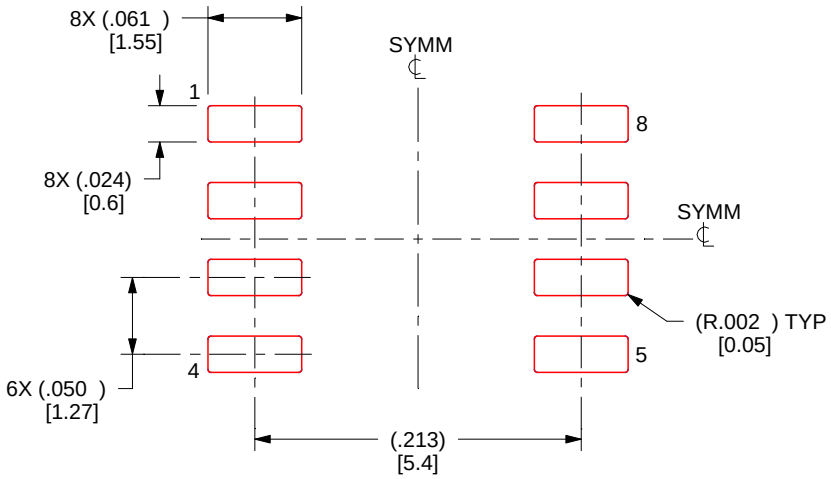
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

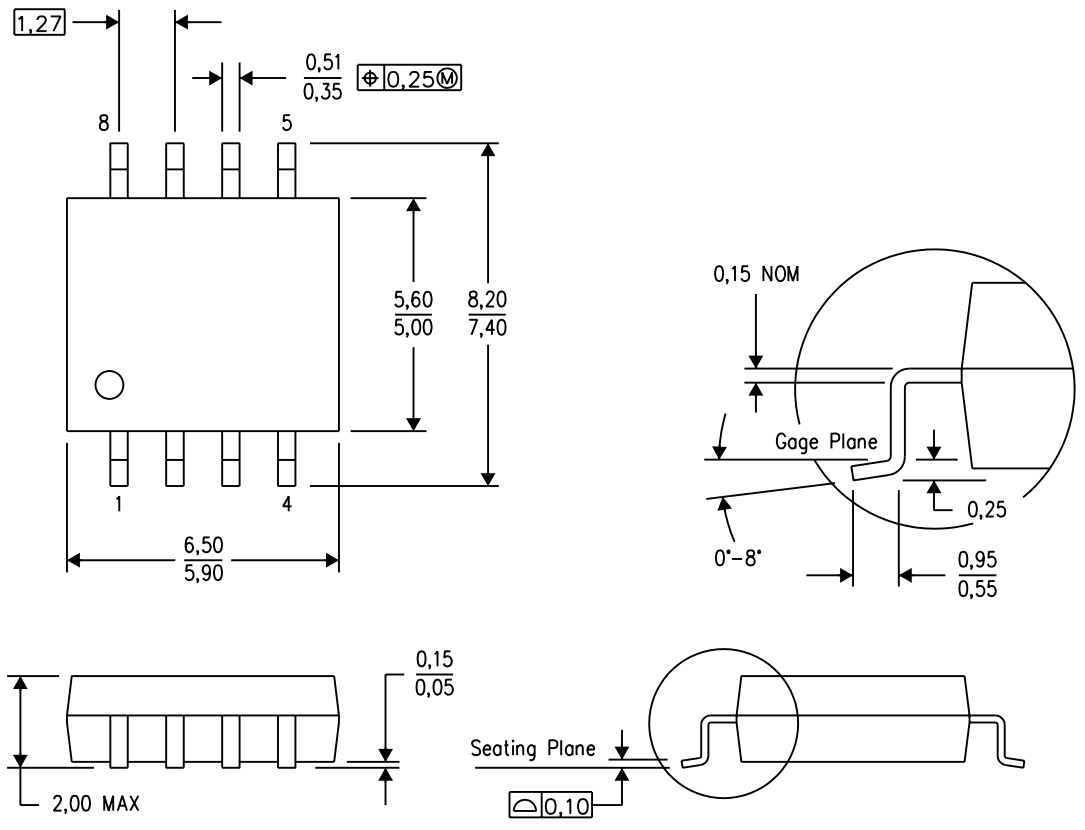
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

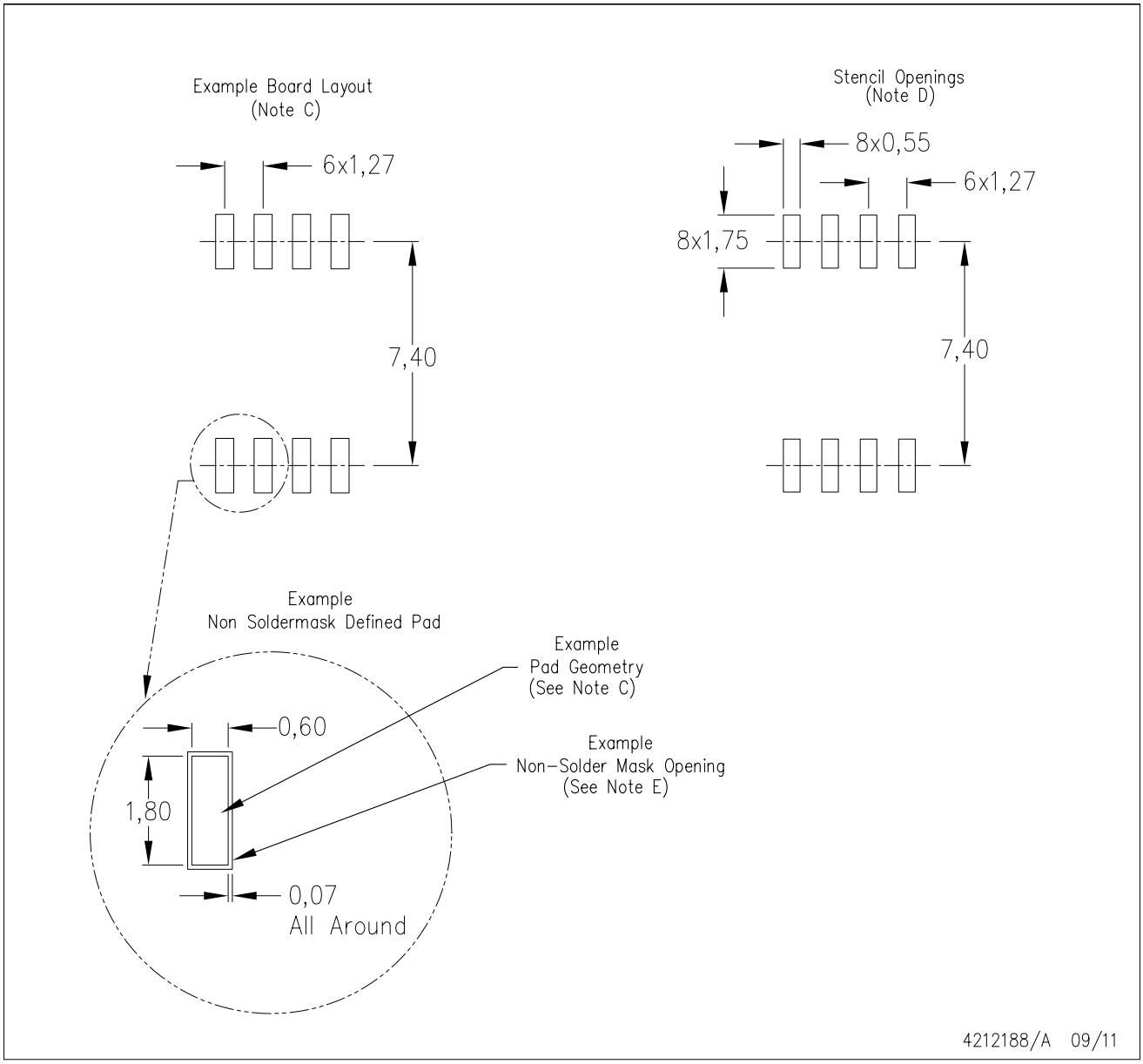
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

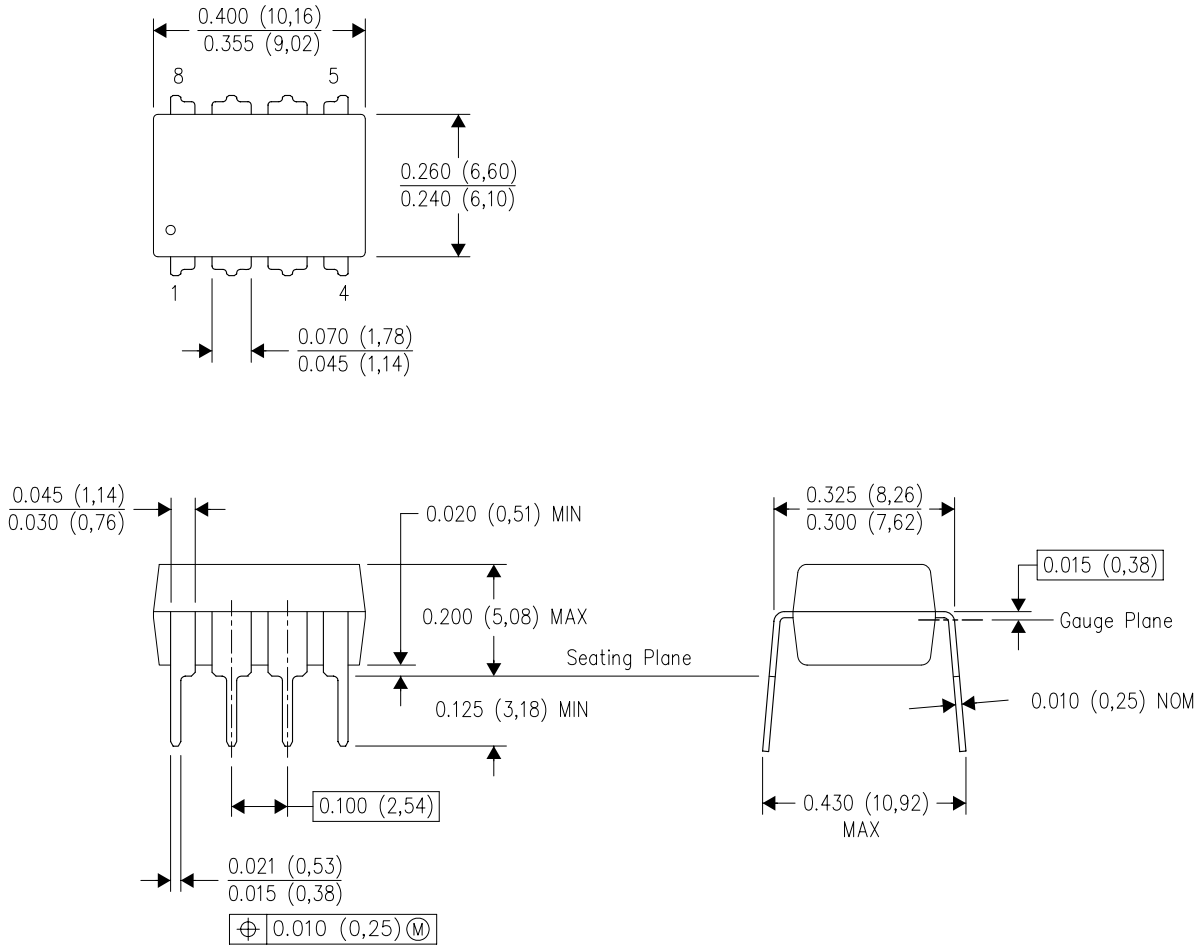
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



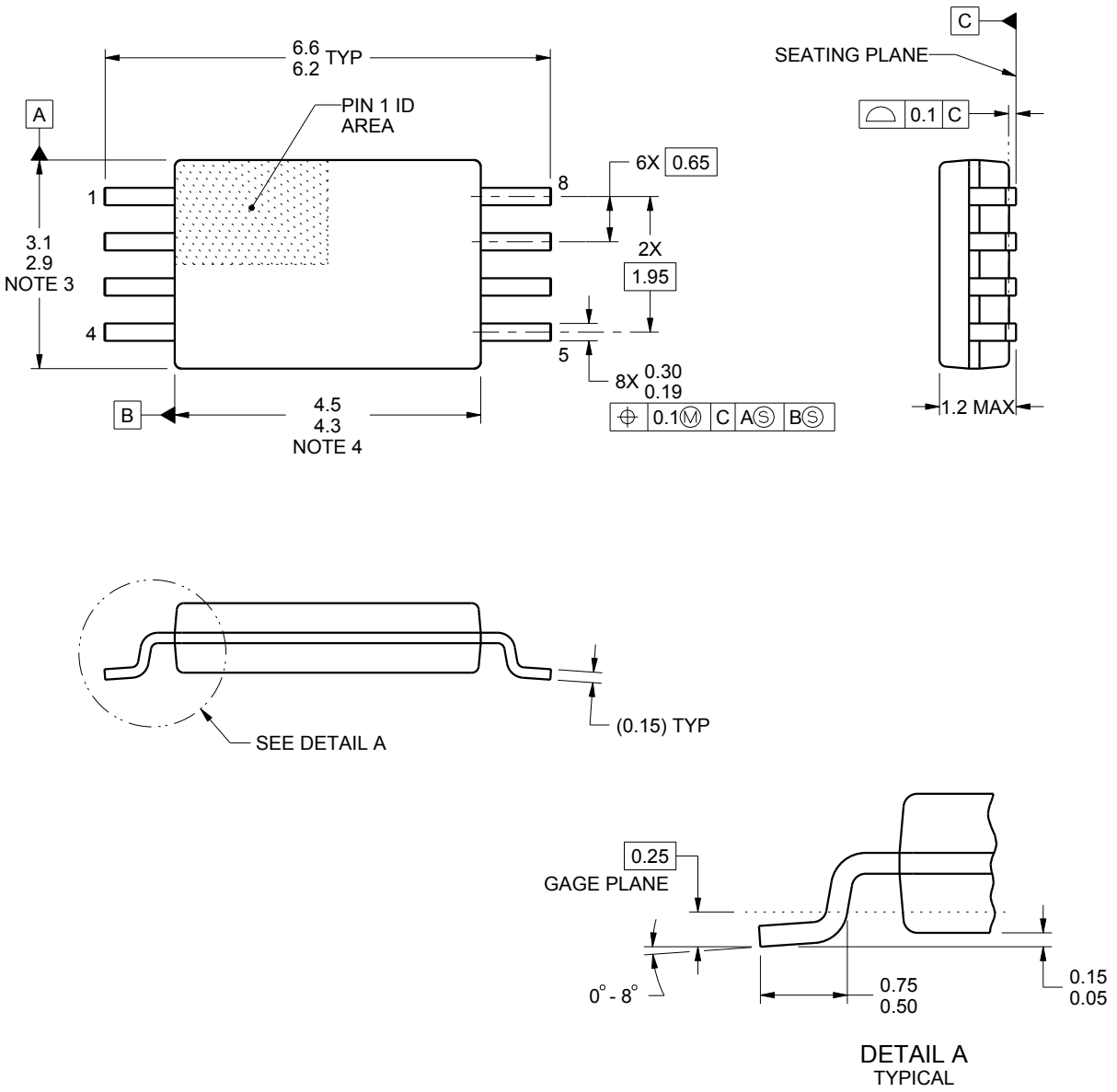
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

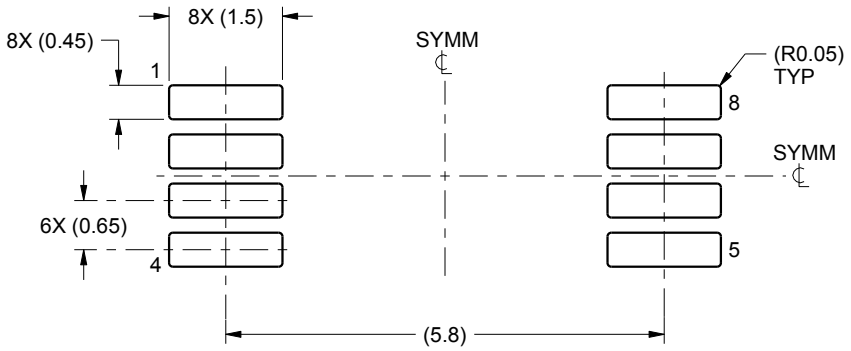
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

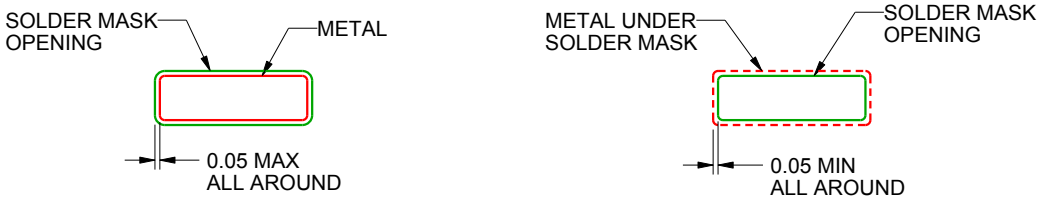


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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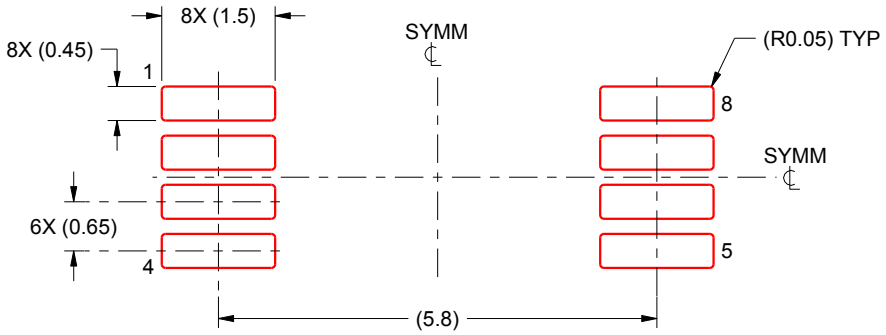
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

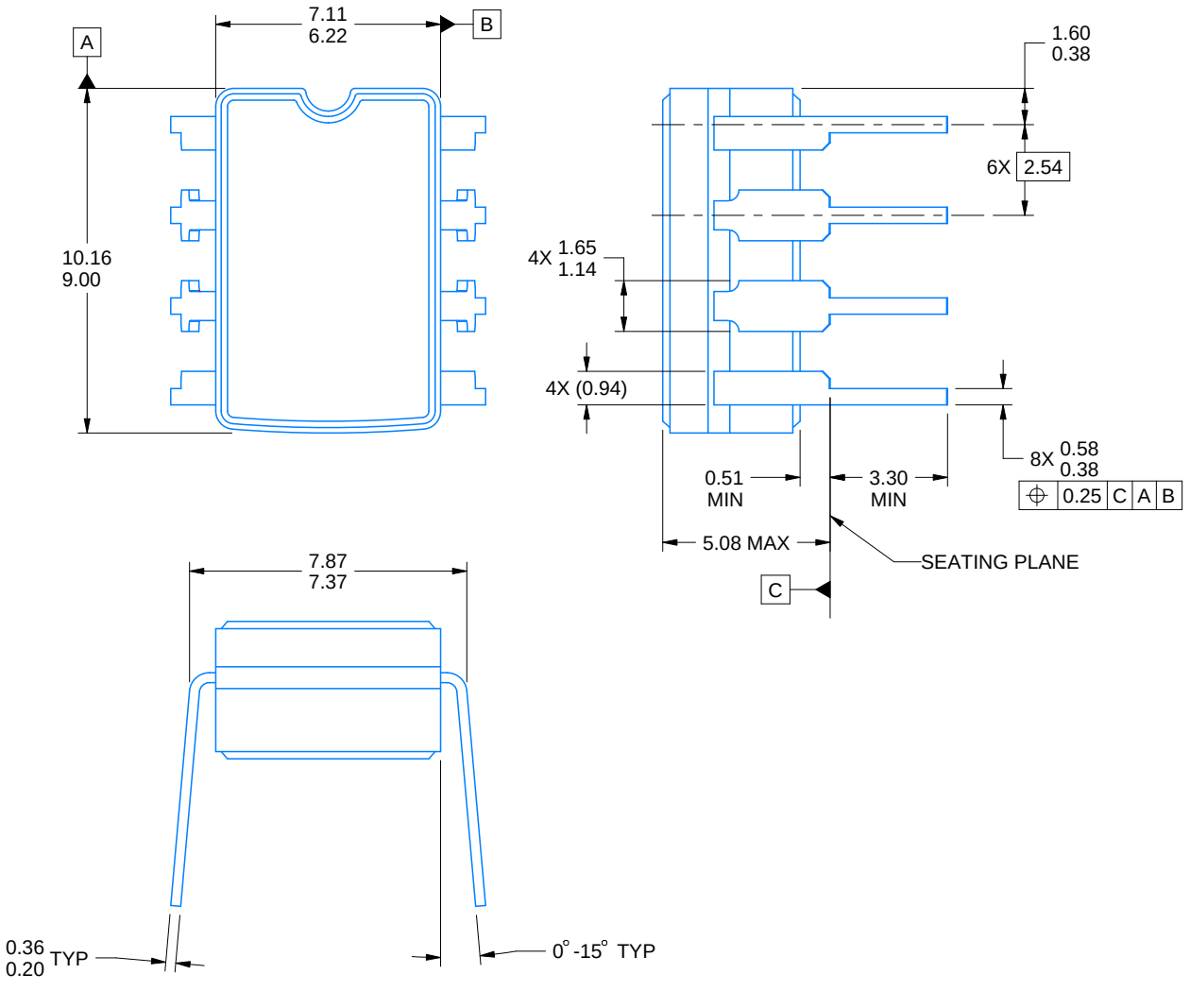
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



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NOTES:

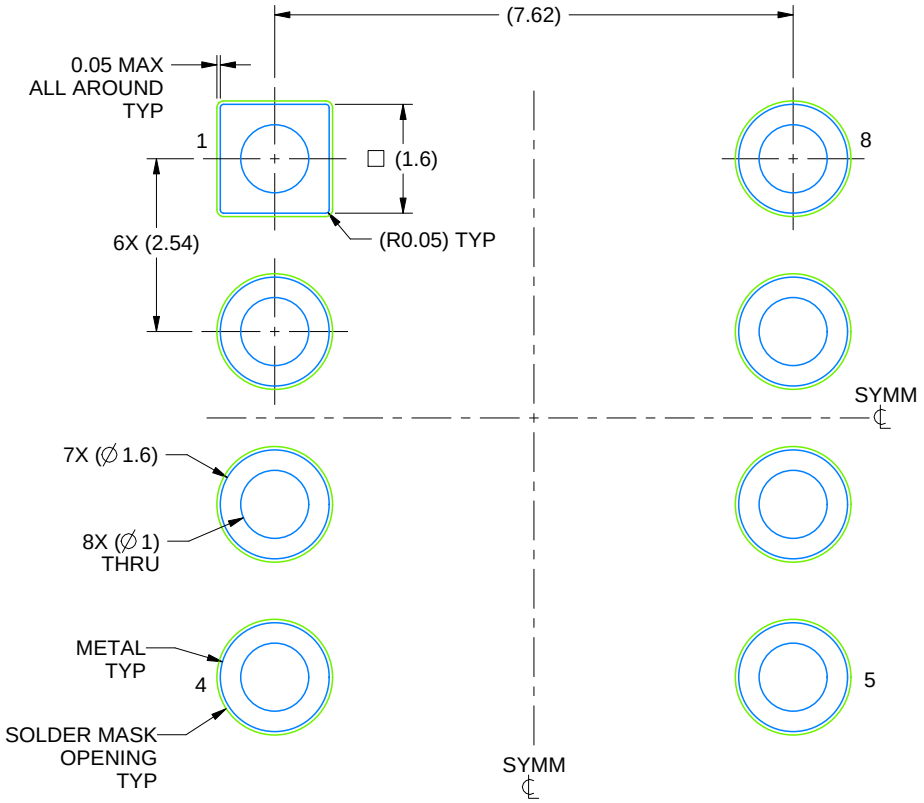
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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