TLC6A598 パワー・ロジック 8 ビット・シフト・レジスタ

1 特長

- 航空電子機器アプリケーションに適した高信頼性と堅牢性
- 広い動作時周辺温度範囲：–55℃～+125℃
- 広い V_{CC} 範囲：3V～5.5V
- 8 つのパワー DMOS トランジスタ出力チャネル
  - 350mA の連続電流
  - 1.1A の電流制限機能
  - 50V の出力クランプ電圧
  - 1Ω (標準値) の低い $R_{ds(on)}$
  - 90mJ (最大値) のアバランシェ・エネルギー
- 保護
  - 過電流保護
  - 開放および短絡負荷の検出
  - シリアル・インターフェイス通信エラーの検出
  - サーマル・シャットダウン保護機能
- 拡張カスケードにより複数段可能
- 単一の入力ですべてのレジスタをクリア
- 巡回冗長性検査 (CRC)
- 低い消費電力
- 24 ピン SOIC DW パッケージ

2 アプリケーション

- 飛行制御システム
- PLC 制御および機能インジケータ
- 計器盤
- リレーまたはソレノイド・ドライバ
- 家電機器用ディスプレイ・パネル
- LED 表示および照明

3 概要

TLC6A598 デバイスは、LED などの比較的大きな負荷電力を必要とするシステムで使用するように設計されたモノリシック、高電圧、大電流出力の 8 ビット・シフト・レジスタです。

本デバイスは、誘導性過渡保護のために電圧クランプを出力に組み込んでいます。パワー・ドライバ・アプリケーションには、リレー、ソレノイド、その他の大電流または高電圧負荷が含まれます。各オープン・ドレイン DMOS トランジスタは、短絡発生時の損傷を防止するために独立したチョッピング電流制限回路を備えています。

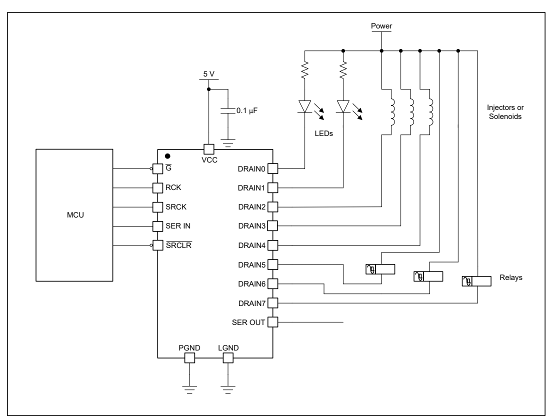
このデバイスには、8 ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが内蔵されており、8 ビットの D タイプ・ストレージ・レジスタへデータを供給します。出力は、50V の出力定格と 350mA の連続シンク電流能力を持つローサイド・オープン・ドレイン DMOS トランジスタです。負荷の開放および短絡の診断機構が搭載されており、安全性保護が強化されています。本デバイスは巡回冗長性検査 (CRC) 機能を備えており、シフト・レジスタのレジスタ値を検証できます。読み戻しモードでは、デバイスは 6 ビットの CRC 剰余を返します。MCU は CRC 剰余を読み戻して、剰余が正しいかどうかをチェックすることで、MCU とデバイスとの間の通信ループが良好かどうかを判定できます。

TLC6A598 の特性は、−55℃～125℃の動作時周辺温度範囲での動作についてのものです。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TLC6A598	SOIC (24)	15.70mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2021) to Revision C (March 2022)	Page
• Updated the ESD level in the *ESD Ratings*, *Overview*, and *Application Information* sections	4

Changes from Revision A (October 2021) to Revision B (December 2021)	Page
• データシートから車載関連の情報をすべて削除	1

Changes from Revision * (June 2021) to Revision A (October 2021)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

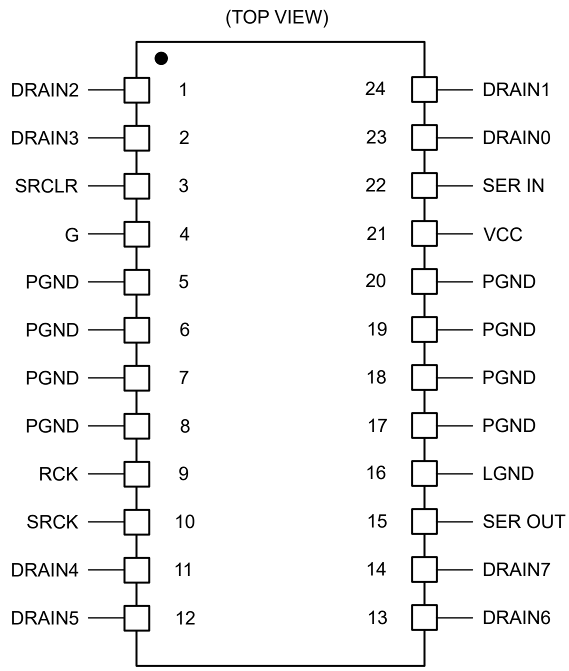


図 5-1. DW Package 24-Pin SOIC Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{SRCLR}}$	3	I	Shift register clear, active-low. The storage register transfers data to the output buffer when $\overline{\text{SRCLR}}$ is high. Driving $\overline{\text{SRCLR}}$ low clears all the registers in the device.
DRAIN0	23	O	Open-drain output
DRAIN1	24	O	Open-drain output
DRAIN2	1	O	Open-drain output
DRAIN3	2	O	Open-drain output
DRAIN4	11	O	Open-drain output
DRAIN5	12	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
$\overline{\text{G}}$	4	I	Output enable, active-low. Channel enable and disable input pin. Having $\overline{\text{G}}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
PGND	5, 6, 7, 8, 17, 18, 19, 20	—	Power ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
LGND	16	—	Signal ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	9	I	Register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK.
SER IN	22	I	Serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.
SER OUT	15	O	Serial data output of the 8-bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus.
SRCK	10	I	Serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	21	I	Power supply pin for the device. TI recommends adding a 0.1-μF ceramic capacitor close to the pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VCC	Supply voltage	–0.3	7	V
V_I	logic input voltage, CLR, EN, G1, G2, RCK, SER IN, SRCK	–0.3	7	V
V_{DS}	Power DMOS Drain-source voltage	–0.3	65	V
I_{SD}	Continuous source-to-drain diode anode current		1	A
I_{SD}	Pulsed source-to-drain diode anode current		2	A
I_D	Pulsed drain current, each output, all outputs on, T_A = 25°C		1.1	A
I_D	Continuous drain current, each output, all outputs on, T_A = 25°C		350	mA
I_D	Peak drain current single output, T_A = 25°C		1.1	A
E_{AS}	Single-pulse avalanche energy, T_A = 25°C		90	mJ
I_{AS}	Avalanche current, T_A = 25°C		500	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±7000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		5.5	V
$I_{(nom)}$	Nominal output current			350	mA
V_{IH}	High-level input voltage	2.4			V
V_{IL}	Low-level input voltage			0.7	V
I_D	Pulsed drain output current, T_A = 25°C, V_{CC} = 5 V	–1.8		0.6	A
T_A	Operating ambient temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TLC6A598 DW (SOIC-24) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	DRAIN0 to DRAIN7 Drain-to-source voltage	I_D = 1 mA	50		65	V
V_{SD}	Source-to-drain forward voltage	IF = 350 mA		0.9	1.1	V
V_{OH}	High-level output voltage	I_{OH} = –20 µA	4.9	4.99		V
	SER OUT	I_{OH} = –4 mA	4.5	4.69		
V_{OL}	Low-level output voltage	I_{OH} = 20 µA			0.02	V
	SER OUT	I_{OH} = 4 mA			0.4	
I_{IH}	High-level input current	V_I = 5 V			1	µA
I_{IL}	Low-level input current	V_I = 0 V	–1			µA
$I_{O(chop)}$	Output current at which chopping starts	T_A = 25°C	0.6	0.8	1.1	A
I_{CC}	Logic supply current	V_{CC} = 5 V, All outputs off, no clock signal		180	300	µA
		V_{CC} = 5 V, All outputs on, no clock signal		300	500	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on		360	600	µA
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5 V, T_C = 85°C		350		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V, T_A = 25°C			1	µA
		V_{DS} = 40 V, T_A = 125°C			1	
$R_{ds(on)}$	Static drain-source on-state resistance	V_{CC} = 5 V, I_D = 350 mA Single channel on, T_A = 25°C		1	1.5	Ω
$R_{ds(on)}$	Static drain-source on-state resistance	V_{CC} = 3.3 V, I_D=350 mA Single channel on, T_A = 25°C		1.1	1.6	Ω
$R_{ds(on)}$	Static drain-source on-state resistance	V_{CC} = 5 V, I_D = 150 mA Single channel on, T_A = 125°C		1.5	2.2	Ω
$R_{ds(on)}$	Static drain-source on-state resistance	V_{CC} = 3.3 V, I_D = 150 mA Single channel on, T_A = 125°C		1.6	2.3	Ω
$I_{(O\_S\_th)}$	Load open and short detection threshold		8.5	15	25	mA
$I_{(O\_S\_hys)}$	Load open and short detection threshold hysteresis			5.7		mA
$T_{SHUTDOWN}$	Thermal shutdown threshold		150	175	200	°C

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

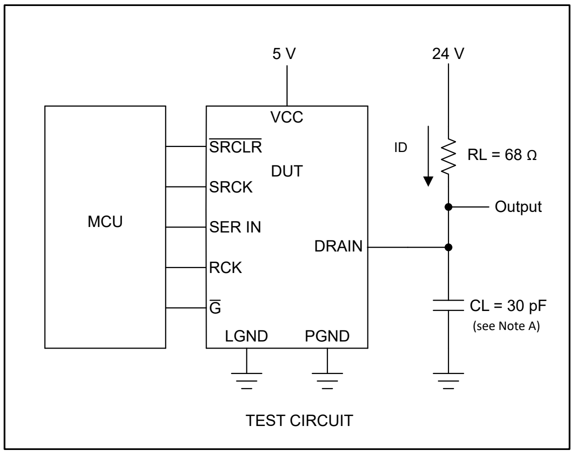
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HYS}	Thermal shutdown hysteresis			18		°C

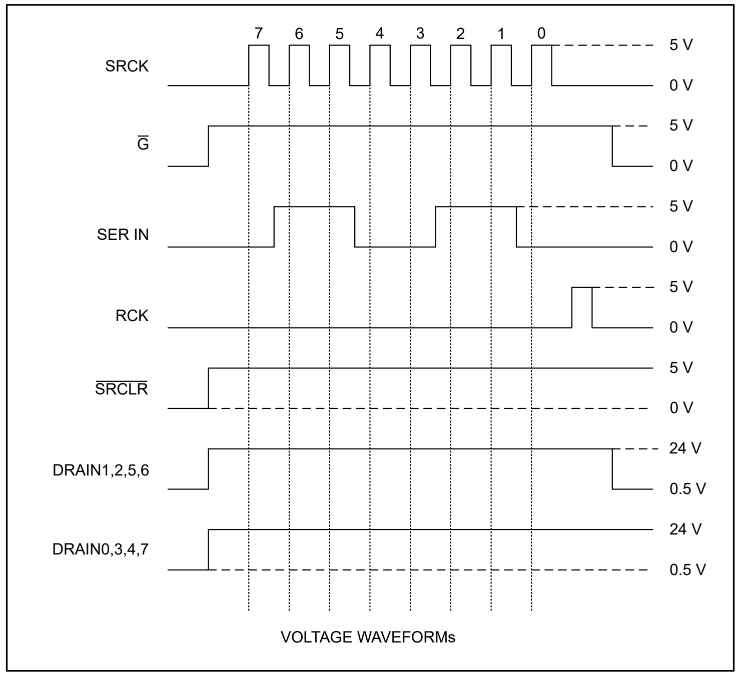
6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time from G to output, low-to-high level		30		ns
t_{PHL}	Propagation delay time from G to output, high-to-low level		22		ns
t_r	Rise time, drain output		25		ns
t_f	Fall time, drain output		35		ns
t_{pd}	Propagation delay time, SRCK falling edge to SEROUT change		10		ns
t_{or}	SEROUT rise time (10% to 90%)		3		ns
t_{of}	SEROUT fall time (90% to 10%)		2		ns
f_{SRCK}	Serial clock frequency			10	MHz
t_{SRCK_WH}	SRCK pulse duration, high	30			ns
t_{SRCK_WL}	SRCK pulse duration, low	30			ns
t_{su}	Setup time, SER IN high before SRCK rise	10			ns
t_h	Hold time, SER IN high after SRCK rise	10			ns
t_w	SER IN pulse duration	20			ns
t_a	Reverse-recovery-current rise time		80		ns
t_{rr}	Reverse-recovery time		100		ns
t_d	Last SRCK rise to RCK rise	200			ns

6.7 Timing Waveforms

図 6-1 shows the resistive-load test circuit and voltage waveforms. One can see from 図 6-1 that with $\overline{G}$ held low and $\overline{SRCLR}$ held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.





A. C_L includes probe and jig capacitance.

図 6-1. Resistive Load Operation

図 6-2 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see the *Functional Block Diagram*). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

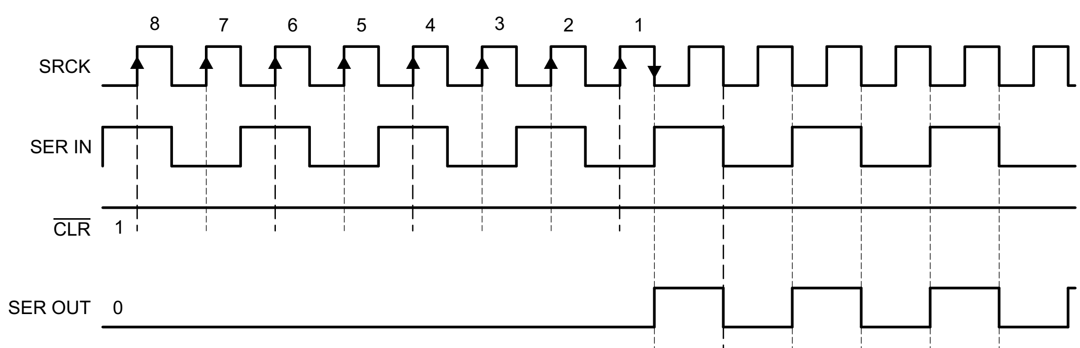
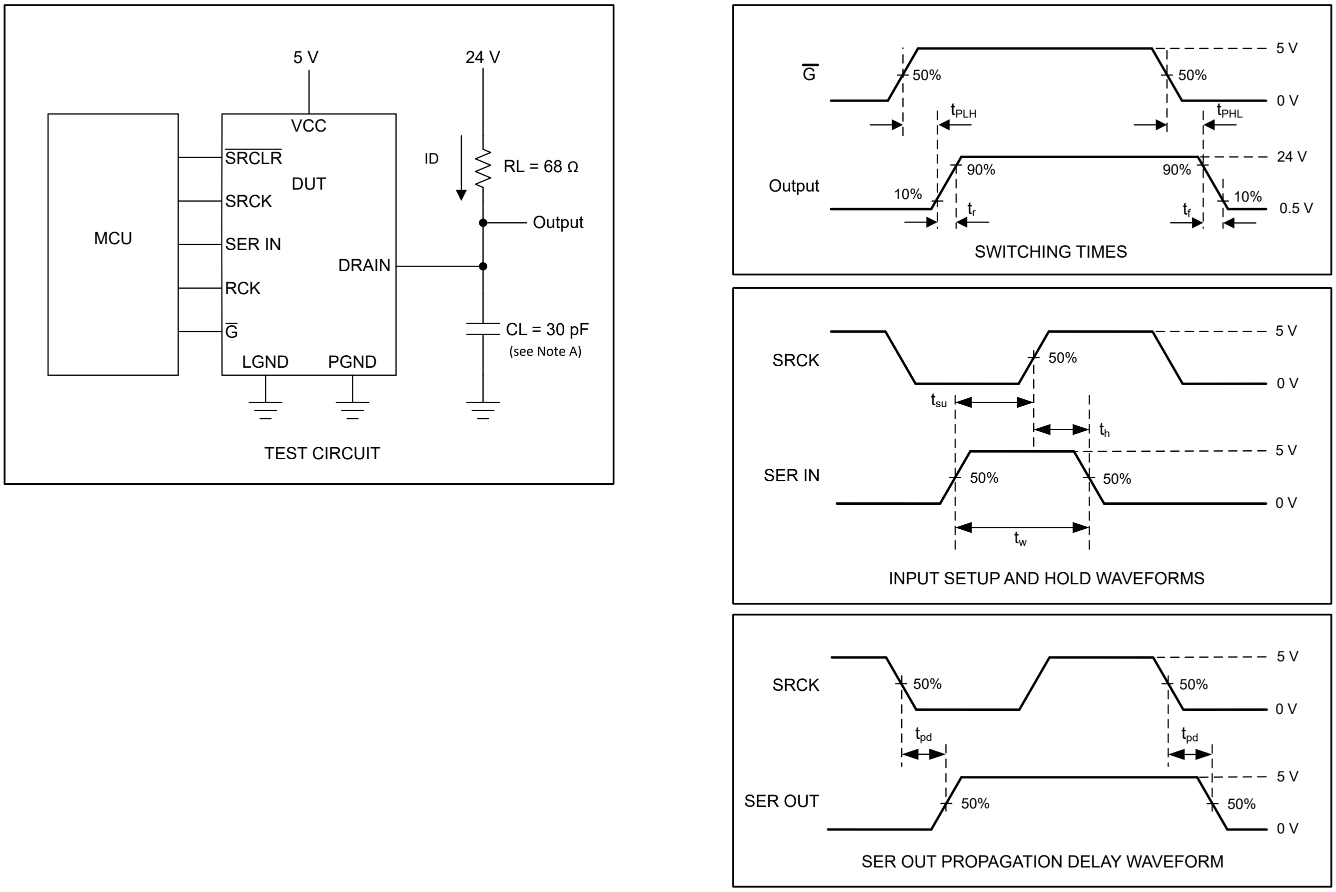


図 6-2. SER IN to SER OUT Waveform

図 6-3 shows the test circuit, switching times, and voltage waveforms.



A. C_L includes probe and jig capacitance.

図 6-3. Switching Times and Voltage Waveforms

6.8 Typical Characteristics

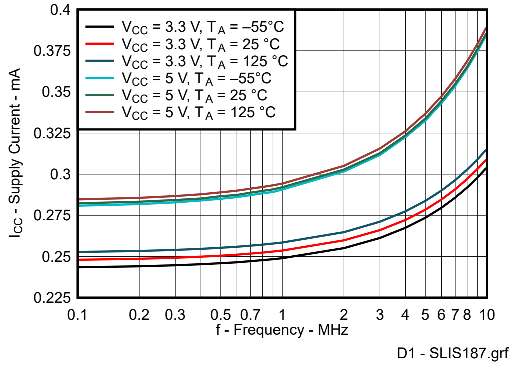


図 6-4. Supply Current vs Frequency

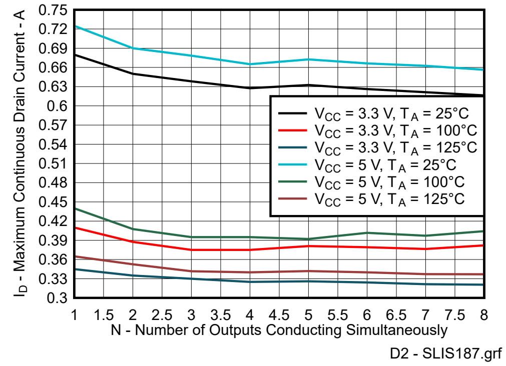
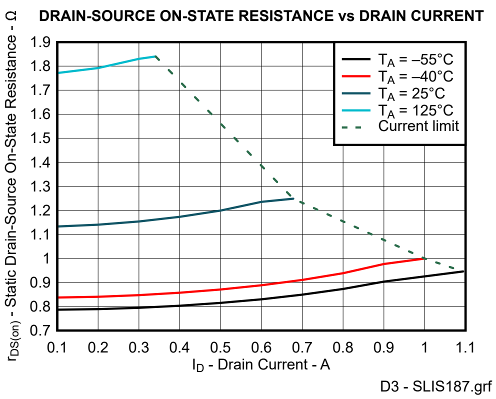
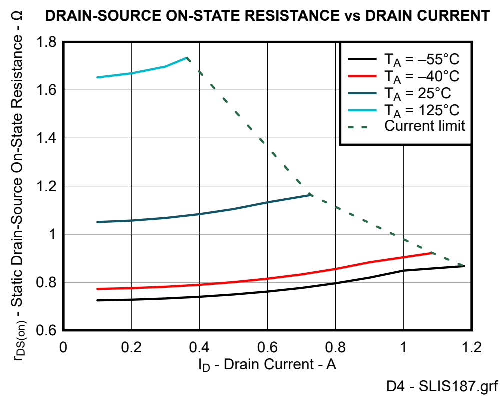


図 6-5. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously



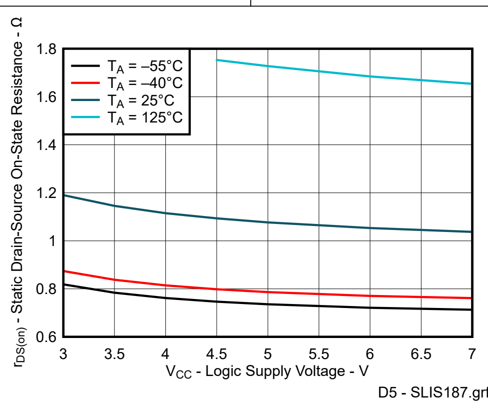
V_{CC} = 3.3 V, T_A = 25 °C

図 6-6. Static Drain-to-Source On-State Resistance vs Drain Current



V_{CC} = 5 V, T_A = 25 °C

図 6-7. Static Drain-to-Source On-State Resistance vs Drain Current

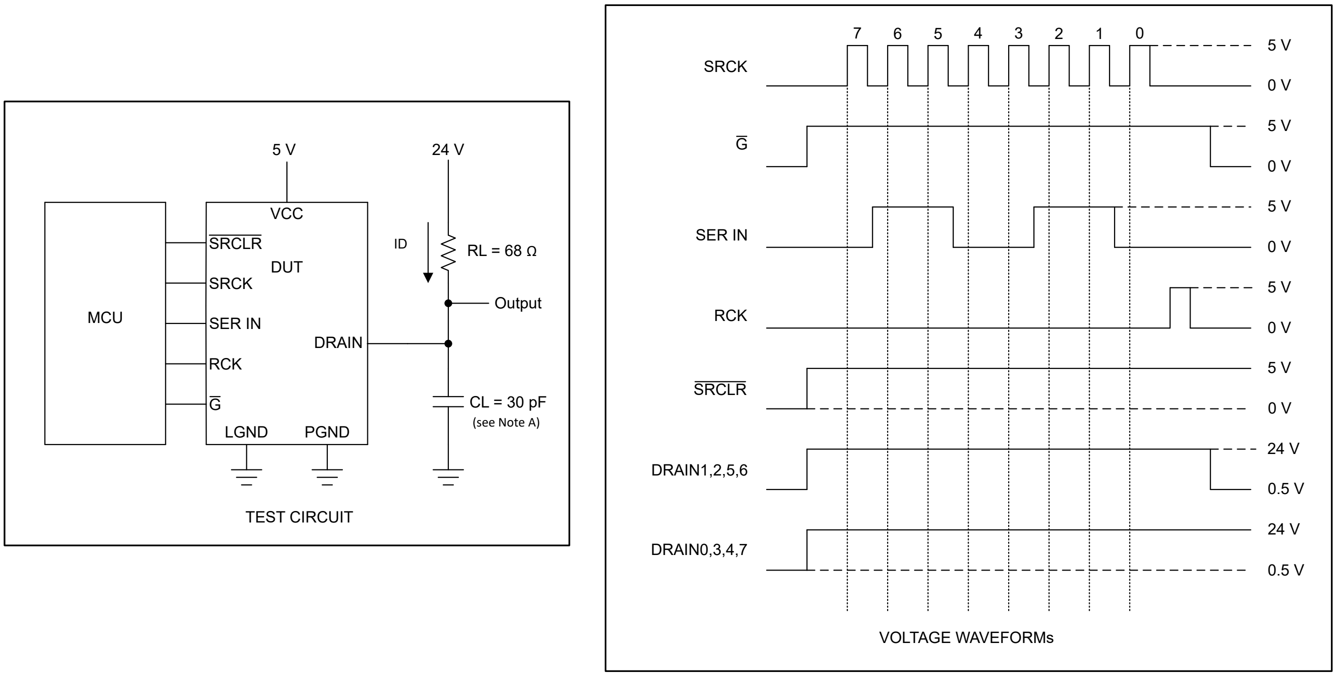


All channels on, I_{DS} = 350 mA

図 6-8. Static Drain-to-Source On-State Resistance vs Supply Voltage

7 Parameter Measurement Information

図 7-1 shows the resistive-load test circuit and voltage waveforms. One can see from 図 7-1 that with $\overline{G}$ held low and $\overline{SRCLR}$ held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.



A. C_L includes probe and jig capacitance.

図 7-1. Resistive-Load Test Circuit and Voltage Waveforms

図 7-2 shows the reverse recovery current test circuit and waveforms of source to drain diode.

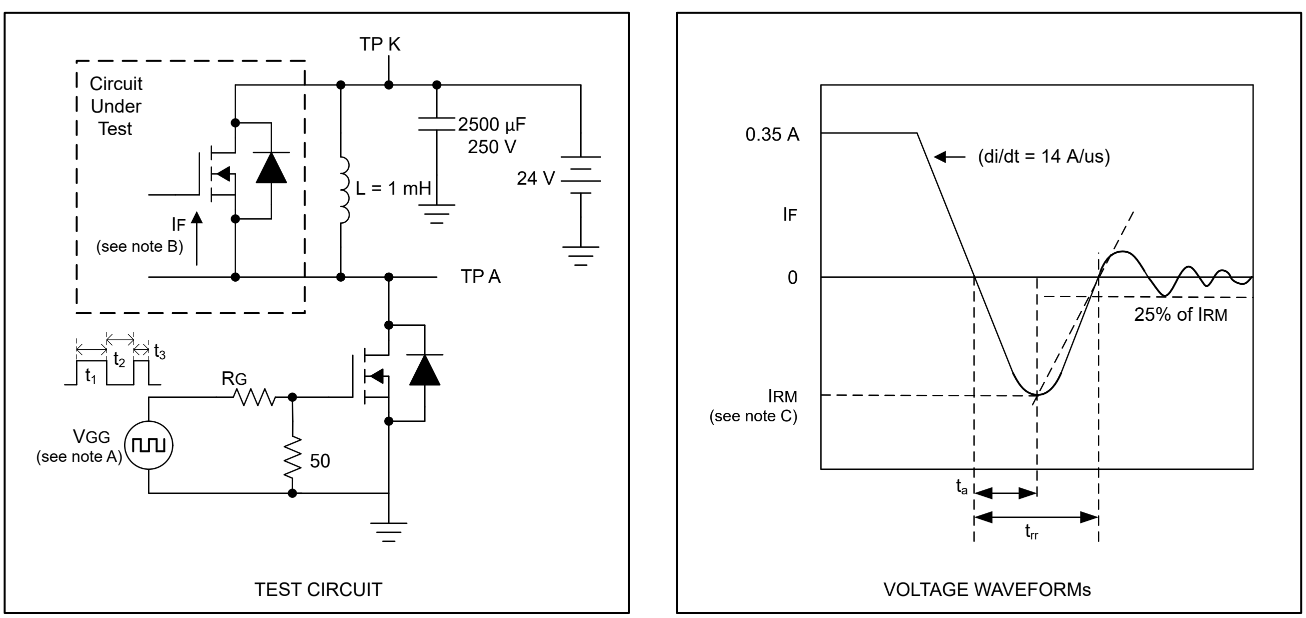


図 7-2. Reverse Recovery Current Test Circuit and Waveforms of Source to Drain Diode

Note

A. The V_{GG} amplitude and R_G are adjusted for di/dt = 14 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.

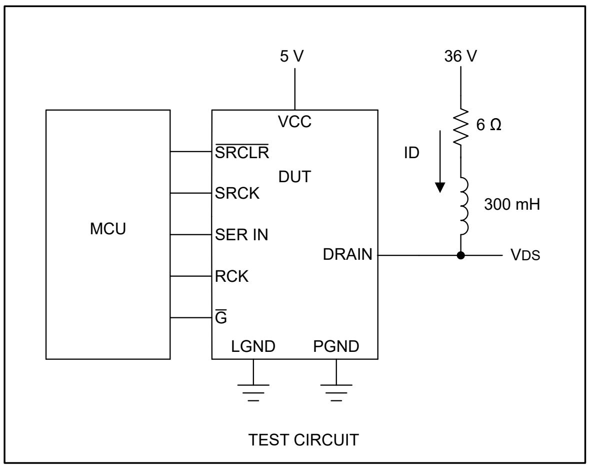
Note

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Note

C. I_{RM} = maximum recovery current.

図 7-3 shows the single pulse avalanche energy test circuit and waveforms.



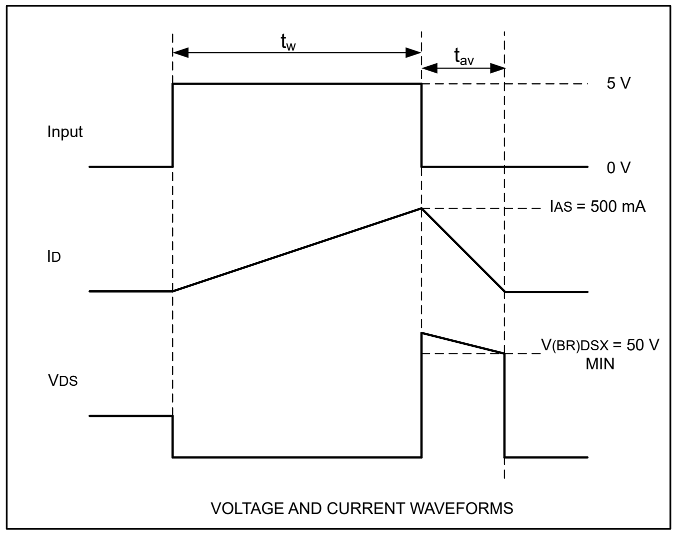


図 7-3. Single Pulse Avalanche Energy Test Circuit and Waveforms

Note

A. The MCU has the following characteristics: t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

Note

B. Input pulse duration, tw, is increased until peak current I_{AS} = 500 mA.

Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av}) / 2$ = 90 mJ.

8 Detailed Description

8.1 Overview

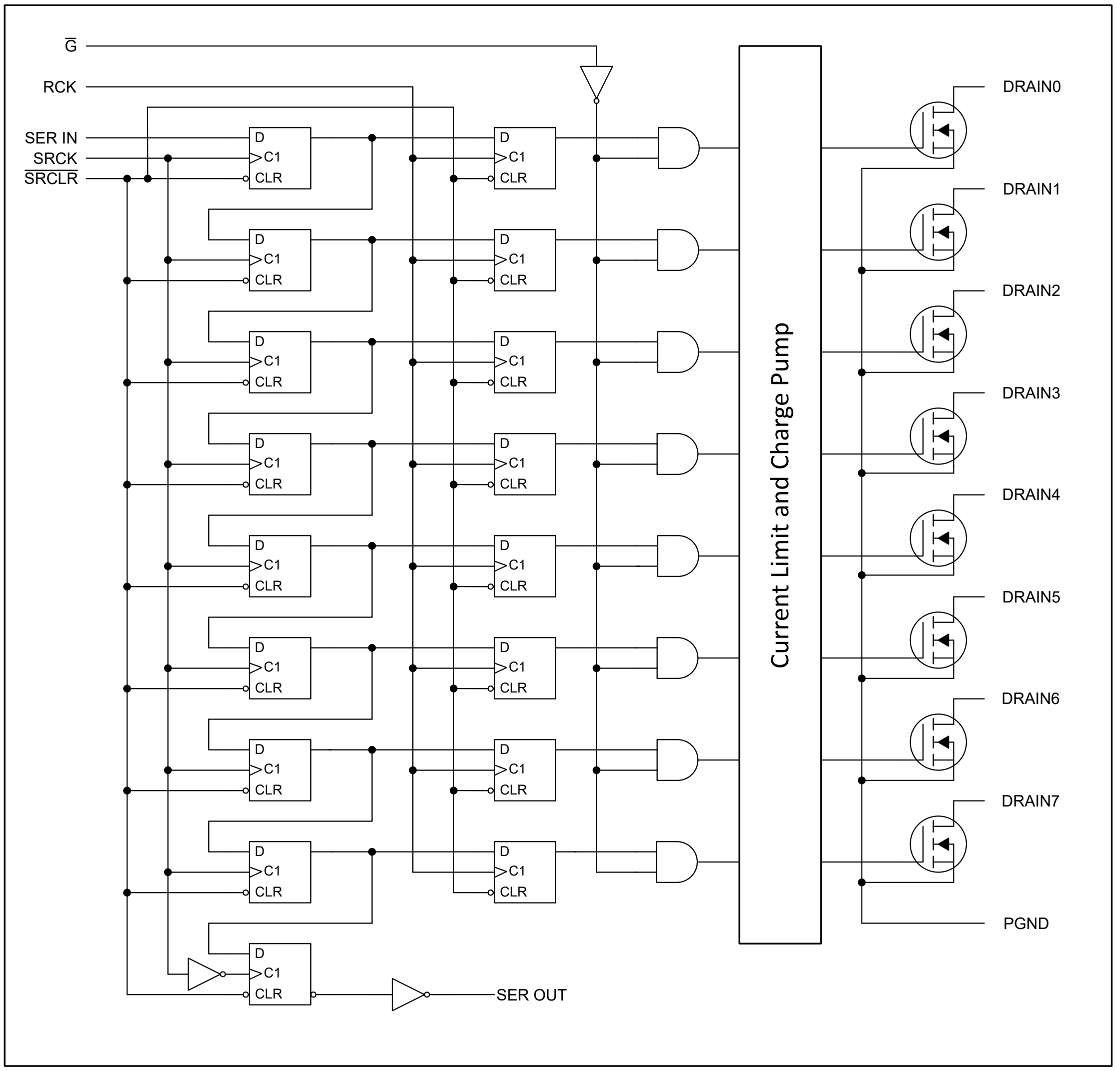
The TLC6A598 device is a monolithic, high-voltage, high-current 8-bit shift register designed to drive relatively high load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other low-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift register clear (CLR) is high. When CLR is low, all registers in the device are cleared. When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. When G is held low, data from the storage register transfers to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability.

The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This action provides improved performance for applications where clock signals can be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50-V and 350-mA continuous sink-current capability. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 7000 V of ESD protection when tested using the human body model and the 1500 V machine model.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial-In Interface

The TLC6A598 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfer through the shift and storage registers is on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high.

8.3.2 Clear Registers

A logic low on the $\overline{\text{SRCLR}}$ pin clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.3 Output Channels

DRAIN0–DRAIN7. These pins can survive up to 50-V LED supply voltage.

8.3.4 Register Clock

RCK is the storage-register clock. Data in the storage register appears at the output whenever the output enable ($\overline{\text{G}}$) input signal is high.

8.3.5 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus in cascade, the data transfers to the next device on the falling edge of SRCK. This connection can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input on the same rising edge of SRCK.

8.3.6 Output Control

Holding the output enable (pin $\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{\text{G}}$ low makes data from the storage register transferred to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sinking current. This pin also can be used for global PWM dimming.

8.3.7 Clamping Structure

When switching off inductive loads, the potential at pin OUT rises to VDS(CL) potential, because the inductance intends to continue driving the current. The clamping voltage is necessary to prevent destruction of the device. See 図 8-1 for the clamping circuit principle. Nevertheless, the maximum allowed load inductance is limited.

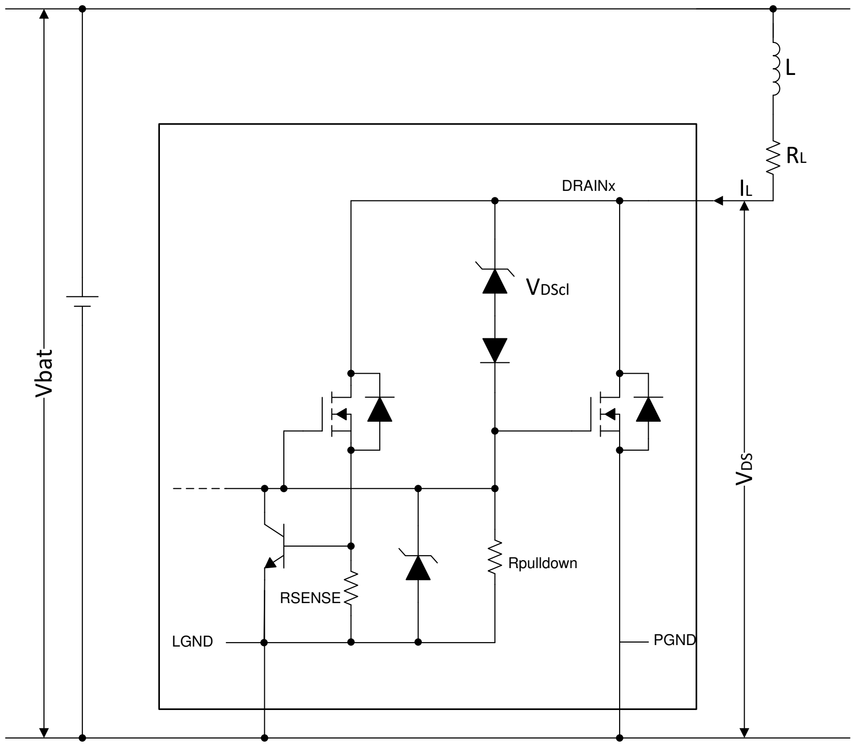


図 8-1. Output Clamp Implementation

During demagnetization of inductive loads, energy has to be dissipated in the TLC6A598. This energy can be calculated with 式 1:

$$E = V_{DS(CL)} \times \left[\frac{V_{bat} - V_{DS(CL)}}{R_L} \times ln\left(1 - \frac{R_L \times I_L}{V_{bat} - V_{DS(CL)}}\right) + I_L\right] \times \frac{L}{I_L} \tag{1}$$

The 式 2 simplifies under the assumption of $R_L = 0$:

$$E = \frac{1}{2} \times L \times {I_L}^2 \times \left(1 - \frac{V_{bat}}{V_{bat} - V_{DS(CL)}}\right) \tag{2}$$

The thermal design of the component limits the maximum energy, which is converted into heat.

8.3.8 Protection Functions

8.3.8.1 Overcurrent Protection

When any output is in on status (the corresponding Data Register bit is set to ‘1’), if the output current through the MOS is sensed to be larger than I_{OK}, it enters chopping mode as below.

図 8-2 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, For example, an incandescent lamp. In region 1, chopping occurs and the peak current is limited to $I_{O(chop)}$. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

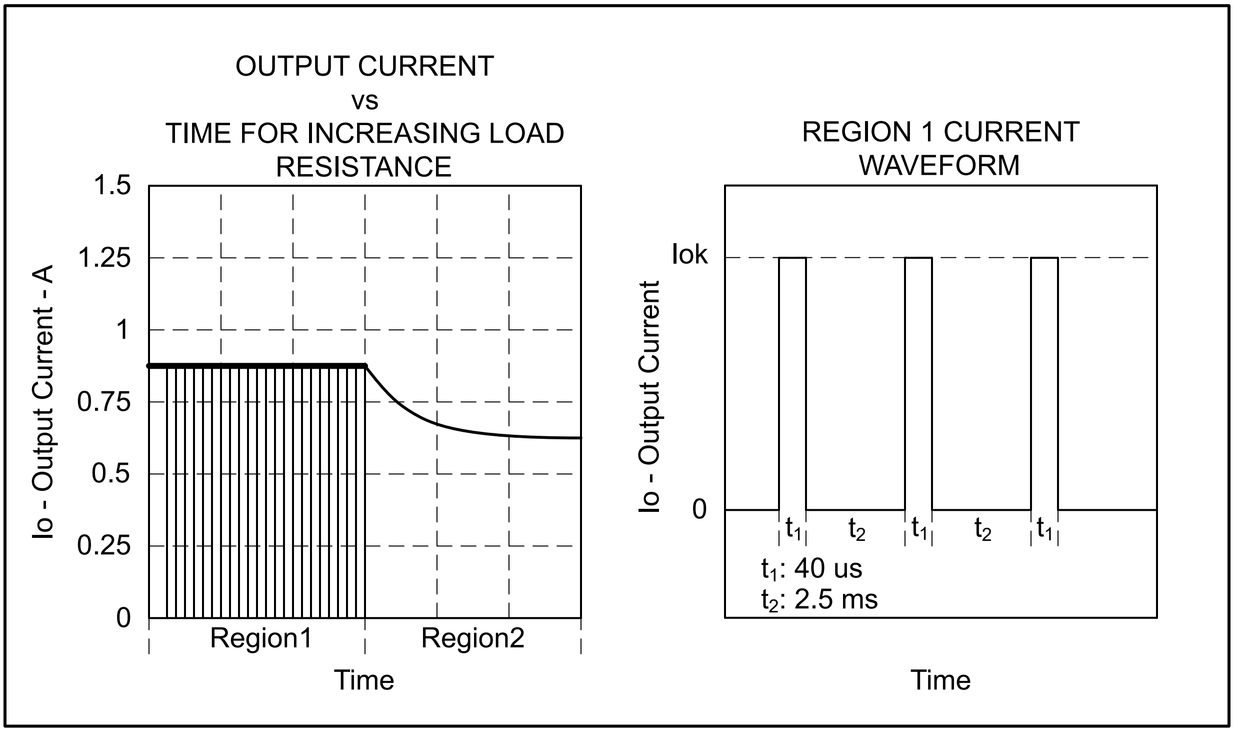


図 8-2. Chopping-Mode Characteristics

Note

Region 1 duty cycle is approximately 2%.

8.3.8.2 Output Detection

When any output is in on status (the corresponding Data Register bit is set to ‘1’), if the current goes through any output is sensed to be lower than I_{OS_th} mA, then an open load condition or short to ground fault is reported to the fault register while the output does not close automatically.

For the inductive load, during the on status of any output, TI recommends to read the fault regs two times. Because the inductive load leads to error detection results and it needs ignore the first time readout results during the set up process of the output current, TI recommends to read the fault regs again after the current through the load is stable.

8.3.8.3 Serial Communication Error

The device provides a cyclic redundancy check to verify register values in the shift registers. In read back mode, the device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct to determine whether the communication loop between MCU and device is good. Shift-Register Communication-Fault Detection gives a detailed description of the CRC check.

8.3.8.4 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. After the junction temperature decreases below 160°C (typical), the device begins to operate again.

8.3.9 Interface

8.3.9.1 Register Write

The TLC6A598 device has a 8-bit configuration register. Data transfers through the shift registers on the rising edge of SRCK and latches into the storage registers on the rising edge of RCK. The data bits control 8 open-drain outputs independently.

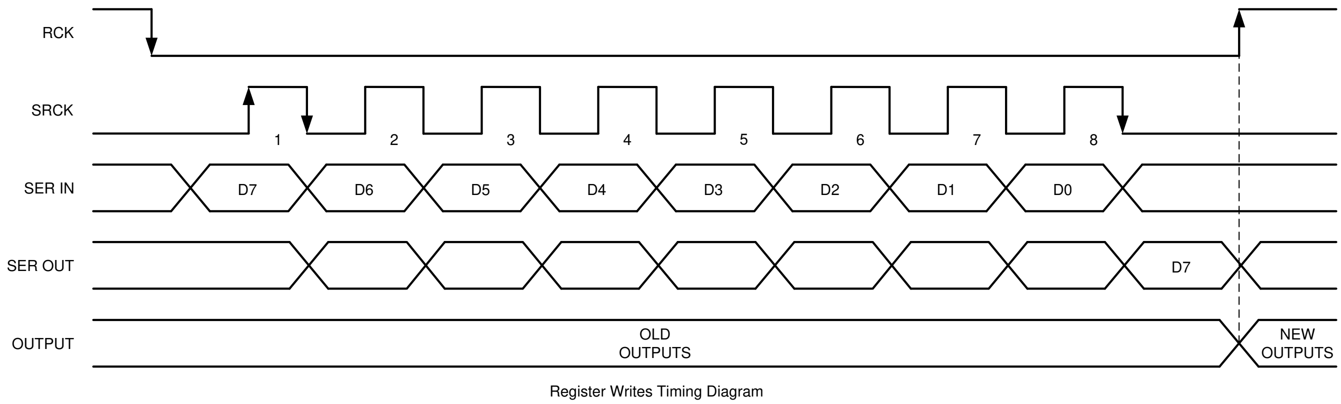


図 8-3. Register Write Timing Diagram

8.3.9.2 Register Read

The fault information loads to shift registers on the rising edge of RCK and can be read out on SER OUT. 図 8-4 shows on the rising edge of the RCK signal, the MSB data "DRAIN7_OCP" appears on the SER OUT pin. On each falling edge of SRCK signal, there is 1 bit of data shifted out on the SER OUT pin. There is a total of 24 bits in the fault information registers. *REgister Maps* describes the details.

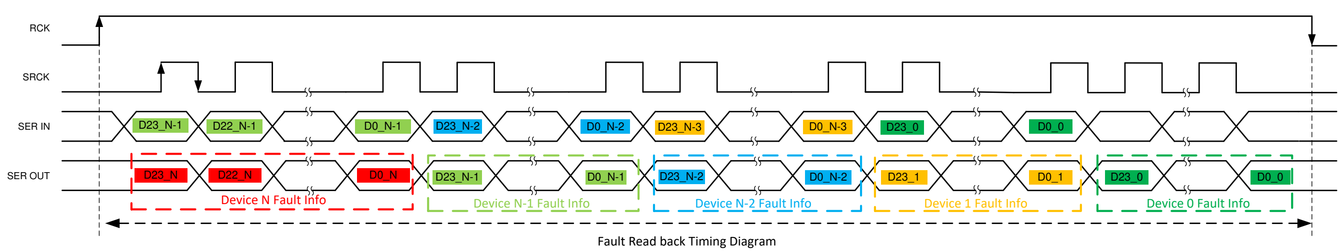


図 8-4. Register Read Timing Diagram

8.3.9.3 Shift-Register Communication-Fault Detection

The TLC6A598 device provides a cyclic redundancy check to verify register values in the shift registers. In read back mode, the TLC6A598 device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct. The CRC checksum provides a read back method to verify shift register values without altering them.

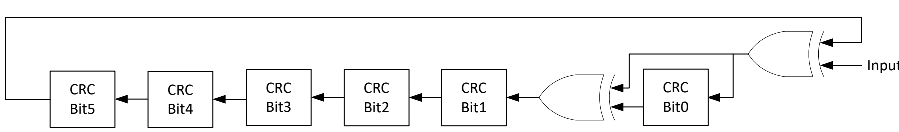


図 8-5. CRC Check Block Diagram

The TLC6A598 device also checks the configuration register for faulty commands. The TLC6A598 configuration register consists of 8 bits. To generate the CRC checksum, the device first shifts left 6 bits and appends 0s, then bit-wise exclusive-ORs the 14 data bits with the polynomial to get the checksum.

For example, if the configuration data is 0xFF and the polynomial is 0x43 (7’b1000011), the CRC checksum is 0x0D (6’b00 1101).

The MCU can read back the CRC checksum and append it to the LSB of 8 bits, and then the 14 bits of data becomes 0x3FCD. Performing the bit-wise exclusive-OR operation with the polynomial must lead to a residual of 0.

8.4 Device Functional Modes

8.4.1 Operation With V_{CC} < 3 V

This device works normally within the range 3 V ≤ V_{CC} ≤ 5.5 V. When the operating voltage is lower than 3 V, correct behavior of the device, including communication interface and current capability, is not assured.

8.4.2 Operation With 5.5 V ≤ V_{CC} ≤ 7 V

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

8.5 Register Maps

表 8-1. Register Map

CONFIGURATION REGISTER								
Field name	DRAIN7	DRAIN6	DRAIN5	DRAIN4	DRAIN3	DRAIN2	DRAIN1	DRAIN0
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	7	6	5	4	3	2	1	0
FAULT READBACK REGISTER								
Bit	23	22	21	20	19	18	17	16
Field name	DRAIN7_OCP	DRAIN6_OCP	DRAIN5_OCP	DRAIN4_OCP	DRAIN3_OCP	DRAIN2_OCP	DRAIN1_OCP	DRAIN0_OCP
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	15	14	13	12	11	10	9	8
Field name	DRAIN7_OorS	DRAIN6_OorS	DRAIN5_OorS	DRAIN4_OorS	DRAIN3_OorS	DRAIN2_OorS	DRAIN1_OorS	DRAIN0_OorS
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	7	6	5	4	3	2	1	0
Field name	TBD	TSD	CRC					
Default value	0h	0h	0h					

表 8-2 lists the memory-mapped registers for the interface.

表 8-2. Interface Registers

OFFSET	ACRONYM	REGISTER NAME	SECTION
0h	Config	Configuration Register	
1h	Fault_Readback	Fault Readback Register	

表 8-3. Interface Access Type Codes

	CODE	DESCRIPTION
Read type	R	Read-only
Read to clear	RC	Read to clear the fault
Write	W	Write-only
Reset or Default Value	-n	Value after reset or the default value

8.5.1 Configuration Register(Offset=0h)[reset=0h]

Configuration register is shown in 表 8-4and described in 表 8-5.

表 8-4. Configuration Register

7	6	5	4	3	2	1	0
DRAIN7	DRAIN6	DRAIN5	DRAIN4	DRAIN3	DRAIN2	DRAIN1	DRAIN0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

表 8-5. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRAIN7	W	0h	• Open-drain output bit for DRAIN7 • HIGH=Output power switch enabled • LOW=Output power switch disabled
6	DRAIN6	W	0h	• Open-drain output bit for DRAIN6 • HIGH=Output power switch enabled • LOW=Output power switch disabled
5	DRAIN5	W	0h	• Open-drain output bit for DRAIN5 • HIGH=Output power switch enabled • LOW=Output power switch disabled
4	DRAIN4	W	0h	• Open-drain output bit for DRAIN4 • HIGH=Output power switch enabled • LOW=Output power switch disabled
3	DRAIN3	W	0h	• Open-drain output bit for DRAIN3 • HIGH=Output power switch enabled • LOW=Output power switch disabled
2	DRAIN2	W	0h	• Open-drain output bit for DRAIN2 • HIGH=Output power switch enabled • LOW=Output power switch disabled
1	DRAIN1	W	0h	• Open-drain output bit for DRAIN1 • HIGH=Output power switch enabled • LOW=Output power switch disabled
0	DRAIN0	W	0h	• Open-drain output bit for DRAIN0 • HIGH=Output power switch enabled • LOW=Output power switch disabled

8.5.2 Fault Readback Register(Offset=1h)[reset=0h]

Fault readback is shown in 表 8-6 and described in 表 8-7.

表 8-6. Fault Readback Register

23	22	21	20	19	18	17	16
DRAIN7_OCP	DRAIN6_OCP	DRAIN5_OCP	DRAIN4_OCP	DRAIN3_OCP	DRAIN2_OCP	DRAIN1_OCP	DRAIN0_OCP
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h
15	14	13	12	11	10	9	8
DRAIN7_OorS	DRAIN6_OorS	DRAIN5_OorS	DRAIN4_OorS	DRAIN3_OorS	DRAIN2_OorS	DRAIN1_OorS	DRAIN0_OorS
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

表 8-6. Fault Readback Register (continued)

23	22	21	20	19	18	17	16
7	6	5	4	3	2	1	0
TBD	TSD	CRC					
RC-0h	RC-0h	RC-0h					

表 8-7. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
23	DRAIN7_OCP	RC	0h	• Over current fault flag for DRAIN7, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
22	DRAIN6_OCP	RC	0h	• Over current fault flag for DRAIN6, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
21	DRAIN5_OCP	RC	0h	• Over current fault flag for DRAIN5, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
20	DRAIN4_OCP	RC	0h	• Over current fault flag for DRAIN4, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
19	DRAIN3_OCP	RC	0h	• Over current fault flag for DRAIN3, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
18	DRAIN2_OCP	RC	0h	• Over current fault flag for DRAIN2, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
17	DRAIN1_OCP	RC	0h	• Over current fault flag for DRAIN1, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
16	DRAIN0_OCP	RC	0h	• Over current fault flag for DRAIN0, read to clear the fault • HIGH=Over current fault detected • LOW=Over current fault not detected
15	DRAIN7_OorS	RC	0h	• Open or short to ground fault flag for DRAIN7, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
14	DRAIN6_OorS	RC	0h	• Open or short to ground fault flag for DRAIN6, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
13	DRAIN5_OorS	RC	0h	• Open or short to ground fault flag for DRAIN5, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected

表 8-7. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	DRAIN4_OorS	RC	0h	• Open or short to ground fault flag for DRAIN4, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
11	DRAIN3_OorS	RC	0h	• Open or short to ground fault flag for DRAIN3, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
10	DRAIN2_OorS	RC	0h	• Open or short to ground fault flag for DRAIN2, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
9	DRAIN1_OorS	RC	0h	• Open or short to ground fault flag for DRAIN1, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
8	DRAIN0_OorS	RC	0h	• Open or short to ground fault flag for DRAIN0, read to clear the fault • HIGH=Open or short to ground fault detected • LOW=Open or short to ground fault not detected
7	TBD	RC	0h	TBD
6	TSD	RC	0h	• Thermal-shutdown detection flag, read to clear the fault • HIGH = Thermal shutdown detected • LOW = Thermal shutdown not detected
5	CRC	R	0h	CRC checksum of configuration registers
4				
3				
2				
1				
0				

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TLC6A598 device is a serial-in, parallel-out, power and logic, 8-bit shift register with low-side open-drain DMOS output ratings of 50-V and 350-mA continuous sink-current capabilities when VCC = 5 V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 7000 V of ESD protection when tested using the human body model and 1500 V when using the machine model.

The serial output (SEROUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. Connect the device (SEROUT) pin to the next device (SERIN) for daisy chain. This connection provides improved performance for applications where clock signals can be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

9.2 Typical Application 1

図 9-1 shows a typical application circuit with TLC6A598 to drive LEDs. The MCU generates all the input signals.

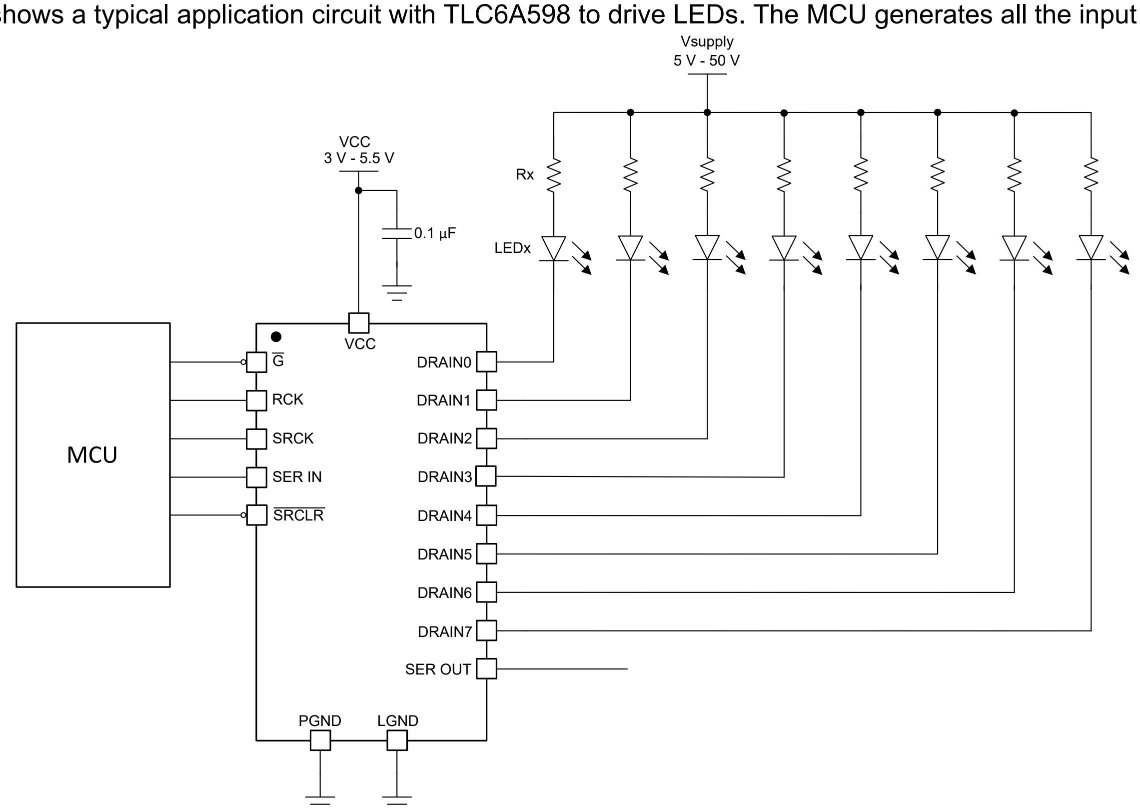


図 9-1. Typical Application With TLC6A598 to Drive LEDs

9.2.1 Design Requirements

表 9-1. System Specifications

DESIGN PARAMETER	DESCRIPTION	EXAMPLE VALUE
V_{supply}	Supply voltage for the LED strings	5 V to 50 V
V_{CC}	Supply voltage for the TLC6A598	3 V to 5.5 V
V_{LED}	LED forward voltage	3.3 V (typical)
I_{LED}	LED current	50 mA to 350 mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- V_{supply}: LED supply voltage
- V_{LEDx}: LED forward voltage
- I_{LED}: LED current
- R_{ON}: Resistance for each output channels when it is on, 1-Ω typical, T_A = 25°C

With these parameters determined, the resistor in series with the LED can be calculated by using the 式 3:

$$R_X = \frac{\left(V_{supply} - V_{LED}\right)}{I_{LED}} - R_{ON} \quad (3)$$

9.2.3 Application Curves

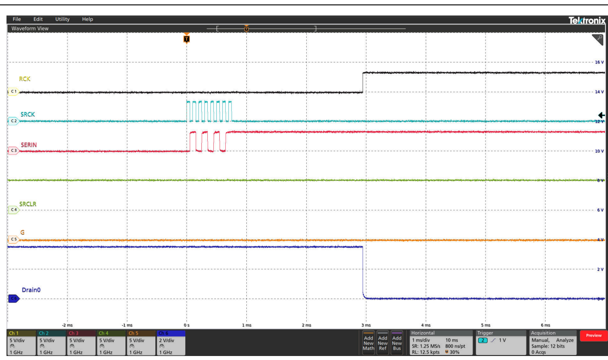


図 9-2. Turn on Drain0/2/4/6

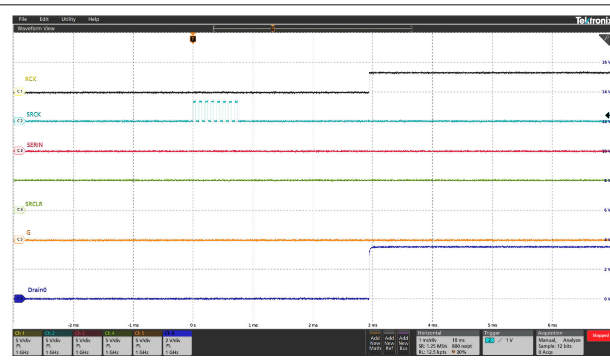


図 9-3. Turn off Drain0/2/4/6

9.3 Typical Application 2

図 9-4 shows a typical cascade application circuit with two TLC6A598 chips configured in cascade topology. The MCU generates all the input signals.

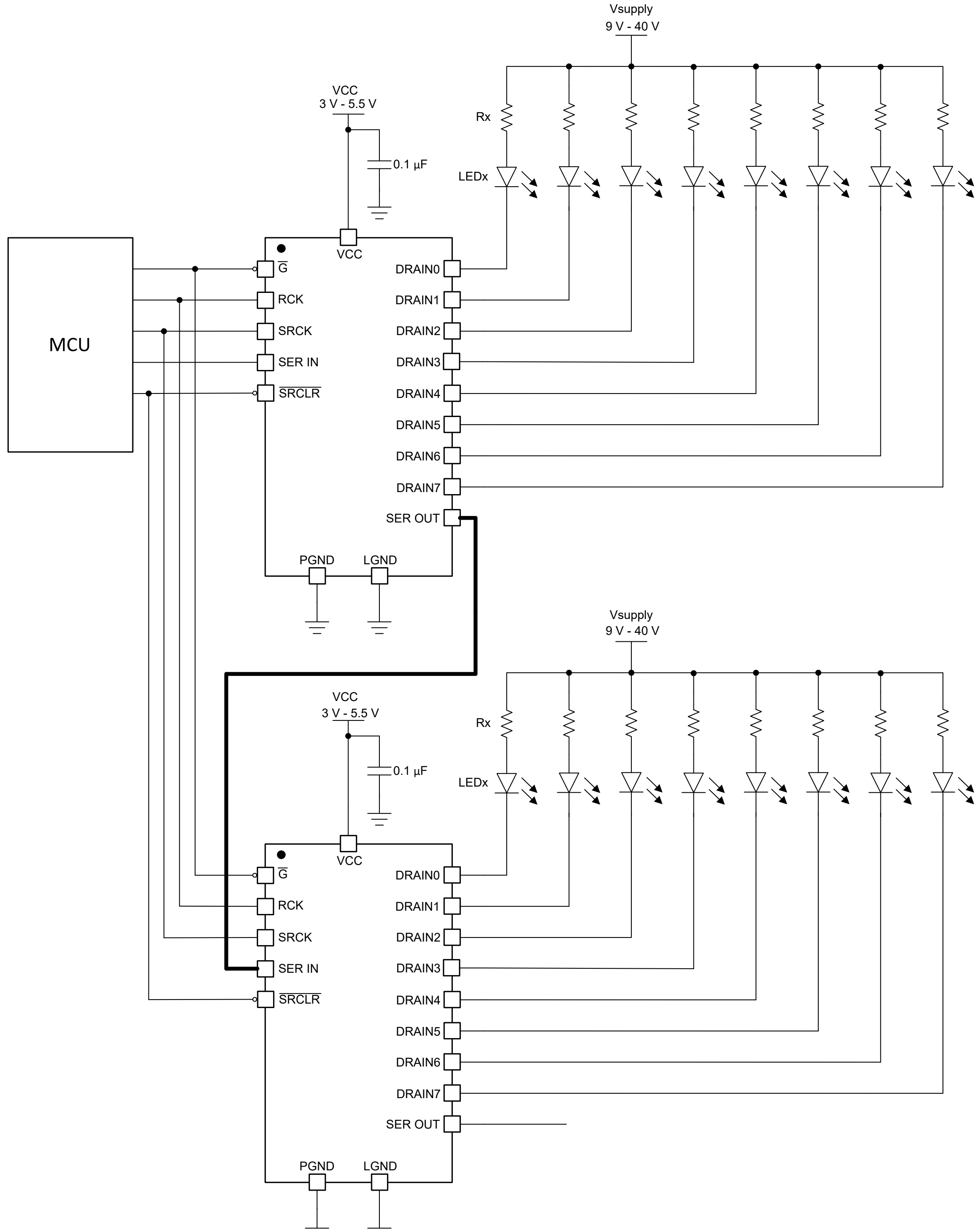


図 9-4. Typical Application With Cascade TLC6A598

9.3.1 Design Requirements

表 9-2. System Specifications

DESIGN PARAMETER	DESCRIPTION	EXAMPLE VALUE
V_{supply}	Supply voltage for the LED strings	5 V to 50 V
V_{CC}	Supply voltage for the TLC6A598	3 V to 5.5 V
V_{LED}	LED forward voltage	3.3 V (typical)
I_{LED}	LED current	50 mA to 350 mA

9.3.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- V_{supply}: LED supply voltage
- V_{LEDx}: LED forward voltage
- I_{LED}: LED current
- R_{ON}: Resistance for each output channels when it is on, 1-Ω typical, T_A = 25°C

With these parameters determined, the resistor in series with the LED can be calculated by using the 式 4:

$$R_X = \frac{\left(V_{supply} - V_{LED}\right)}{I_{LED}} - R_{ON} \tag{4}$$

9.4 Typical Application 3

図 9-5 shows a typical application circuit with TLC6A598 to drive Relays. The MCU generates all the input signals.

Please note that inductive loads, such as stepper motors or relays, can generate negative transients on the DRAINx pins of the device. Typically, this event occurs when the output channel FET turns ON, pulling the DRAINx node to ground. This event can cause the DRAINx node to go below the voltage rating listed in the Absolute Maximum Ratings table, which in effect causes excessive ground current leakage.

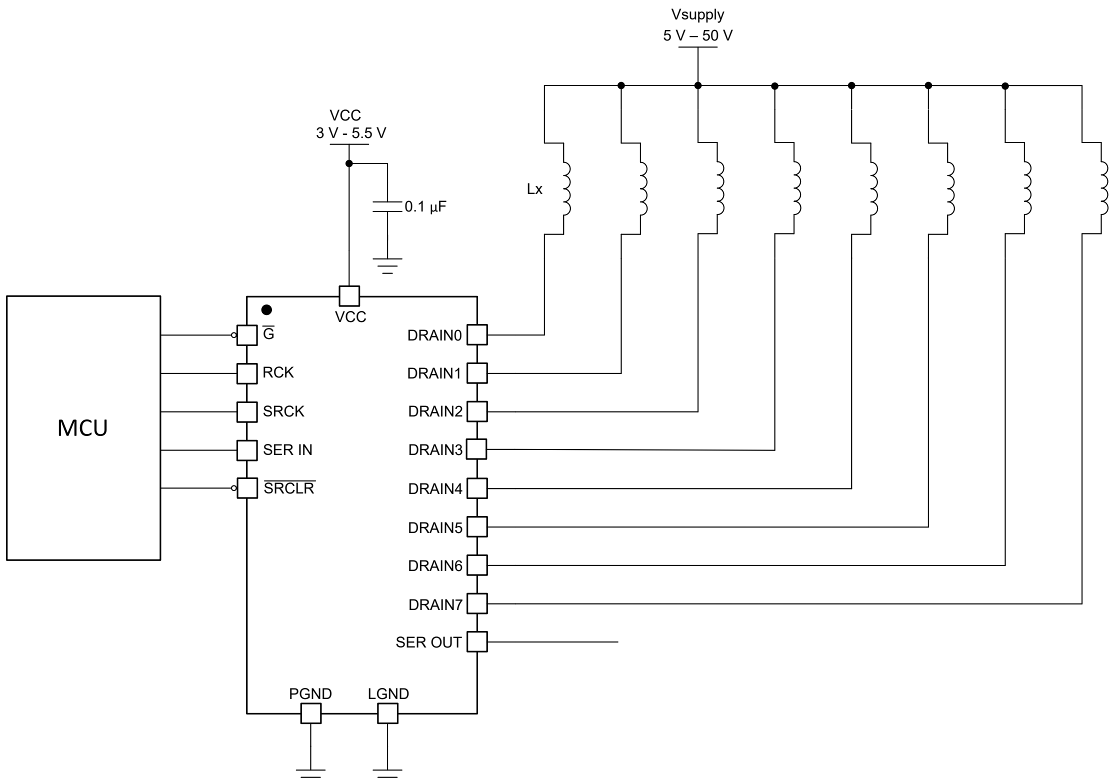


図 9-5. Typical Application With TLC6A598 to Drive Relays

9.4.1 Design Requirements

表 9-3. System Specifications

DESIGN PARAMETER	DESCRIPTION	EXAMPLE VALUE
V_{supply}	Supply voltage for the coil	5 V to 50 V
V_{CC}	Supply voltage for the TLC6A598	3 V to 5.5 V
I_{COIL}	Output current for the coil	30 mA to 350 mA

9.4.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters, as follows:

- V_{supply}: LED supply voltage
- R_{COIL}: Coil resistance
- R_{ON}: Resistance for each output channels when it is on, 1-Ω typical, T_A = 25°C

With these parameters determined, the coil current can be calculated by using the 式 5:

$$I_{COIL} = \frac{V_{supply}}{R_{COIL} + R_{ON}} \quad (5)$$

10 Power Supply Recommendations

The TLC6A598 device is designed to operate with an input voltage supply range from 3 V to 5.5 V. This input supply must be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirements for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pins.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.

All thermal vias must be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

11.2 Layout Example

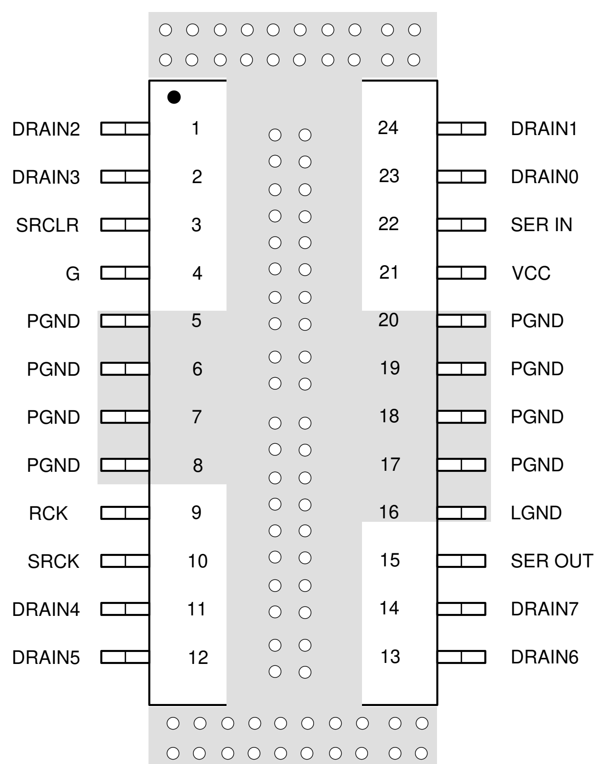


図 11-1. TLC6A598 Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6A598MDWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC6A598M
TLC6A598MDWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC6A598M
TLC6A598MDWRG4.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC6A598M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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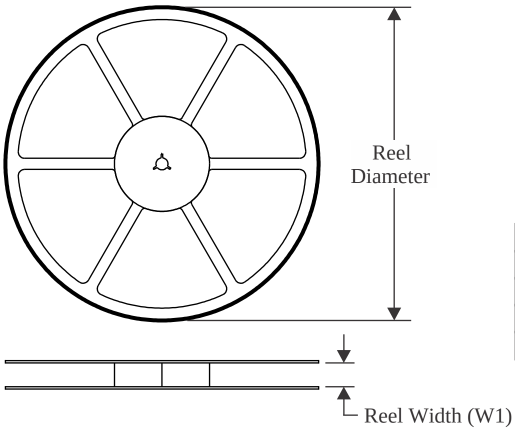
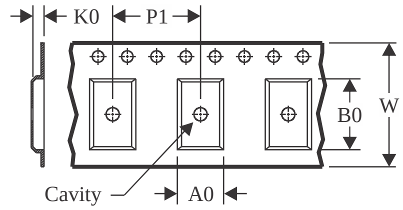
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

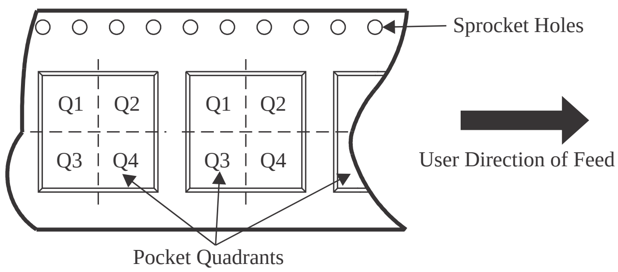


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

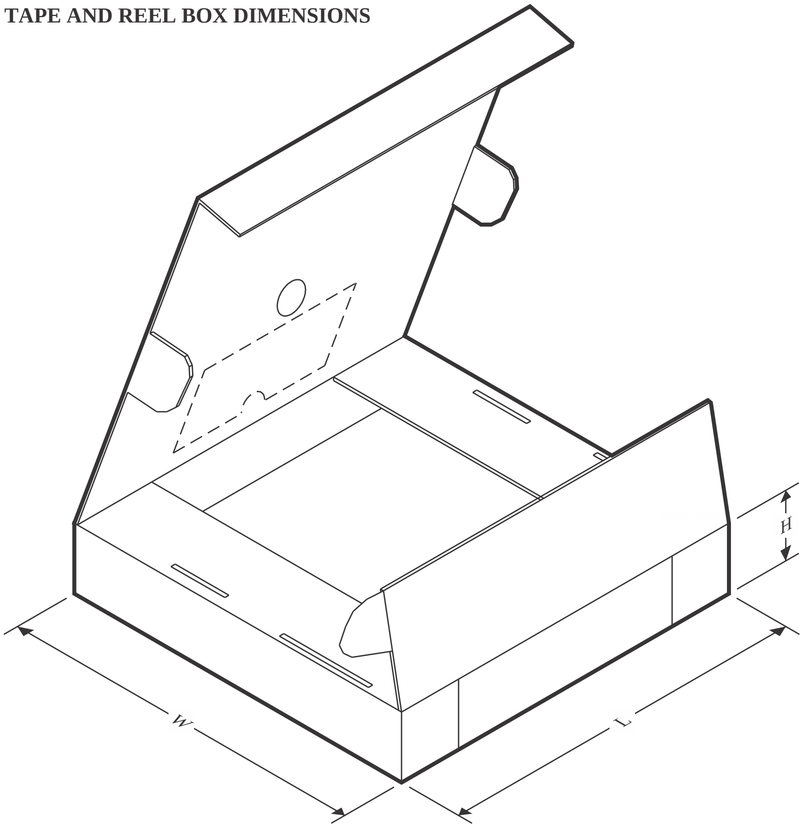
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6A598MDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

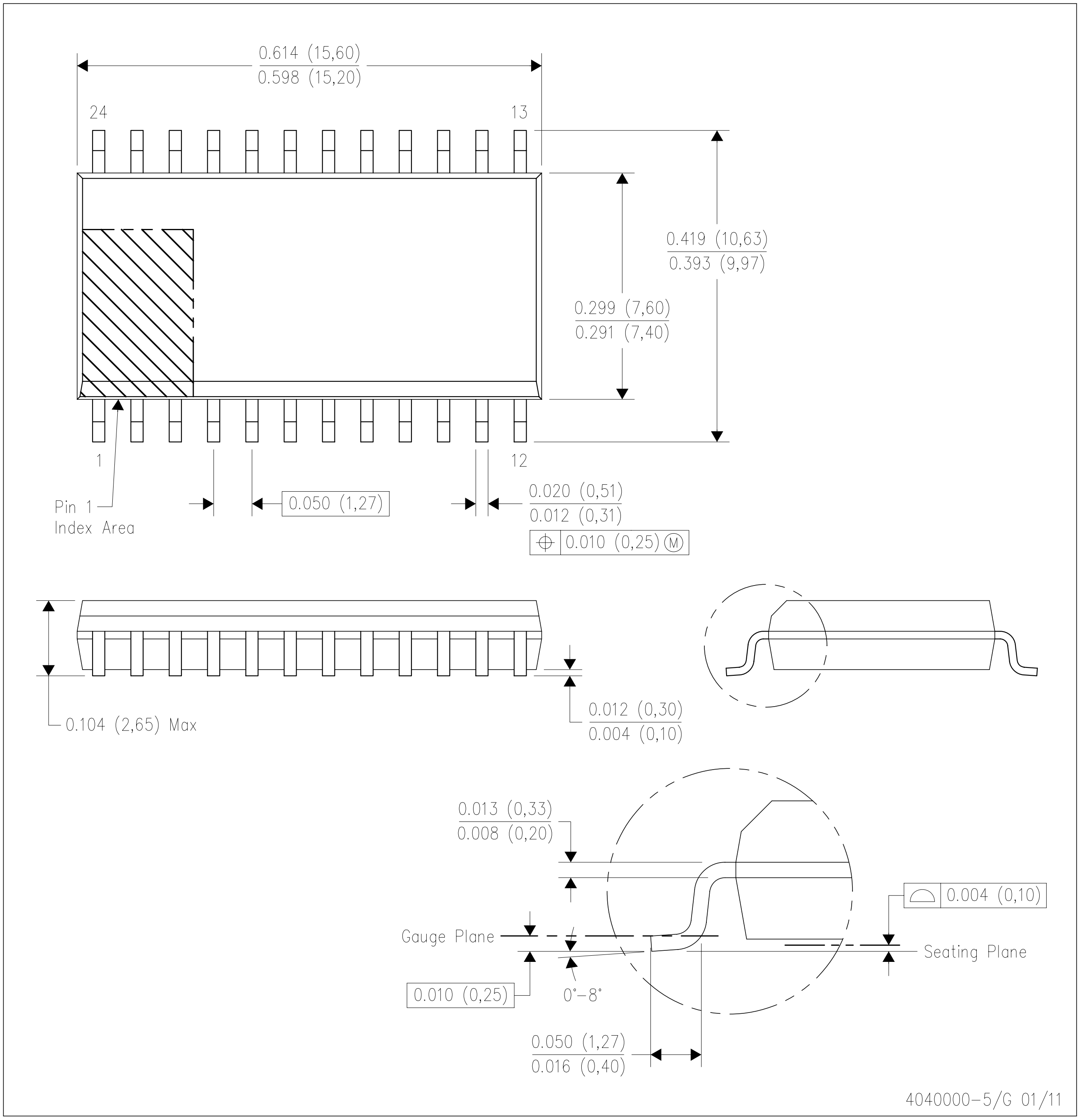
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6A598MDWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.