TLV237x-Q1 550-µA/Channel, 3-MHz Rail-to-Rail Input and Output Operational Amplifiers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Rail-to-Rail Input and Output
- Wide Bandwidth: 3 MHz
- High Slew Rate: 2.4 V/µs
- Supply Voltage Range: 2.7 V to 16 V
- Supply Current: 550 µA/Channel
- Input Noise Voltage: 39 nV/$\sqrt{\text{Hz}}$
- Input Bias Current: 1 pA
- Ultra-Small Packaging:
  - 5-Pin SOT-23 (TLV2371-Q1)

2 Applications

- Engine Control Units (ECU)
- Body Control Modules (BCM)
- Battery Management Systems
- HEV/EV Inverters
- Lane Departure Warning
- White Goods

3 Description

The TLV237x-Q1 devices are single-supply operational amplifiers providing rail-to-rail input and output capability. The TLV237x-Q1 takes the minimum operating supply voltage down to 2.7 V and up to 16 V over the extended automotive temperature range. Therefore, the wide voltage range can support both start-stop functionality and a connection directly to the typical 12-V battery. The rail-to-rail capabilities allow the device to maximize the output signal and avoid clipping.

The CMOS inputs enable high-impedance suitable for engine control units (ECU), body control modules (BCM), battery management systems (BMS), and HEV/EV inverters. This also allows the user to draw a lower offset voltage and maintain low power consumption to help meet overall system needs for quiescent current such as in infotainment or cluster, HEV/EV, and powertrain.

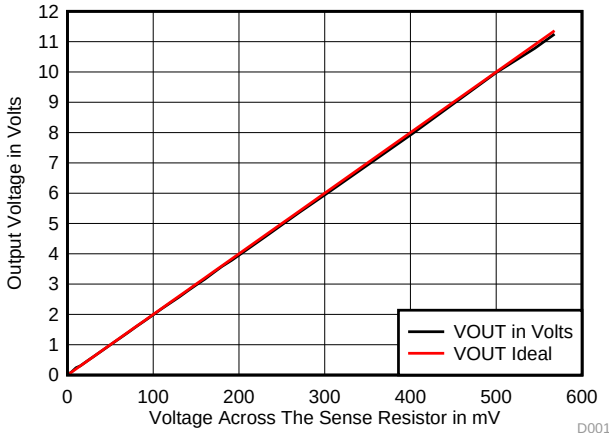
Additionally, the TLV237x-Q1 family supports a high common-mode rail to the supply voltage. This feature sets no gain limitations and can support the input at any level without the concern for any phase reversal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2371-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
TLV2372-Q1	SOIC (8)	4.90 mm × 3.91 mm
TLV2374-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Voltage vs Differential Input in High Current Sensing



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2008) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted 8-Pin MSOP (TLV2372) because the TLV2372-Q1 is not available in MSOP; also removed all references throughout the data sheet ... 1
- Changed list items in *Applications* ... 1
- Removed *Family Package* and *Available Options* tables, see POA at the end of the data sheet ... 1
- Renamed *Selection of Signal Amplifier Products* table to*Device Comparison Table* ... 3
- Changed SHUTDOWN for the TLV237x in the *Device Comparison Table* From: Yes To: — ... 3
- Changed I_{IB} (pA) for the TLV246x in the *Device Comparison Table* From: 1300 To: 1.3 ... 3
- Changed SHUTDOWN for the TLV237x in the *Device Comparison Table* From: Yes To: — ... 3
- Changed GND DESCRIPTION in *Pin Functions: TLV2371-Q1* From: Ground connection To: Negative (lowest) power supply ... 3
- Changed GND DESCRIPTION in *Pin Functions: TLV2372-Q1* From: Ground connection To: Negative (lowest) power supply ... 4
- Removed *Typical Pin 1 Indicators* image ... 4
- Changed GND DESCRIPTION in *Pin Functions: TLV2374-Q1* From: Ground connection To: Negative (lowest) power supply ... 4
- Deleted Lead temperature (260°C maximum) ... 5
- Added additional thermal values to all *Thermal Information* tables ... 6
- Changed $R_{\theta JA}$ values in *Thermal Information: TLV2371-Q1* From: 325.1 To: 228.5 (DBV) and From: 176 To: 138.4 (D) ... 6
- Changed $R_{\theta JA}$ value in *Thermal Information: TLV2372-Q1* From: 176 To: 138.4 (D) ... 6
- Deleted entire DGK (MSOP) column from *Thermal Information: TLV2372-Q1* ... 6
- Changed $R_{\theta JA}$ values in *Thermal Information: TLV2374-Q1* From: 122.3 To: 67 (D) and From: 173.6 To: 121 (PW) ... 6
- Deleted *Maximum Power Dissipation vs Free-Air Temperature* graph ... 23

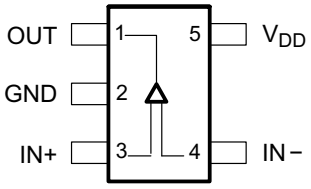
5 Device Comparison Table

Typical values measured at 5 V and 25°C

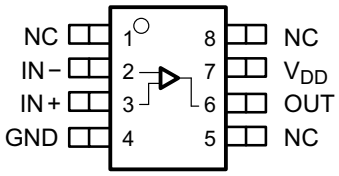
DEVICE	V_{DD} (V)	V_{IO} (µV)	Iq/Ch (µA)	I_{IB} (pA)	GBW (MHz)	SR (V/µs)	SHUTDOWN	RAIL-TO-RAIL	SINGLES, DUALS, QUADS
TLV237x-Q1	2.7 to 16	500	550	1	3	2.4	—	I/O	S, D, Q
TLC227x-Q1	4 to 16	300	1100	1	2.2	3.6	—	O	D, Q
TLV27x-Q1	2.7 to 16	500	550	1	3	2.4	—	O	S, D, Q
TLV246x-Q1	2.7 to 6	150	550	1.3	6.4	1.6	Yes	I/O	S, D, Q
TLV247x-Q1	2.7 to 6	250	600	2	2.8	1.5	—	I/O	S, D, Q
TLV244x-Q1	2.7 to 10	300	725	1	1.8	1.4	—	O	D, Q

6 Pin Configuration and Functions

TLV2371-Q1 DBV Package
5-Pin SOT-23
Top View



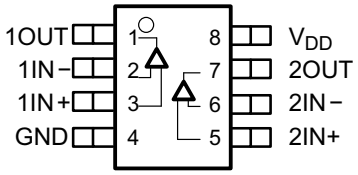
TLV2371-Q1 D Package
8-Pin SOIC
Top View



Pin Functions: TLV2371-Q1

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC		
GND	2	4	—	Negative (lowest) power supply
IN–	4	2	I	Negative (inverting) input
IN+	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V_{DD}	5	7	—	Positive power supply

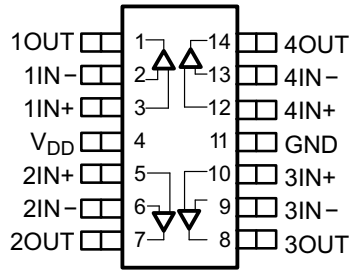
TLV2372-Q1 D Package
8-Pin SOIC
Top View



Pin Functions: TLV2372-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
1OUT	1	O	Output, channel 1
2IN–	6	I	Inverting input, channel 2
2IN+	5	I	Noninverting input, channel 2
2OUT	7	O	Output, channel 2
GND	4	—	Negative (lowest) power supply
V_{DD}	8	—	Positive power supply

TLV2374-Q1 D and PW Packages
14-Pin SOIC or TSSOP
Top View



Pin Functions: TLV2374-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
1OUT	1	O	Output, channel 1
2IN–	6	I	Inverting input, channel 2
2IN+	5	I	Noninverting input, channel 2
2OUT	7	O	Output, channel 2
3IN–	9	I	Inverting input, channel 3
3IN+	10	I	Noninverting input, channel 3
3OUT	8	O	Output, channel 3
4IN–	13	I	Inverting input, channel 4
4IN+	12	I	Noninverting input, channel 4
4OUT	14	O	Output, channel 4
GND	11	—	Negative (lowest) power supply
V_{DD}	4	—	Positive power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}		16.5	V
Differential input voltage, V_{ID}		$\pm V_{DD}$	
Input voltage, V_I	–0.2	V_{DD} + 0.2	V
Input current, I_I		±10	mA
Output current, I_O		±100	mA
Maximum junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
TLV2371-Q1 in DBV package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 3, 4, and 5)	±750	
TLV2371-Q1 in D package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	
TLV2372-Q1 in D package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	
TLV2374-Q1 in D and PW packages					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 7, 8, and 14)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	Single supply	2.7	16	V
		Split supply	±1.35	±8	
V_{ICR}	Common-mode input voltage		0	V_{DD}	V
$V_{(ON)}$	Turnon voltage level (relative to GND pin voltage)			2	V
$V_{(OFF)}$	Turnoff voltage level (relative to GND pin voltage)		0.8		V
T_A	Operating free-air temperature (Q-suffix)		–40	125	°C

7.4 Thermal Information: TLV2371-Q1

THERMAL METRIC[1]		TLV2371-Q1		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	138.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	89.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	78.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	29.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	78.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: TLV2372-Q1

THERMAL METRIC[1]		TLV2372-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: TLV2374-Q1

THERMAL METRIC[1]		TLV2374-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.1	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω	T_A = 25°C		2	4.5	mV
			T_A = –40°C to 125°C			6	
α_{VIO}	Offset voltage drift	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω, T_A = 25°C			2		µV/°C

Electrical Characteristics (continued)

at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_{DD} = 2.7 V	V_{IC} = 0 to V_{DD}, R_S = 50 Ω	T_A = 25°C	50	68		dB
				T_A = –40°C to 125°C	49			
			V_{IC} = 0 to V_{DD} – 1.35 V, R_S = 50 Ω	T_A = 25°C	53	70		
				T_A = –40°C to 125°C	54			
		V_{DD} = 5 V	V_{IC} = 0 to V_{DD}, R_S = 50 Ω	T_A = 25°C	55	72		
				T_A = –40°C to 125°C	54			
			V_{IC} = 0 to V_{DD} – 1.35 V, R_S = 50 Ω	T_A = 25°C	58	80		
				T_A = –40°C to 125°C	57			
		V_{DD} = 15 V	V_{IC} = 0 to V_{DD}, R_S = 50 Ω	T_A = 25°C	64	82		
				T_A = –40°C to 125°C	63			
			V_{IC} = 0 to V_{DD} – 1.35 V, R_S = 50 Ω	T_A = 25°C	67	84		
				T_A = –40°C to 125°C	66			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = V_{DD}/2, R_S = 10 Ω	V_{DD} = 2.7 V	T_A = 25°C	95	106		dB
				T_A = –40°C to 125°C	76			
			V_{DD} = 5 V	T_A = 25°C	80	110		
				T_A = –40°C to 125°C	82			
			V_{DD} = 15 V	T_A = 25°C	77	83		
				T_A = –40°C to 125°C	79			
INPUT								
I_{IO}	Input offset current	V_{DD} = 15 V, V_{IC} = V_{DD}/2, V_O = V_{DD}/2		T_A = 25°C		1	60	pA
				T_A = –40°C to 125°C			500	
I_{IB}	Input bias current	V_{DD} = 15 V, V_{IC} = V_{DD}/2, V_O = V_{DD}/2		T_A = 25°C		1	60	pA
				T_A = –40°C to 125°C			500	
$r_{i(d)}$	Differential input resistance	T_A = 25°C				1000		GΩ
C_{IC}	Common-mode input capacitance	f = 21 kHz, T_A = 25°C				8		pF
OUTPUT								
V_{OH}	High-level output voltage	V_{IC} = V_{DD}/2, I_{OH} = –1 mA, V_{ID} = 1 V	V_{DD} = 2.7 V	T_A = 25°C	2.55	2.58		V
				T_A = –40°C to 125°C	2.48			
			V_{DD} = 5 V	T_A = 25°C	4.9	4.93		
				T_A = –40°C to 125°C	4.85			
			V_{DD} = 15 V	T_A = 25°C	14.92	14.96		
				T_A = –40°C to 125°C	14.9			
		V_{IC} = V_{DD}/2, I_{OH} = –5 mA, V_{ID} = 1 V	V_{DD} = 2.7 V	T_A = 25°C	1.88	2		
				T_A = –40°C to 125°C	1.42			
			V_{DD} = 5 V	T_A = 25°C	4.58	4.68		
				T_A = –40°C to 125°C	4.44			
			V_{DD} = 15 V	T_A = 25°C	14.7	14.8		
				T_A = –40°C to 125°C	14.6			

Electrical Characteristics (continued)

at specified free-air temperature, V_{DD} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{IC} = V_{DD}/2, I_{OH} = 1 mA, V_{ID} = 1 V	V_{DD} = 2.7 V	T_A = 25°C		0.1	0.15	V
				T_A = –40°C to 125°C			0.22	
			V_{DD} = 5 V	T_A = 25°C		0.05	0.1	
				T_A = –40°C to 125°C			0.15	
			V_{DD} = 15 V	T_A = 25°C		0.05	0.08	
				T_A = –40°C to 125°C			0.1	
		V_{IC} = V_{DD}/2, I_{OH} = 5 mA, V_{ID} = 1 V	V_{DD} = 2.7 V	T_A = 25°C		0.52	0.7	
				T_A = –40°C to 125°C			1.15	
			V_{DD} = 5 V	T_A = 25°C		0.28	0.4	
				T_A = –40°C to 125°C			0.54	
			V_{DD} = 15 V	T_A = 25°C		0.19	0.3	
				T_A = –40°C to 125°C			0.35	
POWER SUPPLY								
I_{DD}	Supply current (per channel)	V_O = V_{DD}/2	V_{DD} = 2.7 V	T_A = 25°C		470	560	µA
			V_{DD} = 5 V	T_A = 25°C		550	660	
			V_{DD} = 15 V	T_A = 25°C		750	900	
				T_A = –40°C to 125°C			1200	
PSRR	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 15 V, V_{IC} = V_{DD}/2, no load		T_A = 25°C	70	80		dB
				T_A = –40°C to 125°C	65			
DYNAMIC PERFORMANCE								
UGBW	Unity gain bandwidth	R_L = 2 kΩ, C_L = 10 pF		V_{DD} = 2.7 V, T_A = 25°C		2.4		MHz
				V_{DD} = 5 V to 15 V, T_A = 25°C		3		
SR	Slew rate at unity gain	$V_{O(PP)}$ = V_{DD}/2, R_L = 10 kΩ, C_L = 50 pF	V_{DD} = 2.7 V	T_A = 25°C	1.4	2		V/µs
				T_A = –40°C to 125°C	1			
			V_{DD} = 5 V	T_A = 25°C	1.4	2.4		
				T_A = –40°C to 125°C	1.2			
			V_{DD} = 15 V	T_A = 25°C	1.9	2.1		
				T_A = –40°C to 125°C	1.4			
φ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF, T_A = 25°C				65°		
	Gain margin	R_L = 2 kΩ, C_L = 10 pF, T_A = 25°C				18		dB
t_s	Settling time	V_{DD} = 2.7 V, $V_{(STEP)PP}$ = 1 V, A_V = –1, R_L = 2 kΩ, C_L = 10 pF, 0.1% at 25°C				2.9		µs
		V_{DD} = 5 V or 15 V, $V_{(STEP)PP}$ = 1 V, A_V = –1, R_L = 2 kΩ, C_L = 47 pF, 0.1% at 25°C				2		
NOISE/DISTORTION PERFORMANCE								
THD+N	Total harmonic distortion plus noise	V_{DD} = 2.7 V, $V_{O(PP)}$ = V_{DD}/2 V, R_L = 2 kΩ, f = 10 kHz, T_A = 25°C		A_V = 1		0.02%		
				A_V = 10		0.05%		
				A_V = 100		0.18%		
		V_{DD} = 5 V or 15 V, $V_{O(PP)}$ = V_{DD}/2 V, R_L = 2 kΩ, f = 10 kHz, T_A = 25°C		A_V = 1		0.02%		
				A_V = 10		0.09%		
				A_V = 100		0.5%		
V_n	Equivalent input noise voltage	f = 1 kHz, T_A = 25°C				39		$nV/\sqrt{Hz}$
		f = 10 kHz, T_A = 25°C				35		
I_n	Equivalent input noise current	f = 1 kHz, T_A = 25°C				0.6		$fA/\sqrt{Hz}$

7.8 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	Figure 1, Figure 2, Figure 3
CMRR	Common-mode rejection ratio	vs Frequency	Figure 4
	Input bias and offset current	vs Free-air temperature	Figure 5
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 6, Figure 8, Figure 10
V_{OH}	High-level output voltage	vs High-level output current	Figure 7, Figure 9, Figure 11
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	Figure 12
I_{DD}	Supply current	vs Supply voltage	Figure 13
PSRR	Power supply rejection ratio	vs Frequency	Figure 14
A_{VD}	Differential voltage gain & phase	vs Frequency	Figure 15
	Gain-bandwidth product	vs Free-air temperature	Figure 16
SR	Slew rate	vs Supply voltage	Figure 17
		vs Free-air temperature	Figure 18
φ_m	Phase margin	vs Capacitive load	Figure 19
V_n	Equivalent input noise voltage	vs Frequency	Figure 20
	Voltage-follower large-signal pulse response		Figure 21, Figure 22
	Voltage-follower small-signal pulse response		Figure 23
	Inverting large-signal response		Figure 24, Figure 25
	Inverting small-signal response		Figure 26
	Crosstalk	vs Frequency	Figure 27

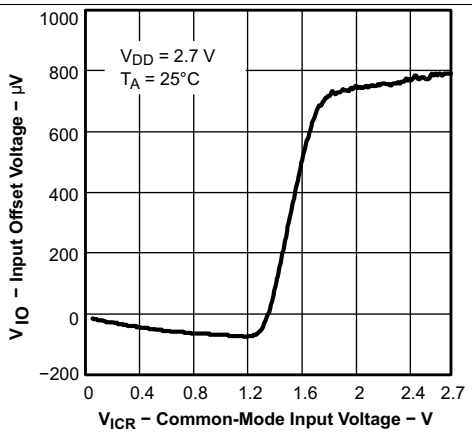


Figure 1. Input Offset Voltage vs Common-Mode Input Voltage

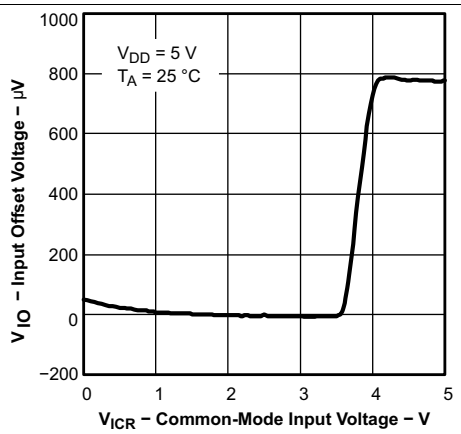


Figure 2. Input Offset Voltage vs Common-Mode Input Voltage

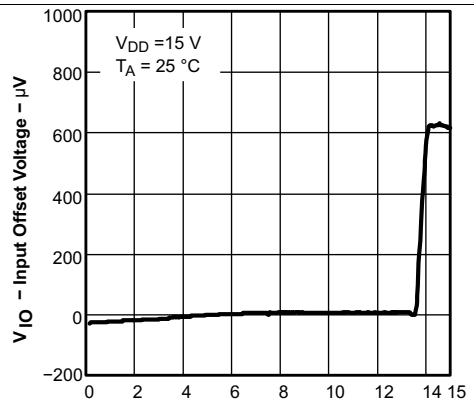


Figure 3. Input Offset Voltage vs Common-Mode Input Voltage

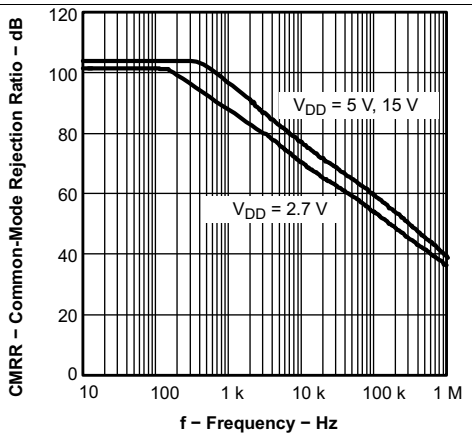


Figure 4. Common-Mode Rejection Ratio vs Frequency

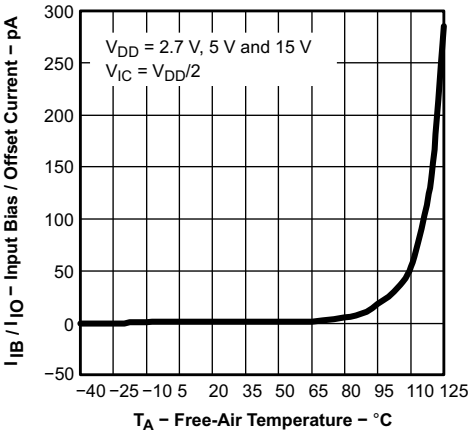


Figure 5. Input Bias and Offset Current vs Free-Air Temperature

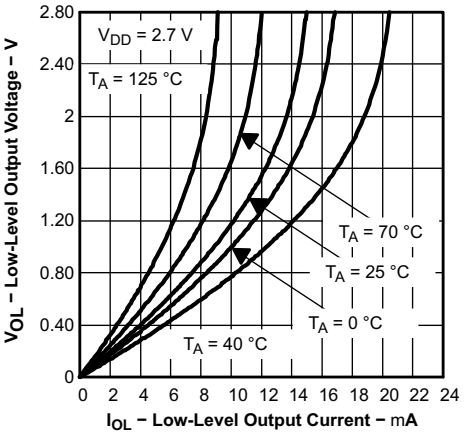


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

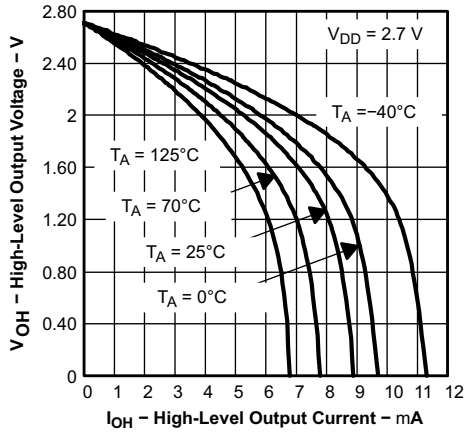


Figure 7. High-Level Output Voltage vs High-Level Output Current

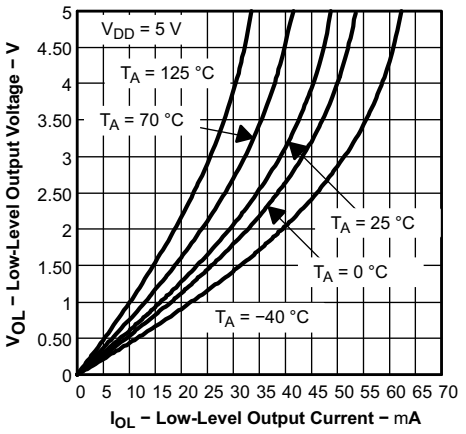


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

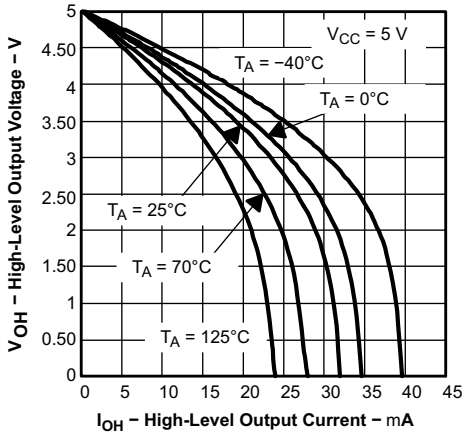


Figure 9. High-Level Output Voltage vs High-Level Output Current

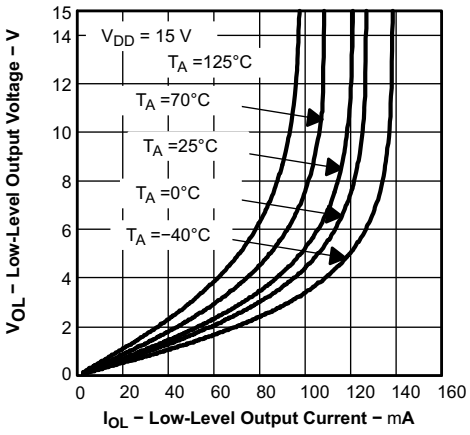


Figure 10. Low-Level Output Voltage vs Low-Level Output Current

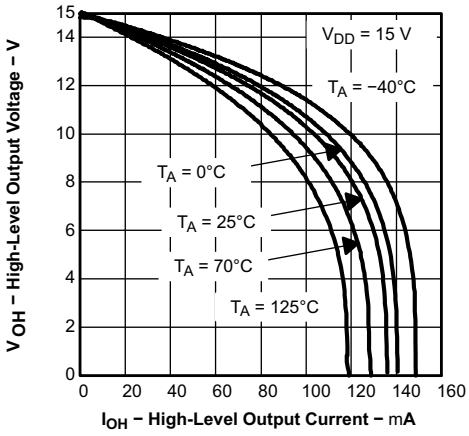


Figure 11. High-Level Output Voltage vs High-Level Output Current

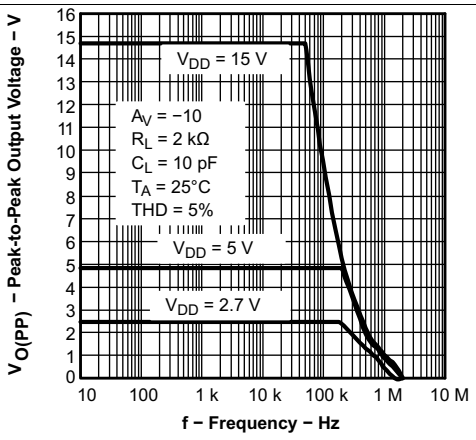


Figure 12. Peak-to-Peak Output Voltage vs Frequency

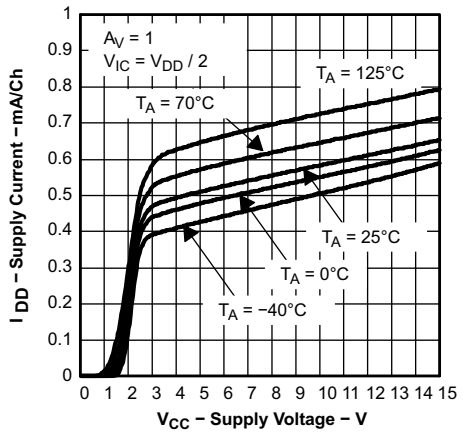


Figure 13. Supply Current vs Supply Voltage

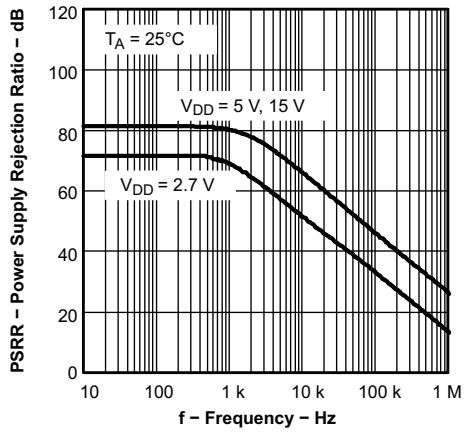


Figure 14. Power Supply Rejection Ratio vs Frequency

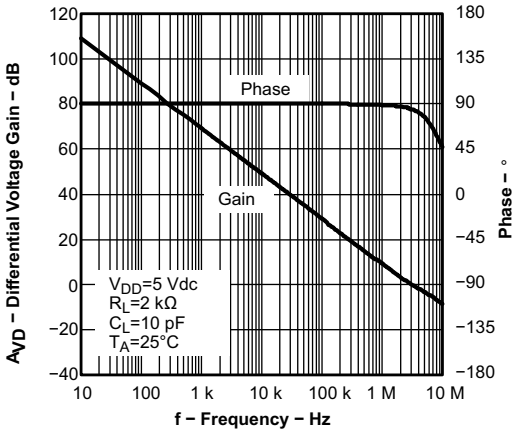


Figure 15. Differential Voltage Gain and Phase vs Frequency

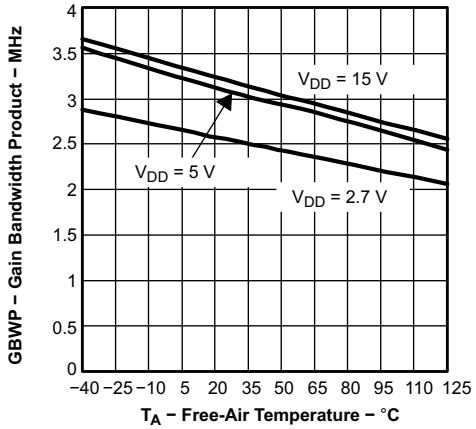


Figure 16. Gain Bandwidth Product vs Free-Air Temperature

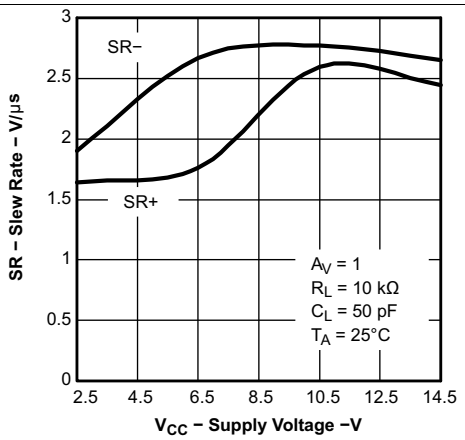


Figure 17. Slew Rate vs Supply Voltage

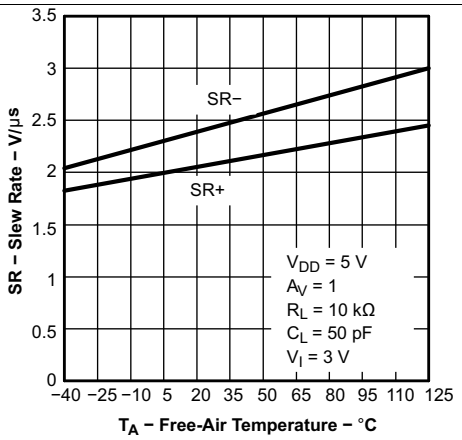


Figure 18. Slew Rate vs Free-Air Temperature

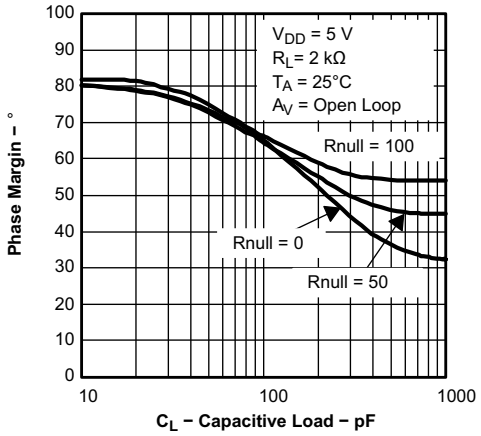


Figure 19. Phase Margin vs Capacitive Load

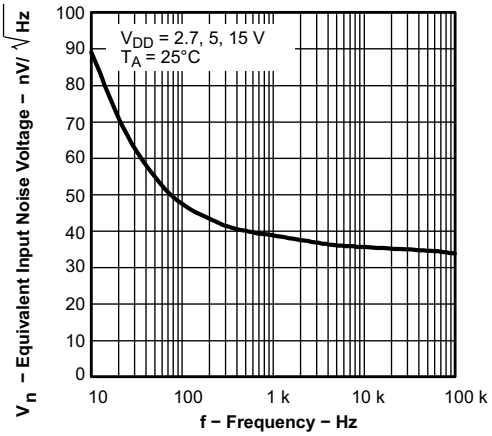


Figure 20. Equivalent Input Noise Voltage vs Frequency

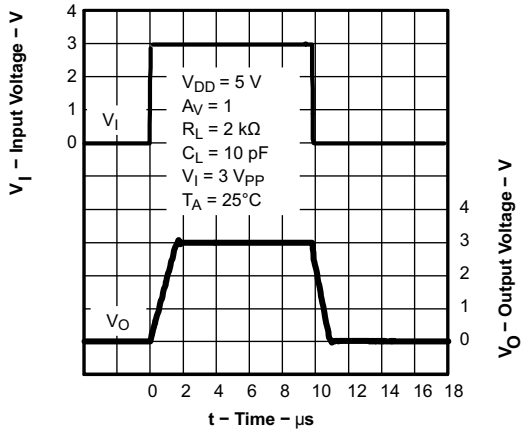


Figure 21. Voltage-Follower Large-Signal Pulse Response

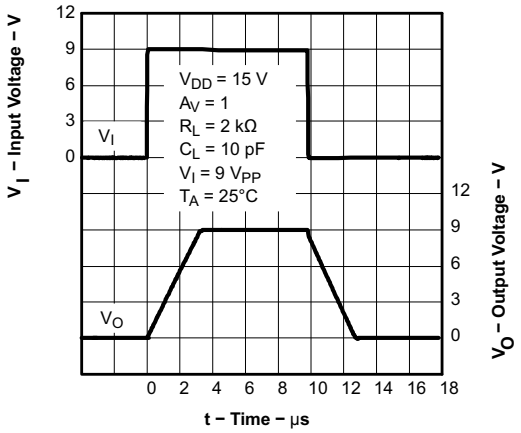


Figure 22. Voltage-Follower Large-Signal Pulse Response

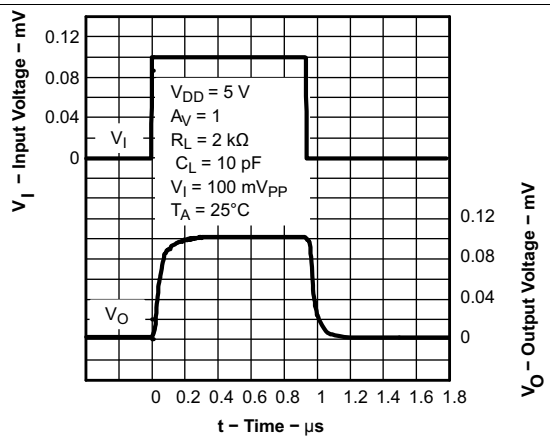


Figure 23. Voltage-Follower Small-Signal Pulse Response

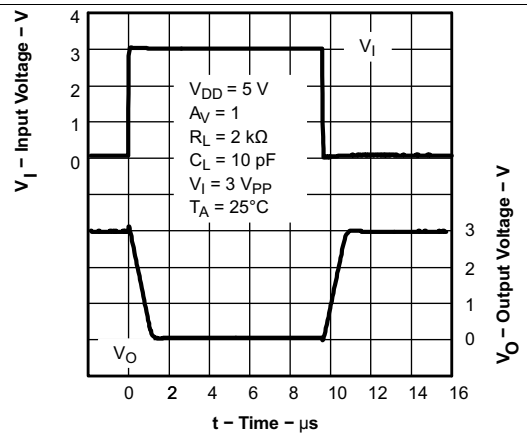


Figure 24. Inverting Large-Signal Response

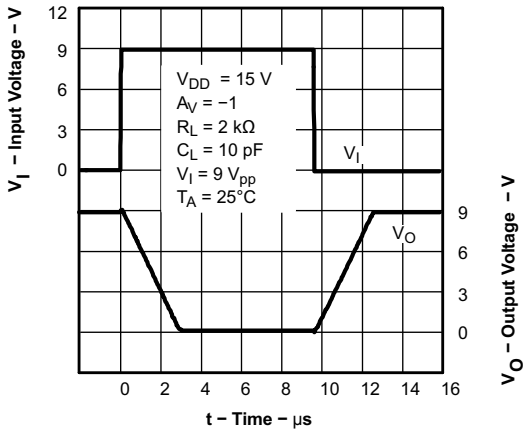


Figure 25. Inverting Large-Signal Response

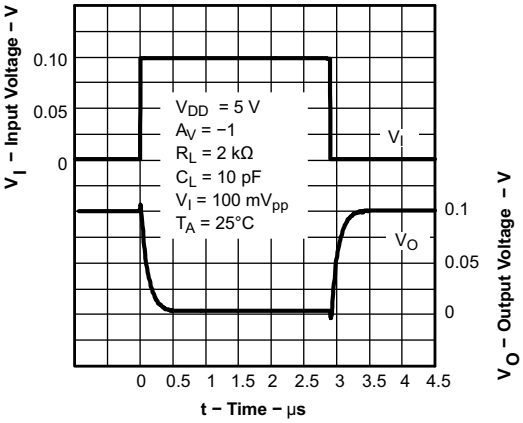


Figure 26. Inverting Small-Signal Response

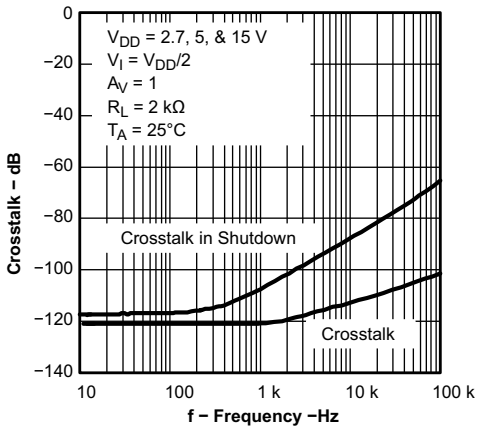


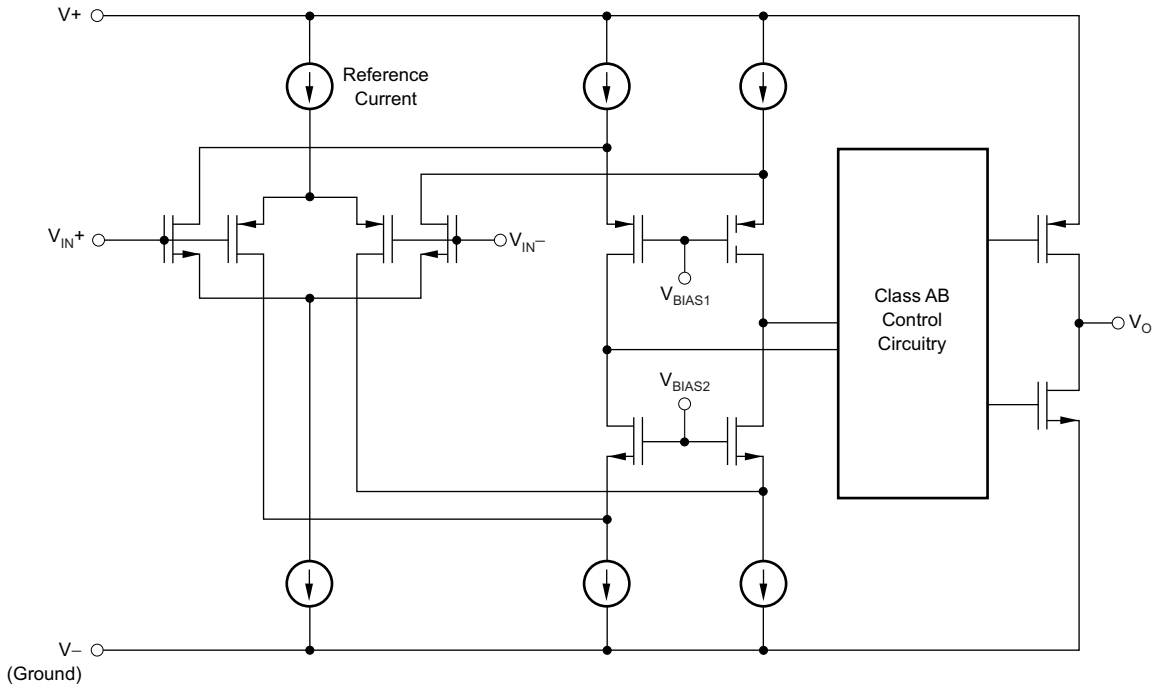
Figure 27. Crosstalk vs Frequency

8 Detailed Description

8.1 Overview

The TLV237x-Q1 single-supply operational amplifiers provide rail-to-rail input and output capability with 3-MHz bandwidth. Consuming only 550 µA, the TLV237x-Q1 is the perfect choice for portable and battery-operated applications. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from a variety of rechargeable cells (±8-V supplies down to ±1.35 V). The rail-to-rail inputs with high input impedance make the TLV237x-Q1 ideal for sensor signal-conditioning applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input Operation

The TLV237x-Q1 input stage consists of two differential transistor pairs, NMOS and PMOS, that operate together to achieve rail-to-rail input operation. The transition point between these two pairs can be seen in Figure 1 through Figure 3 for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active. This is the region in Figure 1 through Figure 3 where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

Feature Description (continued)

8.3.2 Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series (R_{NULL}) with the output of the amplifier, as shown in Figure 28. A minimum value of 20 Ω works well for most applications.

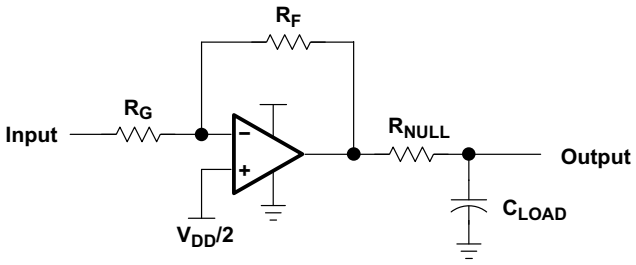
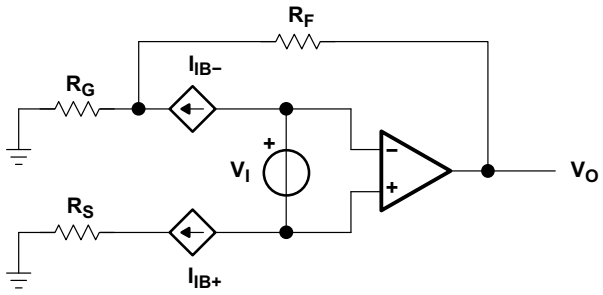


Figure 28. Driving a Capacitive Load

8.3.3 Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset volt age (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 29 can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 29. Output Offset Voltage Model

8.3.4 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 30).

Feature Description (continued)

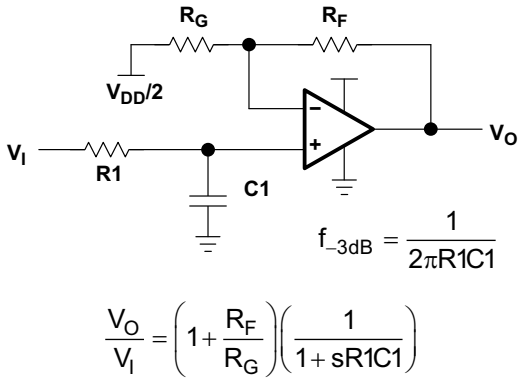


Figure 30. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. The Sallen-Key filter can be used for this task (see Figure 31). For best results, the amplifier must have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

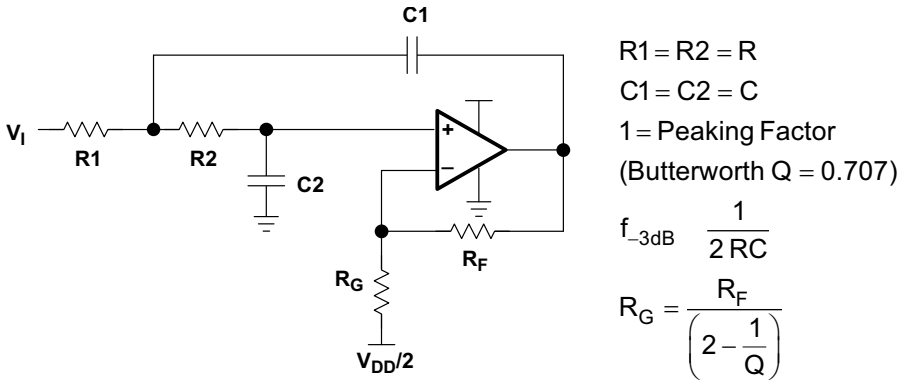


Figure 31. 2-Pole Low-Pass Sallen-Key Filter

8.4 Device Functional Modes

The TLV2371-Q1, TLV2372-Q1, and TLV2374-Q1 have a single functional mode. These devices are operational as long as the power supply voltage is between 2.7 V (±1.35 V) and 16 V (±8 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing for low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors can react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

9.2 Typical Applications

9.2.1 High-Side Current Monitor

The TLV237x-Q1 is rail-to-rail input and output capability and up to 16-V supply voltage. That makes the device suitable in body control model applications and more specific high-side current sensing. The input common mode is at the supply voltage so there is no limitation in differential gain.

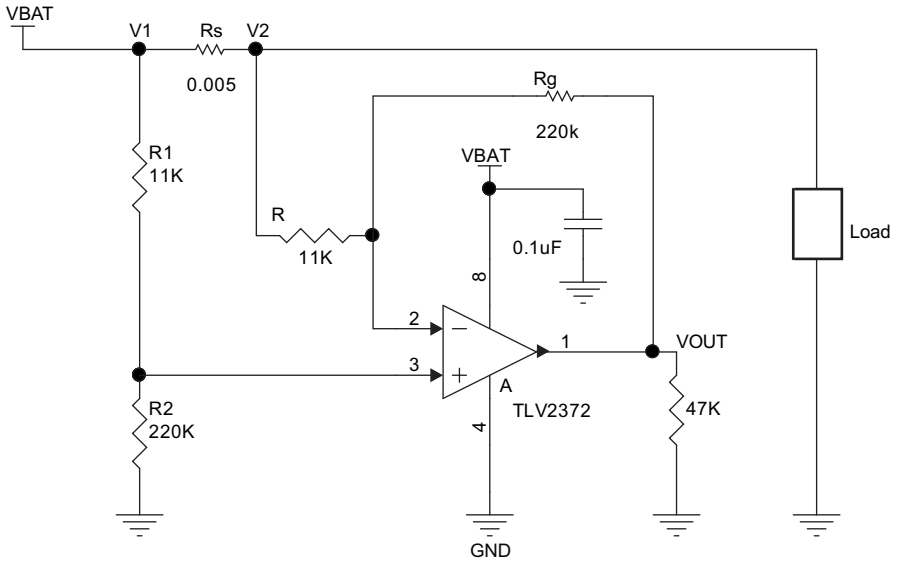


Figure 32. Application Circuit

9.2.1.1 Design Requirements

For this design example, use these parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER		VALUE
V_{BAT}	Battery voltage	12 V
R_{SENSE}		0.05 Ω
I_{LOAD}	Load current	0 A to 10 A
	Operational amplifier	Set in differential configuration with gain = 20

9.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

9.2.1.2.1 Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times\frac{V1+V2}{2}+\frac{1+\frac{1}{2}\left(\frac{R}{R_g}+\frac{R_1}{R_2}\right)}{1+\frac{R_1}{R_2}}(V1-V2)\right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times\frac{V1+V2}{2}+\frac{1+\frac{1}{2}\left(\frac{R}{R_g}+\frac{R_1}{R_2}\right)}{1+\frac{R_1}{R_2}}\times R_S\times I_{load}\right) \quad (2)$$

In an ideal case, R1 = R, R2 = R_g, and V_{OUT} can then be calculated using Equation 3.

$$V_{OUT} = \frac{R_g}{R}\times R_S\times I_{load} \quad (3)$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$ (4)

$R_2 = R \pm \Delta R_2$ (5)

$R = R \pm \Delta R$ (6)

$R_g = R_g \pm \Delta R$ (7)

$$Tol = \frac{\Delta R}{R} \quad (8)$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by Equation 9.

$$V = \pm\left(4\ Tol\right)\frac{Rg}{R+Rg}\ x\,Vbat + \left(1 \pm 2\ Tol\left(1+\frac{2R}{R+Rg}\right)\right)\frac{Rg}{R}\times Rs\times I_{load}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1% (9)

If the resistors are perfectly matched, then Tol = 0 and Vout is calculated using Equation 10.

$$Vout = \frac{Rg}{R}\times Rs\times I_{load} \quad (10)$$

The highest error is from the common mode in Equation 11.

$$\left(4\ Tol\right)\frac{Rg}{R+Rg}\times Vbat \quad (11)$$

Gain of 20, Rg/R = 20, and Tol = 1% in Equation 12.

Common mode error = ((4 × 0.01) / 1.05) × 12 V = 0.457 V (12)

When the gain of 20 and Tol = 0.1%, the common-mode error = 45.7 mV.

The resistors were chosen from 1% batches.

- R1 and R are 11 kΩ
- R2 and Rg are 220 kΩ

Ideal Gain = 220 / 11 = 20

The measured value of the resistors:

- R1 = 10.97 kΩ
- R = 10.96 kΩ
- R2 = 220.23 kΩ
- Rg = 220.15 kΩ

9.2.1.3 Application Curve

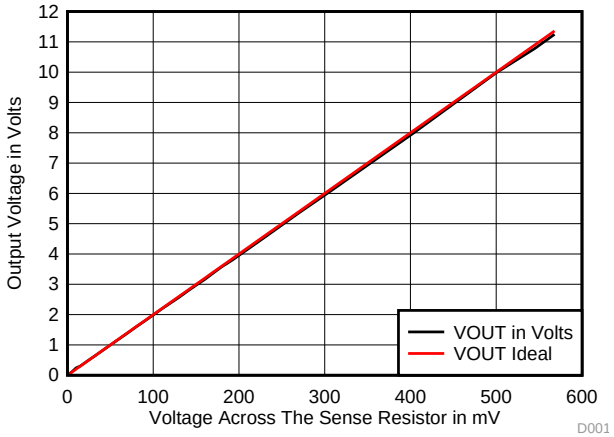


Figure 33. Output Voltage vs Differential Input in High Current Sensing

9.2.2 Inverting Amplifier

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 34. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

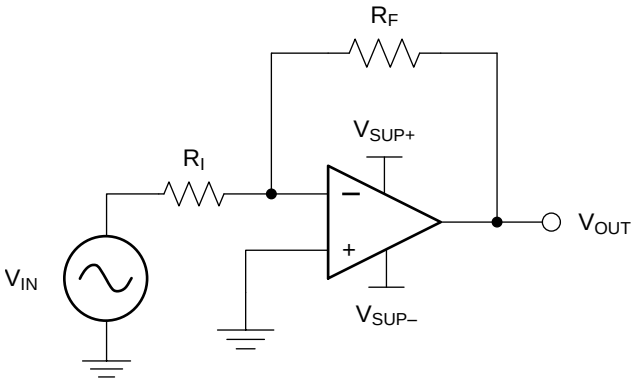


Figure 34. Amplifier Schematic

9.2.3 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

9.2.4 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 13 and Equation 14.

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{13}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{14}$$

When the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kΩ range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that large resistors (hundreds of kΩ) draw the smallest current but generate the highest noise. Small resistors (hundreds of Ω) generate low noise but draw high current. This example uses 10 kΩ for R_I, meaning 36 kΩ is used for R_F. These values are determined by Equation 15.

$$A_V = -\frac{R_F}{R_I} \tag{15}$$

9.2.5 Application Curve

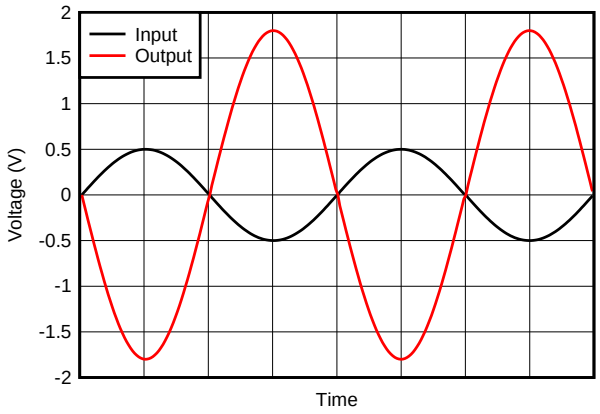


Figure 35. Inverting Amplifier Input and Output

10 Power Supply Recommendations

The TLV237x-Q1 family is specified for operation from 2.7 V to 15 V (±1.35 V to ±7.5 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 16 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement (see *Layout*).

11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLV237x-Q1, follow proper printed-circuit board design techniques. The following is a general set of guidelines:

- Ground planes: TI highly recommends a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling: Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum capacitor among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor must always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor must be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer must strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets: Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs or compact part placements: Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inverting input of the amplifier. Its length must be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components: Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, TI recommends that the lead lengths be kept as short as possible.

11.2 Layout Examples

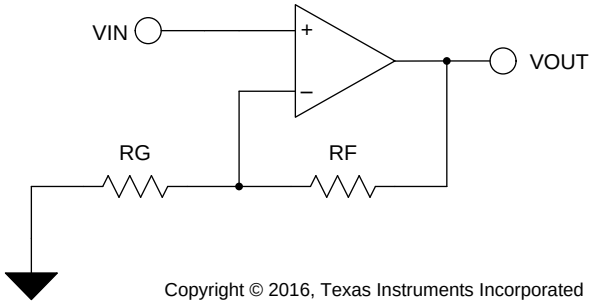


Figure 36. Schematic Representation

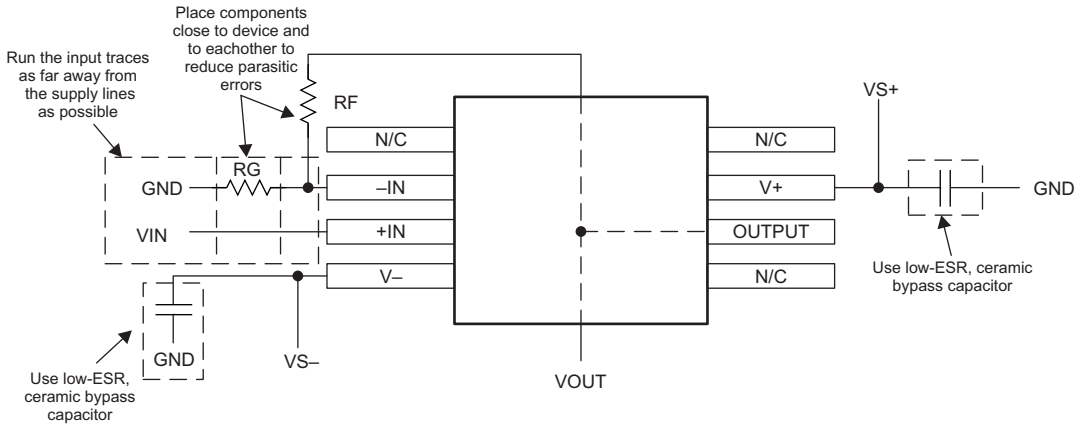


Figure 37. Operational Amplifier Board Layout for Noninverting Configuration

11.3 Power Dissipation Considerations

For a given $R_{\theta JA}$, the maximum power dissipation is calculated by Equation 16.

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (16)$$

where

- P_D = Maximum power dissipation of TLV237x-Q1 IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
  - $R_{\theta JC}$ = Thermal coefficient from junction-to-case
  - $R_{\theta CA}$ = Thermal coefficient from case-to-ambient air (°C/W)

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV2371-Q1	Click here	Click here	Click here	Click here	Click here
TLV2372-Q1	Click here	Click here	Click here	Click here	Click here
TLV2374-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2371QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(371Q, PDVQ)
TLV2371QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(371Q, PDVQ)
TLV2371QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(371Q, PDVQ)
TLV2371QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371Q1
TLV2371QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371Q1
TLV2371QDRG4Q1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371Q1
TLV2372QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2372QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2372QDRG4Q1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2372QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2372QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2372QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372Q1
TLV2374QDRG4Q1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QDRG4Q1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QDRG4Q1.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QDRQ1.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRG4Q1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1
TLV2374QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV2371-Q1, TLV2372-Q1, TLV2374-Q1 :

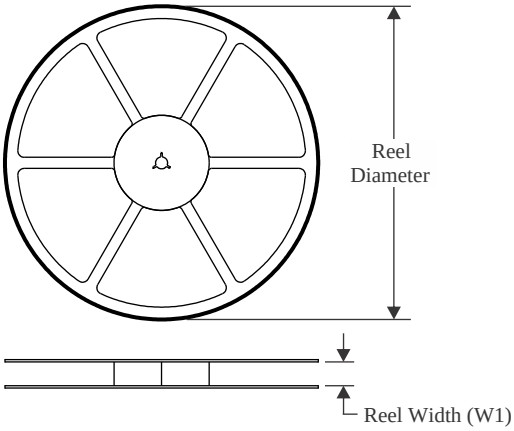
- Catalog : TLV2371, TLV2372, TLV2374
- Enhanced Product : TLV2374-EP

NOTE: Qualified Version Definitions:

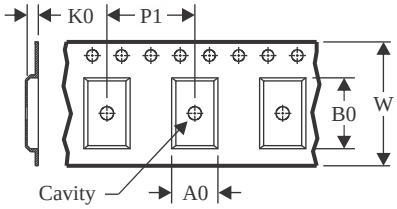
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

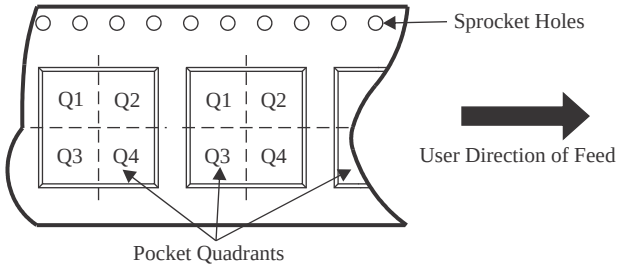


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

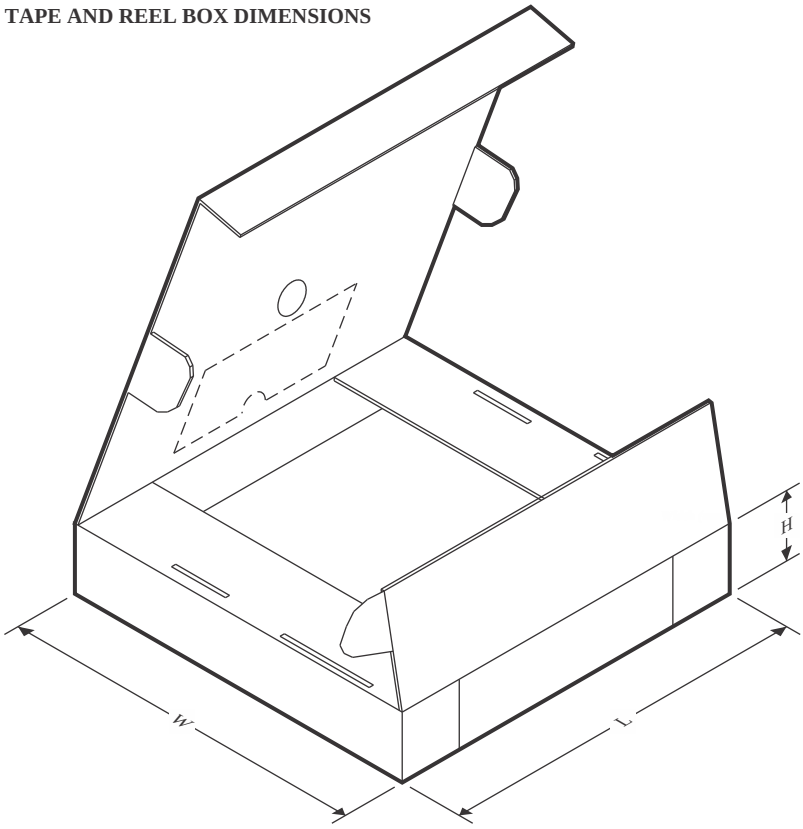
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2371QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2374QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2374QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

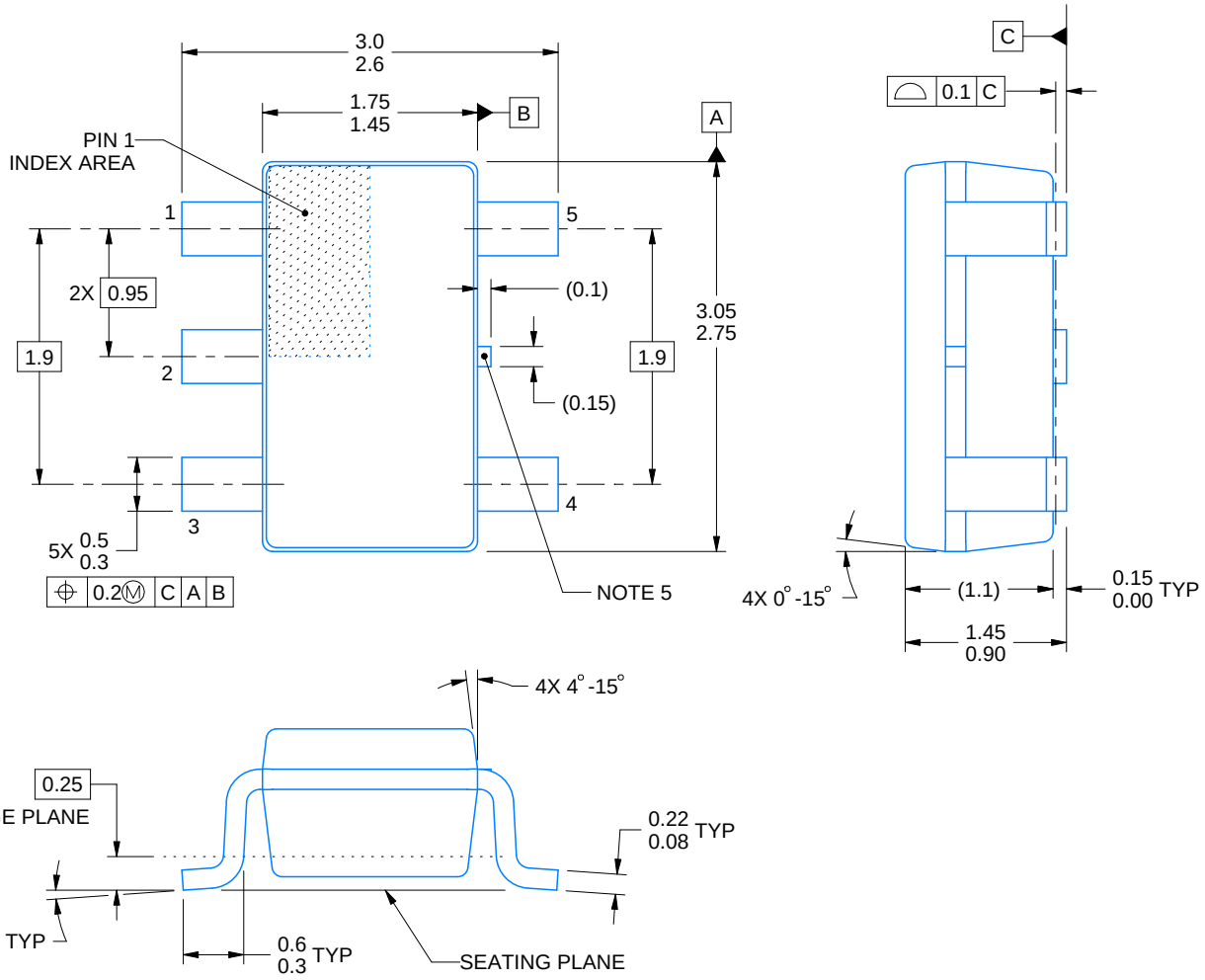
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2371QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2374QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2374QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

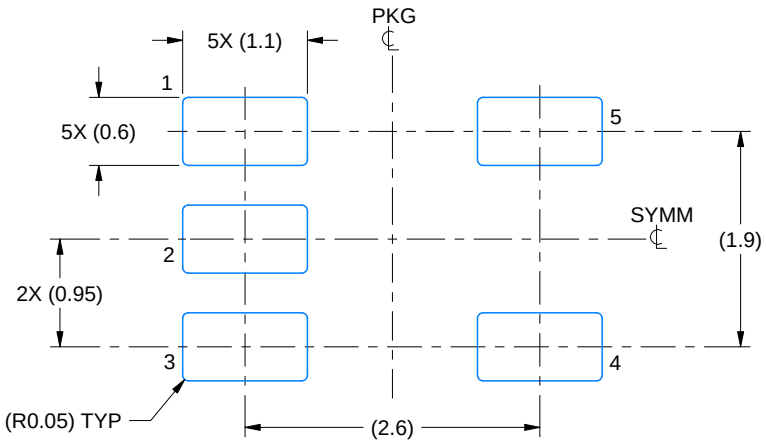
SMALL OUTLINE TRANSISTOR



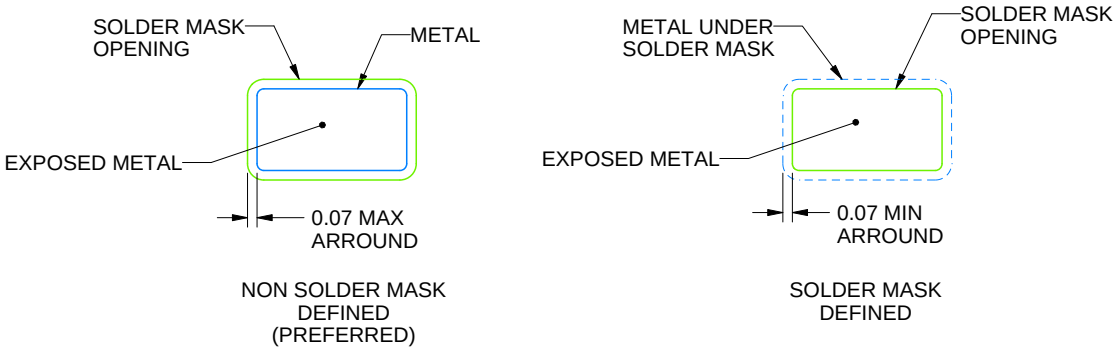
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

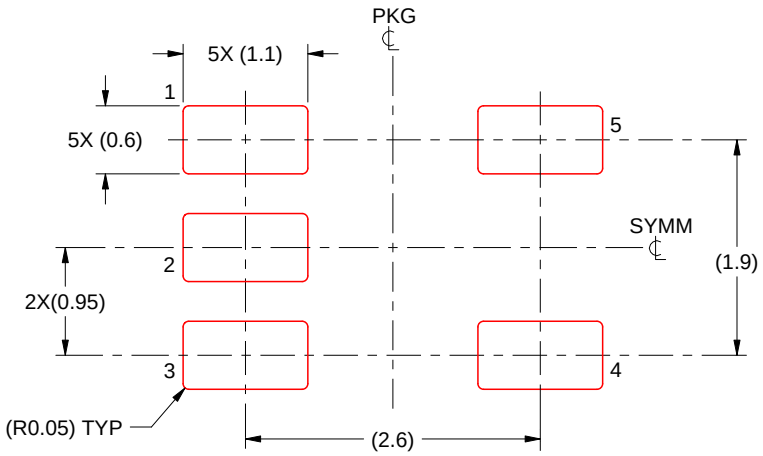


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

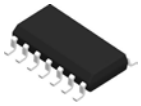


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

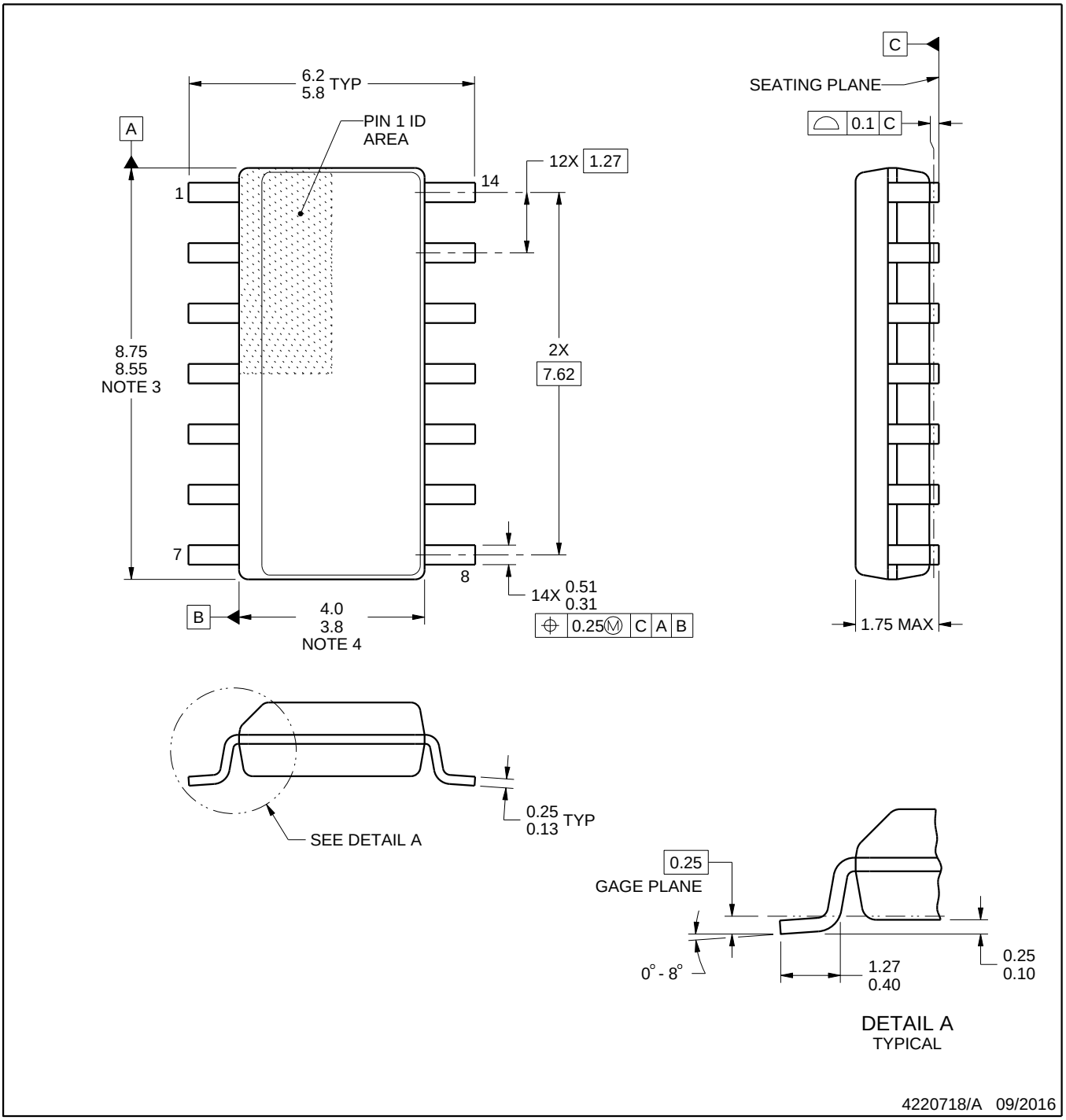


PACKAGE OUTLINE

D0014A

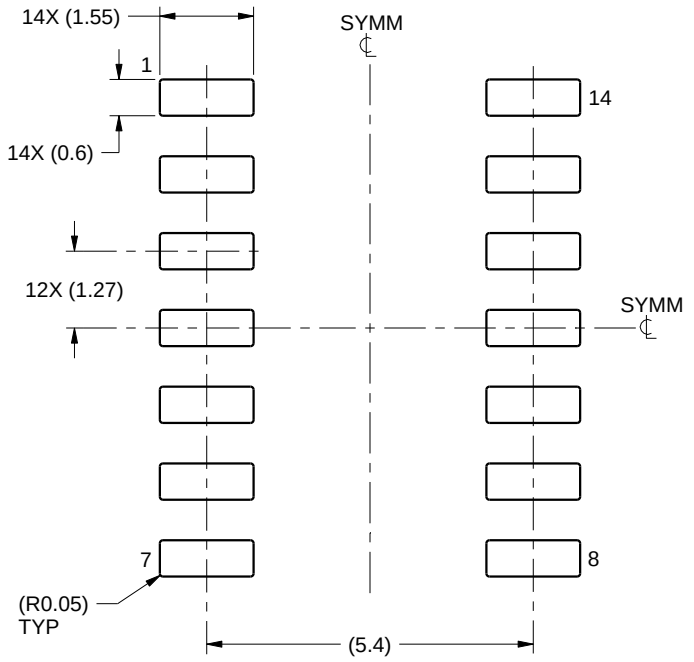
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

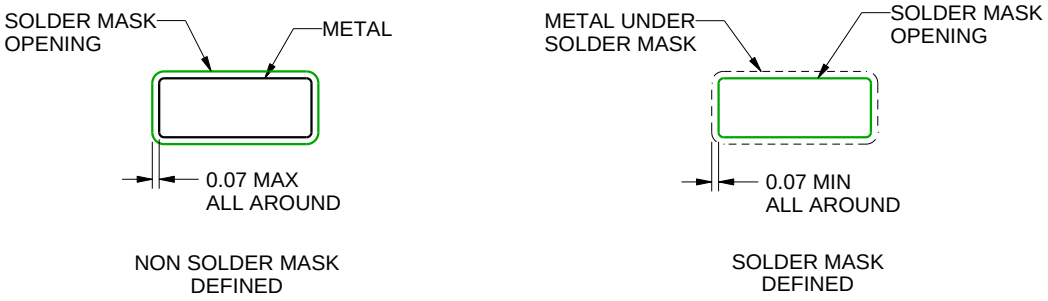


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

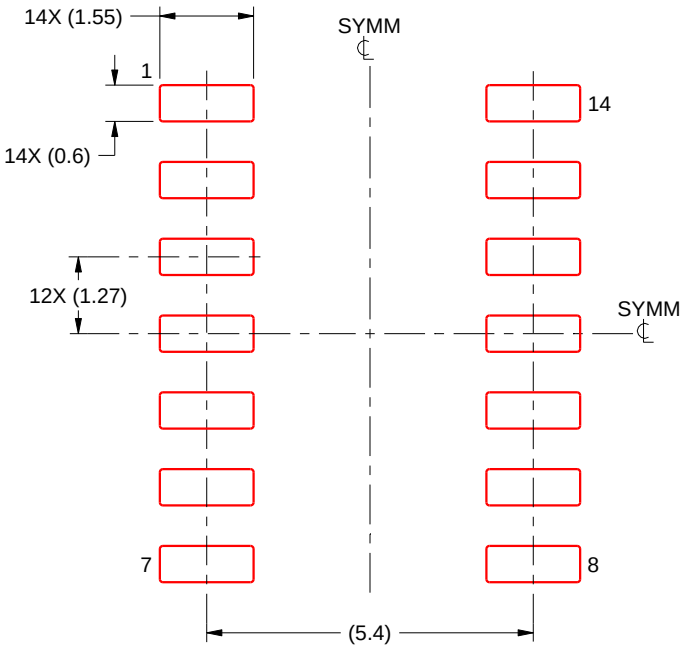
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

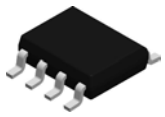


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

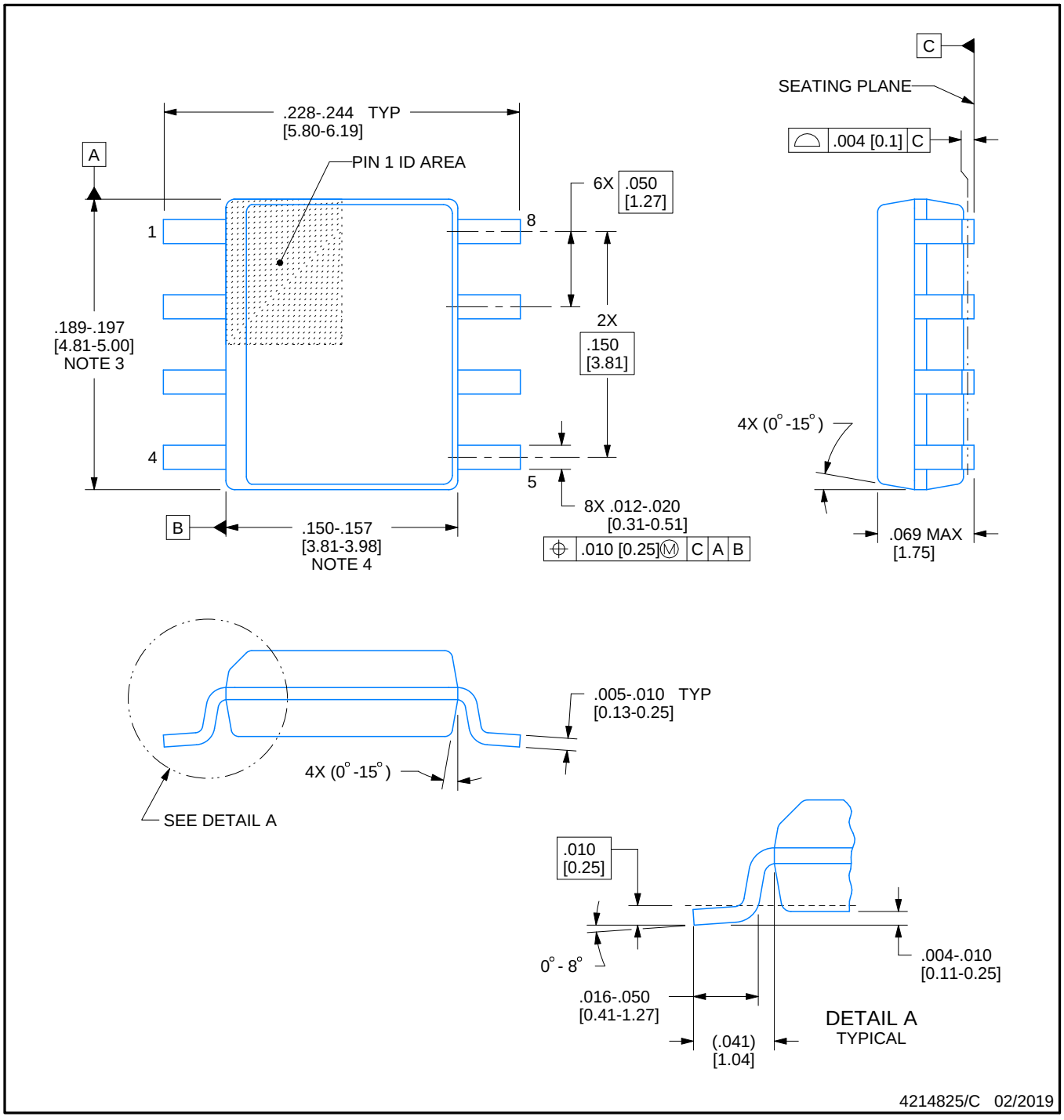


PACKAGE OUTLINE

D0008A

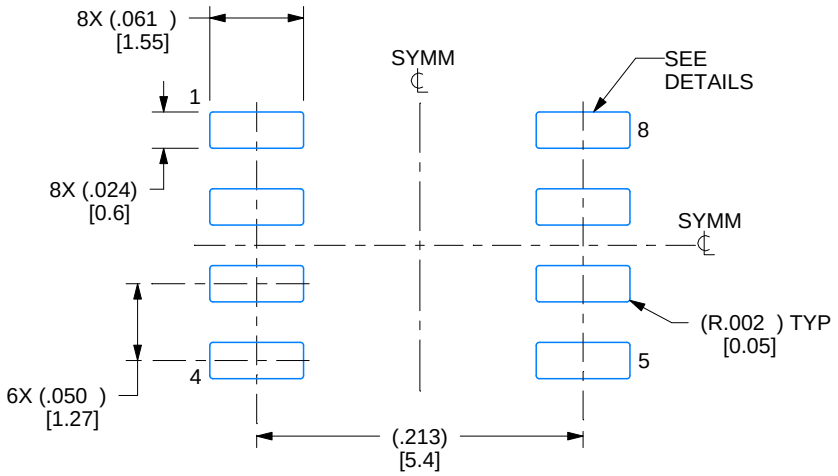
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

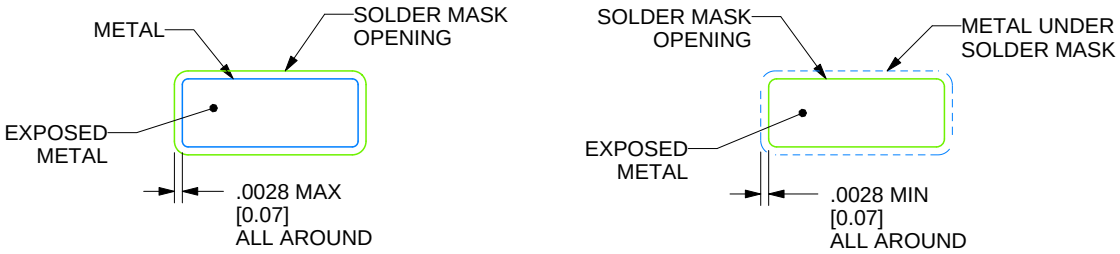


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

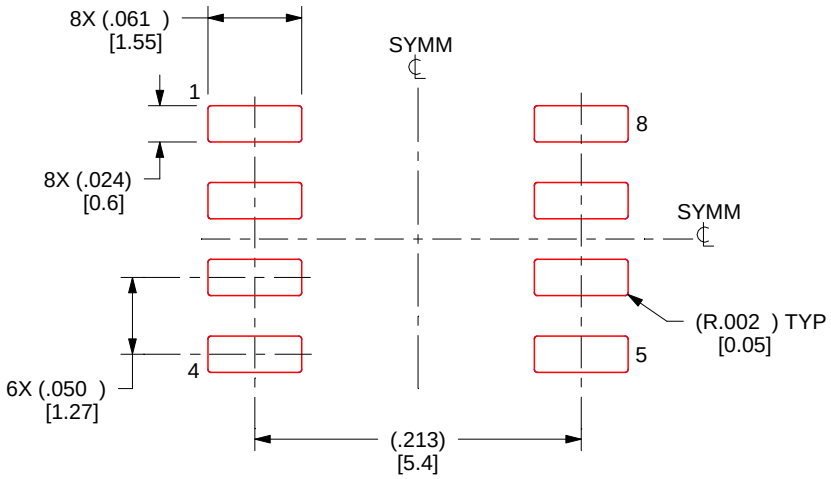
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

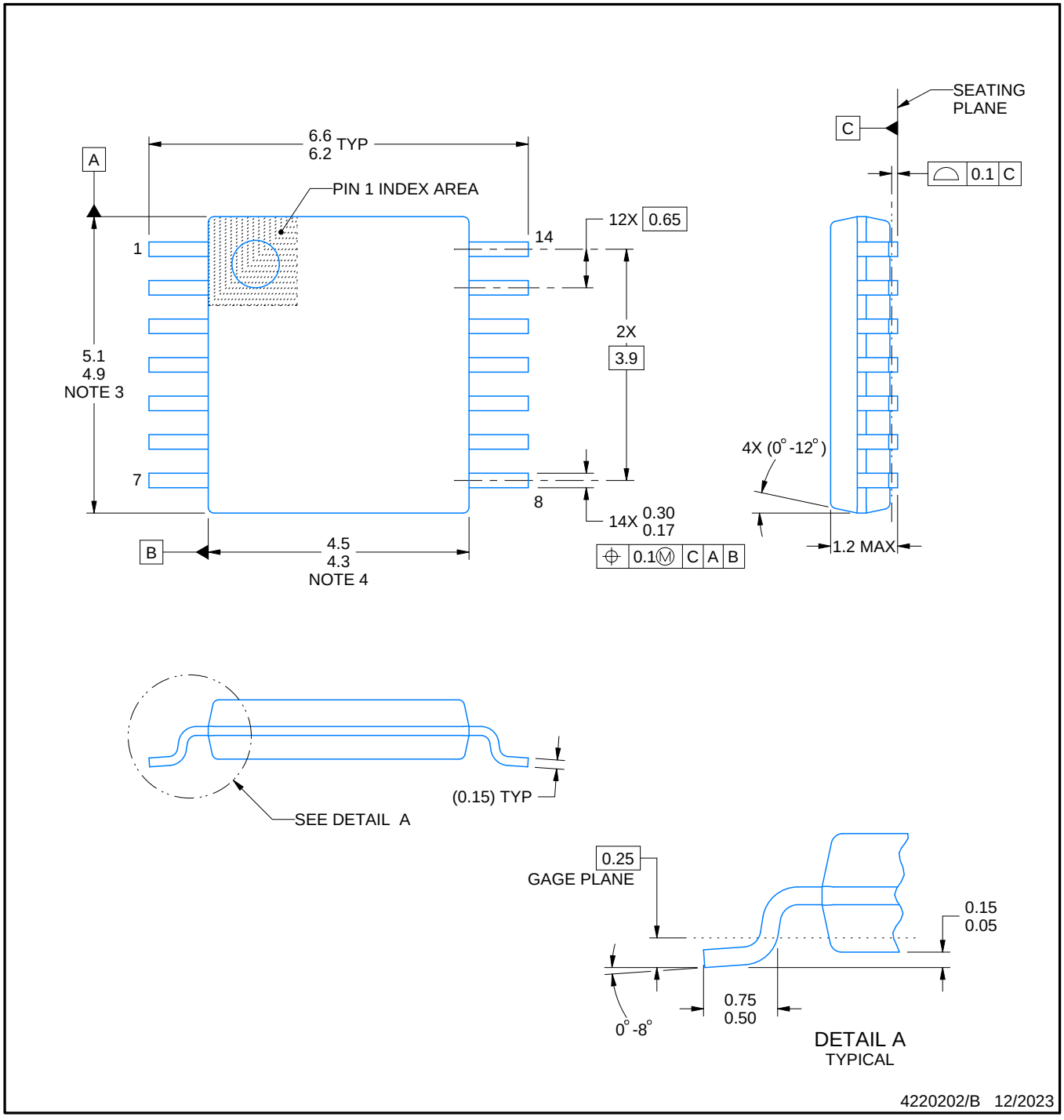
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

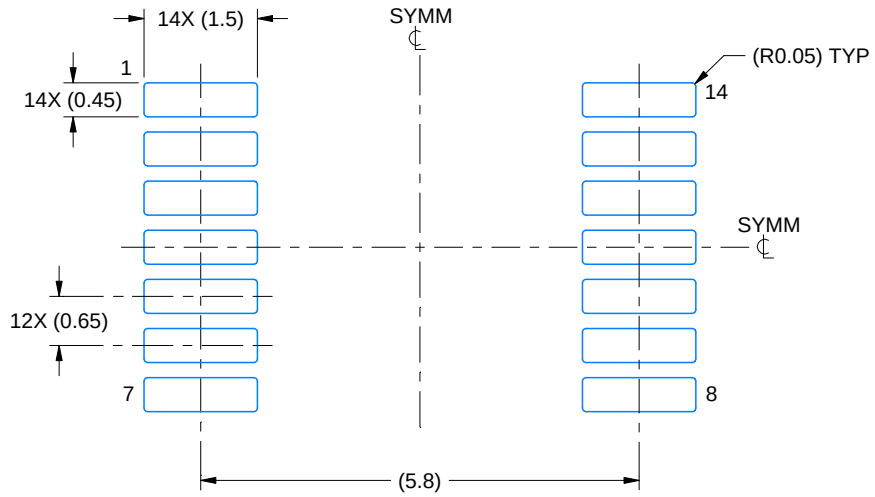
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

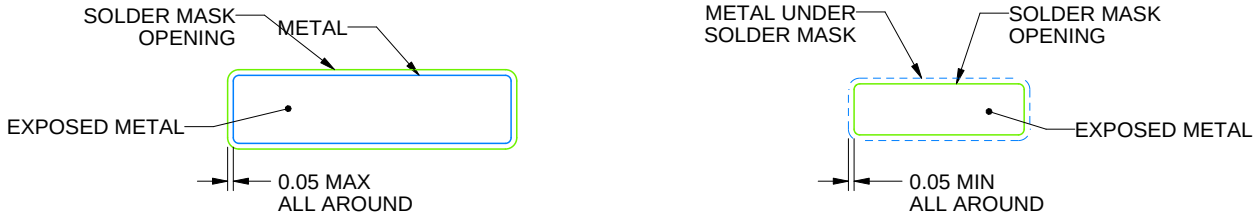


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

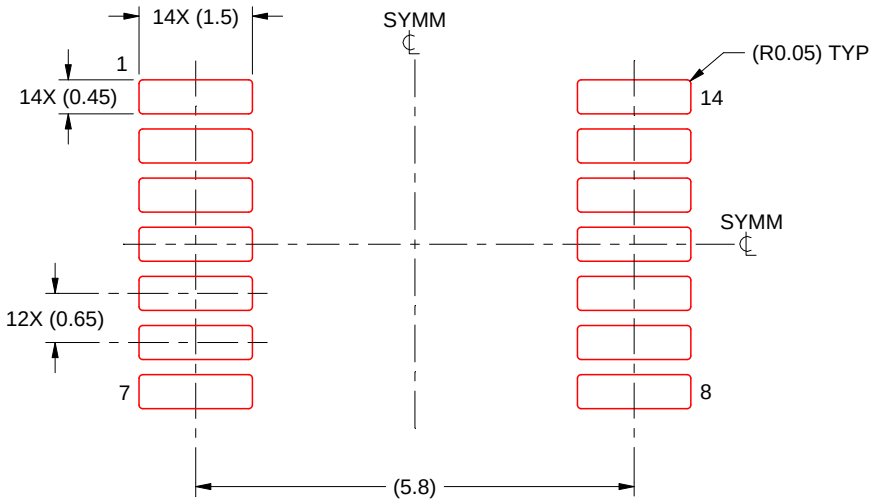


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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