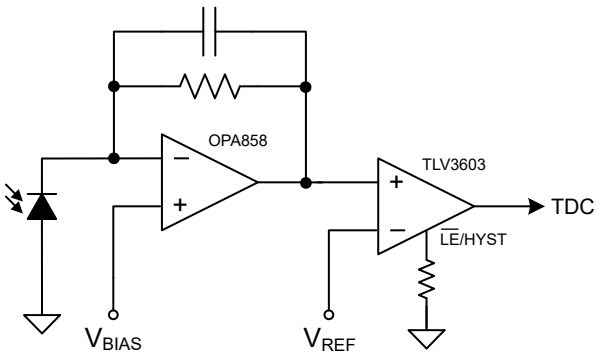
TLV3601-Q1, TLV3603-Q1 325MHz High-Speed Comparator with 2.5ns Propagation Delay

1 Features

- Low propagation delay: 2.5 ns
- Low overdrive dispersion: 600 ps
- High toggle frequency: 325 MHz
- Narrow pulse width detection capability: 1 ns
- Push-Pull output
- Supply range: 2.4V to 5.5 V
- Input common-mode range extends 200 mV beyond both rails
- Low input offset voltage: ±5 mV
- Packages: TLV3601 (5-Pin SC70), TLV3603 (6-Pin SC70)

2 Applications

- DC/DC Converter
- Inverter & Motor Control
- Fuel Cell Control Unit (FCCU)
- Battery Management System (BMS)
- Mechanically Scanning LIDAR
- Audio Amplifier



TLV3603 Application Circuit

3 Description

TLV3601-Q1 and TLV3603-Q1 are 325 MHz, high speed comparators with rail-to-rail inuts and a propagation delay of 2.5 ns. The combination of fast response and wide operating voltage range make the comparators suitale for narrow signal pulse detection and data and clock recovery applictions in LIDAR, range finders, and line receivers.

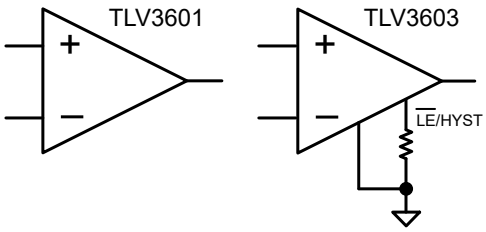
The push-pull (single-ended) outputs of the TLV3601-Q1 and TLV3603-Q1 simplify and save cost on board-to-board wiring for I/O interfaces while reducing power consumption when compared to alternative high-speed differential output comparators. They can directly interface most prevailing digital controllers and IO expanders in the downstream.

TLV3601-Q1 is available in tiny 5-pin SC70 package which makes it well suited for space constrained equipment. TLV3603-Q1 is packaged in a 6-pin SC70 package and maintains the same speed and size as TLV3601-Q1 while offering the additional features of adjustable hysteresis control and output latch capability.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV3601-Q1	SC70 (5)	1.25 mm × 2.00 mm
TLV3603-Q1	SC70 (6)	1.25 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

DATE	REVISION	NOTES
June 2021	*	Initial release.

5 Pin Configuration and Functions

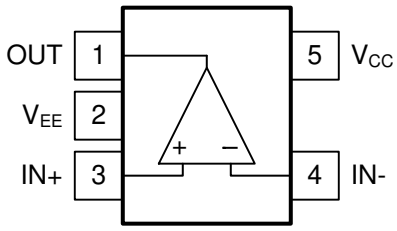

Figure 5-1. DCK Package
5-Pin SC70
Top View

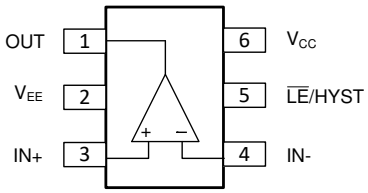

Figure 5-2. DCK Package
6-Pin SC70
Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TLV3601	TLV3603		
IN+	3	3	I	Non-inverting input
IN–	4	4	I	Inverting input
OUT	1	1	O	Output (Push-pull)
V_{EE}	2	2	I	Negative power supply
V_{CC}	5	6	I	Positive power supply
$\overline{LE}$/HYS	-	5	I	Adjustable hysteresis control and latch

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	–0.3	6	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CC} + 0.3	V
Differential Input Voltage (V_{DI} = IN+, IN–)	–5.5	5.5	V
Output Voltage (OUT)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{LE}$/HYS)(2)		±10	mA
Current into Output pins (OUT)(3)		±50	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 50 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		TLV3601 DCK (SC70) 5 PINS	TLV3603 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	165.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139.2	129.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.8	58.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	43.0	39.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.5	58.7	°C/W

6.5 Electrical Characteristics (V_{CC} = 3.3 V)

V_{CC} = 3.3 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input offset voltage	T_A = –40°C to +125°C	–5	±0.5	5	mV
dV_{IO}/dT	Input offset voltage drift			±2.5		µV/°C
V_{CM}	Input common mode voltage range	T_A = –40°C to +125°C	V_{EE} – 0.2		V_{CC} + 0.2	V
V_{HYST} (TLV3601)	Input hysteresis voltage	T_A = –40°C to +125°C	1.5	3	5	mV
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			5		MΩ
I_B	Input bias current	T_A = –40°C to +125°C		1	5	uA
I_{OS}	Input offset current			±0.03		uA
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.2V		80		dB
PSRR	Power-supply rejection ratio	V_{CC} = 2.4 to 5.5V		80		dB
DC Output Characteristics						
V_{OH}	Output high voltage from the rail	I_{SOURCE} = 1 mA T_A = –40°C to +125°C	80	60		mV
V_{OL}	Output low voltage from the rail	I_{SINK} = 1 mA T_A = –40°C to +125°C		60	80	mV
I_{SC_SOURCE}	Output Short-Circuit Current - Source	T_A = –40°C to +125°C	10	50		mA
I_{SC_SINK}	Output Short-Circuit Current - Sink	T_A = –40°C to +125°C	10	50		mA
Power Supply						
I_{CC}	quiescent current	T_A = –40°C to +125°C		6	8	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			1.7		V
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV		2.5	3.5	ns
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV T_A = –40°C to +125°C			5	ns
$t_{CM\_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CC}		200		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 125 mV		600		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 125 mV		330		ps
t_R	Rise time	10% to 90%		0.75		ns
t_F	Fall time	90% to 10%		0.75		ns
t_{JITTER}	RMS Jitter	V_{IN} = 100mV_{P-P}, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz		5		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		325		MHz
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		1.0		ns
Latching/Adjustable Hysteresis (TLV3603 only)						
V_{HYST}	Input hysteresis voltage	V_{HYST} = Logic High		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		3		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150 kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56 kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	T_A = –40°C to +125°C	V_{EE} + 1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	T_A = –40°C to +125°C			V_{EE} + 0.35	V
I_{IH_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{CC} T_A = –40°C to +125°C			15	uA
I_{IL_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{EE}, T_A = –40°C to +125°C			40	uA

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6.5 Electrical Characteristics (V_{CC} = 3.3 V) (continued)

V_{CC} = 3.3 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SETUP}	Latch setup time			–2		ns
t_{HOLD}	Latch hold time			2		ns
t_{PL}	Latch to Q and $\overline{Q}$ delay			7		ns

6.6 Timing Diagrams

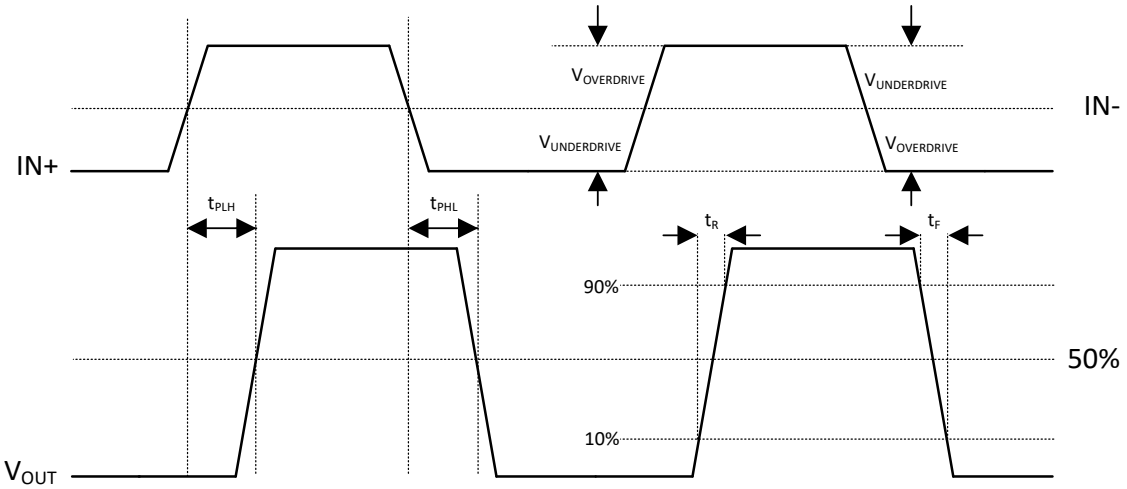


Figure 6-1. General Timing Diagram

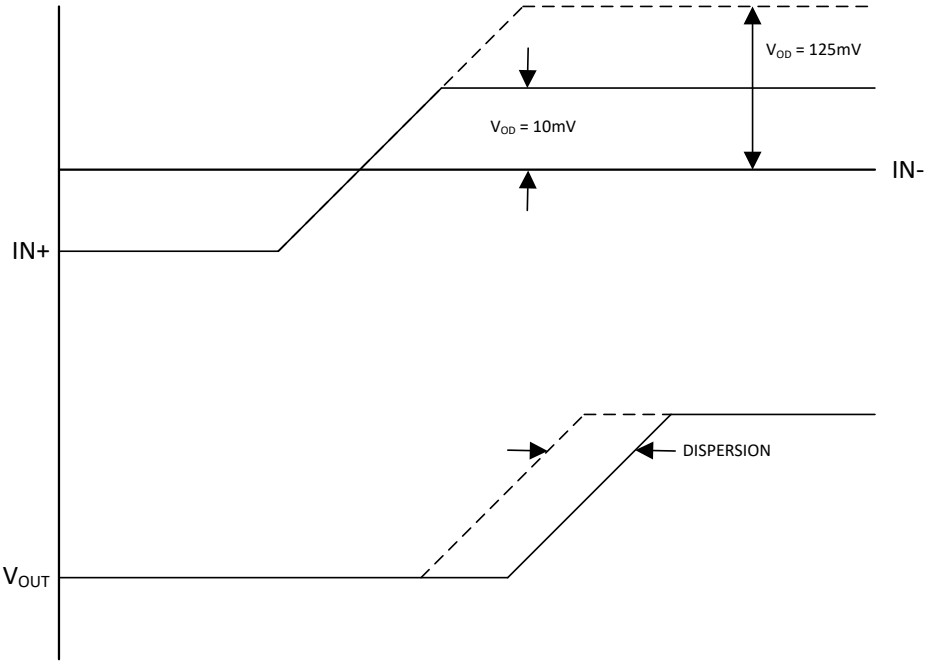


Figure 6-2. Overdrive Dispersion

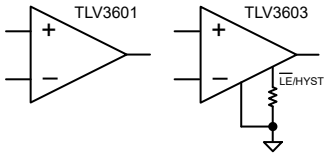
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TLV3601-Q1 and TLV3603-Q1 are high-speed comparators with single-ended (push-pull) output stages. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3601-Q1 is available in a 5-pin SC70 and SOT23, while the TLV3603-Q1 is packaged in a 6-pin SC70 package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3601-Q1 and TLV3603-Q1 are single channel, high speed comparators with a typical propagation delay of 2.5 ns and push-pull outputs. The minimum pulse width detection capability is 1 ns and the typical toggle rate is 325 MHz. These comparators are well-suited for distance measurement applications that utilize a time-of-flight arechitecture as well as systems that suffer from capacitive loading and require data and clock recovery. In addition to their high speed, the TLV3601-Q1 and TLV3603-Q1 offer rail-to-rail input stages capable of operating up to 200 mV beyond each power supply rail combined with a maximum 5 mV input offset. The TLV3603-Q1 also provides adjustable hysteresis via an external resistor for noise supression or a latching mode to hold the output of the comparators.

7.4 Device Functional Modes

The TLV3601-Q1 has a single functional mode and is active when the power supply voltage is greater than 2.4V. The TLV3603-Q1 has two modes of operation. The first is an active mode where the output reflects the condition at the inputs when an external resistor is connected to ground on the LEB/HYST pin. The second is a latch mode where the output is held at its last active state when the LEB/HYST pin is pulled low. The TLV3603-Q1 returns to active mode after a short delay when the pin is pulled high.

7.4.1 Inputs

The TLV3601-Q1 and TLV3603-Q1 feature input stages capable of operating o –200 mV below negative power supply (ground) and 200 mV beyond the positive supply voltage, allowing for zero cross detection and maximizing input dynamic range given a certain power supply. The input stages are protected from conditions where the voltage on either pin exceeds this level by internal ESD protection diodes to VCC and VEE. An external resistor should be used to limit the current to less than 10mA.

7.4.2 Push-Pull (Single-Ended) Output

The TLV3601-Q1 and TLV3603-Q1 outputs have excellent drive capability and are designed to connect directly to CMOS logic input devices. Likewise, the comparator output stages can drive capacitive loads. Transient performance parameters in the Electrical Characteristics Tables and Typical Characteristics section are for a load of 5pF, corresponding to a standard CMOS load. Device performance for larger capacitive loads can be found in the typical performance curves titled Propagation Delay vs Capacitive Load and Toggle Rate vs Capacitive Load. For optimal speed and performance, output load capacitance should be reduced as much as possible.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV360x comparators feature rail-to-rail inputs and outputs on supply voltages as low as 2.4 V. The LVDS output stage is optimal for high speed applications that require low power consumption. The 1ns propagation delay of the device makes it a suitable fit for applications involving optical reception, triggers for test and measurement systems, and transceiver type applications that require a high speed signal to be carried over a certain distance.

8.1.1 Adjustable Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between "logic high" and "logic low" states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be overcome by adding hysteresis to the comparator.

Since the TLV3604 does not have internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Typical Application section for more details. The TLV3605 on the other hand has a LE/HYST pin that can be used to increase the internal hysteresis of the comparator. In order to change the internal hysteresis of the TLV3605, connect a single resistor as shown in the adjusting hysteresis figure between the LE/HYST pin and VEE. A curve of hysteresis versus resistance is provided below to provide guidance in setting the desired amount of hysteresis

8.1.2 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay (see Typical Characteristics). However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.3 Latch Functionality

The latch pin for the TLV3603-Q1 holds the output state of the device when the voltage at the LEB/HYST pin is less than 800mV above VEE. This is particularly useful when the output state is intended to remain unchanged. An important consideration of the latch functionality is the latch hold and setup times. Latch hold time is the minimum time (after the latch pin is asserted) required for properly latching the comparator output. Likewise, latch setup time is defined as the time that the input must be stable before the latch pin is asserted low. The figure below illustrates when the input can transition for a valid latch. Note that the typical setup time in the EC table is negative; this is due to the internal trace delays of the LEB/HYST pin relative to the input pin trace delays. A small delay in the output response is shown below when the TLV3603-Q1 exits a latched output stage.

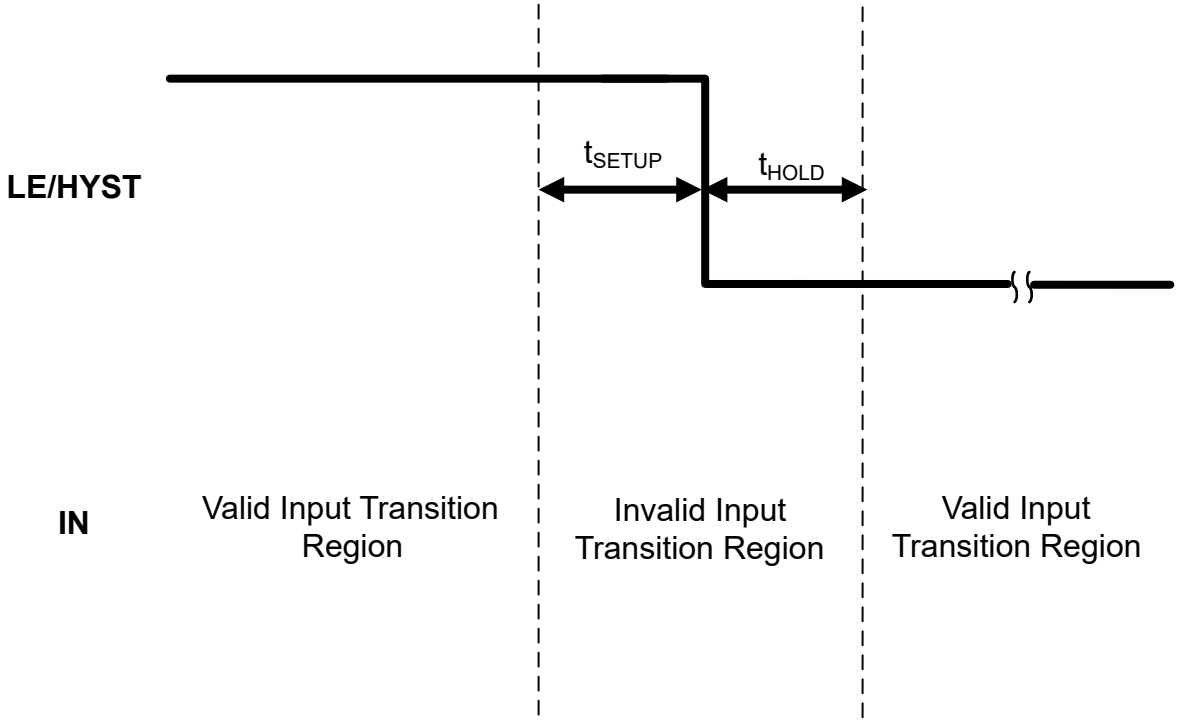


Figure 8-1. Input Change Properly Latched

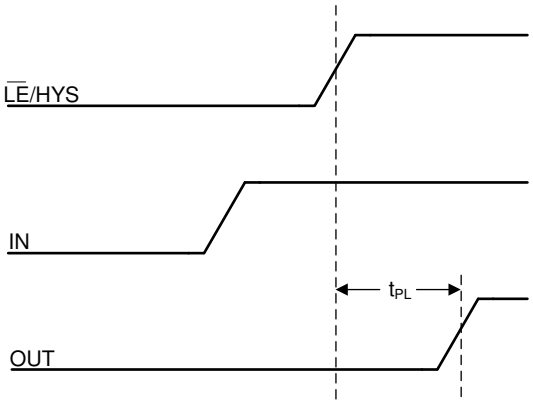


Figure 8-2. Latch Disable with Input Change

8.2 Typical Application

8.2.1 Optical Receiver

The TLV3601-Q1 and TLV3603-Q1 can be used in conjunction with a high performance amplifier such as the OPA858 to create an optical receiver as shown in the figure below. The photodiode is connected to a bias voltage and is being driven with a pulsed laser. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV3601-Q1 and TLV3603-Q1 will then output the proper output signal according to the threshold set (V_{REF}).

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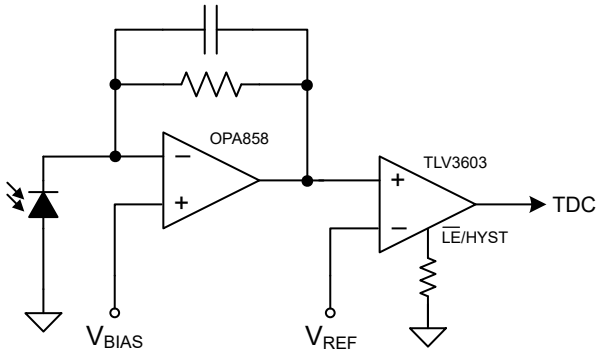


Figure 8-3. Optical Receiver

9 Power Supply Recommendations

The TLV3601-Q1 and TLV3603-Q1 are specified for operation from 2.4 V to 5.5 V. The comparators can operate from single-sided or split bipolar supplies. Many specifications apply from –40°C to 125°C.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.

   Likewise, high performance board materials such as Rogers or high speed FR4 is also recommended.
2. Place a decoupling capacitor (100-pF ceramic, surface-mount capacitor) between V_{CC} and

   V_{EE} as close to the device as possible. Using multiple bypass capacitors in different decade ranges such as 100-pF, 100-nF, and 1-µF provides the best noise reduction across frequency ranges.
3. On the inputs and the output, keep lead lengths as short and minimize capacitive coupling to the traces by having a keepout area around the traces that is 3x the width of the traces. It is also recommended to keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.

10.2 Layout Example

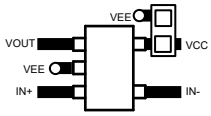


Figure 10-1. TLV3601 Layout Example

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLV3601QDCKTQ1	ACTIVE	SC70	DCK	5	250	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
PLV3603QDCKTQ1	ACTIVE	SC70	DCK	6	250	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

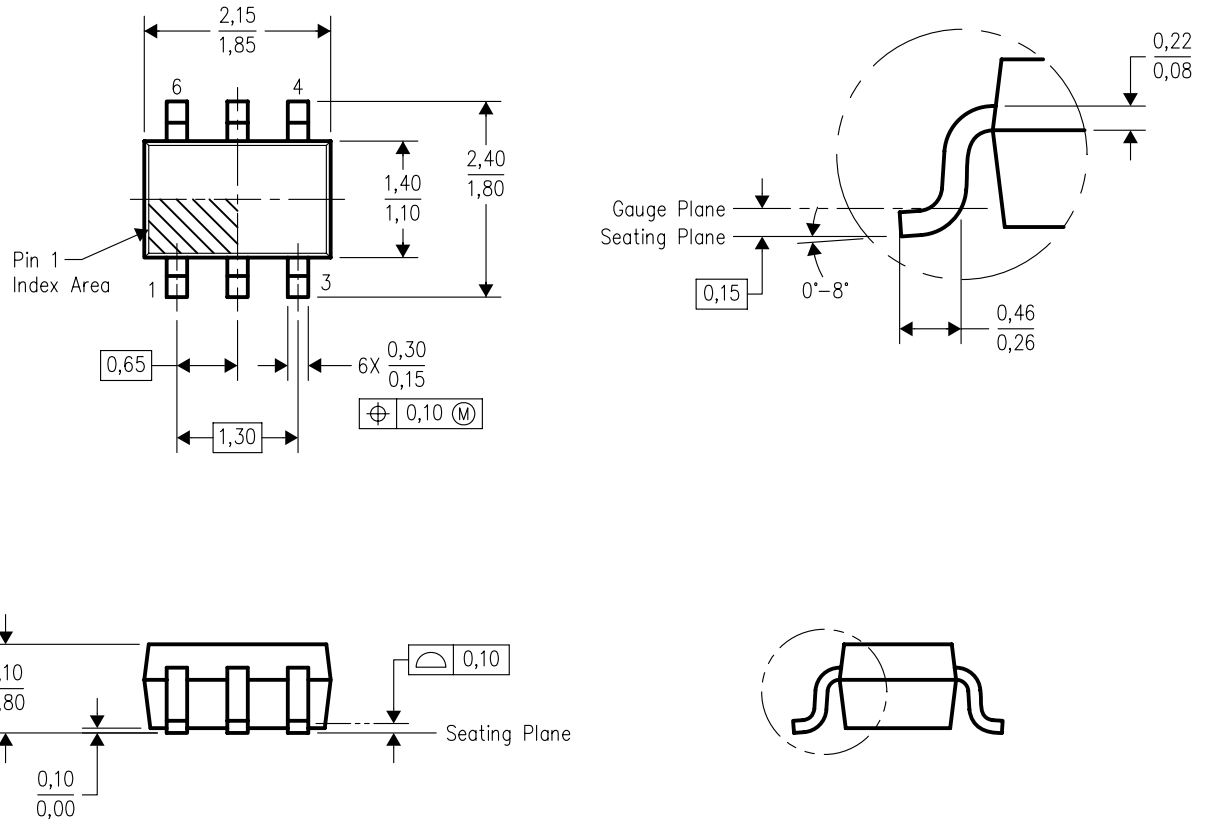
OTHER QUALIFIED VERSIONS OF TLV3601-Q1 :

- Catalog : TLV3601

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

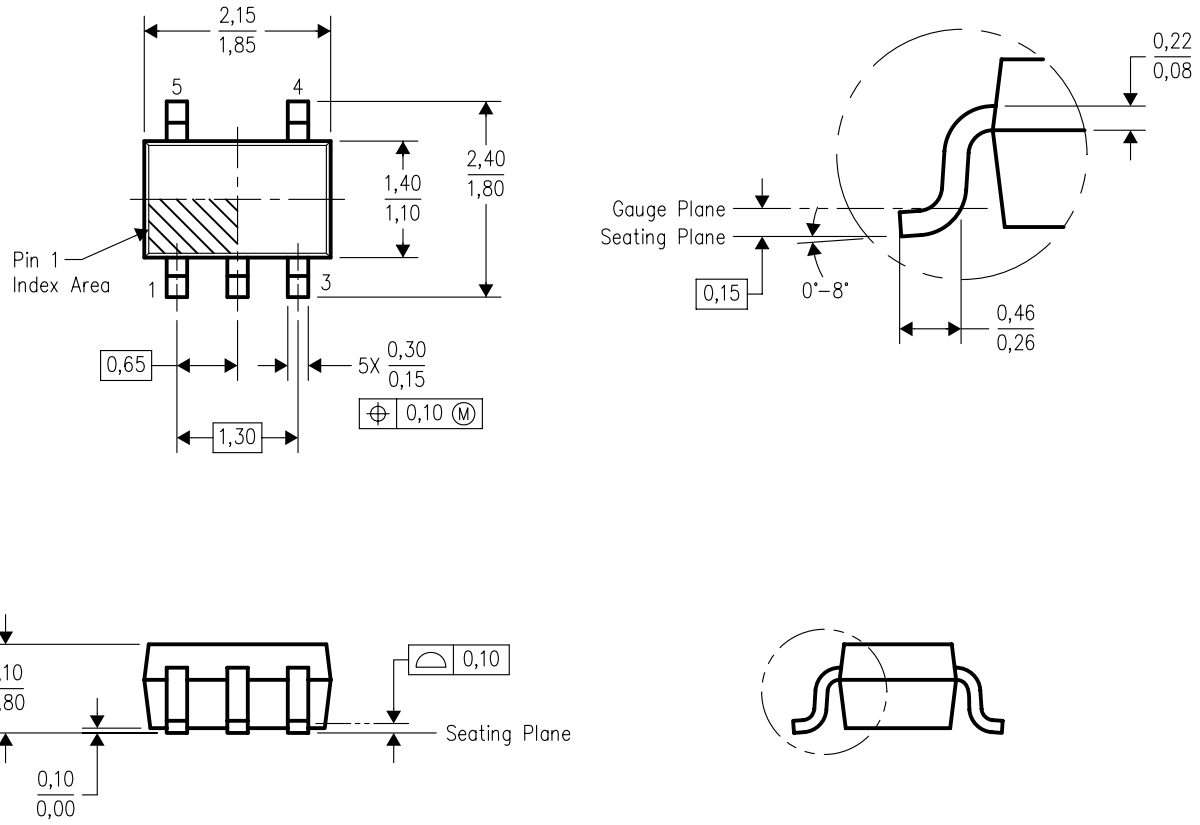
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

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