TLV915x-Q1 4.5MHz、レール ツー レール I/O、低オフセット電圧、低ノイズ車載オペアンプ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:-40℃～+125℃、T_A
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C6
- 低いオフセット電圧:±125μV
- 低いオフセット電圧ドリフト:±0.3μV/℃
- 低ノイズ:1kHz で 10.8nV/√Hz
- 大きい同相除去:120dB
- 低いバイアス電流:±10pA
- レール ツー レール入出力
- 広い帯域幅:4.5MHz GBW
- 高いスルーレート:21V/μs
- 低い静止電流:アンプ 1 個あたり 560μA
- 広い電源範囲:±1.35V～±8V、2.7V～16V
- 堅牢な EMIRR 性能:入力ピンの EMI/RFI フィルタ

2 アプリケーション

- AEC-Q100 グレード 1 機器に対して最適化
- インフォテインメントとクラスタ
- パッシブ型安全運転支援システム
- ボディ・エレクトロニクス / 照明
- HEV/EV のインバータおよびモータ制御
- オンボード・チャージャ (OBC) とワイヤレス・チャージャ
- パワートレイン電流センサ
- 先進運転支援システム (ADAS)
- ハイサイドおよびローサイド電流センシング

3 概要

TLV915x-Q1 ファミリ (TLV9151-Q1、TLV9152-Q1、TLV9154-Q1) は、車載用 16V 汎用オペアンプ ファミリです。これらのデバイスは、レール ツー レールの出力、低いオフセット (±125μV、標準値)、低いオフセット ドリフト (±0.3μV/℃、標準値)、4.5MHz の帯域幅などの優れた DC 精度と AC 性能を備えています。

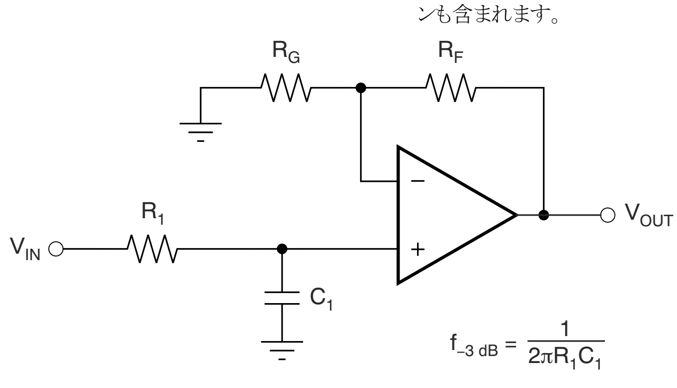
広い差動入力電圧範囲、大きな出力電流 (±75mA)、高いスルーレート (21V/μs)、低ノイズ (10.8nV/√Hz) といった便利な機能を備えた TLV915x は、車載アプリケーションに適した堅牢な低ノイズのオペアンプです。

TLV915x-Q1 ファミリのオペアンプは標準パッケージで供給され、-40℃～125℃で動作が規定されています。

製品情報

部品番号	チャネル数	パッケージ (1)	パッケージ サイズ(2)
TLV9151-Q1	シングル	DBV (SOT-23、5)	2.9mm × 2.8mm
		DCK (SC70、5)	2mm × 2.1mm
	シングル、シャットダウン	DBV (SOT-23、6)	2.9mm × 2.8mm
TLV9152-Q1	デュアル	D (SOIC、8)	4.9mm × 6mm
		PW (TSSOP、8)	3mm × 6.4mm
		DGK (VSSOP、8)	3mm × 4.9mm
TLV9154-Q1	クワッド	D (SOIC、14)	8.65mm × 6mm
		DYY (SOT-23、14)	4.2mm × 3.26mm
		PW (TSSOP、14)	5mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



$$f_{-3\ dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

単極、ローパス フィルタの TLV915x-Q1

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4 Pin Configuration and Functions

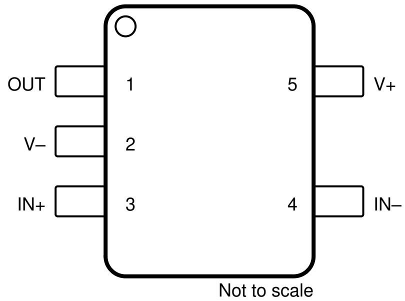


図 4-1. TLV9151-Q1 DBV Package, 5-Pin SOT-23 (Top View)

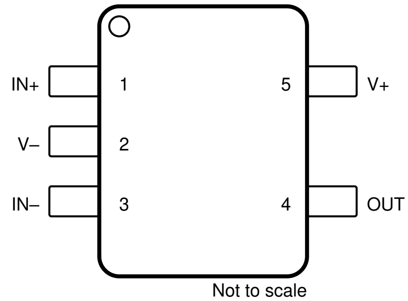


図 4-2. TLV9151-Q1 DCK Package, 5-Pin SC70 (Top View)

表 4-1. Pin Functions: TLV9151-Q1

PIN			TYPE(1)	DESCRIPTION
NAME	DBV	DCK		
IN+	3	1	I	Noninverting input
IN–	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

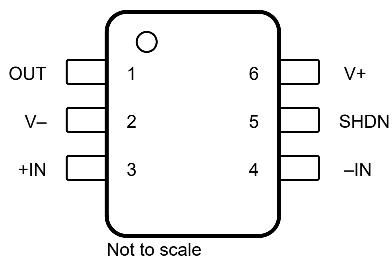


図 4-3. TLV9151S-Q1 DBV Package, 6-Pin SOT-23 (Top View)

表 4-2. Pin Functions: TLV9151S-Q1

PIN		TYPE1	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	4	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amplifier enabled, high = amplifier disabled. See セクション 6.3.9 for more information.
V+	6	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

1. I = input, O = output

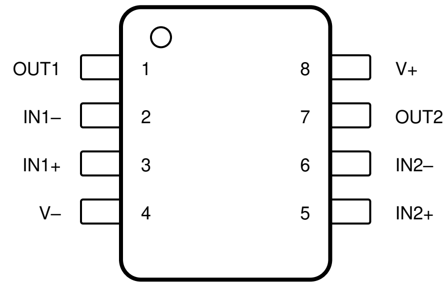


図 4-4. TLV9152-Q1 D, PW and DGK Package, 8-Pin SOIC, TSSOP and VSSOP (Top View)

表 4-3. Pin Functions: TLV9152-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN1–	2	I	Inverting input, channel 1
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

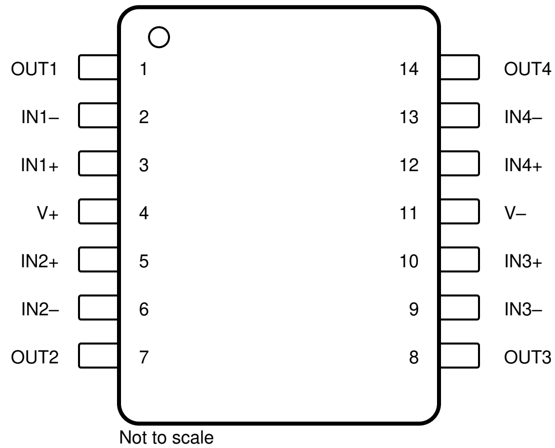


図 4-5. TLV9154-Q1 D, DYY, and PW Package, 14-Pin SOIC, SOT-23, and TSSOP (Top View)

表 4-4. Pin Functions: TLV9154-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	20	V
Signal input pins	Common-mode voltage (3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3)		V_S + 0.2	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	TLV9151SQDBVRQ1 only	±1000	V
			All other devices	±2000	
		Charged device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	16	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
V_{IH}	High level input voltage at shutdown pin (amplifier enabled)	1.1	(V+)	V
V_{IL}	Low level input voltage at shutdown pin (amplifier disabled)	(V–)	0.2	V
T_A	Specified ambient temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC [1]		TLV9151-Q1, TLV9151S-Q1			UNIT
		DBV (SOT-23)		DCK (SC70)	
		5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.4	167.8	202.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	107.9	101.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	49.7	47.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.8	33.9	18.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.3	49.5	47.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC [1]		TLV9152-Q1			Unit
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.6	176.5	185.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.4	68.1	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.1	98.2	115.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.0	12.0	12.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.4	96.7	114.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC [1]		TLV9154-Q1			UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.4	110.7	118.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.6	55.9	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.3	35.3	60.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.5	2.3	6.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.9	35.1	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±125	±895	µV
			T_A = –40°C to 125°C			±925	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.3		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 4 V to 16 V	T_A = –40°C to 125°C		±0.3	±1.5	µV/V
		V_{CM} = V–, V_S = 2.7 V to 16 V(4)			±1	±10.6	
	Channel separation	f = 0 Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
			T_A = –40°C to 125°C(4)			±1	nA
I_{OS}	Input offset current				±10		pA
			T_A = –40°C to 125°C(4)			±1	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			1.8		$µV_{PP}$
					0.3		$µV_{RMS}$
e_N	Input voltage noise density	f = 1 kHz			10.8		nV/√Hz
		f = 10 kHz			9.4		
i_N	Input current noise	f = 1 kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 16 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)	T_A = –40°C to 125°C	99	130		dB
		V_S = 4 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)		82	100		
		V_S = 2.7 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)(4)		75	95		
		V_S = 2.7 V to 16 V, (V+) – 1 V < V_{CM} < (V+) + 0.1 V (Aux input pair)			85		
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 16 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	145		dB
			T_A = –40°C to 125°C		142		
		V_S = 4 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		104	130		
			T_A = –40°C to 125°C		125		
		V_S = 2.7 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V(4)		101	120		
			T_A = –40°C to 125°C		118		

5.7 Electrical Characteristics (続き)

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				4.5		MHz
SR	Slew rate	V_S = 16 V, G = +1, C_L = 20 pF			21		V/µs
t_S	Settling time	To 0.01%, V_S = 16 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			2.5		µs
		To 0.01%, V_S = 16 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			1.5		
		To 0.1%, V_S = 16 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			2		
		To 0.1%, V_S = 16 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			1		
	Phase margin	G = +1, R_L = 10 kΩ			60		°
	Overload recovery time	V_{IN} × gain > V_S			400		ns
THD+N	Total harmonic distortion + noise (1)	V_S = 16 V, V_O = 3 V_{RMS}, G = 1, f = 1 kHz			0.00021%		
OUTPUT							
	Voltage output swing from rail (positive and negative)	V_S = 16 V, R_L = no load			5	10	mV
			T_A = –40°C to 125°C(4)			15	
		V_S = 16 V, R_L = 10 kΩ			50	55	
			T_A = –40°C to 125°C(4)			75	
		V_S = 16 V, R_L = 2 kΩ			200	250	
			T_A = –40°C to 125°C(4)			350	
		V_S = 2.7 V, R_L = no load			1	6	
			T_A = –40°C to 125°C(4)			10	
		V_S = 2.7 V, R_L = 10 kΩ			5	12	
			T_A = –40°C to 125°C(4)			18	
		V_S = 2.7 V, R_L = 2 kΩ			25	40	
			T_A = –40°C to 125°C(4)			60	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				1000		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			525		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			560	685	µA
		I_O = 0 A, (TLV9151-Q1)			560	691	
		I_O = 0 A	T_A = –40°C to 125°C			750	
		I_O = 0 A, (TLV9151-Q1)				769	
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	V_S = 2.7 V to 16 V, all amplifiers disabled, $\overline{SHDN}$ = V–			30	45	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 2.7 V to 16 V, amplifier disabled			320 || 2		MΩ || pF
V_{IH}	Logic high threshold voltage (amplifier enabled)				(V–) + 0.8V	(V–) + 1.1V	V
V_{IL}	Logic low threshold voltage (amplifier disabled)			(V–) + 0.2V	(V–) + 0.8V		V
t_{ON}	Amplifier enable time (full shutdown) (2) (3)	G = +1, V_{CM} = V-, V_O = 0.1 × V_S/2			8		µs
t_{ON}	Amplifier enable time (partial shutdown) (2) (3)	G = +1, V_{CM} = V-, V_O = 0.1 × V_S/2			3		
t_{OFF}	Amplifier disable time (2)	V_{CM} = V-, V_O = V_S/2			3		µs

5.7 Electrical Characteristics (続き)

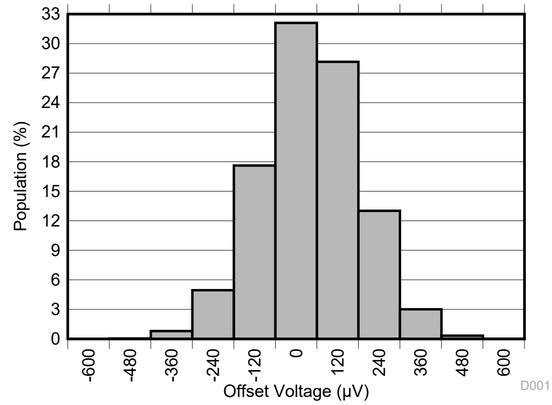
For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	$\overline{\text{SHDN}}$ pin input bias current (per pin)	V_S = 2.7 V to 16 V, (V+) ≥ $\overline{\text{SHDN}}$ ≥ (V–) + 0.9 V		500		nA
		V_S = 2.7 V to 16 V, (V–) ≤ $\overline{\text{SHDN}}$ ≤ (V–) + 0.7 V		150		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.
(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(3) Full shutdown refers to the dual TLVxx2S having both channels 1 and 2 disabled ($\overline{\text{SHDN1}}$ = $\overline{\text{SHDN2}}$ = V–) and the quad TLV9xx4S having all channels 1 to 4 disabled ($\overline{\text{SHDN12}}$ = $\overline{\text{SHDN34}}$ = V–). For partial shutdown, only one $\overline{\text{SHDN}}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.
(4) Specified by characterization only.

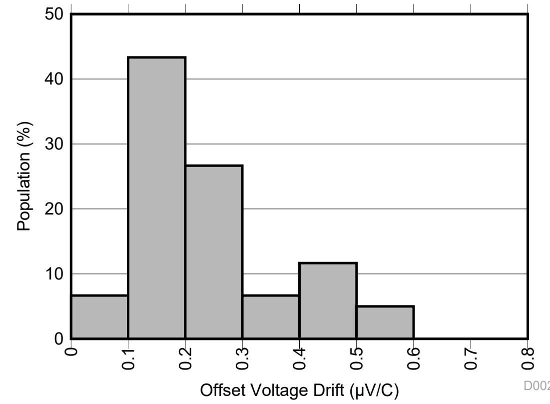
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



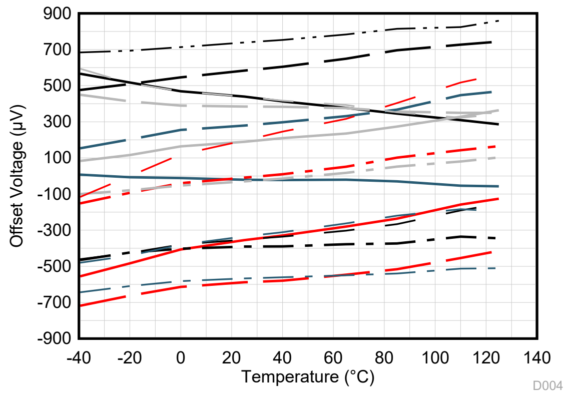
Distribution from 15462 amplifiers, T_A = 25°C

図 5-1. Offset Voltage Production Distribution



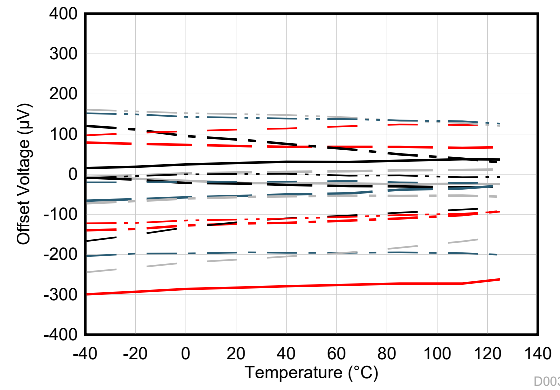
Distribution from 60 amplifiers

図 5-2. Offset Voltage Drift Distribution



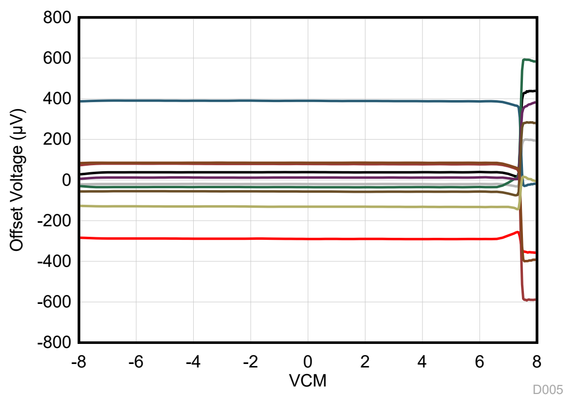
V_{CM} = V+

図 5-3. Offset Voltage vs Temperature



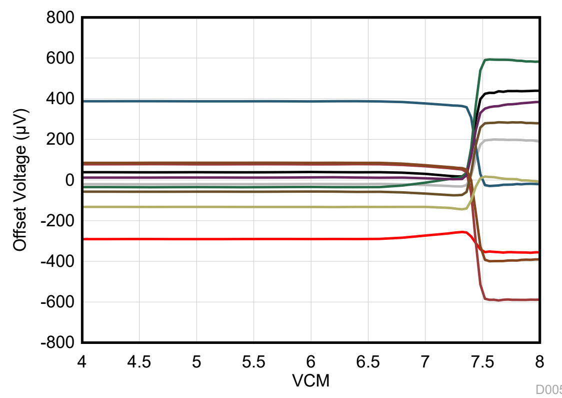
V_{CM} = V–

図 5-4. Offset Voltage vs Temperature



T_A = 25°C

図 5-5. Offset Voltage vs Common-Mode Voltage

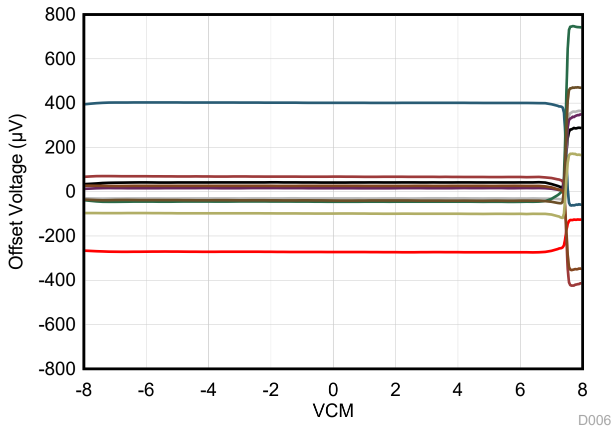


T_A = 25°C

図 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

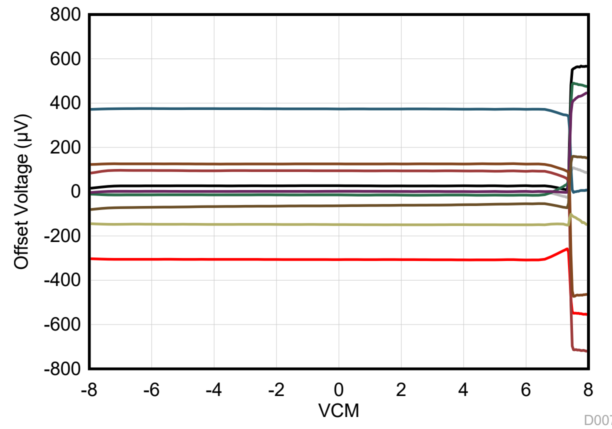
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



T_A = 125°C

図 5-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

図 5-8. Offset Voltage vs Common-Mode Voltage

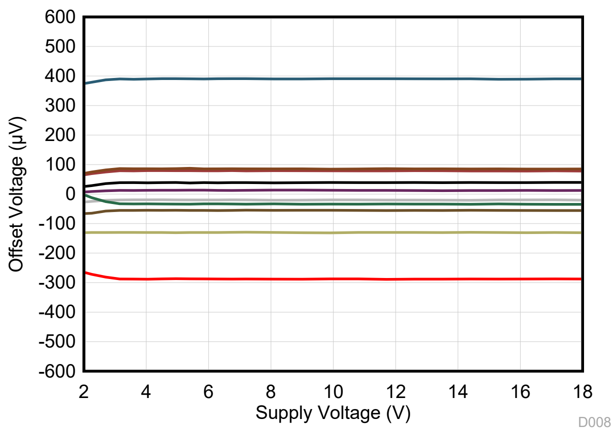
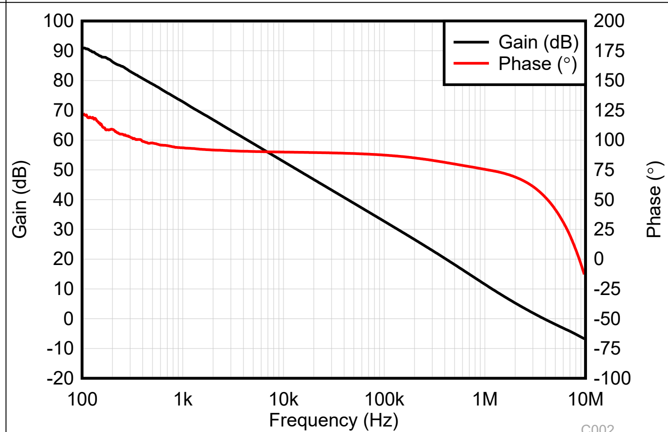


図 5-9. Offset Voltage vs Power Supply



C_L = 20 pF

図 5-10. Open-Loop Gain and Phase vs Frequency

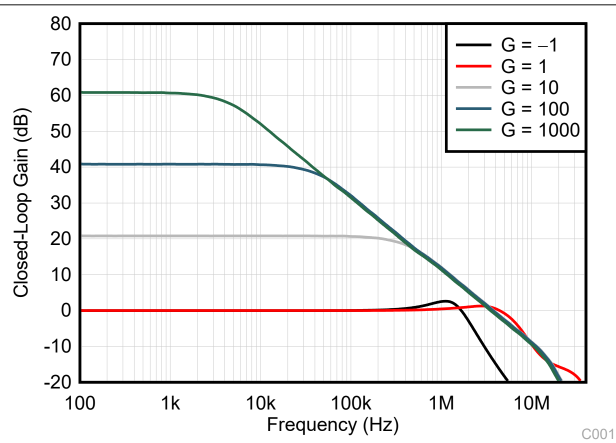


図 5-11. Closed-Loop Gain vs Frequency

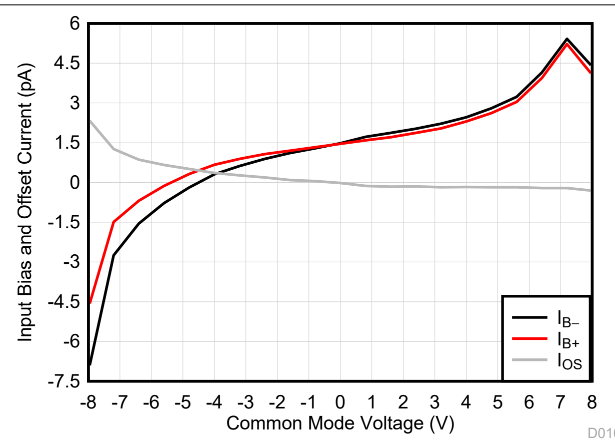


図 5-12. Input Bias Current vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

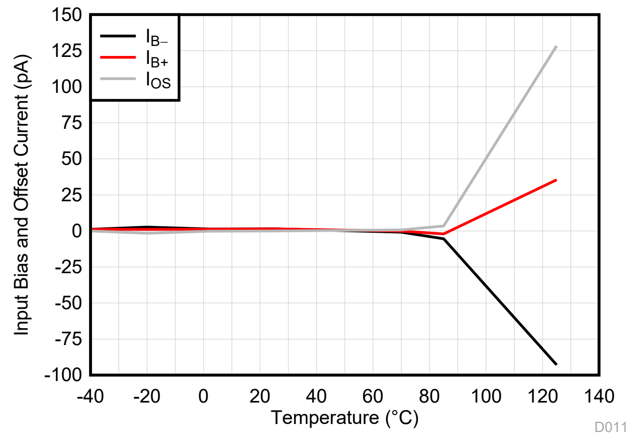


図 5-13. Input Bias Current vs Temperature

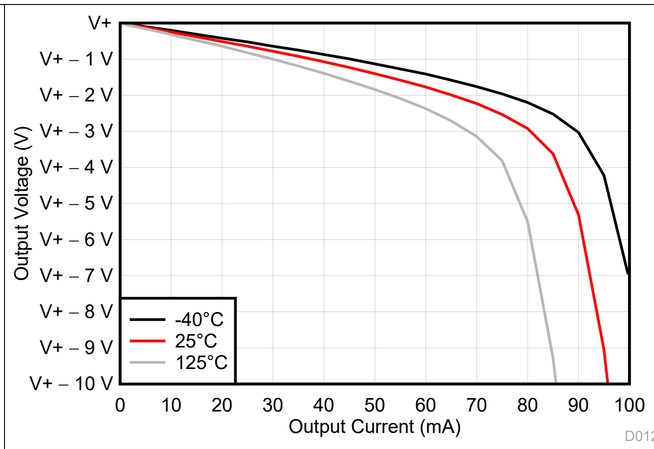


図 5-14. Output Voltage Swing vs Output Current (Sourcing)

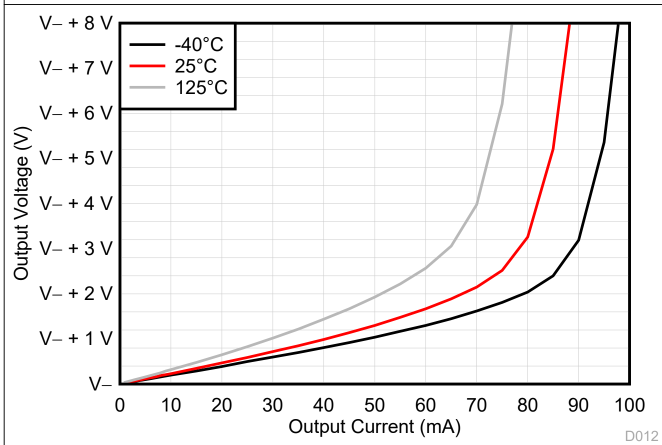


図 5-15. Output Voltage Swing vs Output Current (Sinking)

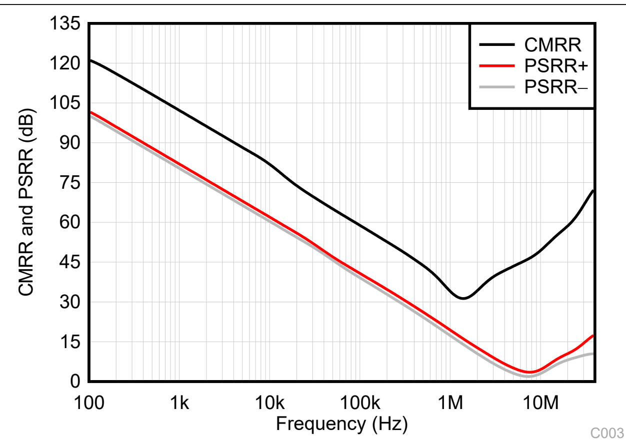
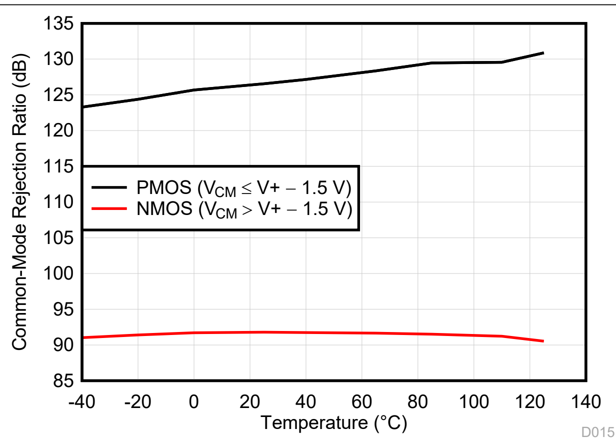
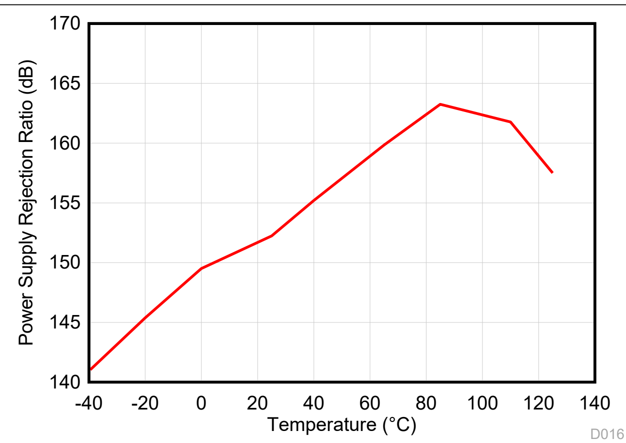


図 5-16. CMRR and PSRR vs Frequency



f = 0 Hz

図 5-17. CMRR vs Temperature (dB)



f = 0 Hz

図 5-18. PSRR vs Temperature (dB)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

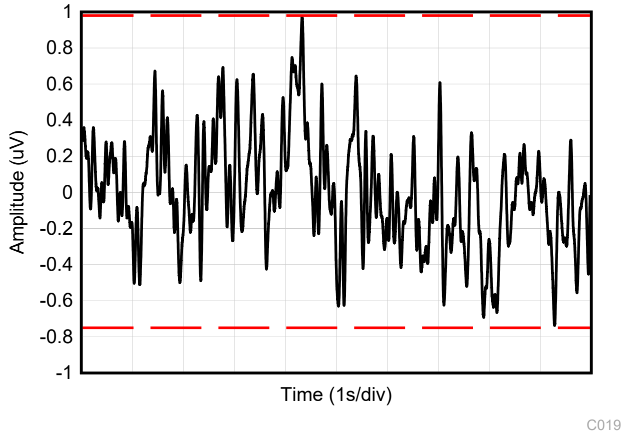


図 5-19. 0.1-Hz to 10-Hz Noise

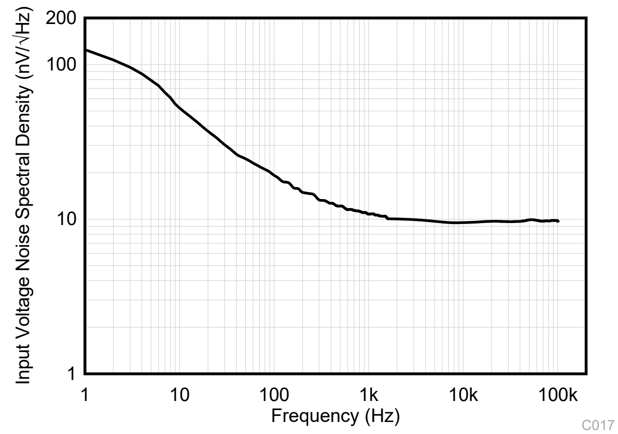
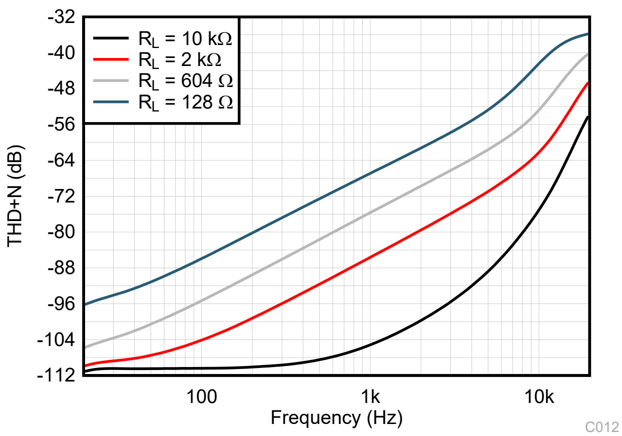
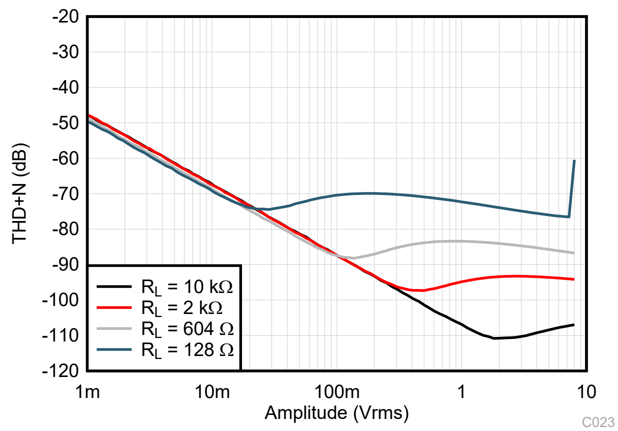


図 5-20. Input Voltage Noise Spectral Density vs Frequency



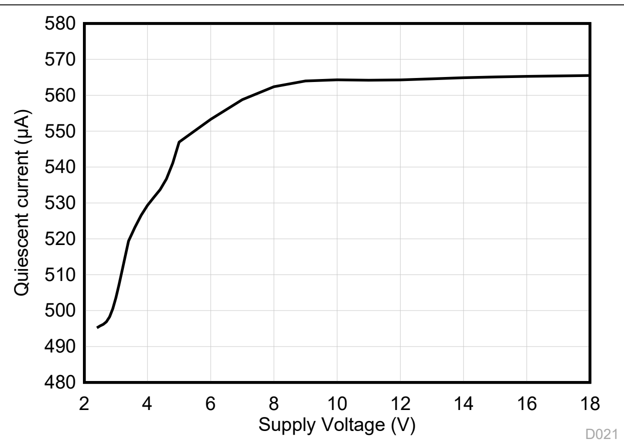
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

図 5-21. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

図 5-22. THD+N vs Output Amplitude



V_{CM} = V–

図 5-23. Quiescent Current vs Supply Voltage

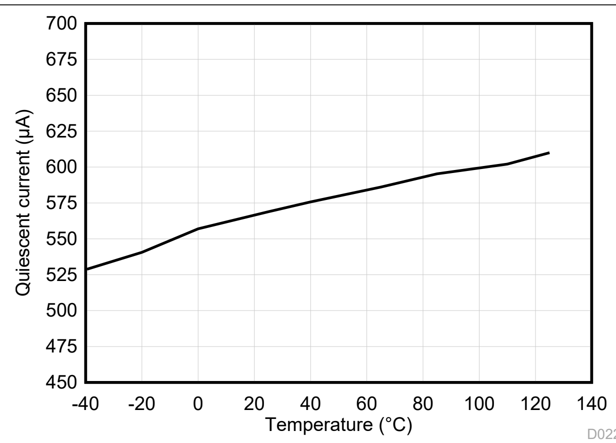


図 5-24. Quiescent Current vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

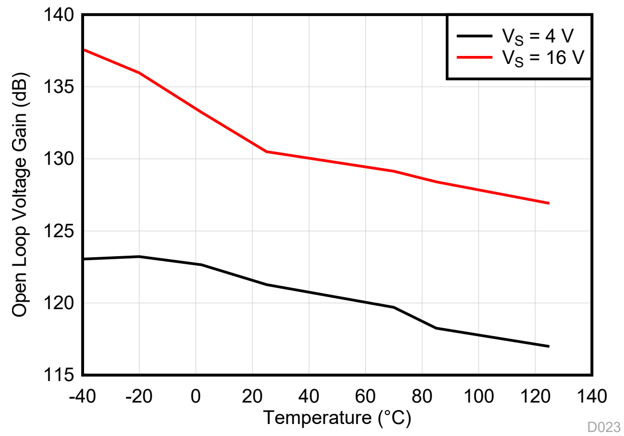


図 5-25. Open-Loop Voltage Gain vs Temperature (dB)

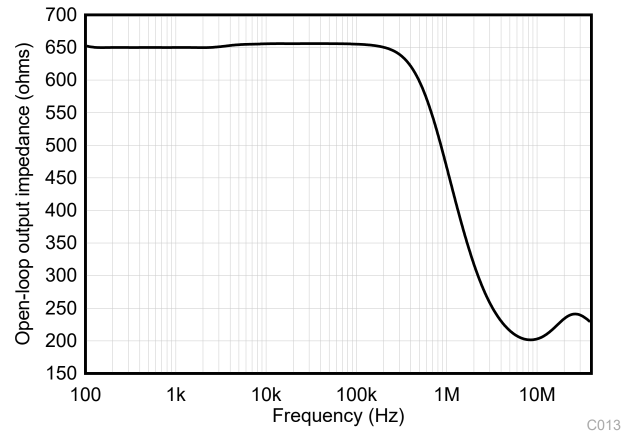
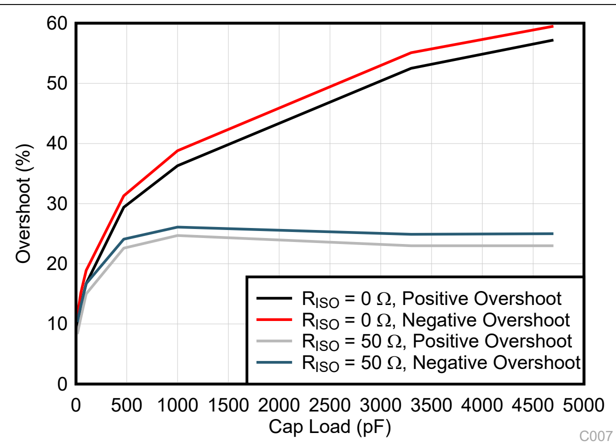
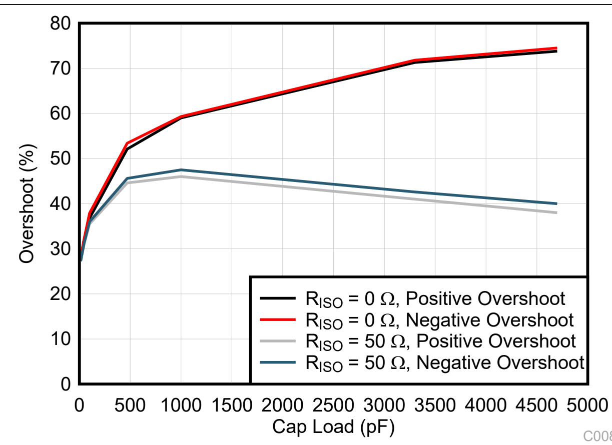


図 5-26. Open-Loop Output Impedance vs Frequency



G = –1, 10-mV output step

図 5-27. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

図 5-28. Small-Signal Overshoot vs Capacitive Load

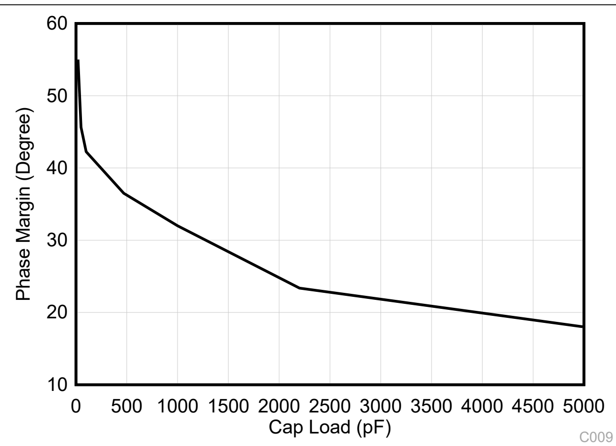
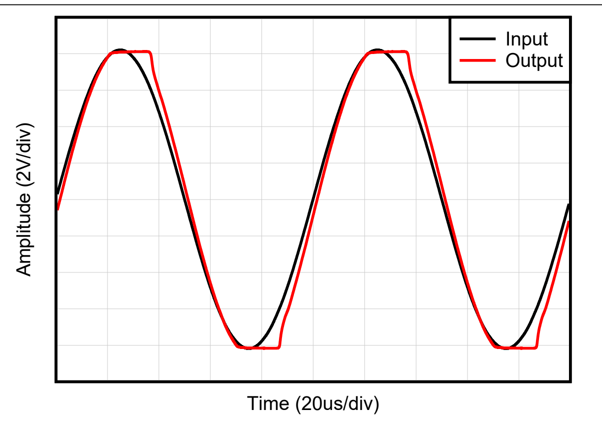


図 5-29. Phase Margin vs Capacitive Load

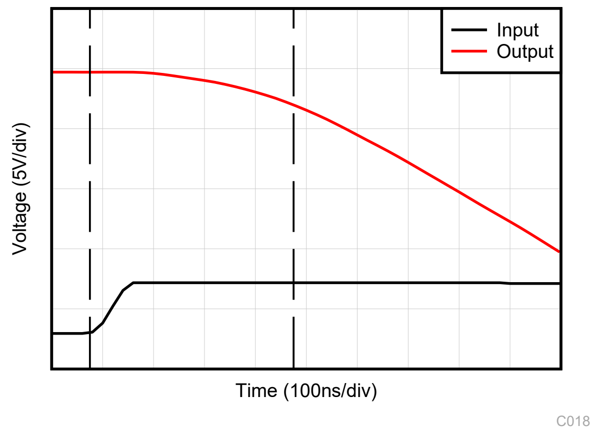


V_{IN} = ±8 V; V_S = V_{OUT} = ±8 V

図 5-30. No Phase Reversal

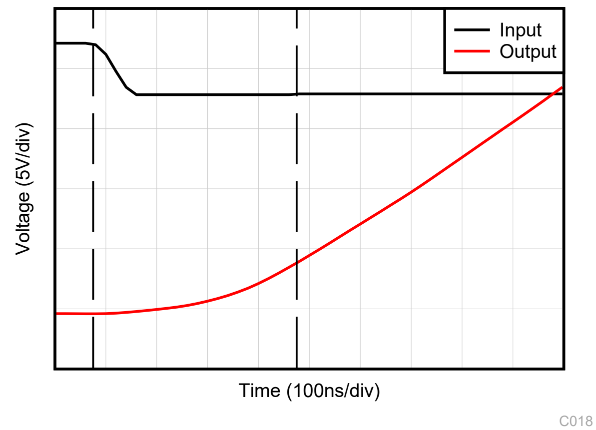
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



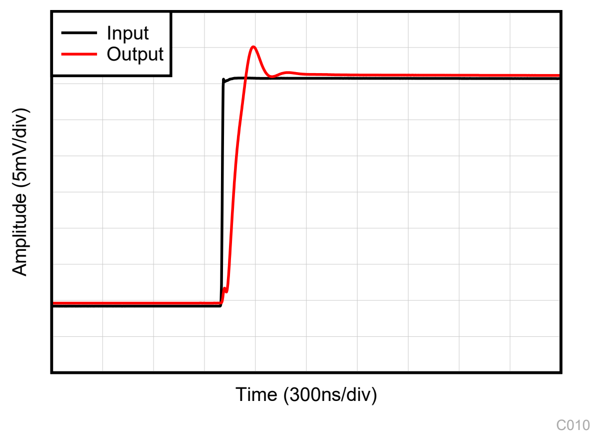
G = –10

図 5-31. Positive Overload Recovery



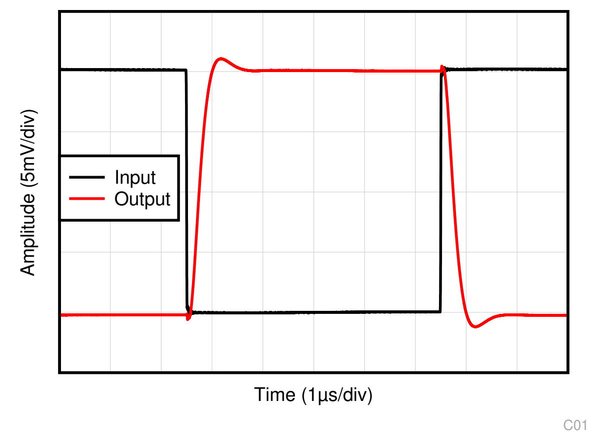
G = –10

図 5-32. Negative Overload Recovery



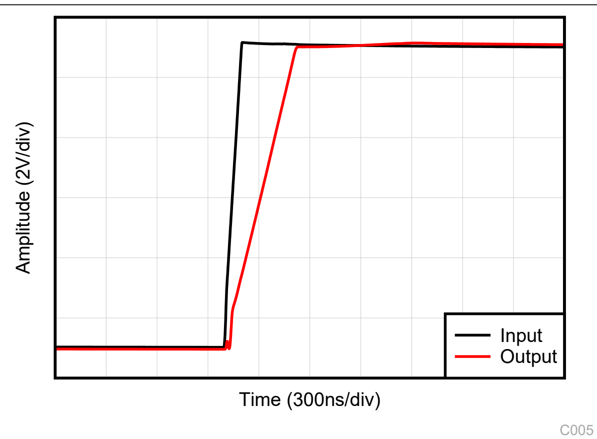
C_L = 20 pF, G = 1, 20-mV step response

図 5-33. Small-Signal Step Response, Rising



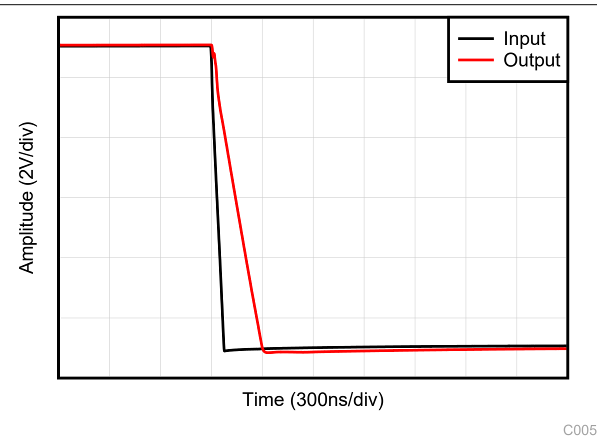
C_L = 20 pF, G = -1, 20-mV step response

図 5-34. Small-Signal Step Response



C_L = 20 pF, G = 1

図 5-35. Large-Signal Step Response (Rising)

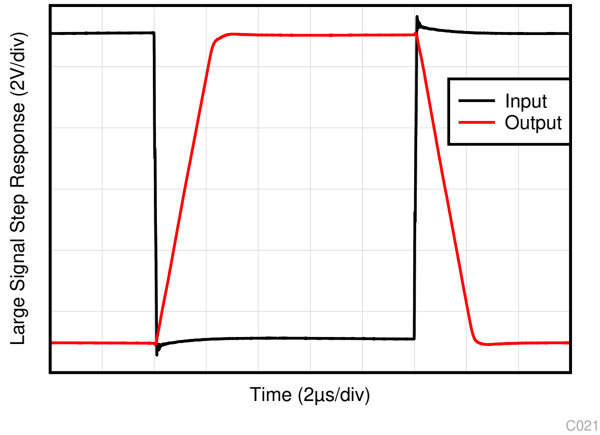


C_L = 20 pF, G = 1

図 5-36. Large-Signal Step Response (Falling)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



C_L = 20 pF, G = –1

図 5-37. Large-Signal Step Response

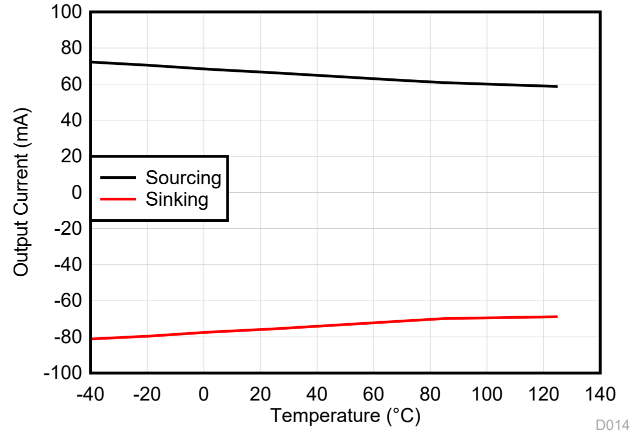


図 5-38. Short-Circuit Current vs Temperature

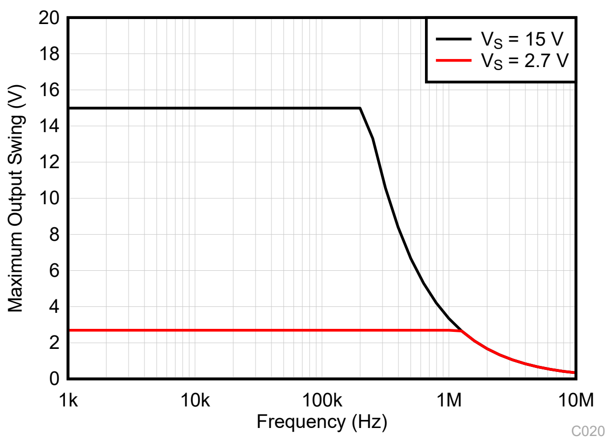


図 5-39. Maximum Output Voltage vs Frequency

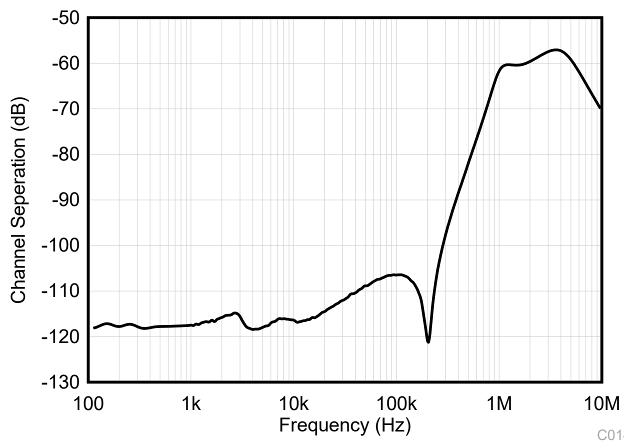


図 5-40. Channel Separation vs Frequency

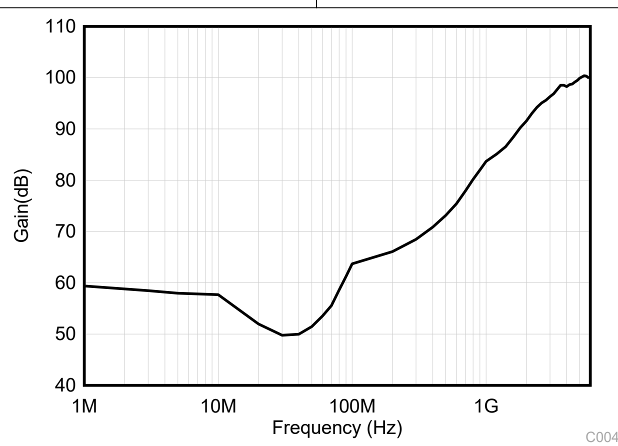


図 5-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency

6 Detailed Description

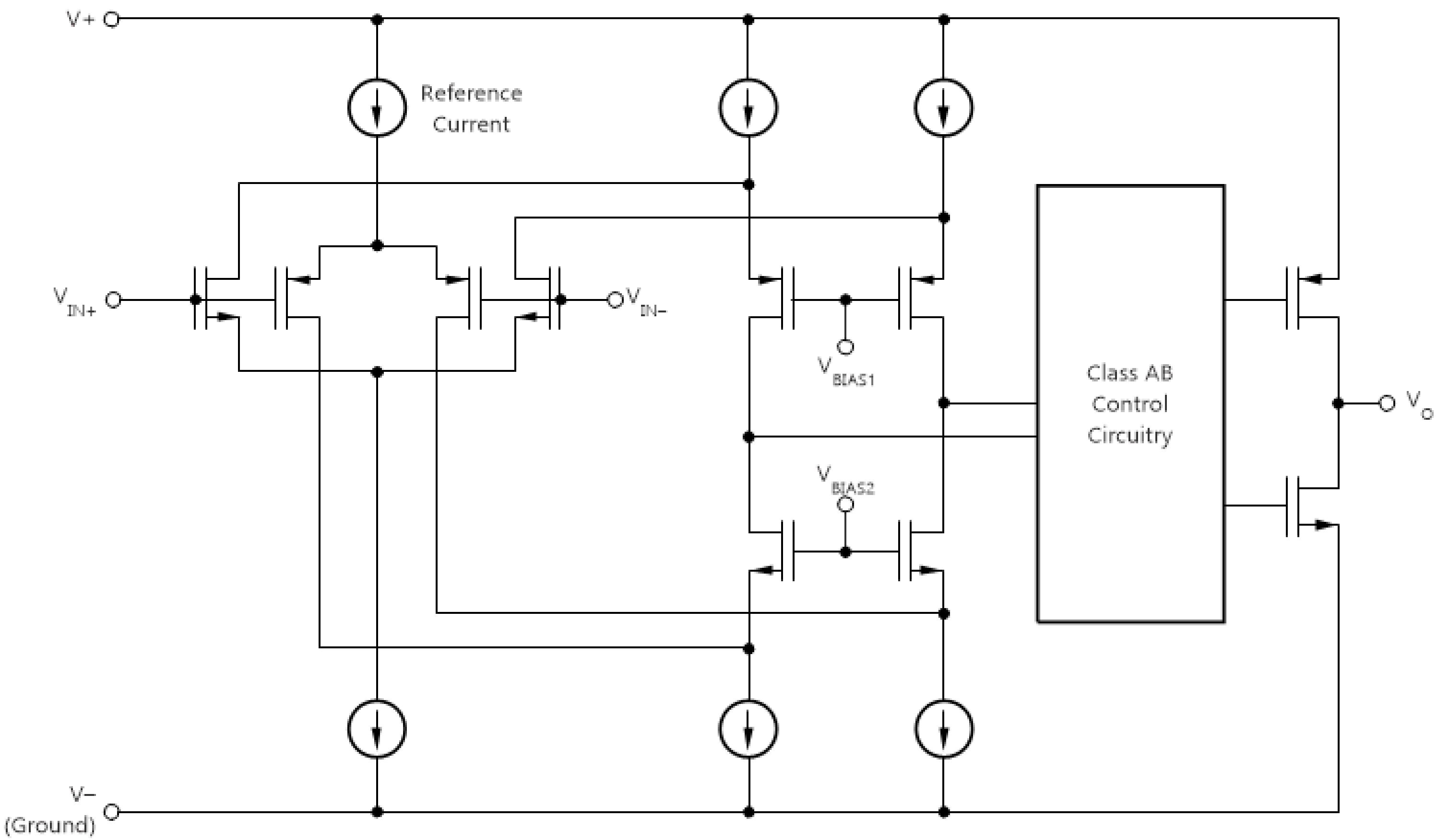
6.1 Overview

The TLV915x-Q1 family (TLV9151-Q1, TLV9152-Q1, and TLV9154-Q1) is a family of 16V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±125 µV, typical), low offset drift (±0.3 µV/°C, typical), and 4.5-MHz bandwidth.

Wide differential and common-mode input-voltage range, high output current (±75 mA), high slew rate (21 V/µs), low power operation (560 µA, typical), and shutdown functionality make the TLV915x-Q1 a robust, high-speed, high-performance operational amplifier for automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 EMI Rejection

The TLV915x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV915x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 6-1 shows the results of this testing on the TLV915x-Q1. 表 6-1 provides the EMIRR IN+ values for the TLV915x-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

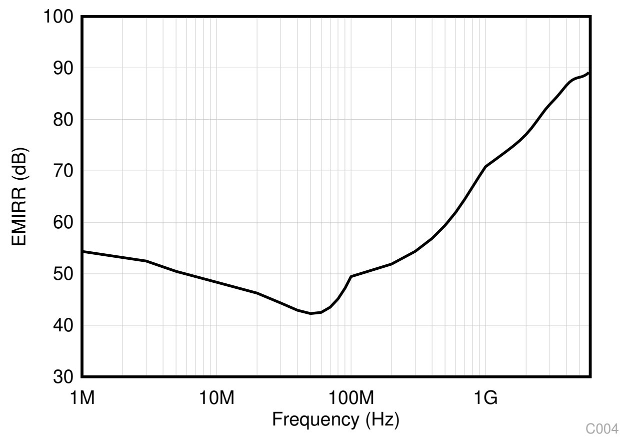


図 6-1. EMIRR Testing

表 6-1. TLV915x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

6.3.2 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV915x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV915x-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 図 6-2 shows an application example for the TLV9151-Q1 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature will reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 図 6-2 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.

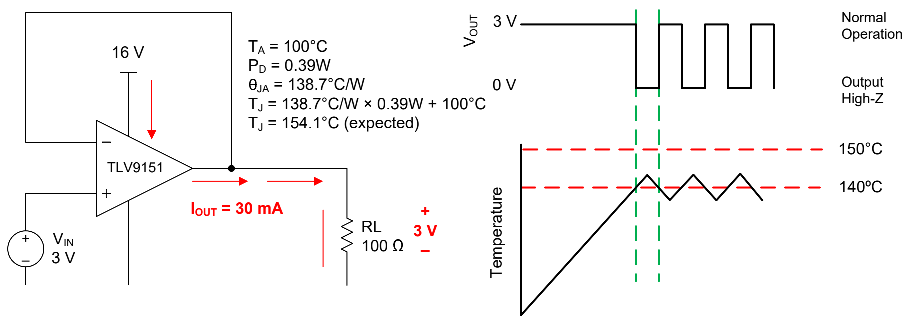


図 6-2. Thermal Protection

6.3.3 Capacitive Load and Stability

The TLV915x-Q1 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 図 6-3 and 図 6-4. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

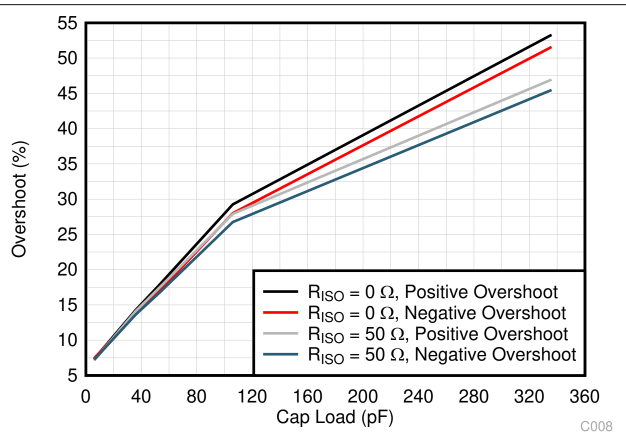


図 6-3. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)

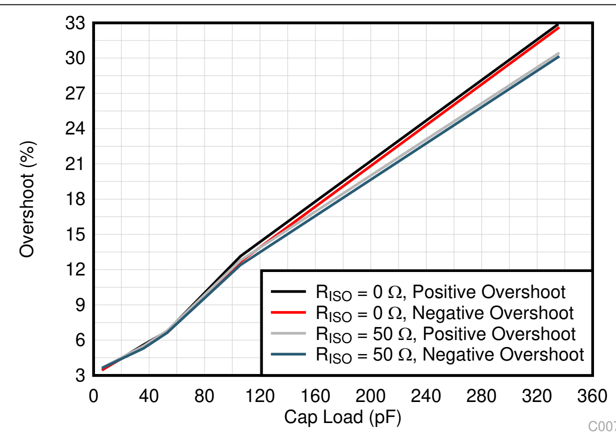


図 6-4. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 図 6-5. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. The high capacitive load drive of the TLV915x-Q1 is designed for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 図 6-5 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

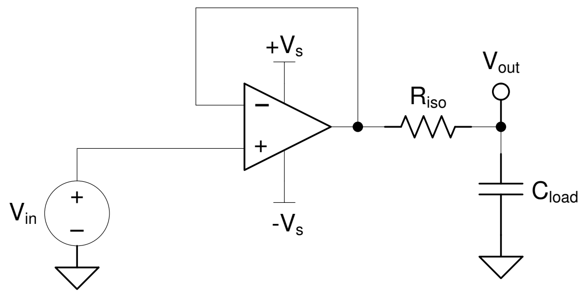


図 6-5. Extending Capacitive Load Drive With the TLV9151-Q1

6.3.4 Common-Mode Voltage Range

The TLV915x-Q1 is a 16-V, rail-to-rail input operational amplifier with an input common-mode range that extends 200 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 図 6-6. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

図 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

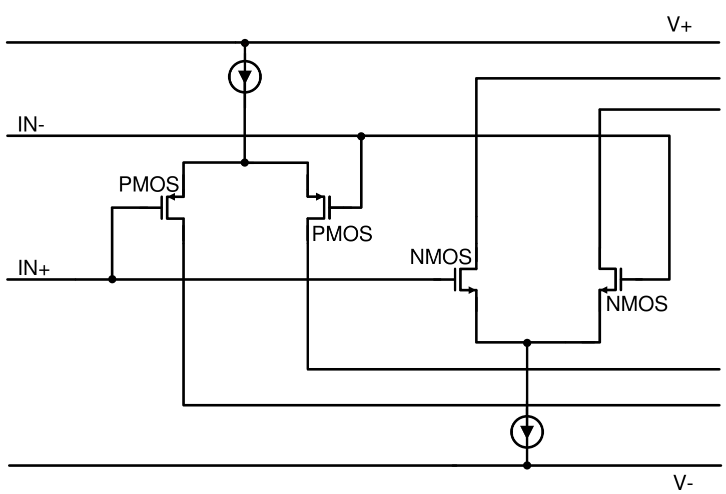


図 6-6. Rail-to-Rail Input Stage

6.3.5 Phase Reversal Protection

The TLV915x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV915x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 図 6-7. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

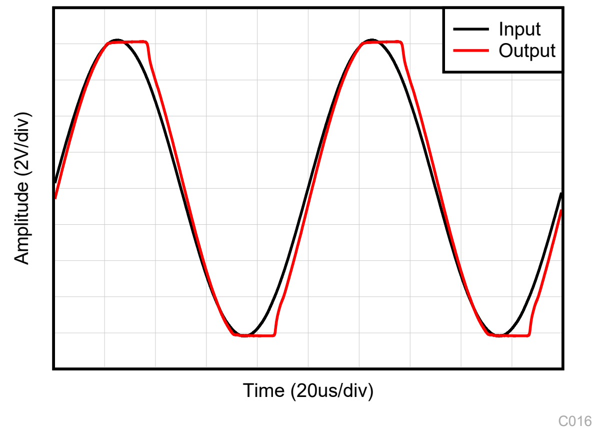


図 6-7. No Phase Reversal

6.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 図 6-8 shows an illustration of the ESD circuits contained in the TLV915x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

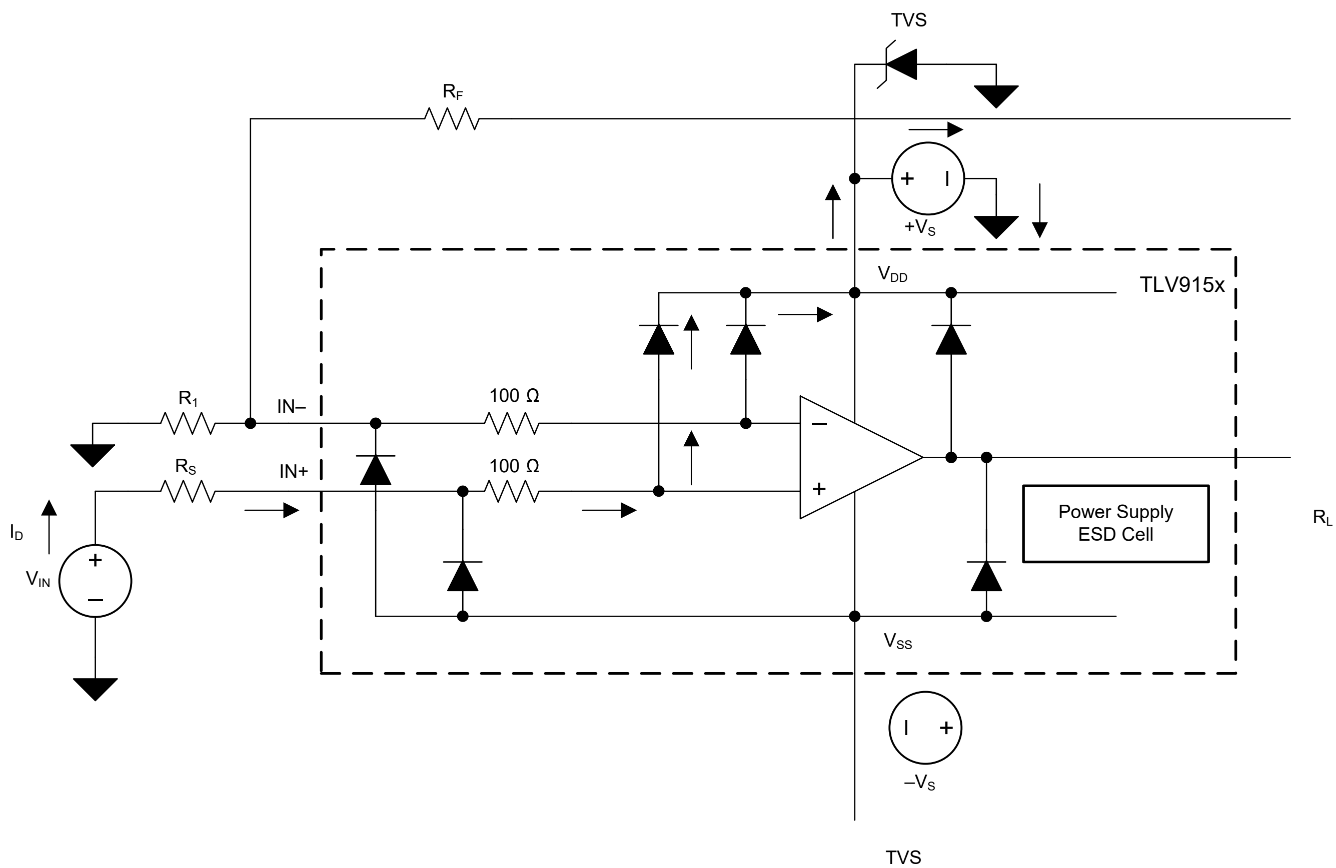


図 6-8. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.7 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV915x-Q1 is approximately 400 ns.

6.3.8 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in セクション 5.7.

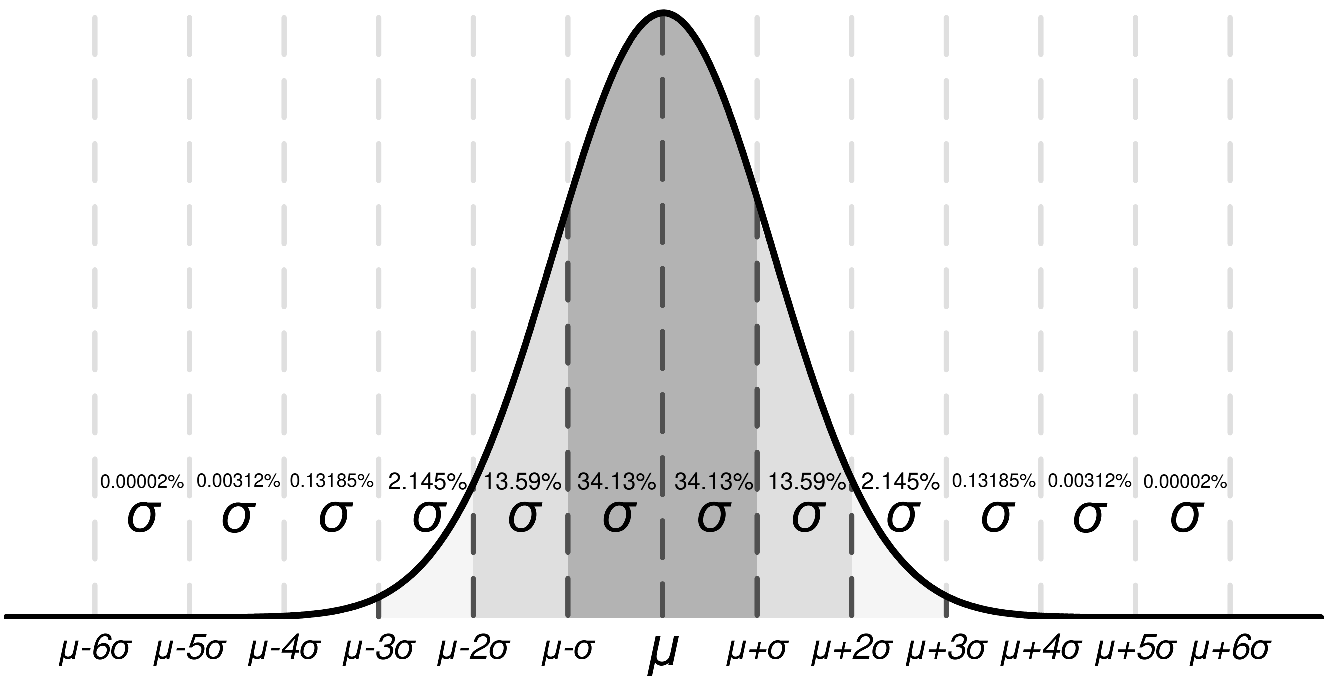


図 6-9. Ideal Gaussian Distribution

図 6-9 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of セクション 5.7 are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

This chart can be used to calculate approximate probability of a specification in a unit; for example, for TLV915x-Q1, the typical input voltage offset is 125 µV, so 68.2% of all TLV915x-Q1 devices are expected to have an offset from –125 µV to 125 µV. At 4 σ (±500 µV), 99.9937% of the distribution has an offset voltage less than ±500 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV915x-Q1 family has a maximum offset voltage of 675 µV at 25°C, and even though this corresponds to about 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 895 µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV915x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on 図 5-2 and the typical value of 0.3 µV/°C in セクション 5.7, it can be calculated that the 6-σ value for offset voltage drift is about 1.8 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.3.9 Shutdown

The TLV915xS-Q1 devices feature one or more shutdown pins (SHDN) that disable the op amp, placing the amplifier into a low-power standby mode. In this mode, the op amp typically consumes about 30 µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to provide smooth switching characteristics. For proper shutdown behavior, the SHDN pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V+. The shutdown pin circuitry includes a pulldown resistor, which inherently pulls the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins must either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V+. Exceeding this voltage level can damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 8 µs; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV915xS-Q1 family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To keep shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV915xS-Q1 without a load, the resulting turnoff time significantly increases.

6.4 Device Functional Modes

The TLV915x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the TLV915x-Q1 is 16 V (±8 V).

The TLV915xS-Q1 devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See セクション 6.3.9 for more information.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TLV915x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 16-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the TLV915x-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

図 7-1 shows the TLV9151-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 図 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.

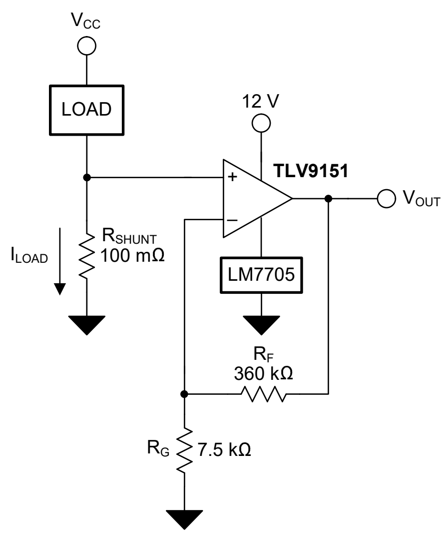


図 7-1. TLV9151-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 図 7-1 is given in 式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\,mV}{1\,A} = 100\,m\Omega \tag{2}$$

Using 式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV9151-Q1 to produce an output voltage of 0 V to 4.9 V. The gain needed by the TLV9151-Q1 to produce the necessary output voltage is calculated using 式 3.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using 式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 式 4 is used to size the resistors, R_F and R_G, to set the gain of the TLV9151-Q1 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. 図 7-2 shows the measured transfer function of the circuit shown in 図 7-1.

7.2.1.3 Application Curves

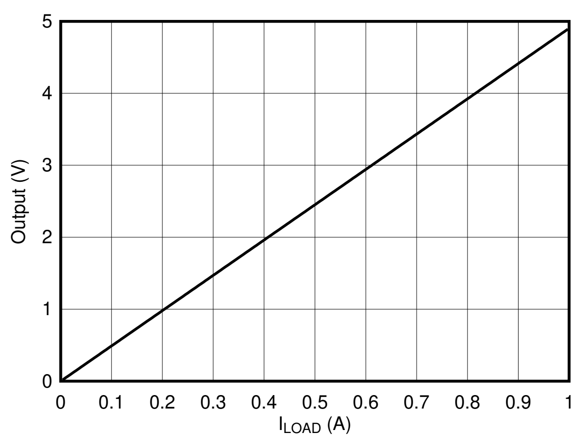


図 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV915x-Q1 is specified for operation from 2.7 V to 16 V (±1.35 V to ±8 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in セクション 5.8.

注意

Supply voltages larger than 16 V can permanently damage the device; see セクション 5.1.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to セクション 7.4.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 図 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

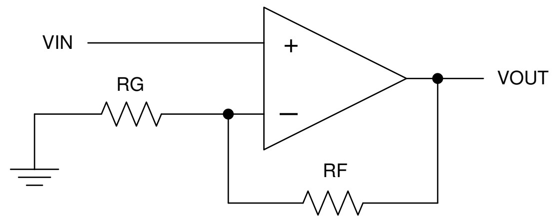


図 7-3. Schematic Representation

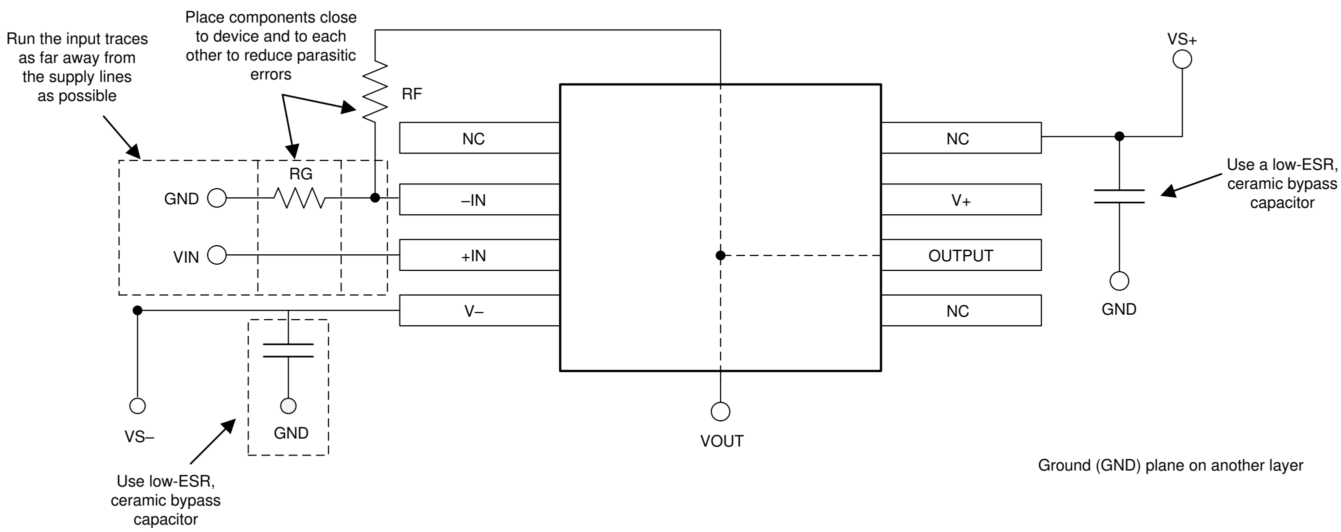


図 7-4. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.1.1.2 TI Precision Designs

The TLV915x-Q1 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* e-book
- Texas Instruments, *AN31 amplifier circuit collection* application note
- Texas Instruments, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution* TI Precision Design
- Texas Instruments, *The EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* analog design journal

8.3 ドキュメントの更新通知を受け取る方法

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8.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (June 2023) to Revision G (March 2024) — **Page**

- データシート全体に 6 ピン SOT-23 (DBV) および 5 ピン SC70 (DCK) パッケージを追加 ... 1
- Added HBM ESD rating for TLV9151SQDBVRQ1 ... 6
- Added the Shutdown performance section to Electrical Characteristic table ... 8
- Added *Shutdown* section to the *Feature Description* ... 25

Changes from Revision E (March 2022) to Revision F (June 2023) — **Page**

- (TSSOP、14) パッケージのステータスをプレビューからアクティブに変更 ... 1

Changes from Revision D (September 2021) to Revision E (March 2022) — **Page**

- Changed maximum PSRR (2.7 V to 16 V) from ±8µV/V to ±10.6µV/V ... 8
- Changed minimum CMRR (at 16 V) from 100 dB to 99 dB ... 8

Changes from Revision C (May 2021) to Revision D (September 2021) — **Page**

- 「製品情報」表の SOIC (14) パッケージからプレビューの注を削除 ... 1
- 「製品情報」表の SOT-23 (14) パッケージからプレビューの注を削除 ... 1
- 「製品情報」表の SOIC (8) パッケージからプレビューの注を削除 ... 1
- 「製品情報」表の SOT-23 (5) パッケージからプレビューの注を削除 ... 1
- Deleted preview note from SOT-23 (14) Package, in *Pin Configuration and Functions* section ... 3
- Deleted preview note from SOIC (14) Package, in *Pin Configuration and Functions* section ... 3
- Deleted preview note from SOIC (8) Package, in *Pin Configuration and Functions* section ... 3
- Deleted preview note from SOT-23 (5) Package, in *Pin Configuration and Functions* section ... 3

Changes from Revision B (March 2021) to Revision C (May 2021) — **Page**

- 「製品情報」表の TSSOP (14) パッケージからプレビューの注を削除 ... 1
- Deleted preview note from TSSOP (14) Package, in *Pin Configuration and Functions* section ... 3

Changes from Revision A (January 2021) to Revision B (March 2021) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9151QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JKF
TLV9151QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JKF
TLV9151QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MT
TLV9151QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MT
TLV9151SQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3BIH
TLV9151SQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3BIH
TLV9152QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27XT
TLV9152QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27XT
TLV9152QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9152Q
TLV9152QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9152Q
TLV9152QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9152
TLV9152QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9152
TLV9154QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9154QD
TLV9154QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9154QD
TLV9154QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9154Q
TLV9154QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9154Q
TLV9154QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9154Q
TLV9154QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9154Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9151-Q1, TLV9152-Q1, TLV9154-Q1 :

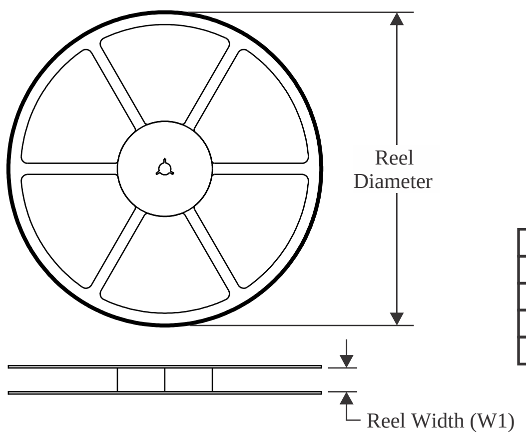
- Catalog : TLV9151, TLV9152, TLV9154

NOTE: Qualified Version Definitions:

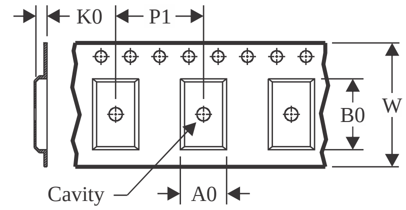
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

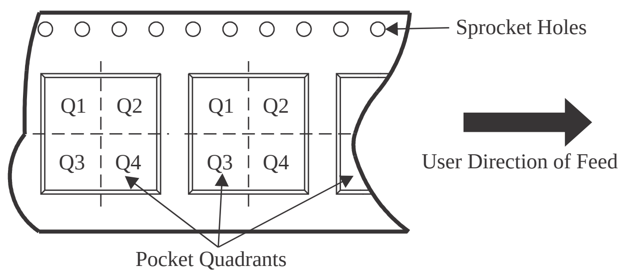


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

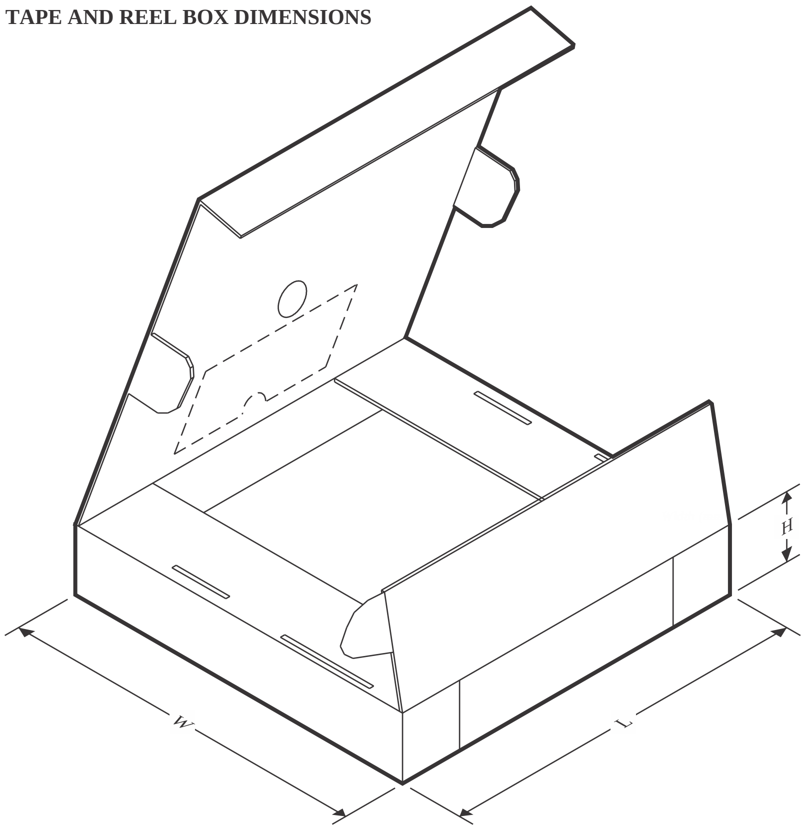
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

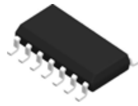
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9151QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9151SQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9152QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV9152QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9152QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9154QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9154QDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9154QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9151QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9151QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV9151SQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9152QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9152QDRQ1	SOIC	D	8	3000	356.0	356.0	35.0
TLV9152QPWRQ1	TSSOP	PW	8	3000	356.0	356.0	35.0
TLV9154QDRQ1	SOIC	D	14	3000	356.0	356.0	35.0
TLV9154QDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9154QPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0

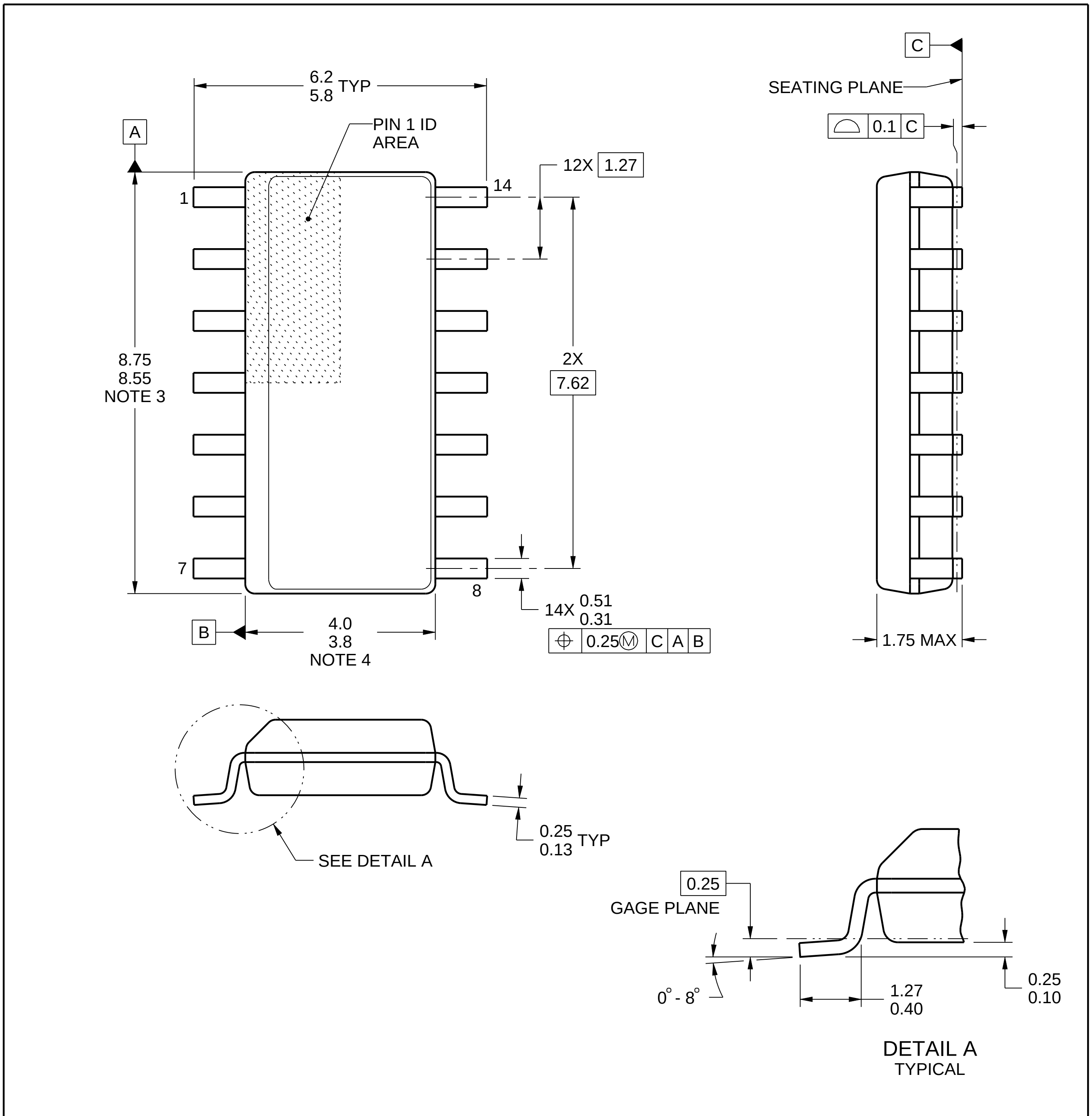


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

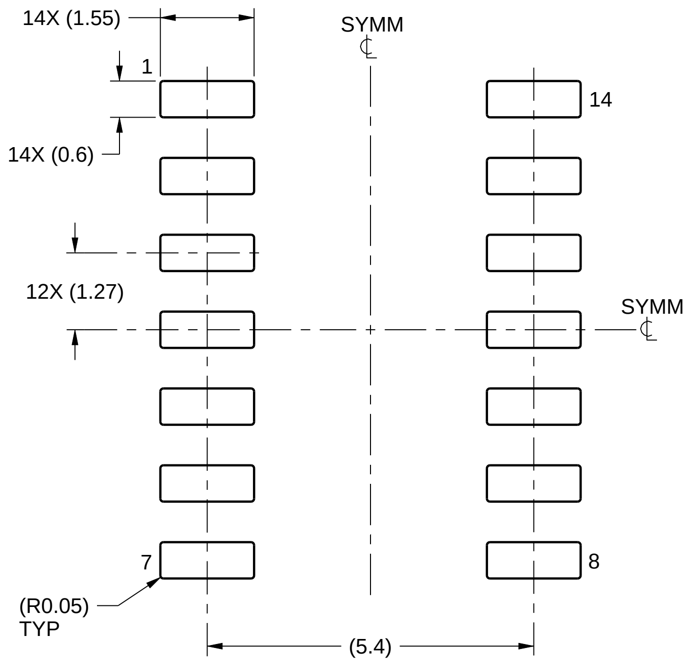
SMALL OUTLINE INTEGRATED CIRCUIT



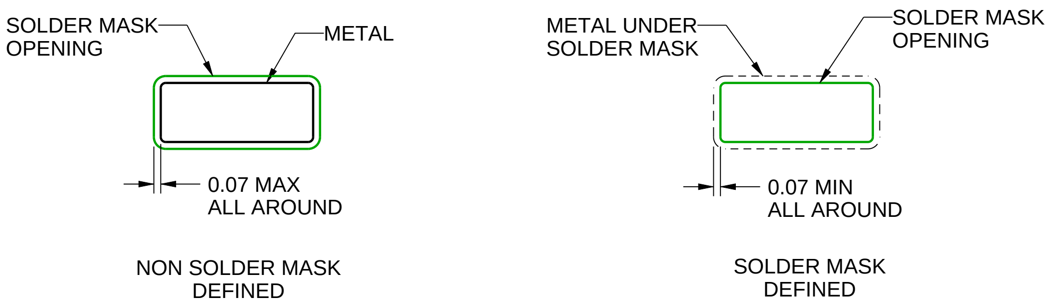
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

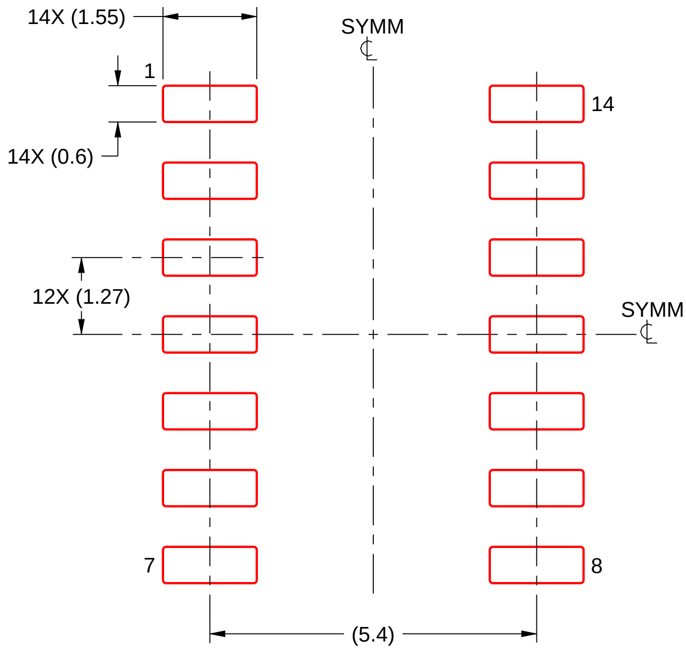


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

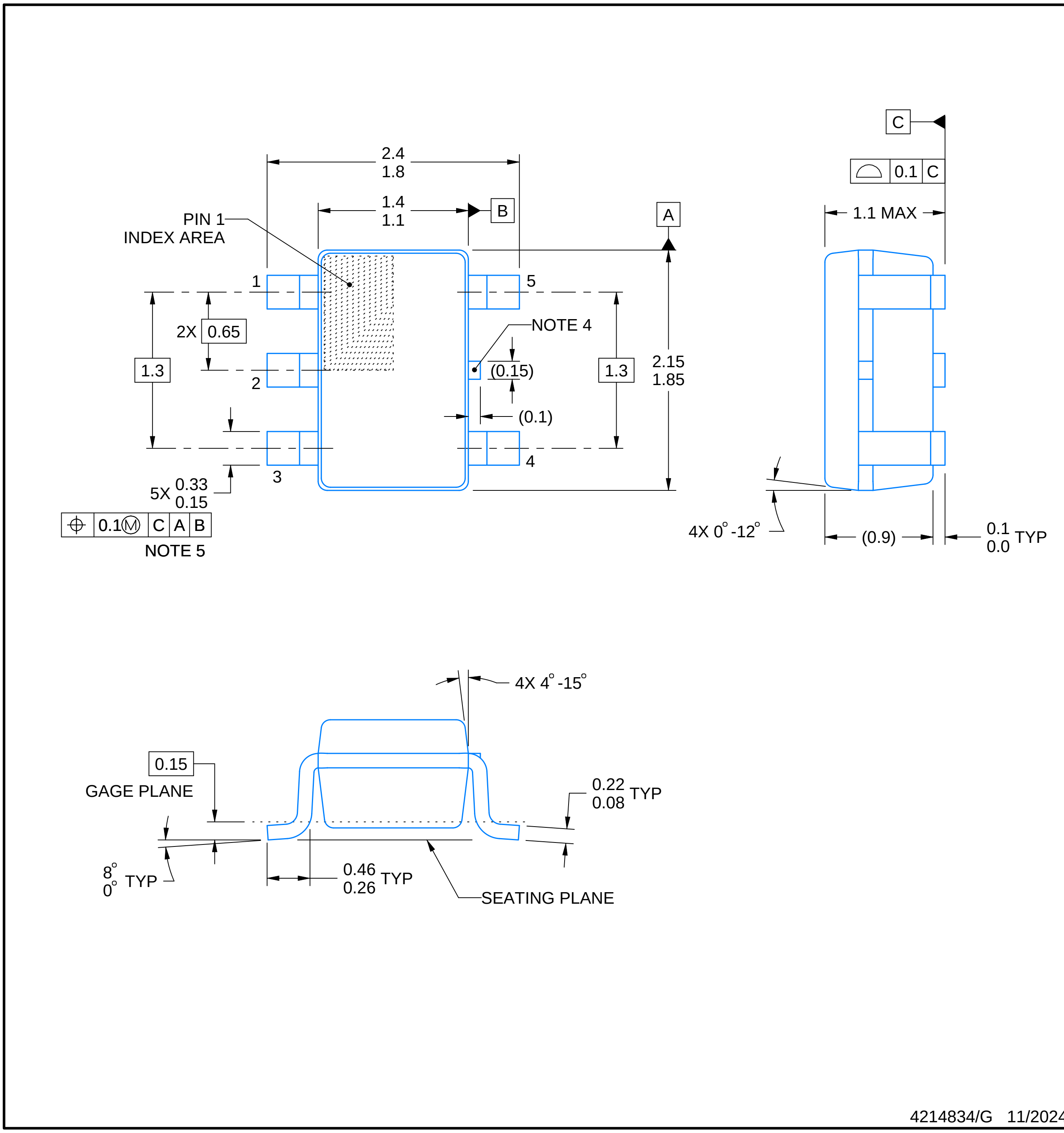
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

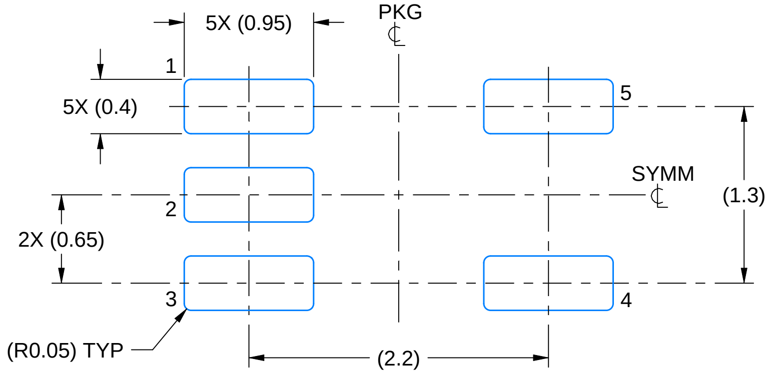
SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

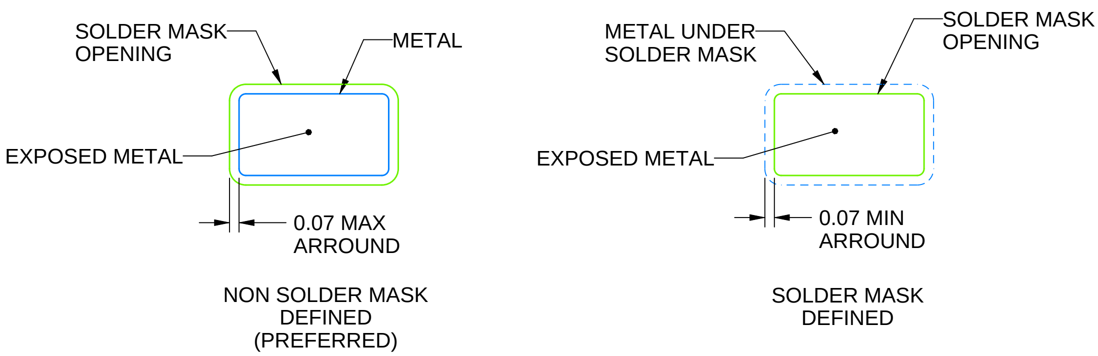


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

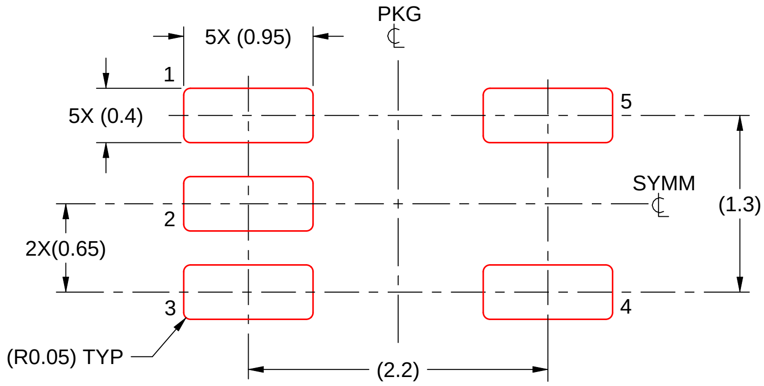


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

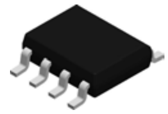


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

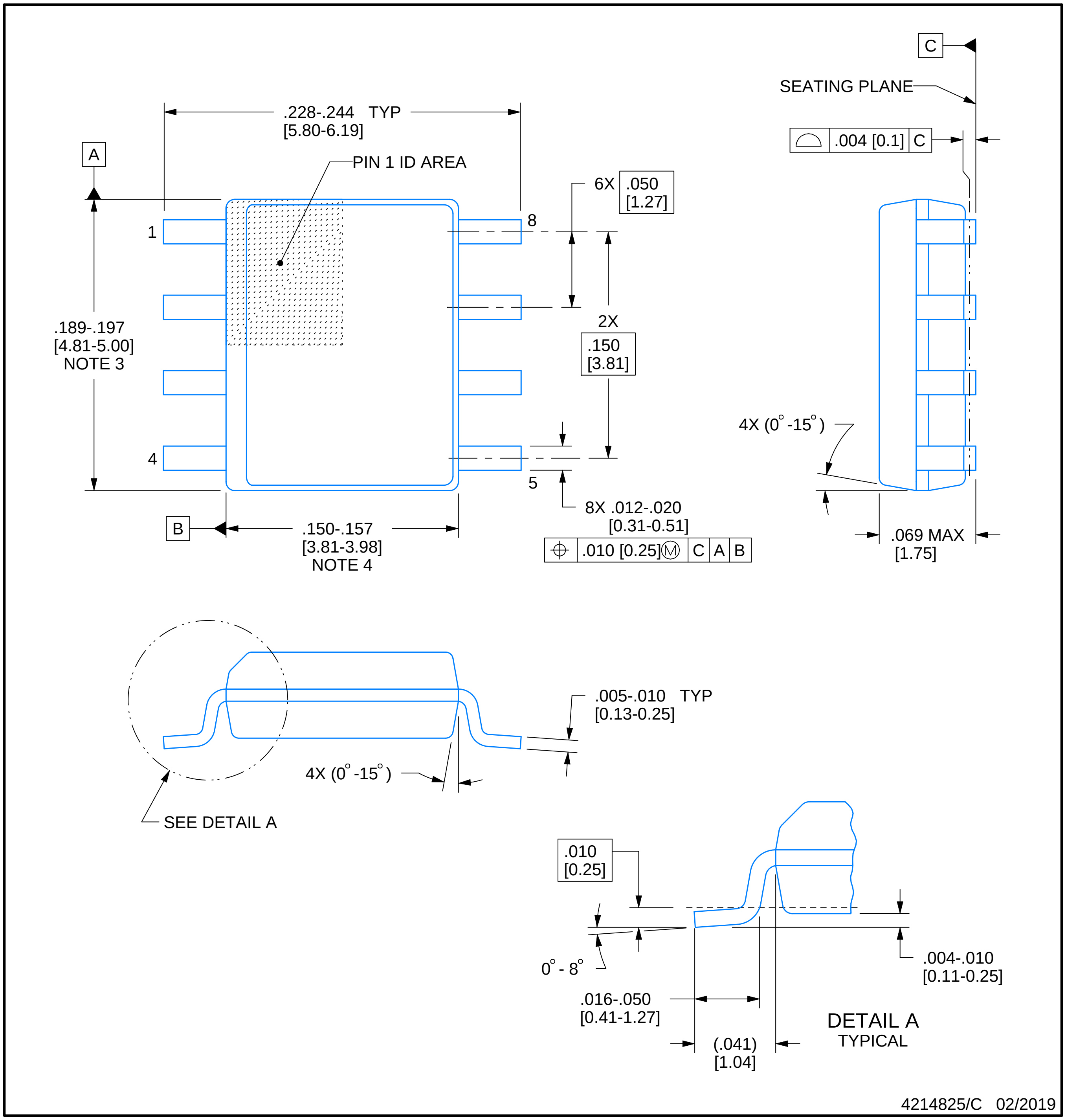
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

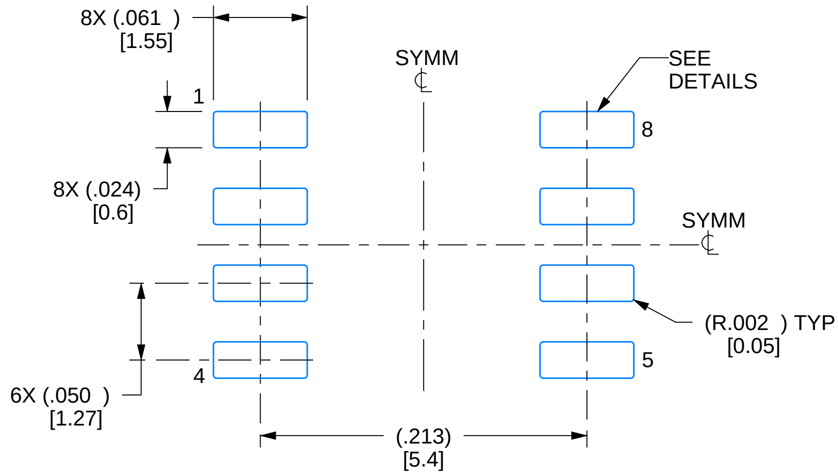
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

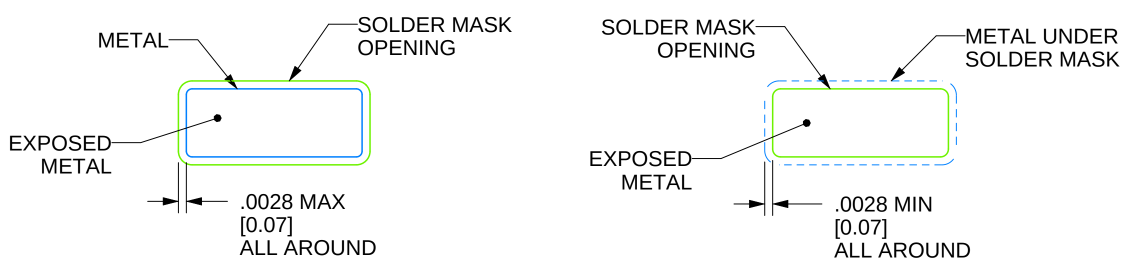


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

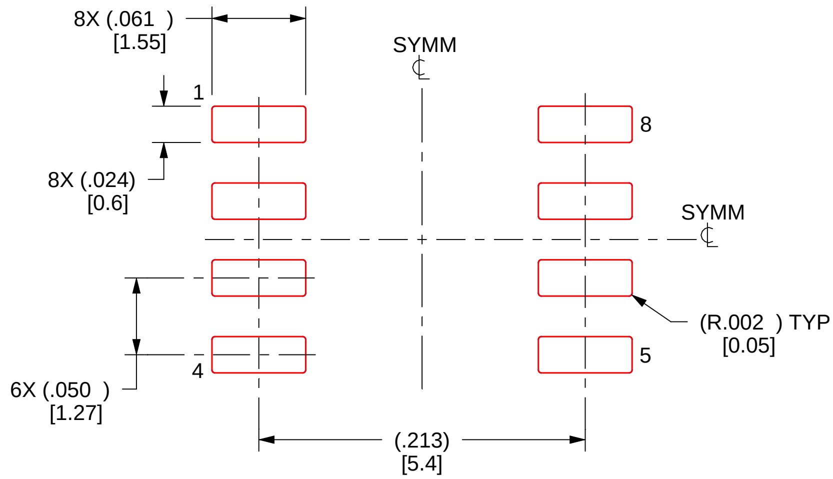
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

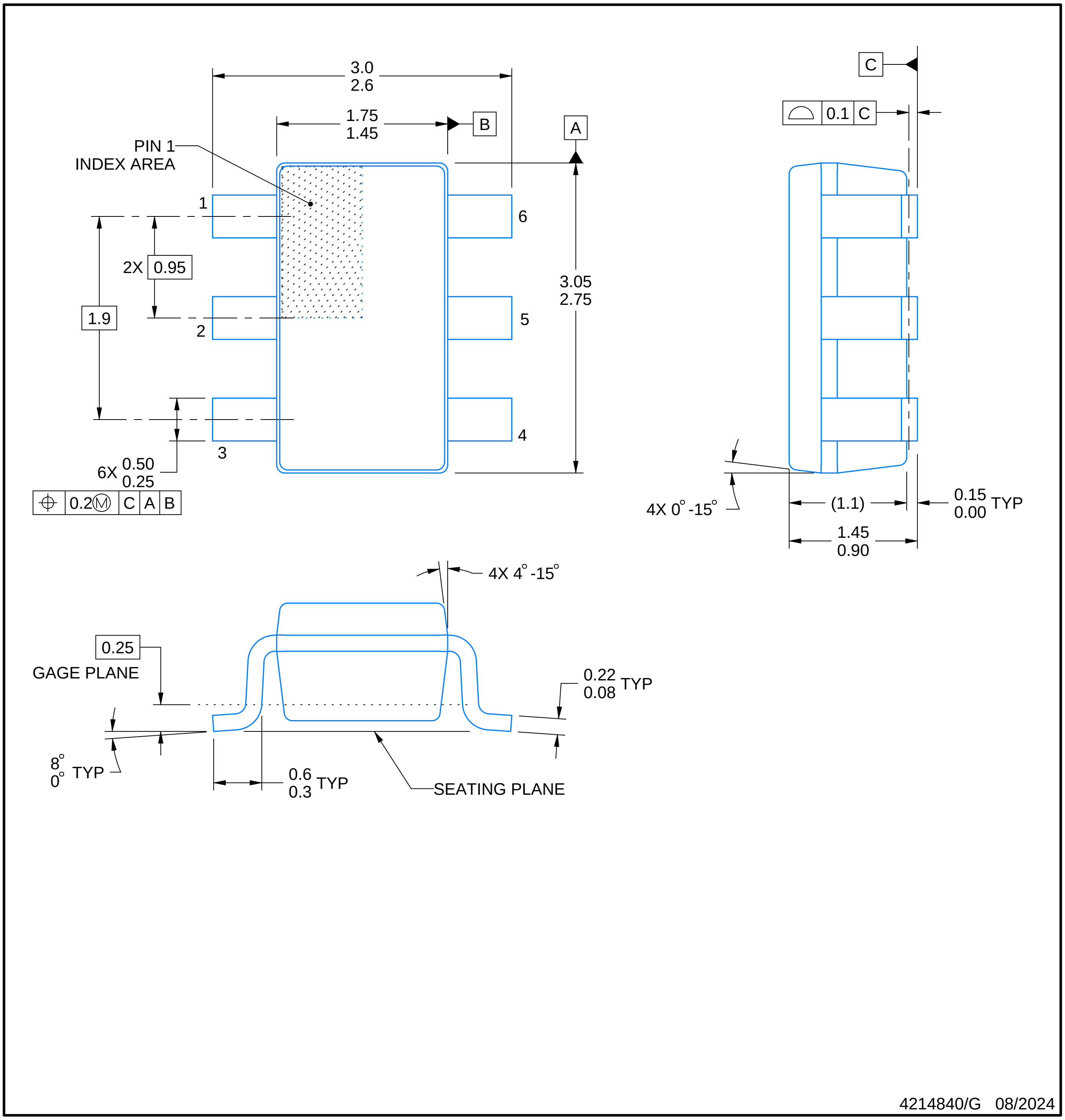


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

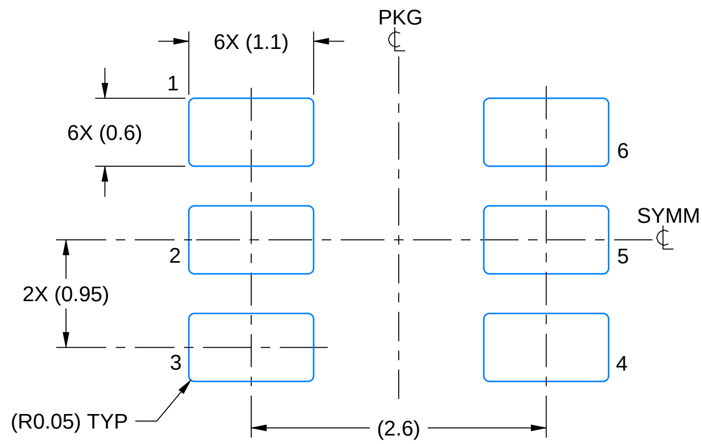
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

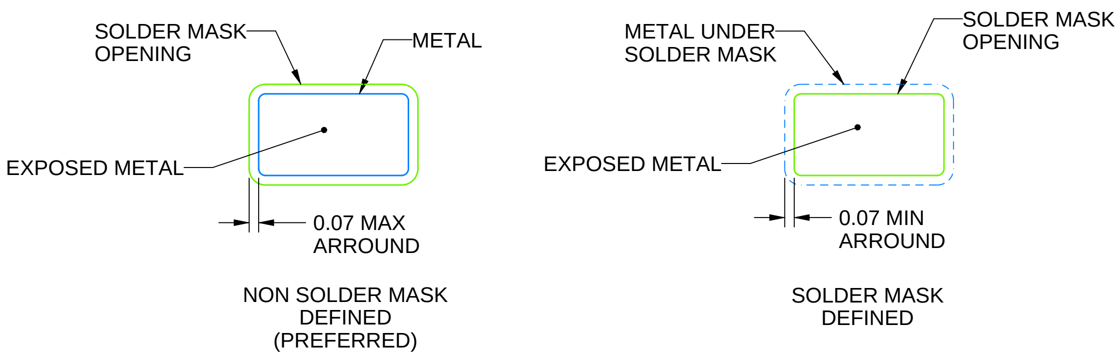


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

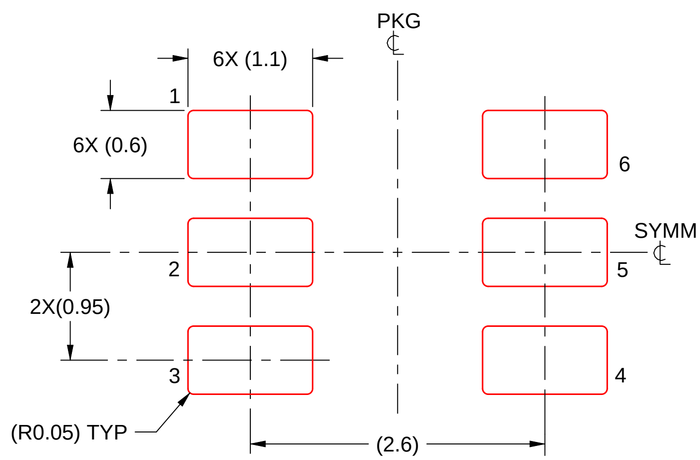


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

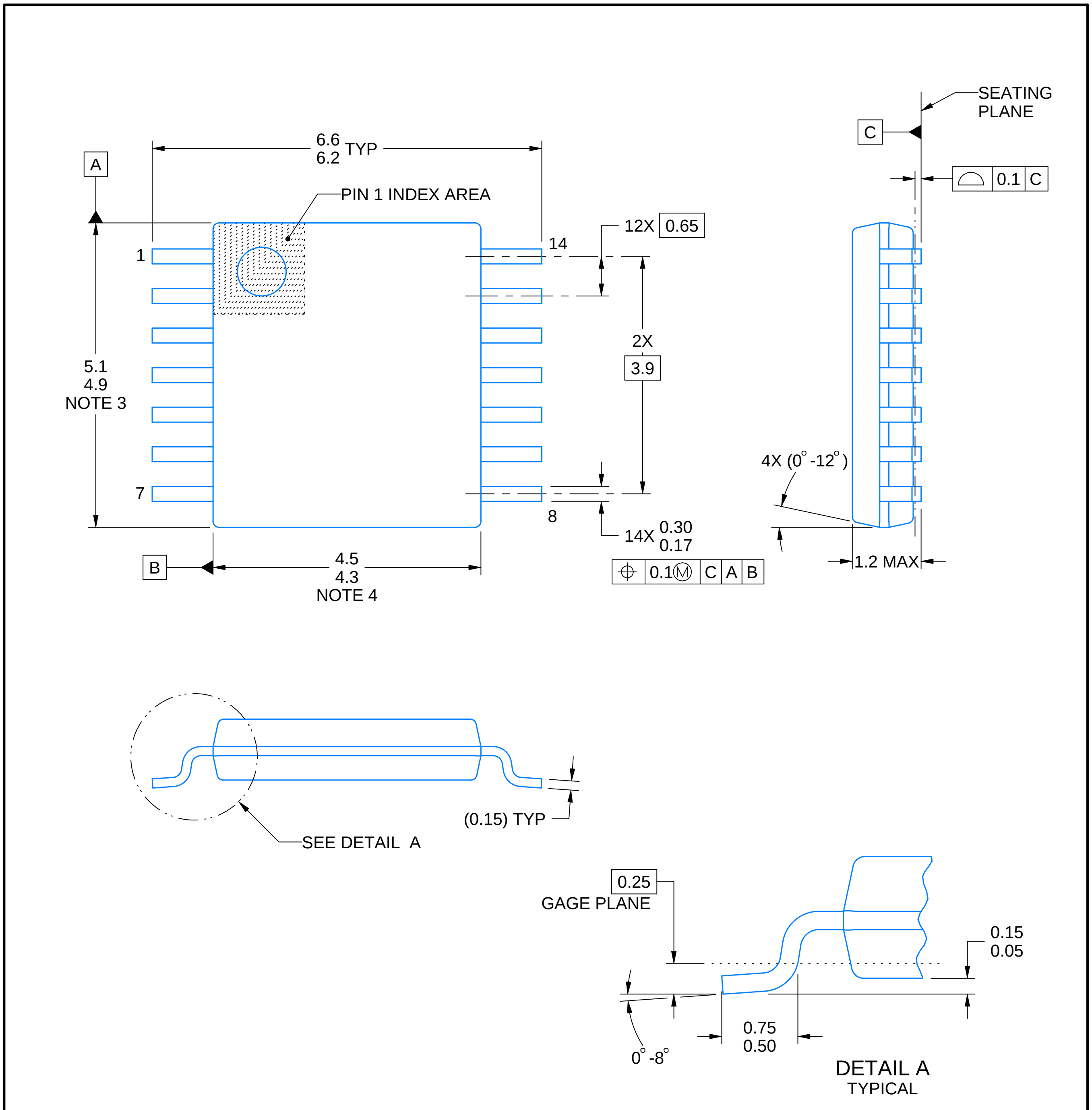


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

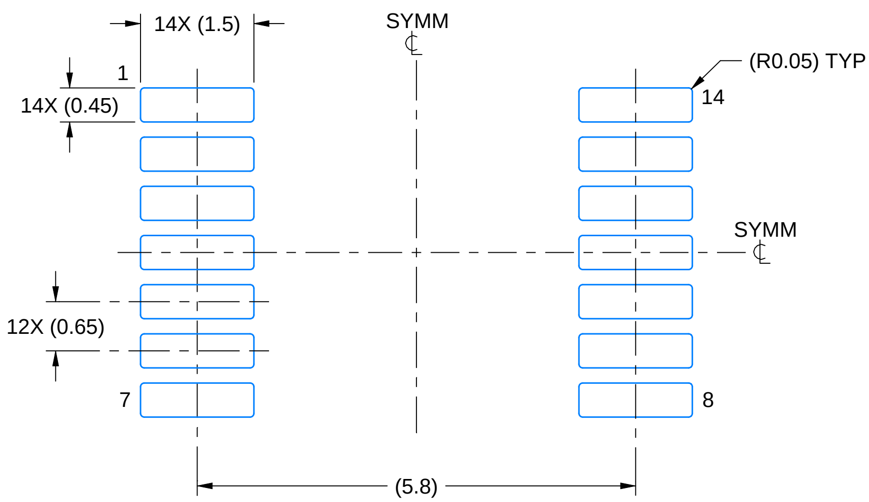
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



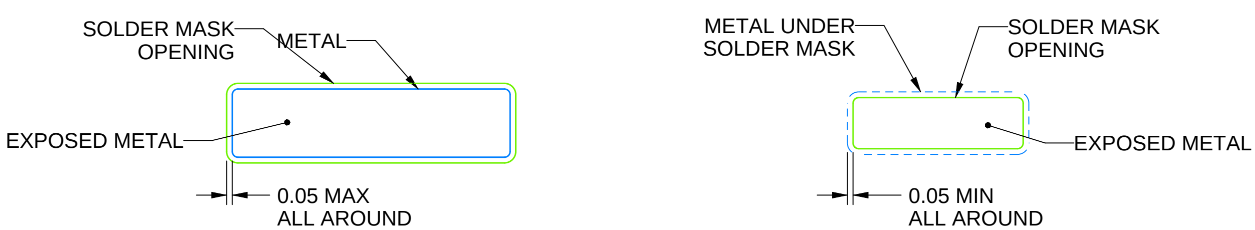
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

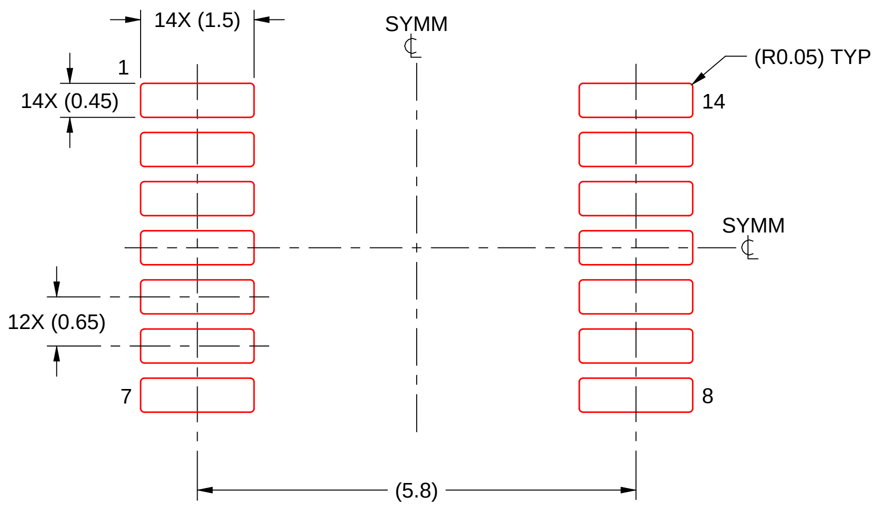


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

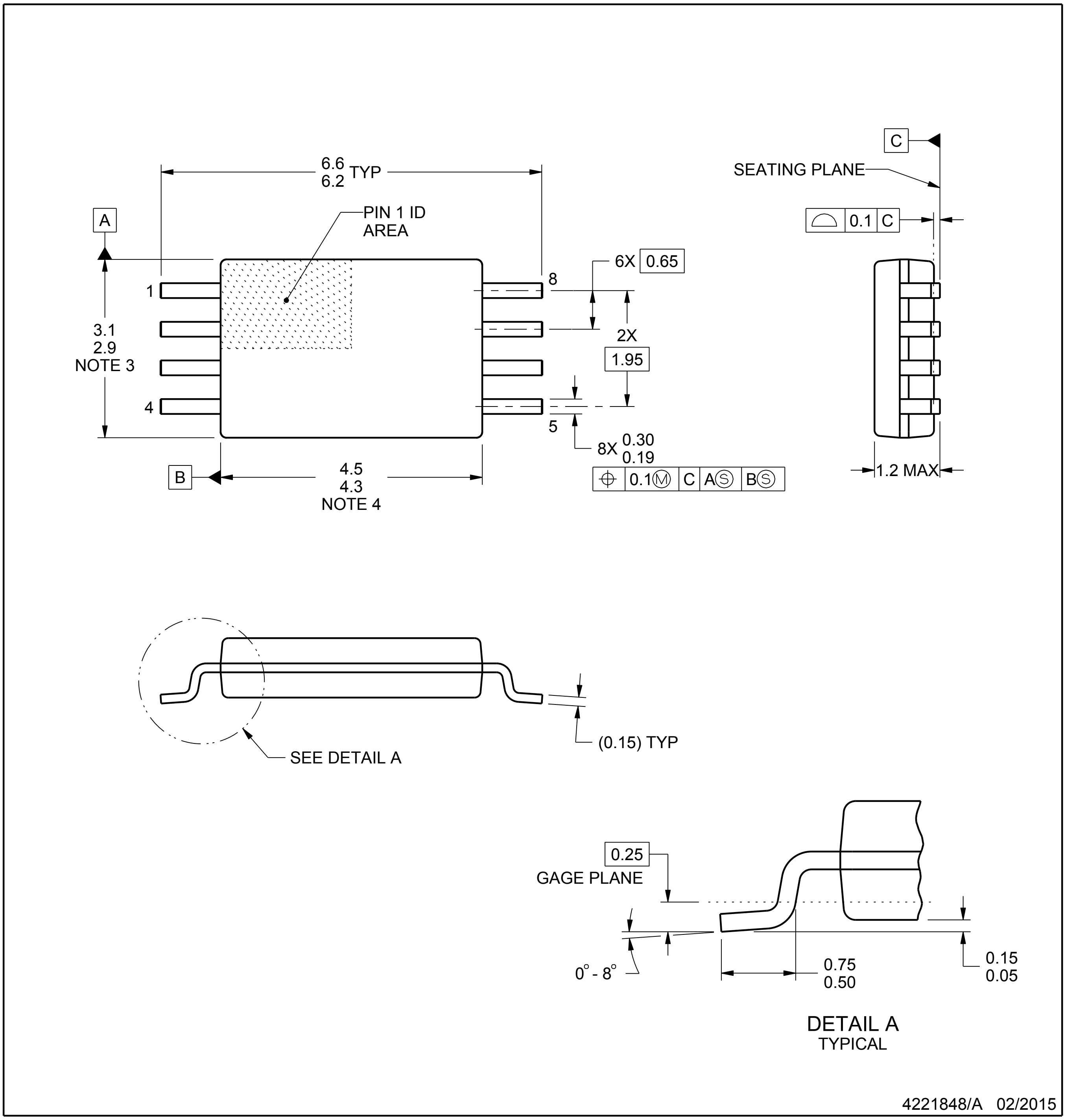


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

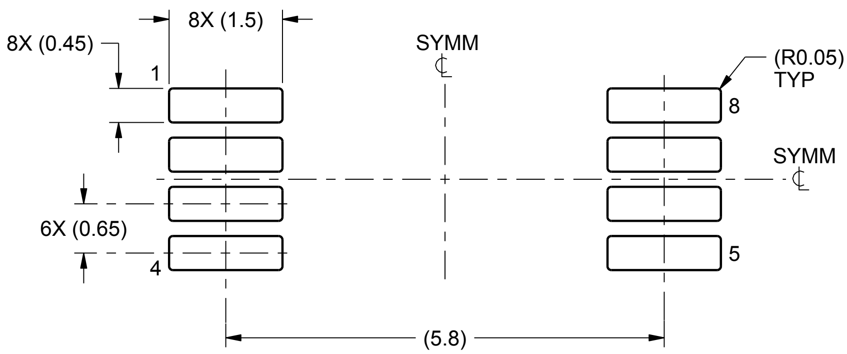
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

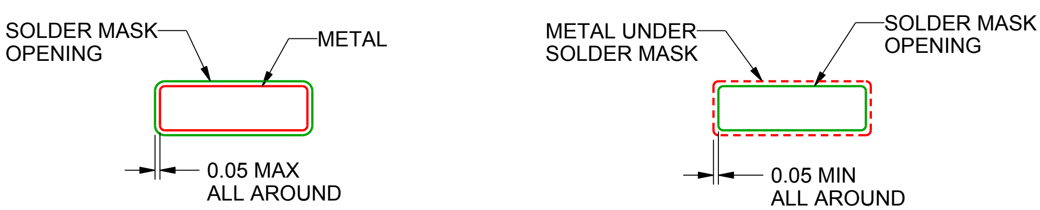


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

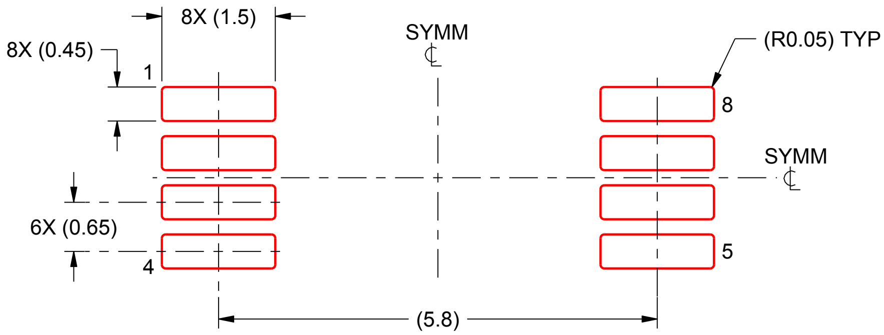
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

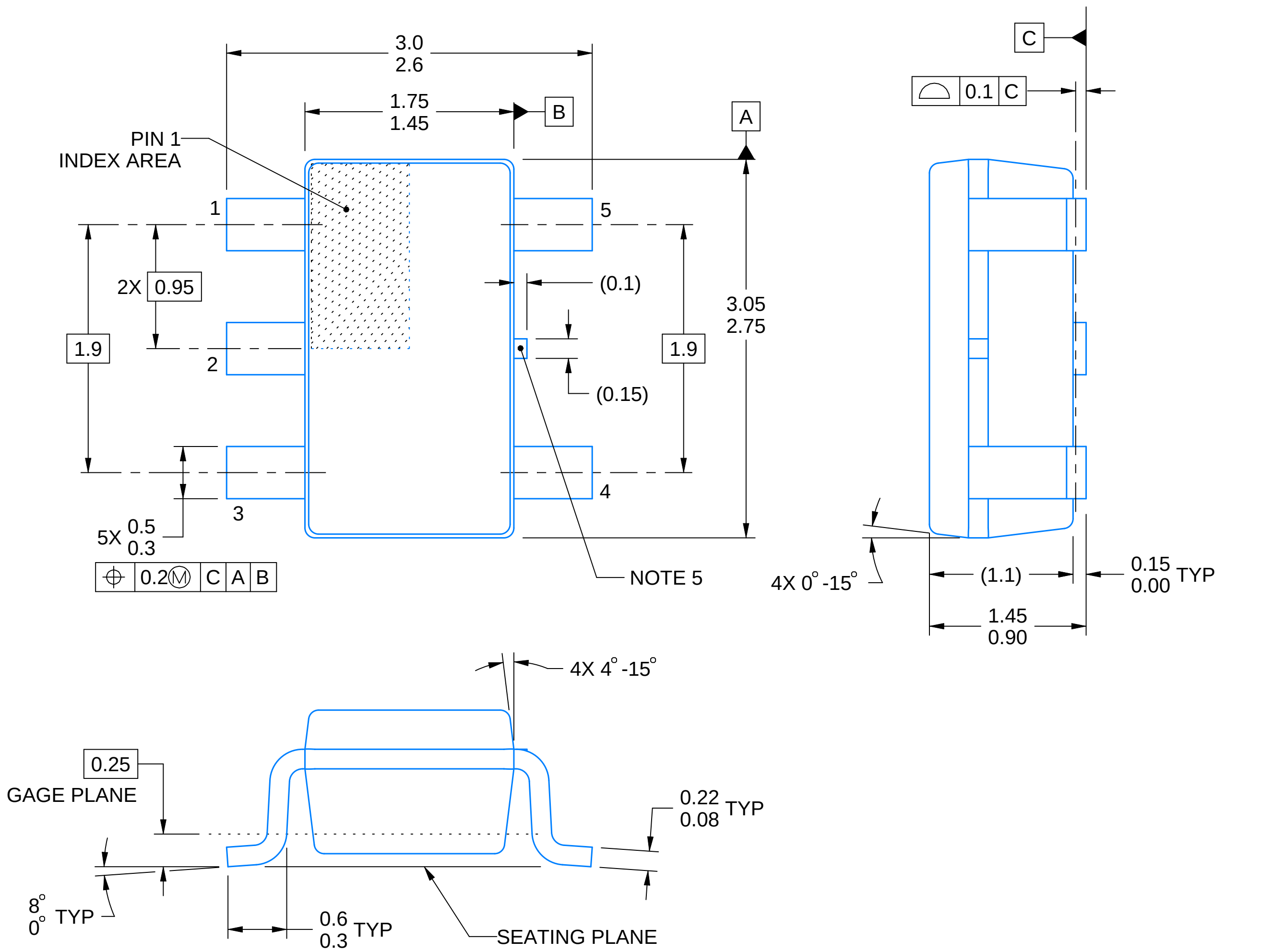


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

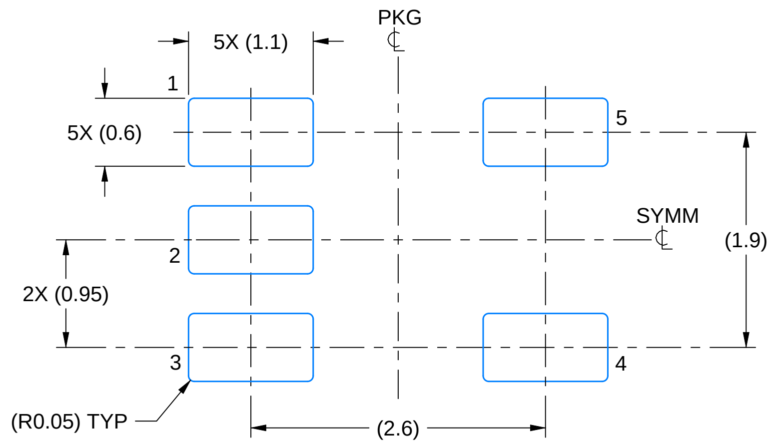
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



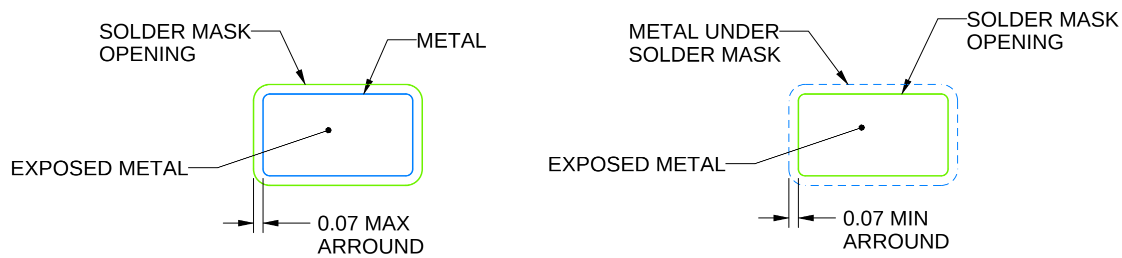
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

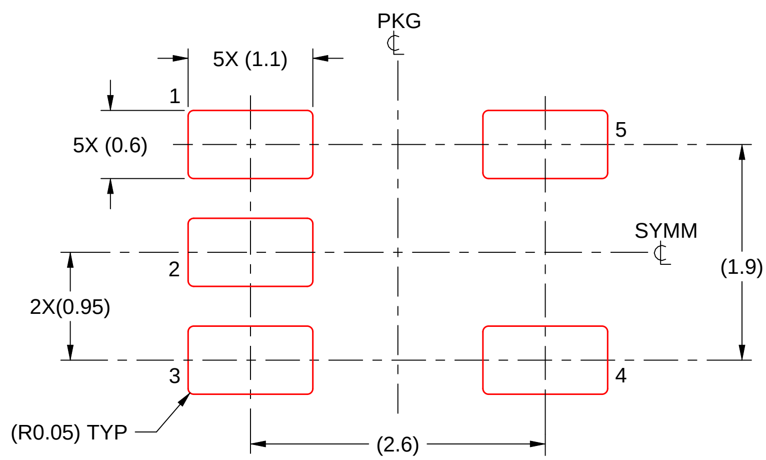
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

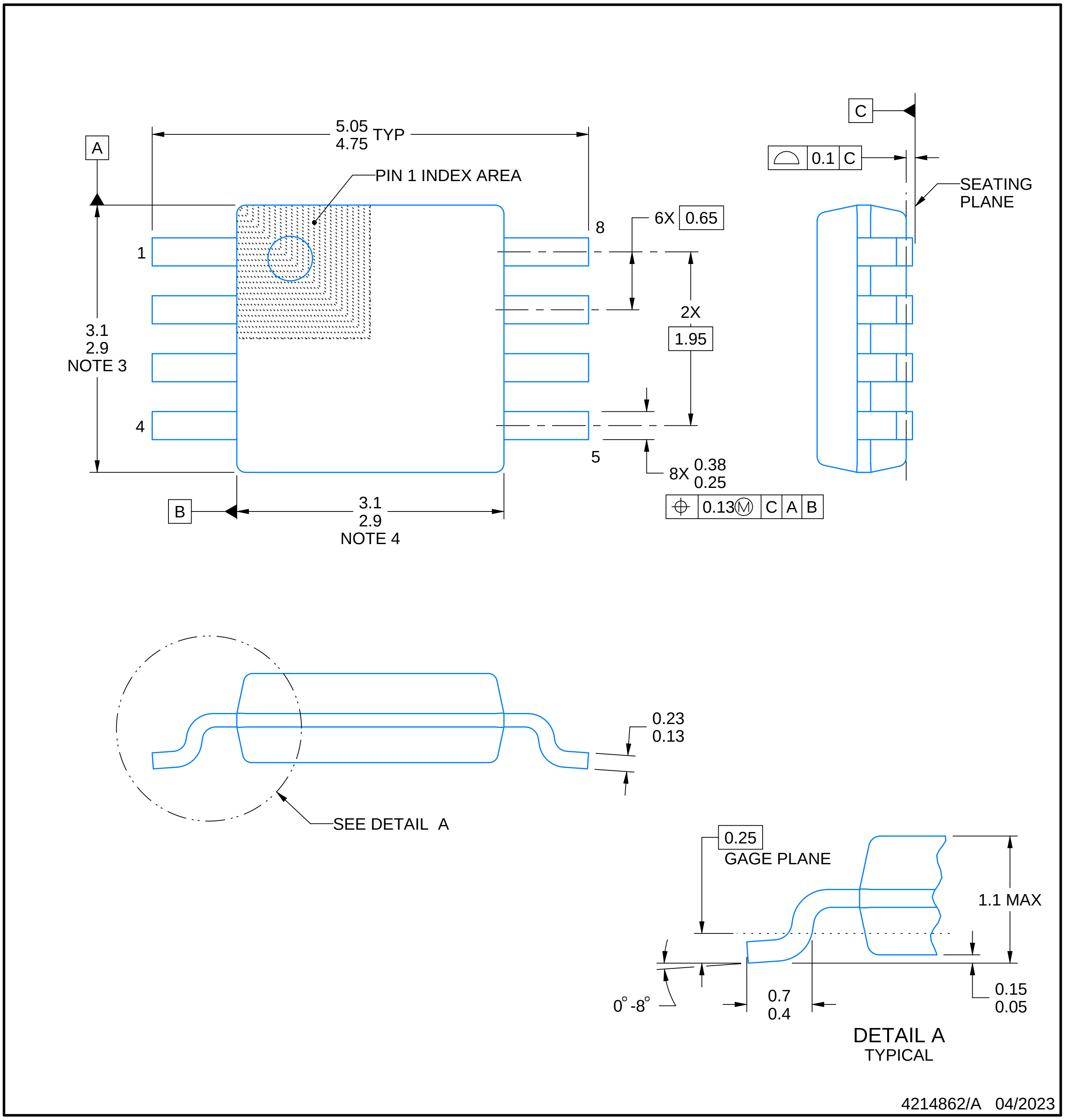


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

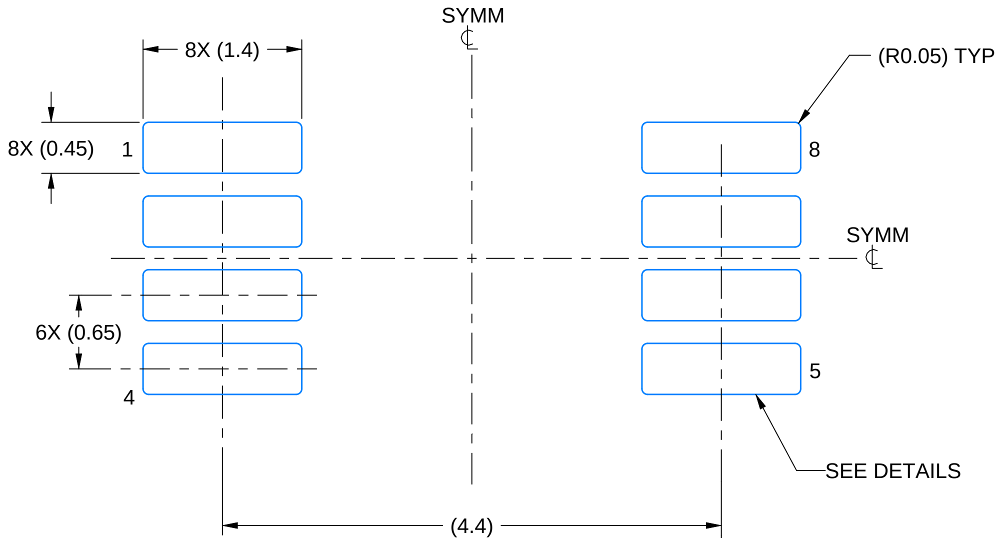


4214862/A 04/2023

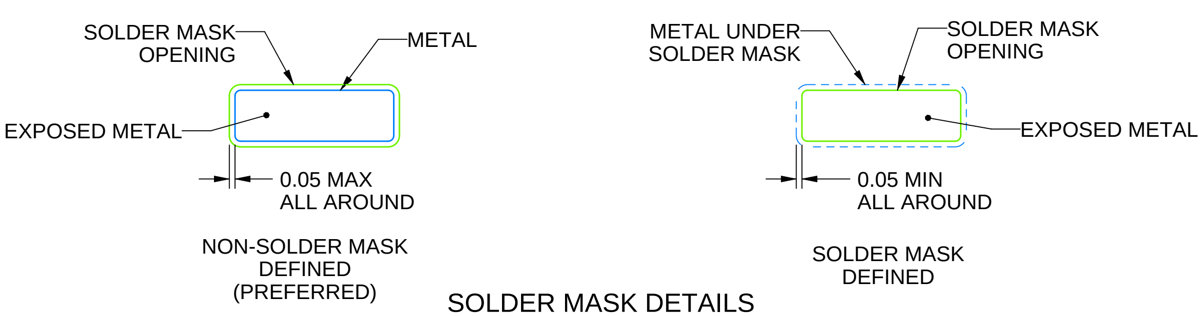
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

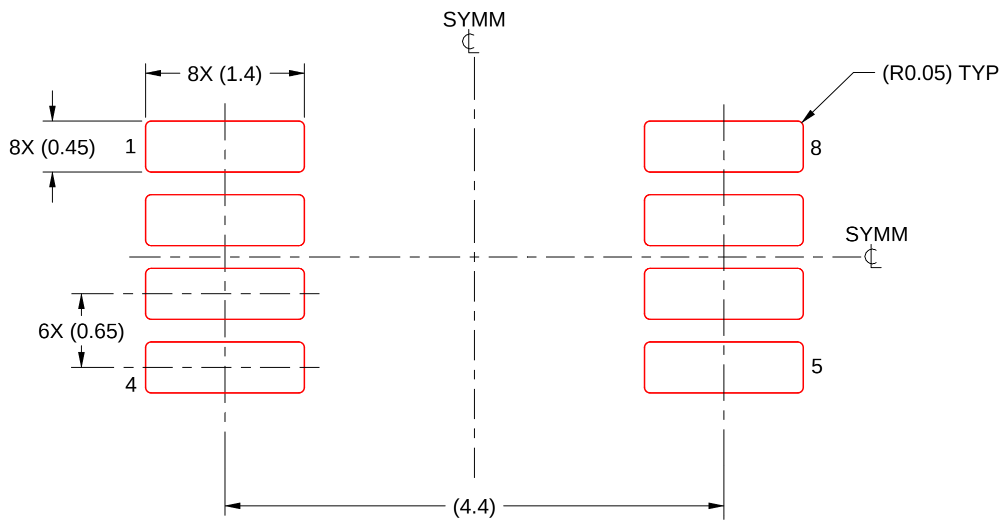


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

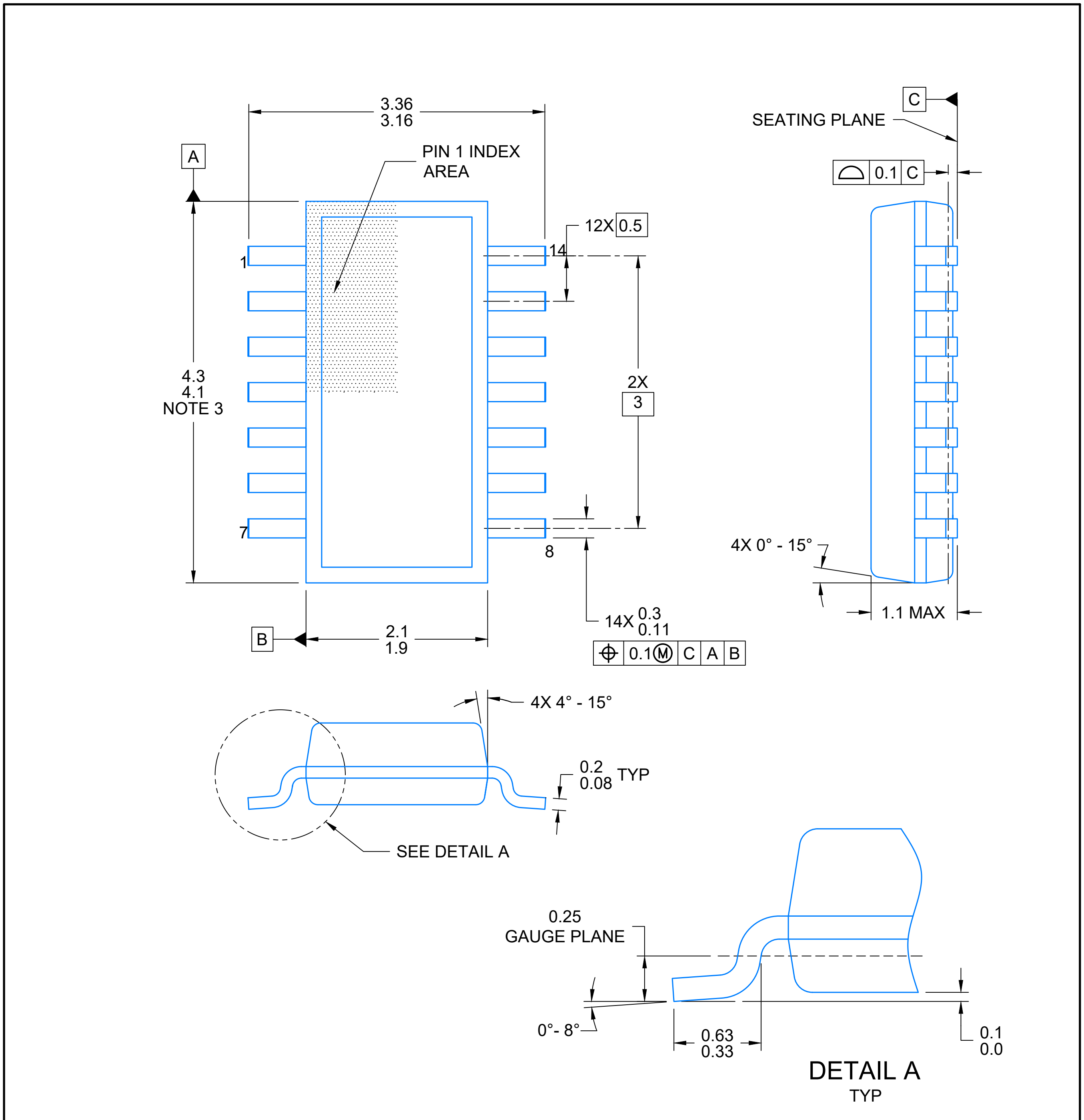


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

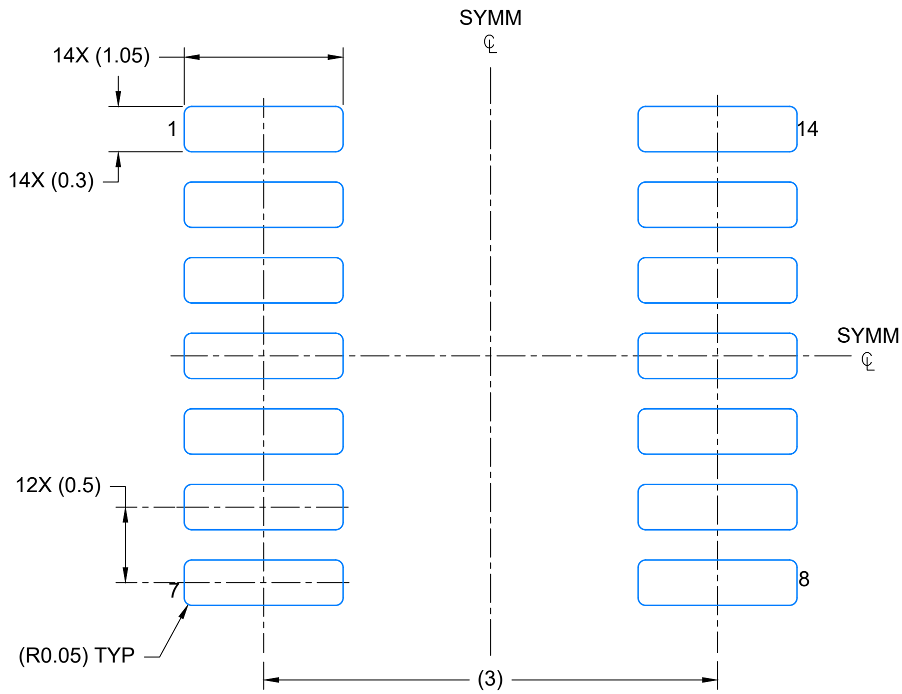
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



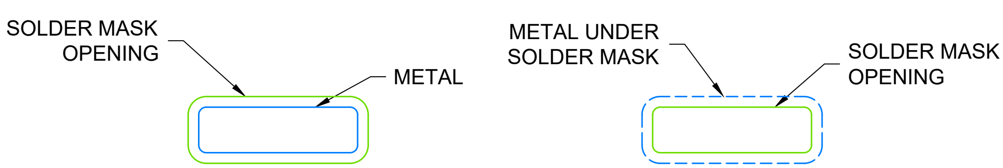
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK DEFINED (PREFERRED)

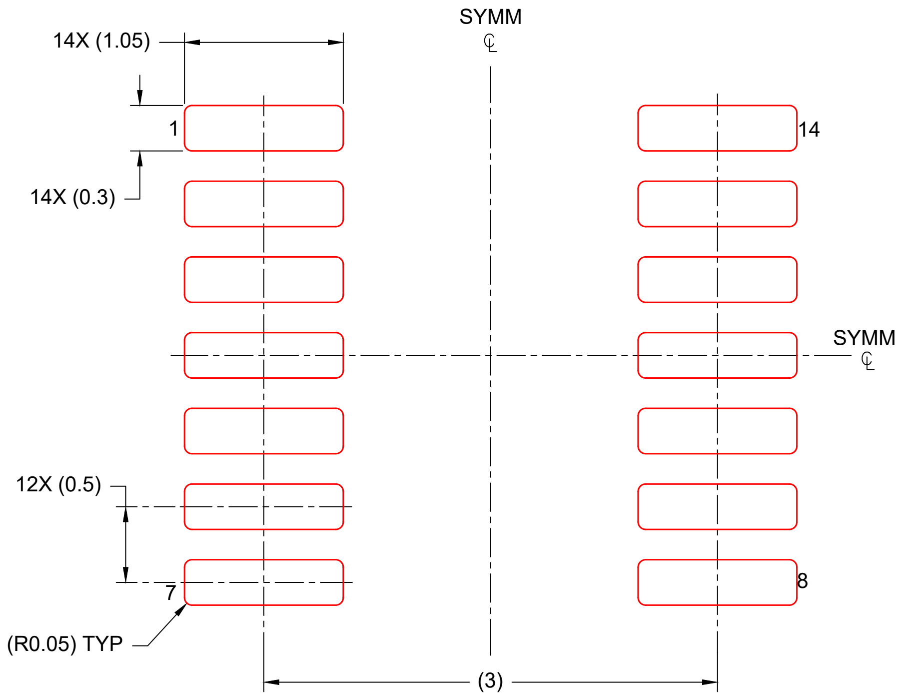
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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