TEXAS INSTRUMENTS
TPS23755
JAJSGY5B – DECEMBER 2018 – REVISED NOVEMBER 2020

TPS23755 フォトカプラなしのフライバック DC/DC コントローラ搭載 IEEE 802.3at PoE PD

1 特長

- タイプ 1 PoE 用の包括的な IEEE 802.3at PD ソリューション
  - Ethernet Alliance (EA) ロゴ認証設計を利用可能
  - 堅牢な 100V、0.36Ω (標準値) ホットスワップ MOSFET
  - プログラム可能な分類レベル
- PWM コントローラと 0.77Ω (標準値) 150V パワー MOSFET を内蔵
  - PSR 付きフライバック・コントローラ
    - 2 次側ダイオード整流器により CCM 動作をサポート
    - ±3% (標準値、12V 出力) の負荷レギュレーション (5% ~ 100% の範囲)
  - ローサイド・スイッチ降圧トポロジをサポート
  - 同期可能な可変スイッチング周波数
  - 高度なスタートアップ
  - プログラム可能なスルーレートと周波数ディザリングにより EMI 低減を強化
- スムーズな遷移で 2 次側アダプタを優先制御
- 接合部温度範囲：–40°C ~ 125°C
- 小型の 6mm × 4mm VSON パッケージ

2 アプリケーション

- IEEE 802.3at 準拠の受電機器
- セキュリティ・カメラ
- IP 電話
- アクセス・ポイント

3 概要

TPS23755 は、Power over Ethernet (PoE) 受電機器 (PD) インターフェイス、150V スイッチング・パワー FET、およびフライバック・トポロジ用に最適化された電流モード DC/DC コントローラを組み合わせたものです。1 次側レギュレーション (PSR)、スペクトラム拡散周波数ディザリング (SSFD)、高度なスタートアップなどの機能を備え高度に統合された TPS23755 は小型の機器に最適なソリューションです。PoE の実装は、13W、タイプ 1 の PD として IEEE 802.3at 規格に対応しています。

DC/DC コントローラの PSR 機能は、補助巻線からの帰還により出力電圧を制御するため、外部シャント・レギュレータおよびフォトカプラは不要です。2 次側ダイオード整流器を使った動作 (通常 12V 以上の出力) 用に最適化されています。通常、コンバータはスイッチング周波数 250kHz 時に連続導通モード (CCM) で動作します。

SFFD およびスルーレート制御により、EMI フィルタのサイズとコストを最小限に抑えることができ、高度なスタートアップにより、コンバータの起動およびヒカップ設計を簡素化すると同時に、使用するバイアス・コンデンサを最小限にできます。

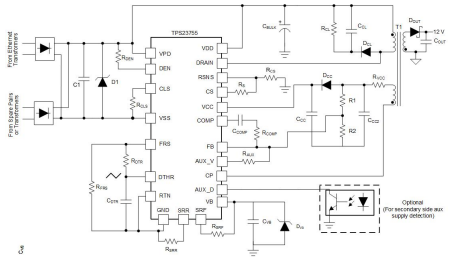
2 次補助電源検出機能により、効率または熱的性能を犠牲にすることなく PoE 入力電力との間でスムーズな遷移を確保しながら、2 次側電源アダプタを優先します。

この DC/DC コントローラは内部ソフトスタート、スロープ補償、ブランキング機能を備えています。非絶縁用途の場合、TPS23755 は降圧トポロジもサポートしています。

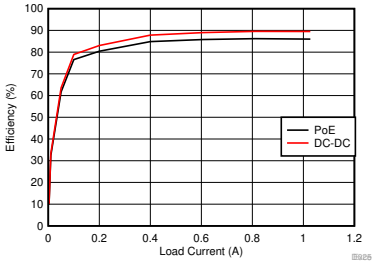
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS23755	VSON (24)	6.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略



効率と負荷電流との関係、12V 出力

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (January 2019) to Revision B (November 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• アプリケーション概略を更新 (Dvb を追加)	1
• Added, "...and 6.2-V Zener diode..."	3
• Added paragraph, "VB is the 5-V bias rail..."	17
• Updated 図 8-1 and 図 8-2 to include Dvb	30
• Added section, "Bias Voltage, CVB and DVB"	32

Changes from Revision * (December 2018) to Revision A (January 2019)	Page
• デバイスのステータスを「量産データ」に変更	1

5 Pin Configuration and Functions

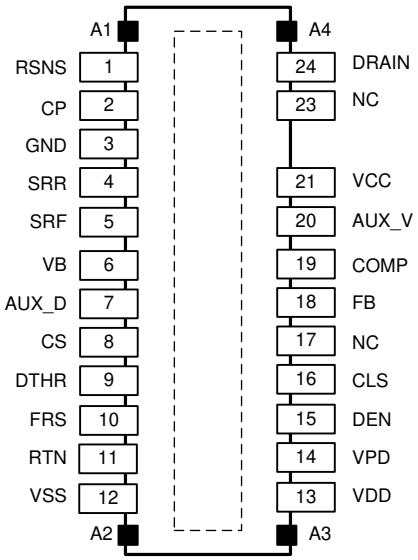


図 5-1. RJJ Package 24-Pin VSON Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RSNS	O	Switching Power FET source connection. Connect to the external power current sense resistor.
2	CP	O	CP provides the clamp for the primary side regulation loop. Connect this pin to the lower end of the second primary side winding of the transformer.
3	GND	—	Power ground used by the flyback power FET gate driver and CP. Connect to RTN.
4	SRR	I	Switching FET Gate sinking current input, used for EMI control. Connect a resistance from SRR to GND to control the Vds rate of rise.
5	SRF	I	Switching FET Gate sourcing current input, used for EMI control. Connect a resistance from SRF to VB to control the Vds rate of fall.
6	VB	O	5-V bias rail for the switching FET gate driver circuit. For internal use only. Bypass with a 0.1-µF ceramic capacitor and 6.2-V Zener diode to GND pin.
7	AUX_D	I	Auxiliary supply detect, internally pulled-up to approximately 5 V. Pull this pin low, typically through an optocoupler from the secondary side, to step down the output voltage of the DC-DC converter when a secondary side auxiliary supply is connected.
8	CS	I	DC-DC controller current sense input. Connect directly to the external power current sense resistor.
9	DTHR	O	Used for spread spectrum frequency dithering. Connect a capacitor from DTHR to RTN and a resistor from DTHR to FRS. If dithering is not used, short DTHR to VB pin.
10	FRS	I/O	This pin controls the switching frequency of the DC-DC converter. Tie a resistor from this pin to RTN to set the frequency.
11	RTN	—	RTN is the output of the PoE hotswap and the reference ground for the DC-DC controller.
12	VSS	—	Negative power rail derived from the PoE source.
13	VDD	—	Source of DC-DC converter start-up current. Connect to VPD for most applications.
14	VPD	—	Positive input power rail for PoE interface circuit. Derived from the PoE source. Bypass with a 0.1 µF to VSS and protect with a TVS.
15	DEN	I/O	Connect a 24.9-kΩ resistor from DEN to VPD to provide the PoE detection signature. Pulling this pin to VSS during powered operation causes the internal hotswap MOSFET to turn off.
16	CLS	O	Connect a resistor from CLS to VSS to program the classification current.
17	NC	—	No connect pin. Leave open.
18	FB	I	Converter error amplifier inverting (feedback) input. It is typically driven by a voltage divider from the auxiliary winding. Also connect to the COMP compensation network.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	COMP	O	Compensation output of the DC-DC convertor error amplifier. Connect the compensation networks from this pin to the FB pin to compensate the converter.
20	AUX_V	O	AUX_V works with AUX_D to step down the output voltage setting of the DC-DC converter when an auxiliary supply is detected. Typically connected to FB pin through a resistor which defines the new voltage setting.
21	VCC	I/O	DC/DC converter bias voltage. The internal startup current source and converter bias winding output power this pin. Connect a 1-µF minimum ceramic capacitor to RTN.
23	NC	—	No connect pin. Leave open.
24	DRAIN	O	Drain connection to the internal switching power MOSFET of the DC/DC controller.
-	PAD	—	The exposed thermal pad must be connected to VSS. A large fill area is required to assist in heat dissipation.
A1-A4	ANCHORS	—	Should be soldered to PCB for mechanical performance. These pins are not connected internally.

6 Specifications

6.1 Absolute Maximum Ratings

Voltage are with respect to V_{VSS} (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VDD, VPD, DEN, GND, RTN(2)	–0.3	100	V
	VDD to RTN	–0.3	100	
	AUX_D, FB, CS, all to RTN	–0.3	6.5	
	SRF to GND	–0.3	6.5	
Voltage	CLS(3)	–0.3	6.5	V
	FRS(3), COMP(3), VB(3), SRR(3), DTHR(3), RSNS(3), AUX_V(3), all to RTN	–0.3	6.5	
	VCC to RTN	–0.3	19	
	DRAIN to GND	–0.3	150	
	CP to GND	–0.3	60	
	GND to RTN	–0.3	0.3	
Sourcing current	VB, VCC	Internally limited		mA
	CLS		35	
	COMP	Internally limited		
Sinking current	RTN	Internally limited		mA
	DEN		1	
	AUX_V		5	
	COMP	Internally limited		
I_{DRAIN}	Switching DRAIN peak current limit		2	A
	Switching DRAIN peak current limit, Buck topology with 16% duty-cycle		3	
Peak sourcing current	CP		1.5	A
$T_{J(max)}$	Maximum junction temperature	Internally Limited		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{RTN} = 0 for V_{RTN} > 80 V.
(3) Do not apply voltage to these pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 contact discharge(3)	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) ESD per EN61000-4-2, applied between RJ-45 and output ground of the TPS23755EVM-894 evaluation module. These were the test levels, not the failure threshold.

6.3 Recommended Operating Conditions

Voltage with respect to V_{VSS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	VDD, VPD, RTN, GND	0		57	V
	VCC to RTN	0		16	
	AUX_D to RTN	0		VB	
	CS to RTN	0		2	
	DRAIN to GND	0		125	
	CP to GND	0		45	
Sinking current	RTN			350	mA
Peak current limit	DRAIN, RSNS			1.6	A
	DRAIN, RSNS, Buck topology with 16% duty-cycle			2.5	
Peak sourcing current	CP			500	mA
Capacitance	VB(1)	0.08	0.1		µF
	VCC	0.8	1		
Resistance	CLS(1)	30			Ω
	SRF to VB			100	
	SRR to GND			15	
Synchronization pulse width input (when used)	FRS	35			ns
T_J	Operating junction temperature	–40		125	°C

(1) Voltage should not be externally applied to this pin.

6.4 Thermal Information

THERMAL METRIC(1)		TPS23755 RJJ (VSON) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: DC-DC Controller Section

Unless otherwise noted, V_{VDD} = 48 V; R_{DEN} = 24.9 kΩ; R_{FRS} = 60.4 kΩ; CLS, AUX_V, RSNS and DRAIN open; CS, AUX_D, and GND connected to RTN; SRR connected to GND; SRF, FB and DTHR connected to VB; C_{VB} = 0.1 µF; C_{CC} = 1 µF; 8.5 V ≤ V_{VCC} ≤ 16 V; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins unless otherwise noted. Typical values are at 25°C. [V_{VSS} = V_{RTN} and V_{VPD} = V_{VDD}] or [V_{VSS} = V_{RTN} = V_{VPD}], all voltages referred to V_{RTN} and V_{GND} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC SUPPLY (VCC)						
V_{CUVR}	Undervoltage lockout	V_{VCC} rising	8	8.25	8.6	V
V_{CUVF}		V_{VCC} falling	5.85	6.1	6.25	V
V_{CUVH}		Hysteresis(1)	2	2.15	2.5	V
I_{RUN}	Operating current, converter switching	V_{VCC} = 10 V, V_{FB} = V_{RTN} = V_{RSNS} , DRAIN with 2-kΩ pull up to 95 V		2.0	2.35	mA
t_{ST}	Start-up time, C_{CC} = 1 µF	V_{DD} = 10.2 V, V_{VCC}(0) = 0 V	0.5	1.0	2.5	ms
		V_{DD} = 35 V, V_{VCC}(0) = 0 V	0.5	0.80	1.5	ms
V_{VC_ST}	VCC startup voltage	Measure V_{VCC} during startup, I_{VCC} = 0 mA	11	13	15.5	V
DC-DC TIMING (FRS)						
f_{SW}	Switching frequency	V_{FB} = V_{RSNS} = V_{RTN}, Measure at DRAIN	223	248	273	kHz
D_{MAX}	Duty cycle	V_{FB} = V_{RSNS} = V_{RTN}, Measure at DRAIN	75%	77.5%	80%	
V_{SYNC}	Synchronization	Input threshold	2	2.2	2.4	V
FREQUENCY DITHERING RAMP GENERATOR (DTHR)						
I_{DTRCH}	Charging (sourcing) current	0.5 V < V_{DTHR} < 1.38 V		3 x I_{FRS}		µA
			47.2	49.6	52.1	µA
I_{DTRDC}	Discharging (sinking) current	0.6 V < V_{DTHR} < 1.5 V		3 x I_{FRS}		µA
			47.2	49.6	52.1	µA
V_{DTUT}	Dithering upper threshold	V_{DTHR} rising until I_{DTHR} > 0	1.41	1.513	1.60	V
V_{DTLT}	Dithering lower threshold	V_{DTHR} falling until I_{DTHR} < 0	0.43	0.487	0.54	V
VDTPP	Dithering pk-pk amplitude		1.005	1.026	1.046	V
ERROR AMPLIFIER (FB, COMP)						
V_{REFC}	Feedback regulation voltage		1.723	1.75	1.777	V
I_{FB_LK}	FB leakage current (source or sink)	V_{FB-RTN} = 1.75 V			0.5	µA
G_{BW}	Small signal unity gain bandwidth		0.9	1.2		MHz
A_{OL}	Open loop voltage gain		70	90		dB
V_{ZDC}	0% duty-cycle threshold	V_{COMP} falling until DRAIN switching stops	1.35	1.5	1.65	V
I_{COMPH}	COMP source current	V_{FB} = V_{RTN} , V_{COMP} = 3 V	1			mA
I_{COMPL}	COMP sink current	V_{FB} = V_{VB} , V_{COMP} = 1.25 V	2.1	6		mA
V_{COMPH}	COMP high voltage	V_{FB} = V_{VB} , 15 kΩ from COMP to RTN	4		5	V
V_{COMPL}	COMP low voltage	V_{FB} = V_{VB} , 15 kΩ from COMP to VB			1.1	V
	COMP to CS gain	ΔV_{CS} / ΔV_{COMP} , 0 V < V_{CS} < 0.5 V	0.475	0.5	0.525	V/V
SOFT-START						
t_{SS}	Soft-start period		8	16	24	ms
t_{CD}	Cool-down period		15	20	26	ms
CURRENT SENSE (CS)						
V_{CSMAX}	Maximum threshold voltage	V_{FB} = V_{RTN}, V_{CS} rising	0.5	0.55	0.6	V

6.5 Electrical Characteristics: DC-DC Controller Section (continued)

Unless otherwise noted, V_{VDD} = 48 V; R_{DEN} = 24.9 kΩ; R_{FRS} = 60.4 kΩ; CLS, AUX_V, RSNS and DRAIN open; CS, AUX_D, and GND connected to RTN; SRR connected to GND; SRF, FB and DTHR connected to VB; C_{VB} = 0.1 µF; C_{CC} = 1 µF; 8.5 V ≤ V_{VCC} ≤ 16 V; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins unless otherwise noted. Typical values are at 25°C. [V_{VSS} = V_{RTN} and V_{VPD} = V_{VDD}] or [V_{VSS} = V_{RTN} = V_{VPD}], all voltages referred to V_{RTN} and V_{GND} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFFDEL_ILM}	Current limit turnoff delay	V_{CS} = 0.65 V	25	41	60	ns
t_{OFFDEL_PW}	PWM comparator turnoff delay	V_{CS} = 0.4 V	25	41	60	
	Blanking delay	In addtition to t_{OFFDEL}	56.5	75	93.5	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referred to CS	120	155	185	mV
I_{SL_EX}	Peak slope compensation current	V_{FB} = V_{RTN}, I_{CS} at maximum duty cycle (ac component)	30	42	54	µA
	Bias current	DC component of CS current	-6.7	-5	-3.3	µA
SWITCHING POWER FET (DRAIN, RSNS)						
BV_{DSS}	Power FET break-down voltage		150			V
$R_{DS(ON)}$	Power FET on resistance			0.77	1.28	Ω
V_{SD}	Source-to-drain diode forward voltage	I_{RSNS} = 500 mA	0.6	1	1.1	V
SECONDARY SIDE AUXILIARY POWER (AUX_D, AUX_V)						
V_{AUXEN}	AUX_D threshold voltage	V_{AUX_D} rising	1.7	2	2.3	V
V_{AUXH}		Hysteresis (1)		0.15		V
I_{pullup}	AUX_D pullup current		70	100	130	µA
V_{AVL}	AUX_V output low voltage	V_{AUX_D} = V_{VB} , 5 KΩ from AUX_V to VB			50	mV
THERMAL SHUTDOWN						
	Turnoff temperature		145	159	165	°C
	Hysteresis(2)			13		°C

(1) The hysteresis tolerance tracks the rising threshold for a given device.
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.6 Electrical Characteristics: PoE and Control

Unless otherwise noted, V_{VPD} = 48 V; R_{DEN} = 24.9 kΩ; R_{FRS} = 60.4 kΩ; CLS, AUX_V, RSNS and DRAIN open; CS, AUX_D, and GND connected to RTN; SRR connected to GND; SRF, FB and DTHR connected to VB; C_{VB} = 0.1 µF; C_{CC} = 1 µF; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins unless otherwise noted. Typical values are at 25°C.
Unless otherwise noted, V_{VPD} = V_{VDD} , V_{VCC} = V_{RTN}. All voltages referred to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PD DETECTION (DEN)							
	Detection bias current	DEN open, V_{VPD} = 10 V, Measure I_{VPD} + I_{VDD} + I_{DEN} + I_{RTN}		3.5	8.3	13.9	µA
I_{lkg}	DEN leakage current	V_{DEN} = V_{VPD} = 57 V, Measure I_{DEN}			0.1	5	µA
	Detection current	Measure I_{VPD} + I_{VDD} + I_{DEN} + I_{RTN} , V_{VPD} = 1.4 V		55.5	56.3	60	µA
		Measure I_{VPD} + I_{VDD} + I_{DEN} + I_{RTN} , V_{VPD} = 10 V		400	407	414.5	µA
V_{PD_DIS}	Hotswap disable threshold			3	4	5	V
PD CLASSIFICATION (CLS)							
I_{CLS}	Classification current	R_{CLS} = 649 Ω	13 V ≤ V_{DD} ≤ 21 V, Measure I_{VPD} + I_{VDD} + I_{DEN} + I_{RTN}	1.8	2.14	2.4	mA
		R_{CLS} = 121 Ω		9.9	10.6	11.3	
		R_{CLS} = 68.1 Ω		17.6	18.6	19.4	
		R_{CLS} = 45.3 Ω		26.5	27.9	29.3	
V_{CL_ON}	Classification regulator lower threshold	Regulator turns on, V_{VPD} rising		10.7	12.1	13	V
V_{CL_HYS}		Hysteresis[1]		0.6	1.1	1.55	V
V_{CU_OFF}	Classification regulator upper threshold	Regulator turns off, V_{VPD} rising		21	22	23	V
V_{CU_HYS}		Hysteresis[1]		0.5	0.77	1	V
I_{lkg}	Leakage current	V_{VPD} = 57 V, V_{CLS} = 0 V, V_{DEN} = V_{VSS}, Measure I_{CLS}				1	µA
RTN (PASS DEVICE)							
	ON-resistance				0.36	0.68	Ω
	Current limit	V_{RTN} = 1.5 V, pulsed measurement		405	550	800	mA
	Inrush current limit	V_{RTN} = 2 V, V_{VPD}: 0 V → 48 V, pulsed measurement		100	140	220	mA
	Foldback voltage threshold	V_{RTN} rising		11	12.3	13.6	V
	Foldback deglitch time	V_{RTN} rising to when current limit changes to inrush current limit		150	387	600	µs
I_{lkg}	Leakage current	V_{VPD} = V_{RTN} = 100 V, V_{DEN} = V_{VSS}				40	µA
PD INPUT SUPPLY (VPD, VDD)							
UVLO_R	Undervoltage lockout threshold	V_{VPD} rising		34.7	35.5	36.7	V
UVLO_H		Hysteresis [1]		4.1	4.5	4.7	V
I_{VPD_VDD}	Operating current	VCC open, 40 V ≤ V_{VPD} = V_{VDD} ≤ 57 V, Startup completed, Measure I_{VPD} + I_{VDD}			300	580	µA
	Off-state current	RTN, GND and VCC open, V_{VPD} = 30 V, Measure I_{VPD}				330	
THERMAL SHUTDOWN							
	Turnoff temperature			145	159	165	°C
	Hysteresis[2]				13		°C

(1) The hysteresis tolerance tracks the rising threshold for a given device.
(2) These parameters are provided for reference only.

6.7 Typical Characteristics

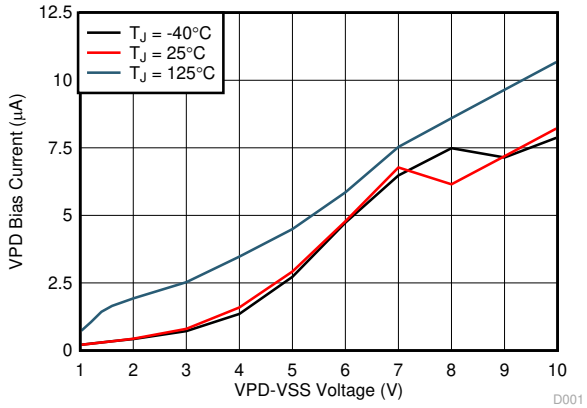


図 6-1. Detection Bias Current vs Voltage

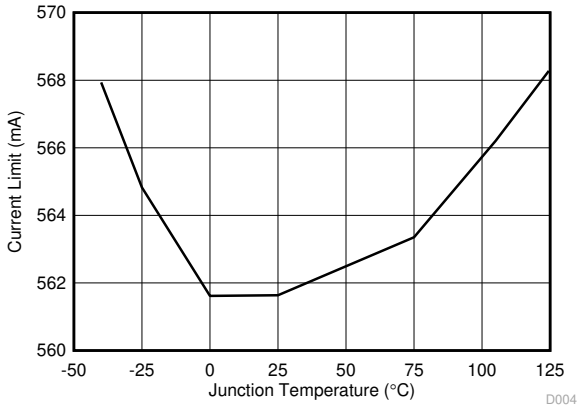


図 6-2. PoE Current Limit vs Temperature

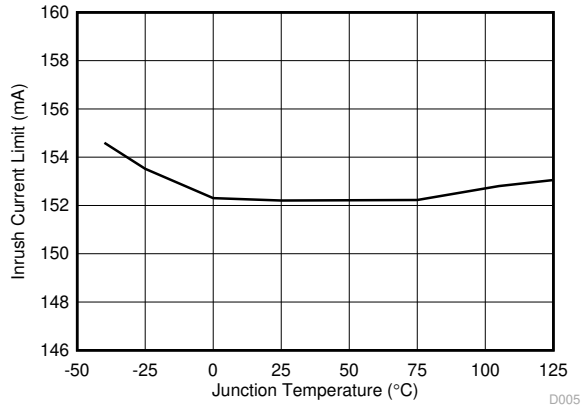


図 6-3. PoE Inrush Current Limit vs Temperature

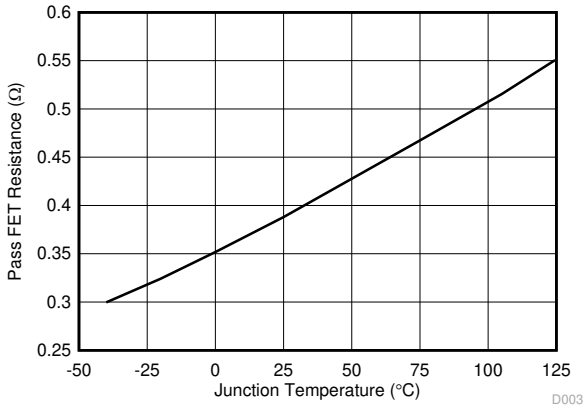


図 6-4. Pass FET Resistance vs Temperature

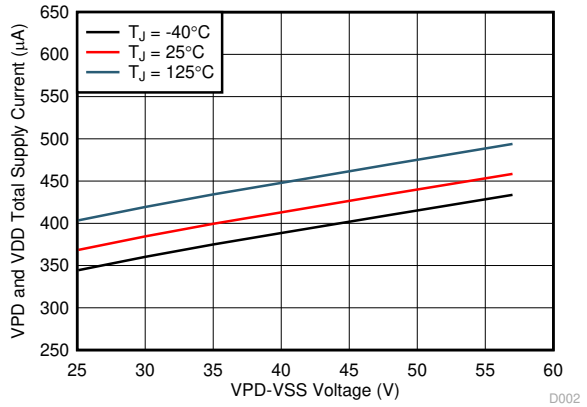


図 6-5. VPD and VDD Supply Current vs Voltage

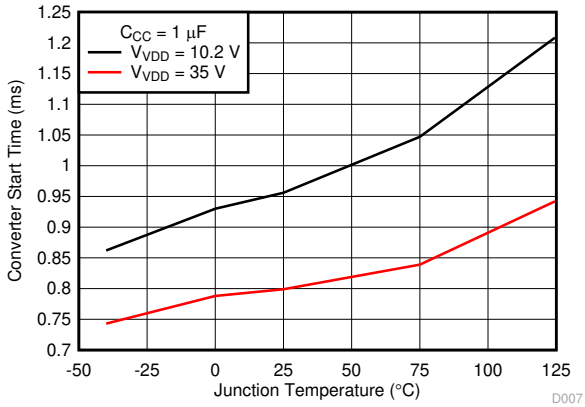


図 6-6. Converter Startup Time vs Temperature

6.7 Typical Characteristics (continued)

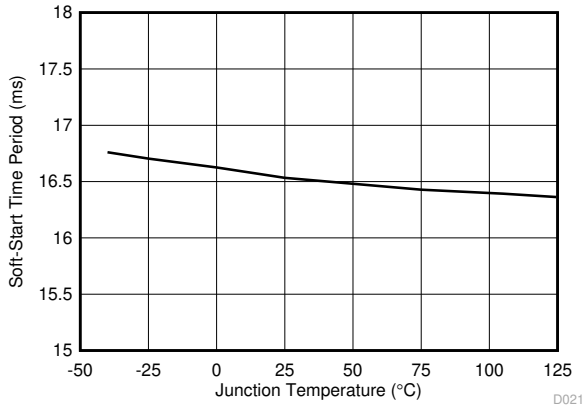


図 6-7. Converter Soft-Start Time vs Temperature

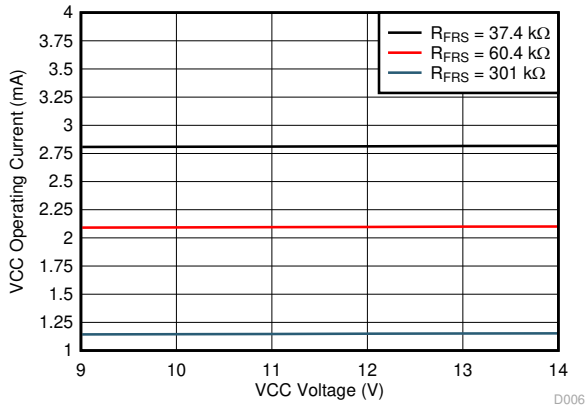


図 6-8. Controller Bias Current vs Voltage

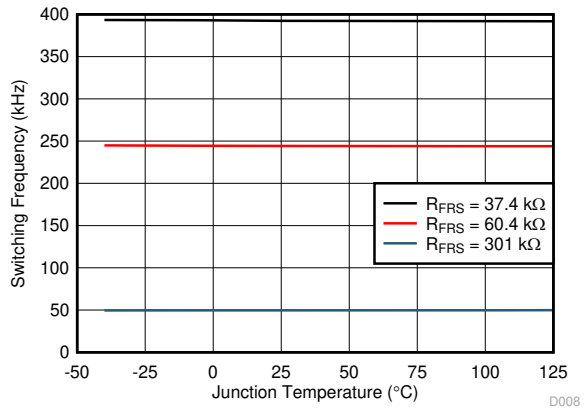


図 6-9. Switching Frequency vs Temperature

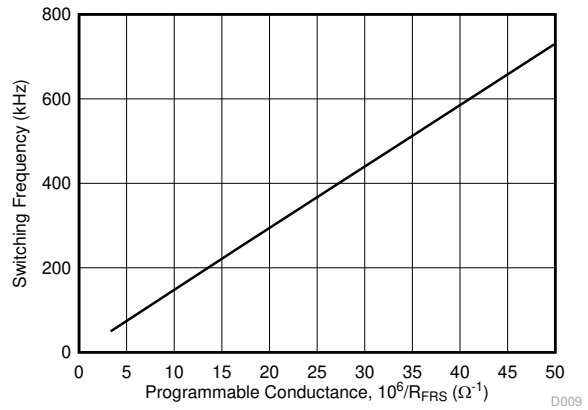


図 6-10. Switching Frequency vs Programmed Resistance

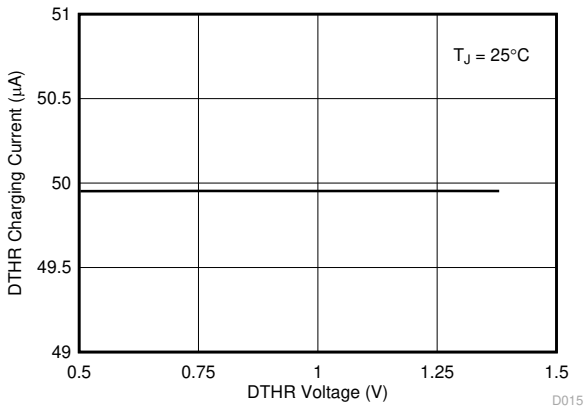


図 6-11. Frequency Dithering Charging Current

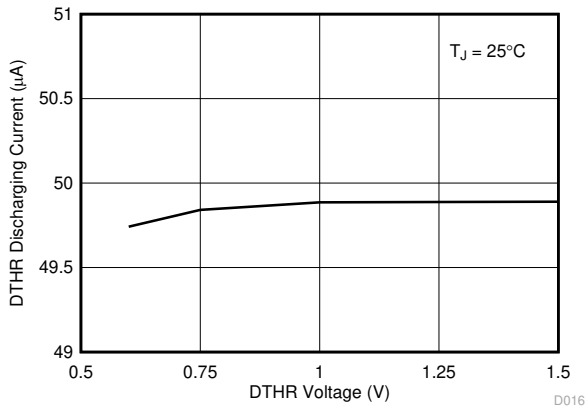


図 6-12. Frequency Dithering Discharging Current

6.7 Typical Characteristics (continued)

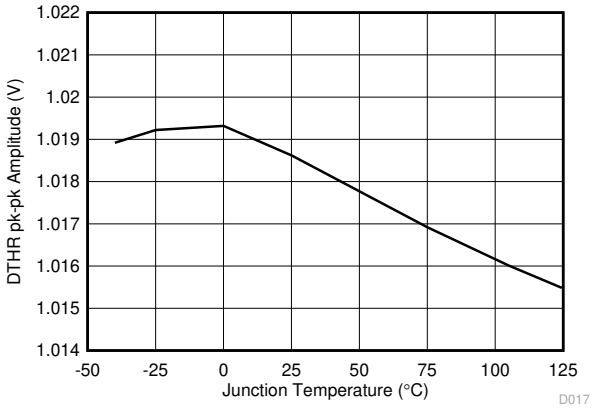


図 6-13. Frequency Dithering Peak-to-Peak Amplitude

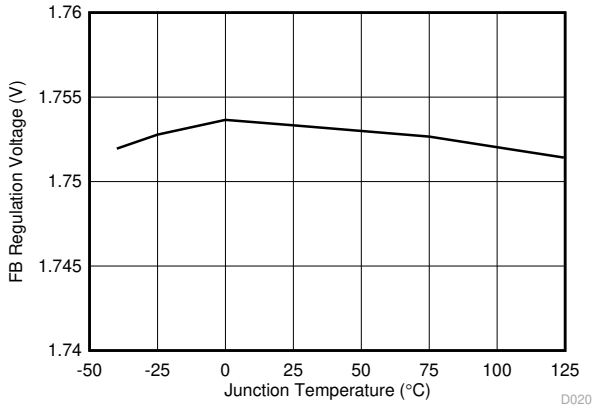


図 6-14. Feedback Regulation Voltage vs Temperature

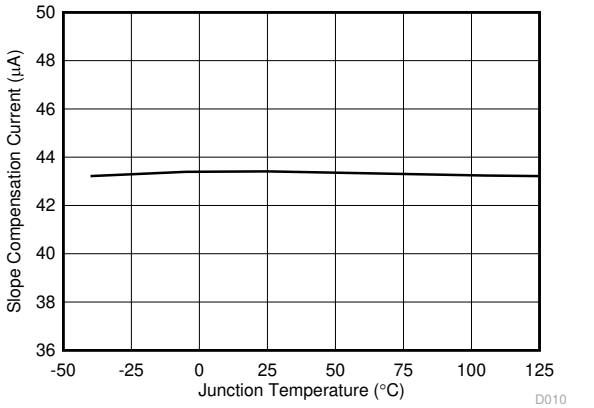


図 6-15. Current Slope Compensation Current vs Temperature

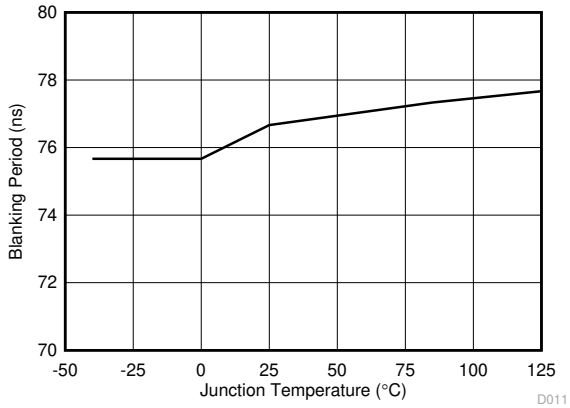


図 6-16. Blanking Period vs Temperature

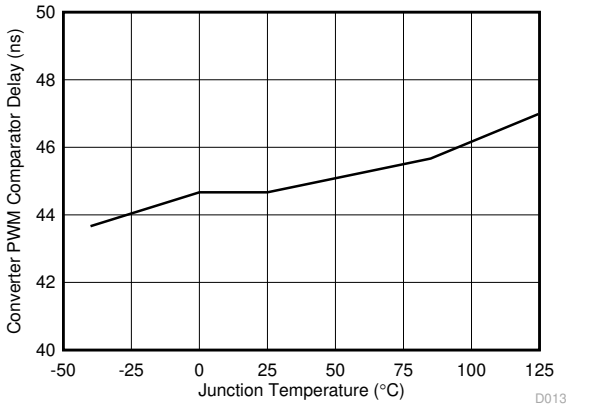


図 6-17. Converter PWM Comparator Delay vs Temperature

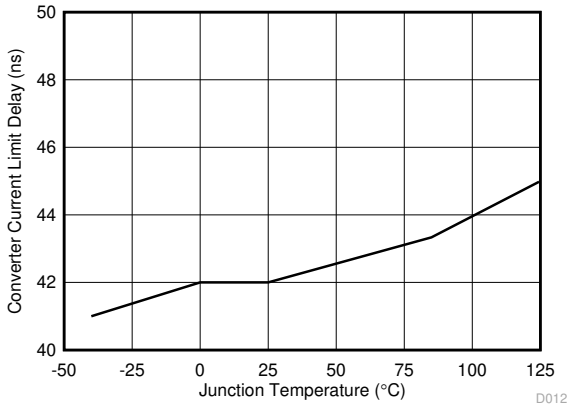


図 6-18. Converter Current Limit Delay vs Temperature

6.7 Typical Characteristics (continued)

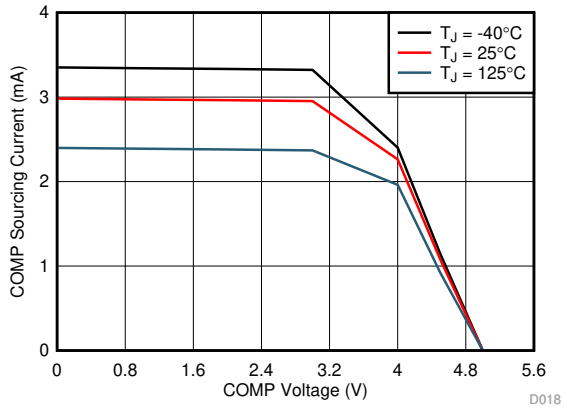


図 6-19. Error Amplifier Source Current

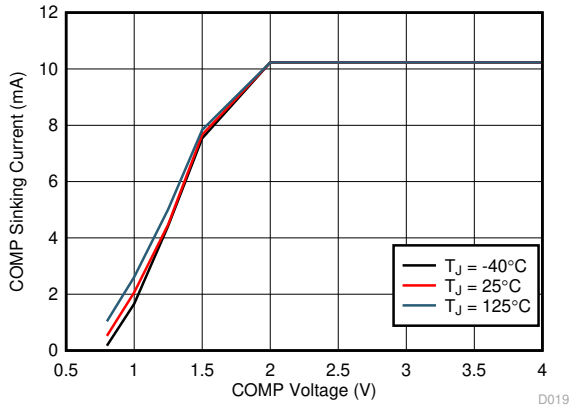


図 6-20. Error Amplifier Sink Current

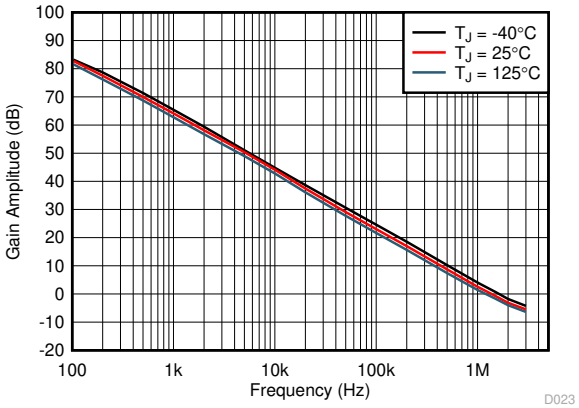


図 6-21. Error Amplifier Gain vs Frequency

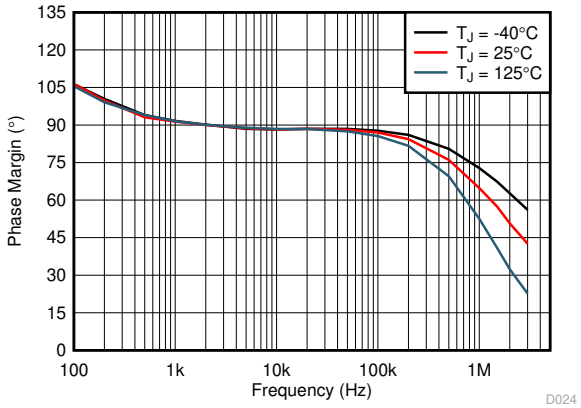


図 6-22. Error Amplifier Phase vs Frequency

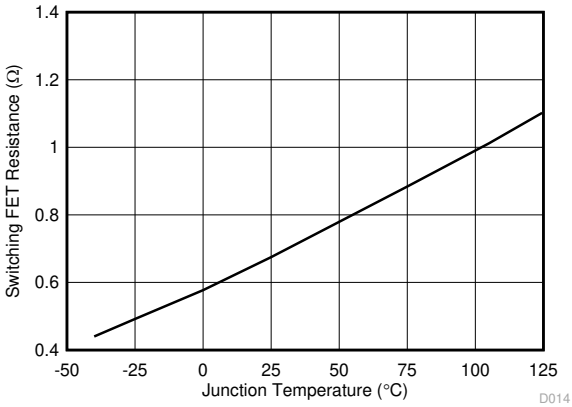


図 6-23. Switching FET Resistance vs Temperature

7 Detailed Description

7.1 Overview

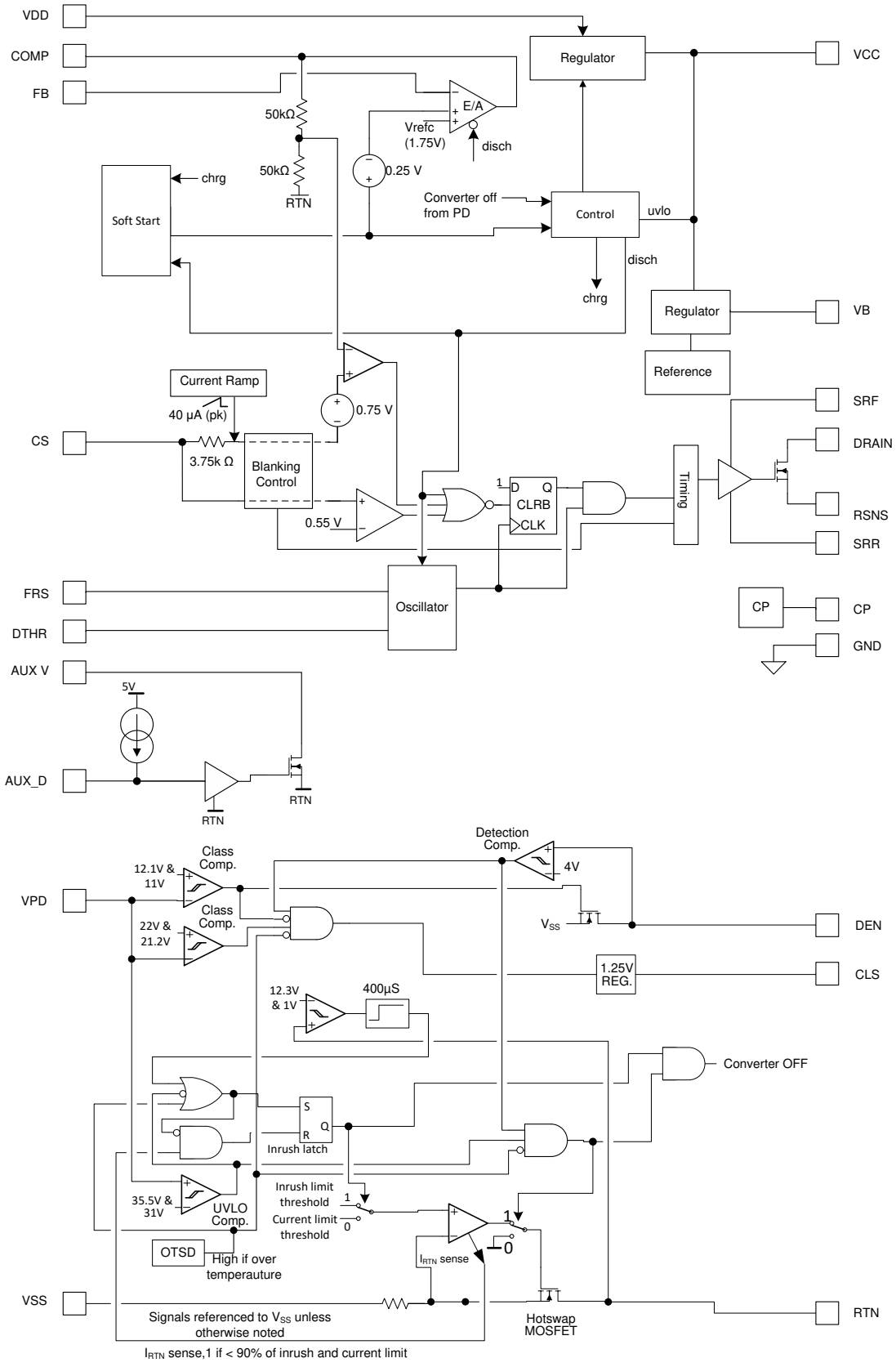
The TPS23755 device is a 24-pin integrated circuit that contains all of the features needed to implement an IEEE802.3at Type-1 powered device (PD), combined with a fully integrated 150-V switching power FET and a current-mode DC-DC controller optimized for flyback switching regulator designs using primary side control. The TPS23755 applies to single-output flyback converter applications where a secondary side diode rectifier is used.

Basic PoE PD functionality supported includes detection, hardware classification, and inrush current limit during startup. DC-DC converter features include startup function and current mode control operation. The TPS23755 device integrates a low 0.36-Ω internal switch to support Type-1 applications.

The TPS23755 features secondary auxiliary power detect (AUX_D) capability, providing priority for a secondary side power adapter, while ensuring smooth transition (via AUX_V) to and from the PoE power input.

The TPS23755 device contains several protection features such as f, current limit foldback, and a robust 100-V internal return switch.

7.2 Functional Block Diagram



7.3 Feature Description

See 図 8-1 for component reference designators (R_{CS} for example), and *Electrical Characteristics: DC-DC Controller Section* for values denoted by reference (V_{CSMAX} for example). Electrical Characteristic values take precedence over any numerical values used in the following sections.

7.3.1 CLS Classification

An external resistor (R_{CLS} in 図 8-1) connected between the CLS pin and VSS provides a classification signature to the PSE. The controller places a voltage of approximately 1.25 V across the external resistor whenever the voltage differential between VPD and VSS lies from about 11 V to 22 V. The current drawn by this resistor, combined with the internal current drain of the controller and any leakage through the internal pass MOSFET, creates the classification current. 表 7-1 lists the external resistor values required for each of the PD power ranges defined by IEEE802.3at. The maximum average power drawn by the PD, plus the power supplied to the downstream load, should not exceed the maximum power indicated in Table 7-1. The TPS23755 supports class 0 – 3 power levels.

表 7-1. Class Resistor Selection

CLASS	POWER AT PD PI		RESISTOR (Ω)
	MINIMUM (W)	MAXIMUM (W)	
0	0.44	12.95	649
1	0.44	3.84	121
2	3.84	6.49	68.1
3	6.49	12.95	45.3

7.3.2 DEN Detection and Enable

DEN pin implements two separate functions. A resistor (R_{DEN} in 図 8-1) connected between VPD and DEN generates a detection signature whenever the voltage differential between VPD and VSS lies from approximately 1.4 to 11 V. Beyond this range, the controller disconnects this resistor to save power. The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} from 23.75 kΩ to 26.25 kΩ, or 25 kΩ ± 5%. TI recommends a resistor of 24.9 kΩ ± 1% for R_{DEN}.

Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET and class regulator to turn off. If the resistance connected between VDD and DEN is divided into two roughly equal portions, then the application circuit can disable the PD by grounding the tap point between the two resistances, while simultaneously spoiling the detection signature which prevents the PD from properly re-detecting.

7.3.3 Internal Pass MOSFET

RTN pin provides the negative power return path for the load. It is internally connected to the drain of the PoE hotswap MOSFET, and the DC-DC controller return. RTN must be treated as a local reference plane (ground plane) for the DC-DC controller and converter primary to maintain signal integrity.

Once V_{VPD} exceeds the UVLO threshold, the internal pass MOSFET pulls RTN to VSS. Inrush limiting prevents the RTN current from exceeding a nominal value of about 140 mA until the bulk capacitance (C_{BULK} in 図 8-1) is fully charged. Inrush ends when the RTN current drops below about 125 mA. The RTN current is subsequently limited to about 0.45 A.

If RTN ever exceeds about 12.3 V for longer than 400 µs, then the PD returns to inrush limiting.

7.3.4 DC-DC Controller Features

The TPS23755 device DC-DC controller implements a typical current-mode control as shown in *Functional Block Diagram*. Features include oscillator, overcurrent and PWM comparators, current-sense blanker, soft start, gate driver and switching power FET. In addition, an internal current-compensation ramp generator, frequency synchronization logic, built-in frequency dithering functionality, thermal shutdown, and start-up current source with control are provided.

The TPS23755 is optimized for isolated converters, and it includes an internal error amplifier. The voltage feedback is from the bias winding. The COMP output of the error amplifier is directly fed to a 2:1 internal resistor divider and an offset of $V_{ZDC}/2$ (approximately 0.75 V) which defines a current-demand control for the pulse width modulator (PWM). A V_{COMP} below V_{ZDC} stops converter switching, while voltages above (V_{ZDC} + 2 × (V_{CSMAX} + V_{SLOPE})) does not increase the requested peak current in the switching MOSFET.

The internal start-up current source and control logic implement a bootstrap-type startup. The startup current source charges C_{CC} from VDD and maintain its voltage when the converter is disabled or during the soft-start period, while operational power must come from a converter (bias winding) output.

The bootstrap source provides reliable start-up from widely varying input voltages, and eliminates the continual power loss of external resistors.

The peak current limit does not have duty cycle dependency unless R_S is used as shown in 図 7-2 to increase slope compensation. This makes it easier to design the current limit to a fixed value.

The DC-DC controller has an OTSD that can be triggered by heat sources including the power switching FET and GATE driver. The controller OTSD turns off the switching FET and resets the soft-start generator.

7.3.4.1 VCC, VB and Advanced PWM Startup

The VCC pin connects to the auxiliary bias supply for the DC-DC controller. The switching MOSFET gate driver draws current directly from the VB pin, which is the output of an internal 5-V regulator fed from VCC. A startup current source from VDD to VCC implements the converter bootstrap startup. VCC must receive power from an auxiliary source, such as an auxiliary winding on the flyback transformer, to sustain normal operation after startup.

The startup current source is turned on during the inrush phase, charging C_{CC} and maintaining its voltage, and it is turned off only after the DC-DC soft-start cycle has been completed, which occurs when the DC-DC converter has ramped up its output voltage, as shown in 図 7-1. Internal loading on VCC and VB is initially minimal while C_{CC} charges, to allow the converter to start. Due to the high current capability of the startup source, the recommended capacitance at VCC is relatively small, typically 1 µF in most applications.

VB is the 5-V bias rail for the switching FET gate driver circuit. A 0.1-µF bypass capacitor between VB and RTN is required. Additionally, a 6.2-V Zener diode from VB to RTN is required.

Once V_{VCC} falls below its UVLO threshold, the converter shuts off and the startup current source is turned back on, initiating a new PWM startup cycle.

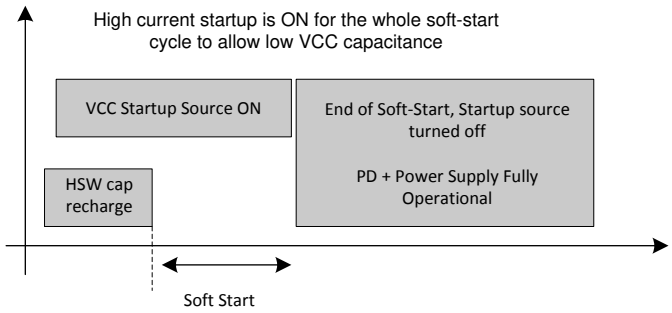


図 7-1. Advanced Startup

7.3.4.2 CS, Current Slope Compensation and Blanking

The current-sense input for the DC-DC converter should be connected to the high side of the current-sense resistor of the switching MOSFET. The current-limit threshold, V_{CSMAX}, defines the voltage on CS above which the switching FET ON-time is terminated regardless of the voltage on COMP output.

Routing between the current-sense resistor and the CS pin must be short to minimize cross-talk from noisy traces such as DRAIN and CP, and to a lower degree to SRR and SRF.

Current-mode control requires addition of a compensation ramp to the sensed inductor (flyback transformer) current for stability at duty cycles near and over 50%. The TPS23755 has a maximum duty cycle limit of 78.5%,

permitting the design of wide input-range flyback converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 78.5%, converters may be designed that run at duty cycles well below this for a narrower, 36-V to 57-V range. The TPS23755 provides a fixed internal compensation ramp that suffices for most applications. R_S (see 図 7-2) may be used if the internally provided slope compensation is not enough. It works with ramp current (I_{PK} = I_{SL-EX}, approximately 40 µA) that flows out of the CS pin when the MOSFET is on. The I_{PK} specification does not include the approximately 5-µA fixed current that flows out of the CS pin.

Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period); however, *Electrical Characteristics: DC-DC Controller Section* specifies the slope peak (V_{SLOPE}) based on the maximum duty cycle. Assuming that the desired slope, $V_{SLOPE-D}$ (in mV/period), is based on the full period, compute R_S per 式 1 where V_{SLOPE}, D_{MAX}, and I_{SL-EX} are from *Electrical Characteristics: DC-DC Controller Section* with voltages in mV, current in µA, and the duty cycle is unitless (for example, D_{MAX} = 0.78).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(V_{SLOPE}(mV)/D_{MAX}\right)\right]}{I_{SL_{EX}}(\mu A)/D_{MAX}} \times 1000 \quad (1)$$

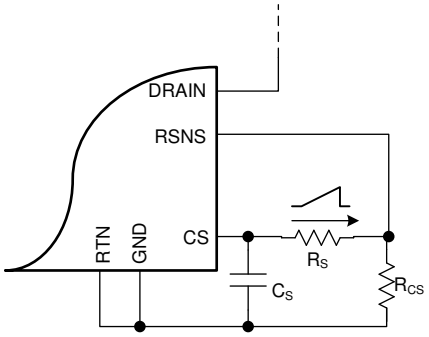


図 7-2. Additional Slope Compensation

Blanking provides an interval between the FET gate drive going high and the current comparator on CS actively monitoring the input. This delay allows the normal turnon current transient (spike) to subside before the comparator is active, preventing undesired short duty cycles and premature current limiting.

The TPS23755 blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. There may be some situations or designers that prefer an R-C approach, for example if the presence of R_S causes increased noise, due to adjacent noisy signals, to appear at CS pin. The TPS23755 provides a pulldown on CS (approximately 400 Ω) during the GATE OFF-time to improve sensing when an R-C filter must be used, by reducing cycle-to-cycle carry-over voltage on C_S.

7.3.4.3 COMP, FB, CP and Opto-less Feedback

The TPS23755 DC-DC controller implements current-mode control, using a voltage control loop error amplifier (pins FB and COMP) to define the input reference voltage of the current mode control comparator which determines the switching MOSFET peak current. Loop compensation components are connected between COMP and FB.

V_{COMP} below V_{ZDC} causes the converter to stop switching. The maximum (peak) current is requested at approximately (V_{ZDC} + 2 × (V_{CSMAX} + V_{SLOPE})). The AC gain from COMP to the PWM comparator is 0.5.

The TPS23755 DC-DC controller can operate with feedback from an auxiliary winding of the flyback power transformer, eliminating the need for external shunt regulator and optocoupler. It also operates with continuously connected feedback, enabling better optimization of the power supply, and resulting in significantly lower noise sensitivity.

The TPS23755 applies to single-output flyback converter applications where a secondary side diode rectifier is used. In typical 12 V output application and when combined with a correctly designed power transformer, ±5% load regulation over a wide (5% to 100%) output current range can be achieved.

7.3.4.4 FRS Frequency Setting and Synchronization

The FRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the TPS23755 converter to a higher frequency. The internal oscillator sets the maximum duty cycle and controls the current-compensation ramp circuit, making the ramp height independent of frequency. R_{FRS} must be selected per 式 2.

$$R_{FRS}\,(k\Omega) = \frac{15000}{f_{SW}\,(kHz)} \tag{2}$$

The TPS23755 may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (> 35 ns) of magnitude V_{SYNC} to FRS as shown in 図 7-3. R_{FRS} must be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential ON-time period, and the OFF-time period does not begin until the pulse terminates. A short pulse is preferred to avoid reducing the potential ON-time.

Figure 7-3 shows examples of nonisolated and transformer-coupled synchronization circuits. R_T reduces noise susceptibility for the isolation transformer implementation. The FRS node must be protected from noise because it is high impedance.

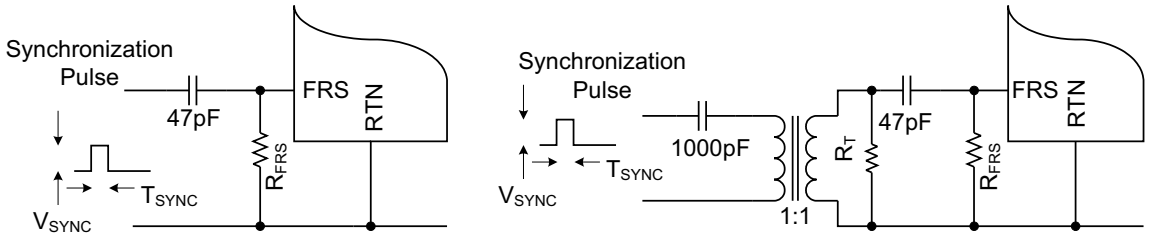


図 7-3. Synchronization

7.3.4.5 Frequency Dithering for Spread Spectrum Applications

The international standard CISPR 22 (and adopted versions) is often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port under section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback*, SLUA469. Additionally, IEEE 802.3at sections 33.3 and 33.4 have requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

A technique referred to as frequency dithering can also be used to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements.

Frequency dithering is a built-in feature of the TPS23755. The oscillator frequency can be dithered by connecting a capacitor from DTHR to RTN and a resistor from DTHR to FRS. An external capacitor, C_{DTR} (図 8-1), is selected to define the modulation frequency f_m. This capacitor is being continuously charged and discharged between slightly less than 0.5 V and slightly above 1.5 V by a current source/sink equivalent to approximately 3x the current through FRS pin. C_{DTR} value is defined according to:

$$C_{DTR} = \frac{3/R_{FRS}\,(\Omega)}{2.052 \times f_m\,(Hz)} \tag{3}$$

f_m should always be higher than 9 kHz, which is the resolution bandwidth applied during conducted emission measurement. Typically, f_m should be set to around 11 kHz to account for component variations.

The resistor R_{DTR} is used to determine Δf, which is the amount of dithering, and its value is determined according to:

$$R_{DTR}\,(\Omega) = \frac{0.513 \times R_{FRS}\,(\Omega)}{\%DTHR} \quad (4)$$

For example, a 13.2% dithering with a nominal switching frequency of 250 kHz results in frequency variation of ±33 kHz.

7.3.4.6 SST and Soft-Start of the Switcher

Converters require a soft-start on the voltage error amplifier to prevent output overshoot on startup. In PoE applications, the PD also needs soft-start to limit its input current at turnon below the limit allocated by the power source equipment (PSE).

The TPS23755 provides primary side closed loop controlled soft-start, which applies a slowly rising ramp voltage to a second control input of the error amplifier. The lower of the reference input and soft-start ramps controls the error amplifier, allowing the output voltage to rise in a smooth monotonic fashion.

The soft-start period of the TPS23755 is internally set to a nominal value of 16 ms.

7.3.4.7 AUX_V, AUX_D and Secondary Adapter Or'ing

The TPS23755's unique auxiliary power detect capability provides priority for a secondary side power adapter, while ensuring smooth transition to and from the PoE power. This can be applied for example in applications where the auxiliary power is the main power, while the PoE input acts as the backup power. The auxiliary voltage is "Ore'd" directly at the output of flyback transformer, on secondary side. See 図 7-4 below where the output voltage is nominally 12 V.

When the auxiliary is present, a signal (AUX_D) tells the PD PWM to lower its output voltage slightly below the auxiliary voltage to ensure the auxiliary has priority to power the main output. When the auxiliary power goes away, the DC-DC converter increases back its output voltage, to ensure seamless transition. One significant advantage of this approach is that the efficiency of the PoE-powered flyback power stage can be optimized independently of the need for seamless transition. The adjustability of the lower voltage level allows the use of highly inaccurate auxiliary voltage sources. Such feature eases the thermal design, in particular when secondary diode rectification is used, since when PoE powered, the flyback stage can deliver power at a higher output voltage, and hence at a lower output current.

In 図 7-4 below, R_{OUT1} ensures that the PSE maintains power while the auxiliary is present, ensuring there will be no power interruption when the auxiliary power is removed.

The lower voltage level is programmable with the R_{AUX} resistor, which impacts the feedback network division ratio. Note however that the flyback power transformer design and resistor selection must be such that V_{VCC} will remain above nominally 6.1 V (V_{CUVF}) while the auxiliary power is present.

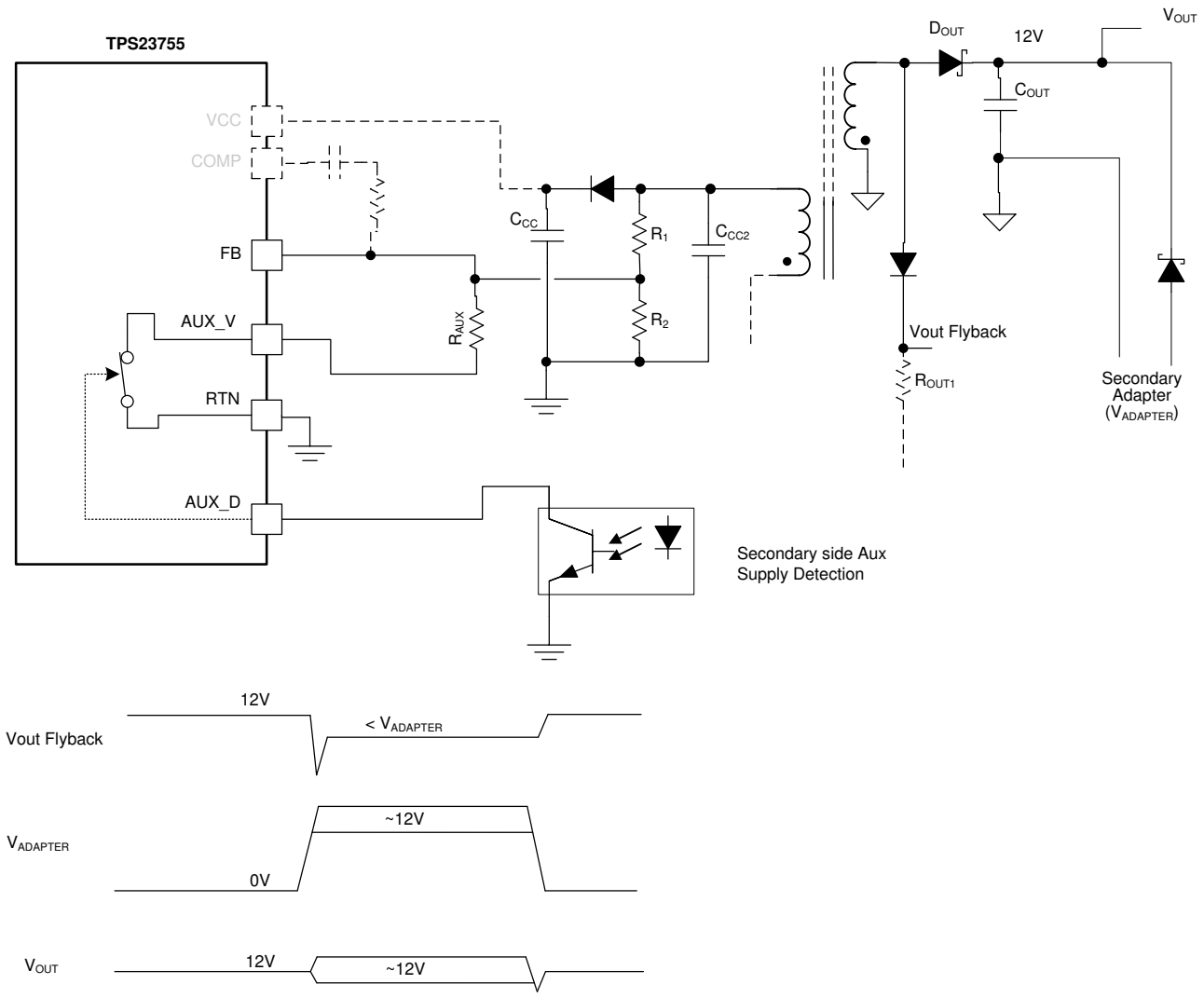


図 7-4. Secondary Side Priority Control with Smooth Transition

7.3.5 Internal Switching FET - DRAIN, RSNS, SRF and SRR

The DRAIN and RSNS provide connection to the drain and source of the integrated switching power FET. RSNS pin is a high current pin and it must have a short connection to the current sense resistor which other end is directly tied to a plane referenced to the GND pin. Current sensing is done with CS pin, which should be connected directly to the high side of the current sense resistor.

The internal FET gate driver is powered from VB voltage rail and the return path is through the GND pin. SRF and SRR pins provide slew rate control of the switching FET. The gate sourcing current is drawn through the SRF pin which is tied to VB pin through a resistor (0-100 Ω). The gate sinking current circulates through the SRR pin which is externally tied to the GND pin either via a low-value resistor (0-15 Ω) or a direct connection.

7.3.6 VPD Supply Voltage

VPD pin connects to the positive side of the input supply. It provides operating power to the PD controller and allows monitoring of the input line voltage. If V_{VPD} falls below its UVLO threshold and goes back above it, or if a thermal shutdown resumes while V_{VPD} is already above its UVLO threshold, the TPS23755 returns to inrush limiting.

7.3.7 VDD Supply Voltage

VDD connects to the source of DC-DC converter startup current. It is connected to VPD for most applications. It may also be isolated by a diode from VPD to support some PoE priority operation.

7.3.8 GND

GND is the power ground used by the flyback power FET gate driver and CP pin. Connect to the RTN plane. VB bypassing capacitor should be directly connected to the GND pin.

7.3.9 VSS

VSS is the PoE input-power return side. It is the reference for the PoE interface circuits, and has a current-limited hotswap switch that connects it to RTN. VSS is clamped to a diode drop above RTN by the hotswap switch. The exposed thermal PAD must be connected to this pin to ensure proper operation.

7.3.10 Exposed Thermal PAD

The exposed thermal PAD is internally connected to VSS pin. It should be tied to a large VSS copper area on the PCB to provide a low resistance thermal path to the circuit board. TI recommends maintaining a clearance of 0.025” between VSS and high-voltage signals such as VPD and VDD.

7.4 Device Functional Modes

7.4.1 PoE Overview

The following text is intended as an aid in understanding the operation of the TPS23755, but it is not a substitute for the actual IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification.

Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a Type 1 device, and devices with high power or enhanced classification is referred to as Type 2 devices. The TPS23755 is intended to power Type 1 devices (up to 13 W), and is fully compliant to IEEE 802.3at for hardware classes 0 - 3. Standards change and must always be referenced when making design decisions.

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable, and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as (hardware) classification. Only Type 2 PSEs are required to do hardware classification. The PD may return the default 13-W current-encoded class, or one of four other choices. The PSE may then power the PD if it has adequate capacity. Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. 図 7-5 shows the operational states as a function of PD input voltage.

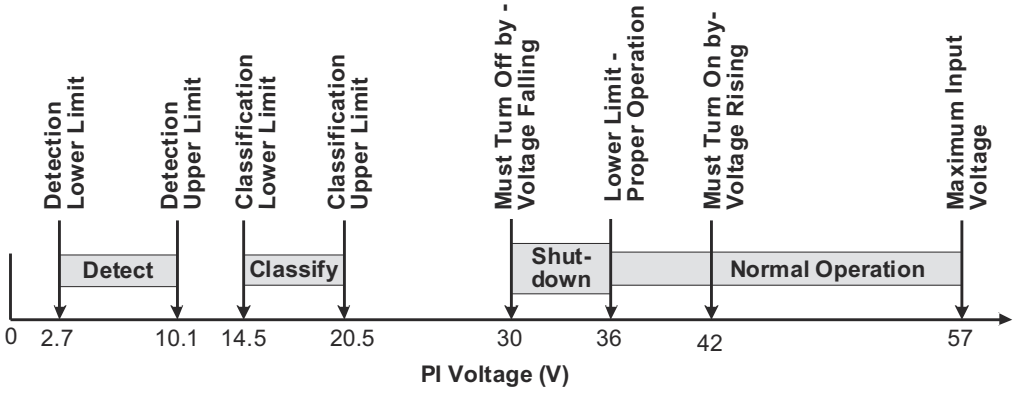


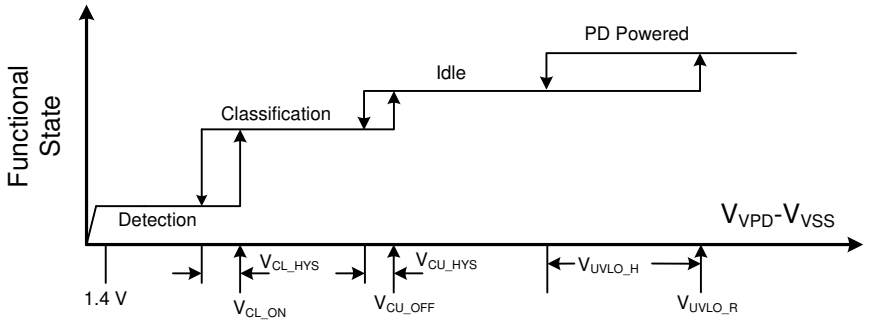
図 7-5. Operational States

The PD input is typically an RJ-45 eight-lead connector which is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable and operating margin. The IEEE 802.3at standard uses a cable resistance of 20 Ω for Type 1 devices to derive the voltage limits at the PD based on the PSE output voltage requirements. Although the standard specifies an output power of 15.4 W at the PSE, only 13 W is available at the PI due to the worst-case power loss in the cable. The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). Power application to the same pin combinations in 1000baseT systems is recognized in IEEE 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23755 specifications.

The PSE is permitted to disconnect a PD if it draws more than its maximum class power over a one second interval. A Type 1 PSE compliant to IEEE 802.3at is required to limit current to between 400 mA and 450 mA during powered operation, and it must disconnect the PD if it draws this current for more than 75 ms. Class 0 and 3 PDs may draw up to 400-mA peak currents for up to 50 ms. The PSE may set lower output current limits based on the declared power requirements of the PD.

7.4.2 Threshold Voltages

The TPS23755 has a number of internal comparators with hysteresis for stable switching between the various states as shown in 図 7-5. 図 7-6 relates the parameters in *Electrical Characteristics: DC-DC Controller Section* and *Electrical Characteristics: PoE and Control* to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance.



Note: Variable names refer to Electrical Characteristic Table parameters

図 7-6. Threshold Voltages

7.4.3 PoE Start-Up Sequence

The waveforms of 図 7-7 demonstrate detection, classification, and start-up from a Type 1 PSE. The key waveforms shown are $V_{VPD-VSS}$, $V_{RTN-VSS}$, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels; however, four levels are shown in this example. Four levels guard against misdetection of a device when plugged in during the detection sequence.

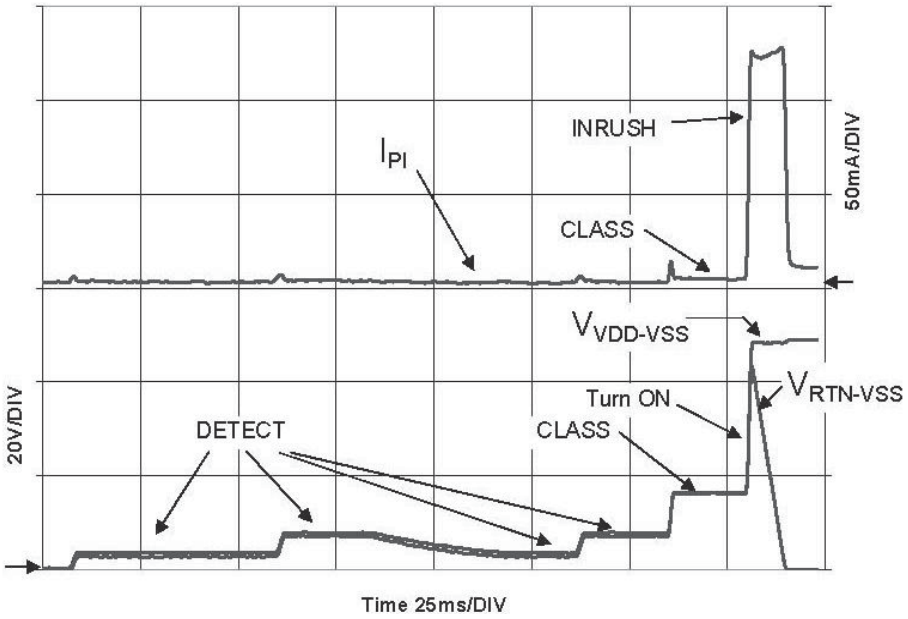


図 7-7. PoE Start-Up Sequence

7.4.4 Detection

The TPS23755 is in detection mode whenever $V_{VPD-V\ SS}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, almost all the internal circuits are disabled, and the DEN pin is pulled to V_{SS}. An R_{DEN} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and the TPS23755 bias loading. The incremental resistance of the input diode bridge may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the effective resistance of the TPS23755 during detection.

7.4.5 Hardware Classification

Hardware classification allows a PSE to determine the power requirements of a PD before starting, and helps with power management once power is applied. The maximum power entries in 表 7-1 determine the class the PD must advertise. A Type 1 PD may not advertise Class 4. The PSE may disconnect a PD if it draws more than its stated Class power. The standard permits the PD to draw limited current peaks; however, the average power requirement always applies.

Voltage from 14.5 V to 20.5 V is applied to the PD for up to 75 ms during hardware classification. A fixed output voltage is sourced by the CLS pin, causing a fixed current to be drawn from VPD through R_{CLS}. The total current drawn from the PSE during classification is the sum of bias and R_{CLS} currents. PD current is measured and decoded by the PSE to determine which of the five available classes is advertised (see Table 7-1). The TPS23755 disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limit or when DEN is active. The CLS output is inherently current-limited, but should not be shorted to VSS for long periods of time.

7.4.6 Maintain Power Signature (MPS)

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum DC current of 10 mA (at a duty cycle of at least 75 ms on every 225 ms) and an AC impedance lower than 26.25 kΩ in parallel with 0.05 µF. The AC impedance is usually accomplished by the minimum C_{BULK} requirement of 5 µF. When DEN is used to force the hotswap switch off,

the DC MPS is not met. A PSE that monitors the DC MPS will remove power from the PD when this occurs. A PSE that monitors only the AC MPS may remove power from the PD.

7.4.7 Start-Up and Converter Operation

The internal PoE undervoltage lockout (UVLO) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits discharges C_{DD}, C_{CC}, and C_{VB} while the PD is unpowered. Thus $V_{VDD-RTN}$ will be a small voltage until just after full voltage is applied to the PD, as seen in 図 7-7.

The PSE drives the PD input voltage to the operating range once it has decided to power up the PD. When V_{PD} rises above the UVLO turnon threshold (V_{UVLO-R}, approximately 35.5 V) with RTN high, the TPS23755 enables the hotswap MOSFET with an approximately 140-mA (inrush) current limit. See the waveforms of 図 7-8 for an example. Converter switching is disabled while C_{DD} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}; however, the converter start-up circuit is allowed to charge C_{CC}. Once the inrush current falls about 10% below the inrush current limit, the PD control switches to the operational level (approximately 450 mA) and converter switching is permitted.

Converter switching is allowed if the PD is not in inrush current limit and the VCC under-voltage lockout (V_{CUVR}) circuit permits it. Continuing the start-up sequence shown in Figurer 7-7, V_{VCC} rises as the start-up current source charges C_{CC} and the converter switching is inhibited by the status of the VCC UVLO. The VB regulator powers the internal converter circuits as V_{VCC} rises.

Once V_{VCC} goes above its UVLO (nominally 8.25 V), the converter switching is enabled following the closed loop controlled soft-start sequence. Note that the startup current source capability is such that it can fully maintain V_{VCC} during the converter soft-start without requiring any significant C_{CC} capacitance, in 48 V input applications. At the end of the soft-start period, the startup current source is turned off. V_{VCC} falls as it powers the internal circuits including the switching MOSFET gate. If the converter control-bias output rises to support V_{VCC} before it falls to V_{CUVF} (nominally 6.1 V), a successful start-up occurs. Figure 7-7 shows a small droop in V_{VCC} while the output voltage rises smoothly and a successful start-up occurs.

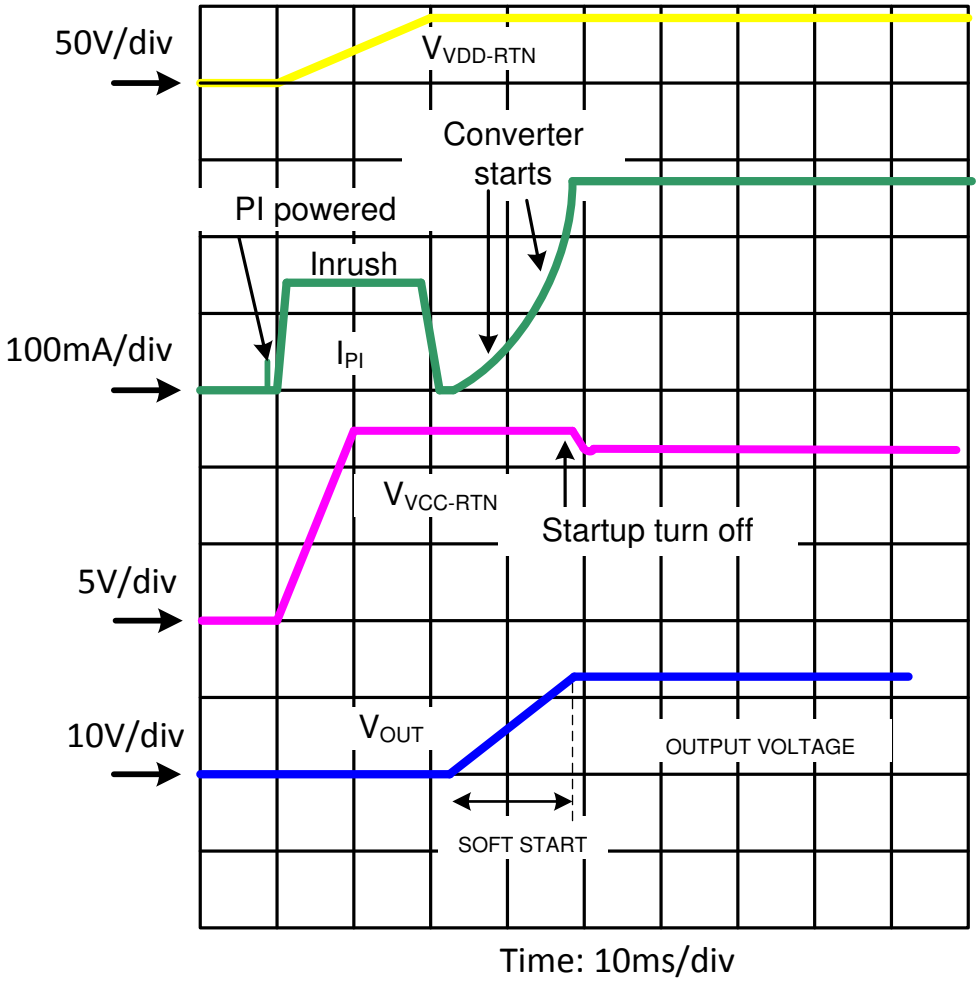


図 7-8. Power Up and Start

The converter shuts off when V_{VCC} falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers VCC. The control circuit discharges VCC until it hits the lower UVLO and turns off. A restart initiates if the converter turns off and there is sufficient VDD voltage. This type of operation is sometimes referred to as *hiccup mode*, which when combined with the soft-start provides robust output short protection by providing time-average heating reduction of the output rectifier.

図 7-9 illustrates the situation when there is severe overload at the main output which causes VCC hiccup. After VCC went below its UVLO due to the overload, the startup source is turned back on. Then, a new soft-start cycle is reinitiated, introducing a short pause before the output voltage is ramped up.

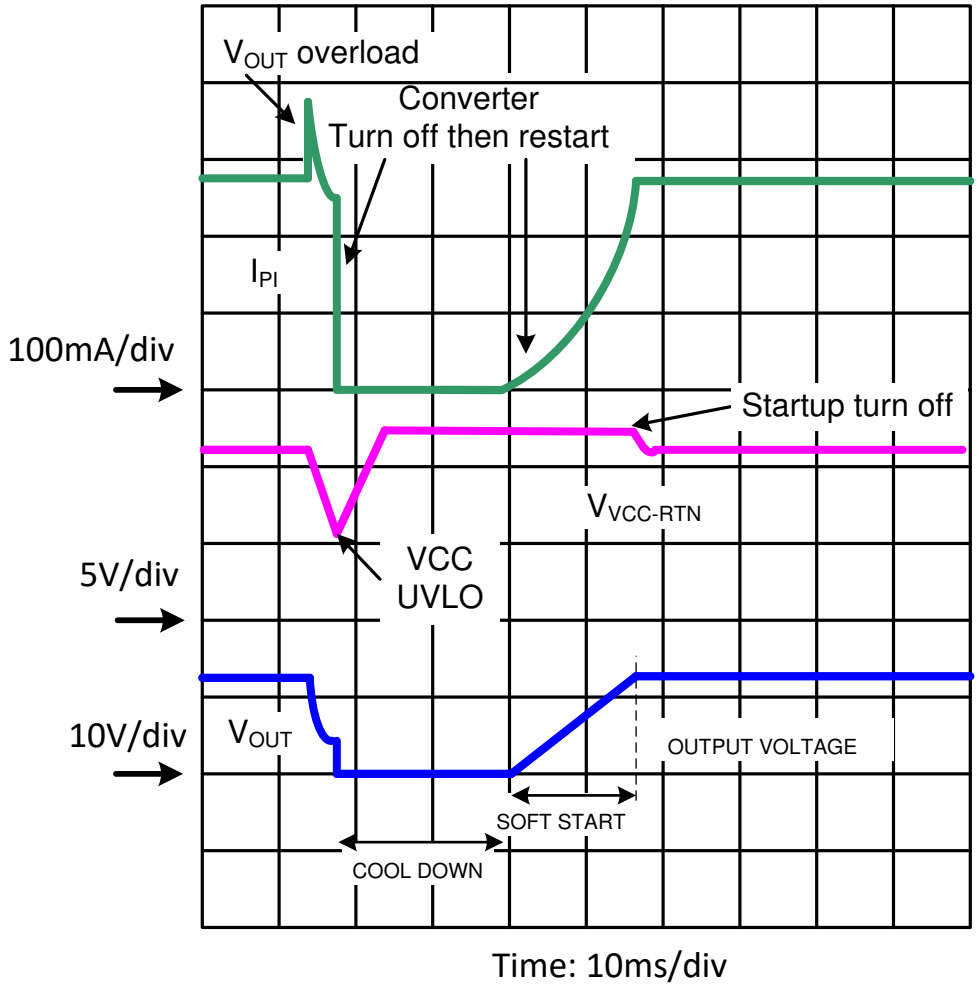


図 7-9. Restart Following Severe Overload at Main Output of Flyback DC-DC Converter

If $V_{VPD-VSS}$ drops below the lower PoE UVLO (UVLO_R – UVLO_H, approximately 31 V), the hotswap MOSFET is turned off, but the converter still runs. The converter stops if V_{VCC} falls below the V_{CUVF} (nominally 6.1 V), the hotswap is in inrush current limit, the SST pin is pulled to ground, $V_{VDD-RTN}$ falls below typically 7.7 V (approximately 0.75 V hysteresis) or the converter is in thermal shutdown.

7.4.8 PD Self-Protection

The PD section has the following self-protection functions.

- Hotswap switch current limit
- Hotswap switch foldback
- Hotswap thermal protection

The internal hotswap MOSFET is protected against output faults with a current limit and deglitched foldback. The PSE output cannot be relied on to protect the PD MOSFET against transient conditions, requiring the PD to provide fault protection. High stress conditions include converter output shorts, shorts from VDD to RTN, or transients on the input line. An overload on the pass MOSFET engages the current limit, with $V_{RTN-VSS}$ rising as a result. If V_{RTN} rises above approximately 12.3 V for longer than approximately 400 µs, the current limit reverts to the inrush limit, and turns the converter off. The 400-µs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. 図 7-10 shows an example of recovery from a 15-V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to 420 mA, full-current limit, and charges the input

capacitor while the converter continues to run. The MOSFET did not go into foldback because $V_{RTN-VSS}$ was below 12 V after the 400-µs deglitch.

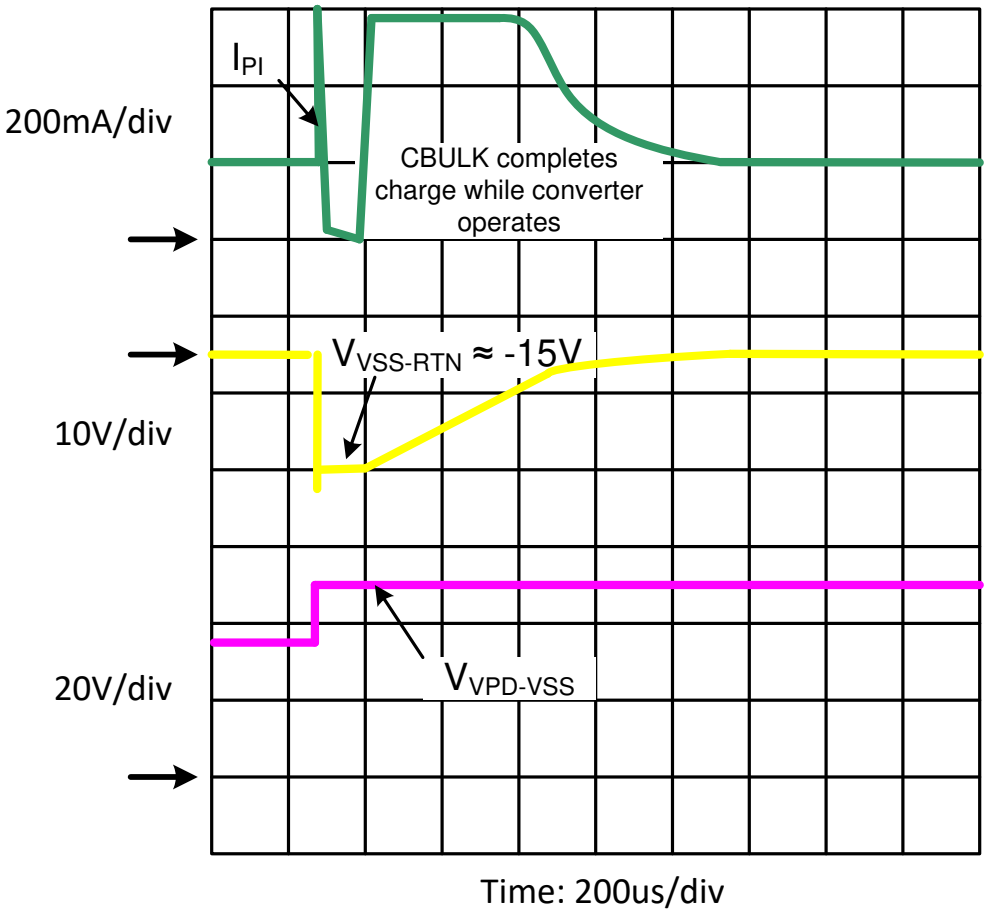


図 7-10. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like start-up or operation into a VPD to RTN short cause high power dissipation in the MOSFET. An overtemperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The PD restarts in inrush current limit when exiting from a PD overtemperature event.

Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with secondary-side adapter ORing to achieve adapter priority. Take care with synchronous converter topologies that can deliver power in both directions.

The hotswap switch is forced off under the following conditions:

- $V_{DE\ N} \leq V_{PD\_DIS}$ when $V_{VPD-VSS}$ is in the operational range
- PD over temperature
- $V_{VPD-VSS}$ < PoE UVLO (approximately 31 V)

7.4.9 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS23755 device supports forced operation from either of the power sources. 図 7-11 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the device input, option 2 applies power between the device PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and

disadvantages. Many of the basic ORing configurations and much of the discussion contained in the application note *Advanced Adapter ORing Solutions using the TPS23753*, (SLVA306), apply to the TPS23755.

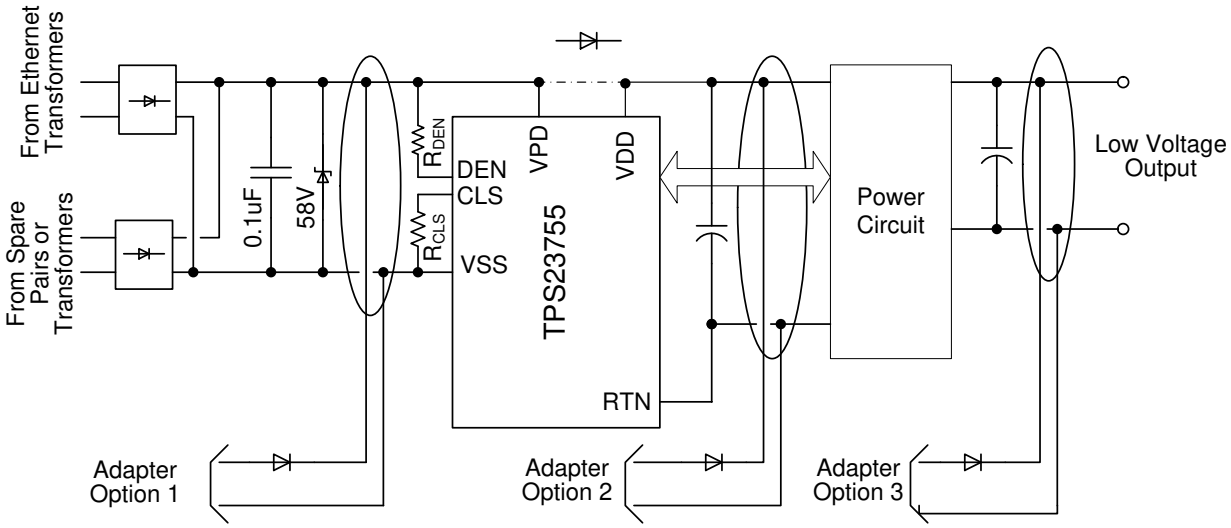


図 7-11. ORing Configurations

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors contributing to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, PD inrush, and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However, the TPS23755 device offers several built-in features that simplify some combinations.

Several examples demonstrate the limitations inherent in ORing solutions. Diode ORing a 48-V adapter with PoE (option 1) presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12-V adapter with PoE using option 2. The converter draws approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{BULK} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12-V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If adapter power is then lost, the PD stops operating until the PSE detects and powers the PD.

The TPS23755 has a unique feature that can be used to achieve seamless transition while applying option 3. It provides adapter priority by reducing the DC-DC output voltage when the adapter voltage is present. An optocoupler is typically driven from the secondary side of the converter when the adapter voltage is present, which commands the converter voltage to go down to a predetermined voltage level, by use of pins AUX_D and AUX_V. This voltage level is lower than the minimum adapter voltage to ensure priority. The DC-DC converter stays in operation, which with appropriate minimum loading can ensure the PSE power will be maintained, to ensure there will be no output power interruption next time the adapter voltage goes down.

The IEEE standards require that the PI conductors be electrically isolated from ground and all other system potentials not part of the PI interface. The adapter must meet a minimum 1500-Vac dielectric withstand test between the output and all other connections for options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse-voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS23755 supports power supply topologies that require a single PWM gate drive with current-mode control. 図 8-1 provides an example of a simple diode rectified primary-side-regulated flyback converter.

8.2 Typical Application

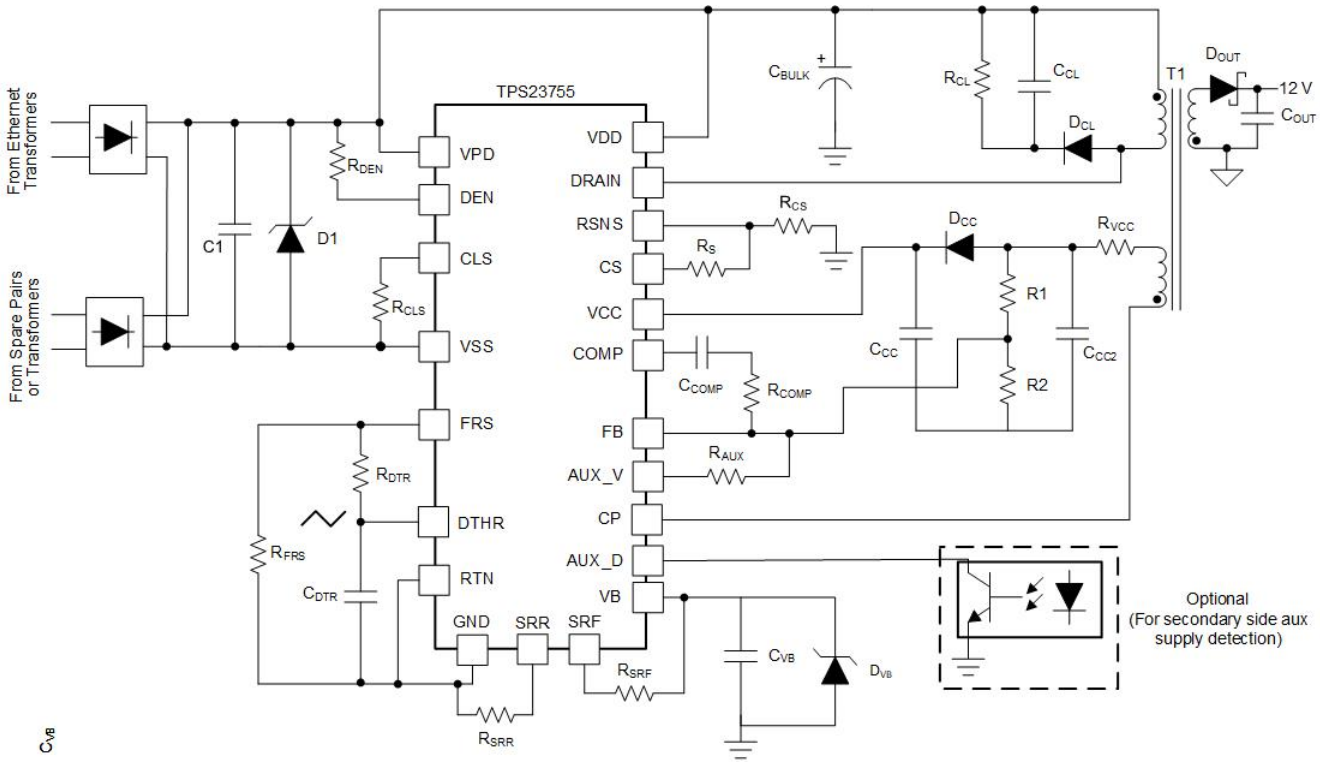


図 8-1. Basic TPS23755 Implementation

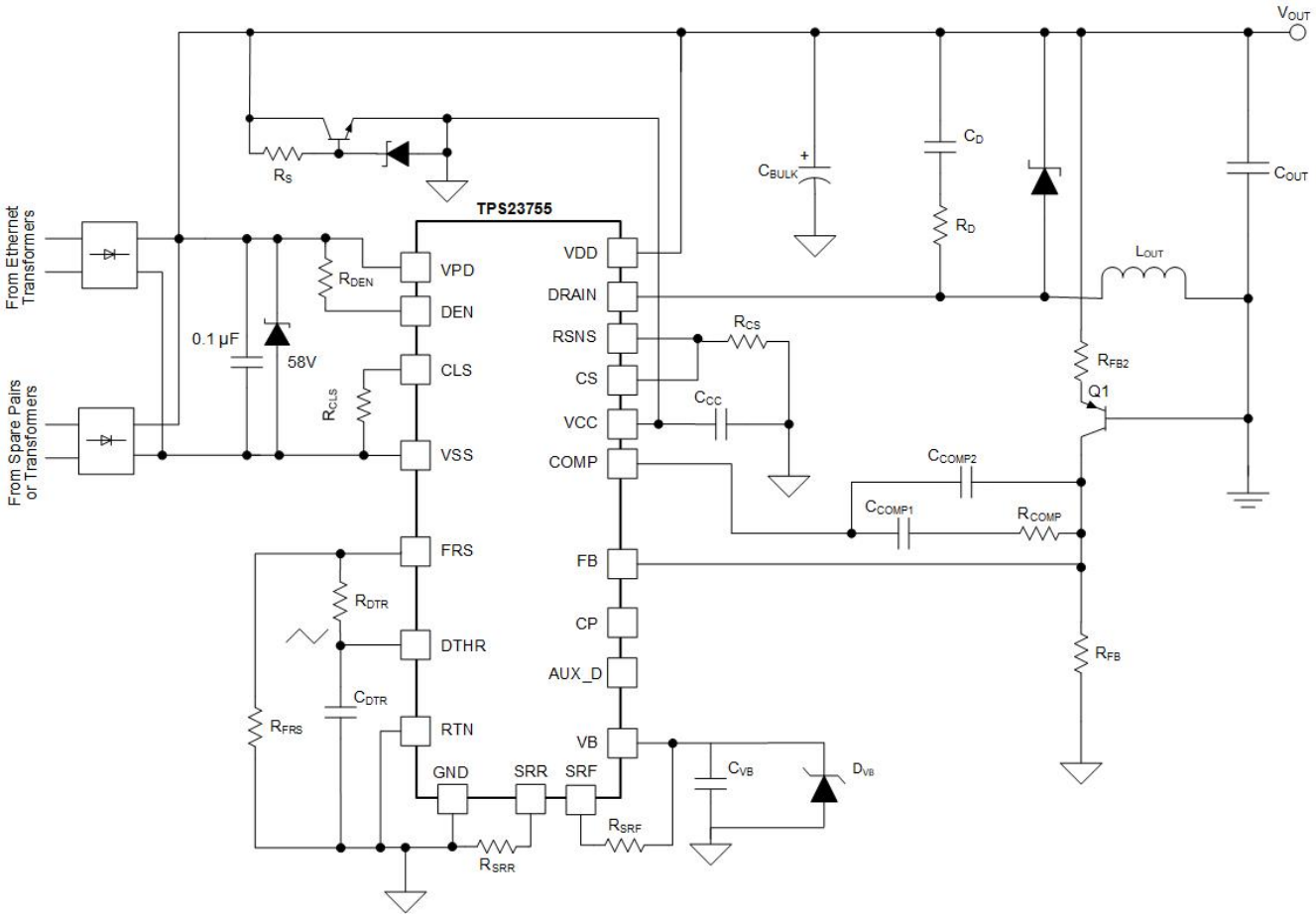


図 8-2. Simplified Buck Application

8.2.1 Design Requirements

Selecting a converter topology along with a design procedure is beyond the scope of this applications section. The TPS23755 is optimized for primary-side-regulated diode rectified flyback topologies for 12 V outputs or higher due to its good balance of high efficiency and output regulation. Typical applications use post regulation to power the system load's lower voltage rails . The TPS23755 can also be used in non-isolated buck topology application like shown in Figure 8-1.

Examples to help in programming the TPS23755 in a primary-side regulated flyback are shown below. For more specific converter design examples refer to the TPS23755EVM-894 EVM: Evaluation Module for TPS23755.

表 8-1. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER INTERFACE					
Input voltage	Applied to the PoE Input	37		57	V
	Applied to the Secondary Input		12		V
Detection voltage	At device terminals	2.7		10.1	V
Classification voltage	At device terminals	14.5		20.5	V
Classification current	R_{CLASS} = 45.3 Ω	26.5		29.3	mA
Inrush current-limit			140		mA
Operating current-limit			550		mA
DC-TO-DC CONVERTER					
Output voltage	V_{IN} = 48 V, $I_{LOAD} \le I_{LOAD}$ (max)		12		V

表 8-1. Design Parameters (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current	37 V ≤ V_{IN} ≤ 57 V		1		A
Output ripple voltage peak-to-peak	V_{IN} = 48 V, I_{LOAD} = 1 A		50		mV
Efficiency, end-to-end	V_{IN} = 48 V, I_{LOAD}= 100 mA		78		%
	V_{IN} = 48 V, I_{LOAD} = 500 mA		86		
	V_{IN} = 48 V, I_{LOAD} = 1 A		87		
Switching frequency			250		kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges reduces the power dissipation in these devices by about 30%. There are, however, some things to consider when using them. The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. To compensate, use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges.

Schottky diode leakage currents and lower dynamic resistances can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing RDEN slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. Care must be taken to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

As a general recommendation, use 0.8 A-1 A, 100-V rated discrete or bridge diodes for the input rectifiers.

8.2.2.2 Protection, D_1

A TVS, D_1, across the rectified PoE voltage per 図 8-1 must be used. A SMAJ58A, or equivalent, is recommended for general indoor applications. Adequate capacitive filtering or a TVS must limit input transient voltage to within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

8.2.2.3 Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from VDD to VSS) of 0.05 µF to 0.12 µF. Typically a 0.1-µF, 100-V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.7 kΩ and 26.3 kΩ, or 25 kΩ ± 5%. Typically a 24.9 kΩ ± 1% is used.

8.2.2.5 Classification Resistor, R_{CLS}

Connect a resistor from CLS to VSS to program the classification current according to the IEEE 802.3at standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to 表 7-1. For Class 3 applications, it is recommended to unpopulate R_{CLS}. A compliant PSE will allocate 13 W to either a Class 0 or a Class 3 compliant PD with no difference in PoE system performance.

8.2.2.6 Bulk Capacitance, C_{BULK}

The bulk capacitance, C_{BULK} must furnish input transients during heavy loads and long cable length conditions. It also helps with stability on the DC/DC converter. It is recommended to use a minimum 10-uF, electrolytic capacitor.

8.2.2.7 Output Voltage Feedback Divider, R_{AUX}, R_1,R_2

R_1, R_2 and R_{AUX} set the output voltage of the bias winding of the converter. For applications that do not use AUX_D functionality, R_{AUX} should not be populated and 式 5 should be used.

$$V_{VCC} = \frac{V_{REFC}\left(R_1 + R_2\right)}{R_2} \tag{5}$$

For secondary side adapter priority applications, the DC/DC output voltage can be set lower than the adapter voltage by pulling AUX_D to RTN. 式 6 should be used first to determine the lower output voltage when adapter is present.

$$V_{VCC} = \frac{V_{REFC}\left(R_1 + R_2\right)}{R_2} \tag{6}$$

when Aux_D is LOW.

Then R_{aux} can be calculated using 式 7 to set the nominal output voltage of the bias winding.

$$V_{VCC} = \frac{V_{REFC}\left(R_1 R_{AUX} + R_1 R_2 + R_2 R_{Aux}\right)}{R_2 R_{AUX}} \tag{7}$$

when Aux_D is HIGH.

When transitioning from the normal operating output voltage to a lower output voltage when Aux_D is pulled LOW, switching may stop until the VCC voltage can reduce its voltage to the lower VCC voltage. The output voltage may drop during this time due to the loss of switching. Typically this is not a concern since the adapter is providing power to the load. A combination of adding a dummy load in parallel with C_{CC} and increasing the secondary output capacitance can minimize the time that switching stops.

In applications that use smooth transition between adapter the PoE, circuitry should be added to keep the PSE connected to the PD and the converter operational while maintaining adapter priority. It is recommended to refer to the TPS23755EVM-894.

8.2.2.8 Setting Frequency, R_{FRS}

The converter switching frequency in PWM mode is set by connecting resistor, R_{FRS} from the FRS pin to RTN. For a converter that requires a 250-kHz switching frequency and using 式 8

$$R_{FRS}\left(k\Omega\right) = \frac{15000}{f_{SW}\left(kHz\right)} = \frac{15000}{250\ kHz} = 60\ k\Omega \tag{8}$$

A standard 60.4-kΩ resistor should be used.

8.2.2.9 Frequency Dithering, R_{DTR} and C_{DTR}

For optimum EMI performance, C_{DTR} and R_{DTR} should be selected as described in *Frequency Dithering for Spread Spectrum Applications* in 式 9 and 式 10.

$$C_{DTR}\left(nF\right) = \frac{3 \Big/ R_{FRS}\left(\Omega\right)}{2.052 \times f_m\left(Hz\right)} = \frac{3 \Big/ 60.4\ k\Omega}{2.052 \times 11000\ Hz} = 2.2\ nF \tag{9}$$

$$R_{DTR}(\Omega) = \frac{0.513 \times R_{FRS}(\Omega)}{\%DTHR} = \frac{0.513 \times 60.4\,k\Omega}{0.132} = 235\ k\Omega \quad (10)$$

A standard 237-kΩ resistor should be used.

8.2.2.10 Bias Voltage, C_{VB} and D_{VB}

VB requires a 0.1 µF capacitor, C_{VB}, to RTN. D_{VB} , a 6.2V Zener diode to RTN, is also required.

Note: D_{VB} on VB is optional in 13W applications when no class resistor is used.

8.2.2.11 Transformer design, T_1

The turns ratio and primary inductance are important parameters to consider in a flyback transformer. The turns ratio act to limit the max duty cycle and reduce stress on the secondary components while the primary inductance sets the current ripple. In CCM operation, the higher inductance allows for a reduced current ripple which can help with EMI performance and noise.

For primary-side regulated flyback converters, the transformer construction is important to maintain good regulation on the secondary output. It is recommended to use LDT0950 for 12-V applications.

8.2.2.12 Current Sense Resistor, R_{CS}

R_{CS} should be chosen based on the peak primary current at the desired output current limit.

$$R_{CS} = \frac{V_{CSMAX}}{I_{Pk-Primary}} \quad (11)$$

8.2.2.13 Current Slope Compensation, R_S

R_S may be used if the internally provided slope compensation is not enough. The down slope of the reflected secondary current through the current sense resistor at each switching period is determined and a percentage (typically 50%-75%) of it will define V_{slope}. If necessary, using LDT0950, it is recommended to start with 251 mV and use 式 12.

$$R_S(\Omega) = \frac{\left[V_{SLOPE_D}(mV) - \left(\frac{V_{SLOPE}(mV)}{D_{MAX}}\right)\right]}{\frac{I_{SL_{EX}}(\mu A)}{D_{MAX}}} \times 1000 = \frac{\left[251\,mV - \left(\frac{155\ mV}{78.5\%}\right)\right]}{\frac{42\ \mu A}{78.5\%}} \times 1000 = 1\,k\Omega \quad (12)$$

8.2.2.14 Bias Supply Requirements, C_{CC}, D_{CC}

Advanced startup in the TPS23755 allows for relatively low capacitance on the bias circuit. It is recommended to use a 1-uF, 10%, 25-V ceramic capacitors on C_{CC}. D_{CC} can be a low cost, general-purpose diode. It is recommended to use MMSD4148 diode (100 V, 200 mA).

8.2.2.15 Switching Transformer Considerations, R_{VCC} and C_{CC2}

R_{VCC} helps to reduce peak charging from the bias winding. Reduced peak charging becomes especially important when tuning hiccup mode operation during output overload. A typical value for R_{VCC} in Class 3 PoE PD applications while maintaining a suitable load regulation is 10 ohms.

8.2.2.16 Primary FET Clamping, R_{CL}, C_{CL}, and D_{CL}

The stored energy in the leakage inductance of the power transformer can cause ringing during the primary FET turnoff. The snubber must be chosen to mitigate primary FET overshoot and oscillation while maintaining high overall efficiency.

It is recommended to use 39 kΩ (125 mW) for R_{CL} and 0.1 uF (100 V) for C_{CL}.

D_{CL} should be an ultra-fast diode with a short forward recovery time allowing the snubber to turn on quickly. The 200-V / 1-A rated diode with a recovery time approximately 25 ns or better is recommended.

8.2.2.17 Converter Output Capacitance, C_{OUT}

The output capacitor is considered as part of the overall stability of the converter, the output voltage ripple, and the load transient response. The output capacitor needs to be selected based on the most stringent of these criteria. The minimum capacitance is typically determined by the output voltage ripple shown in 式 13.

$$C_{OUT} > \frac{I_{OUT}(A) \times D_{max}}{V_{Ripple}(V) \times f_{SW}(Hz)} \tag{13}$$

where D_{max} is the calculated operating max duty cycle shown in 式 14.

$$D_{max} = \frac{V_{OUT} \times N_{PS}}{V_{IN}(min) + V_{OUT} \times N_{PS}} \tag{14}$$

For strict load transient requirements, the C_{OUT} cap may need to be increased. The TPS23755EVM-894 uses two 22 uF ceramic capacitors for an optimized load transient response.

8.2.2.18 Secondary Output Diode Rectifier, D_{OUT}

The output rectifier diode must provide low forward voltage drop at the secondary peak current. Consideration must be given to a safe operating area during output overload conditions.

For a 12 V output, PDS360-13 in a high thermal performance package (60 V reverse voltage, 3-A continuous current max, Vf = 0.62 V max at 3 A) is used in the TPS23755EVM-894.

8.2.2.19 Slew rate control, R_{SRF} and R_{SRR}

R_{SRF} and R_{SRR} minimize primary drain-source oscillations and help optimize EMI performance at high frequencies, the value chosen should be within the recommend operating conditions table in *Recommended Operating Conditions*. It is recommended to start with 10 ohms for R_{SRF} and 10 ohms for R_{SRR} then adjust accordingly during bench and EMI testing.

8.2.2.20 Shutdown at Low Temperatures, D_{VDD} and C_{VDD}

For applications operating near –10°C or less, there may be some extra switching cycles during removal of the PoE input or during shutdown. It is acceptable for most applications; however, for a more monotonic shutdown of the output voltage during power removal, it is recommended to use D_{VDD} and C_{VDD} as shown in 図 8-3. D_{VDD} can be MMSD4148 and C_{VDD} can be 0.22-uF, 100-V capacitor.

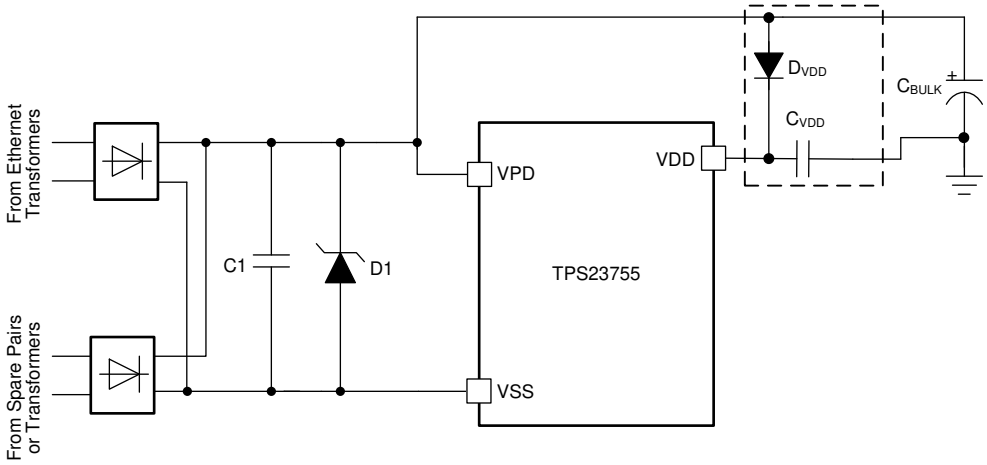


図 8-3. DVDD and CVDD Configuration for Low Temperature Conditions

8.2.3 Application Curves

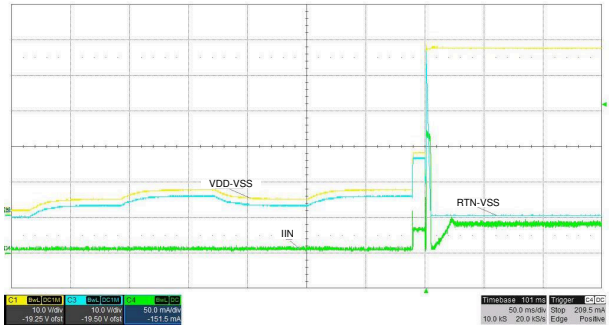


図 8-4. TPS23755 Startup to TPS23861 PSE

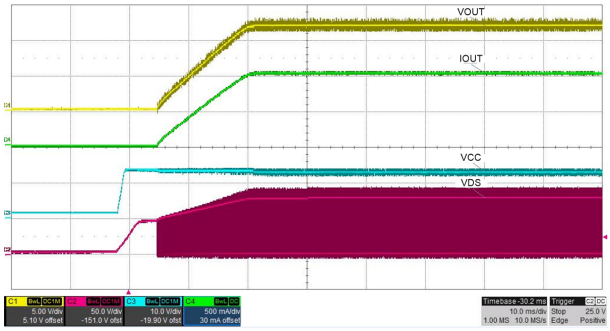


図 8-5. TPS23755 PSR Flyback Startup to Full Load

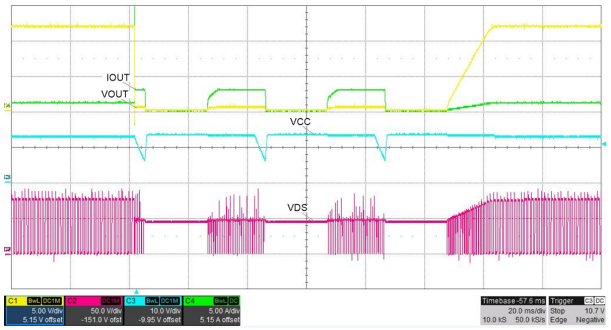


図 8-6. TPS23755 Output Short and Recovery

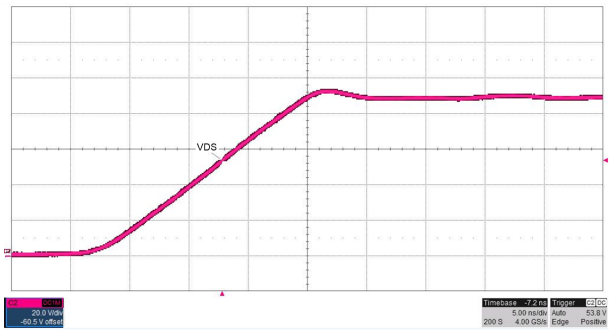


図 8-7. Slew Rate Adjust SRR = 15 Ω

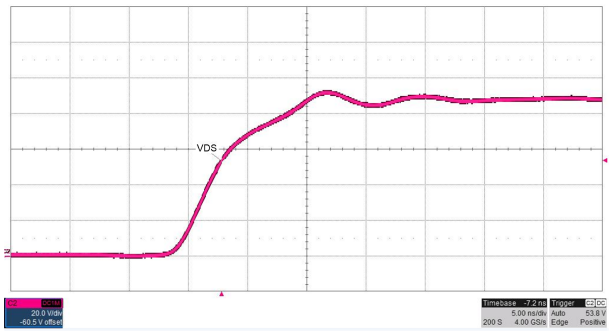


図 8-8. Slew Rate Adjust SRR = 0 Ω

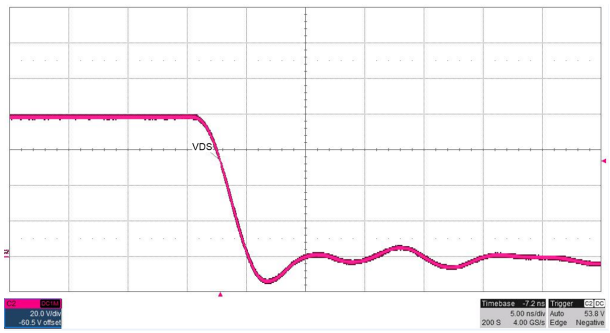


図 8-9. Slew Rate Adjust SRF = 0 Ω

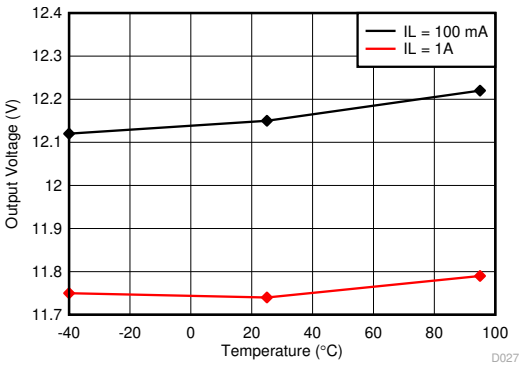


図 8-10. Output Regulation vs. Ambient Temperature

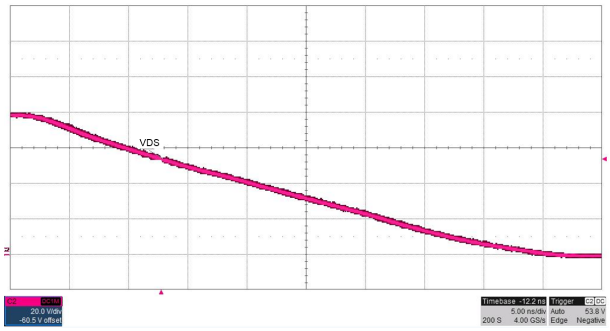


図 8-11. Slew Rate Adjust SRF = 100 Ω

9 Power Supply Recommendations

The TPS23755 converter should be designed such that the input voltage of the converter is capable of operating within the IEEE802.3at recommended input voltage as shown in 図 7-5 and the minimum operating voltage of the adapter if applicable.

10 Layout

10.1 Layout Guidelines

The TPS23755 IC's layout footprint shown in the Example Board Layout should be strictly followed. The below list are key highlights for layout consideration around the TPS23755.

- Pin 22 of the TPS23755 is omitted from the IC to ensure high voltage clearance from Pin 24 (DRAIN). Therefore, the Pin 22 footprint should be removed when laying out the TPS23755.
- It is recommended having at least 8 vias (VSS) connecting the exposed thermal pad through a top layer plane (2 oz copper recommended) to a bottom VSS plane (2 oz. copper recommended) to help with thermal dissipation.
- The Pin24 of the TPS23755 should be near the power transformer and the current sense resistor should be close to Pin 1 of the TPS23755 to minimize the primary loop.

The layout of the PoE front end should follow power and EMI or ESD best-practice guidelines. A basic set of recommendations includes:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1-µF capacitor, and TPS23755 converter input bulk capacitor.
- Make all leads as short as possible with wide power traces and paired signal and return.
- No crossovers of signals from one part of the flow to another are allowed.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- Use large copper fills and traces on SMT power-dissipating devices, and use wide traces or overlay copper fills in the power path.

The DC-to-DC converter layout benefits from basic rules such as:

- Having at least 4 vias (VDD) near the power transformer pin connected to VDD through multiple layer planes to help with thermal dissipation of the power transformer.
- Having at least 6 vias (secondary ground) near the power transformer pin connected to secondary ground through multiple layer planes to help with thermal dissipation of the power transformer.
- Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses, which include the power semiconductors and magnetics.
- Minimize the trace length of high current power semiconductors and magnetic components.
- Where possible, use vertical pairing.
- Use the ground plane for the switching currents carefully.
- Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
- Maintain proper spacing around the high-voltage sections of the converter.

10.2 Layout Example

図 10-1 and 図 10-2 show the top and bottom layer and assemblies of the TPS23755EVM-894 as a reference for optimum parts placement.

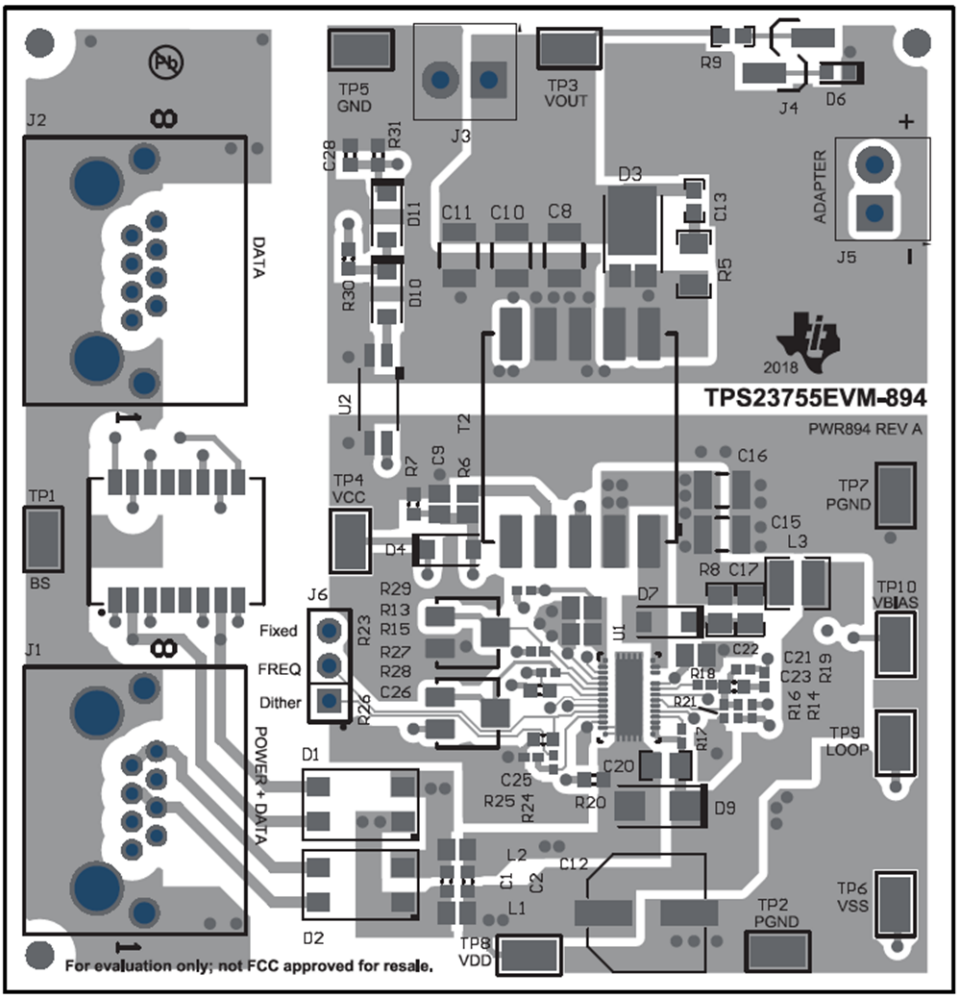


図 10-1. Top Side and Routing

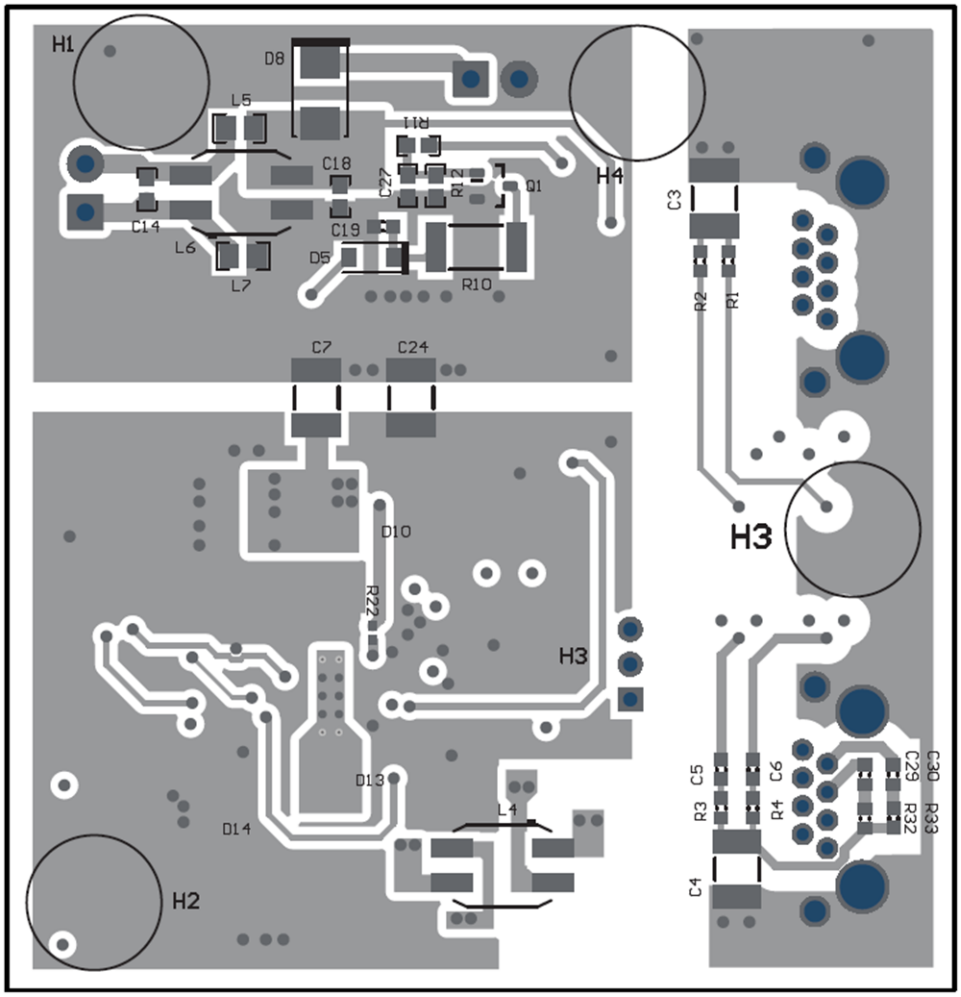


図 10-2. Bottom Side Placement and Routing

11 Device and Documentation Support

11.1 Related documentation

For related documentation, see the following:

- Texas Instruments, Practical Guidelines to Designing an EMI-Compliant PoE Powered Device With Isolated Flyback, application report
- Texas Instruments, TPS23755EVM-894: Evaluation Module, user's guide

11.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

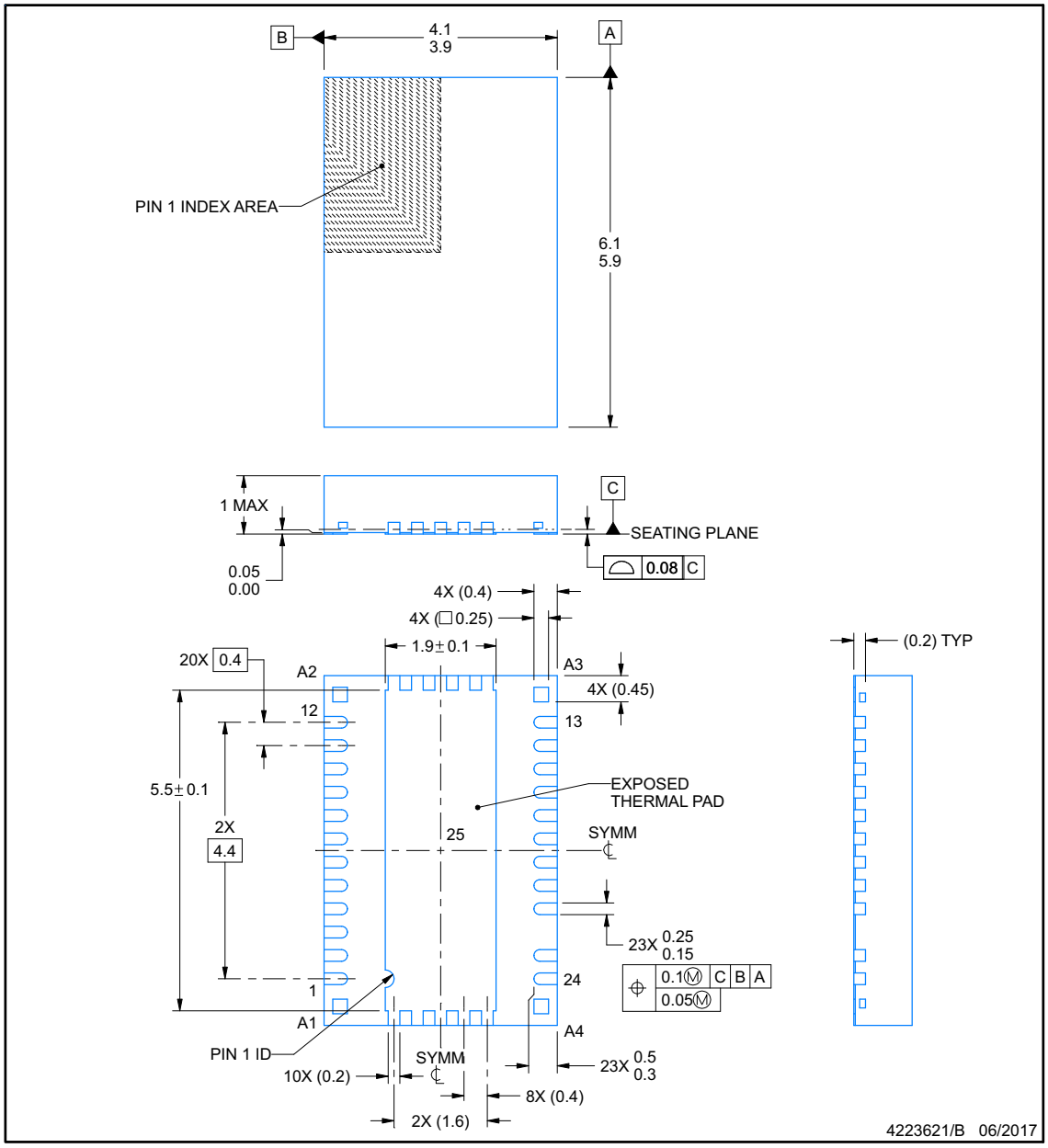
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RJJ0023B

VSON - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

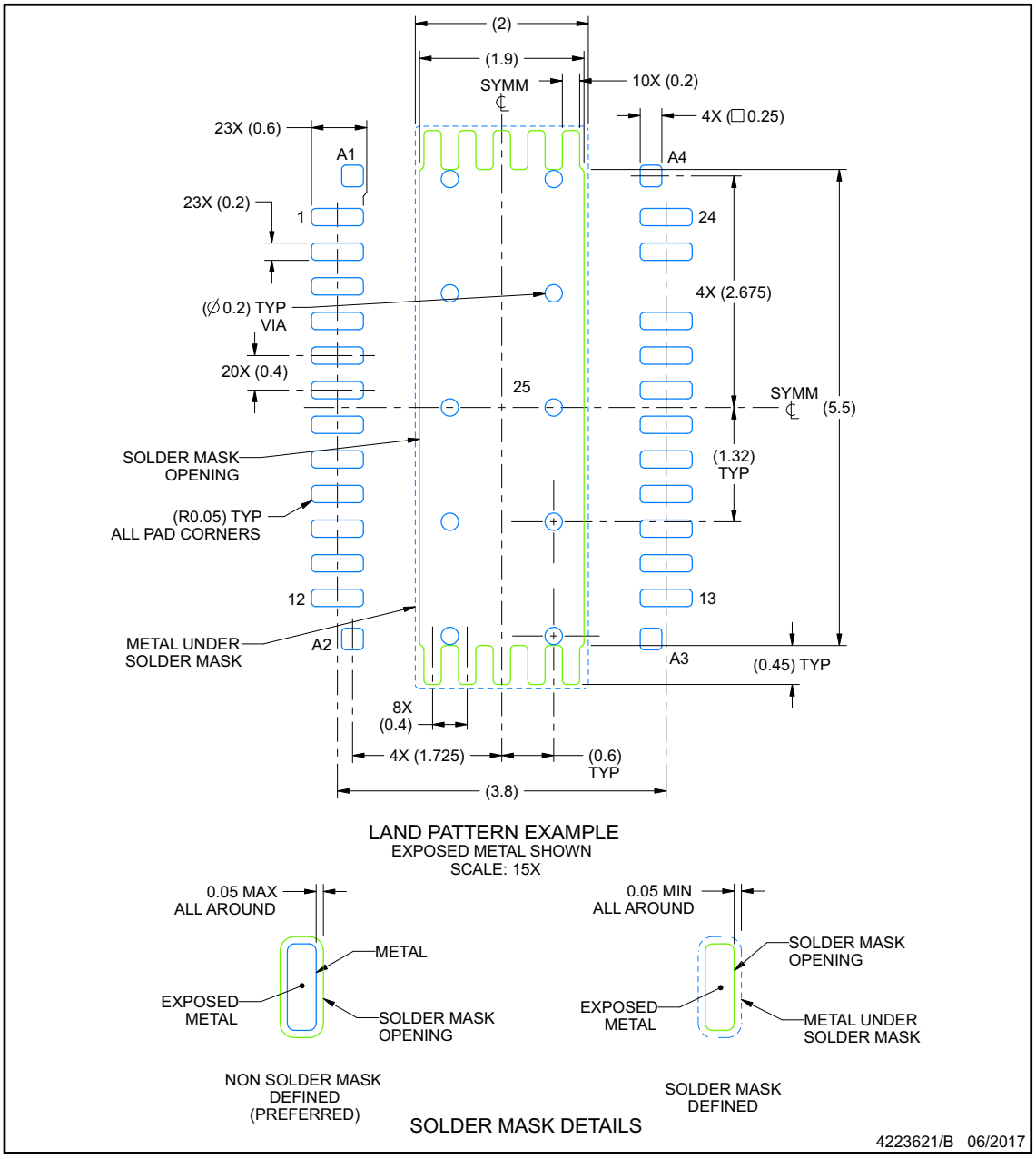
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RJJ0023B

VSON - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



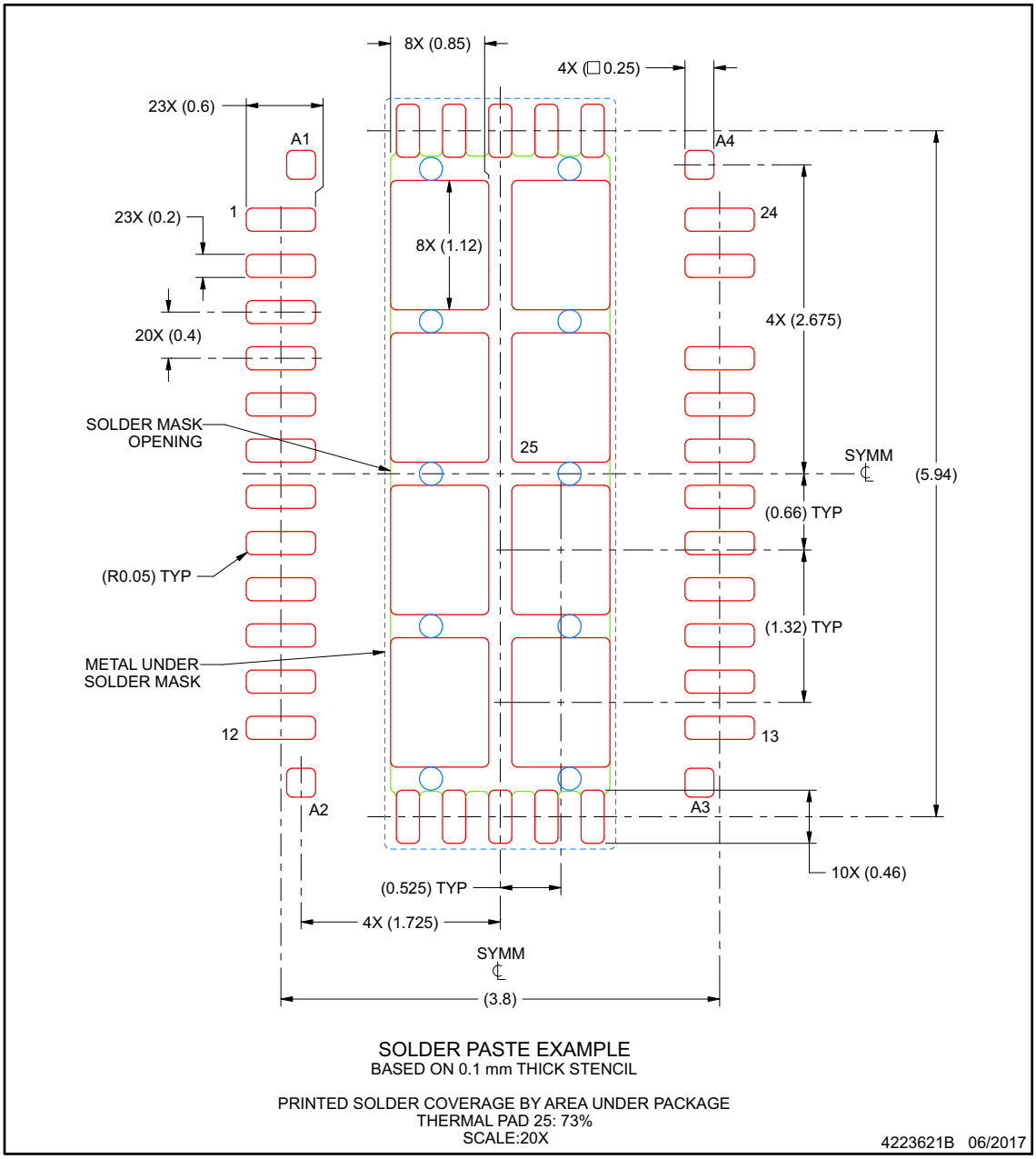
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RJJ0023B — **VSON - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
THERMAL PAD 25: 73%
SCALE:20X

4223621B 06/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS23755RJJR	Active	Production	VSON (RJJ) | 23	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS23755
TPS23755RJJR.Z	Active	Production	VSON (RJJ) | 23	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS23755
TPS23755RJJT	Active	Production	VSON (RJJ) | 23	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS23755
TPS23755RJJT.Z	Active	Production	VSON (RJJ) | 23	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS23755

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

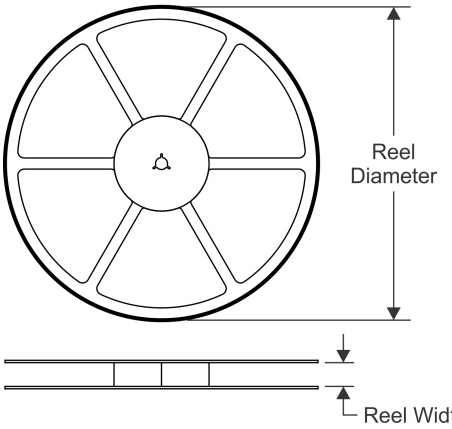
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

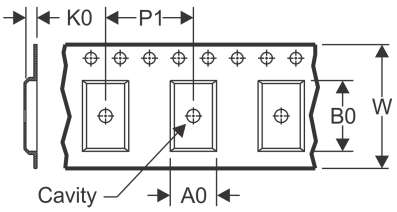
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

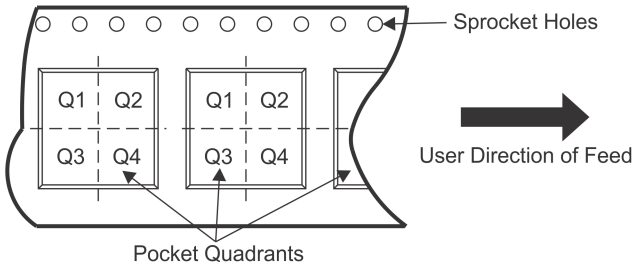


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

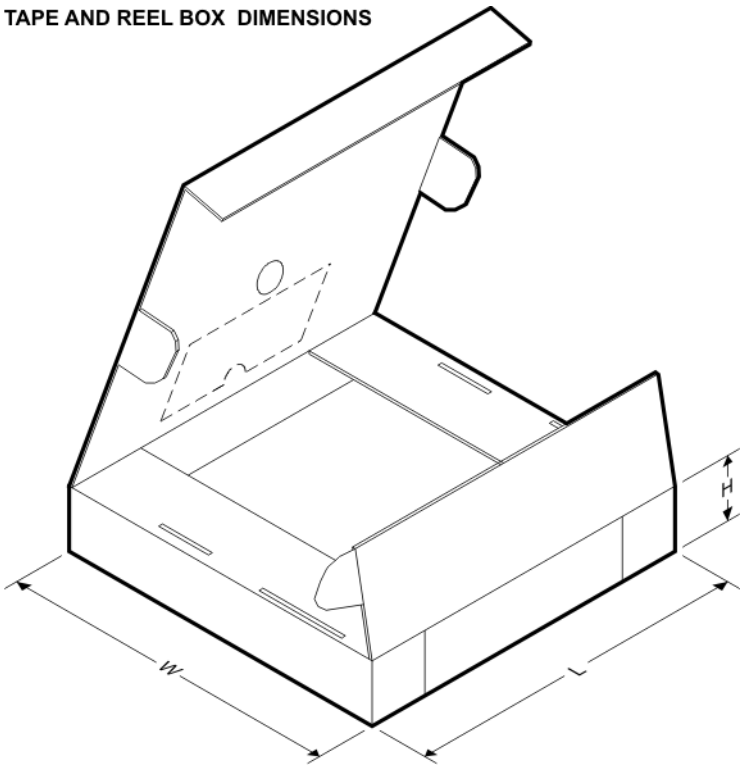
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23755RJJR	VSON	RJJ	23	3000	330.0	12.4	4.25	6.25	1.15	8.0	12.0	Q1
TPS23755RJJT	VSON	RJJ	23	250	180.0	12.4	4.25	6.25	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23755RJJR	VSON	RJJ	23	3000	367.0	367.0	38.0
TPS23755RJJT	VSON	RJJ	23	250	213.0	191.0	35.0

重要なお知らせと免責事項

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