TPS25750 USB Type-C® and USB PD Controller with Integrated Power Switches Optimized for Power Applications

1 Features

- Integrated fully managed power paths
  - Integrated 5-V, 3-A, 36-mΩ sourcing switch (TPS25750S/D)
  - Integrated 28-V, 7-A, 16-mΩ bi-directional load switch (TPS25750D only)
- Standalone USB Type-C PD solution
  - No firmware development or external micro-controller needed
- Integrated robust power path protection
  - Integrated reverse current protection, overvoltage protection, and slew rate control the high-voltage bi-directional power path
  - Integrated undervoltage and overvoltage protection and current limiting for inrush current protection for the 5V/3A source power path
  - 26-V tolerant CC pins for robust protection when connected to non-compliant devices
- Optimized for power applications
  - Integrated I2C control for TI battery chargers
  - Web-based GUI and pre-configured firmware
  - Optimized for power consumer only (sink) (UFP) applications
  - Optimized for power provider (source) and power consumer (sink) (DRP) applications
- USB Type-C power delivery (PD) controller
  - 10 configurable GPIOs
  - BC1.2 charging support
  - USB PD 3.0 compliant
  - USB Type-C specification complaint
  - Cable attach and orientation detection
  - Integrated VCONN switch
  - Physical layer and policy engine
  - 3.3-V LDO output for dead battery support
  - Power supply from 3.3 V or VBUS source

2 Applications

- Power tools, power banks, retail automation and payment
- Wireless speakers, headphones
- Other personal electronics and industrial applications

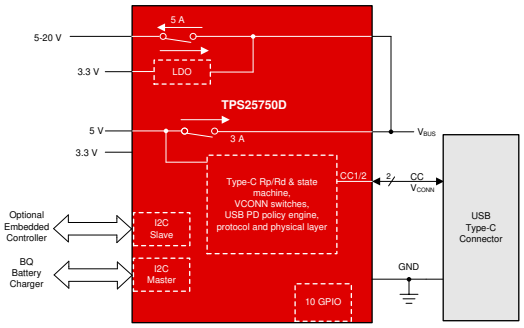
3 Description

The TPS25750 is a highly integrated stand-alone USB Type-C and Power Delivery (PD) controller optimized for applications supporting USB-C PD Power. The TPS25750 integrates fully managed power paths with robust protection for a complete USB-C PD solution. The TPS25750 also integrates control for external battery charger ICs for added ease of use and reduced time to market. The intuitive web based GUI will ask the user a few simple questions on the applications needs using clear block diagrams and simple multiple-choice questions. As a result, the GUI will create the configuration image for the user's application, reducing much of the complexity associated with competitive USB PD solutions.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS25750D	QFN (RJK)	4.0 mm x 6.0 mm
TPS25750S	QFN (RSM)	4.0 mm x 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

Changes from Revision * (July 2020) to Revision A (November 2020)	Page
• Changed data sheet status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

DEVICE NUMBER	5-V SOURCE LOAD SWITCH	INTEGRATED HIGH VOLTAGE BI-DIRECTIONAL LOAD SWITCH (PPHV)	HIGH VOLTAGE GATE DRIVER FOR BI-DIRECTIONAL EXTERNAL PATH (PP_EXT)
TPS25750D	Yes	Yes	No
TPS25750S	Yes	No	Yes

6 Pin Configuration and Functions

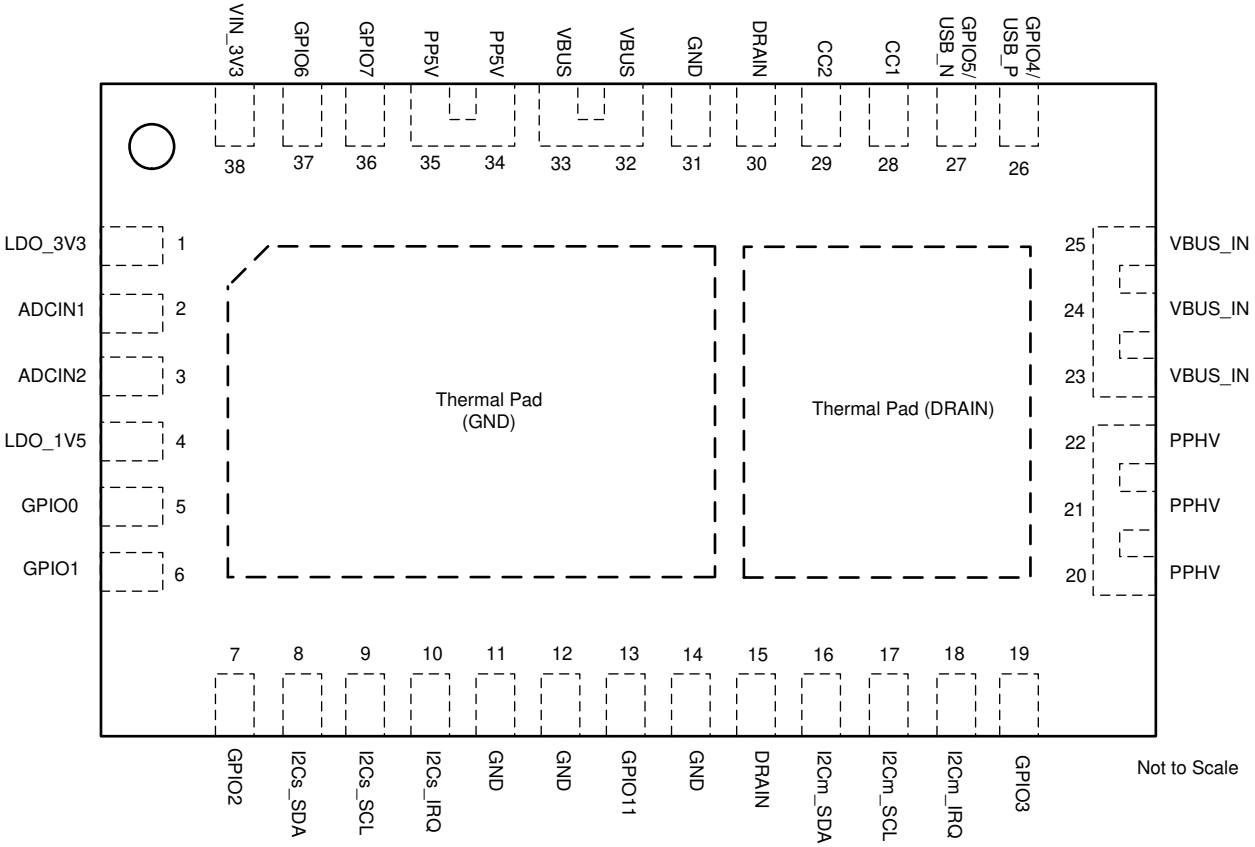

Figure 6-1. Top View of the TPS25750D 38-pin QFN RJK Package

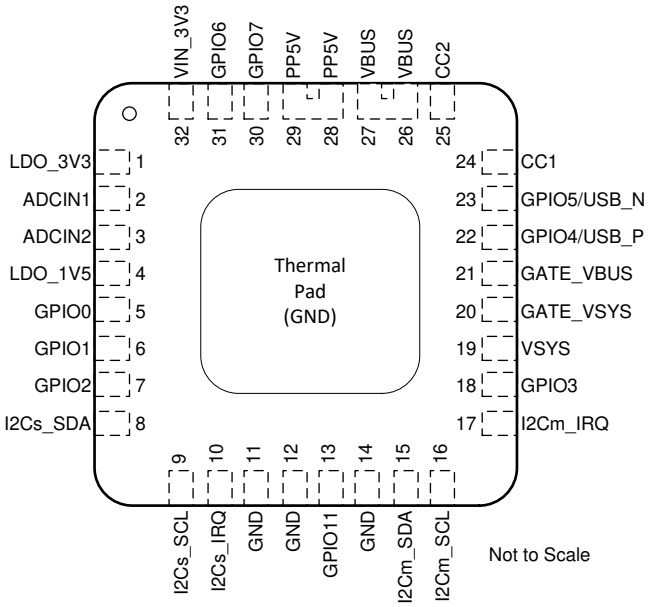

Figure 6-2. Top View of the TPS25750S 32-pin QFN RSM Package

Table 6-1. TPS25750D Pin Functions

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	28	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
CC2	29	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
GND	11, 12, 14, 31	—	—	Ground. Connect to ground plane.
GPIO0	5	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO1	6	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO2	7	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO3	19	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO4(USB_P)	26	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.This may be connected to D+ for BC1.2 support.
GPIO5(USB_N)	27	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. This may be connected to D- for BC1.2 support.
GPIO6	37	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO7	36	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Cs_SCL	9	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused.
I2Cs_SDA	8	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
$\overline{\text{I2Cs\_IRQ}}$	10	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. This can be re-configured to GPIO10. Tie to ground if unused.
I2Cm_SCL	17	O	Hi-Z	I^2C master serial clock. Open-drain output. Tie to pullup voltage through a resistor. Can be grounded if unused.
GPIO11	13	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Cm_SDA	16	I/O	Hi-Z	I^2C master serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Can be grounded if unused.
$\overline{\text{I2Cm\_IRQ}}$	18	I	Hi-Z	I2C master interrupt. Active low. Connect to external voltage through a pull-up resistor.Tie to ground when unused. This can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
DRAIN	15, 30	N/A	—	Connects to drain of internal FET.
PP5V	34, 35	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
PPHV	20, 21, 22	I/O		High-voltage sinking node in the system.
VBUS_IN	23, 24, 25	I/O		5-V to 20-V input.
VBUS	32, 33	O		5-V output from PP5V input to LDO. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	38	I	—	Supply for core circuitry and I/O. Bypass with capacitance C_{VIN_3V3} to GND.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

Table 6-2. TPS25750S Pin Functions

PIN		TYPE[1]	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS.
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS.
GND	11, 12, 14	—	—	Ground. Connect to ground plane.
GPIO0	5	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO1	6	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO2	7	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO3	18	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO4 (USB_P)	22	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. This may be connected to D+ for BC1.2 support.
GPIO5 (USB_N)	23	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. This may be connected to D- for BC1.2 support.
GPIO6	31	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO7	30	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Cs_SCL	9	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused.
I2Cs_SDA	8	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
$\overline{\text{I2Cs\_IRQ}}$	10	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. This can be re-configured to GPIO10. Tie to ground when unused.
I2Cm_SCL	16	O	Hi-Z	I^2C master serial clock. Open-drain output. Tie to pullup voltage through a resistor when used or unused.
GPIO11	13	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Cm_SDA	15	I/O	Hi-Z	I^2C master serial data. Open-drain input/output. Tie to pullup voltage through a resistor when used or unused.
$\overline{\text{I2Cm\_IRQ}}$	17	I	Hi-Z	I2C master interrupt. Active low. Connect to external voltage through a pull-up resistor. Tie to ground when unused. This can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
PP5V	28, 29	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
VSYS	19	I	—	High-voltage sinking node in the system. It is used to implement reverse-current-protection (RCP) for the external sinking paths controlled by GATE_VSYS.
VBUS	26, 27	I/O		5-V to 20-V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

7 Specifications

7.1 Absolute Maximum Ratings

7.1.1 TPS25750D and TPS25750S - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range (2)	PP5V	–0.3	6	V
	VIN_3V3	–0.3	4	
	ADCIN1, ADCIN2	-0.3	4	
	VBUS_IN, VBUS(4)	–0.3	28	V
	CC1, CC2 (4)	–0.5	26	
	GPIOx	-0.3	6.0	
	I2Cm_SDA, I2Cm_SCL, $\overline{\text{I2Cm\_IRQ}}$, $\overline{\text{I2Cs\_IRQ}}$,I2Cs_SCL, I2Cs_SDA	–0.3	4	
Output voltage range (2)	LDO_1V5(3)	–0.3	2	V
	LDO_3V3(3)	–0.3	4	
Source current	Source or sink current VBUS		internally limited	A
	Positive source current on CC1, CC2		1	
	Positive sink current on CC1, CC2 while VCONN switch is enabled		1	
	Positive sink current for I2Cm_SDA, I2Cm_SCL, I2Cm_IRQ, I2Cs_IRQ,I2Cs_SCL, I2Cs_SDA		internally limited	
	Positive source current for LDO_3V3, LDO_1V5		internally limited	
Source current	GPIOx		0.005	A
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

7.1.2 TPS25750D - Absolute Maximum Ratings

		MIN	MAX	UNIT
Input voltage range (1)	PPHV	–0.3	28	V
$V_{PPHV\_VBUS\_IN}$	Source-to-source voltage		28	V
Sink current	Continuous current to/from VBUS_IN to PPHV		7	A
	Pulsed current to/from VBUS_IN to PPHV(2)		10	
T_{J_PPHV} Operating junction temperature	PP_HV switch	–40	175	°C

(1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(2) Pulse duration ≤ 100 µs and duty-cycle ≤ 1%.

7.1.3 TPS25750S - Absolute Maximum Ratings

		MIN	MAX	UNIT
Output voltage range (1)	GATE_VBUS, GATE_VSYS(2)	–0.3	40	V

7.1.3 TPS25750S - Absolute Maximum Ratings (continued)

		MIN	MAX	UNIT
V_{GS}	V_{GATE_VBUS} - V_{VBUS}, V_{GATE_SYS} - V_{VSYS}	–0.5	12	V

(1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(2) Do not apply voltage to these pins.

7.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommeded Operating Conditions

7.3.1 TPS25750D - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage range (1)	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		ADCIN1, ADCIN2,VBUS_IN, VBUS (2)	4	22	
		PPHV	0	22	
V_{IO}	I/O voltage range (1)	I2Cx_SDA, I2Cx_SCL, $\overline{\text{I2Cx\_IRQ}}$, ADCIN1, ADCIN2	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_{PP_HV}	Current from VBUS_IN to PPHV			7	A
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	Current from LDO_3V3		5	mA
T_A	Ambient operating temperature	I_{PP_5V} ≤ 3 A, I_{PP_HV} = 0, I_{PP_CABLE} ≤ 315 mA	–40	85	°C
		I_{PP_5V} ≤ 1.5 A, I_{PP_HV} = 0, I_{PP_CABLE} ≤ 315 mA	–40	105	
		I_{PP_5V} = 0, I_{PP_HV} ≤ 7 A, I_{PP_CABLE} = 0	–40	45	
		I_{PP_5V} = 0, I_{PP_HV} ≤ 6 A, I_{PP_CABLE} = 0	–40	65	
		I_{PP_5V} = 0, I_{PP_HV} ≤ 5 A, I_{PP_CABLE} ≤ 315 mA	–40	85	
		I_{PP_5V} = 0, I_{PP_HV} ≤ 3.5 A, I_{PP_CABLE} ≤ 315 mA	–40	105	
T_{J_PPHV}	Operating junction temperature	PP_HV switch	–40	150	°C
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(2) All VBUS and VBUS_IN pins be shorted together.

7.3.2 TPS25750S - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_I	Input voltage range [1]	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		VBUS	4	22	
		VSYS	0	22	
V_{IO}	I/O voltage range [1]	I2Cx_SDA, I2Cx_SCL, $\overline{\text{I2Cx\_IRQ}}$, ADCIN1, ADCIN2	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	sum of current from LDO_3V3 and GPIOx		5	mA
T_A	Ambient operating temperature	$I_{PP\_5V} \le 1.5$ A, $I_{PP\_CABLE} \le 315$ mA	–40	105	°C
		$I_{PP\_5V} \le 3$ A, $I_{PP\_CABLE} \le 315$ mA	–40	85	
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

7.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS[4]	25 V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10 V	120[2]			µF
C_{VSYS} (TPS25750S)	Capacitance on VSYS Sink from VBUS	25 V		47	100	µF
C_{PPHV} (TPS25750D)	Capacitance on PPHV Sink from VBUS	25 V		47	100	µF
C_{CCy}	Capacitance on CCy pins[3]	6.3 V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This is a requirement from USB PD (cSrcBulkShared). Keep at least 10 µF tied directly to PP5V.
(3) This includes all external capacitance to the Type-C receptacle.
(4) The device can be configured to quickly disable the sinking power path upon certain events. When such a configuration is used, a capacitance on the higher side of this range is recommended.

7.5 Thermal Information

7.5.1 TPS25750D - Thermal Information

THERMAL METRIC[1]		TPS25750D QFN (RJK) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (sinking through PP_HV)	57.4	°C/W
	Junction-to-ambient thermal resistance (sourcing through PP_5V)	46.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance (sinking through PP_HV)	30.5	°C/W
	Junction-to-case (top) thermal resistance (sourcing through PP_5V)	20.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (sinking through PP_HV)	21.1	°C/W
	Junction-to-board thermal resistance (sourcing through PP_5V)	11.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (sinking through PP_HV)	18.2	°C/W
	Junction-to-top characterization parameter (sourcing through PP_5V)	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (sinking through PP_HV)	21.1	°C/W
	Junction-to-board characterization parameter (sourcing through PP_5V)	11.1	°C/W
$R_{\theta JC}$ (bot_GND)	Junction-to-case (bottom GND pad) thermal resistance	1.8	°C/W
$R_{\theta JC}$ (bot_DRAIN)	Junction-to-case (bottom DRAIN pad) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5.2 TPS25750S - Thermal Information

THERMAL METRIC[1]		TPS25750S QFN (RSM) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
V_{VIN3V3_UVLO}	Voltage required on VIN_3V3 for power on	rising, V_{VBUS} = 0	2.56	2.66	2.76	V
		falling, V_{VBUS} = 0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	Voltage on LDO_3V3	V_{VIN_3V3} = 0 V, 10 µA ≤ I_{LOAD} ≤ 18 mA, $_{VBUS}$ ≥ 3.9 V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3} = 50 mA			1.4	Ω
V_{LDO_1V5}	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

7.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	Current into VIN_3V3	Active Source mode: V_{VBUS} = 5.0 V, V_{VIN_3V3} = 3.3 V		3		mA
$I_{VIN\_3V3,ActSnk}$	Current into VIN_3V3	Active Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		3	6	mA
$I_{VIN\_3V3,IdlSrc}$	Current into VIN_3V3	Idle Source mode: V_{VBUS} = 5.0 V, V_{VIN_3V3} = 3.3 V		1.0		mA
$I_{VIN\_3V3,IdlSnk}$	Current into VIN_3V3	Idle Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		1.0		mA
$P_{MstbySnk}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Sink Mode	CCm floating, V_{CCn} = 0.4 V, V_{PP5V} = 5 V, V_{VIN_3V3} = 3.3 V, V_{VBUS} = 5.0 V, GATE_VBUS, GATE_VSYS disabled, and T_J = 25°C		4.1		mW
$P_{MstbySrc}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	CCm floating, CCn tied to GND through 5.1 kΩ, V_{PP5V} = 5 V, V_{VIN_3V3} = 3.3 V, I_{VBUS} = 0, T_J = 25°C		4.5		mW
$I_{PP5V,Sleep}$	Current into PP5V	Sleep source mode: V_{PA_VBUS} = 0 V, V_{PB_VBUS} = 0 V, V_{VIN_3V3} = 3.3 V		2		µA
$I_{VIN\_3V3,Sleep}$	Current into VIN_3V3	Sleep DRP mode: V_{VBUS} = 0 V, V_{VIN_3V3} = 3.3 V		56		µA

7.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J = 25°C		36	38	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A,T_J = 125°C		36	53	mΩ
I_{PP5V_REV}	VBUS to PP5V leakage current	V_{PP5V} = 0 V, V_{VBUS} = 5.5 V, PP_5V disabled, T_J ≤ 85°C, measure I_{PP5V}			5	µA
I_{PP5V_FWD}	PP5V to VBUS leakage current	V_{PP5V} = 5.5 V, V_{VBUS} = 0 V, PP_5V disabled, T_J ≤ 85°C, measure I_{VBUS}			15	µA
I_{LIM5V}	Current limit setting	Configure to setting 0	1.15		1.36	A
I_{LIM5V}	Current limit setting	Configure to setting 1	1.61		1.90	A
I_{LIM5V}	Current limit setting		2.3		2.70	A
I_{LIM5V}	Current limit setting	Configure to setting 3	3.04		3.58	A
I_{LIM5V}	Current limit setting	Configure to setting 4	3.22		3.78	A

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	PP5V to VBUS current sense accuracy	3.64 A ≥ I_{VBUS} ≥ 1 A	3.05	3.5	3.75	A/V
$V_{PP\_5V\_RCP}$	RCP clears and PP_5V starts turning on when V_{VBUS} – V_{PP5V} < $V_{PP\_5V\_RCP}$. Measure V_{VBUS} – V_{PP5V}		10		20	mV
$t_{iOS\_PP\_5V}$	Response time to VBUS short circuit	VBUS to GND through 10 mΩ, C_{VBUS} = 0		1.15		µs
$t_{PP\_5V\_ovp}$	Response time to V_{VBUS} > $V_{OVP4RCP}$	Enable PP_5V, I_{RpDef} being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 20 V at 100 V/ms, C_{PP5V} = 2.5 µF, measure time from OVP detection until reverse current < 100 mA		4.5		µs
$t_{PP\_5V\_uvlo}$	Response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{VBUS} < 0.8 V	R_L = 100 Ω, no external capacitance on VBUS		4		µs
$t_{PP\_5V\_rcp}$	Response time to V_{PP5V} < V_{VBUS} + $V_{PP\_5V\_RCP}$	V_{PP5V} = 5.5 V, I_{RpDef} being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4 V to 21.5 V at 10 V/µs, measure V_{PP5V}. C_{PP5V} = 104 µF, C_{VBUS}=10 µF, measure time from RCP detection until reverse current < 100 mA		0.7		µs
t_{ILIM}	Current clamping deglitch time			5.1		ms
t_{ON}	From enable signal to VBUS at 90% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	2.3	3.3	4.3	ms
t_{OFF}	From disable signal to VBUS at 10% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	0.30	0.45	0.6	ms
t_{RISE}	VBUS from 10% to 90% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	1.2	1.7	2.2	ms
t_{FALL}	VBUS from 90% to 10% of initial value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	0.06	0.1	0.14	ms

7.9 PPHV Power Switch Characteristics - TPS25750D

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPHV}	Resistance from VBUS_IN to PPHV power switch resistance	T_{J_PPHV} = 25°C, I_{PPHV} = 6.5 A		16	19	mΩ
		T_{J_PPHV} = 125°C, I_{PPHV} = 6.5A		24	29	
		T_{J_PPHV} = 150°C, I_{PPHV} = 6.5 A		27	32	mΩ
V_{RCP}	Comparator mode RCP threshold, V_{PPHV} - V_{VBUS}	Setting 0, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
		setting 1, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	4	8	12	mV
		Setting 2, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	6	10	14	mV
		Setting 3, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	8	12	16	mV

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS	Soft start slew rate for GATE_VSYS, setting 0	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	0.35	0.41	0.47	V/ms
	Soft start slew rate for GATE_VSYS, setting 1	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	0.67	0.81	0.95	
	Soft start slew rate for GATE_VSYS, setting 2	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	1.33	1.7	2.0	
	Soft start slew rate for GATE_VSYS, setting 3	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	
t_{PPHV_OFF}	Time allowed to disable the internal PPHV switch in normal shutdown mode	V_{VBUS} = 20 V, V_{PPHV} = 20 V (initially), C_{PPHV}< 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 1V		400	1000	µs
t_{PPHV_OVP}	Time allowed to disable the internal PPHV switch in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator	OVP: $V_{OVP4RCP}$ = setting 57, V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, V_{PPHV} = V_{VBUS_IN} (initially), C_{PPHV}< 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 0.1 V		2	4	µs
t_{PPHV_RCP}	Time allowed to disable the internal PPHV switch in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator	RCP: V_{RCP}= setting 0, V_{VBUS} = 5 V, V_{VSYS} = 5 V initially, then raised to 6 V with dV/dt = 0.1 V/µs, $C_{VBUS=}$10 µF, measure time from V_{VSYS} > V_{BUS} + V_{RCP} to the time of peak voltage on VBUS		1	2	µs
t_{PPHV_FSD}	Time allowed to disable the internal PPHV switch in fast shutdown mode (OVP)	V_{PPHV} = 20 V (initially), V_{VBUS}=20 V then raised to 23 V in 50 ns, r_{OVP} = 1, C_{PPHV} < 1 nF, I_{PPHV} = 0.1 A, switch is off when V_{VBUS_IN} – V_{PPHV} > 0.5 V		0.25	20	µs
t_{PPHV_ON}	Time to enable the internal PPHV switch	V_{VBUS_IN} = 5 V, C_{PPHV} = 0, I_{PPHV} = 0, measure time from register write to enable PPHV until V_{VBUS_IN} - V_{PPHV} < 0.1 V, soft start setting 3	1500	1800	2100	µs

7.10 PP_EXT Power Switch Characteristics - TPS25750S

Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_ON}	Gate driver sourcing current	0 ≤ V_{GATE_VSYS} - V_{VSYS} ≤ 6 V, V_{VSYS} ≤ 22 V, V_{VBUS} > 4 V, measure I_{GATE_VSYS}	8.5		11.5	µA
		0 ≤ V_{GATE_VBUS} - V_{VBUS} ≤ 6 V, 4 V ≤ V_{VBUS} ≤ 22 V, measure I_{GATE_VBUS}	8.5		11.5	µA
V_{GATE_ON}	Sourcing voltage (ON)	0 ≤ V_{VSYS} ≤ 22 V, I_{GATE_VSYS} < 4 µA, measure V_{GATE_VSYS} – V_{VSYS}, V_{VBUS} > 4 V	6		12	V
		4 V ≤ V_{VBUS} ≤ 22 V, I_{GATE_VBUS} < 4 µA, measure V_{GATE_VBUS} – V_{VBUS}	6		12	V
V_{RCP}	Comparator mode RCP threshold, V_{VSYS} - V_{VBUS}	Setting 0, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
		Setting 1, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	4	8	12	mV
		Setting 2, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	6	10	14	mV
		Setting 3, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	8	12	16	mV
I_{GATE_OFF}	Sinking strength	Normal turnoff: V_{VSYS} = 5 V, V_{GATE_VSYS} = 6 V, measure I_{GATE_VSYS}	13			µA
		Normal turnoff: V_{VBUS} = V_{VSYS} = 5 V, V_{GATE_VBUS} = 6 V, measure I_{GATE_VBUS}	13			µA
R_{GATE_FSD}	Sinking strength	Fast turnoff: V_{VSYS} = 5 V, V_{GATE_VSYS} = 6 V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VSYS}			85	Ω
		Fast turnoff: V_{VBUS} = V_{VSYS} = 5 V, V_{GATE_VBUS} = 6 V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VBUS}			85	Ω
$R_{GATE\_OFF\_UVLO}$	Sinking strength in UVLO (safety)	V_{VIN_3V3} = 0 V, V_{VBUS} = 3.0 V, V_{GATE_VSYS} = 0.1 V, measure resistance from GATE_VSYS to GND			1.5	MΩ

Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS	Soft start slew rate for GATE_VSYS, setting 0	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	0.35	0.41	0.47	V/ms
	Soft start slew rate for GATE_VSYS, setting 1	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	0.67	0.81	0.91	
	Soft start slew rate for GATE_VSYS, setting 2	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	1.33	1.7	1.80	
	Soft start slew rate for GATE_VSYS, setting 3	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500 pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	
$t_{GATE\_VBUS\_OFF}$	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode.(1)	V_{VBUS} = 20 V, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when $V_{GATE\_VBUS} - V_{VBUS}$ < 1 V		450	4000	µs
$t_{GATE\_VBUS\_OVP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator(1)	OVP: $V_{OVP4RCP}$ = setting 57, V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when $V_{GATE\_VBUS} - V_{VBUS}$ < 1 V		3	5	µs
$t_{GATE\_VBUS\_RCP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator(1)	RCP: V_{RCP} = setting 0, V_{VBUS} = 5 V, V_{VSYS} = 5 V initially, then raised to 5.5 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when $V_{GATE\_VBUS} - V_{VBUS}$ < 1 V		1	2	µs
$t_{GATE\_VSYS\_OFF}$	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode(1)	V_{VSYS}= 20 V, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when $V_{GATE\_VSYS} - V_{VSYS}$ < 1 V		450	4000	µs
$t_{GATE\_VSYS\_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP)(1)	V_{VBUS} = 20 V initially, then raised to 23 V in 50 ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3 nF, gate is off when $V_{GATE\_VSYS} - V_{VSYS}$ < 1 V, r_{OVP} = 1		0.25	20	µs
$t_{GATE\_VBUS\_ON}$	Time to enable GATE_VBUS (1)	Measure time from when V_{GS} = 0 V until V_{GS} >3 V, where $V_{GS} = V_{GATE\_VBUS} - V_{VBUS}$		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values were measured when Px_GATE_VSYS and Px_GATE_VBUS were used to drive two CSD17571Q2 in common drain back-to-back configuration.

7.11 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS overvoltage protection for RCP programmable range	OVP detected when V_{VBUS} > $V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	Hysteresis		1.75	2	2.25	%
r_{OVP}	Ratio of OVP4RCP input used for OVP4VSYS comparator. r_{OVP} × $V_{OVP4VSYS}$ = $V_{OVP4RCP}$	setting 0		1		V/V
		setting 1		0.95		V/V
		setting 2		0.90		V/V
		setting 3		0.875		V/V
$V_{OVP4VSYS}$	VBUS overvoltage protection range for VSYS protection	OVP detected when r_{OVP} × V_{VBUS} > $V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	Hysteresis	VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 0	1.75	2	2.25	%
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 1	1.8	2.1	2.4	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 2	1.9	2.2	2.5	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 3	2	2.3	2.6	
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22 V, measure I_{VBUS}	4		15	mA

7.12 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pullup)						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	V_{LDO_3V3} > 2.302 V, R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached CCy open circuit voltage while Rp enabled, no load	V_{PP5V} > 3.802 V, R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on CCy	V_{CCy} = 5.5 V, V_{CCx} = 0 V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 3.8 V, measure current into CCy			10	µA
		V_{CCy} = 5.5 V, V_{CCx} = 0 V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 0, T_J ≤ 85°C, measure current into CCy			10	
I_{RpDef}	Current source - USB Default	0 < V_{CCy} < 1.0 V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	Current source - 1.5 A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 1.5 V, measure I_{CCy}	166	180	194	µA
$I_{Rp3.0}$	Current source - 3.0 A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 2.45 V, measure I_{CCy}	304	330	356	µA
Type-C Sink (Rd pulldown)						
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	rising	0.2		0.24	V
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	falling	0.16		0.20	V
	Hysteresis			0.04		V

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SNK2}	Default/1.5-A detection threshold	falling	0.62		0.68	V
V_{SNK2}	Default/1.5-A detection threshold	rising	0.63	0.66	0.69	V
	Hysteresis			0.01		V
V_{SNK3}	1.5-A/3.0-A detection threshold when Rd applied to CCy	falling	1.17		1.25	V
V_{SNK3}	1.5-A/3.0-A detection threshold when Rd applied to CCy	rising	1.22		1.3	V
	Hysteresis			0.05		V
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{CCy} ≤ 2.1 V, measure resistance on CCy, after trimming using trim_cd_rd, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V,	4.6		5.6	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{CCy} ≤ 5.5 V, measure resistance on CCy, after trimming using trim_cd_rd	4.0		6.12	kΩ
V_{CLAMP}	Dead battery Rd clamp	V_{VIN_3V3} = 0 V, 64 µA < I_{CCy} < 96 µA	0.25		1.32	V
		V_{VIN_3V3} = 0 V, 166 µA < I_{CCy} < 194 µA	0.65		1.32	
		V_{VIN_3V3} = 0 V, 304 µA < I_{CCy} < 356 µA	1.20		2.18	
R_{Open}	Resistance from CCy to GND when configured as open	V_{VBUS} = 0, V_{VIN_3V3} = 3.3 V, V_{CCy} = 5 V, measure resistance on CCy	500			kΩ
		V_{VBUS} = 5 V, V_{VIN_3V3} = 0, V_{CCy} = 5 V, measure resistance on CCy	500			kΩ

7.13 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V} = 5 V, I_L = 250 mA, measure resistance from PP5V to CCy			1.2	Ω
I_{LIMVC}	Short circuit current limit	Setting 0, V_{PP5V} = 5 V, R_L=10 mΩ, measure I_{CCy}	350	410	470	mA
I_{LIMVC}	Short circuit current limit	Setting 1, V_{PP5V} = 5 V, R_L=10 mΩ, measure I_{CCy}	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85°C, V_{CCy} = 5.5 V, V_{PP5V} = 0 V, V_{VBUS} = 5 V, LDO forced to draw from VBUS, measure I_{CCy}			10	µA
V_{VC_OVP}	Overvoltage protection threshold for PP_CABLE	V_{PP5V} rising	5.6	5.9	6.2	V
V_{VC_RCP}	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9 V, V_{CCy} = V_{PP5V}, V_{CCx} rising	60	200	340	mV
		V_{PP5V} ≥ 4.9 V, V_{CCy} ≤ 4 V, V_{CCx} rising	210	340	470	mV
t_{VCILIM}	Current clamp deglitch time			1.3		ms
$t_{PP\_CABLE\_FSD}$	Time to disable PP_CABLE after V_{PP5V} > V_{VC_OVP} or V_{CCx} - V_{PP5V} > V_{VC_RCP}	C_L = 0		0.5		µs
$t_{PP\_CABLE\_off}$	From disable signal to CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5 V, C_L = 0	100	200	300	µs

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{iOS\_PP\_CABLE}$	Response time to short circuit	V_{PP5V} = 5 V, for short circuit R_L = 10 mΩ		2		µs

7.14 CC PHY Parameters

Operating under these conditions unless otherwise noted: and (3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on CCy	Standard External load	–75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750 kHz	33	54	75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns
t_{Fall}	Fall time. 90 % to 10 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns
V_{PHY_OVP}	OVP detection threshold for USB PD PHY	0 ≤ V_{VIN_3V3} ≤ 3.6 V, 0 ≤ V_{PP5V} ≤ 5.5 V, V_{VBUS} ≥ 4 V. Initially V_{CC1} ≤ 5.5 V and V_{CC2} ≤ 5.5 V, then V_{CCx} rises	5.5		8.5	V
Receiver						
Z_{BMCRX}	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			MΩ
C_{CC}	Receiver capacitance on CCy(1)	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SNK\_R}$	Rising threshold on CCy for receiver comparator	Sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on CCy for receiver comparator	Source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on CCy for receiver comparator	Sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on CCy for receiver comparator	Source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

7.15 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		Hysteresis		15		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The power paths for each port sourcing from PP5V and PP_CABLE power paths have local sensors that disables them when this temperature is exceeded	Temperature rising	135	150	165	°C
		Hysteresis		10		°C

7.16 ADC Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6-V max scaling, voltage divider of 3		14		mV
		25.2-V max scaling, voltage divider of 21		98		mV
		4.07-A max scaling		16.5		mA
GAIN_ERR	Gain error	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–2.4		2.4	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–2.1		2.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–2.1		2.1	
VOS_ERR	Offset error(1)	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–4.5		4.5	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–4.1		4.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

7.17 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB_P, USB_N						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3 V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3 V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3 V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_RPU	GPIOx internal pullup	Pullup enabled	50	100	150	kΩ
GPIO_RPD	GPIOx internal pulldown	Pulldown enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20	50	ns
GPIO0-7 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3 V, I_{GPIOx}= -2 mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3 V, I_{GPIOx} = 2 mA			0.4	V
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} ≤ V_{LDO_3V3}	–1		1	µA
t_{BOOT}	Time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

7.18 BC1.2 Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
I_{DP_SRC}	DCD source current	V_{LDO_3V3} = 3.3 V	7	10	13	µA

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DM_DWN}	DCD pulldown resistance	V_{USB_N} = 3.6 V	14.25	20	24.8	kΩ
R_{DP_DWN}	DCD pulldown resistance	V_{USB_P} = 3.6 V	14.25	20	24.8	kΩ
V_{LGC_HI}	Threshold for no connection	V_{USB_P} ≥ V_{LGC_HI}, V_{LDO_3V3} = 3.3 V, R_{USB_P} = 300 kΩ	2		3.6	V
V_{LGC_LO}	Threshold for connection	V_{USB_N} ≤ V_{LGC_LO}, V_{LDO_3V3} = 3.3 V, R_{USB_P} = 24.8 kΩ	0		0.8	V
Advertisement and Detection						
V_{DX_SRC}	Source voltage	C_{GPIO4} ≤ 600 pF	0.55	0.6	0.65	V
V_{DX_ILIM}	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	V_{USB_P} ≥ 250 mV	25	75	125	µA
I_{DX_SNK}	Sink Current	V_{USB_N} ≥ 250 mV	25	75	125	µA
R_{DCP_DAT}	Dedicated Charging Port Resistance	0.5 V ≤ V_{USB_P} ≤ 0.7 V, 25 µA ≤ I_{USB_N} ≤ 175 µA			200	Ω

7.19 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2Cs\_IRQ}}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45 V	–1		1	µA
I2Cm_IRQ						
IRQ_VIH	High-Level input voltage	V_{LDO_3V3} = 3.3 V	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	V_{LDO_3V3} = 3.3 V	0.72		1.3	V
IRQ_VIL	low-level input voltage	V_{LDO_3V3} = 3.3 V			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	V_{LDO_3V3} = 3.3 V	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	V_{LDO_3V3} = 3.3 V	0.09			V
IRQ_DEG	input deglitch			20		ns
IRQ_ILKG	$\overline{\text{I2C3m\_IRQ}}$ leakage current	V_{I2C3m_IRQ} = 3.45 V	–1		1	µA
SDA and SCL Common Characteristics (Master, Slave)						
V_{IL}	Input low signal	V_{LDO_3V3} = 3.3 V			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3} = 3.3 V	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3} = 3.3 V	0.165			V
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL} = 0.4 V	15			mA
I_{OL}	Max output low current	V_{OL} = 0.6 V	20			mA
t_f	Fall time from 0.7 × V_{DD} to 0.3 × V_{DD}	V_{DD} = 1.8 V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns
		V_{DD} = 3.3 V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I^2C pulse width surpressed				50	ns
C_I	Pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8 V or 3.3 V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8 V or 3.3 V, SCL low to SDA output valid			3.45	µs

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8 V or 3.3 V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8 V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			0.9	µs
SDA and SCL Fast Mode Plus Characteristics (Slave)						
f_{SCLS}	Clock frequency for Fast Mode Plus(1)	V_{DD} = 1.8 V or 3.3 V	400		800	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8 V or 3.3 V, SCL low to SDA output valid			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			0.55	µs
SDA and SCL Fast Mode Characteristics (Master)						
f_{SCLM}	Clock frequency for master	V_{DD} = 3.3 V		390	410	kHz
$t_{HD;STA}$	Start or repeated start condition hold time	V_{DD} = 3.3 V	0.6			µs
t_{LOW}	Clock low time	V_{DD} = 3.3 V	1.3			µs
t_{HIGH}	Clock high time	V_{DD} = 3.3 V	0.6			µs
$t_{SU;STA}$	Start or repeated start condition setup time	V_{DD} = 3.3 V	0.6			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting data, V_{DD} = 3.3 V	100			ns
$t_{SU;STO}$	Stop condition setup time	V_{DD} = 3.3 V	0.6			µs
t_{BUF}	Bus free time between stop and start	V_{DD} = 3.3 V	1.3			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 3.3 V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 3.3 V, ACK signal from SCL low to SDA (out) low			0.9	µs

(1) Master must control fSCLS to ensure tLOW > tVD; ACK.

7.20 Typical Characteristics

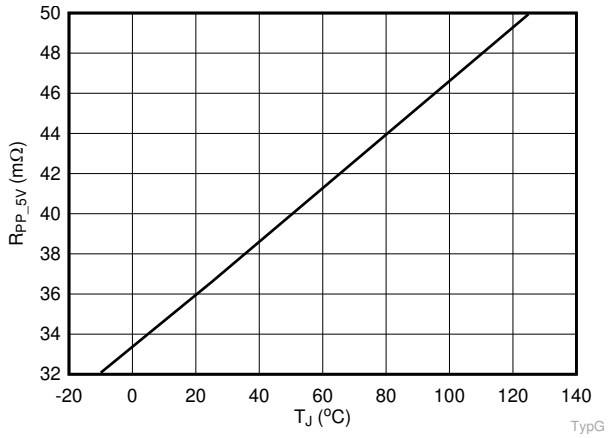

Figure 7-1. PP_5V Rdson vs. Temperature.

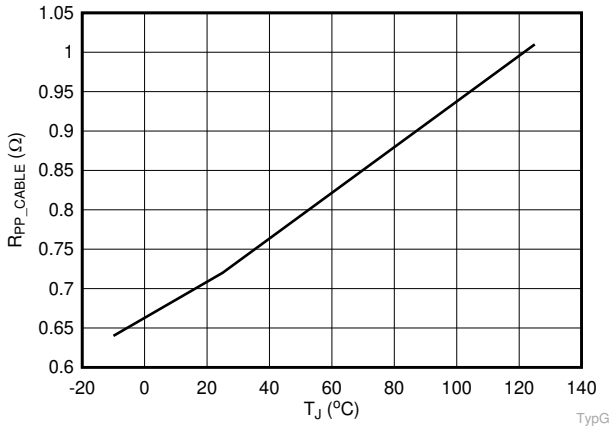

Figure 7-2. PP_CABLE Rdson vs. Temperature

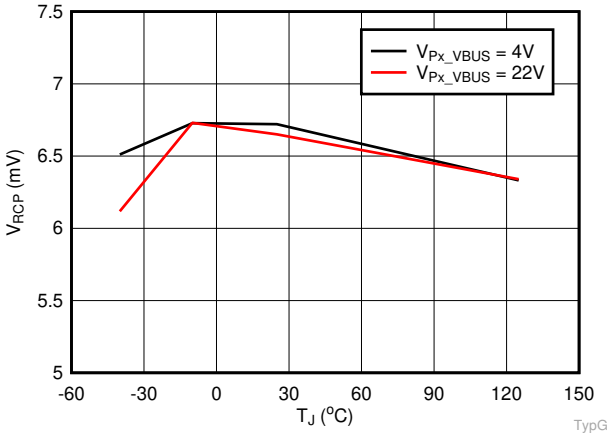

Figure 7-3. V_{RCP} vs. Temperature

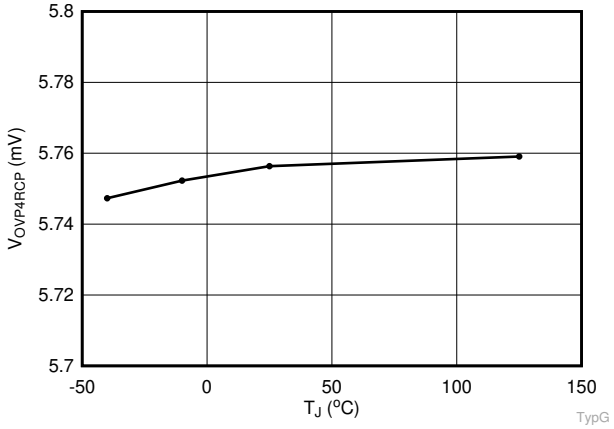

Figure 7-4. $V_{OVP4RCP}$ (Setting 2) vs. Temperature

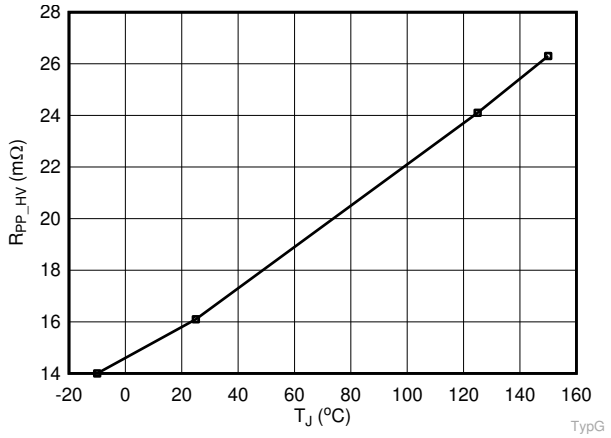

Figure 7-5. R_{PPHV} vs. Temperature for TPS25750D

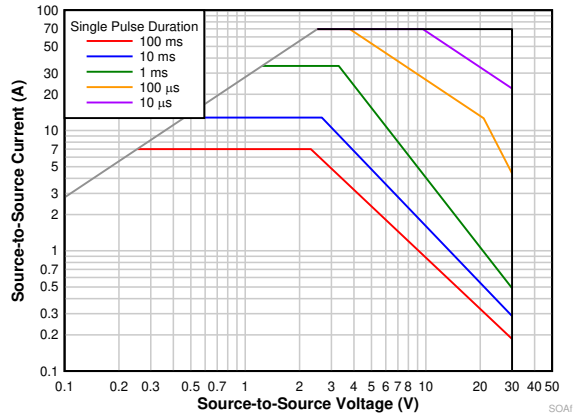

Figure 7-6. Safe-Operating-Area (SOA) of PPHV for TPS25750D

7.20 Typical Characteristics (continued)

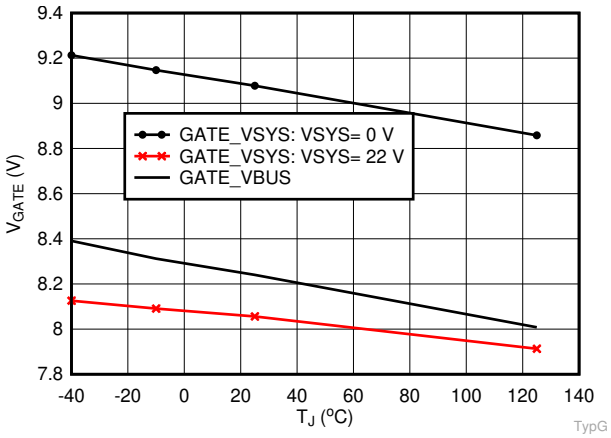

Figure 7-7. $V_{GATE\_VBUS\_ON}$ vs. Temperature for TPS25750S

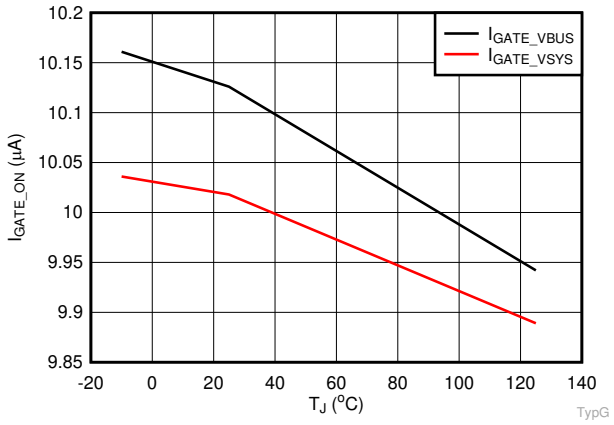

Figure 7-8. $V_{GATE\_VSYS\_ON}$ vs. Temperature for TPS25750S

8 Parameter Measurement Information

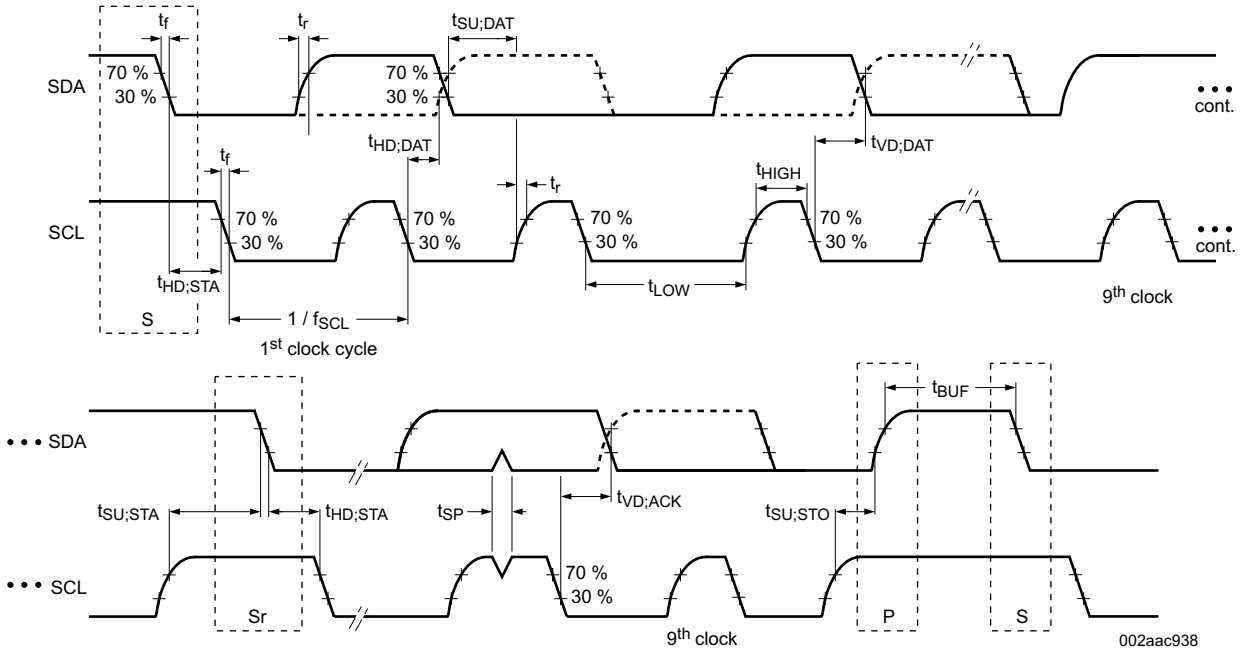

Figure 8-1. I²C Slave Interface Timing

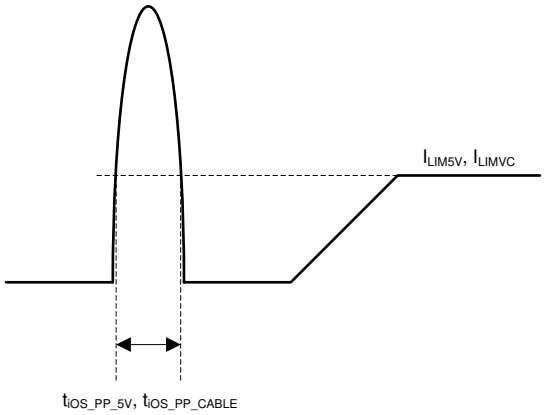

Figure 8-2. Short-circuit Response Time for Internal Power Paths PP_5Vx and PP_CABLEx

9 Detailed Description

9.1 Overview

The TPS25750 is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS25750 communicates with the cable and another USB Type-C and PD device at the opposite end of the cable. It also enables integrated port power switch for sourcing, and controls a high current port power switch for sinking.

The TPS25750 is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switches
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features, and more detailed circuitry, see *USB-PD Physical Layer*.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features, and more detailed circuitry, see *Cable Plug and Orientation Detection*.

The port power switches provide power to the VBUS pin and CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features, and more detailed circuitry, see *Power Paths*.

The power management circuitry receives and provides power to the TPS25750 internal circuitry and LDO_3V3 output. See *Power Management* for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS25750 functionality. A portion of the digital core contains ROM memory, which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS25750, loading of the device configuration information, and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features, and more detailed circuitry, see *Digital Core*.

The TPS25750 has one I^2C master to write to and read from external slave devices such as a battery charger or an optional external EEPROM memory (see *I2C Interface*).

The TPS25750 also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

9.2 Functional Block Diagram

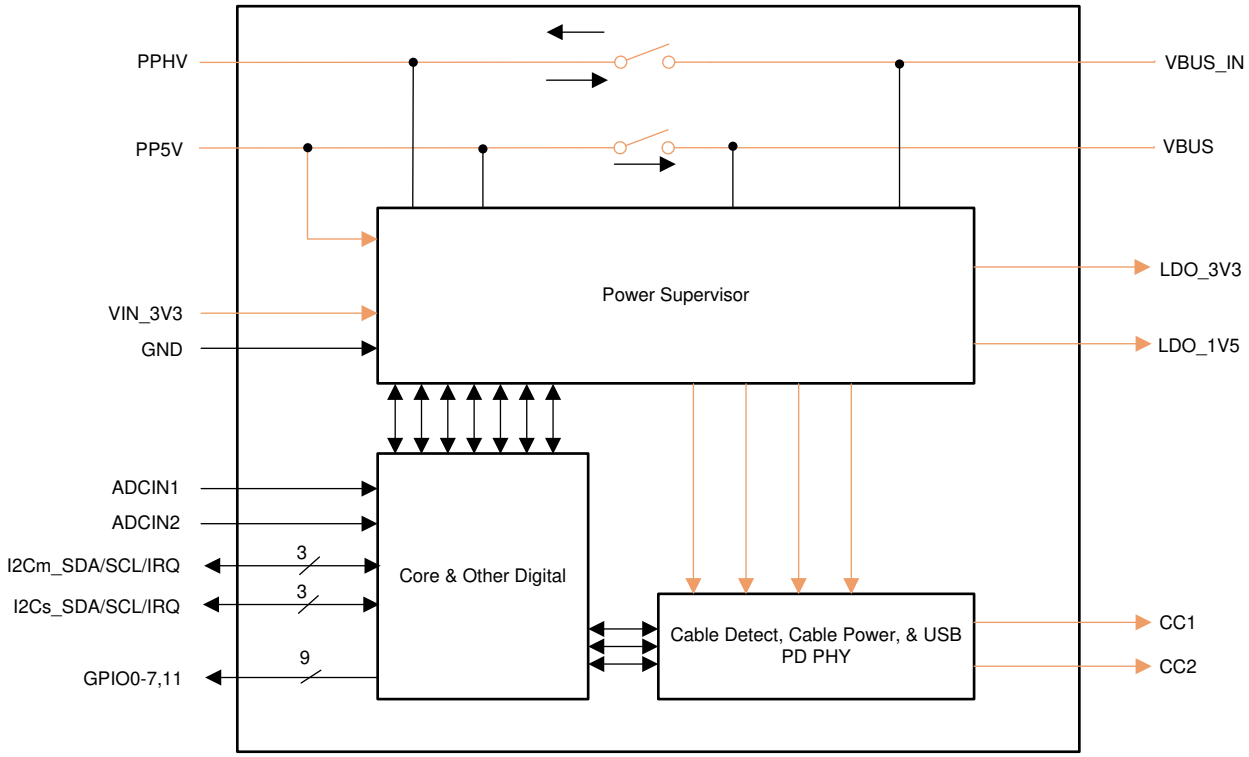

Figure 9-1. TPS25750D

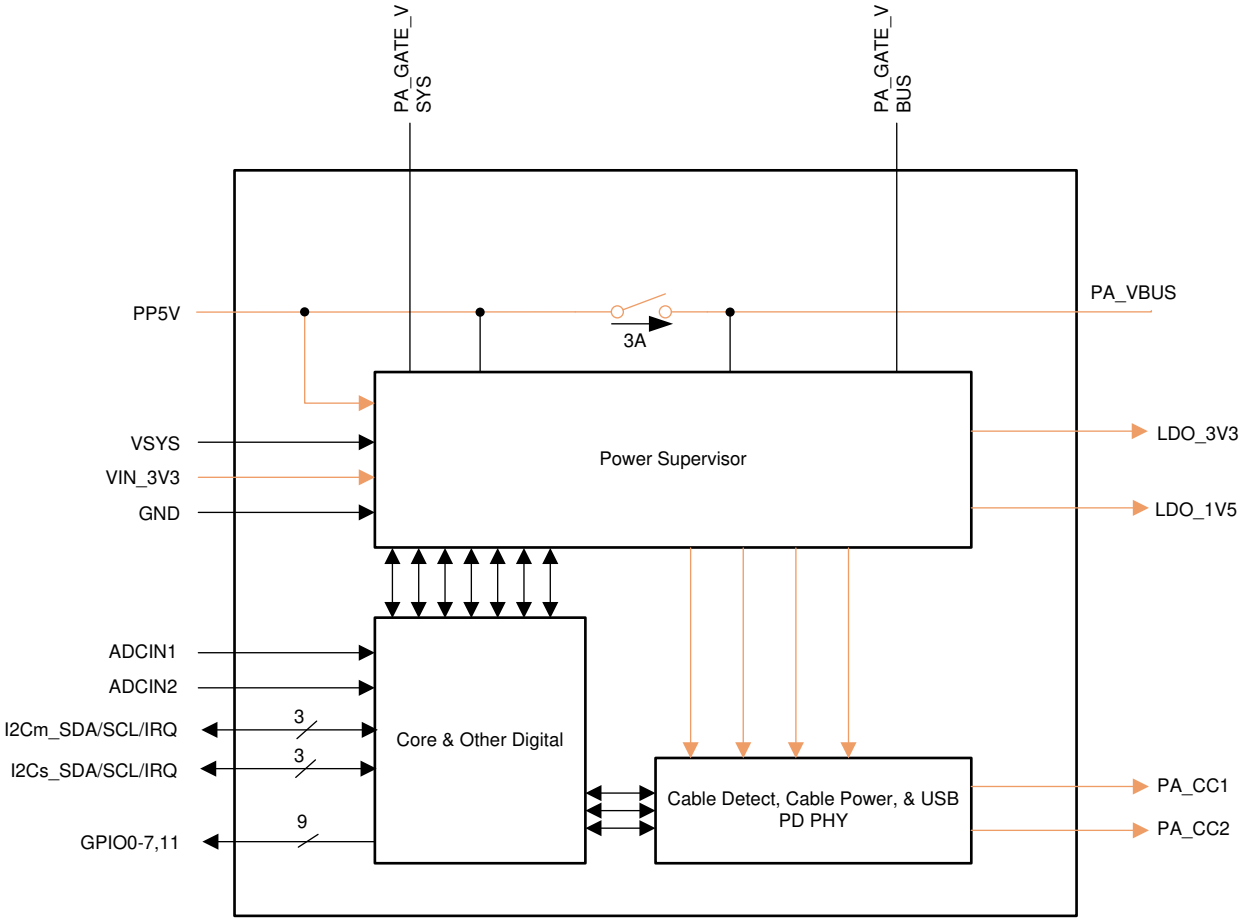

Figure 9-2. TPS25750S

9.3 Feature Description

9.3.1 USB-PD Physical Layer

Figure 9-3 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

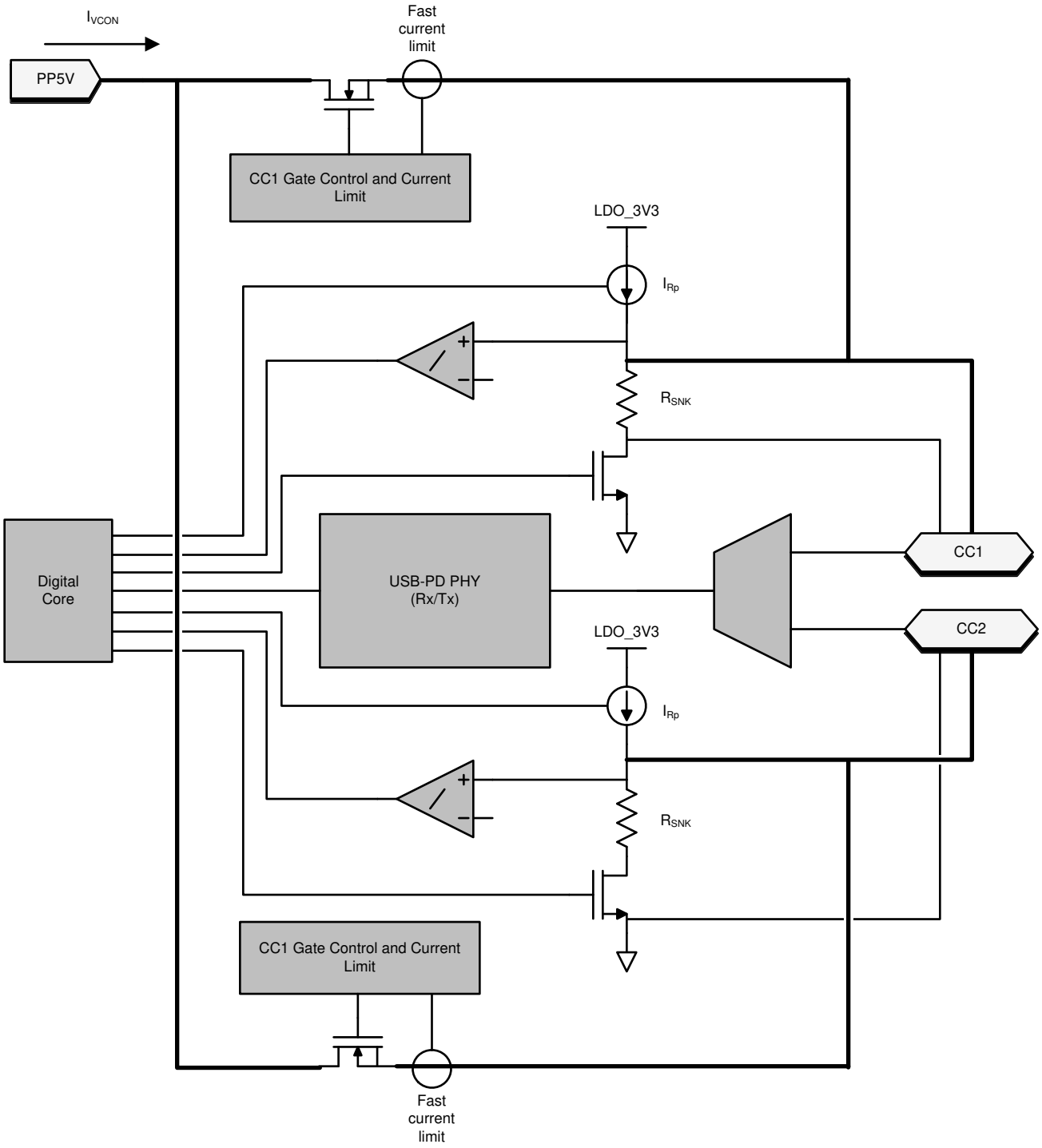

Figure 9-3. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

9.3.1.1 USB-PD Encoding and Signaling

Figure 9-4 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 9-5 illustrates the high-level block diagram of the baseband USB-PD receiver.

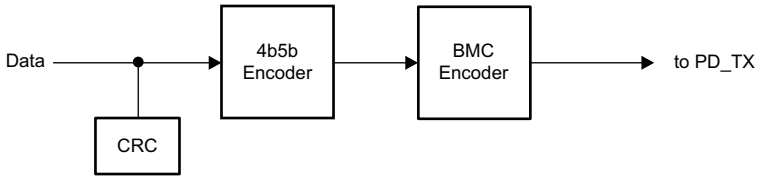

Figure 9-4. USB-PD Baseband Transmitter Block Diagram

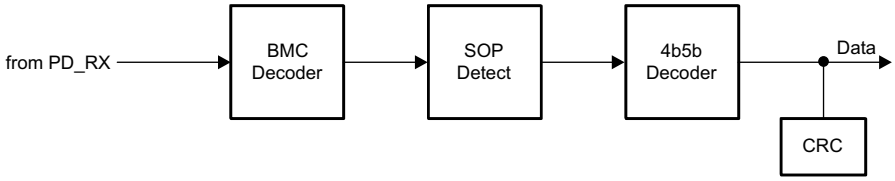

Figure 9-5. USB-PD Baseband Receiver Block Diagram

9.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25750 is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 9-6 illustrates Biphase Mark Coding.

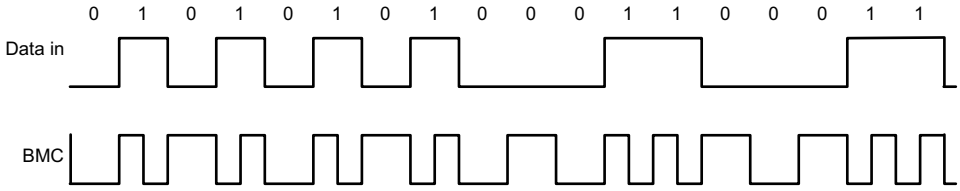

Figure 9-6. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

9.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

9.3.1.4 USB-PD BMC Transmitter

The TPS25750 transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when it is not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. Figure 9-7 shows the USB-PD BMC TX and RX driver block diagram.

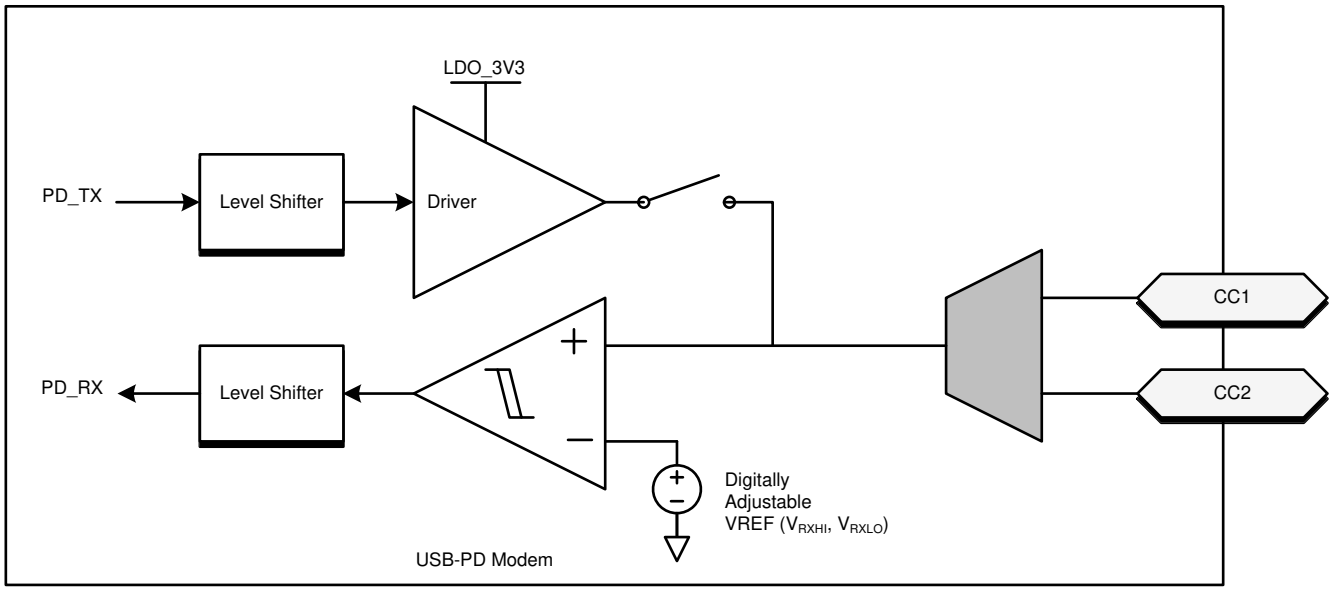

Figure 9-7. USB-PD BMC TX/Rx Block Diagram

Figure 9-8 shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This means that the DC bias can be above or below the VOH of the transmitter driver.

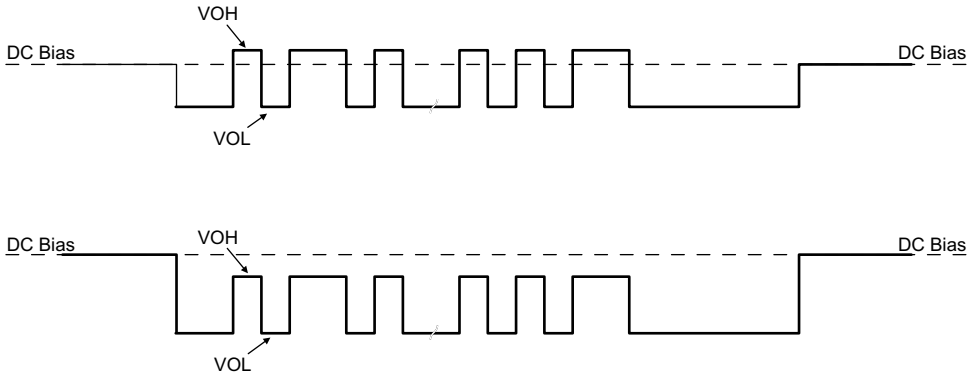

Figure 9-8. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

Figure 9-9 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

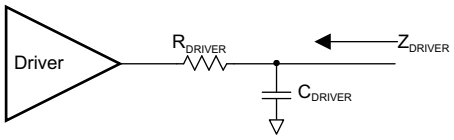

Figure 9-9. ZDRIVER Circuit

9.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS25750 receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 9-10 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

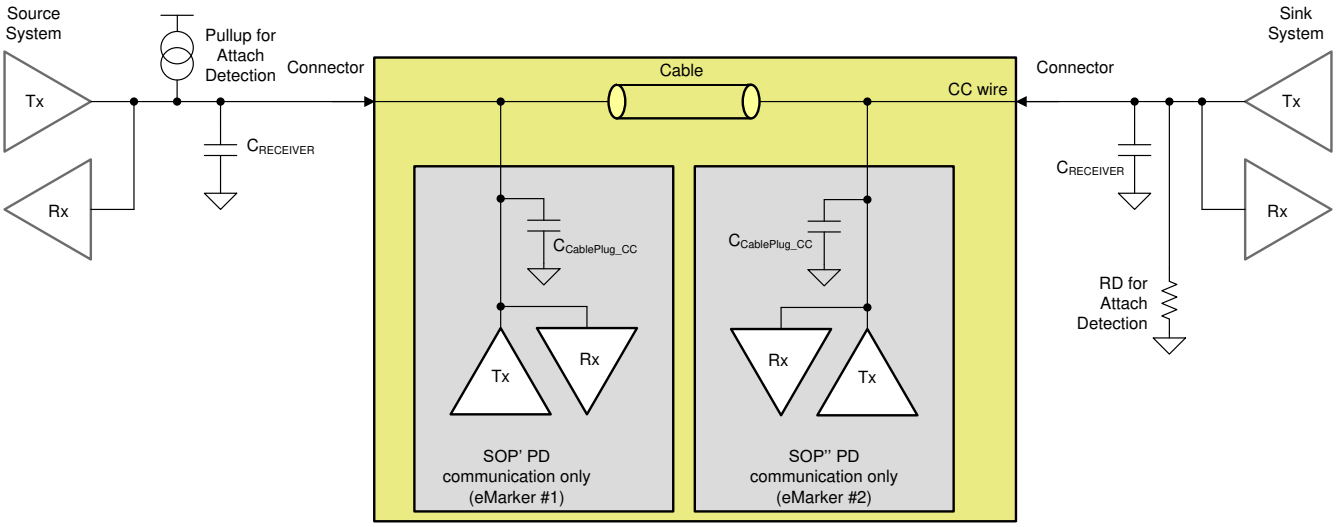

Figure 9-10. Example USB-PD Multi-Drop Configuration

9.3.1.6 Squelch Receiver

The TPS25750 has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification. The CC line is deemed active (that is not idle) when a minimum of NCOUNT transitions occur at the receiver within a time window of TTRANWIN. After waiting TTRANWIN without detecting NCOUNT transitions, the bus is declared idle. The squelch receiver output reflects the state of the CC pin regardless of the source of the tranmission.

9.3.2 Power Management

The TPS25750 power management block receives power and generates voltages to provide power to the TPS25750 internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in Figure 9-11.

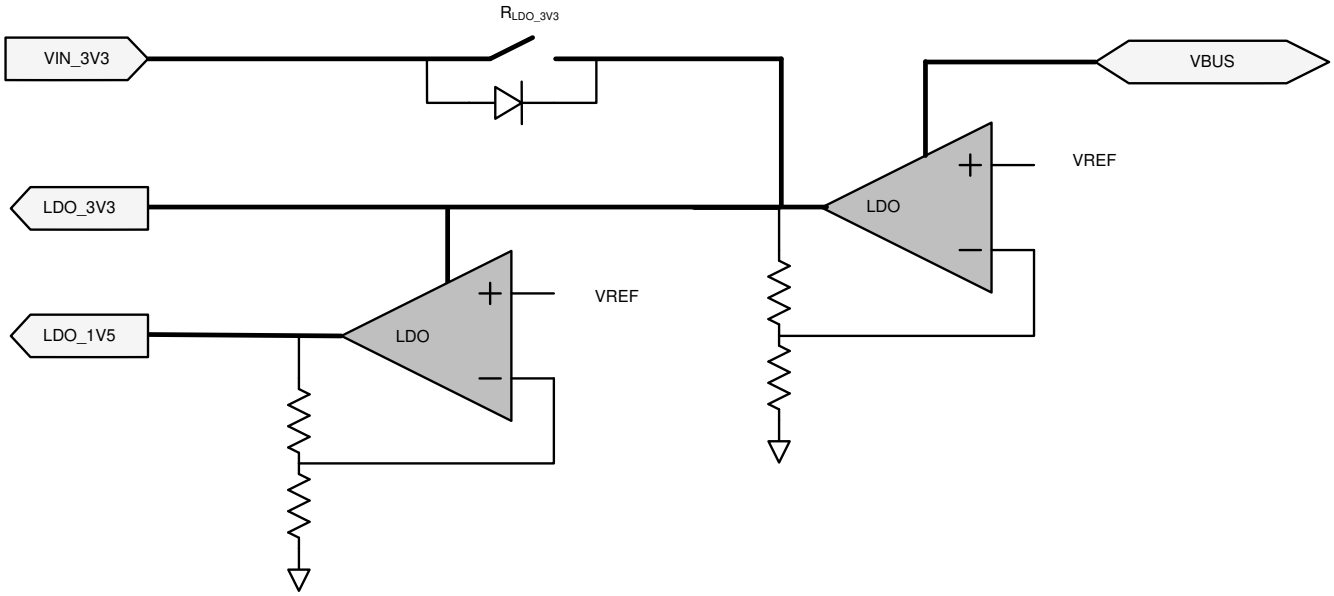

Figure 9-11. Power Supplies

The TPS25750 is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5-V core digital circuitry. When VIN_3V3 power is unavailable and power is available on VBUS, it is referred to as the dead-battery start-up condition. In a dead-battery start-up condition, the TPS25750 opens the VIN_3V3 switch until the host clears the dead-battery flag through I^2C. Therefore, the TPS25750 is powered from the VBUS input with the higher voltage during the dead-battery start-up condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

9.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

9.3.2.2 VBUS LDO

The TPS25750 contains an internal high-voltage LDO which is capable of converting VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used when VIN_3V3 is low (the dead-battery condition). The VBUS LDO is powered from VBUS.

9.3.3 Power Paths

The TPS25750 has internal sourcing power paths: PP_5V and PP_CABLE. TPS25750D has a integrated bidirectional high voltage load switch for sinking power path: PPHV. TPS25750S has a high volatge gate driver for sink path control: PP_EXT. Each power path is described in detail in this section.

9.3.3.1 Internal Sourcing Power Paths

Figure 9-12 shows the TPS25750 internal sourcing power paths available in both TPS25750D and TPS25750S. The TPS25750 features two internal 5-V sourcing power paths. The path from PP5V to VBUS is called PP_5V. The path from PP5V to CCx is called PP_CABLE. Each path contains two back-to-back common drain N-FETs, with current clamping protection, overvoltage protection, UVLO protection, and temperature sensing circuitry. PP_5V can conduct up to 3 A continuously, while PP_CABLE can conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that can appear on VBUS.

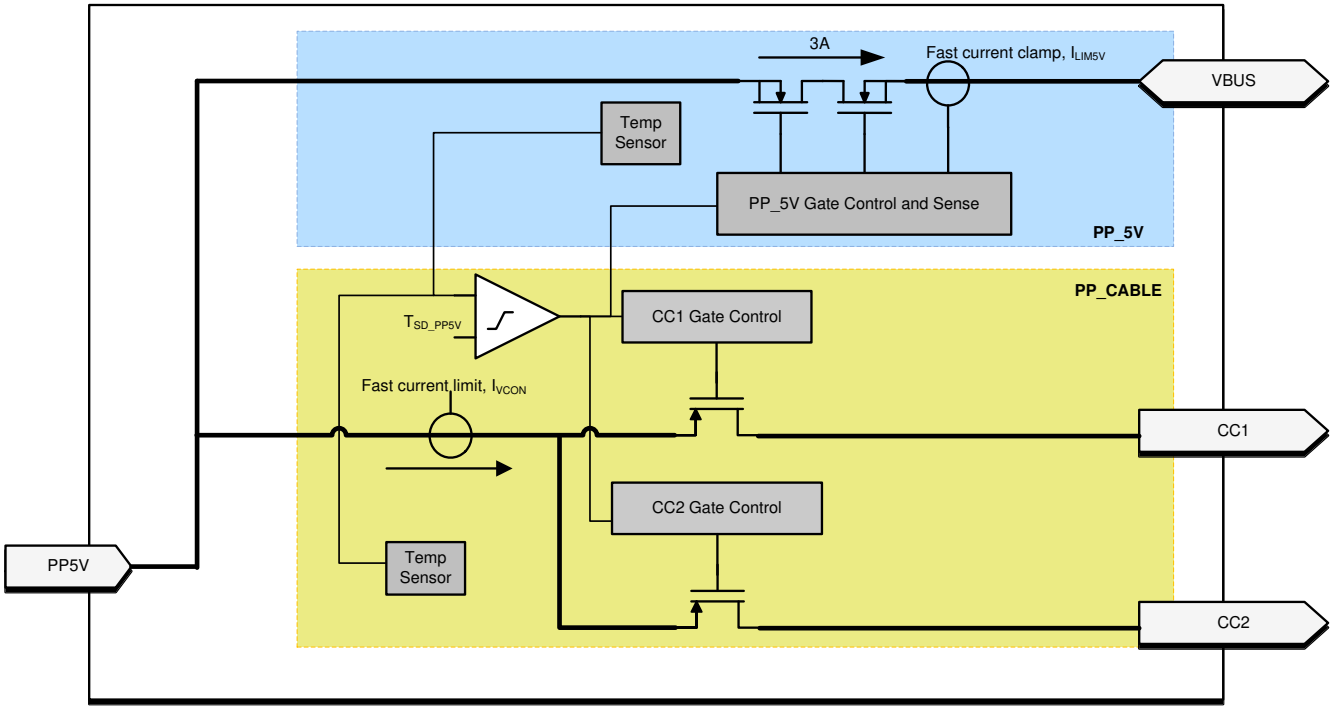

Figure 9-12. Port Power Switches

9.3.3.1.1 PP_5V Current Clamping

The current through the internal PP_5V path are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by application firmware. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS\_PP\_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

9.3.3.1.2 PP_5V Local Overtemperature Shut Down (OTSD)

When PP_5V clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

9.3.3.1.3 PP_5V OVP

The overvoltage protection level is automatically configured based on the expected maximum V_{BUS} voltage, which depends upon the USB PD contract. When the voltage on the VBUS pin of a port exceeds the configured value ($V_{OVP4RCP}$) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_ovp}$ and the port enters into the Type-C ErrorRecovery state.

9.3.3.1.4 PP_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_uvlo}$ and the port that had PP_5V enabled enters into the Type-C ErrorRecovery state.

9.3.3.1.5 PP_5Vx Reverse Current Protection

If $V_{VBUS} - V_{PP5V} > V_{PP\_5V\_RCP}$, then the PP_5V path is automatically disabled within $t_{PP\_5V\_rcp}$. If the RCP condition clears, then the PP_5V path is automatically enabled within t_{ON}.

9.3.3.1.6 PP_CABLE Current Clamp

When enabled and providing VCONN power, the TPS25750 PP_CABLE power switch clamps the current to I_{VCON}. When the current through the PP_CABLE switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source.

9.3.3.1.7 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLE clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_CABLE switch is disabled and latched off within $t_{PP\_CABLE\_off}$. The port then enters the USB Type-C ErrorRecovery state.

9.3.3.1.8 PP_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}), then the PP_CABLE switch is automatically disabled within $t_{PP\_CABLE\_off}$.

9.3.3.2 TPS25750D Internal Sink Path

The TPS25750D has internal controls for internal FETs (GATE_VSYS and GATE_VBUS as shown in Figure 9-13) that require that VBUS_IN be above V_{VBUS_UVLO} before being able to enable the sink path. Figure 9-13 shows a diagram of the sink path. When a sink path is enabled, the circuitry includes a slew rate control loop to ensure that external switches do not turn on too quickly (SS). The TPS25750D senses the PPHV and VBUS voltages to control the gate voltages to enable or disable the FETs.

The sink-path control includes overvoltage protection (OVP) and reverse current protection (RCP).

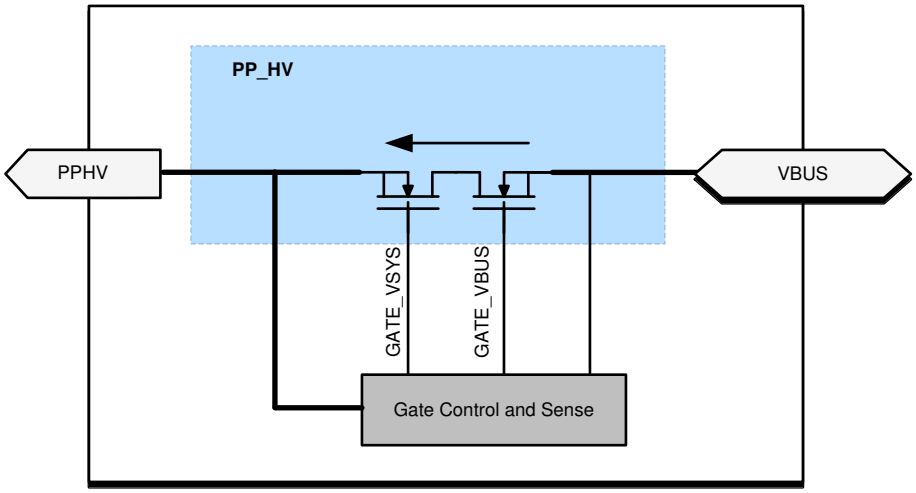

Figure 9-13. Internal Sink Path

9.3.3.2.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures it based on the expected VBUS voltage. If the voltage on VBUS surpasses the configured threshold VOVP4VSYS = VOVP4RCP/rOVP, then GATE_VSYS is automatically disabled within tPPHV_FSD to protect the system. If the voltage on VBUS surpasses the configured threshold VOVP4RCP, then GATE_VBUS is automatically disabled within tPPHV_OVP. When VVBUS falls below VOVP4RCP - VOVP4RCPH, GATE_VBUS is automatically re-enabled within tPPHV_ON since the OVP condition has cleared. This allows two sinking power paths to be enabled simultaneously and GATE_VBUS will be disabled when necessary to ensure that VVBUS remains below VOVP4RCP.

While the TPS25750D is in BOOT mode in a dead-battery scenario (that is VIN_3V3 is low), it handles an OVP condition slightly differently. As long as the OVP condition is present, GATE_VBUS and GATE_VSYS are disabled. Once the OVP condition clears, both GATE_VBUS and GATE_VSYS are re-enabled. Since this is a dead-battery condition, the TPS25750D will be drawing approximately IVIN_3V3, ActSnk from VBUS during this time to help discharge it.

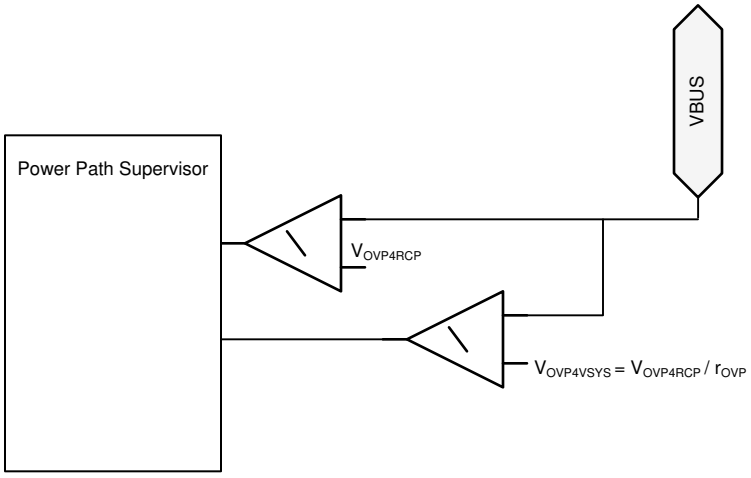

Figure 9-14. Diagram for OVP Comparators

9.3.3.2.2 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the PPHV and VBUS voltages and detects reverse current when the VVSYS surpasses V_{VBUS} by more than V_{RCP}. When the reverse current condition is detected, GATE_VBUS is disabled within tPPHV_RCP. When the reverse current condition is cleared, GATE_VBUS is re-enabled within tPPHV_ON. This limits the amount of reverse current that can flow from PPHV to VBUS through the external N-ch MOSFETs. In reverse current protection mode, the power switch controlled by GATE_VBUS is allowed to behave resistively until the current reaches VRCP/ RPPHV and then blocks reverse current from PPHV to VBUS.

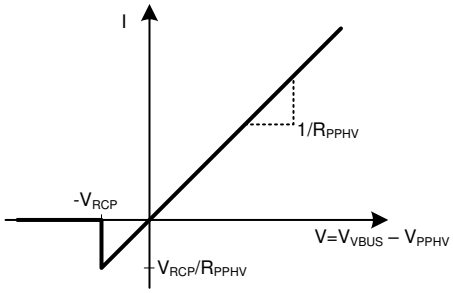

Figure 9-15. Switch I-V Curve for RCP on Sink-path Switches.

9.3.3.2.3 VBUS UVLO

The TPS25750D monitors VBUS voltage and detects when it falls below VVBUS_UVLO. When the UVLO condition is detected, GATE_VBUS is disabled within tPPHV_RCP. When the UVLO condition is cleared, GATE_VBUS is reenabled within tPPHV_ON.

9.3.3.2.4 Discharging VBUS to Safe Voltage

The TPS25750D has an integrated active pulldown (IDSCH) on VBUS for discharging from high voltage to VSAFE0V (0.8 V). This discharge is applied when it is in an Unattached Type-C state.

9.3.3.3 TPS25750S - External Sink Path Control PP_EXT

The TPS25750S has two N-ch gate drivers designed to control a sinking path from VBUS to VSYS. The charge pump for these gate drivers requires VBUS to be above VVBUS_UVLO. When a sink path is enabled, the circuitry includes a slew rate control loop to ensure that external switches do not turn on too quickly (SS). The TPS25750S senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The sink-path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS25750S and the gate pin of the N-ch MOSFET will slow down the turnoff time when OVP or RCP occurs. Any such resistance must be minimized, and not allowed to exceed 3 Ω.

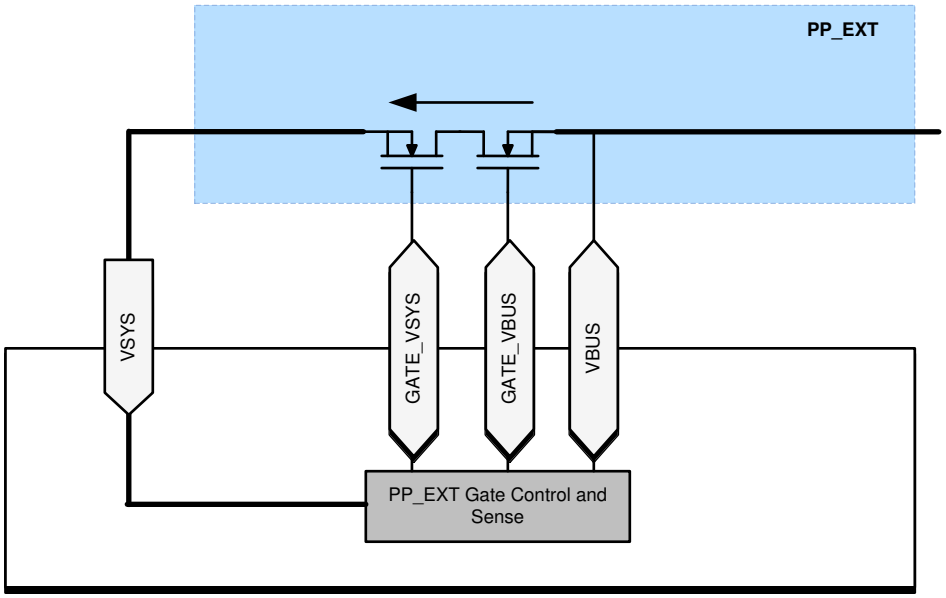

Figure 9-16. PP_EXT External Sink Path Control

Figure 9-17 shows the GATE_VSYS gate driver in more detail.

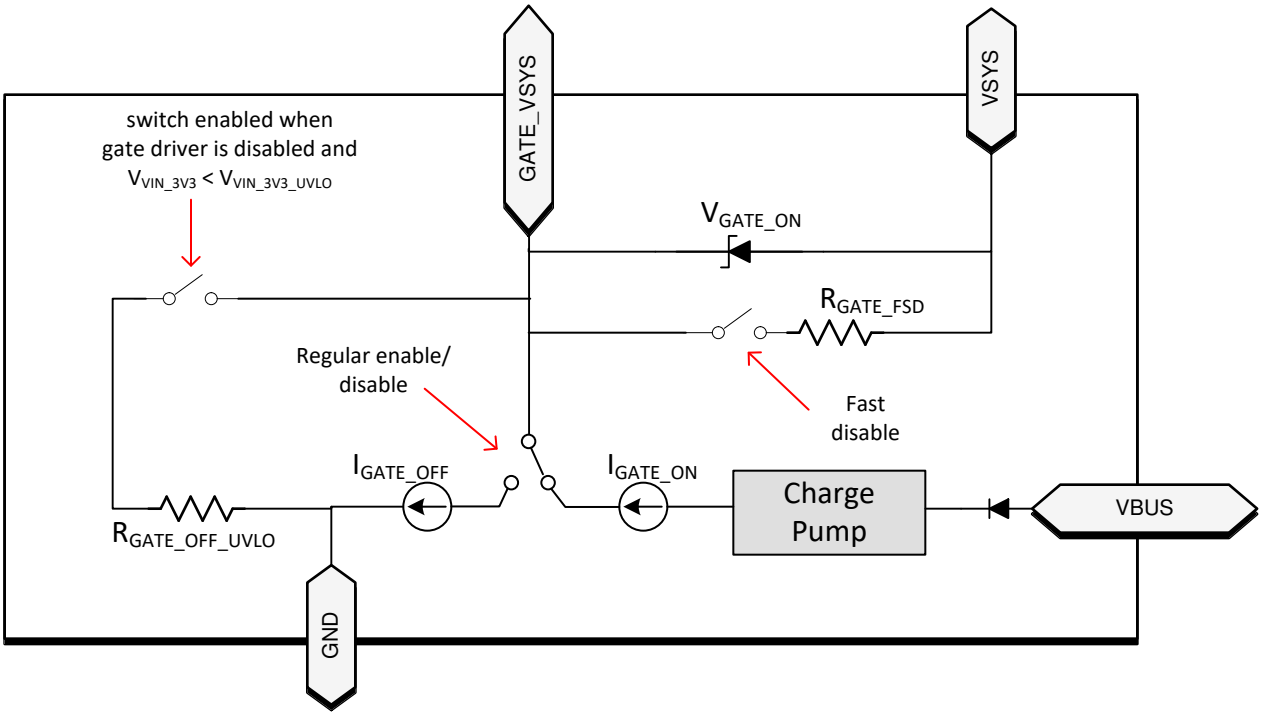

Figure 9-17. Details of the VSYS Gate Driver

9.3.3.3.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures it based on the expected VBUS voltage. If the voltage on VBUS surpasses the configured threshold VOVP4VSYS = VOVP4RCP/rOVP, then GATE_VSYS is automatically disabled within tPPHV_FSD to protect the system. If the voltage on VBUS surpasses the configured threshold VOVP4RCP, then GATE_VBUS is automatically disabled within tPPHV_OVP. When VVBUS falls below VOVP4RCP - VOVP4RCPH, GATE_VBUS is automatically re-enabled within tPPHV_ON since the OVP condition has cleared. This allows two sinking power paths to be enabled simultaneously and GATE_VBUS will be disabled when necessary to ensure that VVBUS remains below VOVP4RCP.

While the TPS25750D is in BOOT mode in a dead-battery scenario (that is VIN_3V3 is low), it handles an OVP condition slightly differently. As long as the OVP condition is present, GATE_VBUS and GATE_VSYS are disabled. Once the OVP condition clears, both GATE_VBUS and GATE_VSYS are re-enabled. Since this is a dead-battery condition, the TPS25750D will be drawing approximately IVIN_3V3, ActSnk from VBUS during this time to help discharge it.

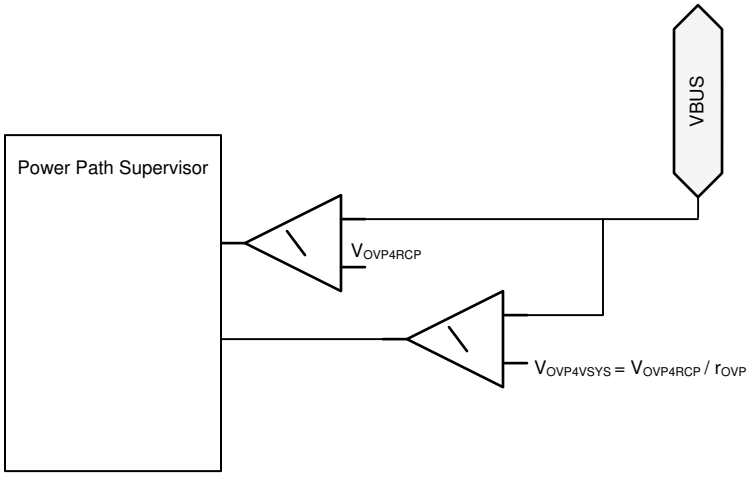

Figure 9-18. Diagram for OVP Comparators

9.3.3.3.1.1 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the PPHV and VBUS voltages and detects reverse current when the VVSYS surpasses V_{VBUS} by more than V_{RCP}. When the reverse current condition is detected, GATE_VBUS is disabled within tPPHV_RCP. When the reverse current condition is cleared, GATE_VBUS is re-enabled within tPPHV_ON. This limits the amount of reverse current that can flow from PPHV to VBUS through the external N-ch MOSFETs. In reverse current protection mode, the power switch controlled by GATE_VBUS is allowed to behave resistively until the current reaches VRCP/ RPPHV and then blocks reverse current from PPHV to VBUS.

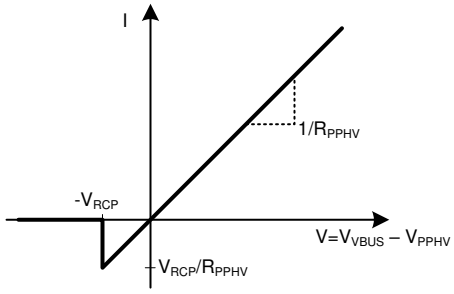

Figure 9-19. Switch I-V Curve for RCP on Sink-path Switches.

9.3.3.3.1.2 VBUS UVLO

The TPS25750D monitors VBUS voltage and detects when it falls below VVBUS_UVLO. When the UVLO condition is detected, GATE_VBUS is disabled within tPPHV_RCP. When the UVLO condition is cleared, GATE_VBUS is reenabled within tPPHV_ON.

9.3.3.3.1.3 Discharging VBUS to Safe Voltage

The TPS25750D has an integrated active pulldown (IDSCH) on VBUS for discharging from high voltage to VSAFE0V (0.8 V). This discharge is applied when it is in an Unattached Type-C state.

9.3.4 Cable Plug and Orientation Detection

Figure 9-20 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

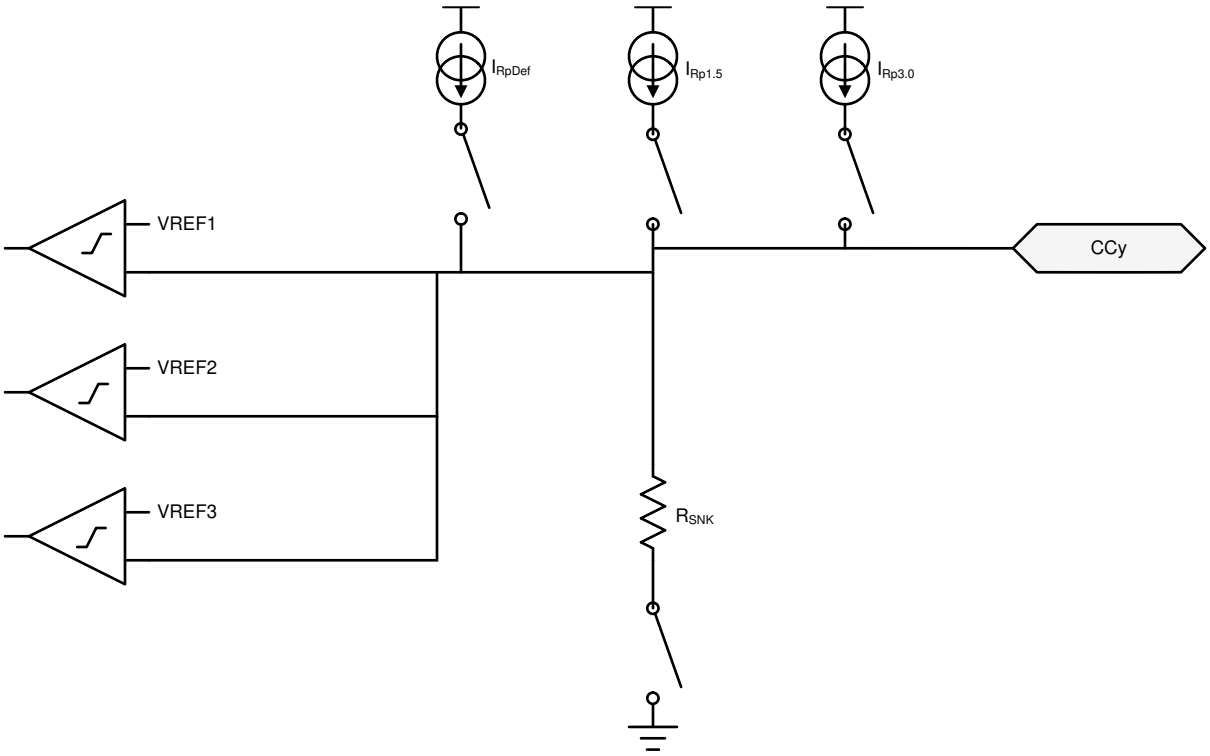

Figure 9-20. Plug and Orientation Detection Block

9.3.4.1 Configured as a Source

When configured as a source, the TPS25750 detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS25750 monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 9-1 shows the Cable Detect States for a Source.

Table 9-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).

Table 9-1. Cable Detect States for a Source (continued)

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either CCy pin for detach.

When a TPS25750 port is configured as a Source, a current I_{RpDef} is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin, a pulldown resistance of Rd to GND exists. The current I_{RpDef} is then forced across the resistance Rd, generating a voltage at the CCy pin. The TPS25750 applies I_{RpDef} until it closes the switch from PP5V to VBUS, at which time application firmware can change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the CCy pin is connected to an active cable VCONN input, the pulldown resistance is different (Ra). In this case, the voltage on the CCy pin will lower the PD controller recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

9.3.4.2 Configured as a Sink

When a TPS25750 port is configured as a Sink, the TPS25750 presents a pulldown resistance R_{SNK} on each CCy pin and waits for a Source to attach and pull up the voltage on the pin. The Sink detects an attachment by the presence of VBUS and determines the advertised current from the Source based on the voltage on the CCy pin.

9.3.4.3 Configured as a DRP

When a TPS25750 port is configured as a DRP, the TPS25750 alternates the CCy pins of the port between the pulldown resistance, R_{SNK}, and pullup current source, I_{Rp}.

9.3.4.4 Dead Battery Advertisement

The TPS25750 supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. TPS25750 hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS.

9.3.5 Overvoltage Protection (CC1, CC2)

The TPS25750 detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP_CABLE within $t_{PP\_CABLE\_FSD}$ and disable the USB PD transmitter.

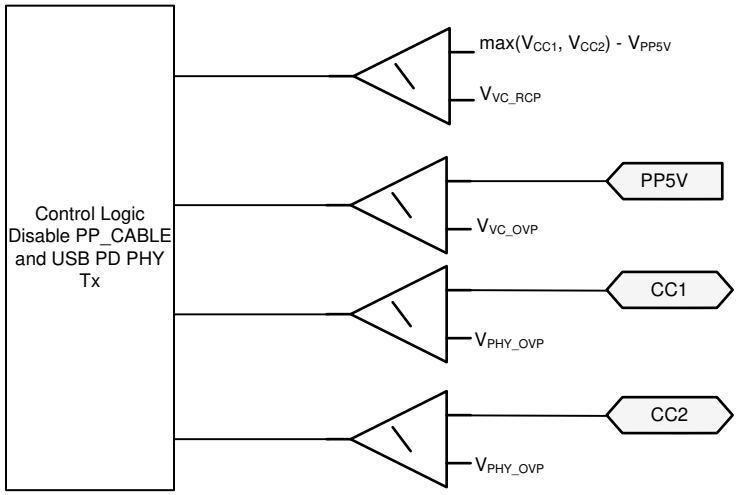

Figure 9-21. Overvoltage and Reverse Current Protection for CC1 and CC2

9.3.6 ADC

The TPS25750 ADC is shown in Figure 9-22. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

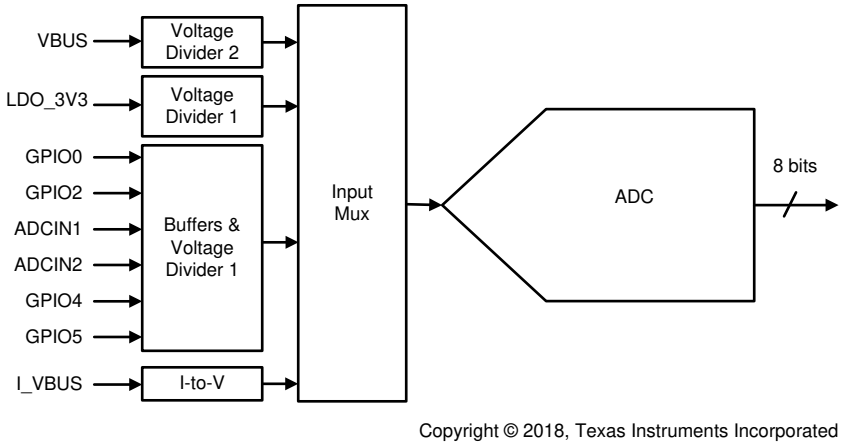

Figure 9-22. SAR ADC

9.3.7 BC 1.2 (USB_P, USB_N)

The TPS25750 supports BC 1.2 as a Portable Device or Downstream Port using the hardware shown in Figure 9-23.

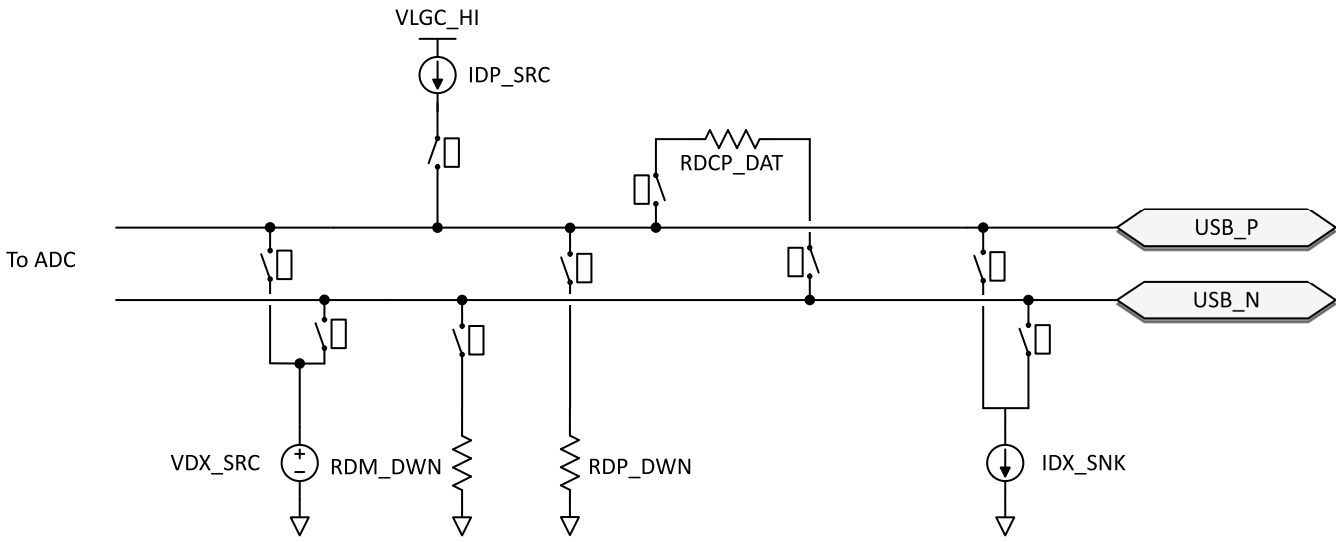

Figure 9-23. BC1.2 Hardware Components (External for DRP)

9.3.8 Digital Interfaces

The TPS25750 contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include one I^2C Master, one I2C Slave and additional GPIOs.

9.3.8.1 General GPIO

GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input . The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V5 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

Table 9-2. GPIO Functionality Table

Pin Name	Type	Special Functionality
GPIO0	I/O	General-purpose input or output
GPIO1	I/O	General-purpose input or output
GPIO2	I/O	General-purpose input or output
GPIO3	I/O	General-purpose input or output
GPIO4	I/O	D+, or used as a general-purpose input or output
GPIO5	I/O	D-, or used as a general-purpose input or output
GPIO6	I/O	General-purpose input or output
GPIO7	I/O	General-purpose input or output
$\overline{\text{I2Cs\_IRQ}}$(GPIO10)	O	IRQ for optional I2Cs, or used as a general-purpose output
GPIO11	O	General-purpose output
$\overline{\text{I2Cm\_IRQ}}$(GPIO12)	I	IRQ for I2Cm, or used as a general-purpose input

9.3.8.2 I^2C Interface

The TPS25750 features two I^2C interfaces that uses an I^2C I/O driver like the one shown in Figure 9-24. This I/O consists of an open-drain output and an input comparator with de-glitching.

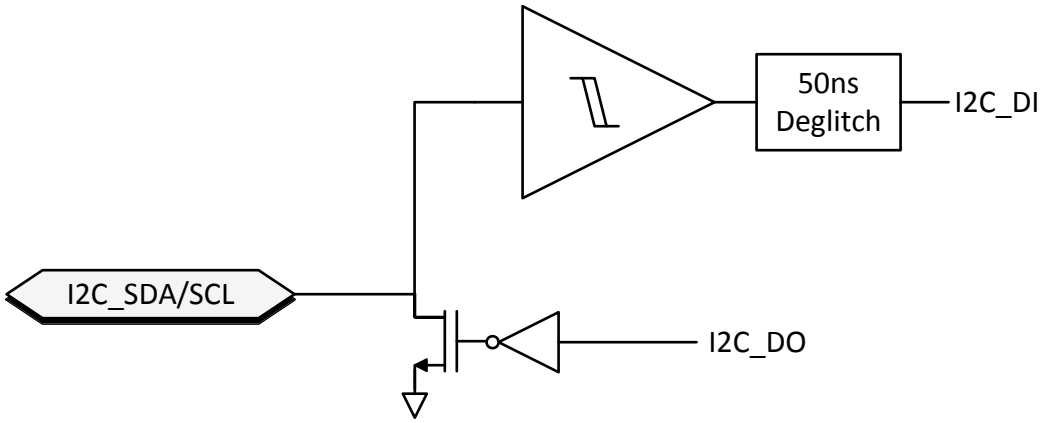

Figure 9-24. I²C Buffer

9.3.9 Digital Core

Figure 9-25 shows a simplified block diagram of the digital core.

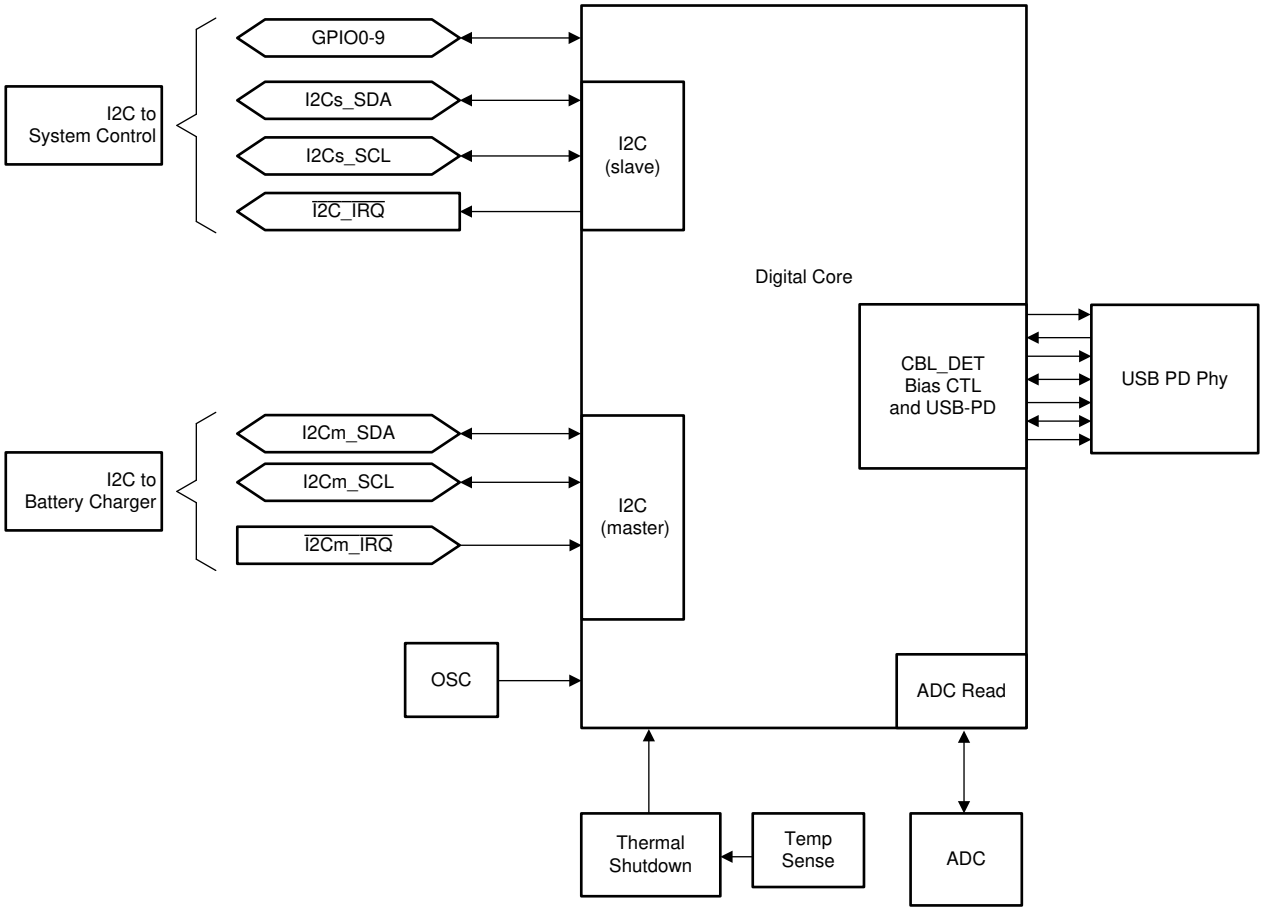

Figure 9-25. Digital Core Block Diagram

9.3.10 I²C Interface

The TPS25750 has one I2C slave interface ports: I2Cs. I2C port I2Cs is comprised of the I2Cs_SDA, I2Cs_SCL, and $\overline{\text{I2Cs\_IRQ}}$ pins. This interface provide general status information about the TPS25750, as well as the ability to control the TPS25750 behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS25750 is in 'APP ' mode it is recommended to use Standard Mode or Fast Mode (that is a clock speed no higher than 400 kHz). However, in the 'BOOT' mode when a patch bundle is loaded Fast Mode Plus may be used (see fSCLS).

The TPS25750 has one I^{2}C master interface port. I^{2}C is comprised of the I2C_SDA and I2C_SCL pins. This interface can be used to read from or write to external slave devices.

During boot, the TPS25750 attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit slave address of 0x50. The EEPROM should be at least 32 kilo-bytes.

Table 9-3. I^{2}C Summary

I^{2}C BUS	TYPE	TYPICAL USAGE
I2Cs	Slave	Optionally can be connected to an external MCU. Also used to load the patch and application configuration.
I2Cm	Master	Connect to a I^{2}C EEPROM, Battery Charger. Use the LDO_3V3 pin as the pullup voltage. Multi-master configuration is not supported.

9.3.10.1 I^{2}C Interface Description

The TPS25750 supports Standard and Fast mode I^{2}C interfaces. The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I^{2}C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 9-26 shows the start and stop conditions of the transfer. Figure 9-27 shows the SDA and SCL signals for transferring a bit. Figure 9-28 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

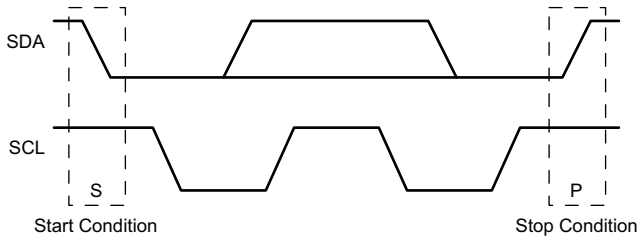

Figure 9-26. I^{2}C Definition of Start and Stop Conditions

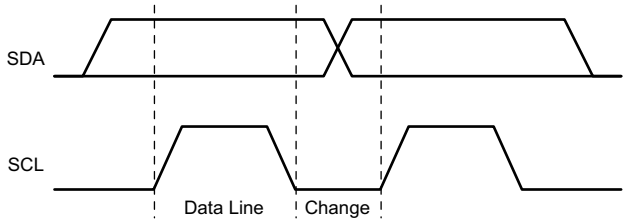

Figure 9-27. I²C Bit Transfer

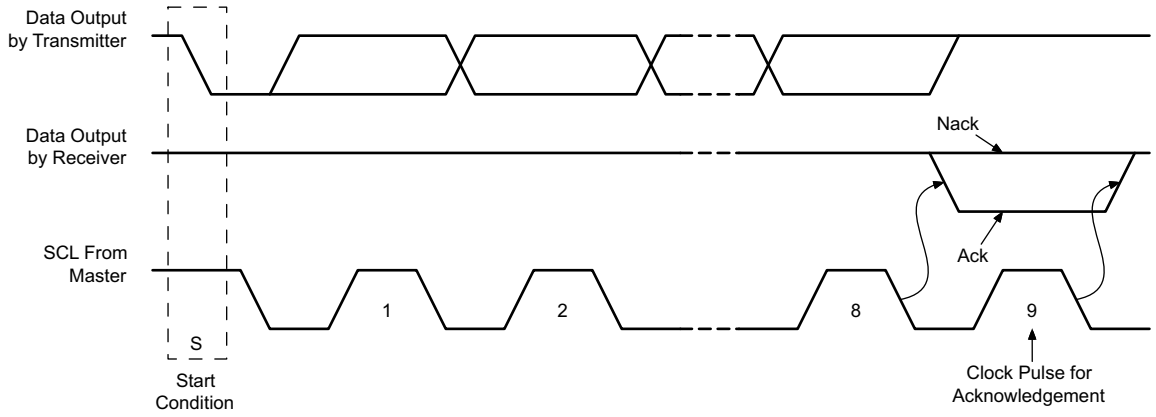

Figure 9-28. I²C Acknowledgment

9.3.10.1.1 I²C Clock Stretching

The TPS25750 features clock stretching for the I²C protocol. The TPS25750 slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

9.3.10.1.2 I²C Address Setting

The host should only use I2Cs_SCL/SDA for loading a patch bundle. Once the boot process is complete, the port has a unique slave address on the I2Cm_SCL/SDA bus as selected by the ADCINx pins.

Table 9-4. I²C Default Slave Address for I2Cs_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	Slave Address								Available During BOOT
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	0	1	0	0	0	0	0	R/W	Yes
#2	0	1	0	0	0	0	1	R/W	Yes
#3	0	1	0	0	0	1	0	R/W	Yes
#4	0	1	0	0	0	1	1	R/W	Yes

(1) See *Pin Strapping to Configure Default Behavior* details about ADCIN1 and ADCIN2 decoding.

9.3.10.1.3 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS25750. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 9-29 and Figure 9-30 show the write and read protocol for the I²C slave interface, and a key is included in Figure 9-31 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

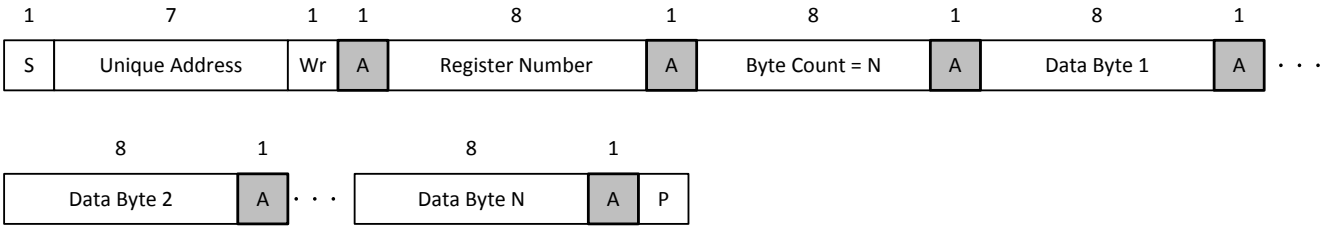

Figure 9-29. I²C Unique Address Write Register Protocol

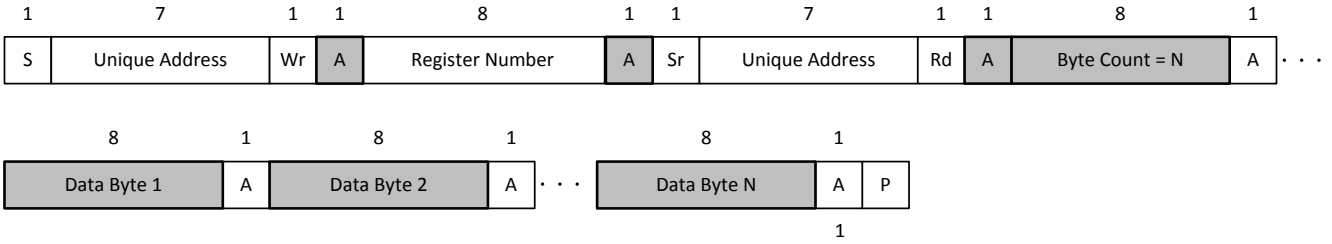

Figure 9-30. I²C Unique Address Read Register Protocol

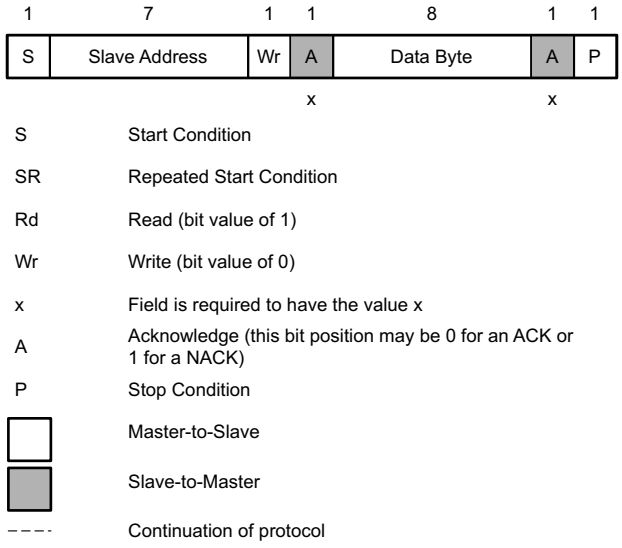

Figure 9-31. I²C Read/Write Protocol Key

9.4 Device Functional Modes

9.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device will read the ADCINx pins and set the configurations based on the table below. It then attempts to load a configuration from an external EEPROM on the I2Cm bus. If no EEPROM is detected, then the device will wait for an external host to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, it cannot be shared for multiple devices. The external EEPROM shall be at 7-bit slave address 0x50.

Table 9-5. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value[2]	ADCIN2 decoded value[2]	I²C address Index[1]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 9-5. Device Configuration using ADCIN1 and ADCIN2 (continued)

ADCIN1 decoded value[2]	ADCIN2 decoded value[2]	I²C address Index[1]	Dead Battery Configuration
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V. This cannot be used when a patch is loaded from EEPROM. This option is not recommended for systems that can boot from 5 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode. This is recommended when the application loads the patch from EEPROM.
0	0	#2	
6	0	#3	
5	7	#4	

(1) See *I²C Address Setting* to see the exact meaning of I²C Address Index.
(2) See *Pin Strapping to Configure Default Behavior* for how to configure a given ADCINx decoded value.

9.4.2 Power States

The TPS25750 can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in Table 9-6. The device will automatically transition between the three power states based on the circuits that are active and required. See Figure 9-32. In the Sleep state, the TPS25750 will detect a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I^2C transactions
- Voltage alert
- Fault alert

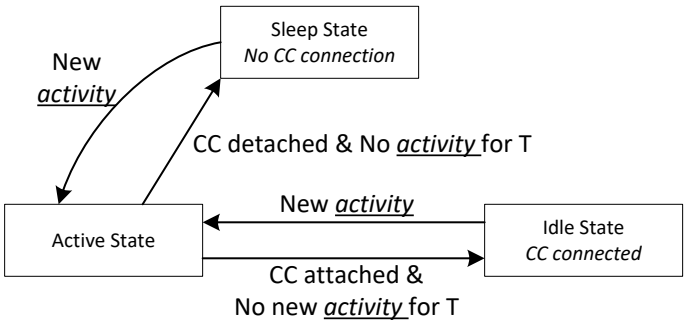

Figure 9-32. Flow Diagram for Power States

Table 9-6. Power Consumption States

	ACTIVE SOURCE MODE(1)	ACTIVE SINK MODE(5)	IDLE SOURCE MODE	IDLE SINK MODE	MODERN STANDBY SOURCE MODE(3)	MODERN STANDBY SINK MODE(4)	SLEEP MODE(2)
PP_5V	enabled	disabled	enabled	disabled	enabled	disabled	disabled
PP_HV (TPS25750D)	disabled	enabled	disabled	enabled	disabled	disabled	disabled
PP_EXT (TPS25750S)	disabled	enabled	disabled	enabled	disabled	disabled	disabled
PP_CABLE	enabled	enabled	enabled	enabled	disabled	disabled	disabled
external CC1 termination	Rd	Rp 3.0A	Rd	Rp 3.0A	open	open	open
external CC2 termination	open	open	open	open	open	open	open

(1) This mode is used for: $I_{VIN\_3V3,ActSrc}$.
(2) This mode is used for: $I_{VIN\_3V3,Sleep}$
(3) This mode is used for: $P_{MstbySrc}$
(4) This mode is used for: $P_{MstbySnk}$
(5) This mode is used for: $I_{VIN\_3V3,ActSnk}$

9.4.3 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25750 during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground.

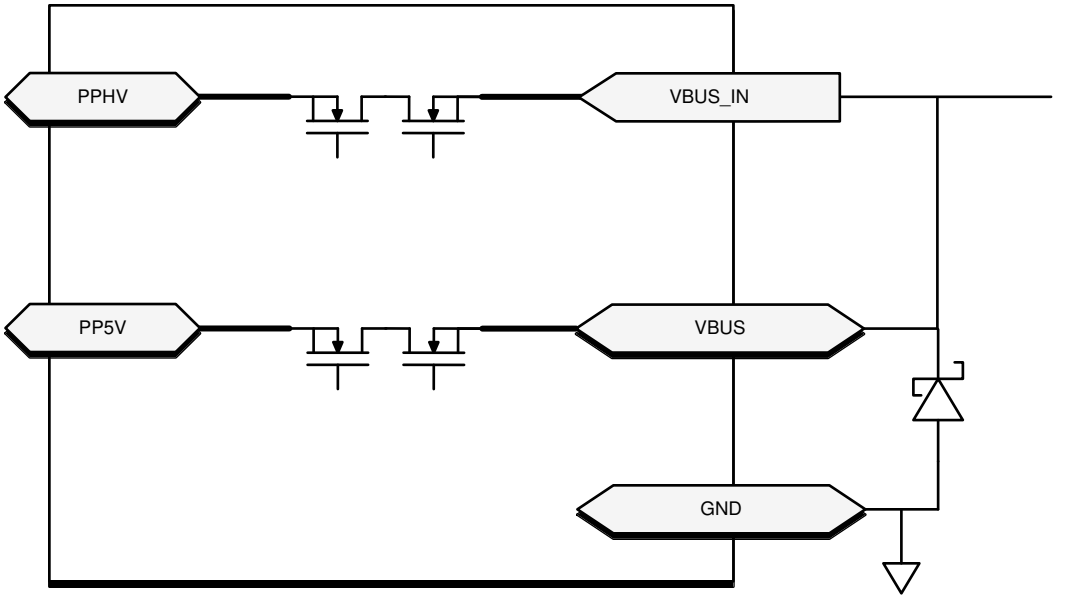

Figure 9-33. TPS25750D Schottky for Current Surge Protection

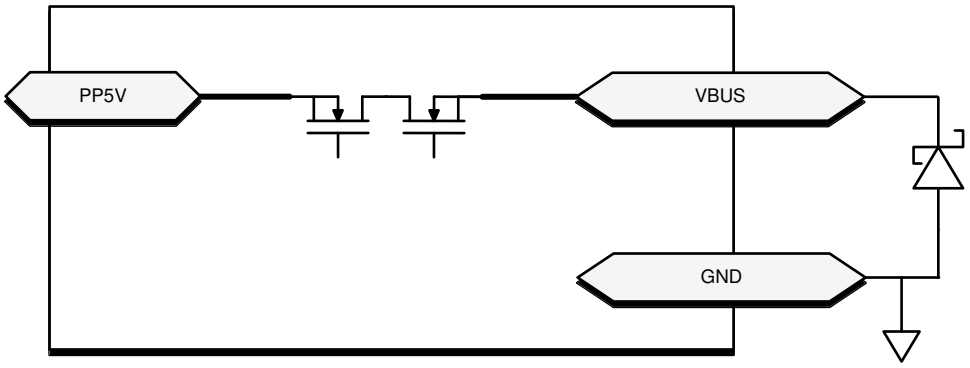

Figure 9-34. TPS25750S Schottky for Current Surge Protection

9.4.4 Thermal Shutdown

The TPS25750 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. Once the temperature falls by at least T_{SDH_PP5V}, the path can be configured to resume operation or remain disabled until re-enabled by firmware.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS25750 is a stand-alone Type-C PD controller for power-only USB-PD applications. Initial device configuration is configured from an external EEPROM through a firmware configuration bundle loaded on to the device during boot.The bundle is loaded over I ^{2}C from an external EEPROM. The TPS25750 firmware configuration can be customized for each specific application. The firmware configuration can be generated through the Application Customization Tool.

The TPS25750 works very well in single port power applications supporting the following PD architectures.

- Designs for both Power Provider (Source) and Power Consumer (Sink)
- Designs for Power Consumer (Sink)

An external EEPROM is required to download a pre-configured firmware on the TPS25750 device through the I ^{2}C interface.

The TPS25750 firmware can be configured using the Application Customization Tool for the application-specific PD charging architecture requirements and data roles. The Tool also provides additional optional firmware configuration that integrates control for select Battery Charger Products (BQ). The TPS25750 I ^{2}C Master interfaces with the Battery Chargers with pre-configured GPIO settings and I^{2}C master events. The Application Customization Tool available with the TPS25750 provides details of the supported Battery Charger Products (BQ).

10.2 Typical Application

10.2.1 USB-PD Power Application Design Considerations

10.2.1.1 Supported Power Configurations

The Application Customization Tool available with TPS25750 lets the user select one of the following Power Application configurations and generates a pre-configured firmware.

Figure 10-1 shows the Power Source and Sink configuration when the TPS25750 is connected to a 5-V DC.

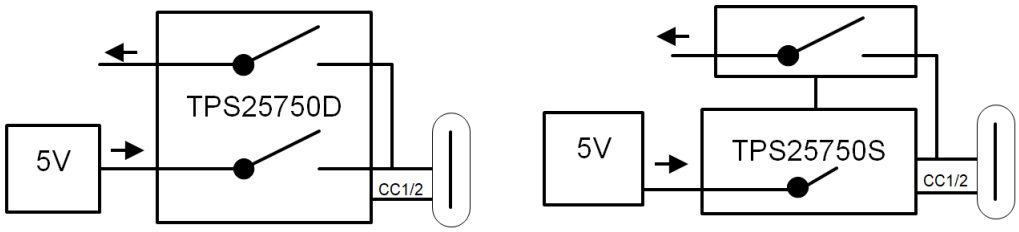

Figure 10-1. Power Source and Sink Configuration with 5-V DC

Figure 10-2 shows the Power Source and Sink configuration when the Battery Charger (BQ) is connected to the high voltage power path.

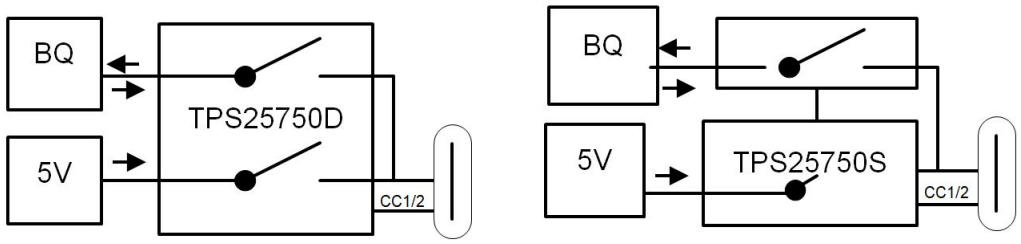

Figure 10-2. Power Source and Sink configuration with the Battery Charger (BQ)

Figure 10-3 shows the configuration where the a 5-V DC is connected to the source path and a Battery Charger (BQ) is connected to the sink path.

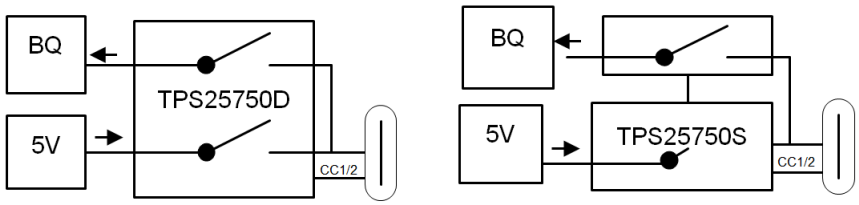

Figure 10-3. Power Source and Sink configuration with 5V DC and Battery Charger (BQ)

In a Sink Only Configuration, the TPS25750 can be used as shown in Figure 10-4.

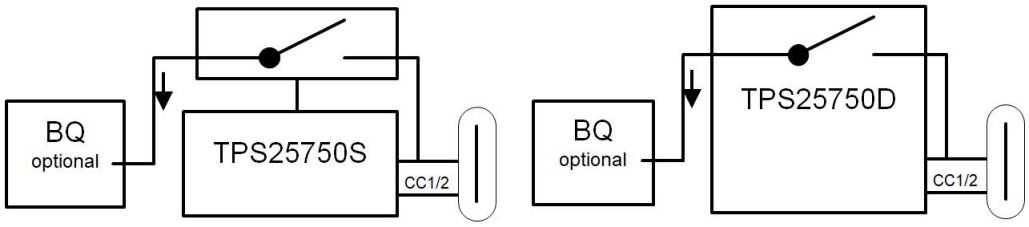

Figure 10-4. Power Consumer (Sink) Only Configuration

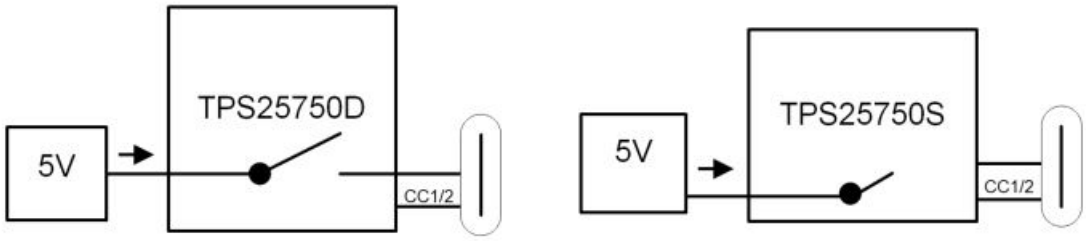

Figure 10-5. Power Source Only Configuration

In a Source Only Configuration, the TPS25750 can be used with a 5V source as shown in Figure 10-5

10.2.2 Application Block Diagram

Figure 10-6 shows the system block diagram for TPS25750D connected to a supported Battery Charger (BQ).

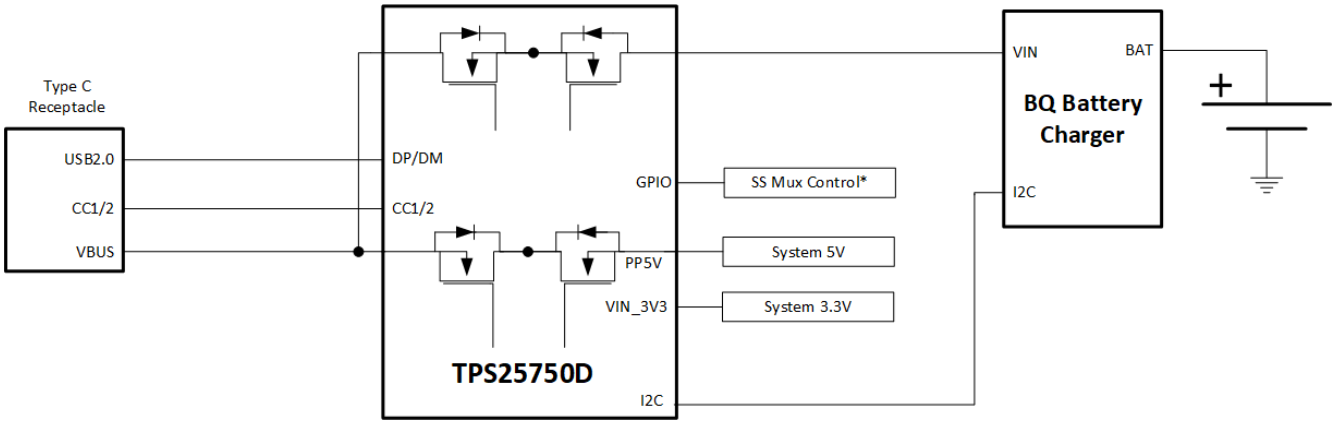

Figure 10-6. Power Only Battery Charger Application Block Diagram

10.2.3 Type-C VBUS Design Considerations

USB Type-C and PD allows for voltages up to 20 V with currents up to 5 A. This introduces power levels that can damage components touching or hanging off of VBUS. Under normal conditions, all high power PD contracts must start at 5 V and then transition to a higher voltage. However, there are some devices that are not compliant to the USB Type-C and Power Delivery standards and can have 20 V on VBUS. This can cause a 20-V hot plug that can ring above 30 V. Adequate design considerations are recommended below for these non-compliant devices.

10.2.3.1 Design Requirements

Table 10-1 shows VBUS conditions that can be introduced to a USB Type-C and PD Sink. The system should be able to handle these conditions to ensure that the system is protected from non-compliant, damaged USB PD sources, or both. A USB Sink should be able to protect from the following conditions being applied to its VBUS. *Detailed Design Procedure* explains how to protect from these conditions.

Table 10-1. VBUS Conditions

CONDITION	VOLTAGE APPLIED
Abnormal VBUS Hot Plug	4 V - 21.5 V
VBUS Transient Spikes	4 V - 43 V

10.2.3.2 Detailed Design Procedure

10.2.3.2.1 Type-C Connector VBUS Capacitors

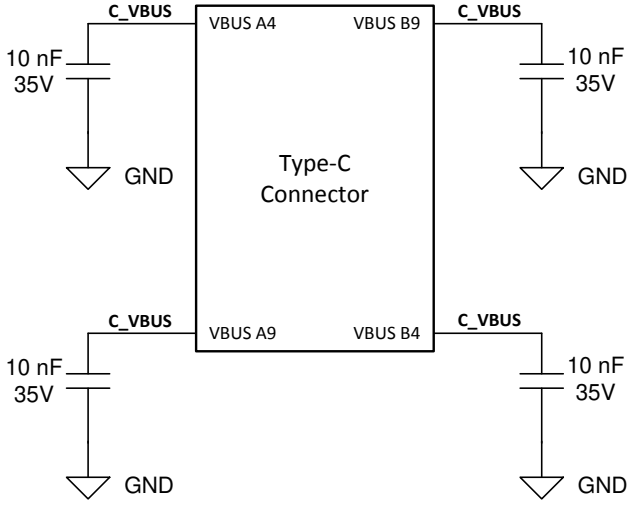

Figure 10-7. Type-C Connector VBUS Capacitors

The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have a very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

10.2.3.2.2 TPS25750 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents can cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough, it can damage the body diodes of IC devices. Ideally, a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS can ring below GND which can damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS25750 is the only device connected to VBUS, place the Schottky Diode close to the VBUS pin of the TPS25750. Figure 10-9 and Figure 10-10 show a short condition with and without a Schottky diode on VBUS. Without the Schottky diode, VBUS rings 2-V below GND and oscillates after settling to 0 V. With the Schottky diode, VBUS drops 750 mV below GND (Schottky diode Vf) and the oscillations are minimized.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system. A TVS diode can also act as a “pseudo schottky diode” as they will also start to conduct when VBUS goes below GND.

10.2.3.2.3 VBUS Snubber Circuit

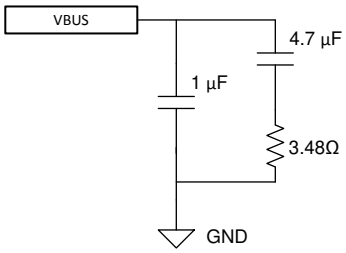

Figure 10-8. VBUS Snubber

Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is a great solution because in general, it is much smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the overvoltage directly, it changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF. The RC snubber values chosen support up to 4-m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7-µF capacitor in series with a 3.48-Ω resistor. In parallel with the RC Snubber a 1-µF capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit is shown in Figure 10-8.

10.2.4 Application Curves

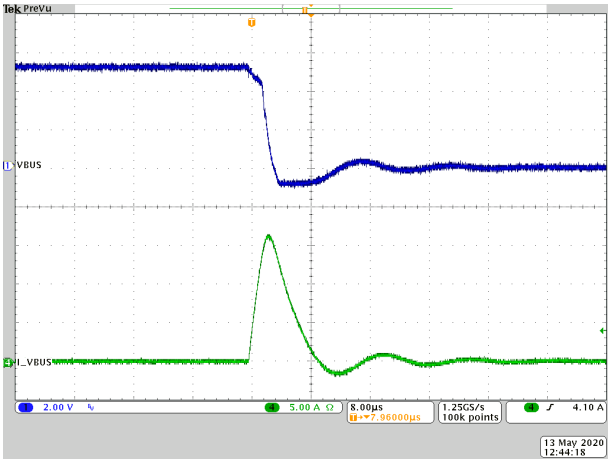

Figure 10-9. VBUS Short to Ground (Zoomed In)

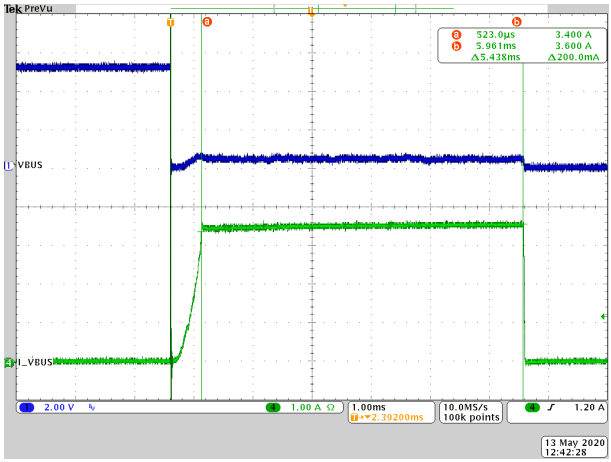

Figure 10-10. VBUS Short to Ground (Zoomed Out)

11 Power Supply Recommendations

11.1 3.3-V Power

11.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS25750 device. The VIN_3V3 switch (see *Power Management*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3-V supply is available and the dead-battery flag is cleared. The recommended capacitance C_{VIN_3V3} (see *Recommended Capacitance*) should be connected from the VIN_3V3 pin to the GND pin).

11.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see *Recommended Capacitance*) from the LDO_1V5 pin to the GND pin.

11.3 Recommended Supply Load Capacitance

Recommended Capacitance lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

12 Layout

12.1 TPS25750D - Layout

12.1.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

12.1.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25750 is placed on top and its components on bottom, the solution size will be at its smallest.

12.1.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS25750.

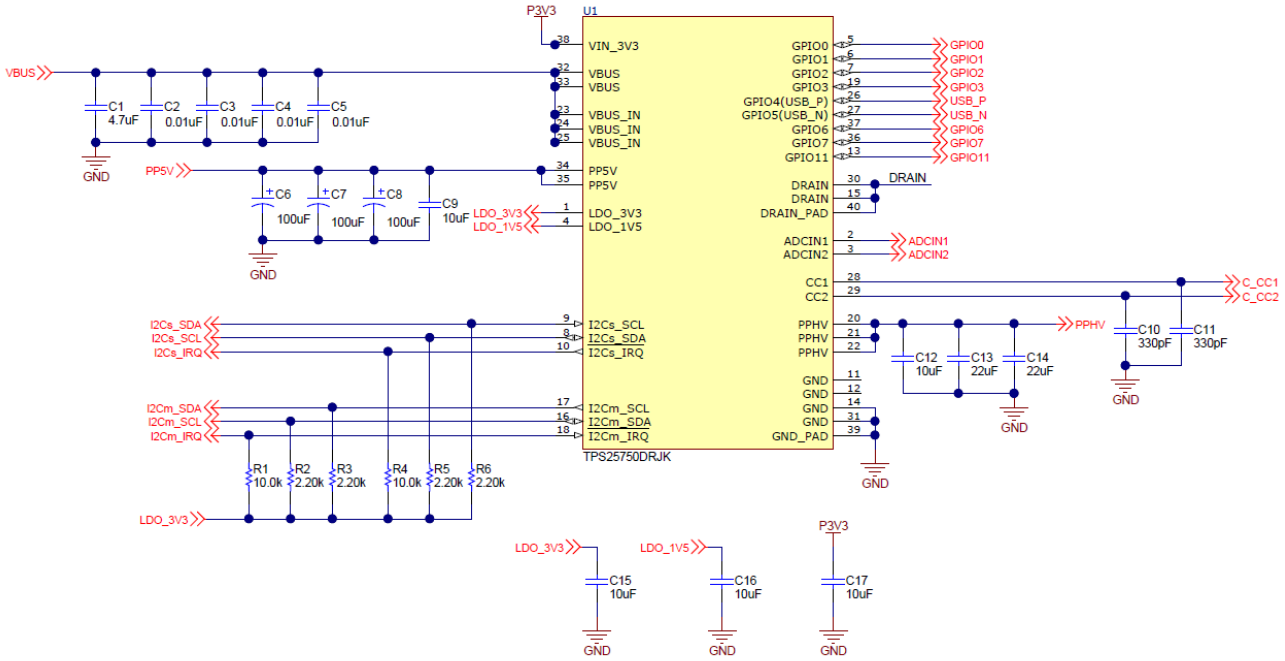

Figure 12-1. Example Schematic

12.1.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25750D is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS25750D. When placing the VBUS, PPHV, and PP5V capacitors, it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS25750D or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS25750D should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS25750D close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

Figure 12-2 through Figure 12-5 show the placement in 2-D and 3-D.

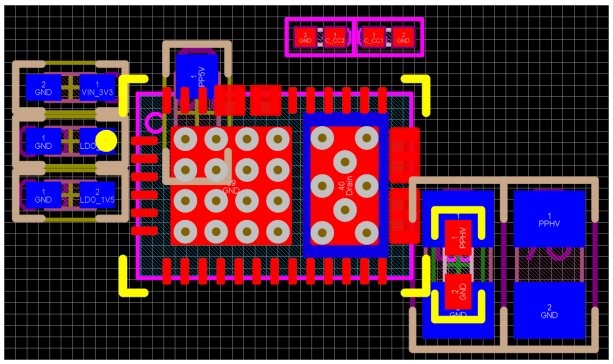

Figure 12-2. Top View Layout

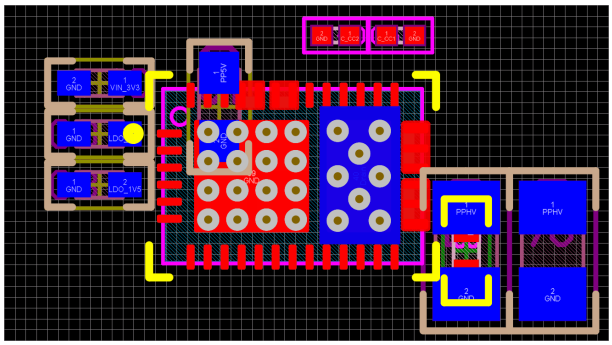

Figure 12-3. Bottom View Layout

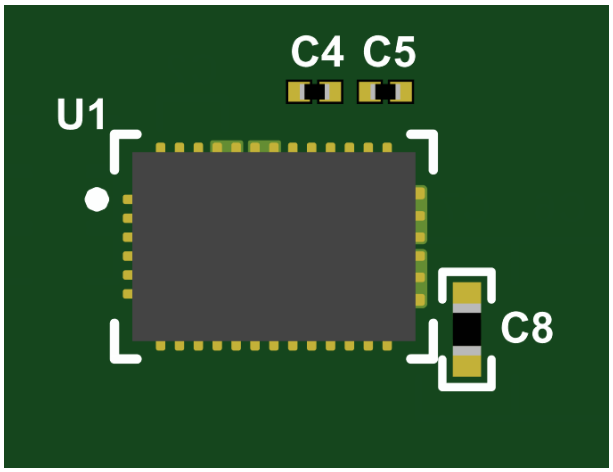

Figure 12-4. Top View 3-D

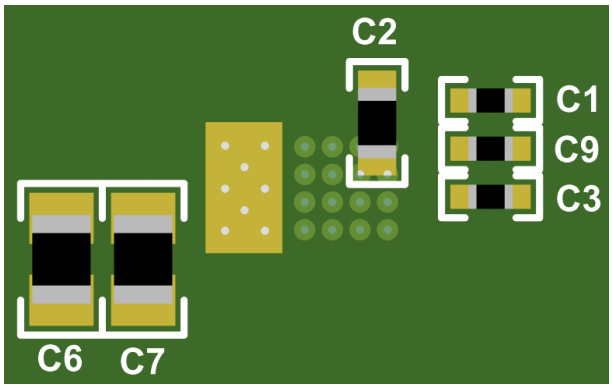

Figure 12-5. Bottom View 3-D

12.1.4 Routing PP_5V, VBUS, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for PP5V, VBUS, VBUS_IN, and PPHV. Connect PP5V and VBUS from the top layer to the bottom layer using at least 6 8-mil hole and 16-mil diameter vias. See Figure 12-6 for the recommended via sizing. For VBUS_IN and PPHV, connect from the top to bottom layer using 15 8-mil hole and 16-mil diameter vias. The via placement and copper pours are highlighted in Figure 12-7.

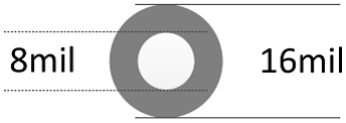

Figure 12-6. Recommended Minimum Via Sizing

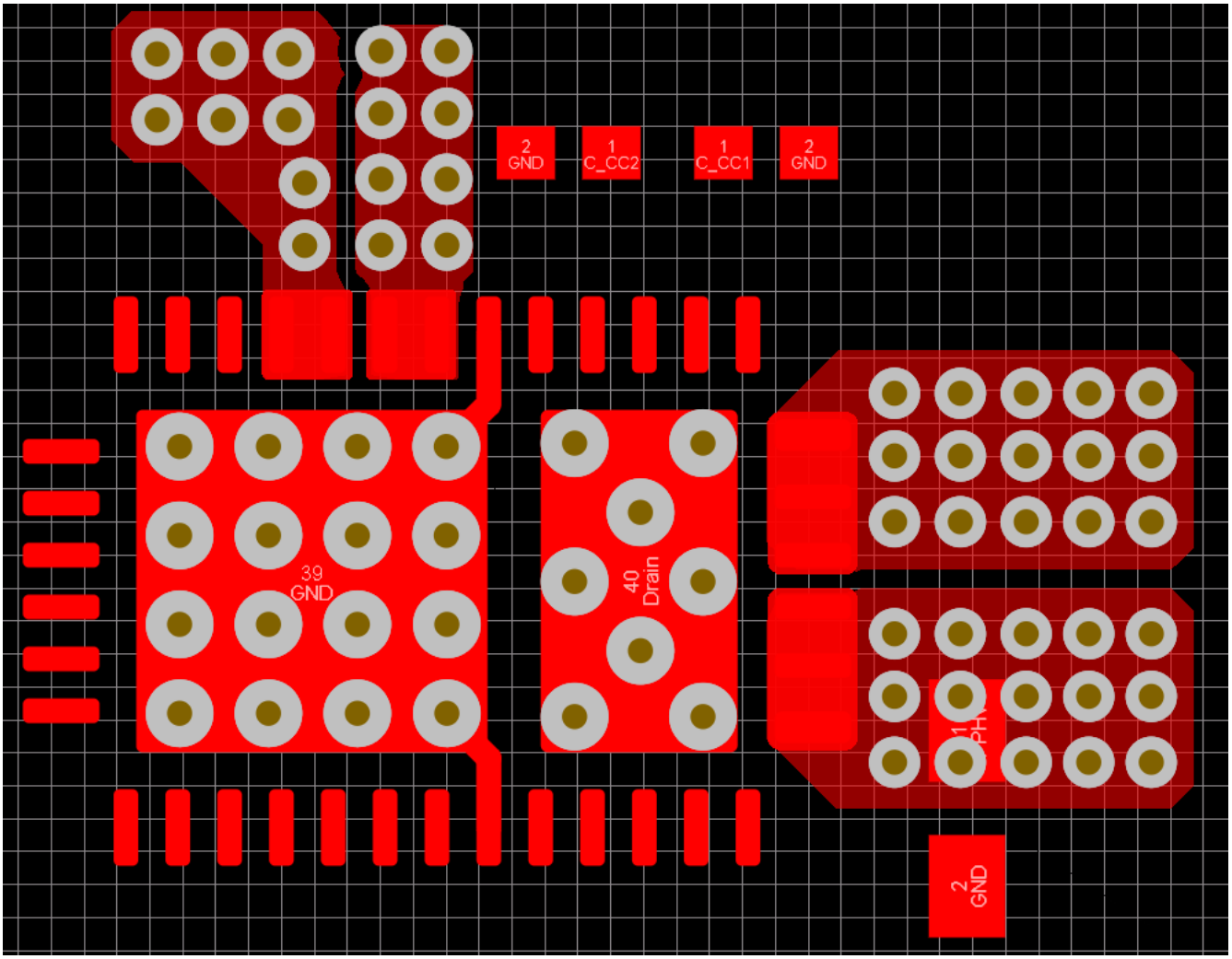

Figure 12-7. PP5V, VBUS, VBUS_IN, and PPHV Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 will be routed to their respective decoupling capacitors. Additionally, a copper pour on the bottom side is added to connect PP5V and PPHV to their decoupling capacitors located on the bottom of the PCB. This is highlighted in Figure 12-8.

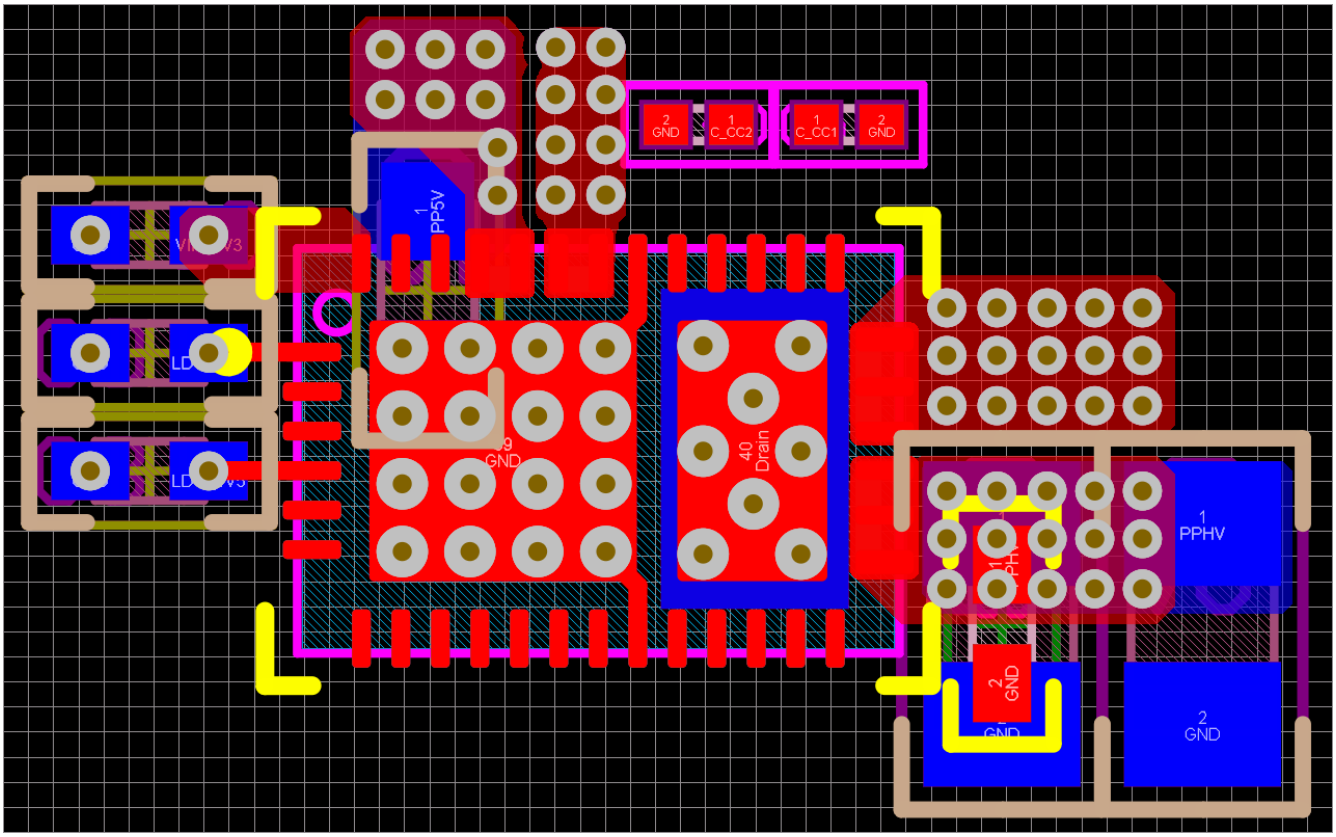

Figure 12-8. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

12.1.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil or 10-mil trace. The following images highlights how the CC lines and GPIOs are routed out.

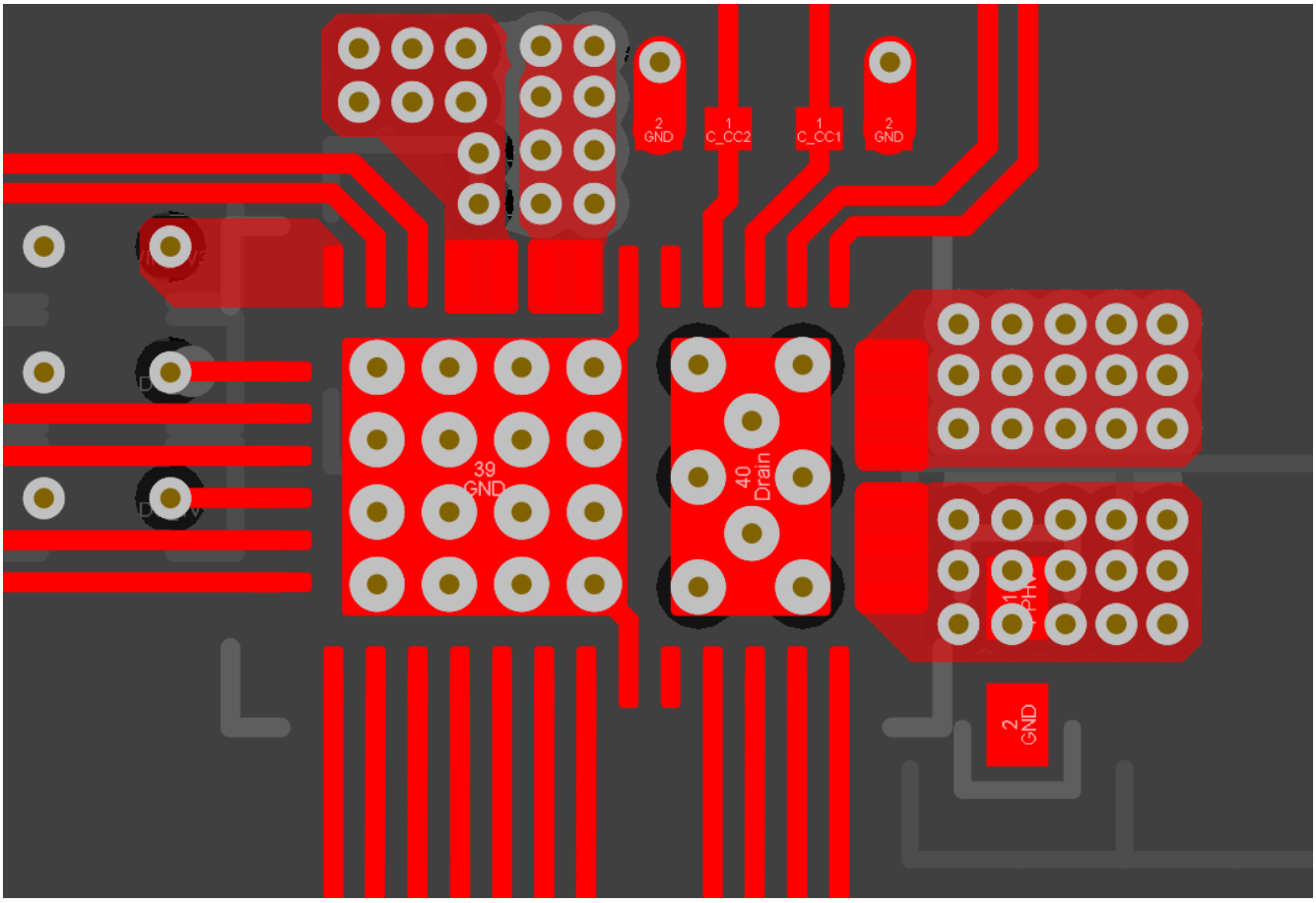

Figure 12-9. Top Layer GPIO Routing

Table 12-1. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
CC1, CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	8
Component GND	10
GPIO	8

12.2 TPS25750S - Layout

12.2.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

12.2.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25750 is placed on top and its components on bottom, the solution size will be at its smallest.

12.2.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS25750S.

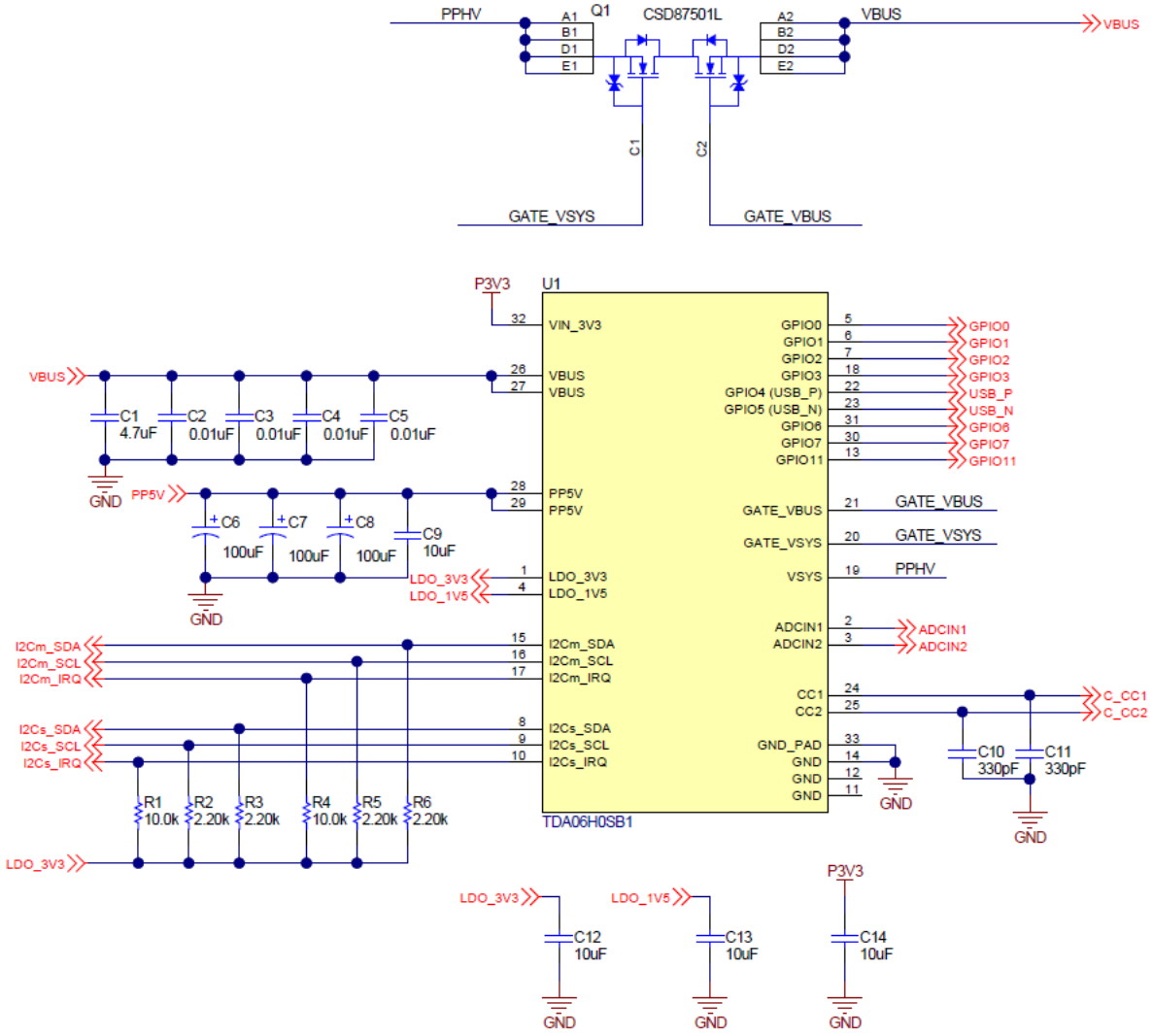

Figure 12-10. Example Schematic

12.2.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25750S is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the

components on the bottom side, it is recommended that they are placed directly under the TPS25750S. When placing the PP5V capacitors it is easiest to place them with the GND terminal of the capacitors to face inward the TPS25750S or to the side. All other components that are for pins on the GND pad side of the TPS25750S should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS25750S close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

Figure 12-11 through Figure 12-14 show the placement in 2-D and 3-D.

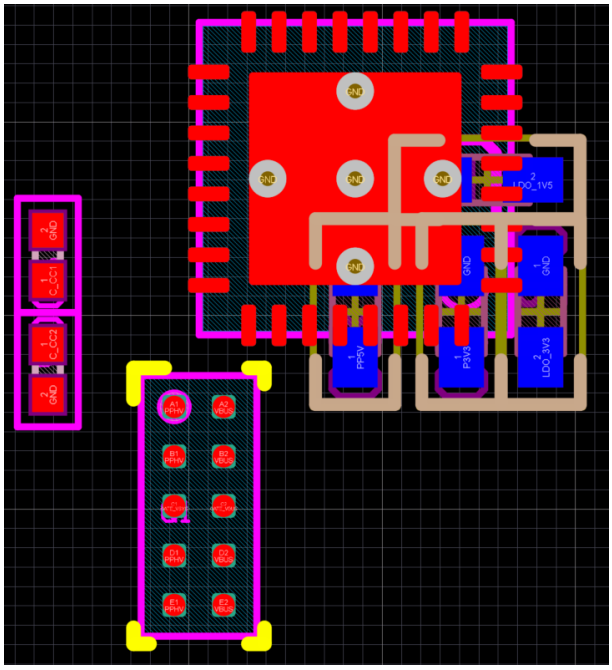

Figure 12-11. Top View Layout

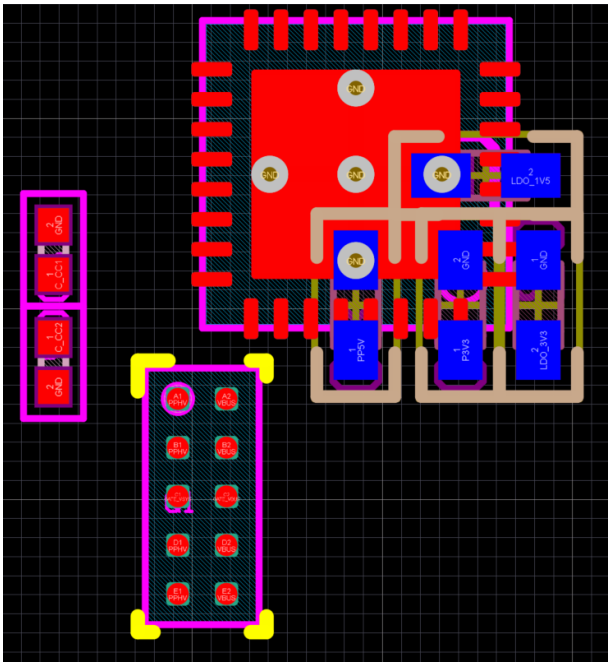

Figure 12-12. Bottom View Layout

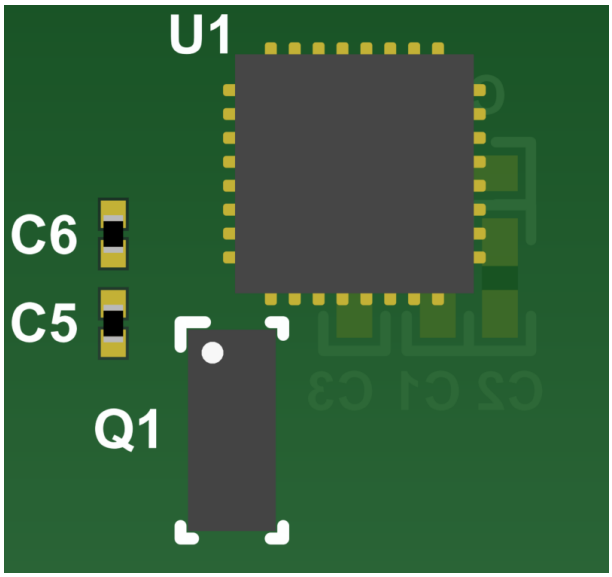

Figure 12-13. Top View 3-D

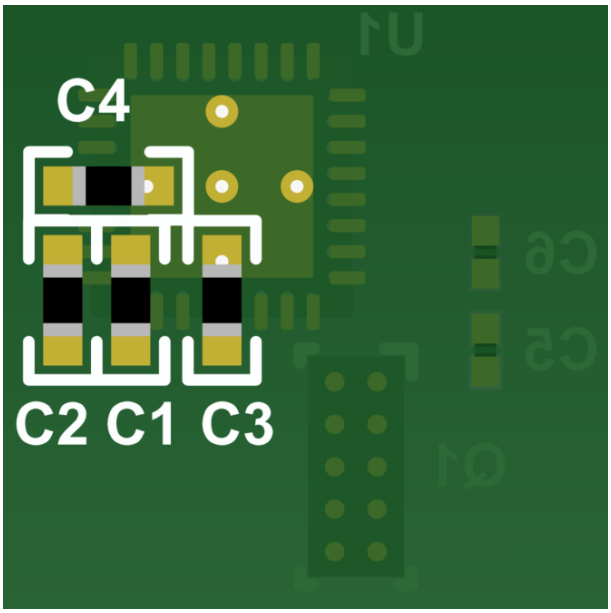

Figure 12-14. Bottom View 3-D

12.2.4 Routing PP5V, VBUS, PPHV, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for PP5V, VBUS, and PPHV. Connect PP5V from the top layer to the bottom layer using at least 8, 8-mil hole and 16-mil diameter vias. Connect PPHV from the top layer to the bottom layer using at least 12, 8-mil hole and 16-mil diameter vias. See Figure 12-15 for the recommended via sizing. The via placement and copper pours are highlighted in Figure 12-16.

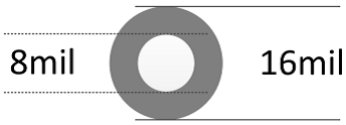

Figure 12-15. Recommended Minimum Via Sizing

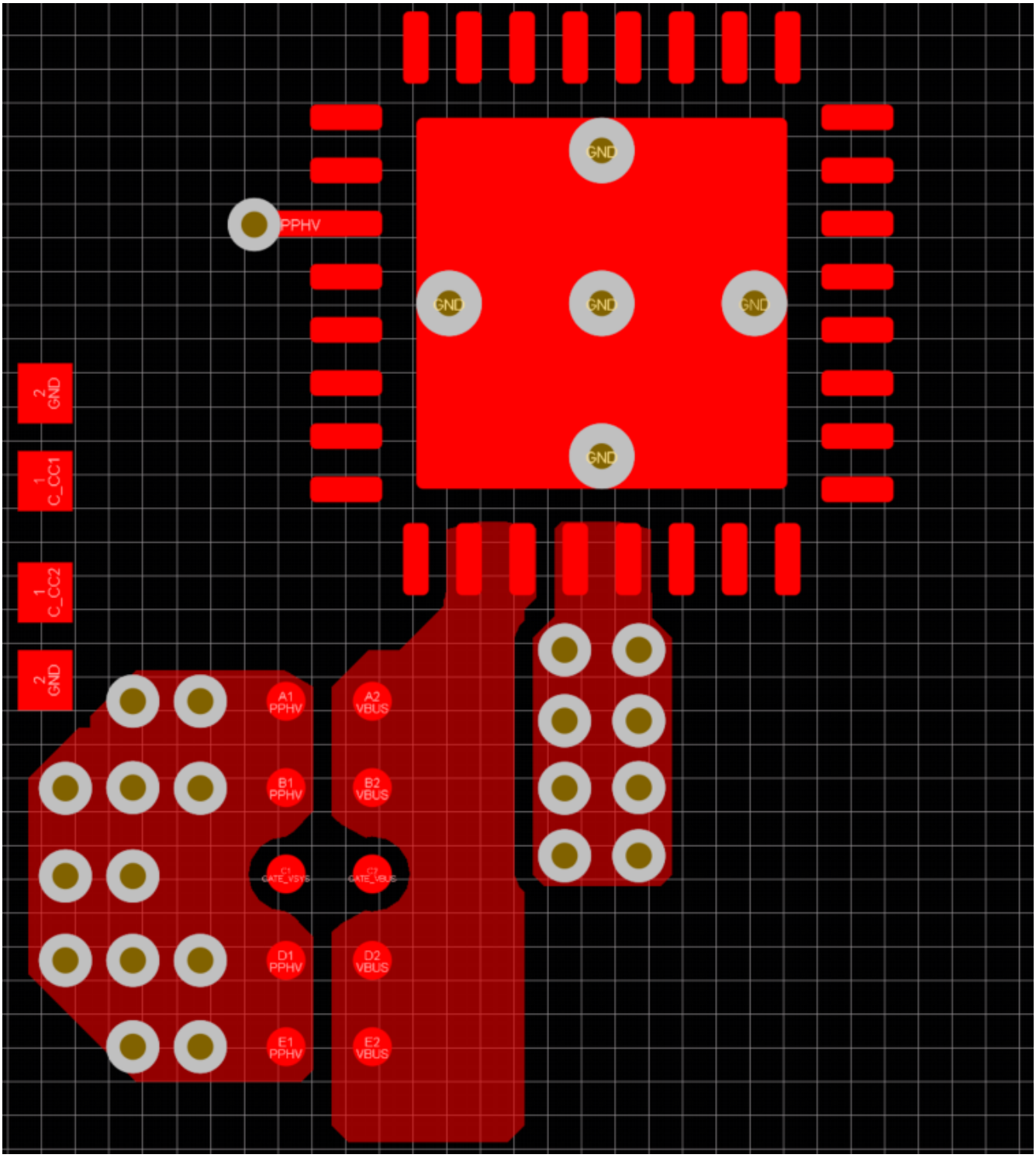

Figure 12-16. PP5V and VBUS1/2 Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 will be routed to their respective decoupling capacitors. Additionally, a copper pour on the bottom side is added to connect PP5V to the decoupling capacitors located on the bottom of the PCB. This is highlighted in Figure 12-17.

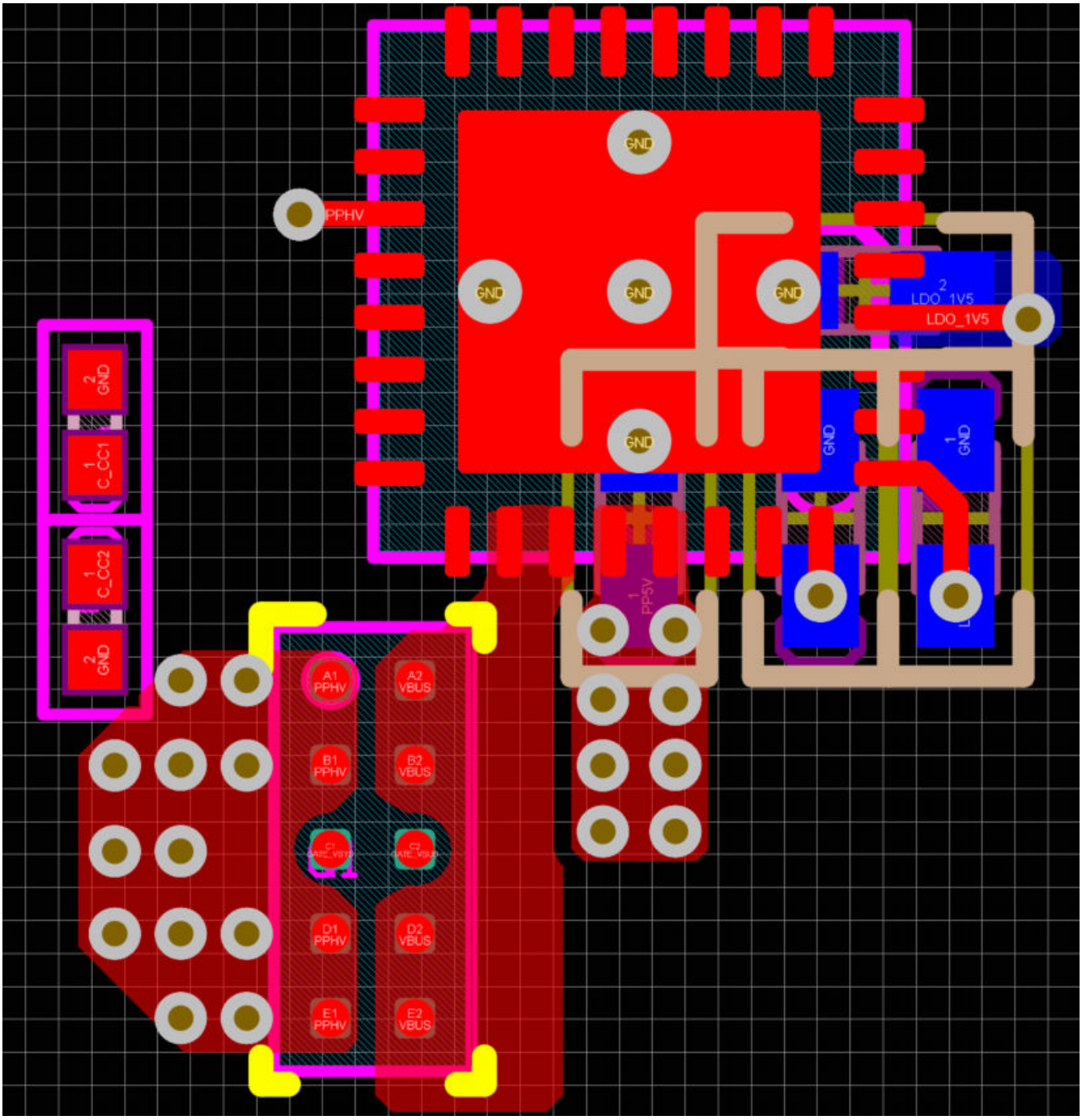

Figure 12-17. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

Figure 12-18 and Figure 12-19 show how to properly connect VSYS and the SYS_Gate control signals for the external N-FETs. The control signals can be routed on an internal layer using a 12-mil trace, and the trace going to VSYS should be as short as possible to minimize impedance, so placing a via directly on the high-voltage power path is ideal.

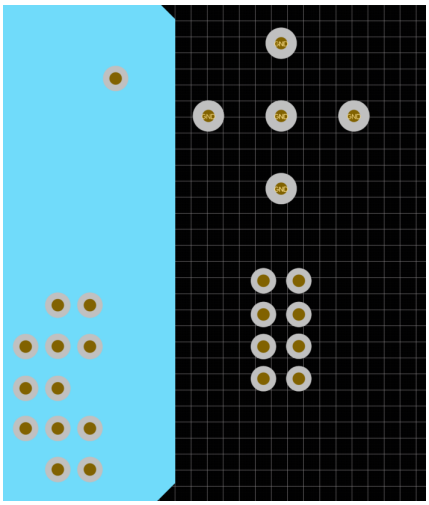

Figure 12-18. Top Polygon Pours

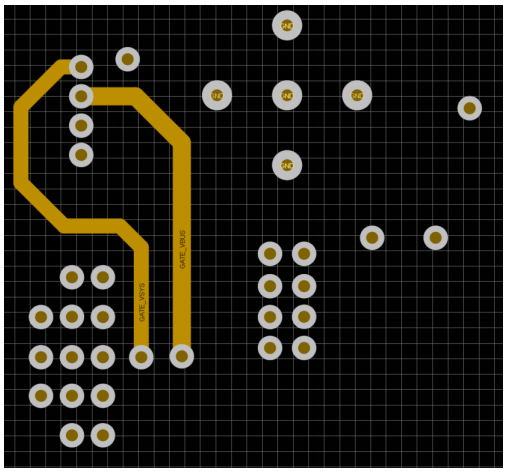

Figure 12-19. Bottom Polygon Pours

12.2.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil trace or a 10-mil trace.The following images highlight how the CC lines and GPIOs are routed out.

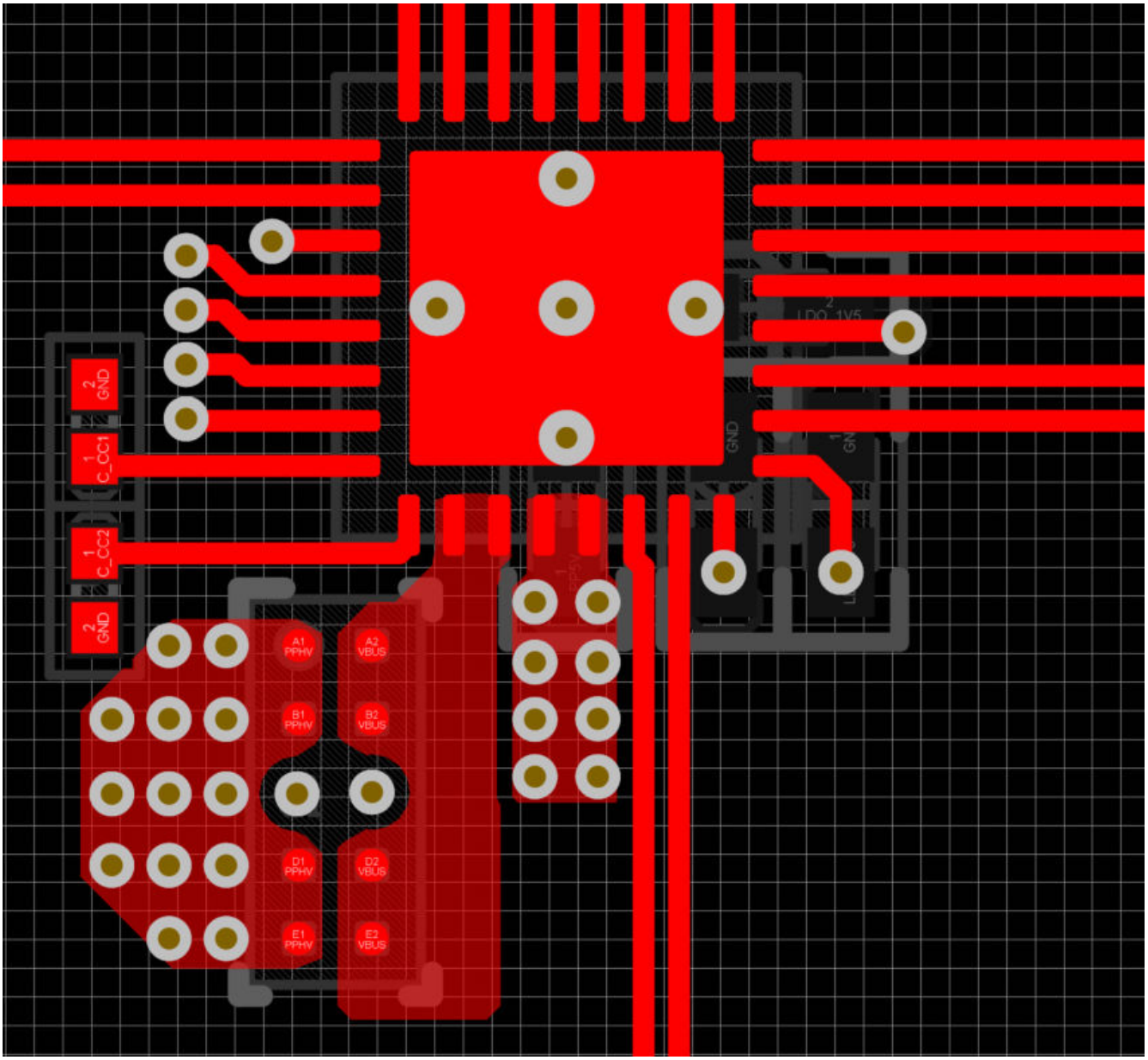

Figure 12-20. Top Layer GPIO Routing

Table 12-2. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
PA_CC1, PA_CC2, PB_CC1, PB_CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

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All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25750DRJKR	NRND	Production	WQFN (RJK) | 38	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	25750D
TPS25750SRSMR	NRND	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25750

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

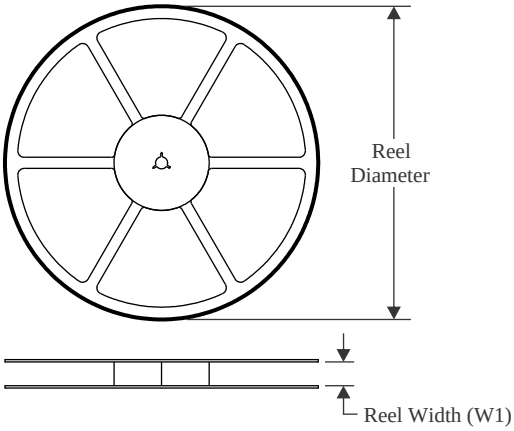
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

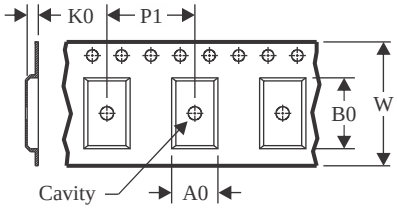
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

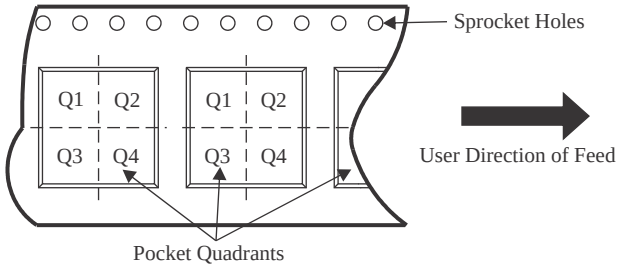


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

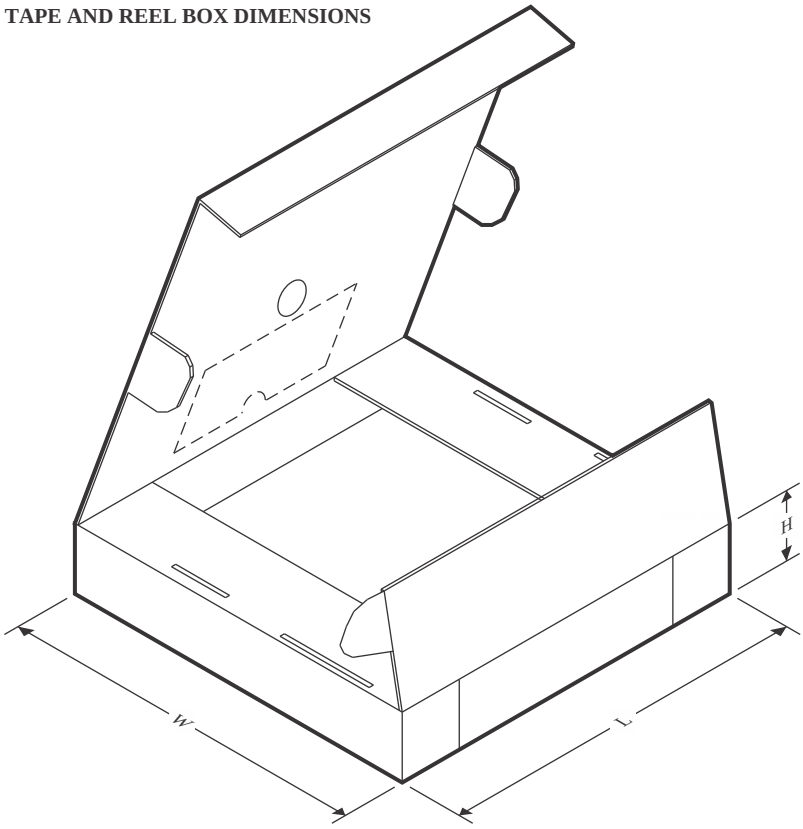
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25750DRJKR	WQFN	RJK	38	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TPS25750SRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25750DRJKR	WQFN	RJK	38	3000	338.0	355.0	50.0
TPS25750SRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

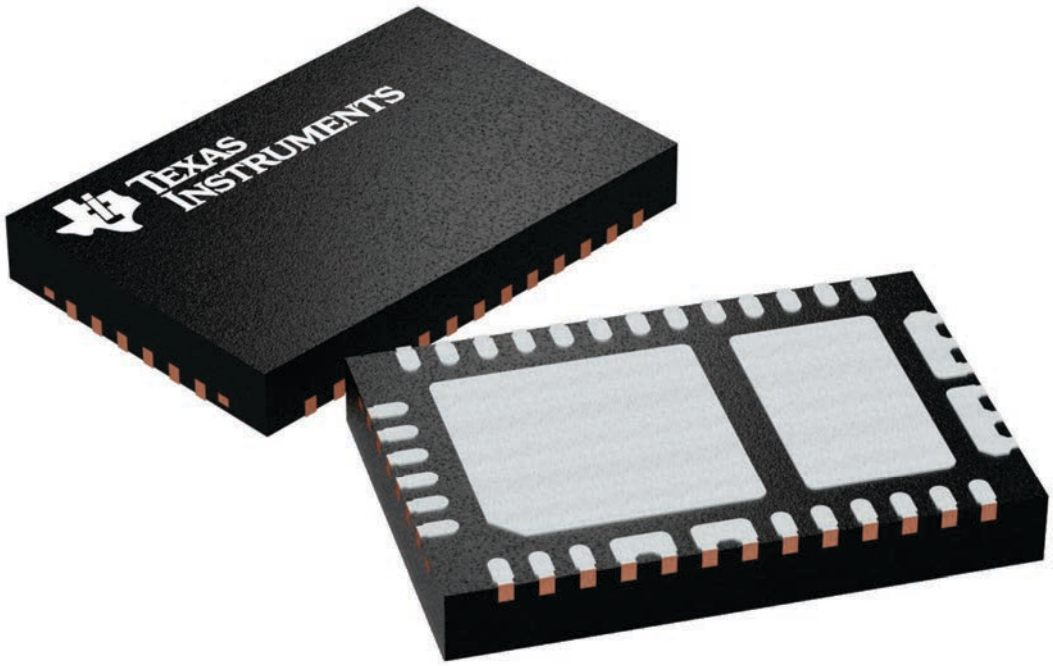
RJK 38

WQFN - 0.8 mm max height

6 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



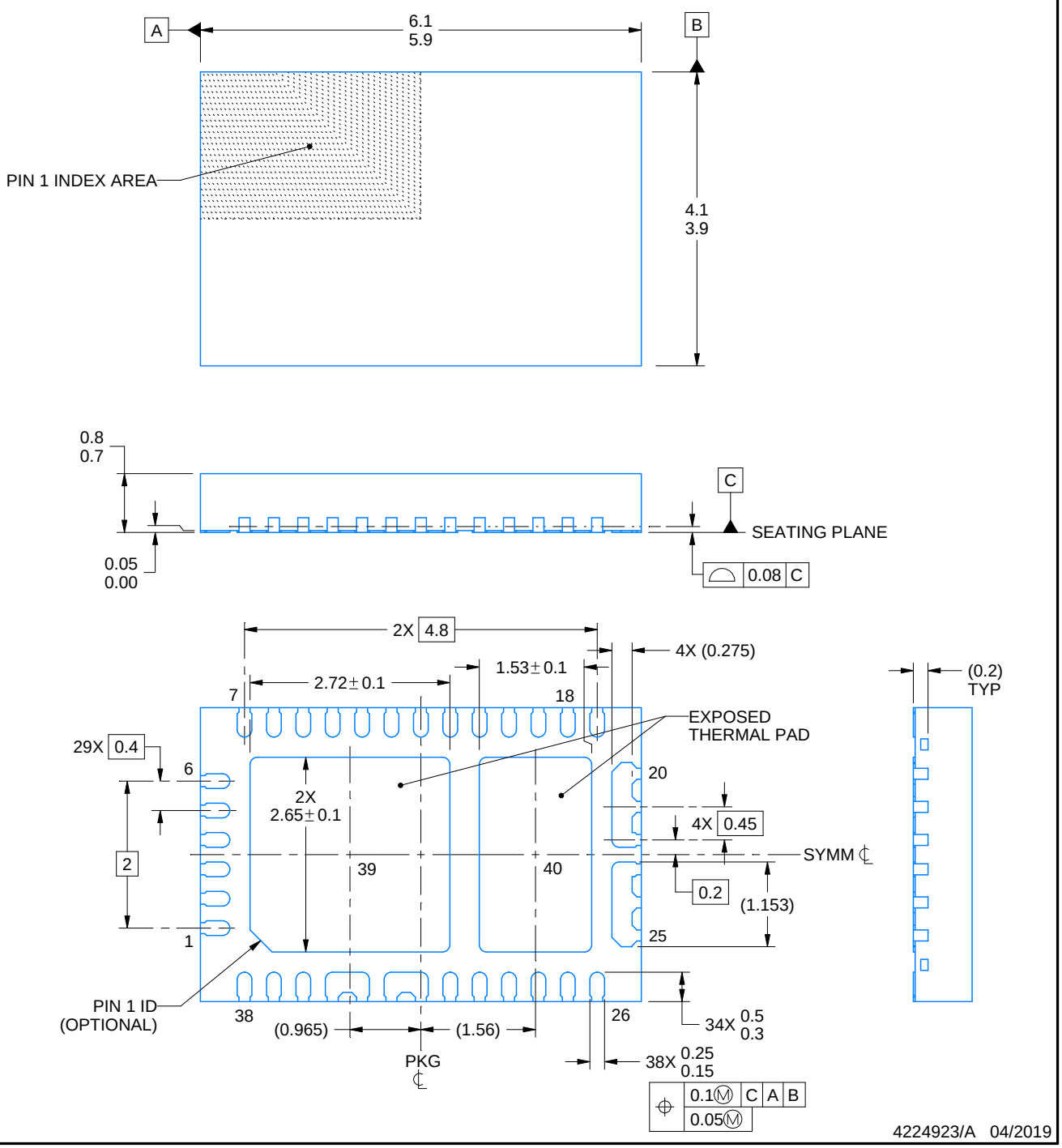
4224943/A

PACKAGE OUTLINE

RJK0038B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

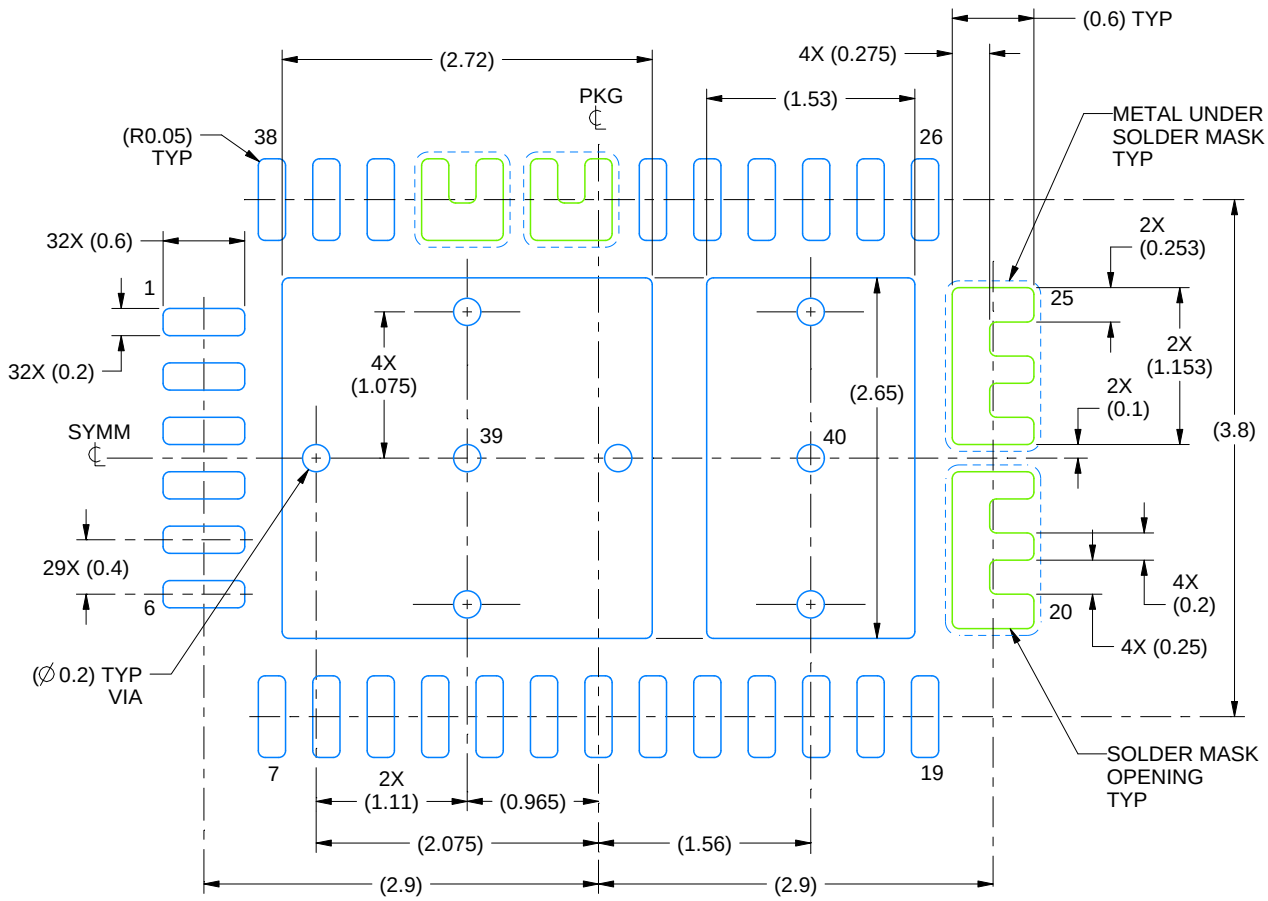
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

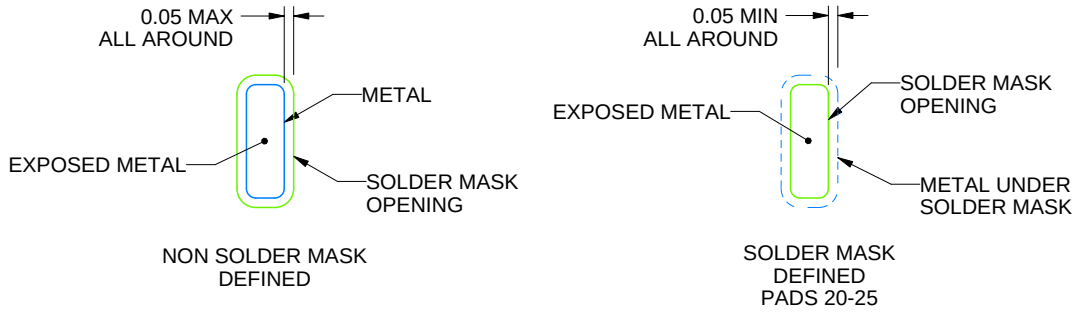
RJK0038B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

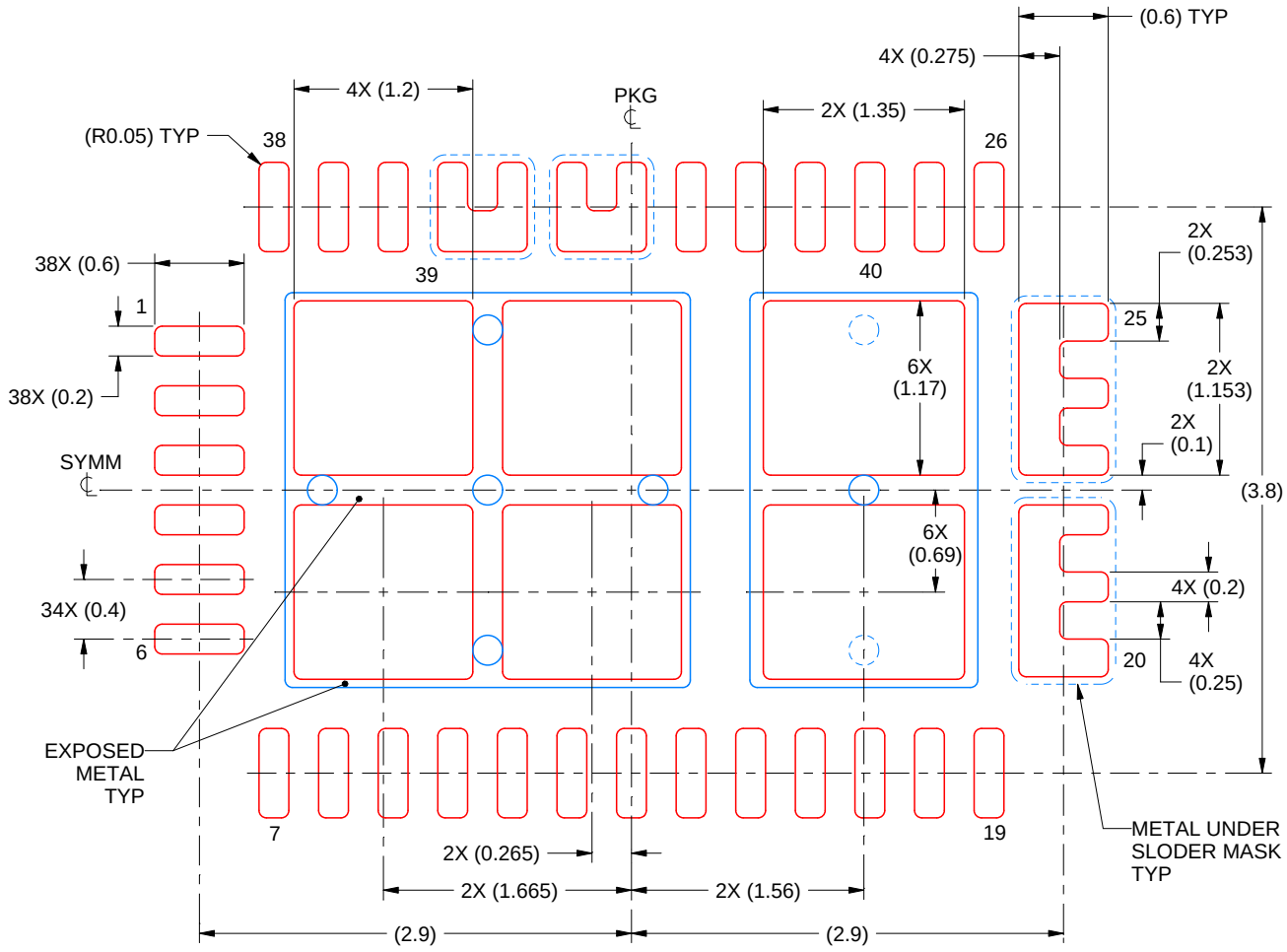


SOLDER MASK DETAILS
NOT TO SCALE

4224923/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 39 & 40
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224923/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

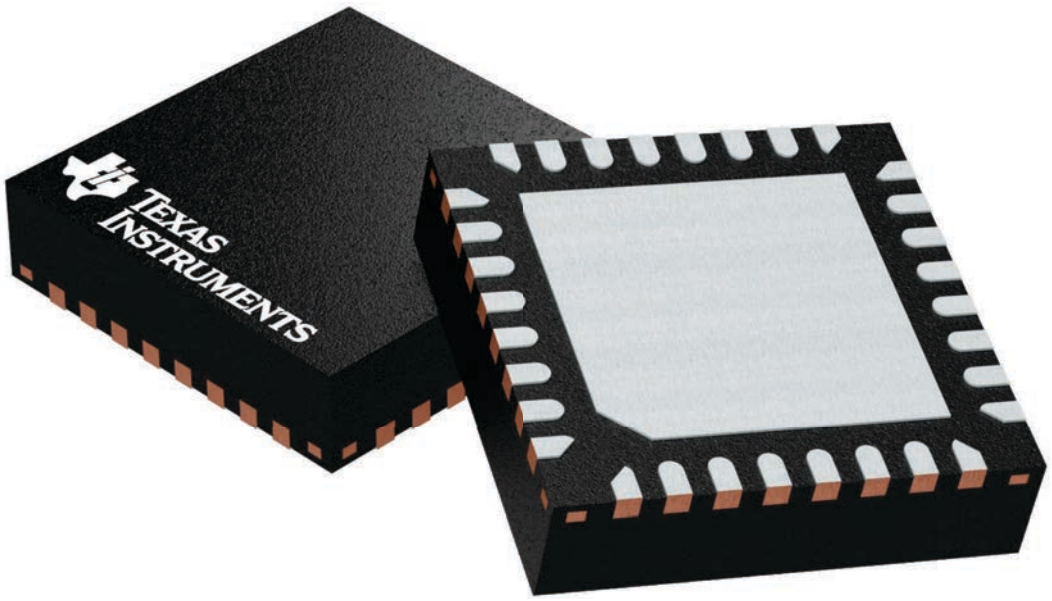
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



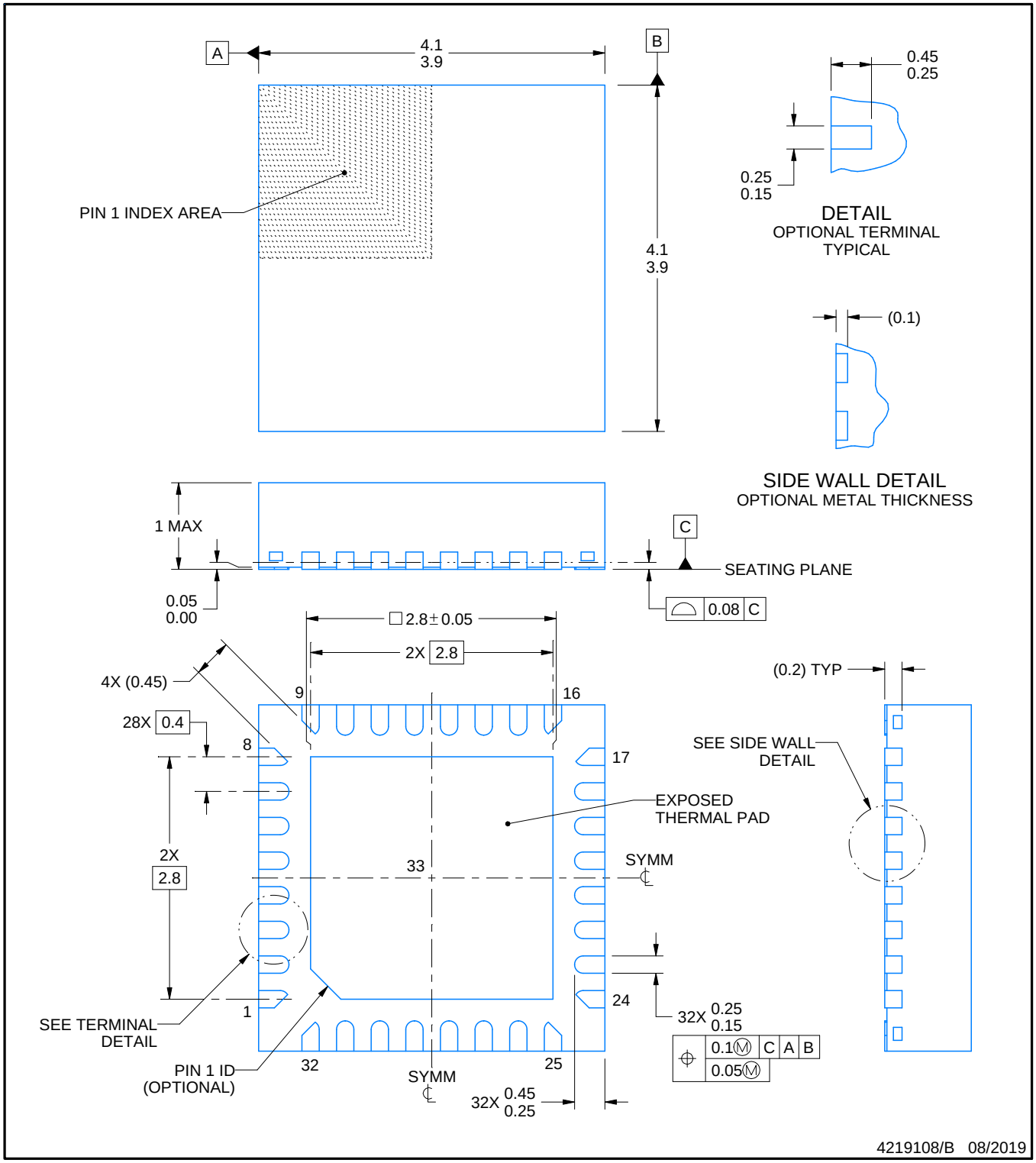
4224982/A

PACKAGE OUTLINE

RSM0032B

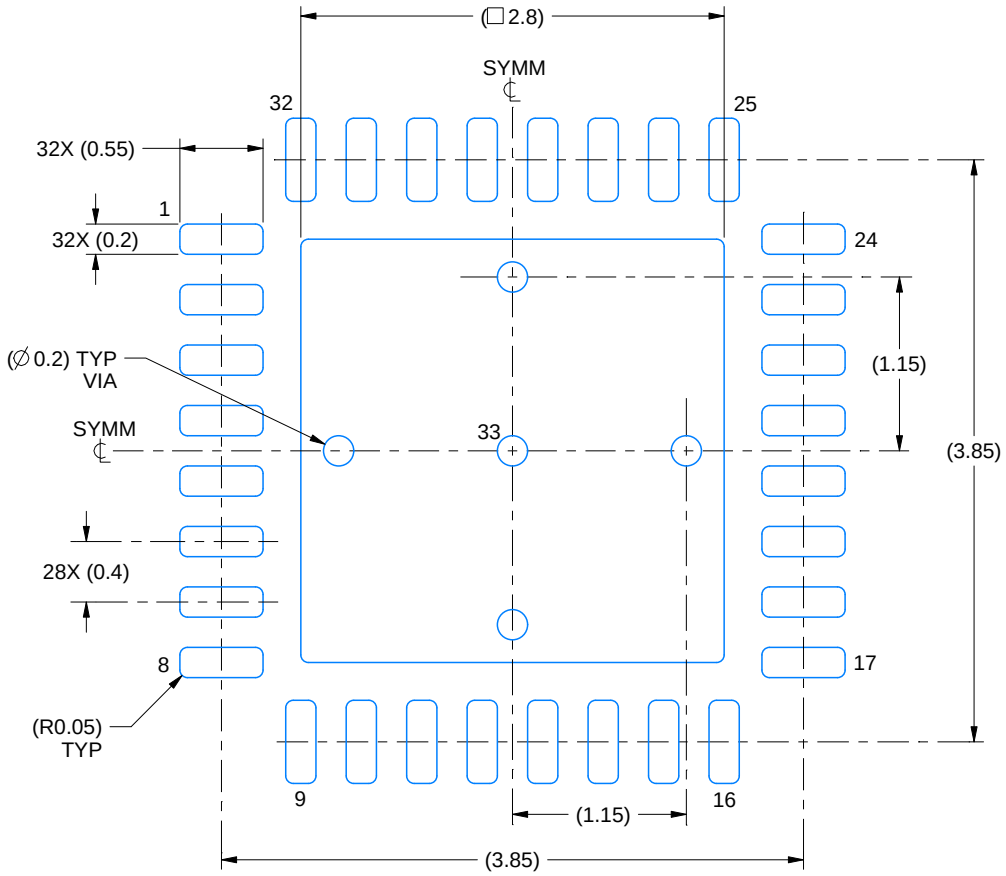
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

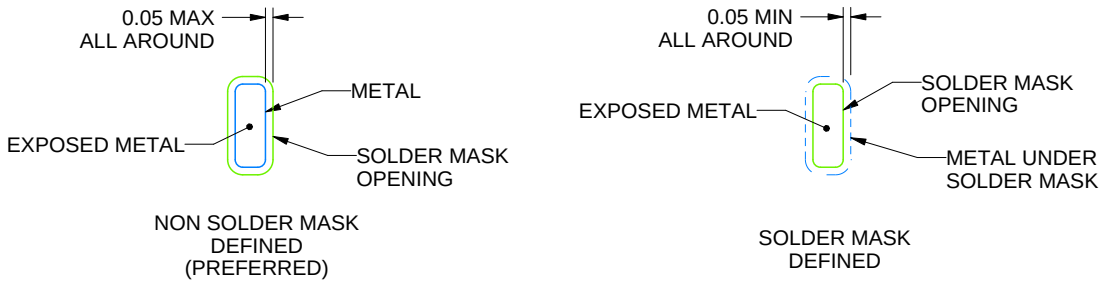


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

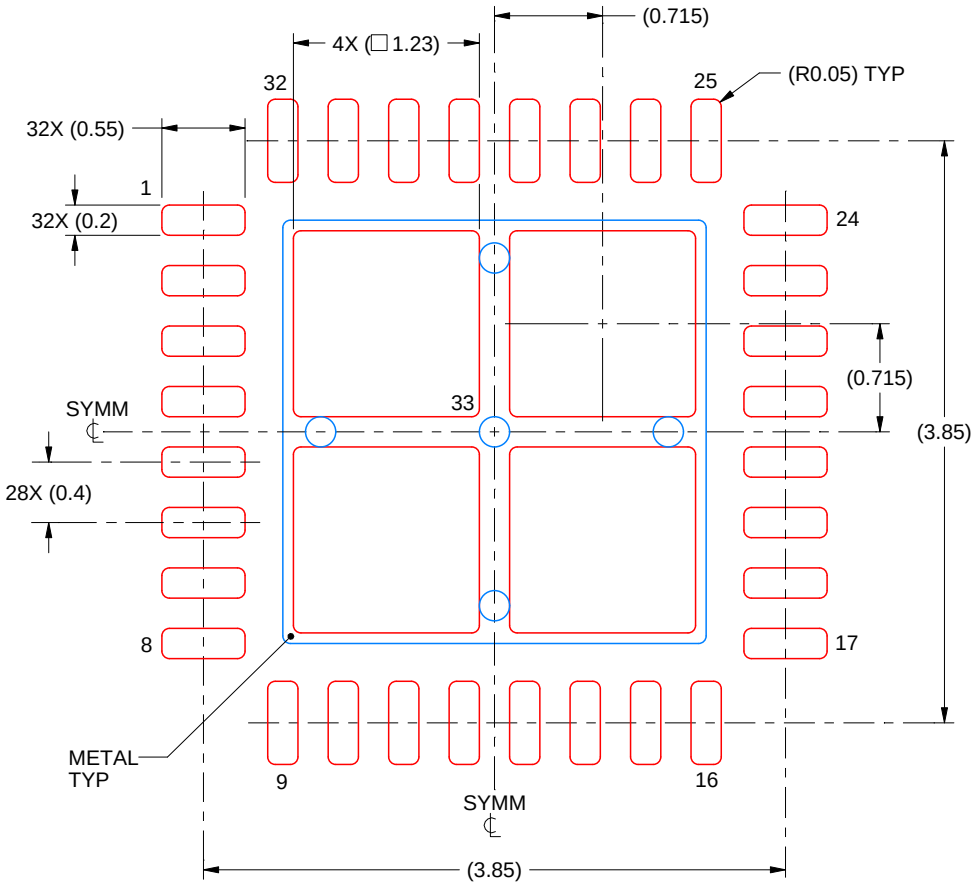


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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