TPS27S100x 40V、4A、80mΩ のシングル・チャネル・ハイサイド・スイッチ

1 特長

- 完全な診断機能を持つ 80mΩ のシングル・チャネル・ハイサイド・スイッチ
  - TPS27S100A：オープン・ドレインのステータス出力
  - TPS27S100B：電流モニタのアナログ出力
- 広い動作電圧範囲：3.5V～40V
- 非常に低いスタンバイ電流：0.5µA 未満
- 動作時接合部温度範囲：–40～150°C
- 入力制御、3.3V および 5V ロジック互換
- 高精度の電流モニタ：1A で ±30mA
- 電流制限を外付け抵抗で変更可能 (0.5A～6A)、0.5A で ±20%
- 診断イネーブル機能によって MCU、アナログ、デジタル・インターフェイスの多重化が可能
- IN および OUT ピンの非常に優れた ESD 保護
  - ±16kV IEC 61000-4-2 ESD 接触放電
  - ±4kV IEC 61000-4-4 電気的高速過渡
  - ±1.0kV/42ΩのIEC 61000-4-5サージ
- 保護
  - 過負荷および GND への短絡保護
  - 誘導性負荷の負電圧クランプ
  - 低電圧誤動作防止 (UVLO) 保護
  - 自己回復可能なサーマル・シャットダウンおよびスイング
  - GND 喪失保護
- 診断機能
  - オンおよびオフ状態での出力開放負荷および電源への短絡の検出
  - 過負荷およびグランドへの短絡の検出
  - サーマル・シャットダウンおよびスイング検出
- 熱的に強化された 14 ピン PWP または 16 ピン QFN パッケージ

2 アプリケーション

- プログラマブル・ロジック・コントローラ
- ビルディング・オートメーション
- テレコムおよびネットワーク

3 概要

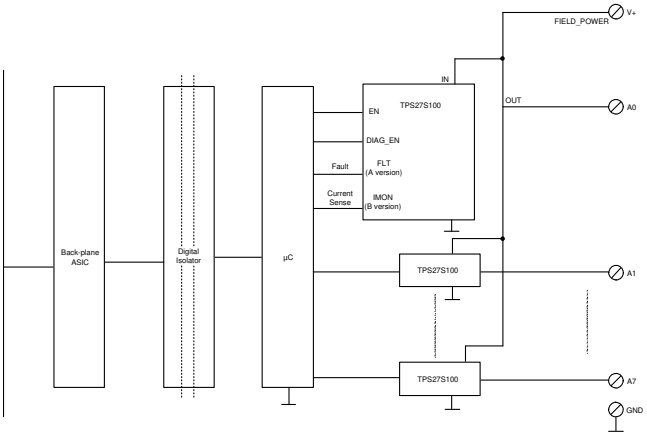
TPS27S100xはシングル・チャネルの完全に保護されたハイサイド・スイッチで、NMOSおよびチャージ・ポンプが内蔵されています。包括的な診断機能と高精度の電流監視機能によって、インテリジェントな負荷制御が可能です。可変の電流制限機能により、システム全体の信頼性が大幅に向上します。デバイス診断レポートには2つのバージョンがあり、デジタル・フォルト状態と、アナログ電流監視出力の両方をサポートします。高精度の電流監視と可変の電流制限機能は、市場での差別化に役立ちます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
TPS27S100x	HTSSOP (14)	4.40mm×5.00mm
	QFN (16)	4.00mm×3.5mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



目次

4 改訂履歴

Revision A (February 2018) から **Revision B** に変更 **Page**

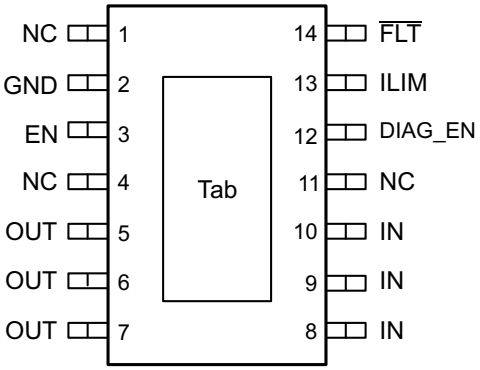
- 「*特長*」セクションに QFN パッケージを追加 ... 1
- 「*製品情報*」表にパッケージ QFN (16) と本体サイズ 4.00mm × 3.5mm を追加 ... 1
- 「*代表的なアプリケーションの回路図*」を更新 ... 1
- Added RRK Package to the *Pin Out Drawing* and *Pin Functions* table ... 3
- Updated the *Specifications Absolute Maximum Ratings* table ... 4
- Changed the Operation junction temperature range MAX from 150°C to 125°C in the *Specifications Recommended Operating Conditions* table ... 4
- Added RRK package to the *Specifications Thermal Information* table ... 4
- Updated the Operating Current section in the *Specifications Electrical Characteristics* table ... 4

2017年**10**月発行のものから更新 **Page**

- Added footnote 2 and 3 to the *Electrical Characteristics* table ... 4
- Added reverse current protection information to the *Reverse Current Protection* section ... 22

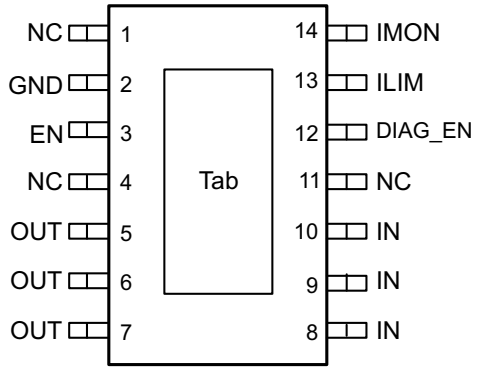
5 Pin Configuration and Functions

TPS27S100A PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



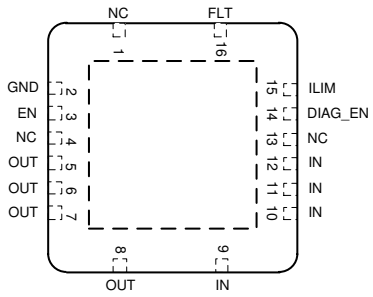
NC – No internal connection

TPS27S100B PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



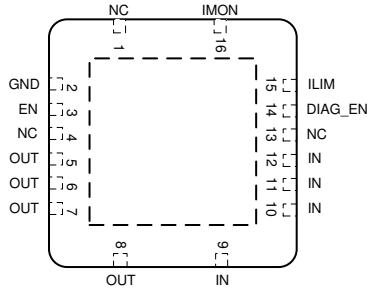
NC – No internal connection

TPS27S100A RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



NC – No internal connection

TPS27S100B RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS27S100A PWP	TPS27S100B PWP	TPS27S100A RRK	TPS27S100B RRK		
DIAG_EN	12	12	14	14	I	Enable and disable pin for diagnostic functions. Connect to device GND if not used.
EN	3	3	3	3	I	Enable control for channel activation.
$\overline{FLT}$	14	—	16	—	O	Open-drain diagnostic status output. Leave floating if not used.
GND	2	2	2	2	—	Ground pin.
ILIM	13	13	15	15	O	adjustable current-limit pin. Connect to device GND if external current limit is not used.
IMON	—	14	—	16	O	Current-monitor output. Leave floating if not used.
IN	8, 9, 10	8, 9, 10	9, 10, 11, 12	9, 10, 11, 12	I	Power supply.
NC	1, 4, 11	1, 4, 11	1, 4, 13	1, 4, 13	—	No-connect pin; leave floating.
OUT	5, 6, 7	5, 6, 7	5, 6, 7, 8	5, 6, 7, 8	O	Output, connected to load.
Thermal pad	—	—	—	—	—	Thermal pad. Connect to device GND or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply voltage		40	V
Supply voltage (for transients less than 400 ms)		48	V
Current on GND pin, t < 2 minutes	–250	100	mA
Voltage on EN and DIAG_EN pins	–0.3	7	V
Current on EN and DIAG_EN pins	–10		mA
Voltage on $\overline{FLT}$ pin	–0.3	7	V
Current on $\overline{FLT}$ pin	–30	10	mA
Voltage on ILIM pin	–0.3	7	V
Voltage on IMON pin	–2.7	6.5	V
Inductive load switch-off energy dissipation, single pulse(3)		70	mJ
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Test condition: V_{IN} = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-µm Cu, 2- × 35-µm Cu. 600-mm^2 board copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) (1)	IN, OUT, GND	±5000	V
		Human body model (HBM) (1)	Other pins	±4000	
		Charged device model (CDM)		±750	
$V_{(ESD)}$	Electrostatic discharge	Contact/Air discharge, per IEC 61000-4-2 (2)	IN, OUT	±16000	V
$V_{(ESD)}$		Electrical fast transient, per IEC 61000-4-4 (2)	IN, OUT	±4000	V
$V_{(ESD)}$		Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 µs (2)	IN, OUT	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Tested with application circuit shown in 図 35 with C_{VIN1}= 47 µF, C_{VIN2}= 100 nF, C_{VOUT}= 22 nF and SM15T30A TVS input clamp. Supply voltage of 24 V DC is always ON, EN Inputs are High, so output is High (ON) and floating (no load).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Operating voltage	5	40	V
V_{ENx}	Voltage on EN and DIAG_EN pins	0	5	V
V_{FLT}	Voltage on $\overline{FLT}$ pin	0	5	V
$I_{L,nom}$	Nominal dc load current	0	4	A
T_J	Operating junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	41	42.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	29.7	31.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	25.1	16.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.8	16.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	4.6	°C/W

6.5 Electrical Characteristics

5 V < V_{IN} < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{IN(nom)}$	Nominal operating voltage		4		40	V
$V_{IN(uvr)}$	Undervoltage restart	V_{IN} rises up	3.5	3.7	4	V
$V_{IN(uvf)}$	Undervoltage shutdown	V_{IN} falls down	3	3.2	3.5	V
$V_{(uv,hys)}$				0.5		V
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 5 V < V_{IN} < 30 V, no load; –40°C T_J < 125°C		2.5	3.2	mA
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 5 V < V_{IN} < 40 V, no load; –40°C T_J < 150°C		2.5	5	mA
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 24-Ω load			10	mA
$I_{(off)}$	Standby mode current	V_{IN} = 24 V, V_{EN} = V_{DIAG_EN} = V_{IMON} = V_{ILIM} = V_{OUT} = 0 V, T_J = 25°C			2	µA
$I_{(off,diag)}$	Standby current with diagnostic enabled	V_{IN} = 24 V, V_{EN} = 0 V, V_{DIAG_EN} = 5 V			1.2	mA
$t_{(off,deg)}$	Standby mode deglitch time(1)	EN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.		2		ms
$I_{lkg(out)}$	Off-state output leakage current	V_{IN} = 24 V, V_{EN} = V_{OUT} = 0, T_J = 25°C			0.5	µA
POWER STAGE						
$r_{DS(on)}$	On-state resistance	V_{IN} > 5 V, T_J = 25°C		80	100	mΩ
		V_{IN} > 5 V, T_J = 150°C			166	mΩ
		V_{IN} = 3.5 V, T_J = 25°C			120	mΩ
$I_{ILIM(int)}$	Internal current limit	Internal current limit value, ILIM pin connected to GND	7		13	A
$I_{ILIM(TSD)}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		5		A
		External current limit value under thermal shutdown as a percentage of the external current limit setting value		50		%
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage		50		70	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain-to-source diode voltage	V_{EN} = 0, I_{OUT} = −0.2 A		0.7		V
$I_{(R1)}$	Continuous reverse current from source to drain	t < 60 s, V_{EN} = 0, T_J = 25°C. Short-to-supply condition.		2		A
$I_{(R2)}$	Continuous reverse current from source to drain	t < 60 s, V_{EN} = 0, T_J = 25°C. With GND network, 1-kΩ resistor in parallel with A diode. Reverse-polarity condition.		3		A
LOGIC INPUT (EN AND DIAG_EN)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(EN,pd)}$	EN pulldown resistor			500		kΩ
$R_{(DIAG,pd)}$	DIAG_EN pulldown resistor			150		kΩ

(1) Value is specified by design, not subject to production test.

Electrical Characteristics (continued)

5 V < V_{IN} < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
$V_{(ol,off)}$	Open-load detection threshold in off-state	V_{EN} = 0 V, When V_{IN} – V_{OUT} < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$. Open load detected.	1.4	1.8	2.6	V
$I_{(ol,off)}$	Off-state output sink current with open load	V_{EN} = 0 V, V_{IN} = V_{OUT} = 24 V, T_J = 125°C.	–150			µA
$t_{d(ol,off)}$	Open-load detection-threshold deglitch time in off state	V_{EN} = 0 V, When V_{IN} – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.		600		µs
$I_{(ol,on)}$	Open-load detection threshold in on state	V_{EN} = 5 V, when I_{OUT} < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$. Open load detected. Version A only	2	6	10	mA
$t_{d(ol,on)}$	Open-load detection-threshold deglitch time in on-state	V_{EN} = 5 V, when I_{OUT} < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$. Open load detected.		700		µs
$V_{(FLT)}$	Fault low output voltage	I_{FLT} = 2 mA			0.4	V
$T_{(SD)}$	Thermal shutdown threshold			175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset			155		°C
$T_{(SW)}$	Thermal swing shutdown threshold			60		°C
$T_{(hys)}$	Hysteresis for resetting the thermal shutdown and swing			10		°C
CURRENT MONITOR AND CURRENT LIMIT						
$K_{(IMON)}$	Current sense current ratio			500		
$K_{(ILIM)}$	Current limit current ratio			2000		
$dK_{(IMON)}/K_{(IMON)}$	Current-monitor accuracy	I_{load} ≥ 5 mA	–80		80	%
		I_{load} ≥ 25 mA	–12		12	
		I_{load} ≥ 50 mA	–8		8	
		I_{load} ≥ 0.1 A	–5		5	
		I_{load} ≥ 1 A	–3		3	
$dK_{(ILIM)}/K_{(ILIM)}$	External current-limit accuracy(2), (3)	I_{limit} ≥ 0.5 A, 25°C < T_J < 150°C	–20		20	%
		I_{limit} ≥ 0.5 A, -40°C < T_J < 25°C	–28		28	%
$dK_{(ILIM)}/K_{(ILIM)}$	External current-limit accuracy(2), (3)	I_{limit} ≥ 1.6 A, 25°C < T_J < 150°C	–15		15	%
		I_{limit} ≥ 1.6 A, -40°C < T_J < 25°C	–18		18	
$V_{IMON(lin)}$	Current-monitor voltage linear voltage range(1)	V_{IN} ≥ 5 V	0		4	V
$I_{OUT(lin)}$	Current-monitor voltage linear current range(1)	V_{IN} ≥ 5 V, $V_{IMON(lin)}$ ≤ 4 V	0		4	A
$V_{IMON(H)}$	IMON pin voltage in Fault mode	V_{IN} ≥ 7 V, fault mode	4.3	4.75	4.9	V
		V_{IN} ≥ 5 V, fault mode	Min(V_{IN} – 0.8, 4.3)		4.9	
$I_{IMON(H)}$	IMON pin current in Fault mode	V_{IMON} = 4.3 V, V_{IN} > 7 V, fault mode	10			mA
$V_{IMON(th)}$	Current limit internal threshold voltage(1)			1.233		V

(2) External current limit set is recommended to be higher than 500 mA.
(3) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting.

6.6 Timing Requirements – Current Monitor Characteristics(1)

			MIN	NOM	MAX	UNIT
$t_{IMON(off1)}$	IMON settling time from DIAG_EN disabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 5 to 0 V. IMON to 10% of sense value.			10	µs
$t_{IMON(on1)}$	IMON settling time from DIAG_EN enabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 0 to 5 V. IMON to 90% of sense value.			10	µs
$t_{IMON(off2)}$	IMON settling time from EN falling edge	V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. EN from 5 to 0 V. IMON to 10% of sense value.			10	µs
		V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. EN from 5 to 0 V. Current limit triggered.			180	µs
$t_{IMON(on2)}$	IMON settling time from EN rising edge	V_{IN} = 24 V, V_{DIAG_EN} = 5 V, I_{load} ≥ 100 mA. V_{EN} from 0 to 5 V. IMON to 90% of sense value.			150	µs

(1) Value specified by design, not subject to production test.

6.7 Switching Characteristics

V_{IN} = 24 V, R_{load} = 24 Ω, over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	EN rising edge to V_{OUT} = 10%, DIAG_EN high	20		50	µs
$t_{d(off)}$	Turn-off delay time	EN falling edge to V_{OUT} = 90%, DIAG_EN high	40		80	µs
$dV/dt_{(on)}$	Slew rate on	V_{OUT} = 10% to 90%, DIAG_EN high	0.1		0.5	V/µs
$dV/dt_{(off)}$	Slew rate off	V_{OUT} = 90% to 10%, DIAG_EN high	0.1		0.5	V/µs

(1) Value specified by design, not subject to production test.

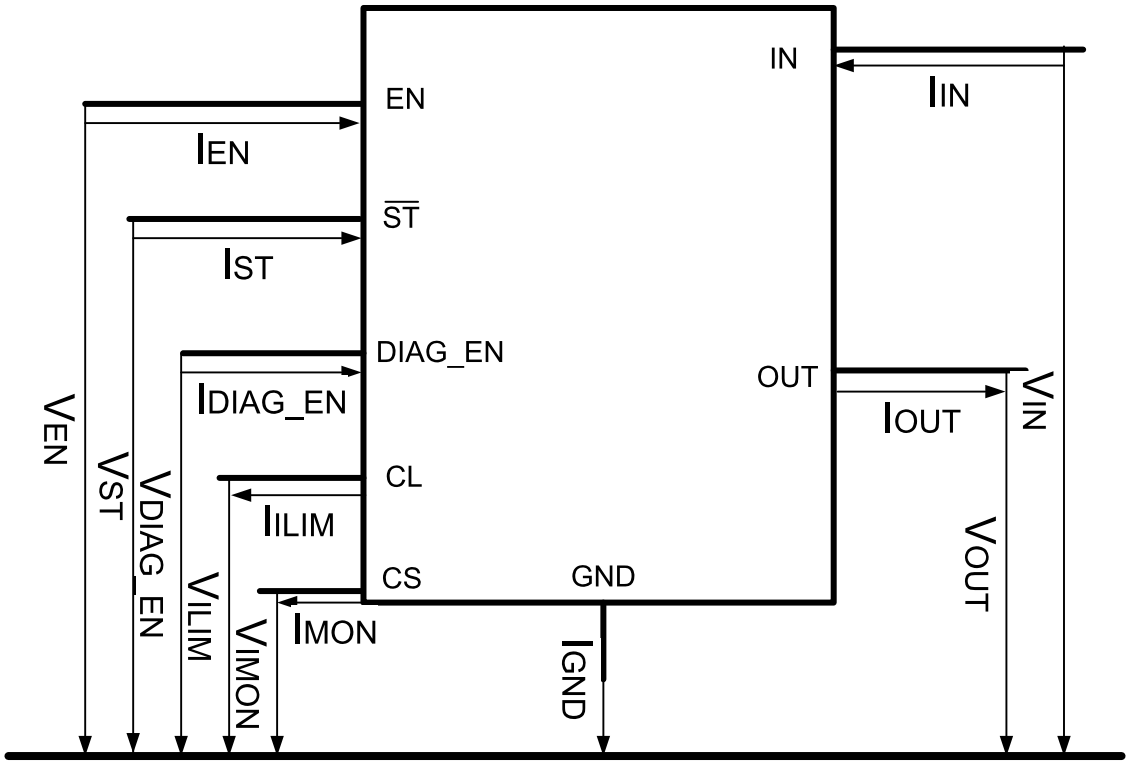


Figure 1. Pin Current and Voltage Conventions

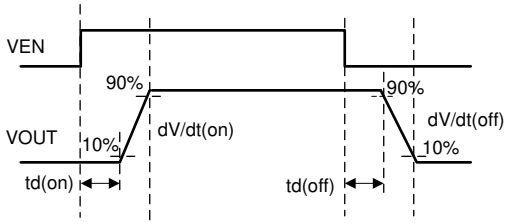


Figure 2. Output Delay Characteristics

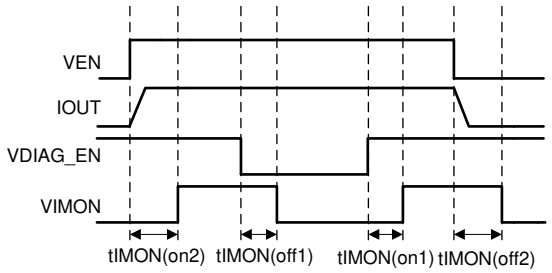


Figure 3. Current sense Delay Characteristics

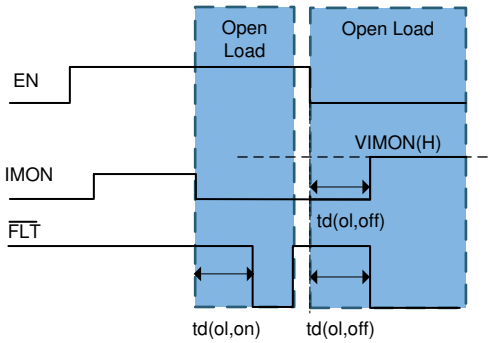


Figure 4. Open Load Blanking Time Characteristics

6.8 Typical Characteristics

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

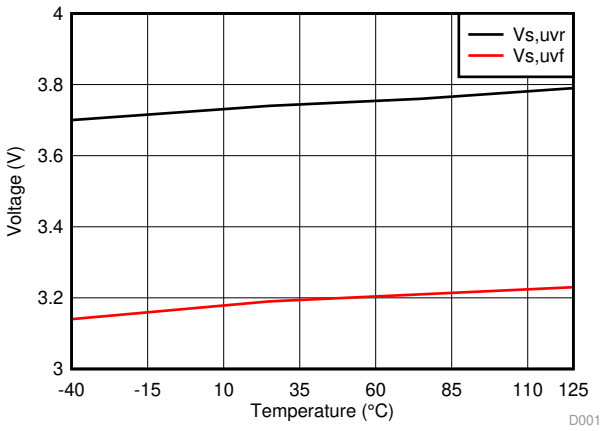


図 5. IN Pin Undervoltage Rising and Falling Thresholds $V_{IN,UVR}$ and $V_{IN,UVF}$

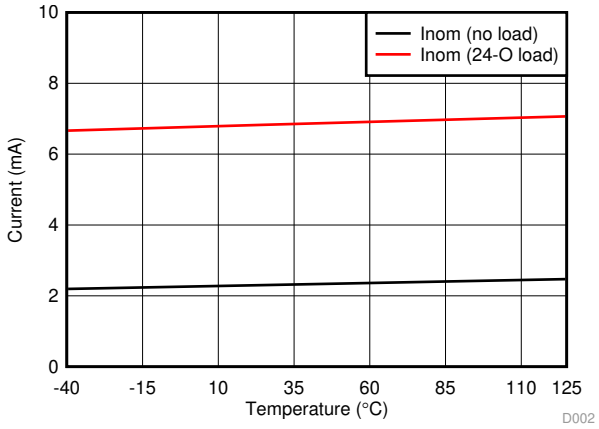


図 6. I_{nom} With No Load and 24-Ω Load

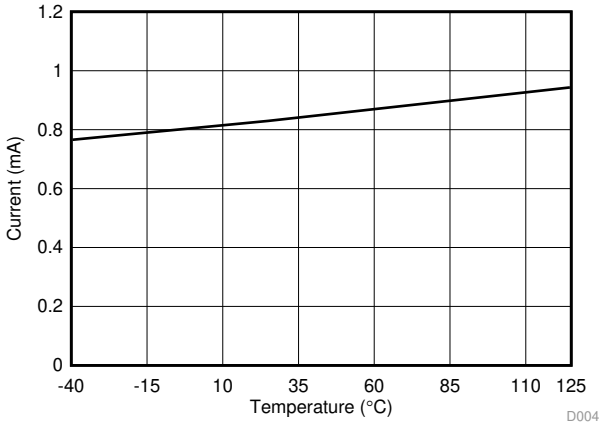


図 7. $I_{off,diag}$ as a Function of Temperature

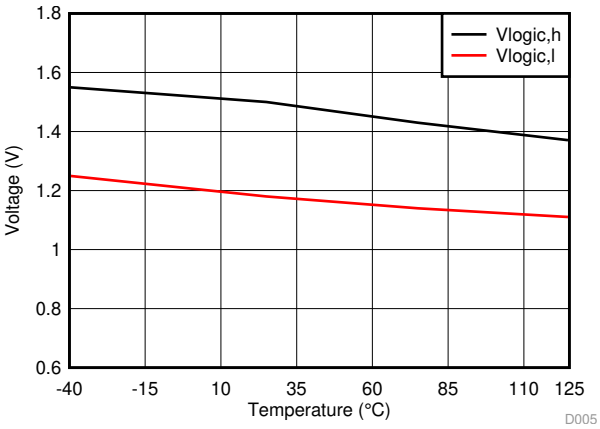


図 8. $V_{logic,h}$ and $V_{logic,l}$

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

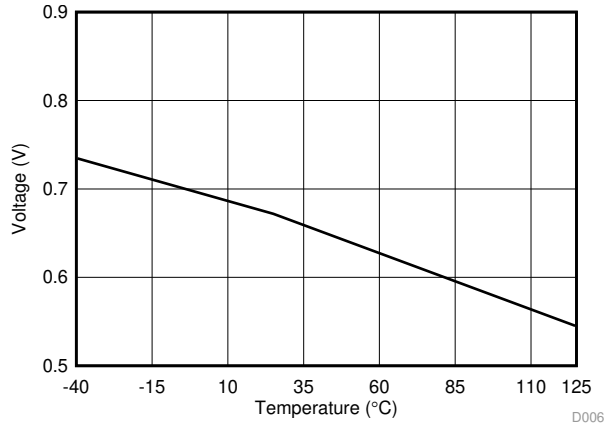


図 9. Drain-to-source Diode Voltage VF

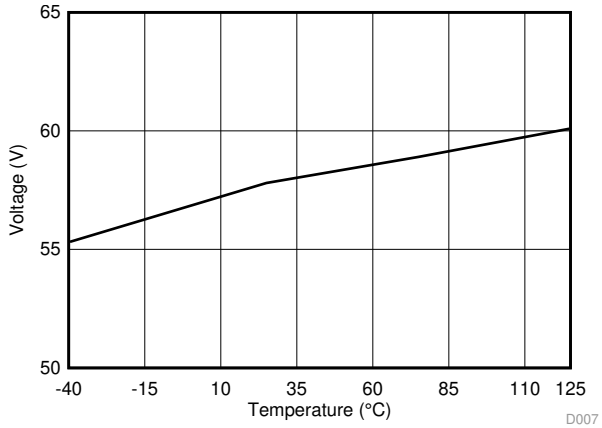


図 10. $V_{DS,\ Clamp}$

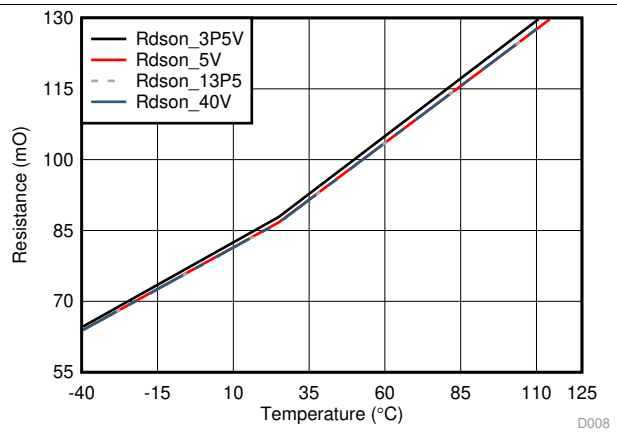


図 11. FET R_{DSON}

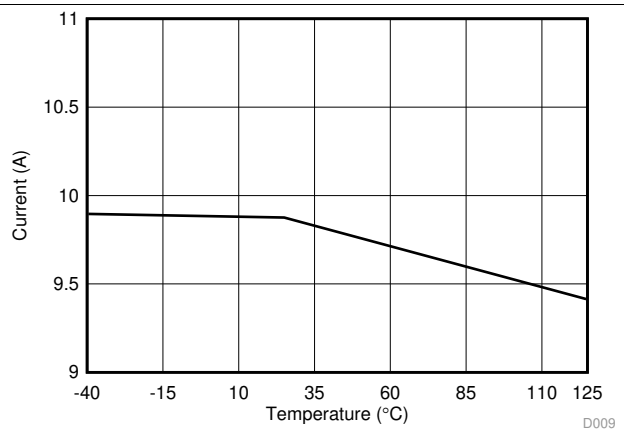


図 12. Current Limit $I_{lim,nom}$

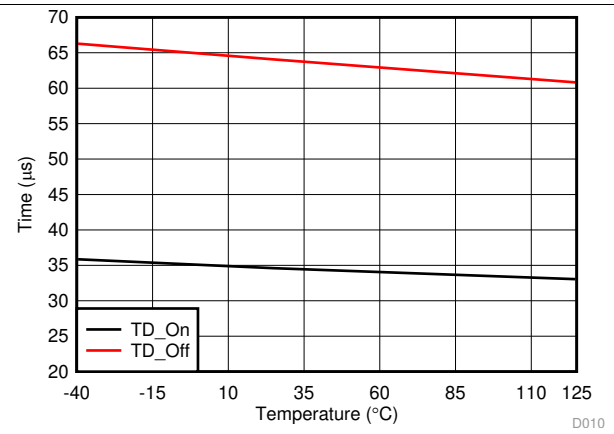


図 13. TDon and TDoff

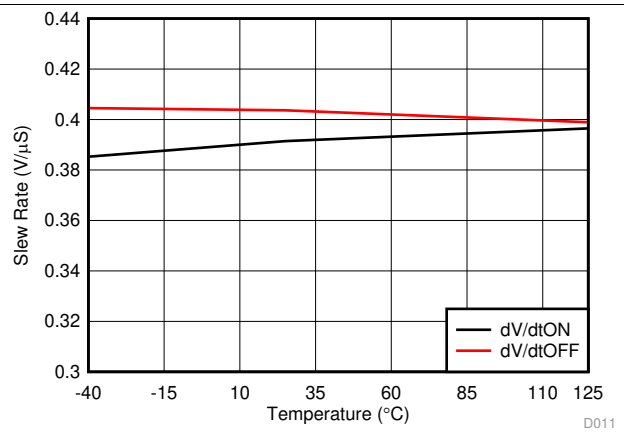


図 14. dV/dtON and dV/dtOFF

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

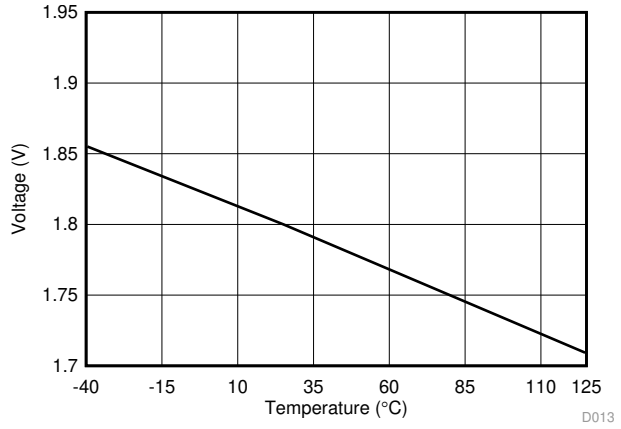


図 15. $V_{ol,off}$

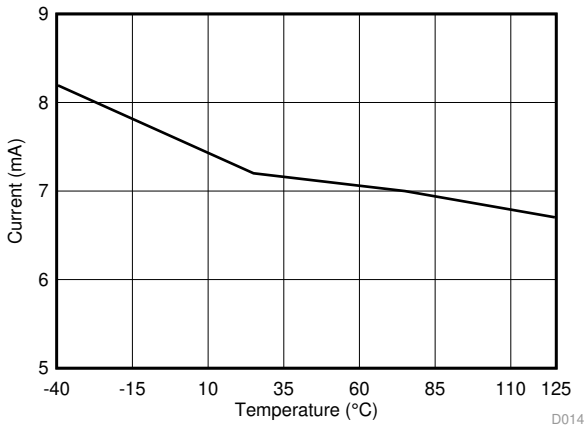


図 16. $I_{ol,on}$

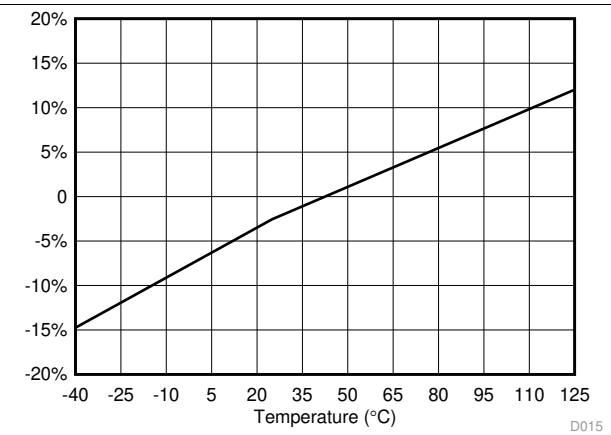


図 17. $K_{(IMON)}$ at I_{OUT} = 5 mA, V_{IN} = 24 V

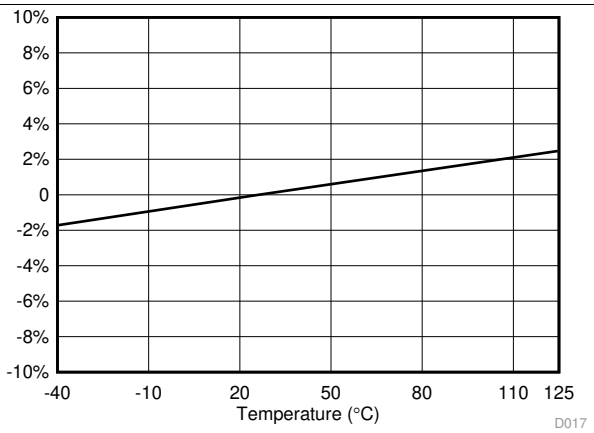


図 18. $K_{(IMON)}$ at I_{OUT} = 25 mA, V_{IN} = 24 V

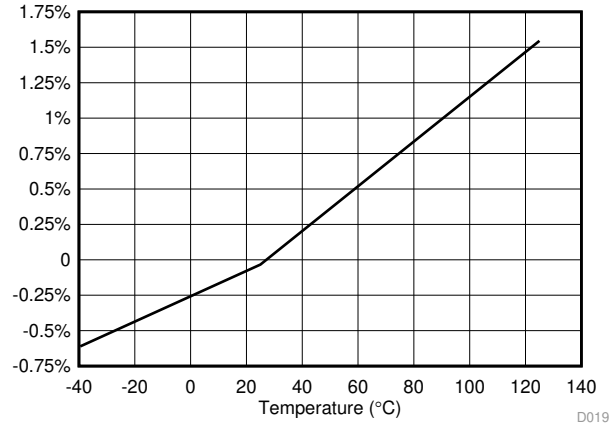


図 19. $K_{(IMON)}$ at I_{OUT} = 50 mA, V_{IN} = 24 V

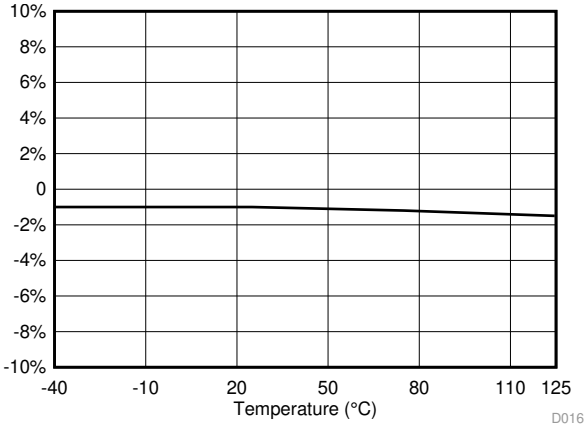


図 20. $K_{(IMON)}$ at I_{OUT} = 100 mA, V_{IN} = 24 V

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

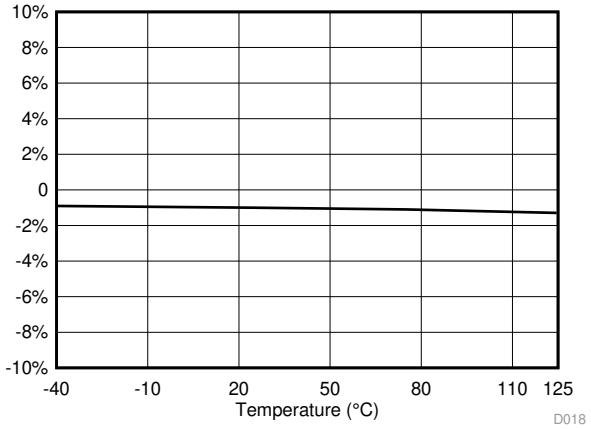


図 21. $K_{(IMON)}$ at I_{OUT} = 1 A, V_{IN} = 24 V

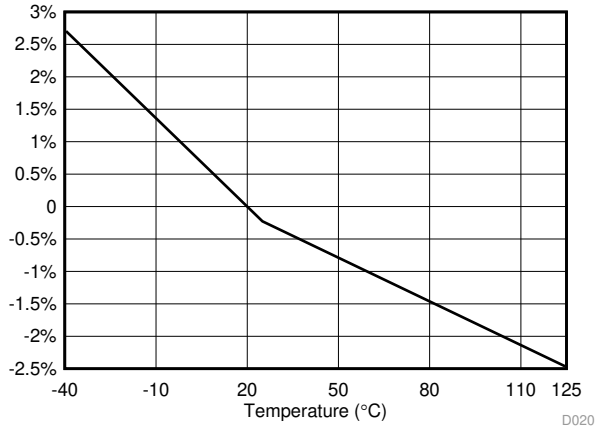


図 22. $K_{(ILIM)}$ at I_{ILIM} = 0.5 A, V_{IN} = 24 V

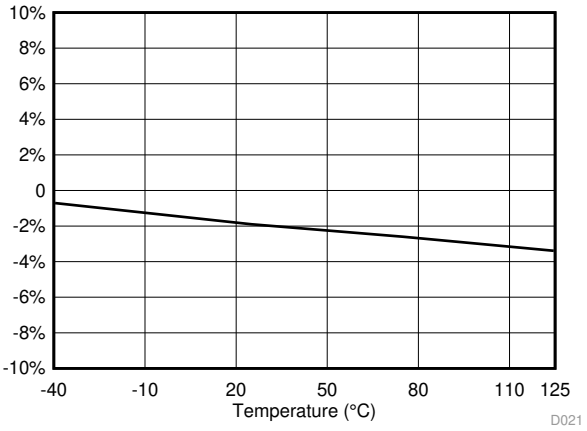


図 23. $K_{(ILIM)}$ at I_{ILIM} = 1.6 A, V_{IN} = 24 V

7 Detailed Description

7.1 Overview

The TPS27S100x is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. Full diagnostics and high-accuracy current-monitor features enable intelligent control of the load. An adjustable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital fault status and analog current monitor output.

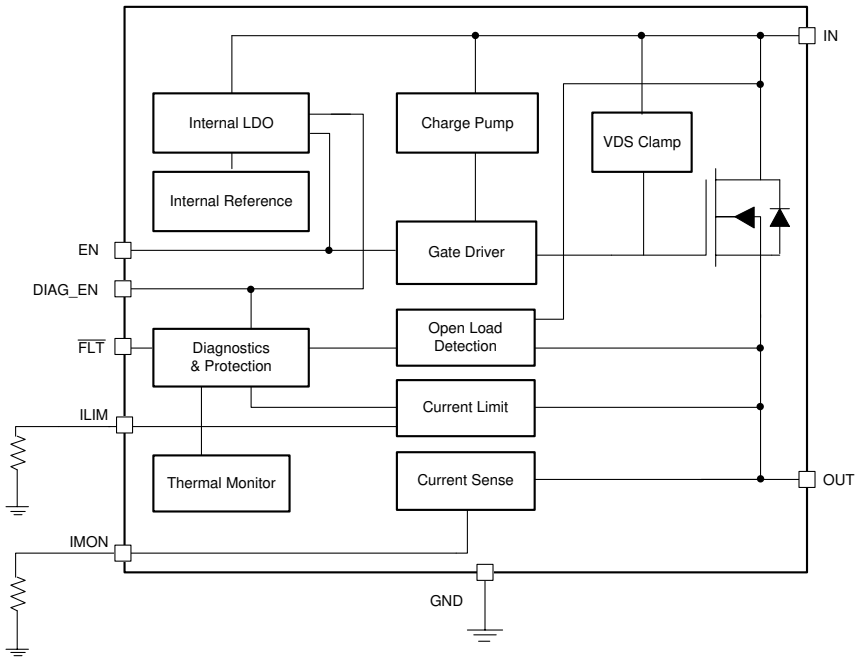
For TPS27S100A, the digital fault status report is implemented with an open-drain structure. For TPS27S100B, high-accuracy current-monitor allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source a fraction (1 / $K_{(IMON)}$) of the load current. $K_{(IMON)}$ is a nearly constant value across the temperature and supply voltage.

The external high-accuracy current limit allows setting the current limit value by application. Under start-up or short-circuit conditions, it improves the reliability of the system significantly by clamping the inrush current effectively. It can also save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit is also implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, motors, and so forth. During switching-off cycle, both the energy of the power supply and the inductive load are dissipated on the device itself. See *Inductive-Load Switching-Off Clamp* for more details.

The TPS27S100x device can be used as a high-side switch to drive a wide variety of resistive, inductive, and capacitive loads.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Accurate Current Monitor

For TPS27S100B, the high-accuracy current-monitor function is internally implemented, which allows a better real-time monitoring effect. A current mirror is used to source 1 / K_{IMON} of the load current, flowing out to the external resistor between the IMON and GND.

Feature Description (continued)

K_{IMON} is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage range. Each part is factory calibrated during production test, so user-calibration is not required in most cases.

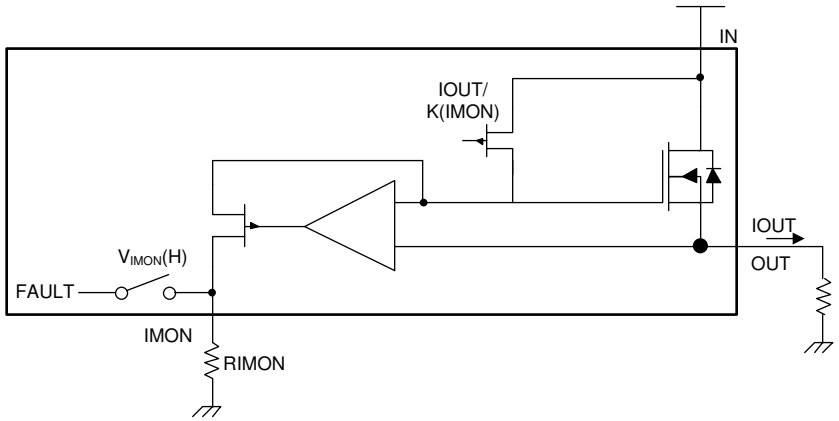


図 24. Current-monitor Block Diagram

When a fault occurs, the IMON pin also works as a fault report with a pullup voltage, $V_{IMON(H)}$.

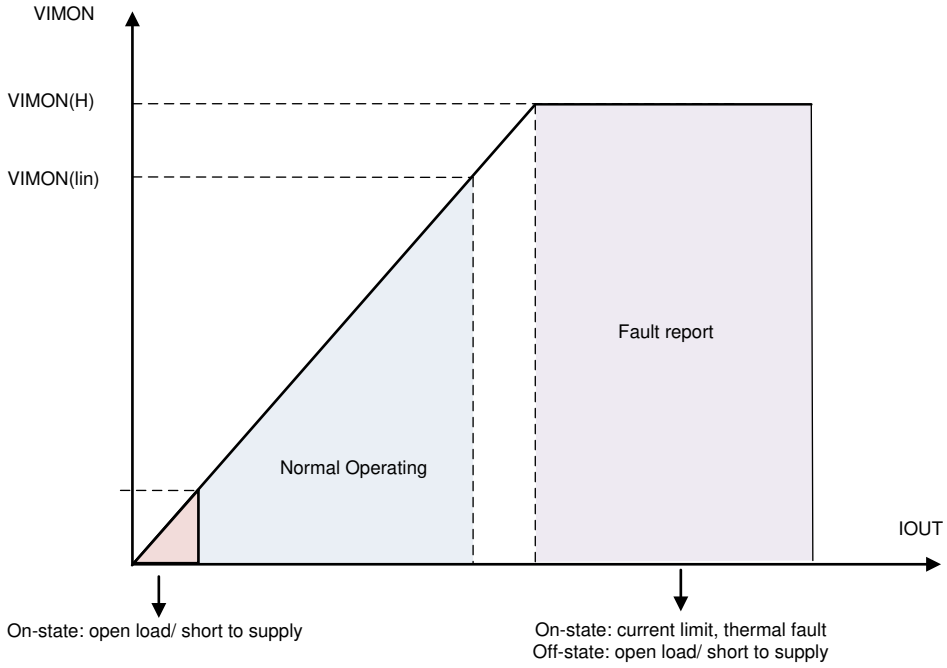


図 25. IMON Output-Voltage Curve

Use Equation 1 to calculate R_{IMON}. Also, please ensure V_{IMON} is within the current-sense linear region $V_{IMON(lin)}$ across the full range of the load current.

$$R_{IMON} = \frac{V_{IMON}}{I_{IMON}} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} \quad (1)$$

Feature Description (continued)

7.3.2 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from over-stressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When the current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{ILIM(TSD)}$ to reduce the power dissipation on the power FET.

The device has two current-limit thresholds.

Internal current limit – The internal current limit is fixed at $I_{ILM(int)}$. Tie the ILIM pin directly to the device GND for large-transient-current applications.

External adjustable current limit – An external resistor is used to set the current-limit threshold. Use Equation 2 below to calculate the R_{ILIM}. $V_{ILIM(th)}$ is the internal band-gap voltage. $K_{(ILIM)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$R_{ILIM} = \frac{V_{IILM(th)} \cdot K_{(ILIM)}}{I_{OUT}} \quad (2)$$

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND.

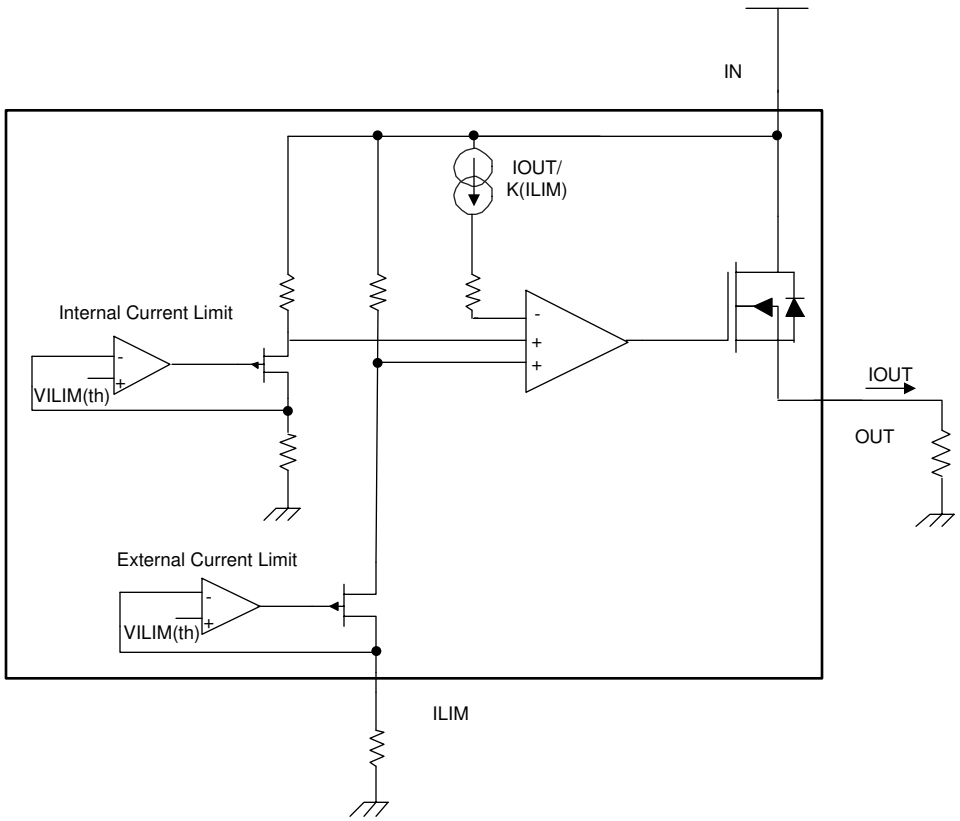


図 26. Current-Limit Block Diagram

For better protection from a hard short-to-GND condition (when the EN pin is enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

Feature Description (continued)

7.3.3 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

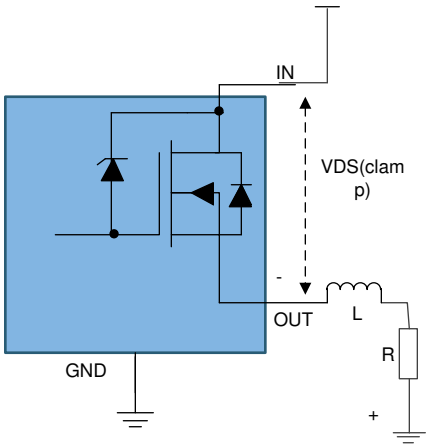


図 27. Drain-to-Source Clamping Structure

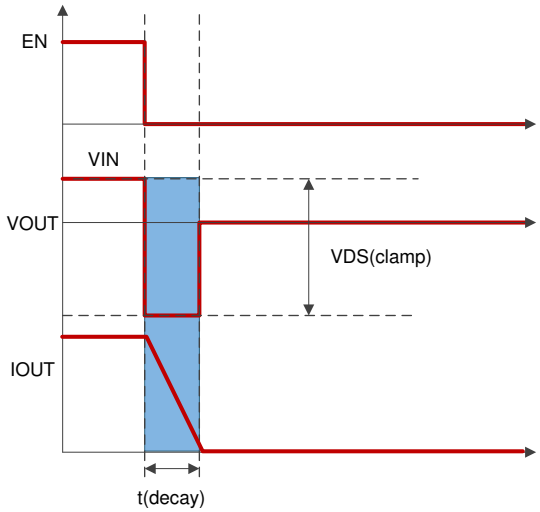


図 28. Inductive-Load Switching-Off Diagram

7.3.4 Full Protections and Diagnostics

表 1 is when DIAG_EN enabled. When DIAG_EN is low, all the diagnostics is disabled accordingly. The output is in high-impedance mode. Refer to 表 2 for details.

表 1. Fault Table

CONDITIONS	IN	OUT	CRITERION	$\overline{\text{FLT}}$ (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Normal	L	L		H	0	
	H	H		H	In linear region	
Short to GND	H	L	Current limit triggered.	L	$V_{IMON(H)}$	AUTO

Feature Description (continued)

表 1. Fault Table (continued)

CONDITIONS	IN	OUT	CRITERION	$\overline{FLT}$ (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Open load(1) Short to supply	H	H	TPS27S100A: $I_{OUT} < I_{(ol,on)}$ TPS27S100B: Judged by users	L	Almost 0	AUTO
	L	H	$V_{IN} - V_{OUT} < V_{(ol,off)}$	L	$V_{IMON(H)}$	AUTO
Thermal shutdown	H		T_{SD} triggered	L	$V_{IMON(H)}$	Recovery when $T_J < T_{(SD,rst)}$ or when EN toggles.
Thermal swing	H		T_{SW} triggered	L	$V_{IMON(H)}$	AUTO

(1) Need external pull-up resistor during off-state

表 2. DIAG_EN Logic Table

DIAG_EN	EN	PROTECTIONS AND DIAGNOSTICS
HIGH	ON	See 表 1
	OFF	See 表 1
LOW	ON	Diagnostics disabled, protection normal IMON or $\overline{FLT}$ is high Impedance
	OFF	Diagnostics disabled, no protections IMON or $\overline{FLT}$ is high impedance

7.3.4.1 Short-to-GND and Overload Detection

When the switch is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{ILIM(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

7.3.4.2 Open-Load Detection

When the channel is on, for TPS27S100A, if the current flowing through the output is less than $I_{(ol,on)}$, the device recognizes an open-load fault. For TPS27S100B, if an open-load event occurs, it can be detected as an ultra-low V_{IMON} and handled by the microcontroller.

When the channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{IN} - V_{OUT} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

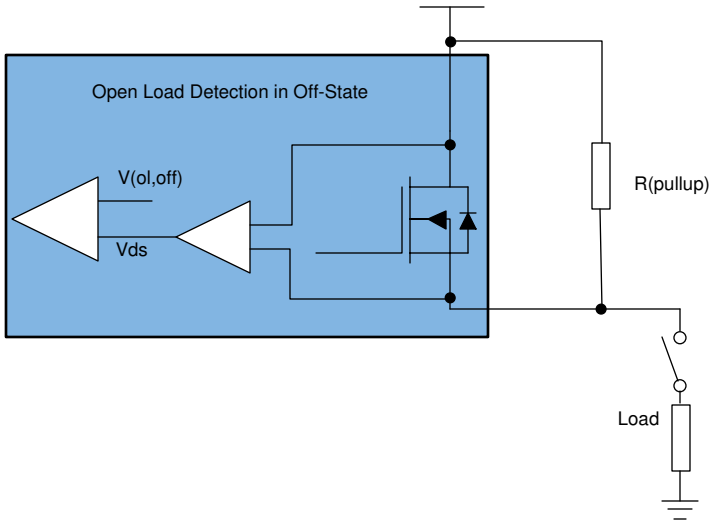


図 29. Open-Load Detection Circuit in Off-State

7.3.4.3 Short-to-Supply Detection

Short-to-Supply has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See 表 1 for more details.

7.3.4.4 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the respective output turns off.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

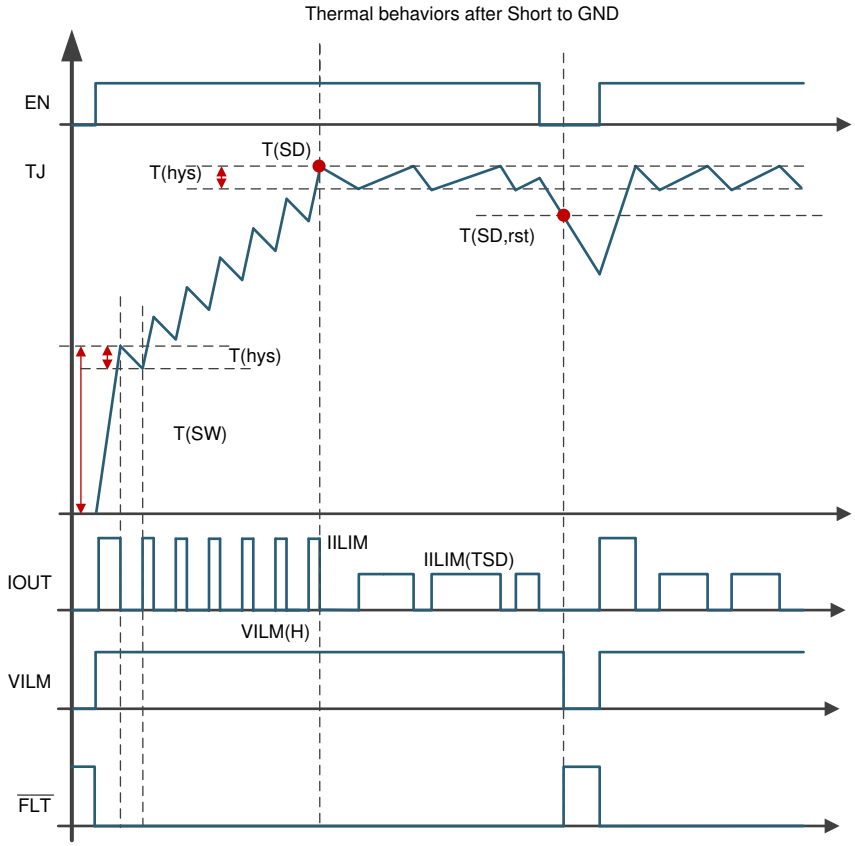


図 30. Thermal Behavior Diagram

7.3.4.5 UVLO Protection

The device monitors the supply voltage V_{IN}, to prevent unpredicted behaviors when V_{IN} is too low. When V_{IN} falls down to $V_{IN(uvf)}$, the device shuts down. When V_{IN} rises up to $V_{IN(uvr)}$, the device turns on.

7.3.4.6 Loss of GND Protection

When loss of GND occurs, output is shut down regardless of whether the EN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

7.3.4.7 Reverse Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

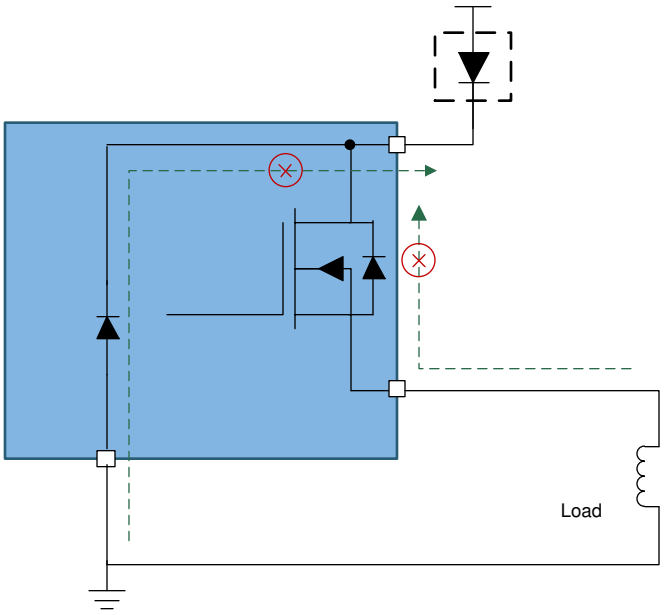


図 31. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

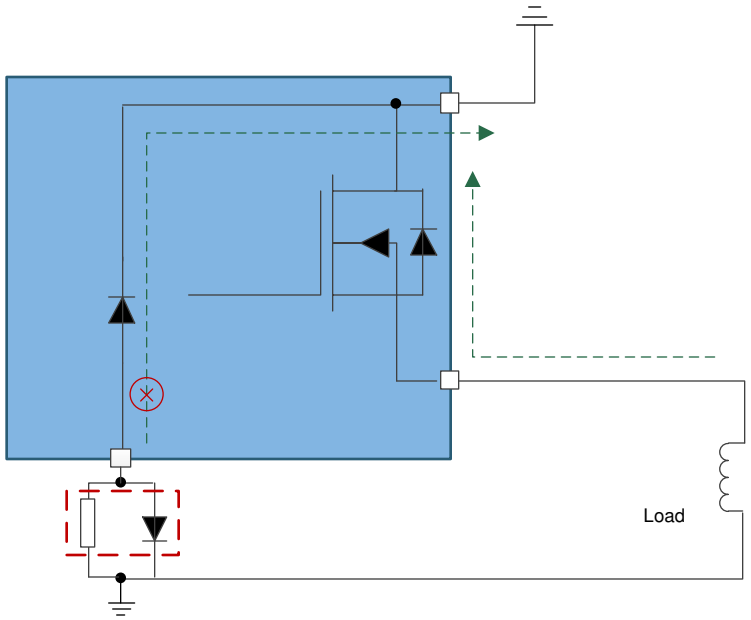


図 32. Reverse-Current External Protection, Method 2

7.3.4.8 Protection for MCU I/Os

TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

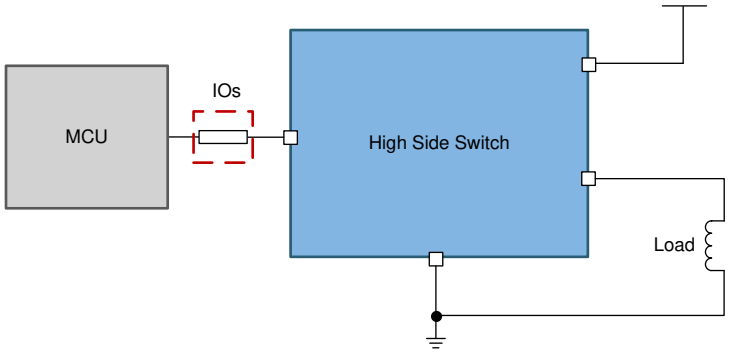


図 33. MCU I/O External Protection

7.4 Device Functional Modes

7.4.1 Working Mode

The device has three working modes: the normal mode, the standby mode, and the standby mode with diagnostics.

Device Functional Modes (continued)

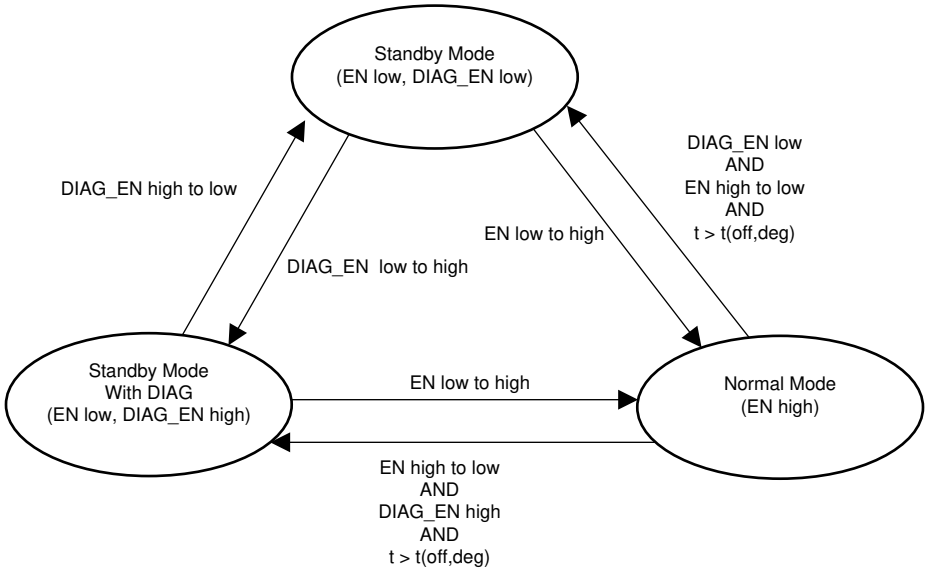


図 34. Working Modes

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is capable of driving a wide variety of resistive, inductive, and capacitive loads. Full diagnostics and high accuracy current-monitor features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

図 35 shows an example of how to design the external circuitry parameters.

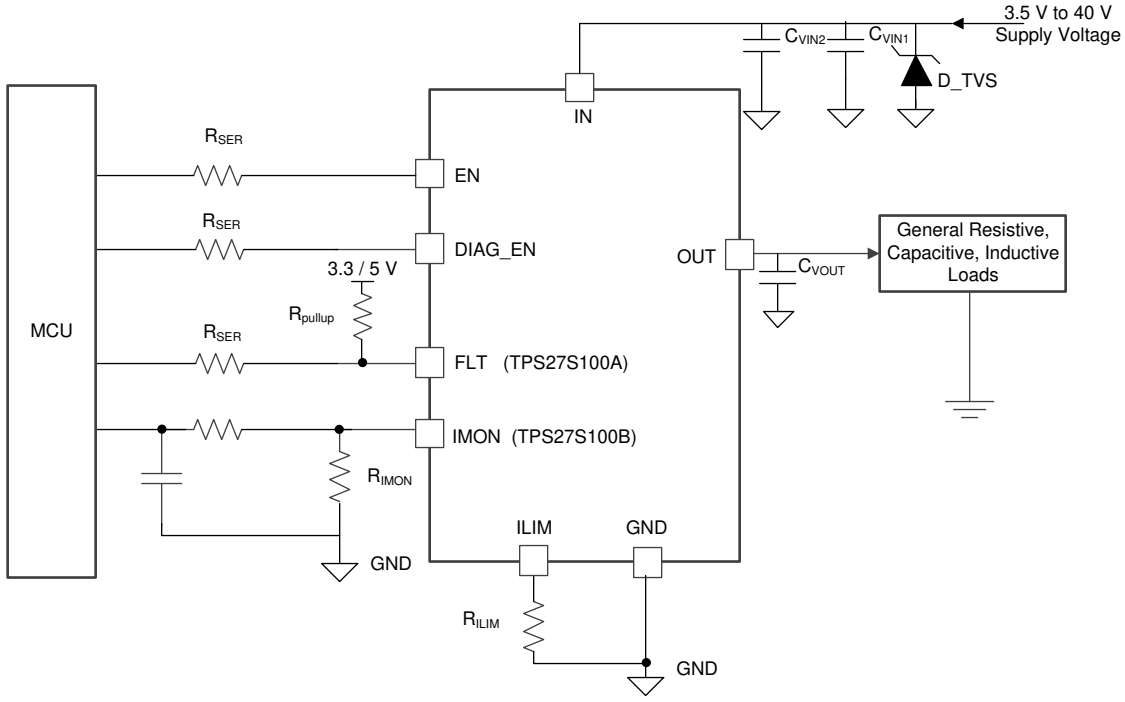


図 35. Typical Application Circuitry

表 3. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SER}	15 kΩ	Protect microcontroller and device I/O pins
R_{IMON}	1 kΩ	Translate the sense current into sense voltage
C_{SNS}	100 pF - 10 nF	Low-pass filter for the ADC input
R_{ILIM}	0.82 kΩ	Set current limit threshold
$C_{VIN1/2}$	4.7 nF to Device GND	Filtering of high frequency noise
	220 nF to Module GND	Stabilize the input supply and voltage spike suppression for surge transient immunity.
C_{OUT}	22 nF	Immunity to ESD
D_{TVS}	36V TVS diode	Transient voltage clamp for surge transient immunity

8.2.1 Design Requirements

- V_{IN} range from 9 V to 30 V
- Nominal current of 2 A
- Current Monitor for fault monitoring
- Expected current limit value of 5 A
- Full diagnostics with 5-V MCU

8.2.2 Detailed Design Procedure

To keep the 2-A nominal current in the 0 to 4-V current-sense range, calculate the R_{IMON} resistor using Equation 3. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{IMON} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} = \frac{4 \times 500}{2} = 1000\ \Omega \tag{3}$$

To set the adjustable current limit value at 5-A, calculate R_{ILIM} using Equation 4.

$$R_{ILIM} = \frac{V_{LIM(th)} \cdot K_{(ILIM)}}{I_{OUT}} = \frac{1.233 \cdot 2000}{5} = 493.2\ \Omega \tag{4}$$

TI recommends R_{SER} = 10 kΩ for 5-V MCU, and R_{pullup} = 10 kΩ as the pull-up resistor.

8.2.3 Application Curves

図 36 shows a an example of initial inrush or short-circuit current limit. Test conditions: EN is from low to high, load is resistive short-to-GND or with a 470-µF capacitive load, external current limit is 2 A. CH1 is the output current. CH3 is the EN step.

図 37 shows an example of current limit during hard short-circuit. Test conditions: EN is high, load is (5 µH + 100 mΩ), external current limit is 1 A. A short to GND suddenly happens.

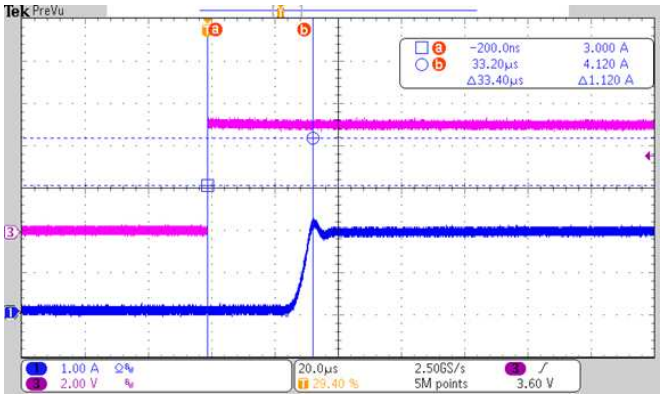


図 36. Initial Short-to-GND Waveform

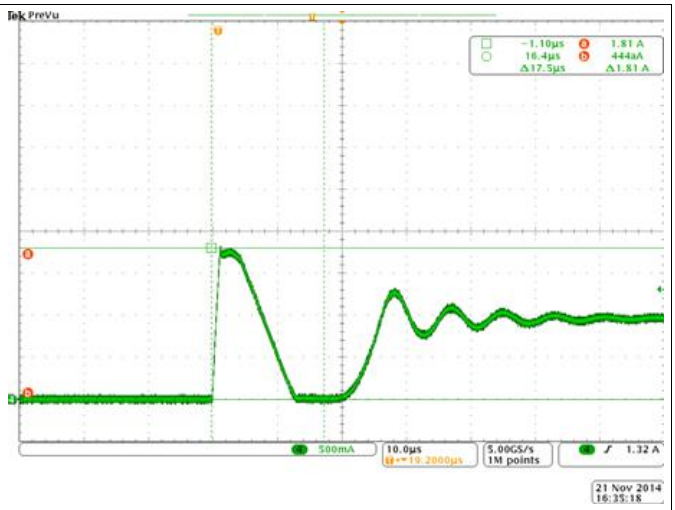


図 37. Hard Short-to-GND Waveform

9 Power Supply Recommendations

The device is qualified for both 12-V and 24-V applications. The typical power input is a 12-V or 24-V industrial power supply.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

10.2 Layout Example

10.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

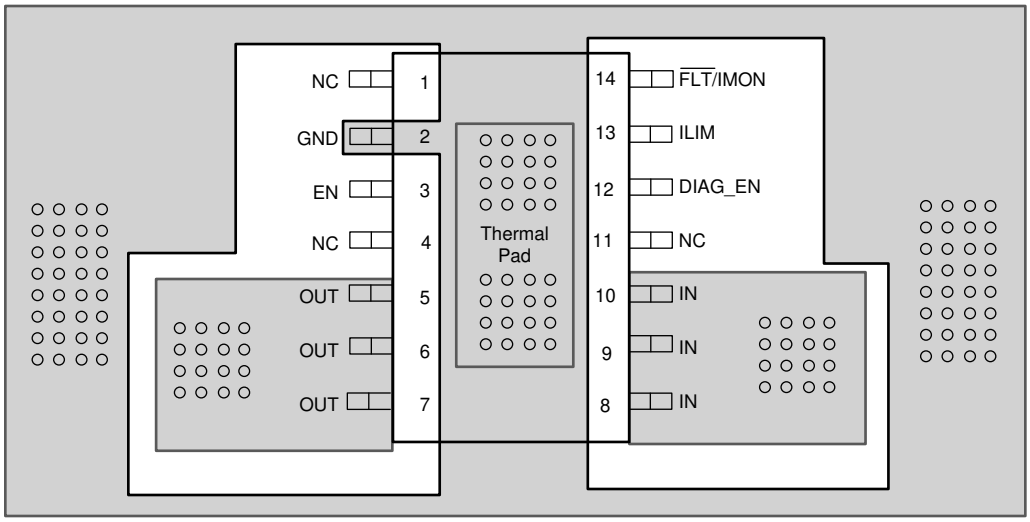


図 38. Layout Without a GND Network

Layout Example (continued)

10.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

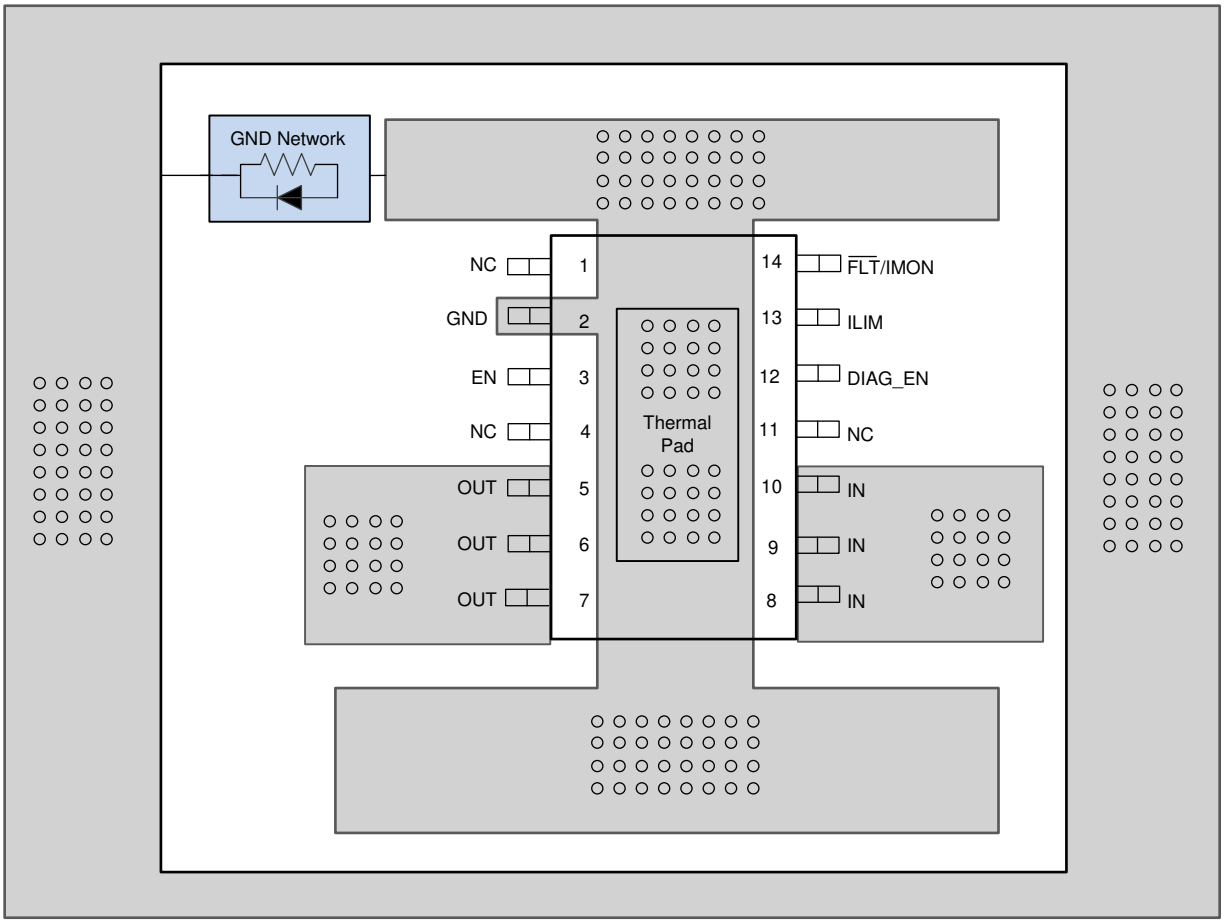


図 39. Layout With a GND Network

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS27S100APWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A
TPS27S100APWPR.A	Active	Production	null (null) |	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A
TPS27S100APWPRG4.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A
TPS27S100APWPT	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A
TPS27S100APWPT.A	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A
TPS27S100ARRKR	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A
TPS27S100ARRKR.A	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A
TPS27S100ARRKT	Active	Production	WQFN (RRK) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A
TPS27S100ARRKT.A	Active	Production	WQFN (RRK) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A
TPS27S100BPWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B
TPS27S100BPWPR.A	Active	Production	null (null) |	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B
TPS27S100BPWPT	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B
TPS27S100BPWPT.A	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B
TPS27S100BRRKR	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B
TPS27S100BRRKR.A	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B
TPS27S100BRRKRG4	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B
TPS27S100BRRKRG4.A	Active	Production	WQFN (RRK) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B
TPS27S100BRRKT	Active	Production	WQFN (RRK) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B
TPS27S100BRRKT.A	Active	Production	WQFN (RRK) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

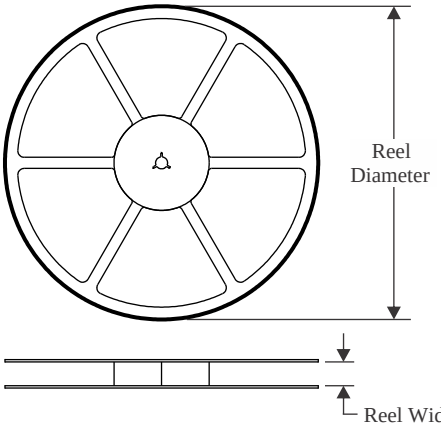
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

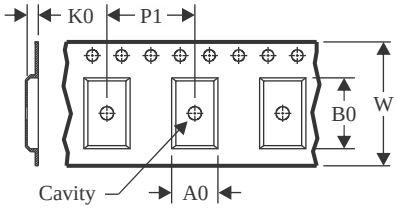
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

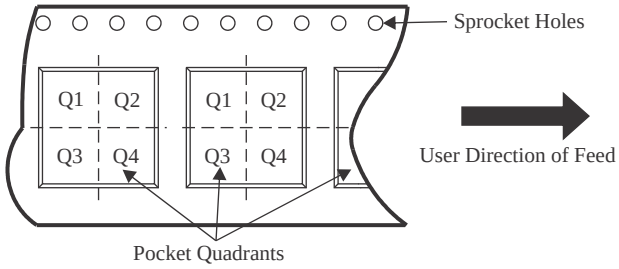


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

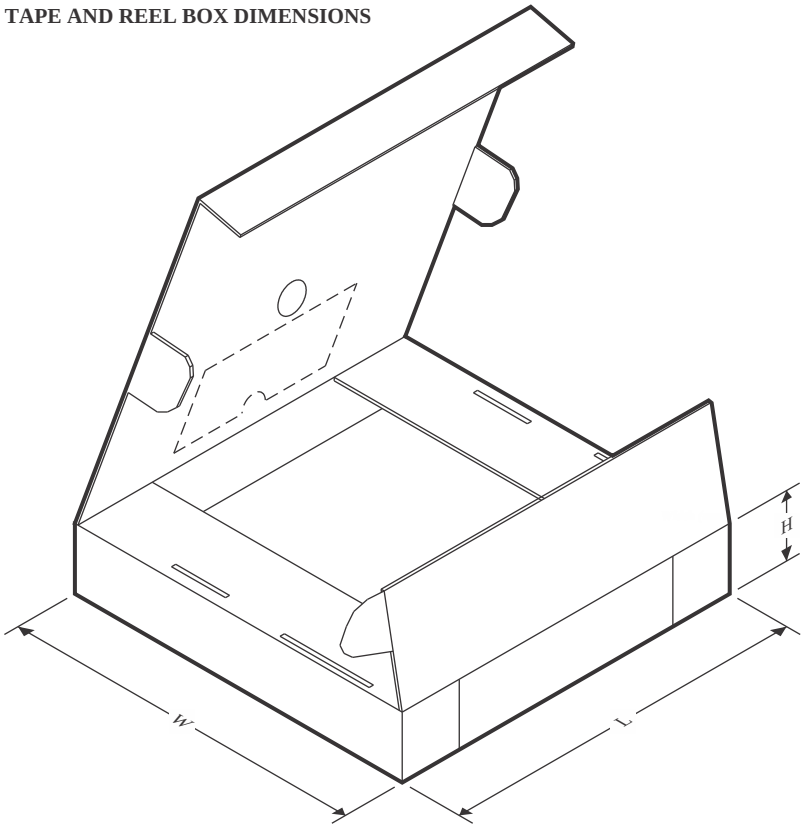
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27S100APWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100ARRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100ARRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100BRRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BRRKRG4	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BRRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

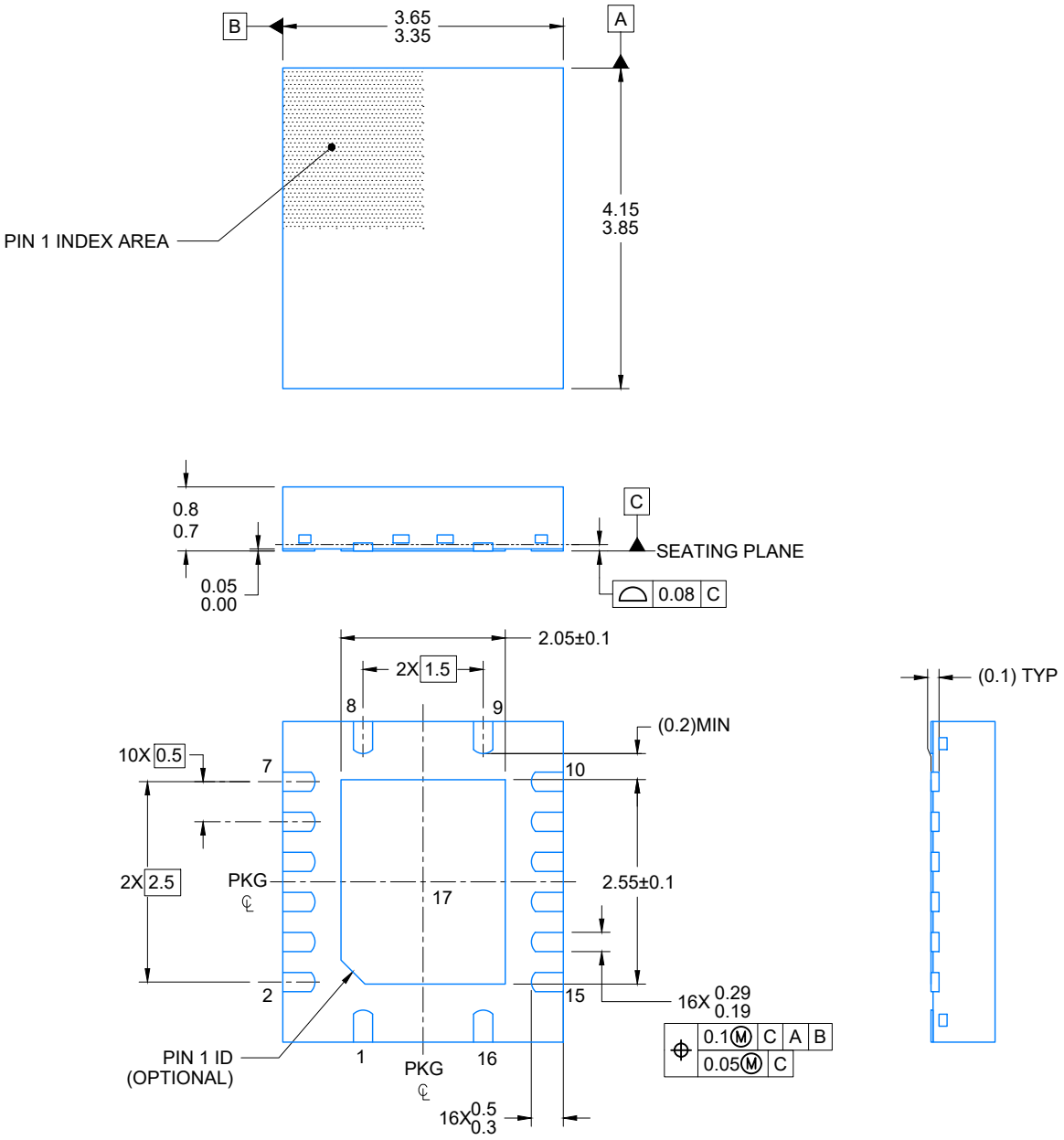
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27S100APWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100ARRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100ARRKT	WQFN	RRK	16	250	210.0	185.0	35.0
TPS27S100BPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100BRRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100BRRKRG4	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100BRRKT	WQFN	RRK	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

RRK0016A

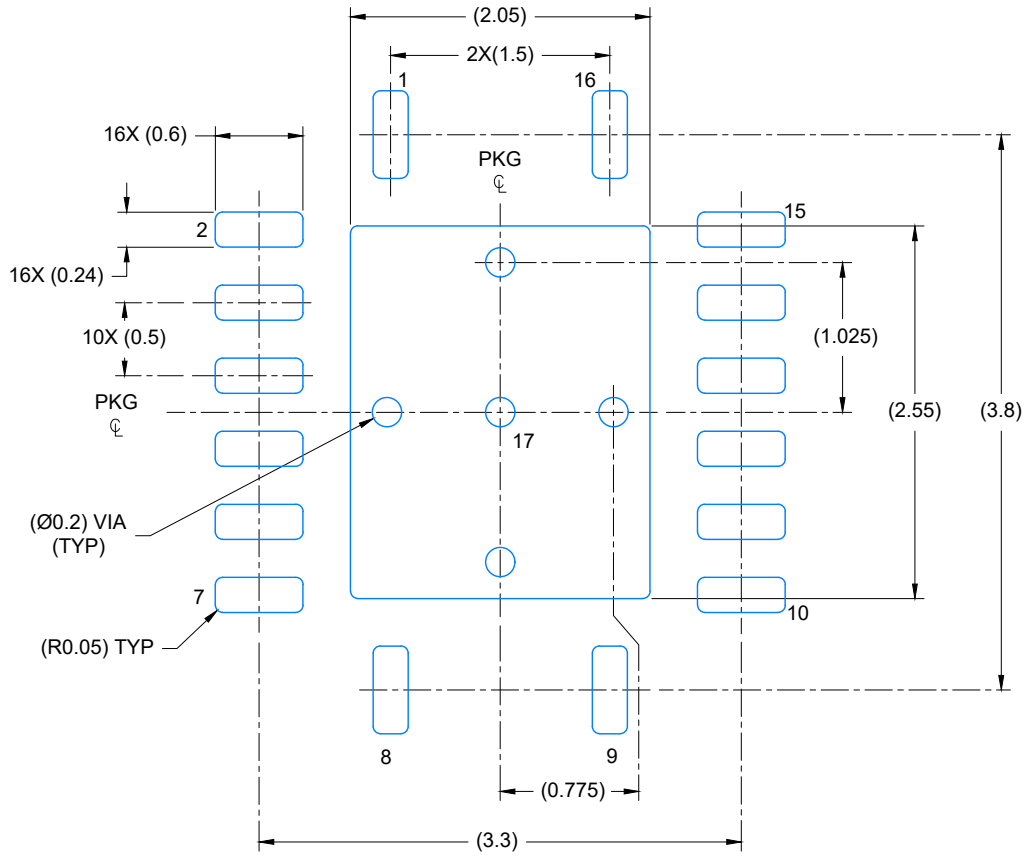
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

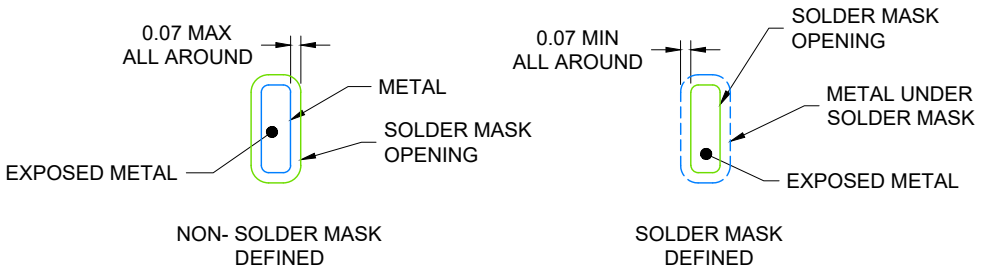


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4424663 / B 03/2020

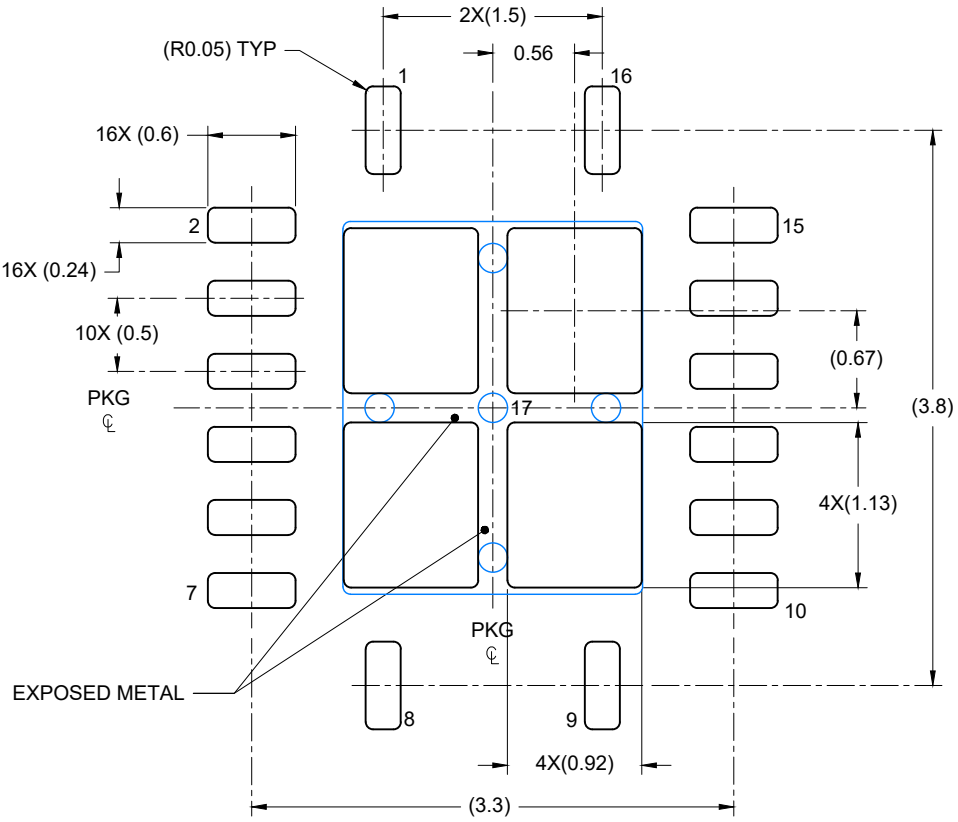
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 80%
SCALE: 20X

4424663 / B 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

GENERIC PACKAGE VIEW

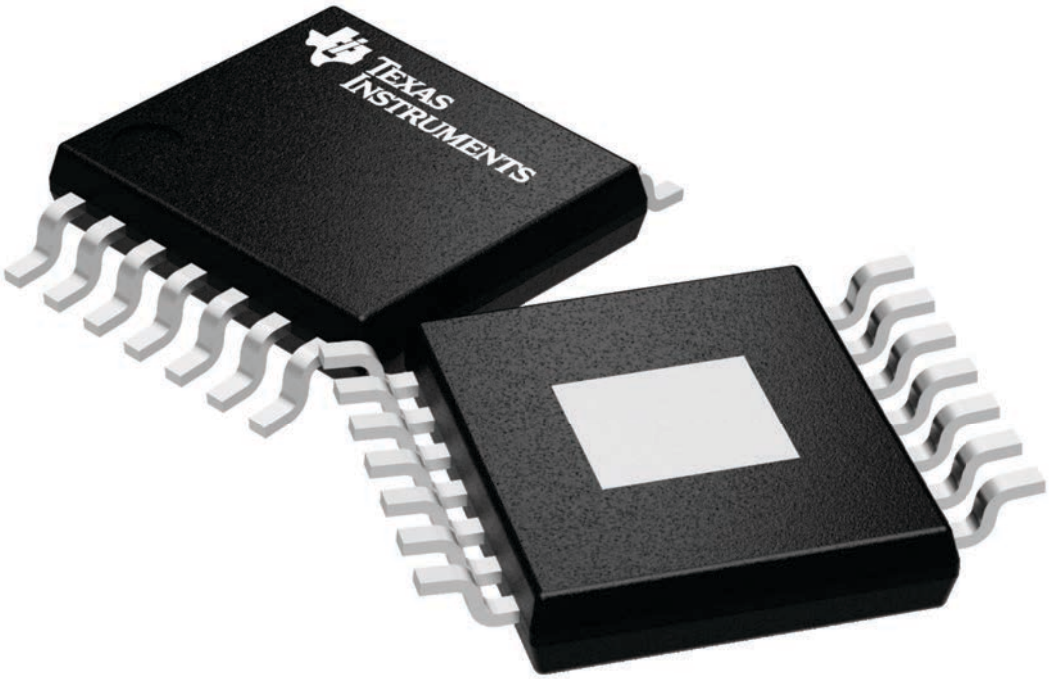
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



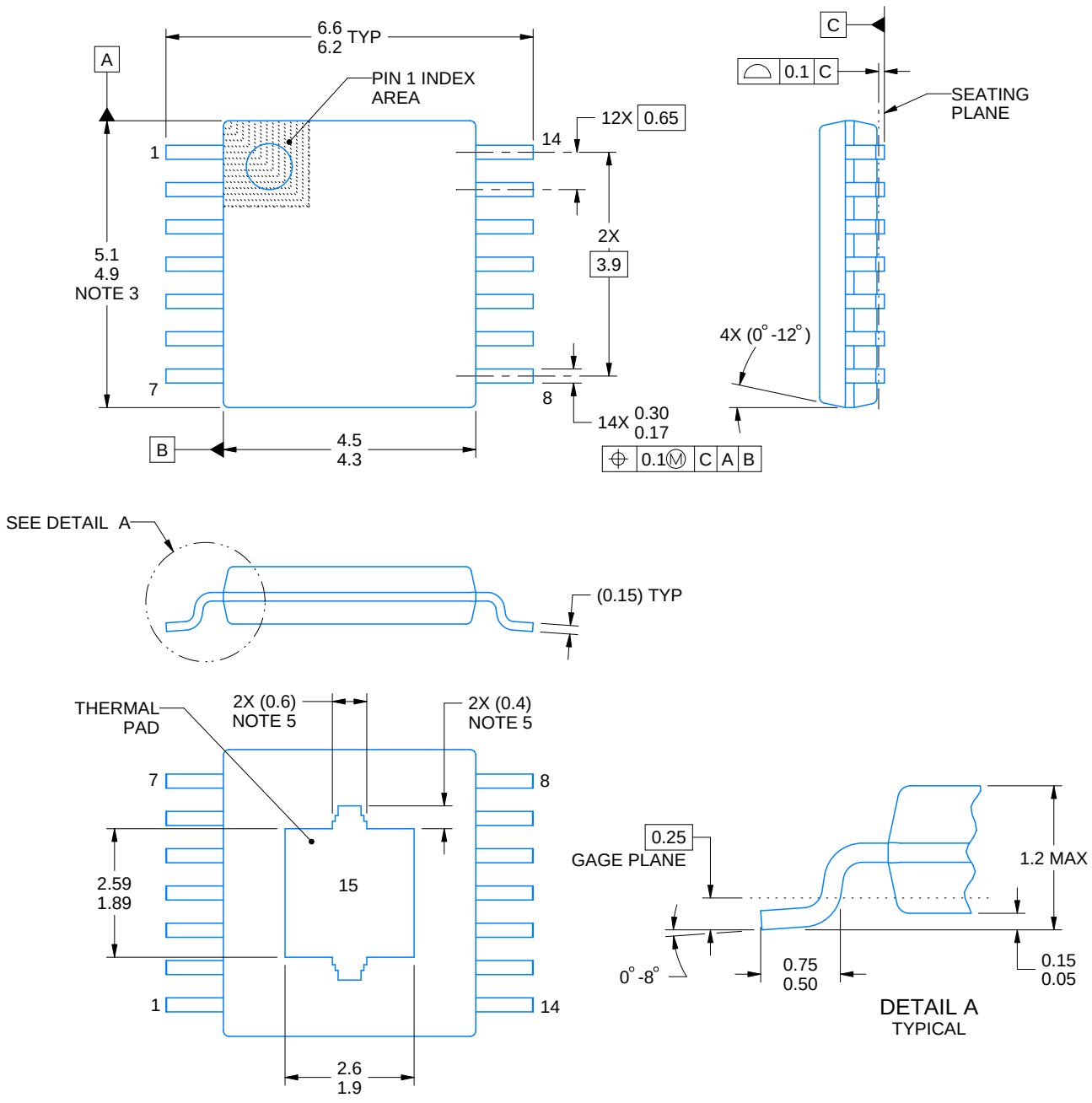
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

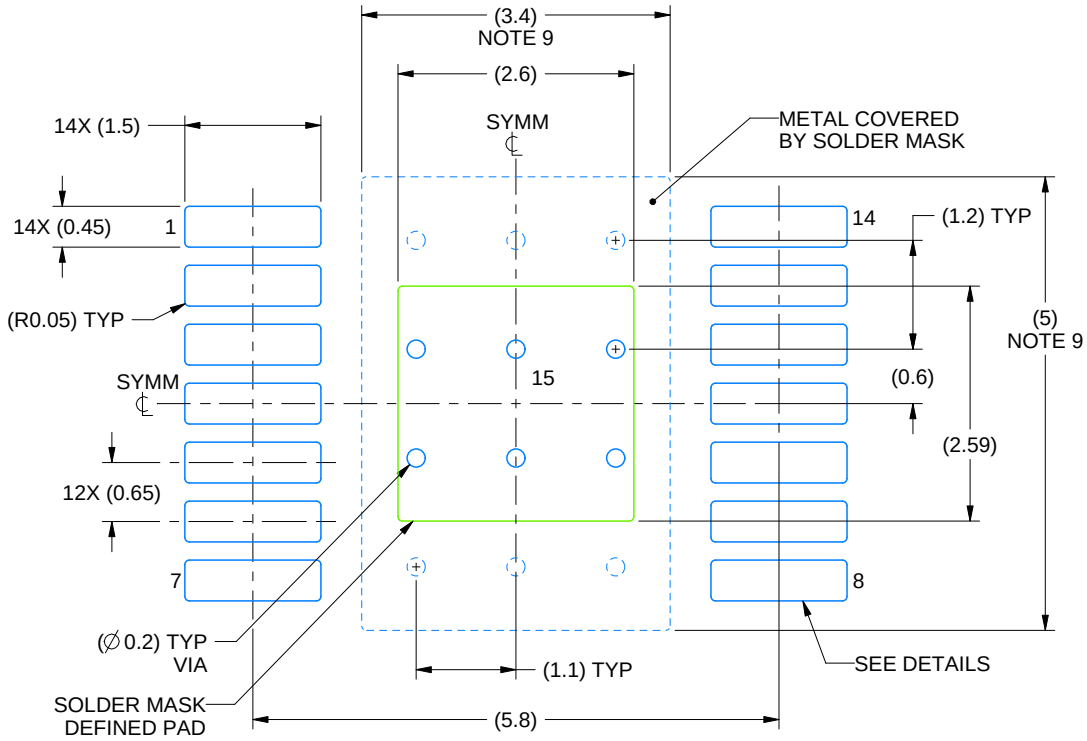
SMALL OUTLINE PACKAGE



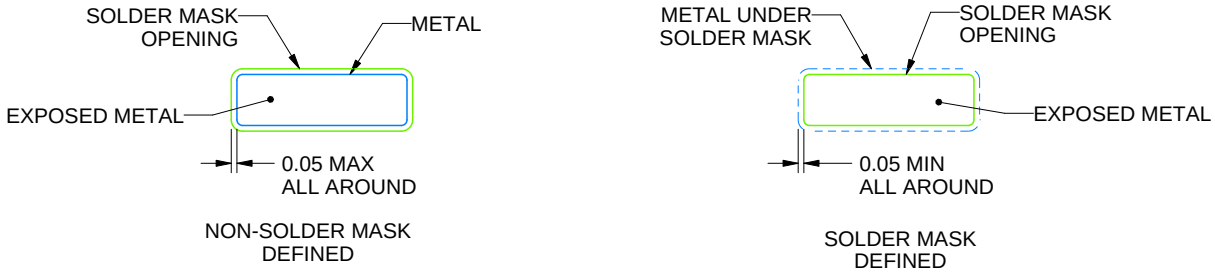
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

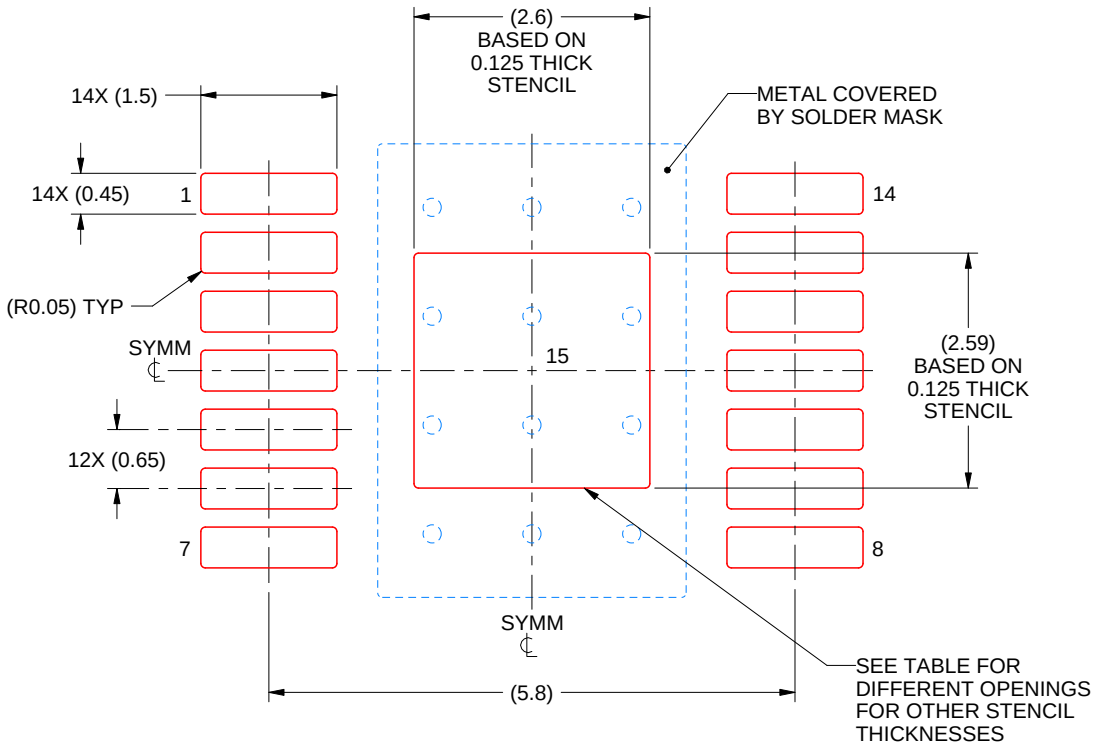


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265