

TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

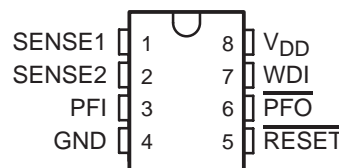
- Qualified for Automotive Applications
- Dual Supervisory Circuits With Power Fail for DSP and Processor-Based Systems
- Voltage Monitor for Power Fail or Low-Battery Warning
- Watchdog Timer With 0.8-s Time-Out
- Power-On Reset Generator With Integrated 100-ms Delay Time
- Open-Drain Reset and Power-Fail Output
- Supply Current of 15 μ A (Typ)
- Supply Voltage Range . . . 2.7 V to 6 V
- Defined $\overline{\text{RESET}}$ Output From $V_{\text{DD}} \geq 1.1$ V
- SO-8 Package
- Temperature Range . . . -40°C to 125°C
- Applications Include:
Multivoltage DSPs and Processors
Portable Battery-Powered Equipment
Embedded Control Systems
Intelligent Instruments
Automotive Systems

description

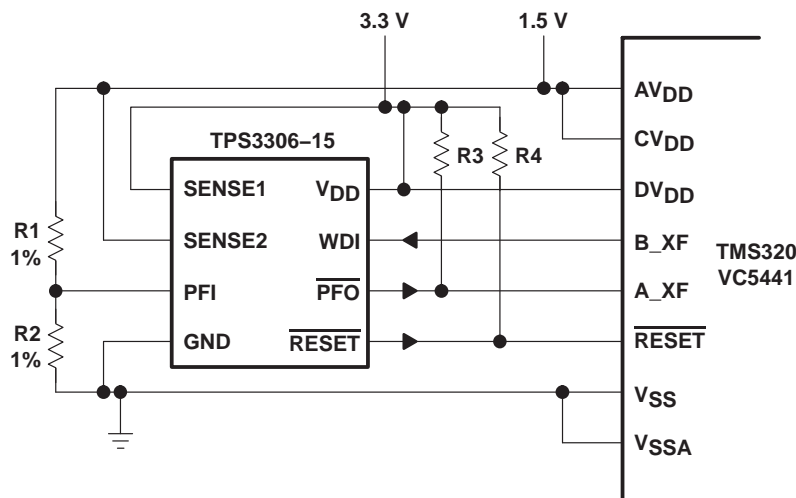
The TPS3306 family is a series of supervisory circuits designed for circuit initialization, which require two supply voltages, primarily in DSP and processor-based systems.

The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V.

D PACKAGE
(TOP VIEW)



TYPICAL OPERATING CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2008 Texas Instruments Incorporated

TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

description (continued)

The various supervisory circuits are designed to monitor the nominal supply voltage, as shown in the following supply-voltage monitoring table.

SUPPLY-VOLTAGE MONITORING

| DEVICE | NOMINAL SUPERVISED VOLTAGE | | THRESHOLD VOLTAGE (TYP) | |
|------------|----------------------------|--------|-------------------------|--------|
| | SENSE1 | SENSE2 | SENSE1 | SENSE2 |
| TPS3306-15 | 3.3 V | 1.5 V | 2.93 V | 1.4 V |
| TPS3306-18 | 3.3 V | 1.8 V | 2.93 V | 1.68 V |
| TPS3306-20 | 3.3 V | 2 V | 2.93 V | 1.85 V |
| TPS3306-25 | 3.3 V | 2.5 V | 2.93 V | 2.25 V |
| TPS3306-33 | 5 V | 3.3 V | 4.55 V | 2.93 V |

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage, V_{DD} , becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSEn inputs and keep $\overline{\text{RESET}}$ active as long as SENSEn remains below the threshold voltage, V_{IT} .

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(\text{typ})} = 100 \text{ ms}$, starts after SENSE1 and SENSE2 inputs have risen above V_{IT} . When the voltage at SENSE1 or SENSE2 input drops below the V_{IT} , the output becomes active (low) again.

The integrated power-fail (PFI) comparator with separate open-drain ($\overline{\text{PFO}}$) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3306-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of the watch-dog timer (WDI). When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(\text{out})} = 0.50 \text{ s}$, $\overline{\text{RESET}}$ becomes active for the time period t_d . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3306-xx devices are available in standard 8-pin SO packages.

The TPS3306-xxQ family is characterized for operation over a temperature range of -40°C to 125°C .

AVAILABLE OPTIONS†

| T _A | PACKAGED DEVICES‡ | | TOP-SIDE MARKING |
|--|-------------------|-----------------|------------------|
| | SMALL OUTLINE (D) | | |
| -40°C to 125°C | Tape and reel | TPS3306-15QDRQ1 | 615Q1 |
| | Tape and reel | TPS3306-18QDRQ1 | 618Q1 |
| | Tape and reel | TPS3306-20QDRQ1 | 620Q1 |
| | Tape and reel | TPS3306-25QDRQ1 | 625Q1 |
| | Tape and reel | TPS3306-33QDRQ1 | 633Q1 |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

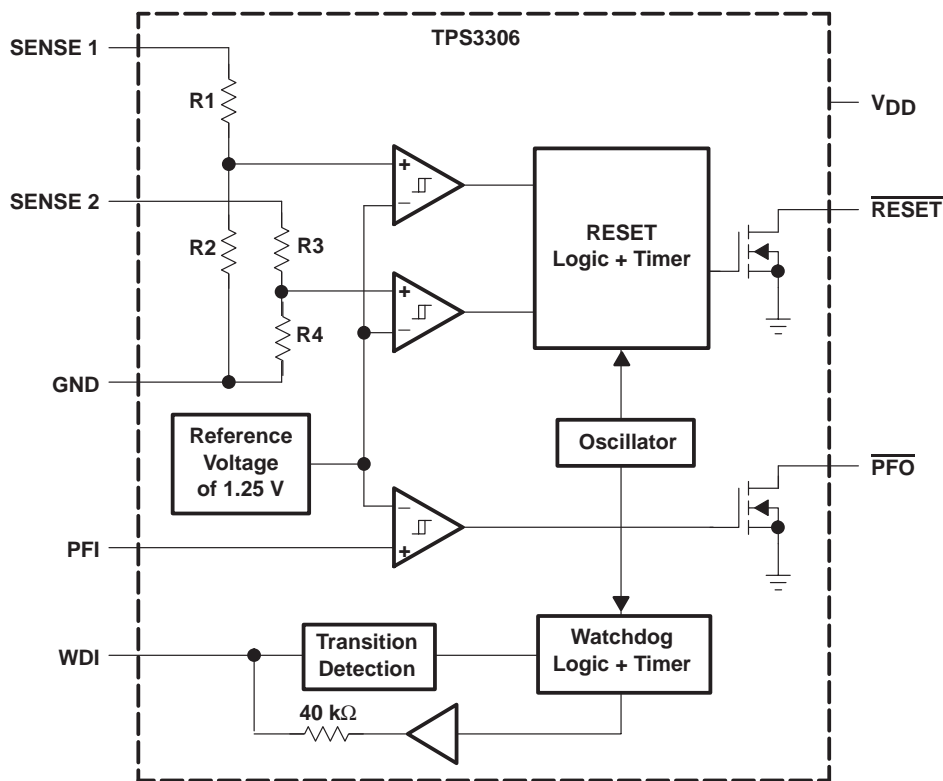
SGLS241B – MARCH 2004 – REVISED APRIL 2008

FUNCTION/TRUTH TABLES

| SENSE1 > V _{IT1} | SENSE2 > V _{IT2} | $\overline{\text{RESET}}$ |
|---------------------------|---------------------------|---------------------------|
| 0 | 0 | L |
| 0 | 1 | L |
| 1 | 0 | L |
| 1 | 1 | H |

| PFI > V _{IT} | $\overline{\text{PFO}}$ | TYPICAL DELAY |
|-----------------------|-------------------------|---------------|
| 0→1 | L→H | 0.5 μs |
| 1→0 | H→L | 0.5 μs |

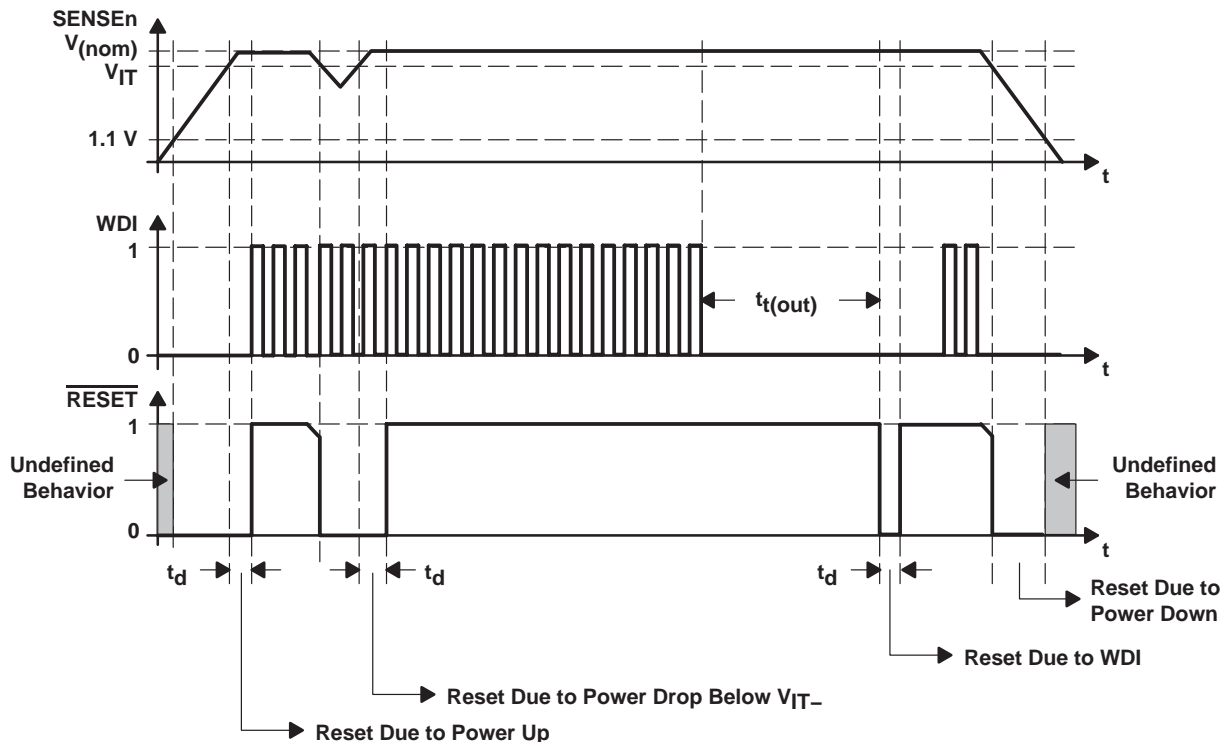
functional block diagram



TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

timing diagram



Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|--|
| GND | 4 | I | Ground |
| PFI | 3 | I | Power-fail comparator input |
| PFO | 6 | O | Power-fail comparator output, open drain |
| RESET | 5 | O | Active-low reset output, open drain |
| SENSE1 | 1 | I | Sense voltage 1 |
| SENSE2 | 2 | I | Sense voltage 2 |
| WDI | 7 | I | Watchdog timer input |
| VDD | 8 | I | Supply voltage |

detailed description

watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to typically toggle the watchdog input (WDI) within 0.8 s to avoid a time-out occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high-impedance driver, the watchdog is disabled and is retriggered internally.



saving current while using the watchdog

WDI is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If, instead, WDI is externally driven high for the majority of the time-out period, a current of $5\text{ V}/40\text{ k}\Omega \approx 125\text{ }\mu\text{A}$ can flow into WDI.

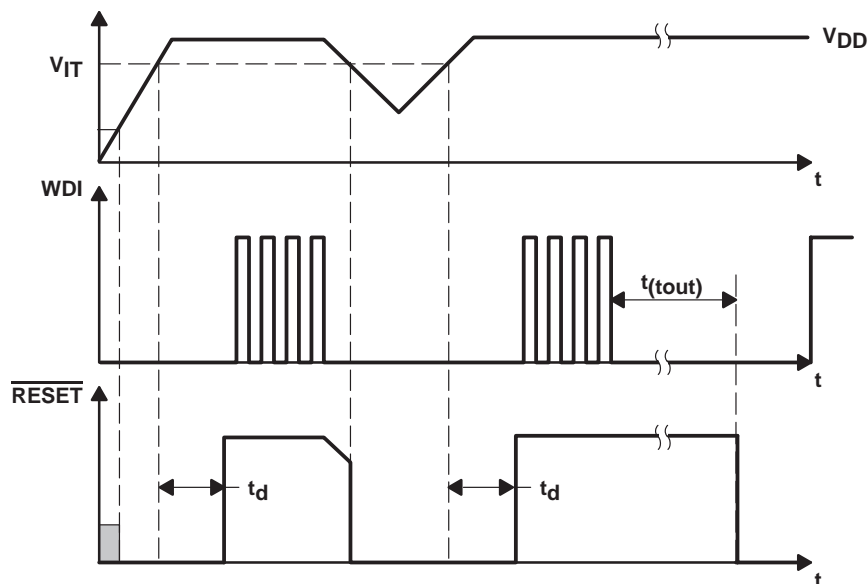
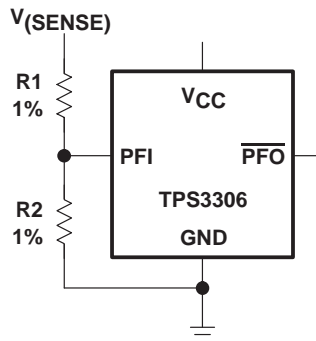


Figure 1. Watchdog Timing

power-fail comparator (PFI and PFO)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.25 V. If the input voltage falls below the power-fail threshold (V_{PFI}) of 1.25 V (typ), the power-fail output (\overline{PFO}) goes low. If \overline{PFO} goes above 1.25 V plus about 10-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above 1.25 V. The sum of both resistors should be approximately 1 M Ω , to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave \overline{PFO} unconnected.

$$V_{PFI,trip} = 1.25\text{ V} \times \frac{R_1 + R_2}{R_2}$$



TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage (see Note1): V_{DD} | 7 V |
| All other pins | -0.3 V to 7 V |
| Maximum low output current, I_{OL} | 5 mA |
| Maximum high output current, I_{OH} | -5 mA |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) | ± 20 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | -40°C to 125°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Soldering temperature | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than $t = 1000$ h continuously.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |

recommended operating conditions at specified temperature range

| | MIN | MAX | UNIT |
|---|---------------------|-------------------------------|------|
| Supply voltage, V_{DD} | 2.7 | 6 | V |
| Input voltage at WDI and PFI, V_I | 0 | $V_{DD} + 0.3$ | V |
| Input voltage at SENSE1 and SENSE2, V_I | 0 | $(V_{DD} + 0.3)V_{IT}/1.25$ V | V |
| High-level input voltage at WDI, V_{IH} | $0.7 \times V_{DD}$ | | V |
| Low-level input voltage at WDI, V_{IL} | | $0.3 \times V_{DD}$ | V |
| Operating free-air temperature range, T_A | -40 | 125 | °C |



TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------------------------|---|---|---|--------------------------|------|------|----|
| V _{OL} | Low-level output voltage | V _{DD} = 2.7 V to 6 V, I _{OL} = 20 μA | | | 0.2 | V | |
| | | V _{DD} = 3.3 V, I _{OL} = 2 mA | | | 0.4 | | |
| | | V _{DD} = 6 V, I _{OL} = 3 mA | | | 0.4 | | |
| Power-up reset voltage (see Note 2) | | V _{DD} ≥ 1.1 V, I _{OL} = 20 μA | | | 0.4 | V | |
| V _{IT} | Negative-going input threshold voltage (see Note 3) | V _{DD} = 2.7 V to 6 V, T _A = -40°C to 125°C | VSENSE1, VSENSE2 | 1.35 | 1.4 | 1.44 | V |
| | | | | 1.62 | 1.68 | 1.74 | |
| | | | | 1.79 | 1.85 | 1.91 | |
| | | | | 2.18 | 2.25 | 2.34 | |
| | | | | 2.84 | 2.93 | 3.04 | |
| | | | | 4.44 | 4.55 | 4.68 | |
| | PFI | 1.2 | 1.25 | 1.3 | | | |
| V _{hys} | Hysteresis | V _{IT} = 1.25 V | PFI | | 10 | mV | |
| | | | VSENSEn | V _{IT} = 1.4 V | | | 15 |
| | | | | V _{IT} = 1.68 V | | | 15 |
| | | | | V _{IT} = 1.86 V | | | 20 |
| | | | | V _{IT} = 2.25 V | | | 20 |
| | | | | V _{IT} = 2.93 V | | | 30 |
| | | | | V _{IT} = 4.55 V | | | 40 |
| I _{H(AV)} | Average high-level input current | WDI | WDI = V _{DD} = 6 V, Time average (dc = 88%) | | 100 | 150 | μA |
| I _{L(AV)} | Average low-level input current | WDI | WDI = 0 V, V _{DD} = 6 V, Time average (dc = 12%) | | -15 | -20 | μA |
| I _H | High-level input current | WDI | WDI = V _{DD} = 6 V | | 120 | 170 | μA |
| | | SENSE1 | VSENSE1 = V _{DD} = 6 V | | 5 | 10 | |
| | | SENSE2 | VSENSE2 = V _{DD} = 6 V | | 6 | 10 | |
| I _L | Low-level input current | WDI | WDI = 0 V, V _{DD} = 6 V | | -120 | -170 | μA |
| I _I | Input current | PFI | V _{DD} = 6 V, 0 V ≤ V _I ≤ V _{DD} | | -30 | 30 | nA |
| I _{DD} | Supply current | | | | 15 | 40 | μA |
| C _i | Input capacitance | | V _I = 0 V to V _{DD} | | 10 | | pF |

NOTES: 2. The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

timing requirements at V_{DD} = 2.7 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------|--------|---|-----|-----|------|
| t _w | SENSEn | VSENSEnL = V _{IT} - 0.2 V, VSENSEnH = V _{IT} + 0.2 V | 6 | | μs |
| | WDI | V _{IH} = 0.7 × V _{DD} , V _{IL} = 0.3 × V _{DD} | 100 | | ns |



TPS3306-15-Q1, TPS3306-18-Q1, TPS3306-20-Q1, TPS3306-25-Q1, TPS3306-33-Q1 DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER FAIL

SGLS241B – MARCH 2004 – REVISED APRIL 2008

switching characteristics at $V_{DD} = 2.7\text{ V to }6\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------|---------------------------|--|-----|-----|-----|---------------|
| $t_{t(out)}$ Watchdog time-out | | | $V_{I(SENSEn)} \geq V_{IT} + 0.2\text{ V}$, See timing diagram | 0.5 | 0.8 | 1.2 | s |
| t_d Delay time | | | $V_{I(SENSEn)} \geq V_{IT} + 0.2\text{ V}$, See timing diagram | 70 | 100 | 140 | ms |
| t_{PHL} Propagation (delay) time, high- to low-level output | SENSEn | $\overline{\text{RESET}}$ | $V_{IH} = V_{IT} + 0.2\text{ V}$, $V_{IL} = V_{IT} - 0.2\text{ V}$ | | 1 | 5 | μs |
| t_{PHL} Propagation (delay) time, high- to low-level output | PFI | $\overline{\text{PFO}}$ | | | 0.5 | 1 | μs |
| t_{PLH} Propagation (delay) time, low- to high-level output | | | | | | | |

TYPICAL CHARACTERISTICS

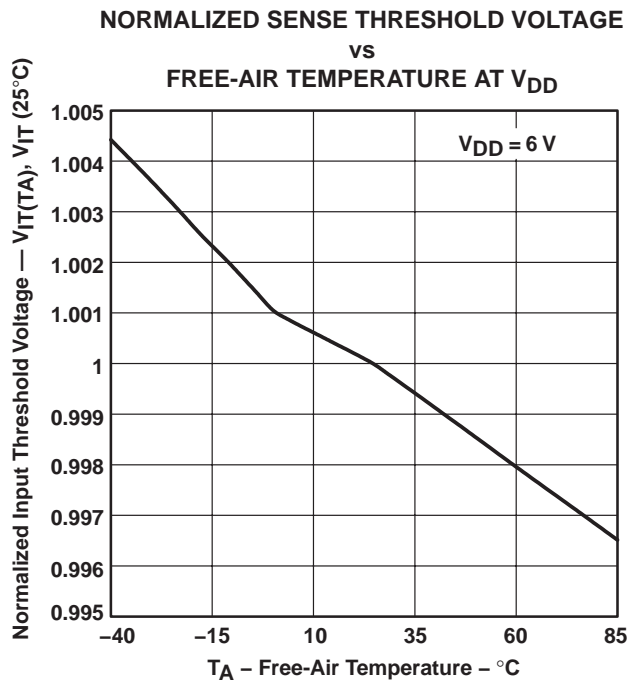


Figure 2

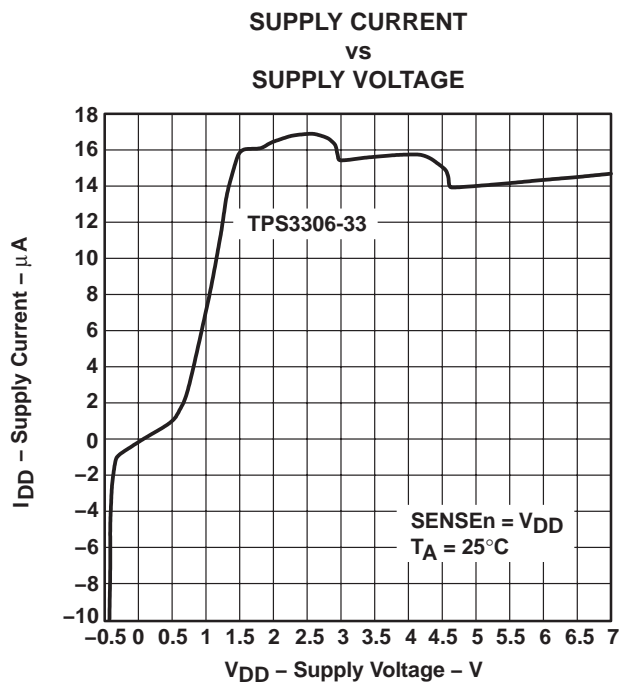


Figure 3

TYPICAL CHARACTERISTICS

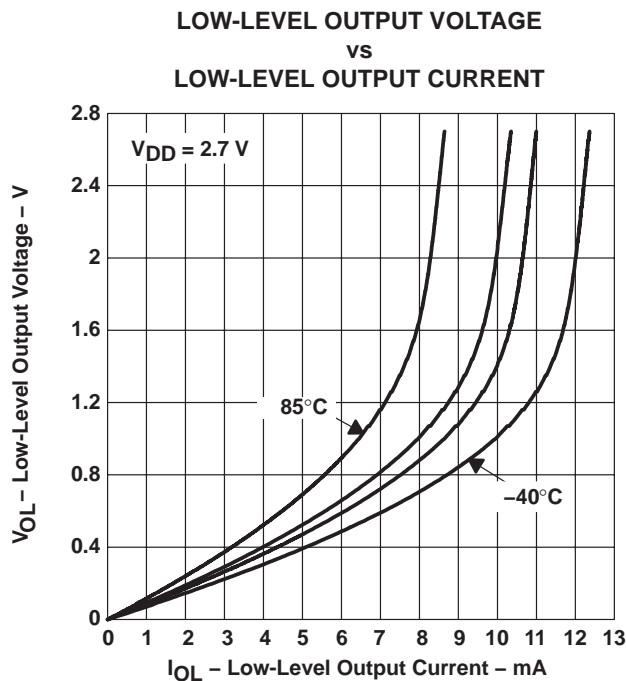


Figure 4

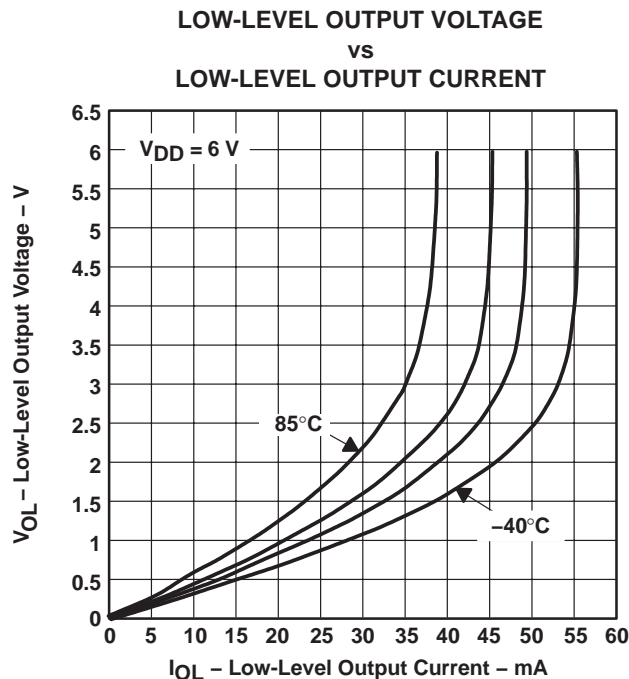


Figure 5

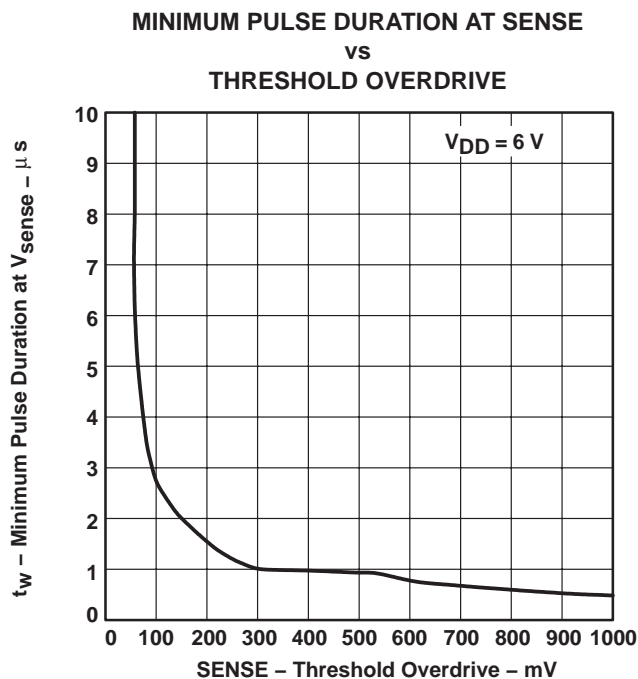


Figure 6

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TPS3306-15QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 615Q1 | Samples |
| TPS3306-15QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 615Q1 | Samples |
| TPS3306-18QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 618Q1 | Samples |
| TPS3306-18QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 618Q1 | Samples |
| TPS3306-20QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 620Q1 | Samples |
| TPS3306-25QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 625Q1 | Samples |
| TPS3306-33QDRG4Q1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 633Q1 | Samples |
| TPS3306-33QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 633Q1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3306-Q1 :

- Catalog: [TPS3306](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3306-15QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-18QDRG4Q1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-18QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-20QDRG4Q1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-25QDRG4Q1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-33QDRG4Q1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3306-33QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS3306-15QDRQ1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-18QDRG4Q1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-18QDRQ1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-20QDRG4Q1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-25QDRG4Q1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-33QDRG4Q1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS3306-33QDRQ1 | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated