

# TPS51604 Synchronous Buck FET Driver for High-Frequency CPU Core Power

## 1 Features

- Reduced Dead-Time Drive Circuit for Optimized CCM
- Automatic Zero Crossing Detection for Optimized DCM Efficiency
- Multiple Low-Power Modes for Optimized Light-Load Efficiency
- Optimized Signal Path Delays for High-Frequency Operation
- Integrated BST Switch Drive Strength Optimized for Ultrabook FETs
- Optimized for 5-V FET Drive
- Conversion Input Voltage Range ( $V_{IN}$ ): 4.5 to 28 V
- 2-mm x 2-mm, 8-Pin, WSON Thermal Pad Package

## 2 Applications

- Tablets Using High-Frequency CPUs With the Following Power Input:
  - Adapter
  - Battery
  - NVDC
  - 5-V or 12-V Rails

## 3 Description

The TPS51604 drivers are optimized for high-frequency CPU  $V_{CORE}$  applications. Advanced features such as reduced dead-time drive and auto zero crossing are used to optimize efficiency over the entire load range.

The  $\overline{SKIP}$  pin provides the option of CCM operation to support controlled management of the output voltage. In addition, the TPS51604 supports two low-power modes. With the PWM input in tri-state, quiescent current is reduced to 130  $\mu A$ , with immediate response. When  $\overline{SKIP}$  is held at tri-state, the current is reduced to 8  $\mu A$  (typically 20  $\mu s$  is required to resume switching). Paired with the appropriate TI controller, the drivers deliver an exceptionally high performance power supply system.

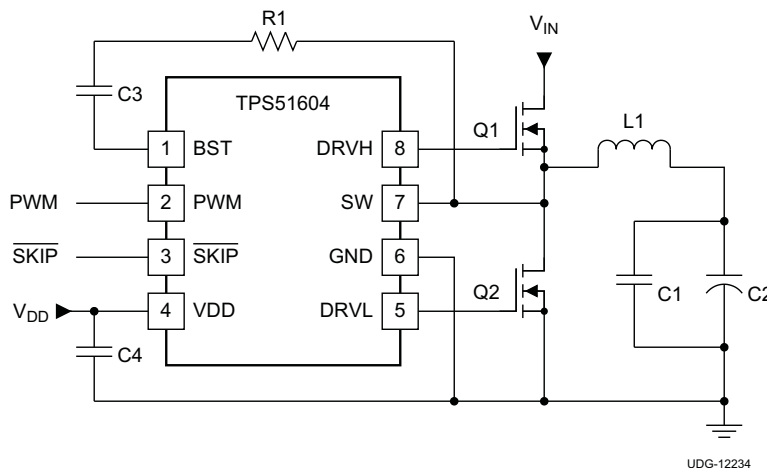
The TPS51604 device is packaged in a space saving, thermally-enhanced 8-pin, 2-mm x 2-mm WSON package and operates from  $-40^{\circ}C$  to  $105^{\circ}C$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51604	WSON (8)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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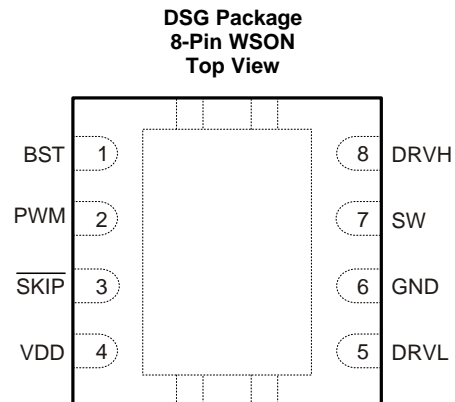
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2013) to Revision B	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
BST	1	I	High-side N-channel FET bootstrap voltage input; power supply for high-side driver
DRVH	8	O	High-side N-channel gate drive output
DRVL	5	O	Synchronous low-side N-channel gate drive output
GND	6	G	Synchronous low-side N-channel gate drive return and device reference
PWM	2	I	PWM input. A tri-state voltage on this pin turns off both the high-side (DRVH) and low-side drivers (DRVL)
$\overline{\text{SKIP}}$	3	I	When $\overline{\text{SKIP}}$ is LO, the zero crossing comparator is active. The power chain enters discontinuous conduction mode when the inductor current reaches zero. When $\overline{\text{SKIP}}$ is HI, the zero crossing comparator is disabled, and the driver outputs follow the PWM input. A tri-state voltage on $\overline{\text{SKIP}}$ puts the driver into a very-low power state.
SW	7	I/O	High-side N-channel gate drive return. Also, zero-crossing sense input
VDD	4	I	5-V power supply input; decouple to GND with a ceramic capacitor with a value of 1 $\mu\text{F}$ or greater
Thermal Pad		G	Tie to system GND plane with multiple vias

(1) I = Input, O = Output, G = Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1) (2)</sup>

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD	−0.3	6	V
	PWM, $\overline{\text{SKIP}}$	−0.3	6	
Output voltage	BST	−0.3	35	V
	BST (transient <20 ns)	−0.3	38	
	BST to SW; DRVH to SW	−0.3	6	
	SW	−2	30	
	DRVH, SW (transient <20 ns)	−5	38	
	DRVL	−0.3	6	
Ground pins	GND to PAD	−0.3	0.3	V
Operating junction temperature, $T_J$		−40	125	°C
Storage temperature range, $T_{\text{stg}}$		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VDD	4.5	5	5.5	V
	PWM, $\overline{\text{SKIP}}$	−0.1		5.5	
Output voltage	BST	−0.1		34	V
	BST to SW; DRVH to SW	−0.1		5.5	
	SW	−1		28	
	DRVL	−0.1		5.5	
Ground pins	GND to PAD	−0.1		0.1	V
Operating junction temperature, $T_J$		−40		105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS51604	UNIT
		WSN (DSG)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.1	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	74.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	2.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	34.9	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	11.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

These specifications apply for  $-40^{\circ}\text{C} \leq T_J \leq 105^{\circ}\text{C}$ , and  $V_{\text{VDD}} = 5\text{ V}$  unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT SUPPLY						
I <sub>CC</sub>	Supply current (operating)	$\overline{V_{SKIP}} = V_{VDD}$ or $\overline{V_{SKIP}} = 0\text{ V}$ , PWM = High		160	600	μA
		$\overline{V_{SKIP}} = V_{VDD}$ or $\overline{V_{SKIP}} = 0\text{ V}$ , PWM = Low		250		
		$\overline{V_{SKIP}} = V_{VDD}$ or $\overline{V_{SKIP}} = 0\text{ V}$ , PWM = Float		130		
		$\overline{V_{SKIP}} = \text{Float}$		8		
VDD UNDERVOLTAGE LOCKOUT (UVLO)						
V <sub>UVLO</sub>	UVLO threshold	Rising threshold			4.15	V
		Falling threshold		3.7		
V <sub>UVHYS</sub>	UVLO hysteresis			0.2		V
PWM AND $\overline{SKIP}$ I/O SPECIFICATIONS						
R <sub>I</sub>	Input impedance	Pullup to VDD		1.7		MΩ
		Pulldown (to GND)		800		kΩ
V <sub>IL</sub>	Low-level input voltage				0.6	V
V <sub>IH</sub>	High-level input voltage		2.65			V
V <sub>IHH</sub>	Hysteresis			0.2		V
V <sub>TS</sub>	Tri-state voltage		1.3		2.0	V
t <sub>THOLD(off1)</sub>	Tri-state activation time (falling) PWM			60		ns
t <sub>THOLD(off2)</sub>	Tri-state activation time (rising) PWM			60		ns
t <sub>TSKF</sub>	Tri-state activation time (falling) $\overline{SKIP}$			1		μs
t <sub>TSKR</sub>	Tri-state activation time (rising) $\overline{SKIP}$			1		μs
t <sub>3RD(PWM)</sub>	Tri-state exit time PWM				100	ns
t <sub>3RD(<math>\overline{SKIP}</math>)</sub>	Tri-state exit time $\overline{SKIP}$				50	μs
HIGH-SIDE GATE DRIVER (DRVH)						
t <sub>R(DRVH)</sub>	Rise time	DRVH rising, C <sub>DRVH</sub> = 3.3 nF; 20% to 80%		30		ns
t <sub>RPD(DRVH)</sub>	Rise time propogation delay	C <sub>DRVH</sub> = 3.3 nF		40		ns
R <sub>SRC</sub>	Source resistance	Source resistance, (V <sub>BST</sub> – V <sub>SW</sub> ) = 5 V, high state, (V <sub>BST</sub> – V <sub>DRVH</sub> ) = 0.1 V		4	8	Ω
t <sub>F(DRVH)</sub>	Fall time	DRVH falling, C <sub>DRVH</sub> = 3.3 nF		8		ns
t <sub>FPD(DRVH)</sub>	Fall-time propagation delay	C <sub>DRVH</sub> = 3.3 nF		25		ns
R <sub>SNK</sub>	Sink resistance	Sink resistance, (V <sub>BST</sub> – V <sub>SW</sub> ) forced to 5 V, low state (V <sub>DRVH</sub> – V <sub>SW</sub> ) = 0.1 V		0.5	1.6	Ω
R <sub>DRVH</sub>	DRVH to SW resistance <sup>(1)</sup>			100		kΩ

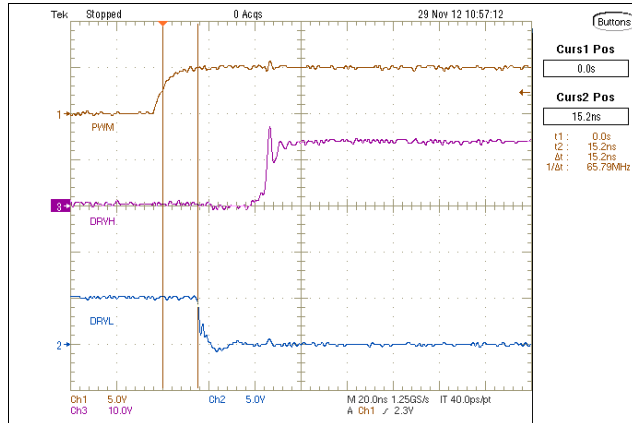
(1) Specified by design. Not production tested.

## Electrical Characteristics (continued)

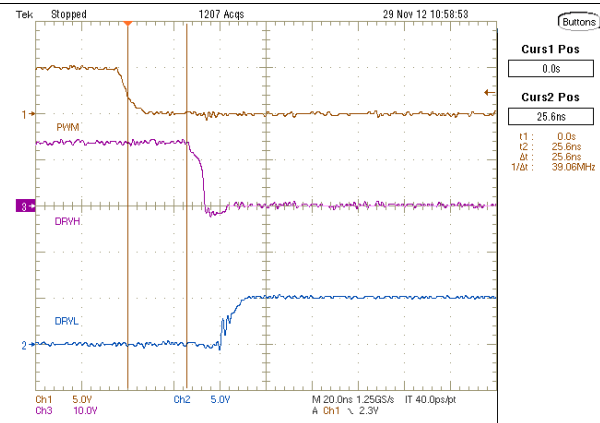
These specifications apply for  $-40^{\circ}\text{C} \leq T_J \leq 105^{\circ}\text{C}$ , and  $V_{\text{VDD}} = 5\text{ V}$  unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOW-SIDE GATE DRIVER (DRV_L)</b>						
$t_{\text{R(DRV_L)}}$	Rise time	DRV_L rising, $C_{\text{DRV_L}} = 3.3\text{ nF}$ ; 20% to 80%		15		ns
$t_{\text{RPD(DRV_L)}}$	Rise time propagation delay	$C_{\text{DRV_L}} = 3.3\text{ nF}$		35		ns
$R_{\text{SRC}}$	Source resistance	Source resistance, $(V_{\text{VDD}} - \text{GND}) = 5\text{ V}$ , high state, $(V_{\text{VDD}} - V_{\text{DRV_L}}) = 0.1\text{ V}$		1.5	3	$\Omega$
$t_{\text{F(DRV_L)}}$	Fall time	DRV_L falling, $C_{\text{DRV_L}} = 3.3\text{ nF}$		10		ns
$t_{\text{FPD(DRV_L)}}$	Fall-time propagation delay	$C_{\text{DRV_L}} = 3.3\text{ nF}$		15		ns
$R_{\text{SNK}}$	Sink resistance	Sink resistance, $(V_{\text{VDD}} - \text{GND}) = 5\text{ V}$ , low state, $(V_{\text{DRV_L}} - \text{GND}) = 0.1\text{ V}$		0.4	1.6	$\Omega$
$R_{\text{DRV_L}}$	DRV_L to GND resistance <sup>(1)</sup>			100		k $\Omega$
<b>GATE DRIVER DEAD-TIME</b>						
$t_{\text{R(DT)}}$	Rising edge		0	20	35	ns
$t_{\text{F(DT)}}$	Falling edge		0	10	25	ns
<b>ZERO CROSSING COMPARATOR</b>						
$V_{\text{ZX}}$	Zero crossing offset	SW voltage rising	-2.25	0	2.00	mV
<b>BOOTSTRAP SWITCH</b>						
$V_{\text{FBST}}$	Forward voltage	$I_{\text{F}} = 10\text{ mA}$		120	240	mV
$I_{\text{RLEAK}}$	Reverse leakage	$(V_{\text{BST}} - V_{\text{VDD}}) = 25\text{ V}$			2	$\mu\text{A}$
$R_{\text{DS(on)}}$	On-resistance			12	24	$\Omega$

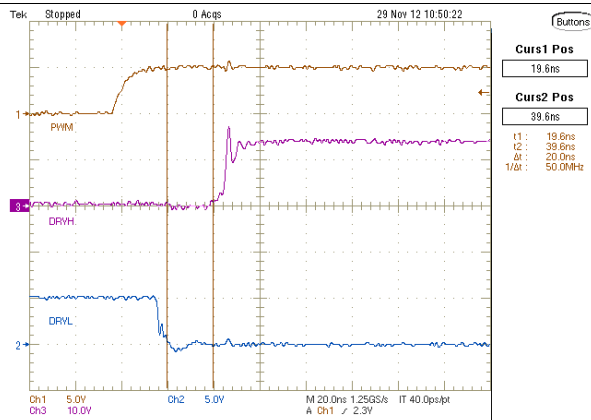
## 6.6 Typical Characteristics



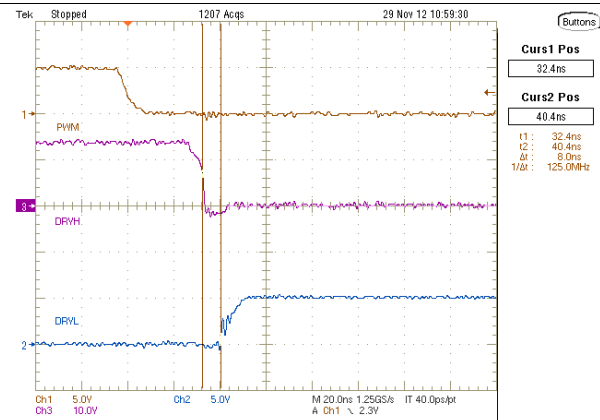
**Figure 1. PWM High to DRVL Low**



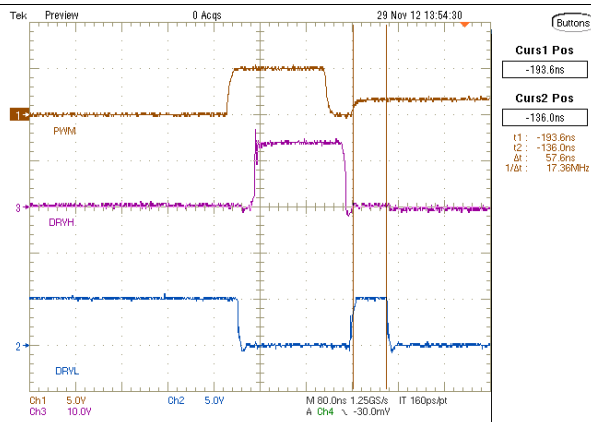
**Figure 2. PWM Low to DRVH Low**



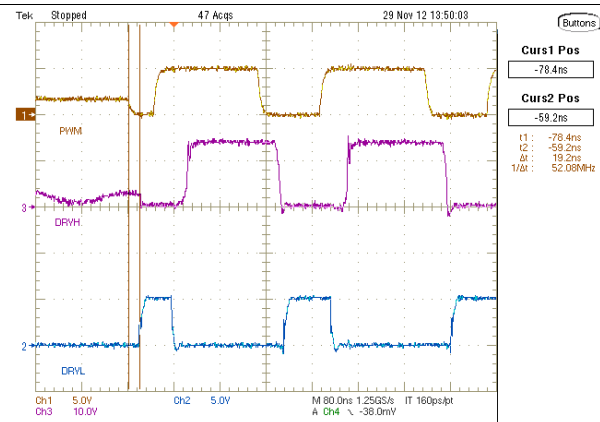
**Figure 3. DRVL Low to DRVH High**



**Figure 4. DRVH Low to DRVL High**



**Figure 5. PWM Low to Tri-State**



**Figure 6. PWM Tri-State to Low**

## Typical Characteristics (continued)

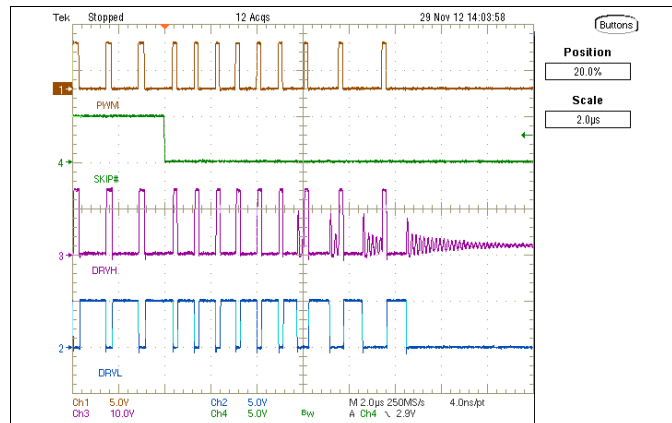


Figure 7. SKIP Mode Entry

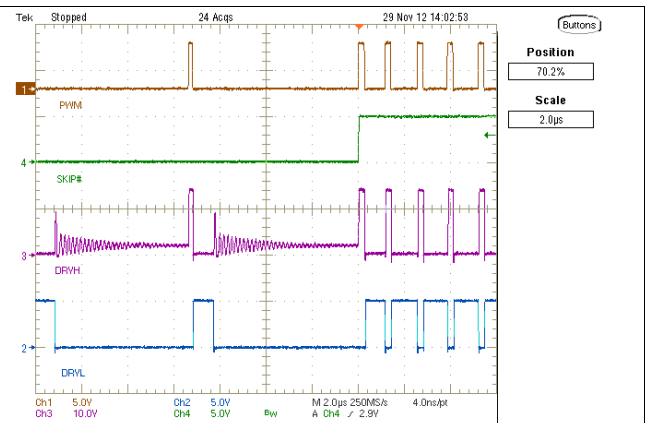


Figure 8. SKIP Mode Exit

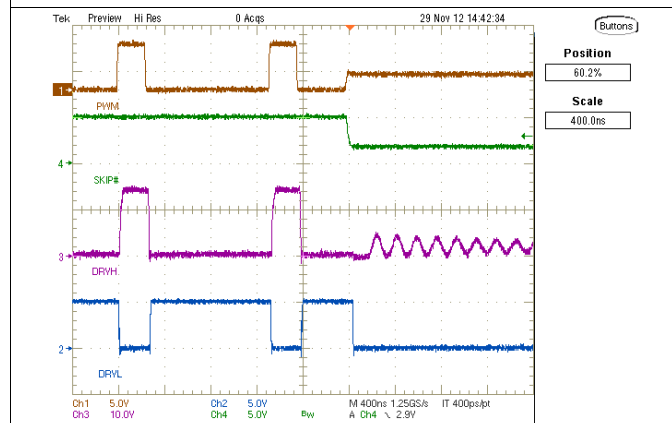


Figure 9. Very-Low-Power Mode Entry

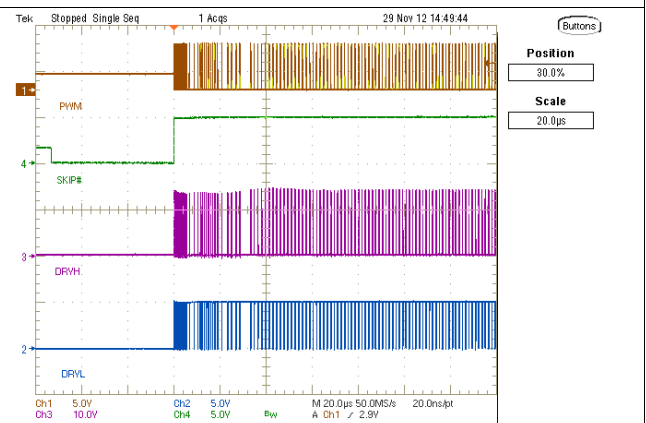
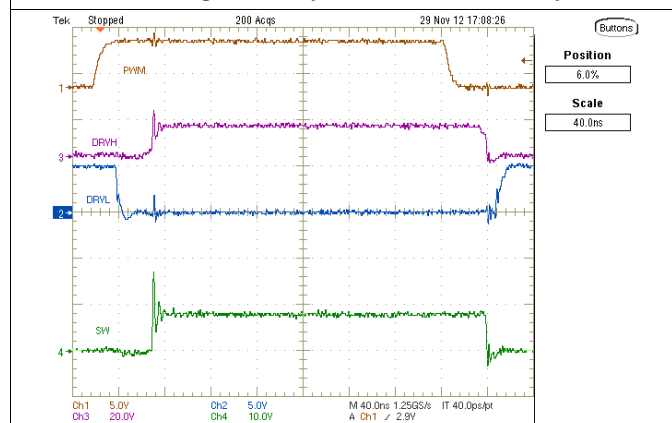
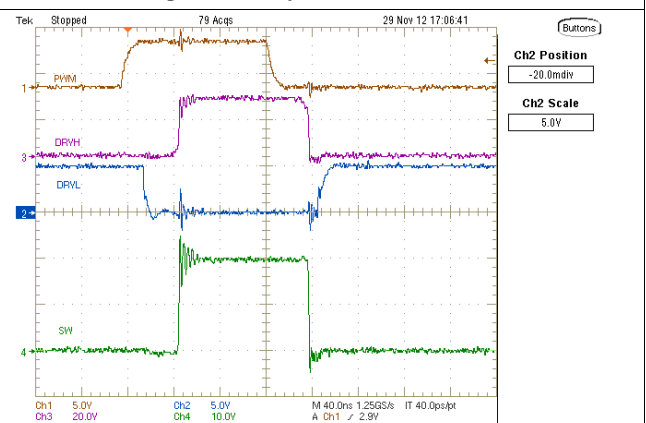


Figure 10. Very-Low-Power Mode Exit



$V_{IN} = 8V$

Figure 11. SW Node-Ringing



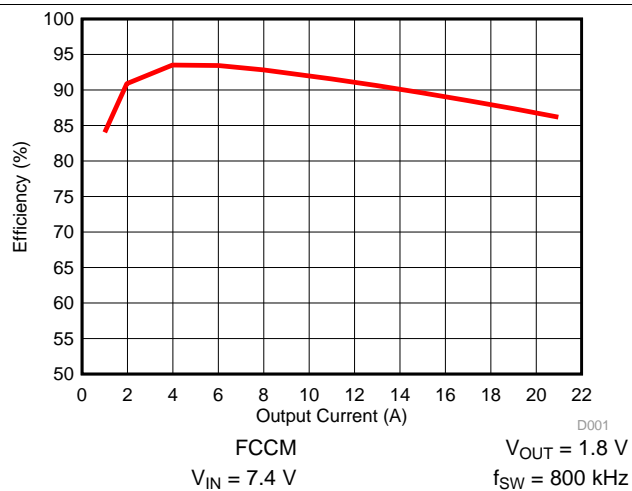
$V_{IN} = 20V$

Figure 12. SW Node-Ringing

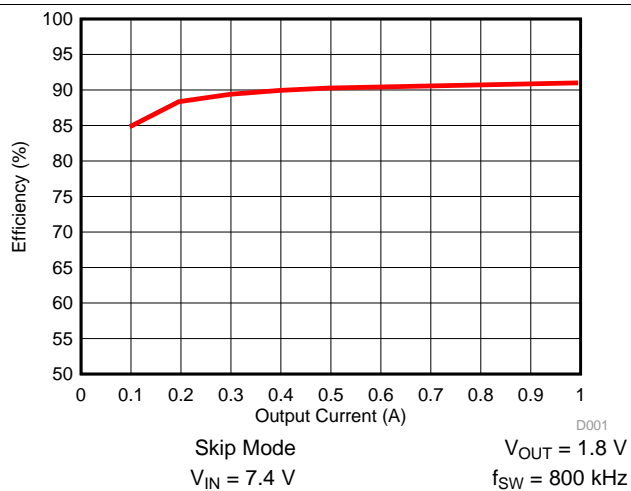


## 6.7 Typical Power Block MOSFET Characteristics

Power block MOSFET: CSD87330, Inductor: 0.22  $\mu$ F, 1.1-m $\Omega$  DCR



**Figure 13. Efficiency vs Output Current, FCCM**



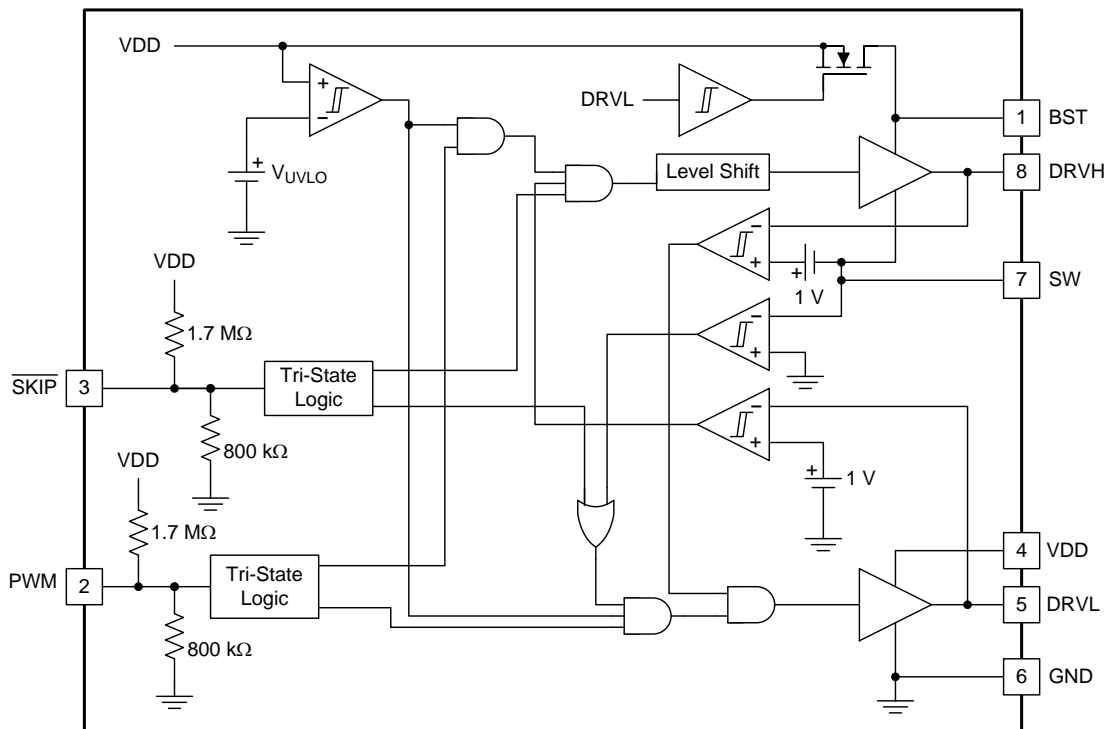
**Figure 14. Efficiency vs Output Current, SKIP Mode**

## 7 Detailed Description

### 7.1 Overview

The TPS51604 device is a synchronous-buck MOSFET driver designed to drive both high-side and low-side MOSFETs. It allows high-frequency operation with current driving capability matched to the application. The integrated boost switch is internal. The TPS51604 device employs dead-time reduction control and shoot-through protection, which helps avoid simultaneous conduction of high-side and low-side MOSFETs. Also, the drivers improve light-load efficiency with integrated DCM-mode operation using adaptive crossing detection. Typical applications yield a steady-state duty cycle of 60% or less. For high steady-state duty cycle applications, including a small external Schottky diode may help to ensure sufficient charging of the bootstrap capacitor.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

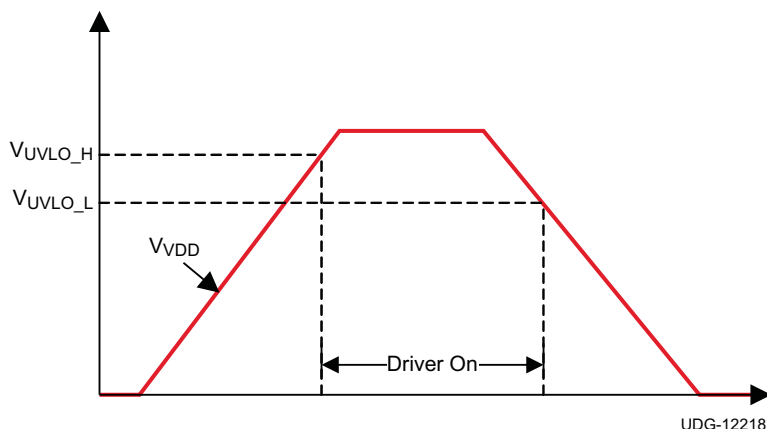
#### 7.3.1 UVLO Protection

The UVLO comparator evaluates the VDD voltage level. As  $V_{VDD}$  rises, both DRVH and DRVL hold actively low at all times until  $V_{VDD}$  reaches the higher UVLO threshold ( $V_{UVLO\_H}$ ). Then, the driver becomes operational and responds to PWM and SKIP commands. If VDD falls below the lower UVLO threshold ( $V_{UVLO\_L} = V_{UVLO\_H} - \text{Hysteresis}$ ), the device disables the driver and drives the outputs of DRVH and DRVL actively low. [Figure 15](#) shows this function.

#### CAUTION

Do not start the driver in the very low power mode ( $\overline{\text{SKIP}}$  = Tri-state).

## Feature Description (continued)



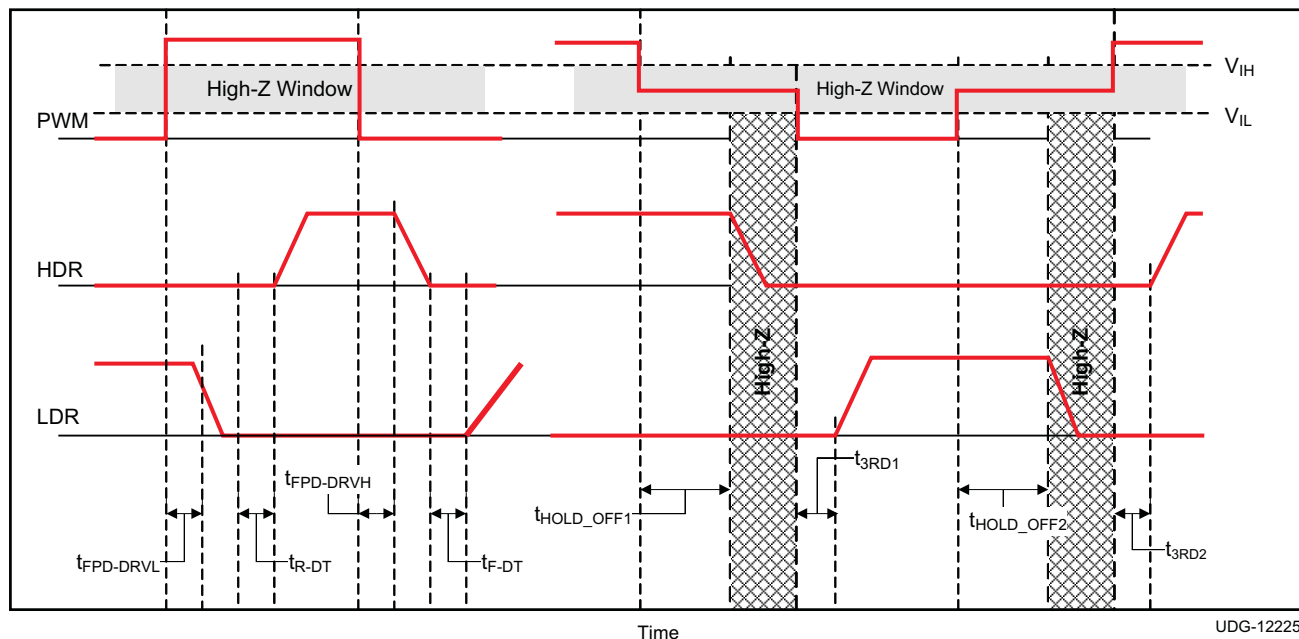
**Figure 15. UVLO Operation**

### 7.3.2 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of a tri-state condition follows the timing diagram outlined in Figure 16.

When VDD reaches the UVLO\_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined as the PWM voltage range between PWM logic high ( $V_{IH}$ ) and logic low ( $V_{IL}$ ) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3-V (typical) and 5-V (typical) PWM drive signals.

When the PWM exits the tri-state condition, the driver enters CCM for a period of 4  $\mu$ s, regardless of the state of the SKIP pin. Typical operation requires this time period in order for the auto-zero comparator to resume.



**Figure 16. PWM Tri-State Timing Diagram**

## Feature Description (continued)

### 7.3.3 $\overline{\text{SKIP}}$ Pin

The  $\overline{\text{SKIP}}$  pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When  $\overline{\text{SKIP}}$  is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When  $\overline{\text{SKIP}}$  is high, the ZX comparator disables, and the converter enters FCCM mode. When the  $\overline{\text{SKIP}}$  pin is in a tri-state condition, typical operation forces the gate driver outputs low and the driver enters a very-low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When the  $\overline{\text{SKIP}}$  pin voltage is pulled either low or high, the driver wakes up and is able to accept PWM pulses in less than 50  $\mu\text{s}$ .

Table 1 shows the logic functions of UVLO, PWM,  $\overline{\text{SKIP}}$ , DRVH, and DRVL.

**Table 1. Logic Functions of the TPS51604**

UVLO	PWM	$\overline{\text{SKIP}}$	DRVL	DRVH	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High <sup>(1)</sup>	Low	DCM <sup>(1)</sup>
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	Low power
Inactive	—	Tri-state	Low	Low	Very-low power

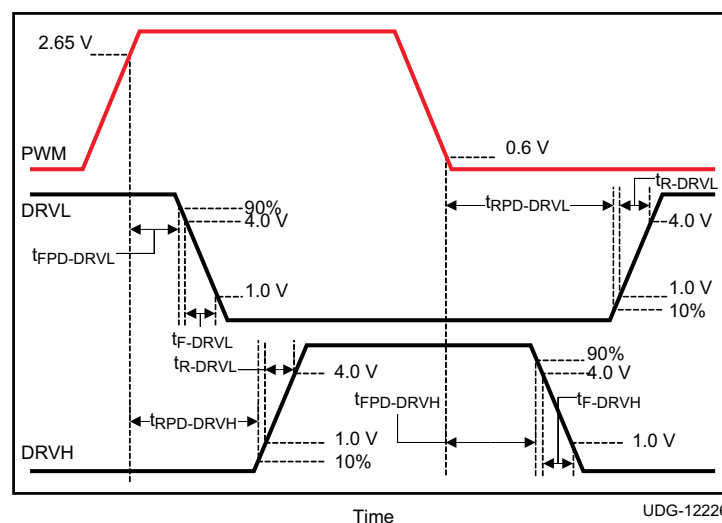
(1) Until zero crossing protection occurs.

#### 7.3.3.1 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

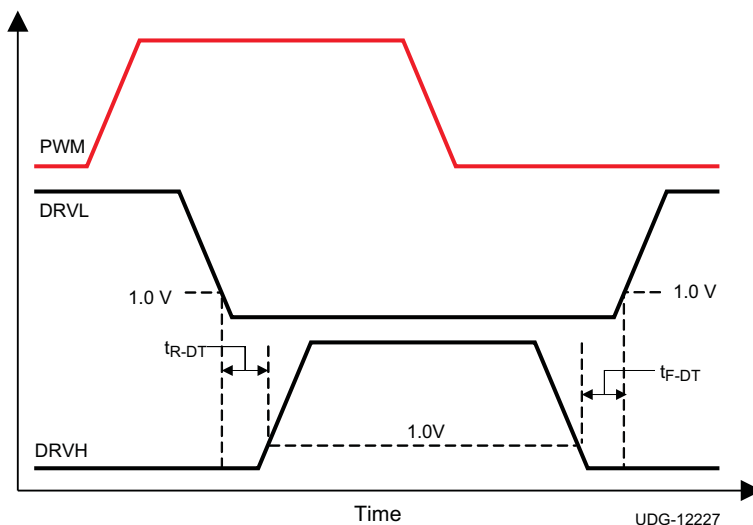
#### 7.3.4 Adaptive Dead-Time Control and Shoot-Through Protection

The driver utilizes an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and maintain high efficiency. When the PWM input voltage becomes high, the low-side MOSFET gate voltage begins to fall after a propagation delay. At the same time, DRVL voltage is sensed, and high-side driving voltage starts to increase after DRVL voltage is lower than a proper threshold.



**Figure 17. Rise and Fall Timing and Propagation Delay Definitions**

Typical operation manages to near zero the dead-time between the low-side gate turn-off to high-side gate voltage turn-on, and high-side gate turn-off to low-side gate turn-on, in order to avoid simultaneous conduction of both MOSFETs, as well as to reduce body diode conduction and recovery losses. This operation also reduces ringing on the leading edge of the SW waveform.



**Figure 18. Dead-Time Definitions**

### 7.3.5 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and BST pin is replaced by a FET, which is gated by the DRVL signal.

## 7.4 Device Functional Modes

The TPS51604 device operates in CCM mode when the  $\overline{\text{SKIP}}$  pin is high, and it enters DCM mode when the  $\overline{\text{SKIP}}$  pin is low. When both the  $\overline{\text{SKIP}}$  pin and the PWM pin are in a tri-state condition, it forces the gate driver outputs low and the driver enters a very-low-power state.

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The TPS51604 driver is optimized for high-frequency CPU  $V_{\text{CORE}}$  applications. Advanced features such reduced dead-time drive and Auto Zero Crossing are used to optimize efficiency over the entire load range.

### 8.2 Typical Application

[Figure 19](#) and [Figure 20](#) show a 2-phase design example where TPS51604 device works with the TPS51632 controller and the CSD87381 power block.

## Typical Application (continued)

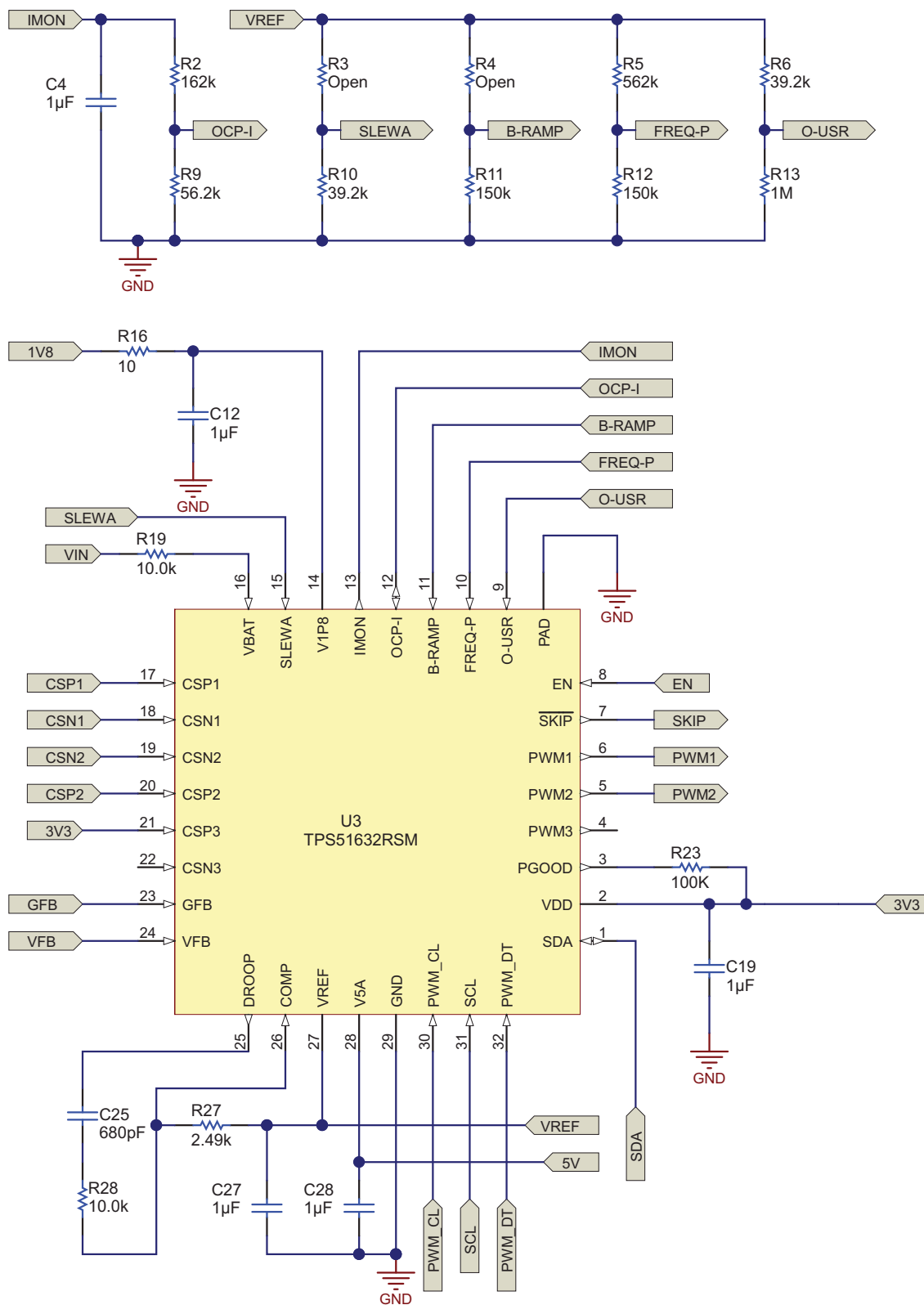
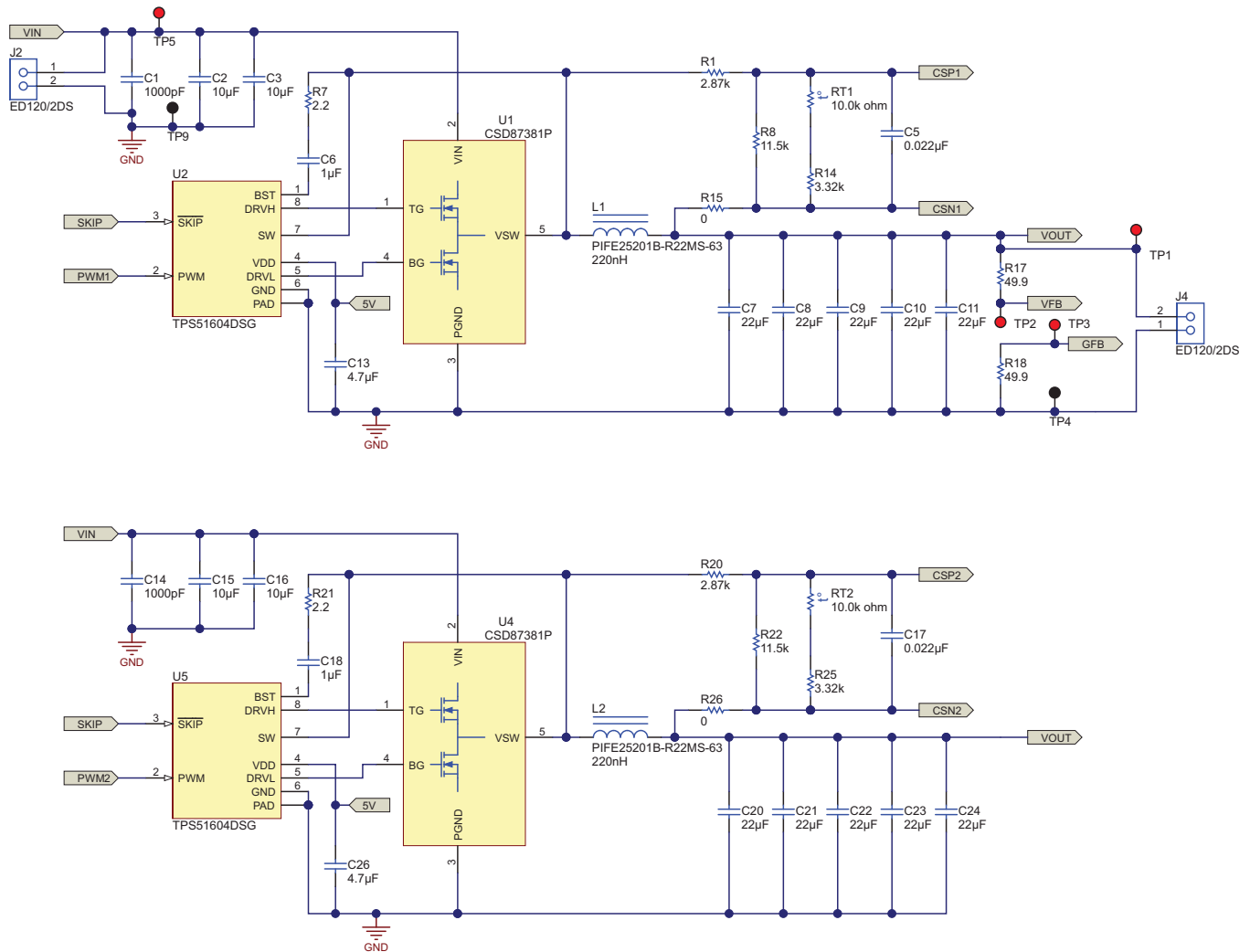


Figure 19. Controller Schematic

## Typical Application (continued)



**Figure 20. Driver, Power Block, and Output Stage Schematic**



## Typical Application (continued)

### 8.2.1 Design Requirements

The design example uses the input parameters summarized in [Table 2](#).

**Table 2. Design Requirements**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage		6	12	20	V
$V_{OUT}$	Output voltage			1.2		V
$V_{P\_P}$	Output ripple voltage	$I_{OUT} = 12\text{ A}$		20		mV
$I_{OUT}$	Output current		0		12	A
$\eta$	Efficiency	$I_{OUT} = 12\text{ A}$ , $V_{IN} = 12\text{ V}$		80%		
$f_{SW}$	Switching frequency			1000		kHz

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Step 1: Select the Input (VDD) Capacitor

A 5-V power supply is suggested for VDD. Place a ceramic capacitor with a value of 1  $\mu\text{F}$  or greater between VDD and GND.

#### 8.2.2.2 Step 2: Select Boot Capacitor and Boot Resistor

The boot capacitor is the power supply for high-side driver. Place a ceramic capacitor with a value of 0.1  $\mu\text{F}$  or greater between the BST pin and the SW pin.

To reduce the voltage spike on switch node, use a boot resistor with a value of several Ohms in series with boot capacitor to slow the turn-on of high-side FET.

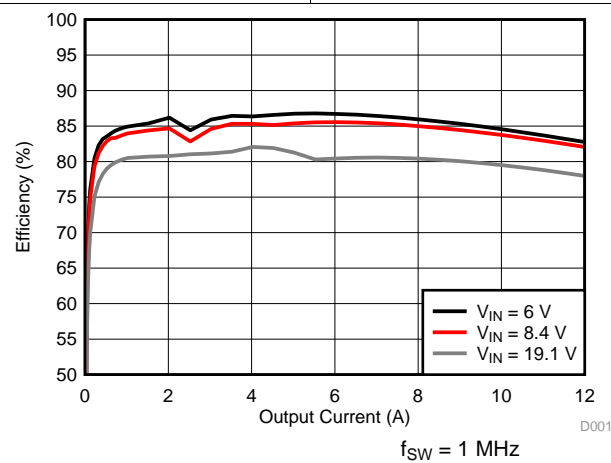
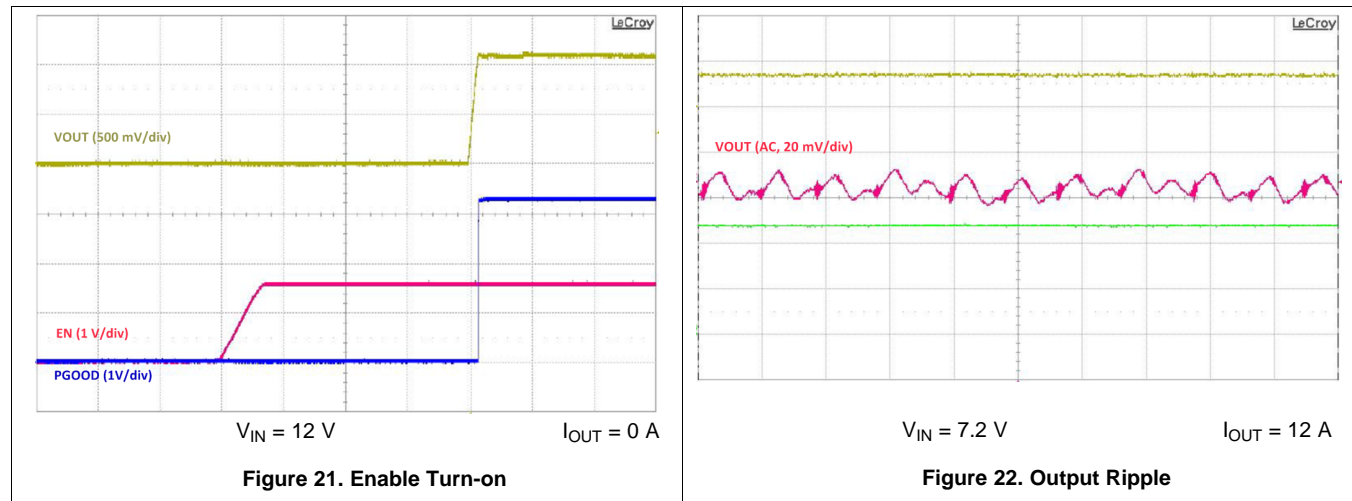
#### 8.2.2.3 Step 3: Establish Connection Between TPS51604 and Controller

Connect the PWM pin of the TPS51604 device to the PWM pin of the controller. The TRIP pins can be used for DCM mode or very-low-power state. Leave the TRIP pin floating if it is not in use.

#### 8.2.2.4 Step 4: Establish Connection Between TPS51604 and the Power Block

Connect the DRVH pin of the TPS51604 device to the gate of the high-side FET of the power block. Connect the DRVL pin of the TPS51604 device to the gate of the low-side FET of the power block. Connect the SW pins of the TPS51604 device to the switch node as required by the high-side driver for the power block.

## 8.2.3 Application Curves



**Figure 23. Efficiency vs. Load**

## 9 Power Supply Recommendations

The voltage range for the VDD pin is between 4.5 V and 5.5 V. A 5-V power supply is recommended for the VDD pin of the TPS51604 device.

## 10 Layout

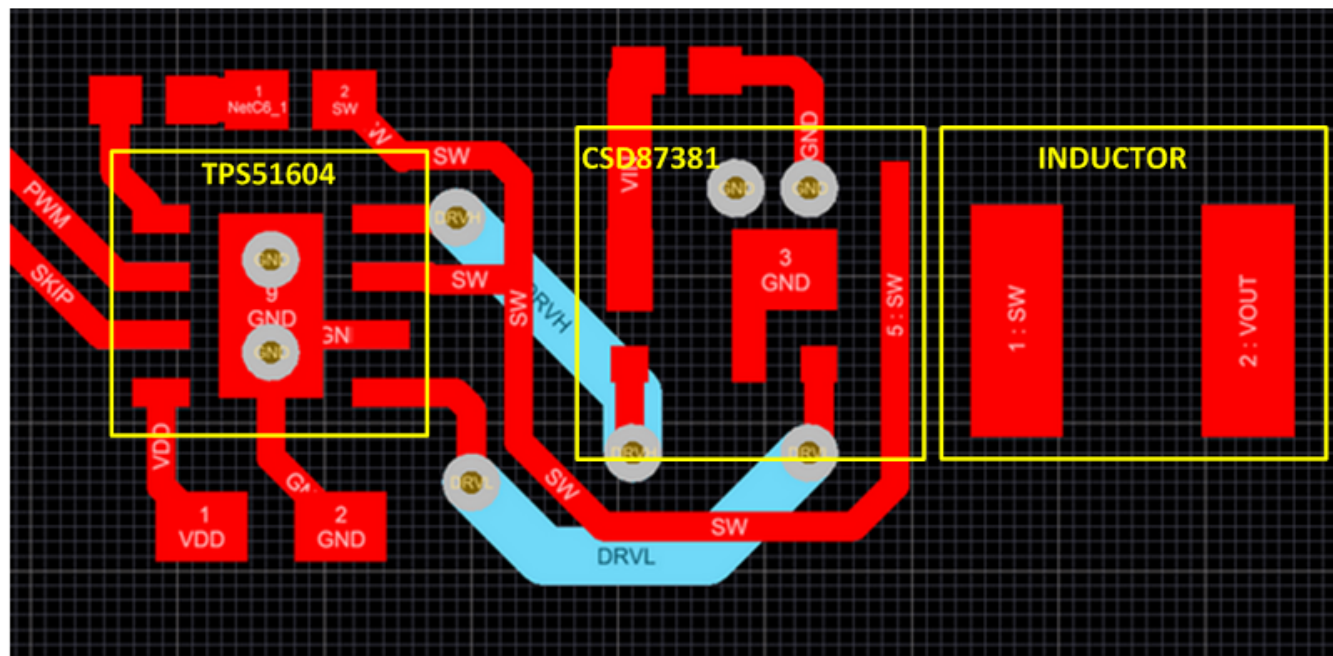
### 10.1 Layout Guidelines

To improve the switching characteristics and design efficiency, these layout rules must be considered:

- Locate the driver as close as possible to the MOSFETs.
- Locate the VDD and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET, but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the switch-node as for the GND.
- Use wide traces for DRVH and DRVL closely following the related SW and GND traces. A width of between 80 and 100 mils is preferable where possible.
- Place the bypass capacitors as close as possible to the driver.
- Avoid PWM and enable traces going close to the SW and pad where high dV/dT voltage can induce significant noise into the relatively high-impedance leads.

A poor layout can decrease the reliability of the entire system.

### 10.2 Layout Example



**Figure 24. Layout Recommendation**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

For the Power Stage Designer, go to [www.ti.com/tool/powerstage-designer](http://www.ti.com/tool/powerstage-designer).

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

- TPS51632 3-2-1 Phase D-Cap+™ Step-Down Driverless Controller for Tegra® CPUs [SLUSBM3](#)
- CSD87330 30-V Synchronous Buck NexFET™ Power Block [SLPS284](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

D-Cap+, NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS51604DSGR</a>	Active	Production	WSO (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604
TPS51604DSGR.A	Active	Production	WSO (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604
<a href="#">TPS51604DSGT</a>	Active	Production	WSO (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604
TPS51604DSGT.A	Active	Production	WSO (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604
TPS51604DSGTG4	Active	Production	WSO (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604
TPS51604DSGTG4.A	Active	Production	WSO (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF TPS51604 :**

- Automotive : [TPS51604-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51604DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51604DSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51604DSGTG4	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51604DSGR	WSN	DSG	8	3000	182.0	182.0	20.0
TPS51604DSGT	WSN	DSG	8	250	182.0	182.0	20.0
TPS51604DSGTG4	WSN	DSG	8	250	182.0	182.0	20.0



## GENERIC PACKAGE VIEW

**DSG 8**

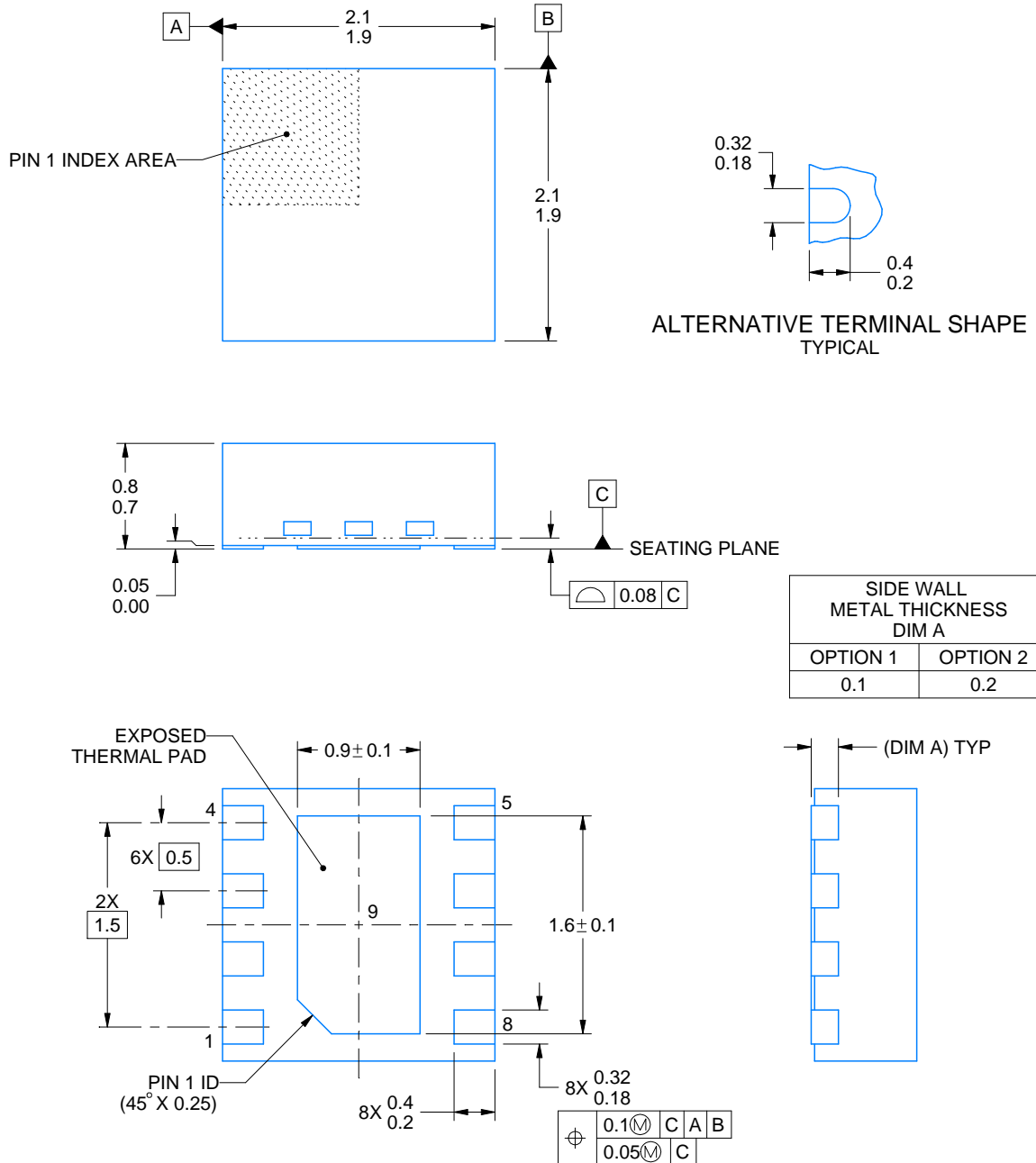
**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





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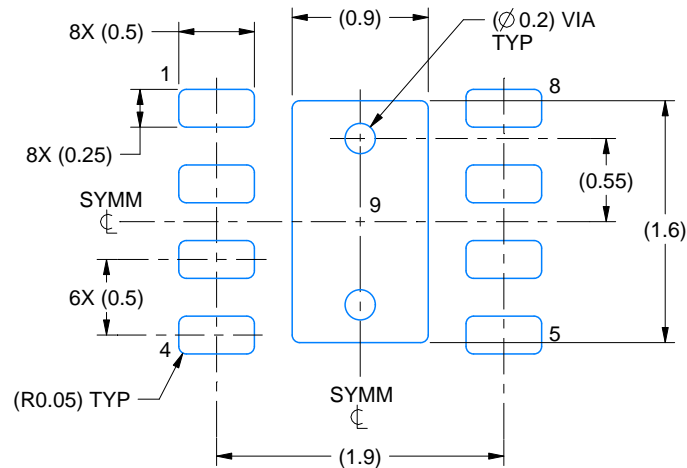
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

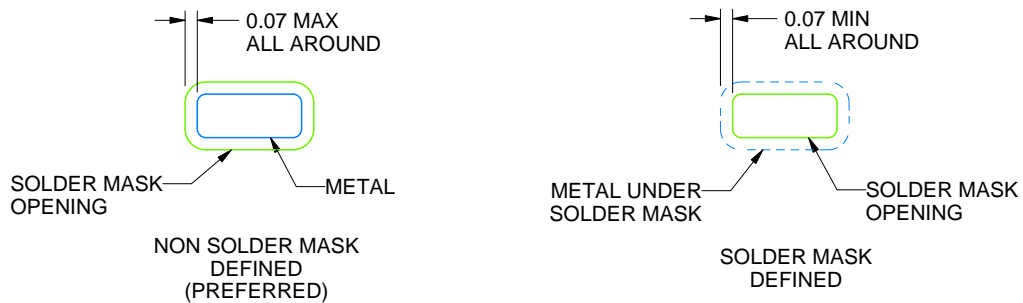
**DSG0008A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

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NOTES: (continued)

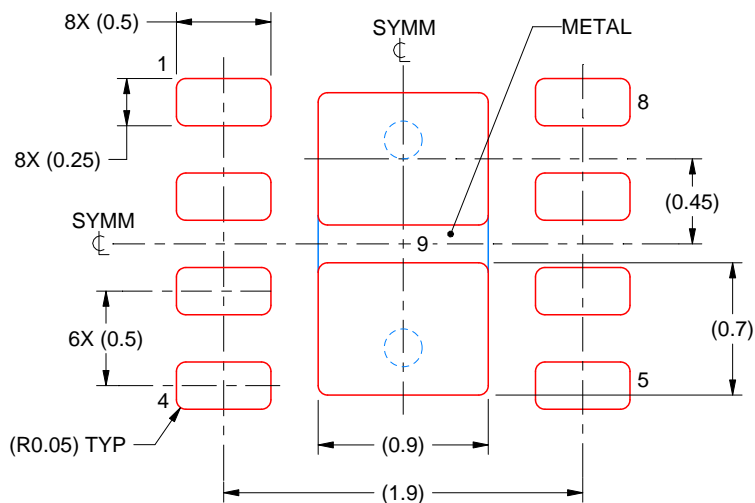
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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