TPS730 Low-Noise, High PSRR, RF, 200mA, Low-Dropout Linear Regulator

1 Features

- 200mA low-dropout regulator with enable
- Available in fixed voltages from 1.8V to 3.3V and adjustable voltages (1.22V to 5.5V)
- High PSRR (68dB at 100Hz)
- Low noise:
  - 55μV_{RMS} (legacy chip)
  - 69μV_{RMS} (new chip)
- Stable with a 2.2µF ceramic capacitor
- Excellent load, line transient response
- Very low dropout voltage: 120mV (typ)
- For a more updated portfolio device, see the TPS7A20

2 Applications

- TV applications
- Connected peripherals and printers
- Portable medical equipment
- Home theater and entertainment applications
- Building automation

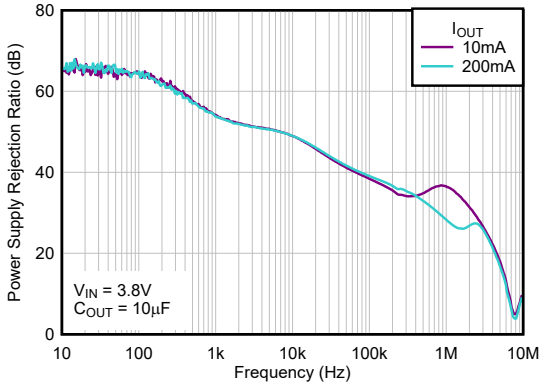
3 Description

The TPS730 is a low-dropout (LDO) voltage regulator that features high power-supply rejection ratio (PSRR) and offers excellent line and load transient responses. This device is stable with a small 2.2µF ceramic capacitor on the output. The TPS730 offers low dropout voltages (for example, 120mV typical at 200mA). The low output noise and great PSRR makes this device designed to power sensitive analog loads. The TPS730 offers a flexible option for post regulation with the adjustable capability.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS730	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DBV (SOT-23, 6)	2.9mm × 2.8mm
	YZQ (DSBGA, 5)	1.35mm × 1mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Ripple Rejection vs Frequency

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4 Pin Configuration and Functions

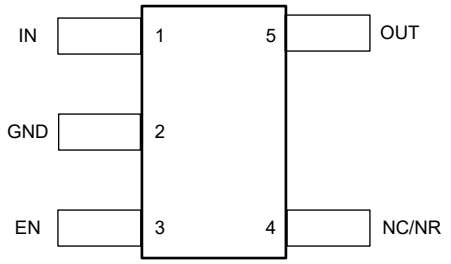


Figure 4-1. DBV Package, 5-Pin SOT-23 Fixed-Voltage Version (Top View)

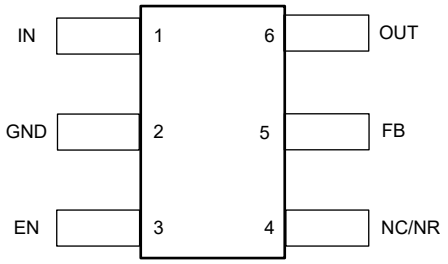


Figure 4-2. DBV Package, 6-Pin SOT-23 Adjustable-Voltage Version (Top View)

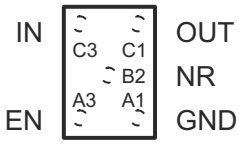


Figure 4-3. YZQ Package, 5-Pin DSBGA (Top View, Legacy Chip)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV	YZQ		
EN	3	A3	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	—	I	Feedback pin. This terminal is the feedback input pin for the adjustable device. Fixed voltage versions in the DBV package do not have this pin.
GND	2	A1	—	Regulator ground.
IN	1	C3	I	Input to the device.
NC/NR	4	B2	—	Noise-reduction pin (legacy chip). Connecting an external capacitor to this pin filters noise generated by the internal band gap. This configuration improves power-supply rejection and reduces output noise for the legacy chip and YZQ package. No connect pin (new chip). This pin is not internally connected. Connect to GND for improved thermal performance or leave floating. For lower noise performance on a fixed device, refer to the TPS7A20. For lower noise performance on the adjustable version, consider using a feed-forward capacitor.
OUT	6	C1	O	Output of the regulator.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} , V_{EN}, V_{OUT} (legacy chip)	–0.3	6	V
	V_{IN} , V_{EN} (new chip)	–0.3	6.5	V
	V_{OUT} (new chip)	–0.3	V_{IN} + 0.3 (2)	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J (DBV package)	–40	150	°C
	Operating junction, T_J (YZQ package, legacy chip only)	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, V all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{EN}	Enable voltage	0		5.5	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor (legacy chip)	0.1	1		µF
	Input capacitor (new chip)	1			
C_{OUT}	Output capacitor	2.2(1) (2)	10		µF
C_{NR}	Noise reduction capacitor(3)	0	10		nF
C_{FF}	Feed-forward capacitor (legacy chip)		15		pF
	Feed-forward capacitor (new chip)(4)	0	10	100	nF
R_2	Lower feedback resistor (legacy chip)		30.1		kΩ
F_{EN}	Enable toggle frequency (new chip)			10	kHz

(1) If C_{FF} is not used or V_{OUT}(nom) < 1.8V, the minimum recommended C_{OUT} = 4.7µF.
(2) The minimum effective capacitance is 0.47 µF for the new chip only.
(3) Legacy chip only. The new chip does not have a Noise Reduction pin. For more information please refer to Pin Functions table.
(4) Feed-forward capacitor is optional and not required for stability.

5.4 Thermal Information

THERMAL METRIC[1]		TPS793				UNIT
		DBV (SOT23-6)	YZQ (DSBGA)	DBV (SOT23-6)[2]	DBV (SOT23-5)[2]	
		6 PINS	5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	178.5	171.7	182.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	1.4	110.8	114.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	62.1	85.4	79.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.9	54.4	56.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	62.1	85.2	78.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Packaging application note.
(2) New Chip.

5.5 Electrical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range [1]		2.7		5.5	V
I_{OUT}	Continuous output current		0		200	mA
V_{FB}	Internal reference (TPS73001)		1.201	1.225	1.25	V
V_{OUT}	Output voltage range (TPS73001)		V_{FB}		5.5 – $V_{DROPOUT}$	V
	Output voltage accuracy	0µA < I_{OUT} < 200mA, V_{OUT}+ 1V < V_{IN} < 5.5V	-2%	$V_{OUT(nom)}$	2%	
$\Delta V_{OUT}/\Delta VIN$	Line regulation [1]	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V		0.05		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0µA ≤ I_{OUT} ≤ 200mA		5		mV
V_{DO} [2]	Dropout voltage	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 200mA		120	210	mV
I_{CL}	Output current limit	V_{OUT} = 0V(Legacy chip)	285		600	mA
		V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{OUT} = 0.9 x $V_{OUT(NOM)}$ (new chip only)	320		460	
I_{SC}	Short-circuit current limit	V_{OUT} = 0V (New Chip)		175		mA
I_{GND}	Quiescent current (GND current)	0µA ≤ I_O ≤ 200mA (Legacy Chip)		170	220	µA
		0µA ≤ I_O ≤ 200mA(New Chip)		250	1000	
I_{SHDN}	Shutdown current	V_{EN} = 0V, 2.7V < V_I < 5.5V (legacy chip)[3]		0.07	1	µA
		V_{EN} = 0V, 2.7V < V_I < 5.5V (new chip)[3]		0.01	1	
I_{FB}	Feedback pin current	V_{FB} = 1.8V (legacy chip)			1	µA
		V_{FB} = 1.8V (new chip)			0.05	

5.5 Electrical Characteristics (continued)

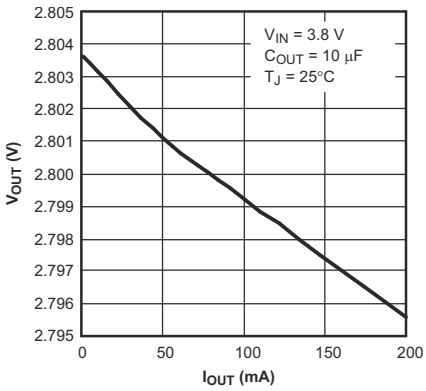
over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio	f = 100Hz	I_{OUT} = 10mA (legacy chip)		70		dB
			I_{OUT} = 10mA (new chip)		64		
			I_{OUT} = 200mA (legacy chip)		68		
			I_{OUT} = 200mA (new chip)		65		
		f = 10kHz	I_{OUT} = 200mA (legacy chip)		70		
			I_{OUT} = 200mA (new chip)		49		
		f = 100kHz	I_{OUT} = 200mA (legacy chip)		43		
			I_{OUT} = 200mA (new chip)		39		
Vn	Output noise voltage	BW = 200Hz to 100kHz, I_{OUT} = 200mA	C_{NR} = 0.01µF		33		μV_{RMS}
		BW = 200Hz to 100kHz, I_{OUT} = 200mA	(new chip)[4]		69		
t_{STR}	Time, start-up	R_L = 14 Ω, C_{OUT} = 1µF	C_{NR} = 0.001µF		50		µs
			C_{NR} = 0.0047µF		50		
			C_{NR} = 0.01µF		50		
			(new chip)[4]		500		
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		1.7		V_{IN}	V
		2.7V ≤ V_{IN} ≤ 5.5V (new chip)		0.85		V_{IN}	
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		0		0.7	V
		2.7V ≤ V_{IN} ≤ 5.5V (new chip)		0		0.425	
I_{EN}	Enable pin current	V_{EN} = 0 V		–1		1	µA
V_{UVLO}	UVLO threshold	V_{IN} rising (legacy chip)		2.25		2.65	V
		V_{IN} rising (new chip)		1.32		1.6	
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{CC} rising (legacy chip)			100		mV
		V_{CC} rising (new chip)			130		

(1) Minimum VIN is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Dropout is not measured for the TPS73018 and TPS73025 because minimum V_{IN} = 2.7V.
(3) For adjustable versions, this parameters applies only after V_{IN} is applied; then V_{EN} transitions high to low.
(4) New Chip does not have a Noise Reduction pin.

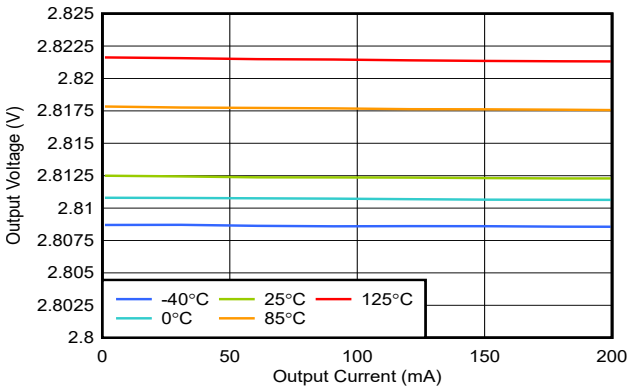
5.6 Typical Characteristics

over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



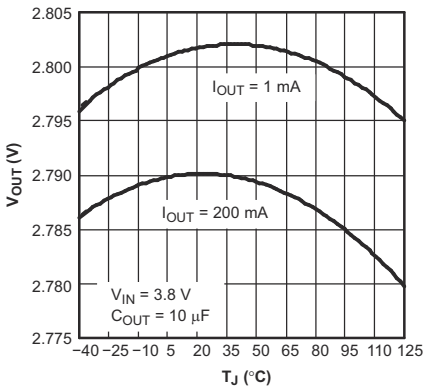
Legacy chip

Figure 5-1. TPS730 Output Voltage vs Output Current



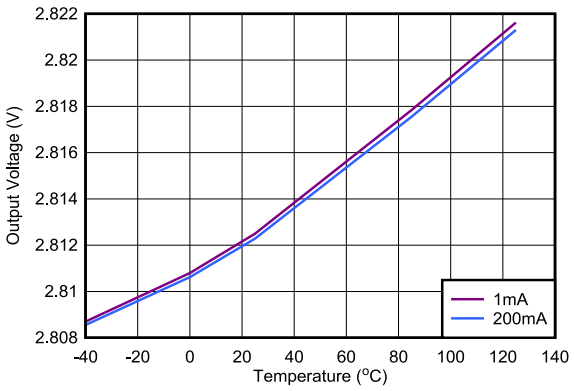
New chip

Figure 5-2. TPS730 Output Voltage vs Output Current



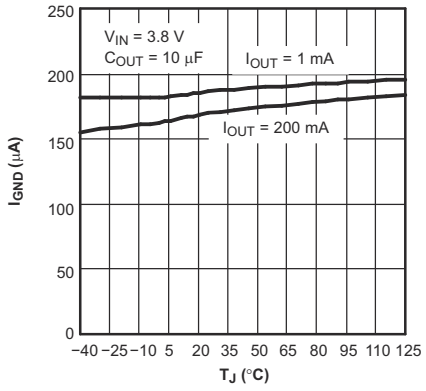
Legacy chip

Figure 5-3. TPS730 Output Voltage vs Junction Temperature



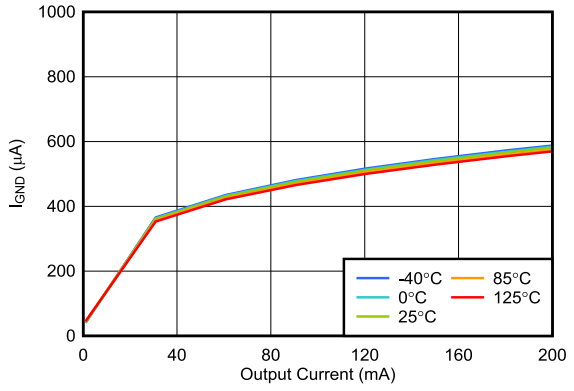
New chip

Figure 5-4. TPS730 Output Voltage vs Junction Temperature



Legacy chip

Figure 5-5. TPS730 Ground Current vs Junction Temperature

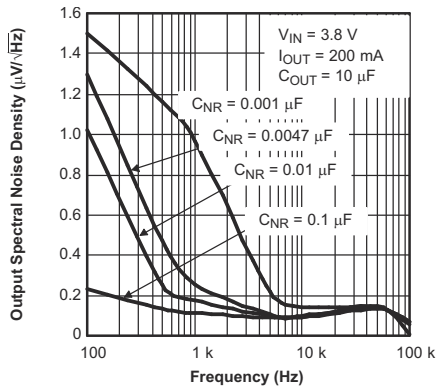


New chip

Figure 5-6. TPS730 Ground Current vs Junction Temperature

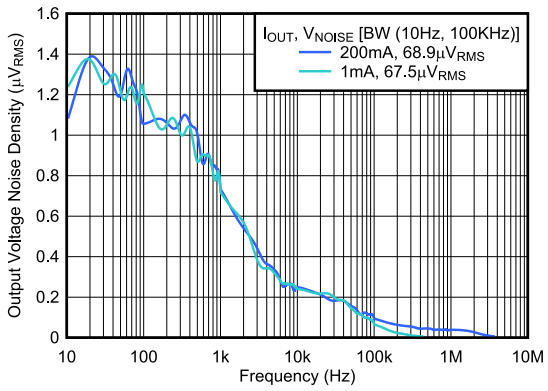
5.6 Typical Characteristics (continued)

over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



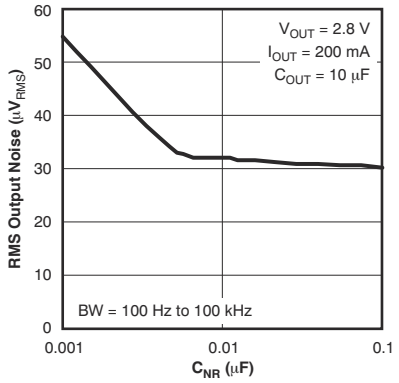
Legacy chip

Figure 5-7. TPS730 Output Spectral Noise Density vs Frequency



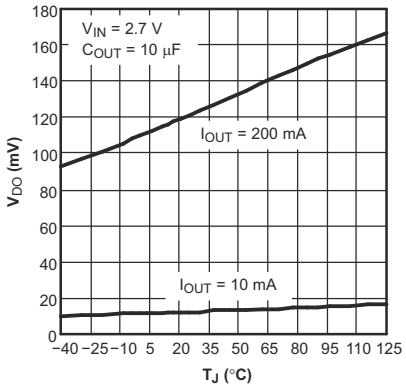
C_{OUT} = 10uF (new chip)

Figure 5-8. TPS730 Output Spectral Noise Density vs Frequency



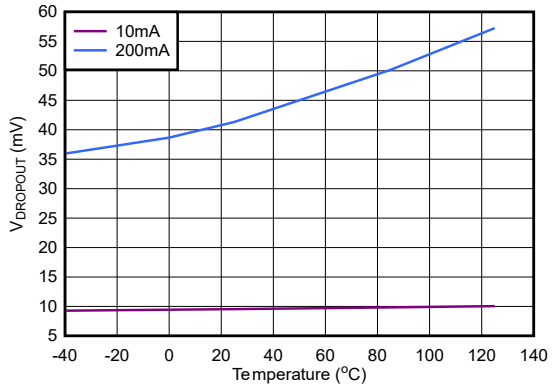
Legacy chip

Figure 5-9. Root Mean Square Output Noise vs C_{NR}



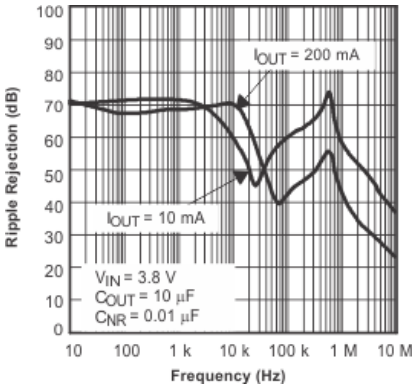
Legacy chip

Figure 5-10. TPS730 Dropout Voltage vs Junction Temperature



New chip

Figure 5-11. TPS730 Dropout Voltage vs Junction Temperature



Legacy chip

Figure 5-12. TPS730 Ripple Rejection vs Frequency

5.6 Typical Characteristics (continued)

over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

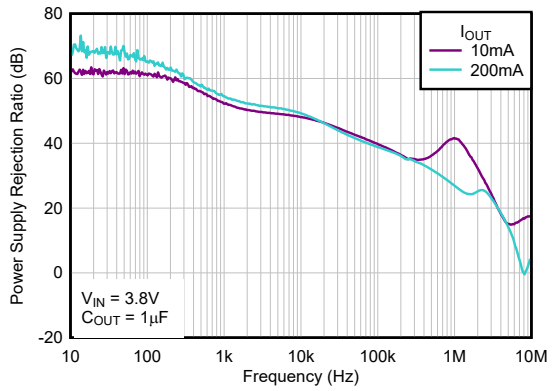


Figure 5-13. TPS730 Ripple Rejection vs Frequency

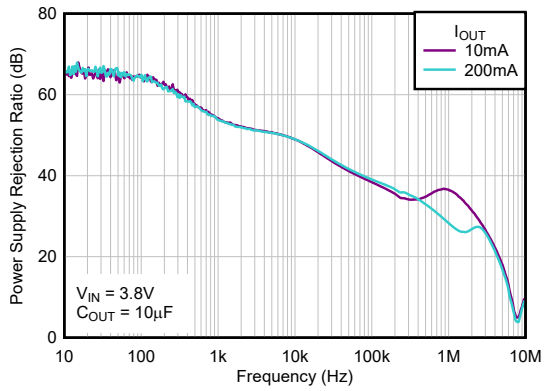


Figure 5-14. TPS730 Ripple Rejection vs Frequency

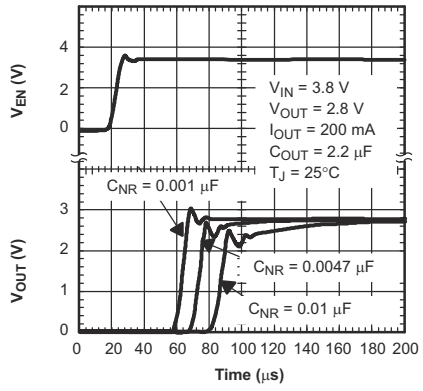


Figure 5-15. TPS730 Output Voltage, Enable Voltage vs Time (Start-Up)

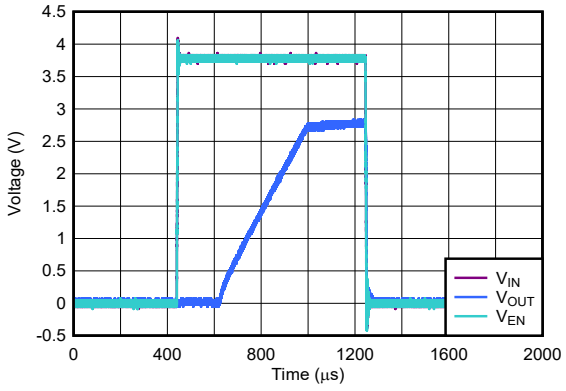


Figure 5-16. TPS730 Output Voltage, Enable Voltage vs Time (Start-Up)

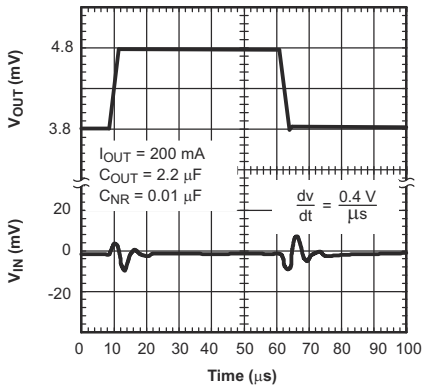


Figure 5-17. TPS730 Line Transient Response

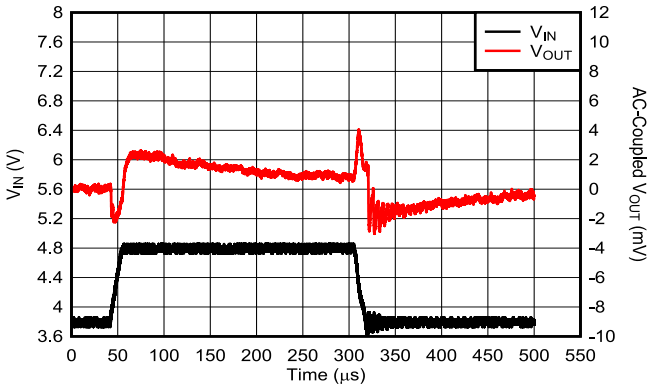
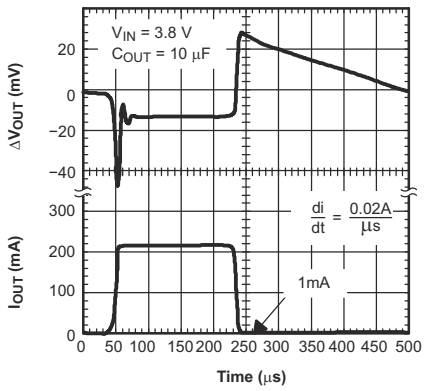


Figure 5-18. TPS730 Line Transient Response

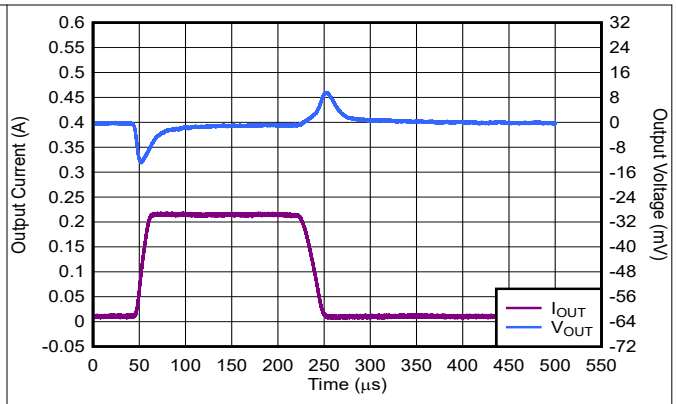
5.6 Typical Characteristics (continued)

over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



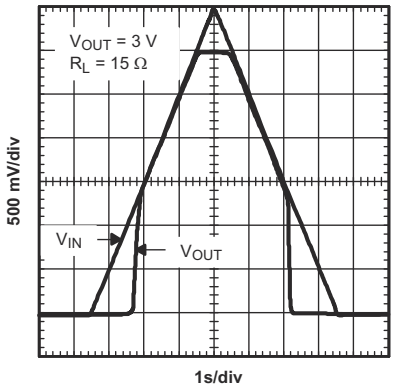
Legacy chip

Figure 5-19. TPS730 Load Transient Response



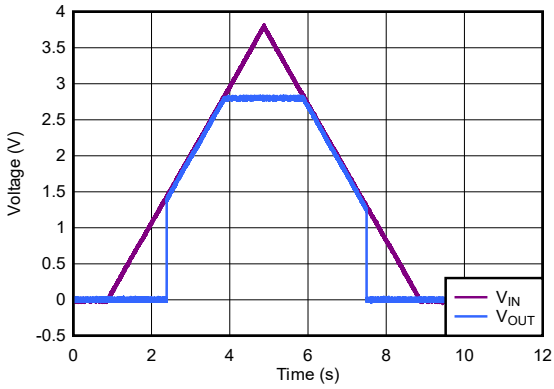
New chip

Figure 5-20. TPS730 Load Transient Response



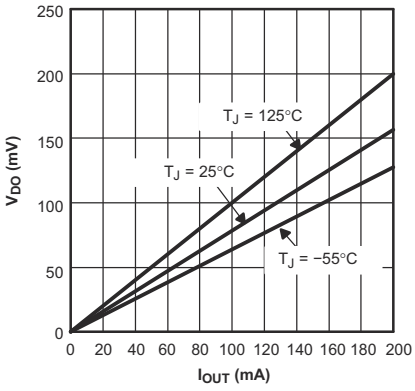
Legacy chip

Figure 5-21. Power-Up and Power-Down



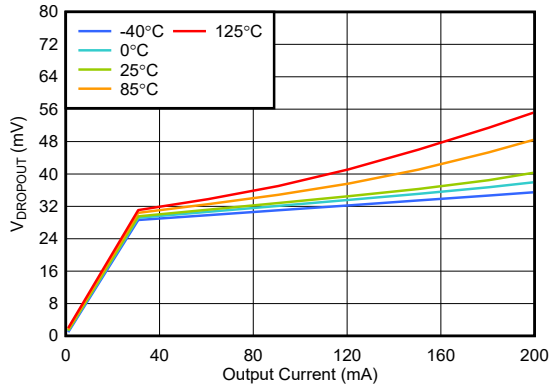
New chip

Figure 5-22. Power-Up and Power-Down



Legacy chip

Figure 5-23. Dropout Voltage vs Output Current

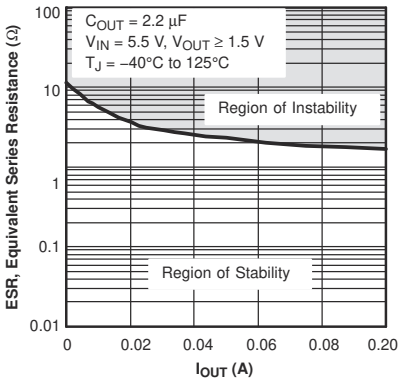


New chip

Figure 5-24. Dropout Voltage vs Output Current

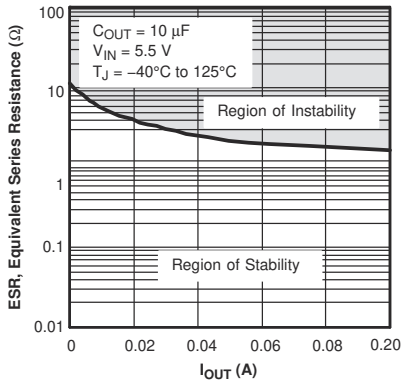
5.6 Typical Characteristics (continued)

over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



Legacy chip

Figure 5-25. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current



Legacy chip

Figure 5-26. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS730 low-dropout (LDO) regulator is optimized for use in noise-sensitive, battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current, and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

6.2 Functional Block Diagrams

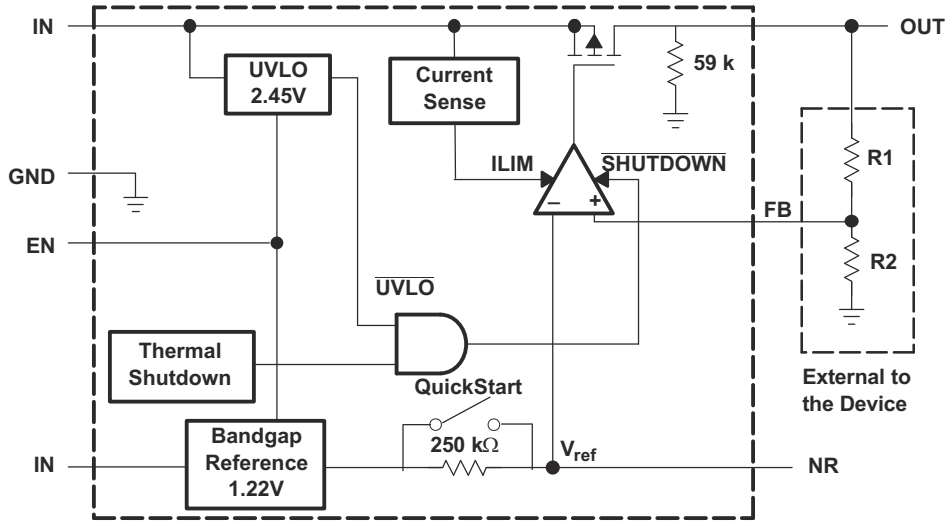


Figure 6-1. TPS730 Block Diagram (Adjustable-Voltage Version, Legacy Chip)

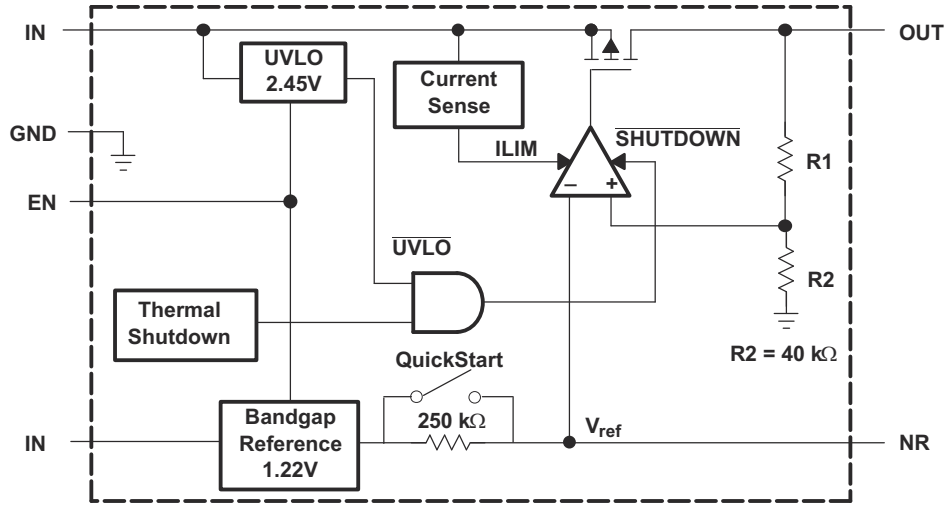


Figure 6-2. TPS730 Block Diagram (Fixed-Voltage Versions, Legacy Chip)

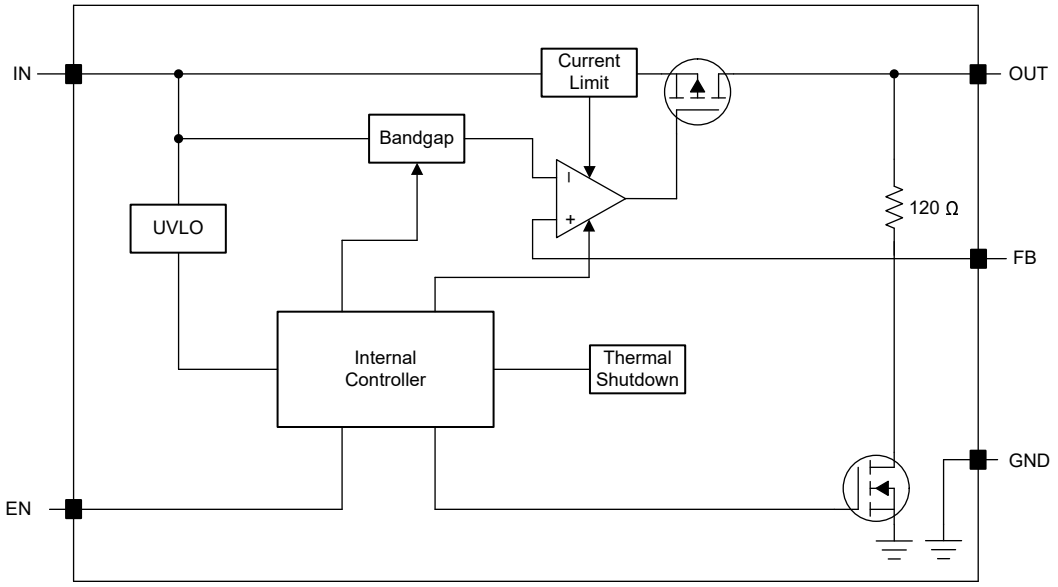


Figure 6-3. TPS730 Block Diagram (Adjustable Version, New Chip)

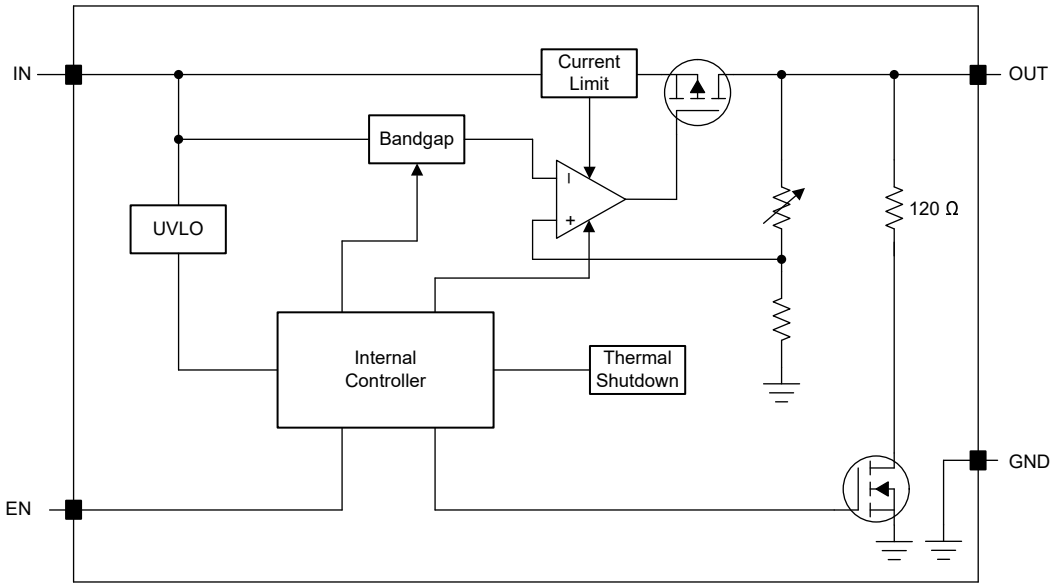


Figure 6-4. TPS730 Block Diagram (Fixed Version, New Chip)

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

The TPS730 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

6.3.3 Foldback Current Limit

The TPS730 features internal current limiting and thermal protection. During normal operation, the TPS730 limits output current to approximately 400mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, do not exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit (I_{SC})*. I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-5 shows a diagram of the foldback current limit.

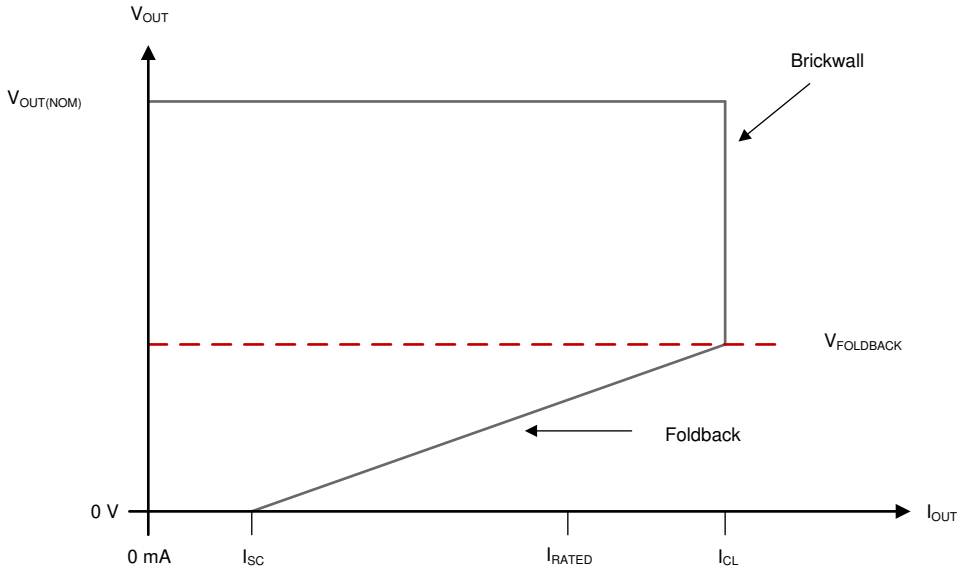


Figure 6-5. Foldback Current Limit

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$(1)

(1) Approximate value for thermal shutdown.

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature
- The input voltage is less than $UVLO_{falling}$

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS730 low-dropout (LDO) regulator is optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

7.1.1 Adjustable Operation

The output voltage of the TPS73001 adjustable regulator is programmed using an external resistor divider as shown in Figure 7-1. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

- V_{REF} = 1.225 V typical (the internal reference voltage)

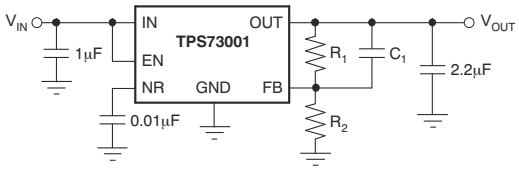
Resistors R_1 and R_2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues and other problems. The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 50 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB. For output voltages < 1.8 V, the value of this capacitor should be 100 pF. For output voltages > 1.8 V, use Equation 3 to calculate the approximate value of this capacitor.

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

Figure 7-1 shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.22V	short	open	0pF
2.5V	31.6kΩ	30.1kΩ	22pF
3.3V	51kΩ	30.1kΩ	15pF
3.6V	59kΩ	30.1kΩ	15pF

Figure 7-1. TPS73001 Adjustable LDO Regulator Programming

7.1.2 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

7.1.3 Input and Output Capacitor Requirements

The TPS730 legacy chip requires a 0.1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the device, for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS730 new chip requires a 1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the device, for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS730 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2µF. Any 2.2µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1µF ceramic capacitor can be used. If a feed-forward capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8V is chosen, then the minimum recommended output capacitor is 4.7µF instead of 2.2µF. Table 7-1 lists the recommended output capacitor sizes for several common configurations.

Table 7-1. Output Capacitor Sizing

CONDITION	C_{OUT} (µF)
V_{OUT} < 1.8 V or C_{FF} = 0 nF	4.7
V_{OUT} > 1.8 V, I_{OUT} > 100 mA	2.2
V_{OUT} > 1.8 V, I_{OUT} < 100 mA	1

7.1.4 Noise-Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The TPS730 (legacy chip) has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor must be no more than 0.1 µF to verify that the capacitor is fully charged during the quick-start time provided by the internal switch shown in the *Functional Block Diagram* section.

Note

C_{NR} is not required. The TPS730 (new chip) has a NC (no connect) pin instead; keeping a C_{NR} does not impact device performance.

7.1.5 Reverse Current Operation

The TPS730 legacy chip PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate. If extended reverse voltage operation in anticipated, external limiting to 5% of the rated output current is recommended.

The TPS793 new chip, as with most modern LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 7-2 shows one approach of protecting the device.

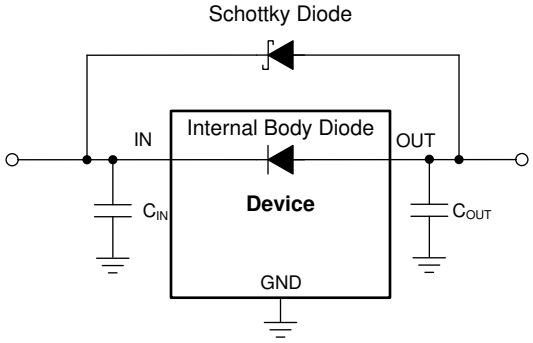


Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2 Typical Application

A typical application circuit is shown in Figure 7-3.

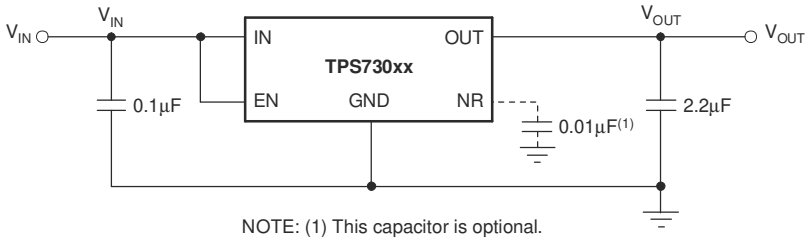


Figure 7-3. Typical Application Circuit

7.2.1 Design Requirements

Table 7-2 lists the design requirements.

Table 7-2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

7.2.2 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 1µF is used as the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 10 µF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to Figure 7-7.

7.2.3 Application Curves

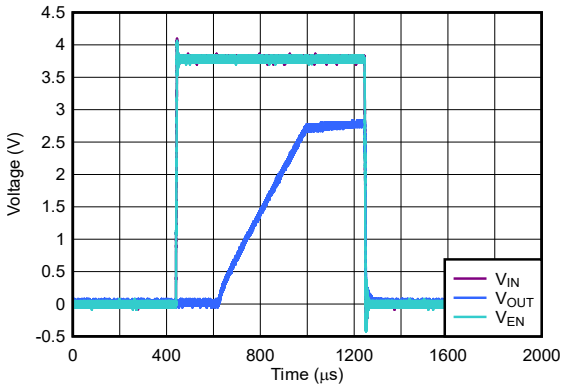


Figure 7-4. TPS730 Output Voltage, Enable Voltage vs Time (Start-Up)

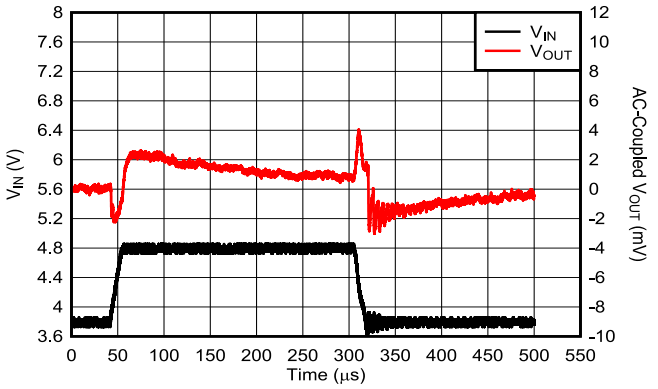


Figure 7-5. TPS730 Line Transient Response

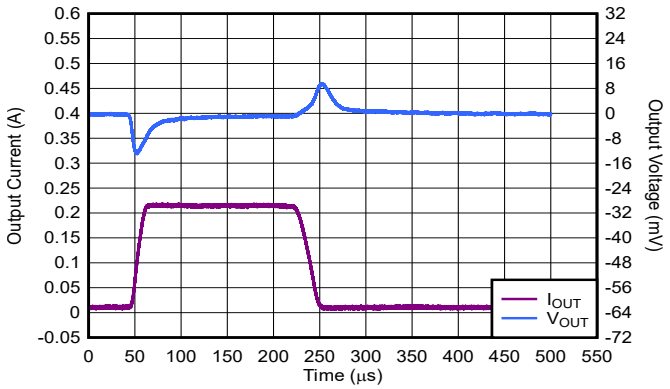


Figure 7-6. TPS730 Load Transient Response

7.3 Best Design Practices

Do place at least one, low-ESR, 2.2-µF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1-µF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the NR pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

7.4 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1-µF input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

7.5.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

7.5.1.2 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS730 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS730 into thermal shutdown degrades device reliability.

7.5.1.3 Power Dissipation

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 4:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\Theta JA}} \tag{4}$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{5}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Figure 7-7 illustrates the maximum ambient temperature versus the power dissipation of the TPS730. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS730 does not operate above a junction temperature of 125°C.

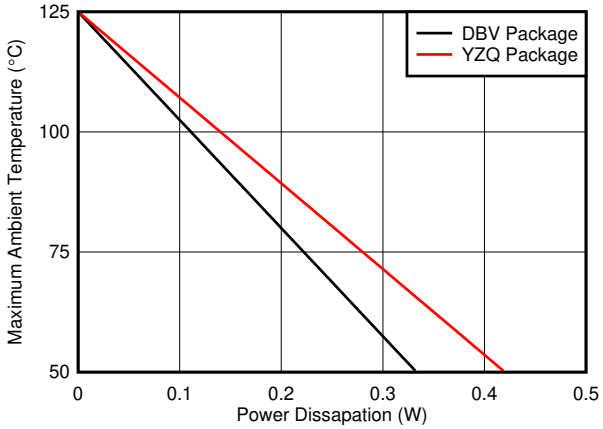


Figure 7-7. Maximum Ambient Temperature vs Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 6.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

where:

- P_D is the power dissipation shown by Equation 5
- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface*

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

7.5.2 Layout Examples

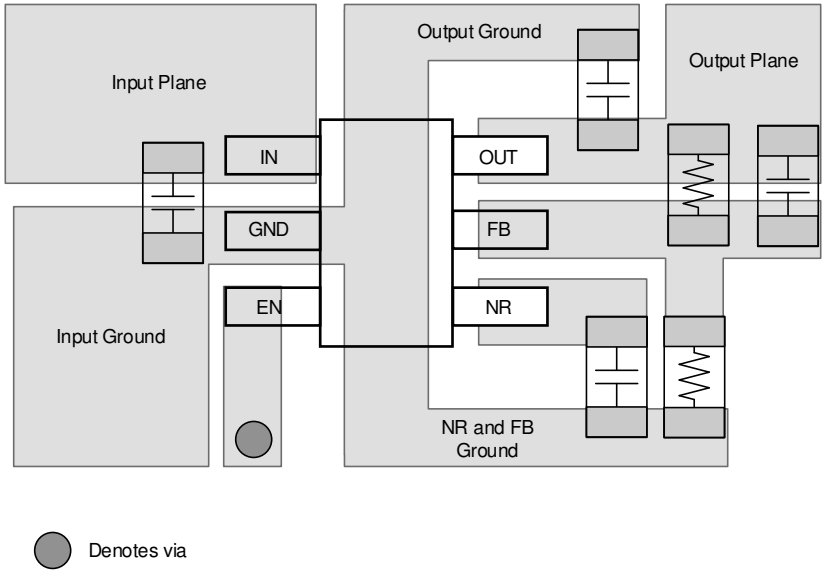


Figure 7-8. Layout Example (DBV Adjustable Package, Legacy Chip)

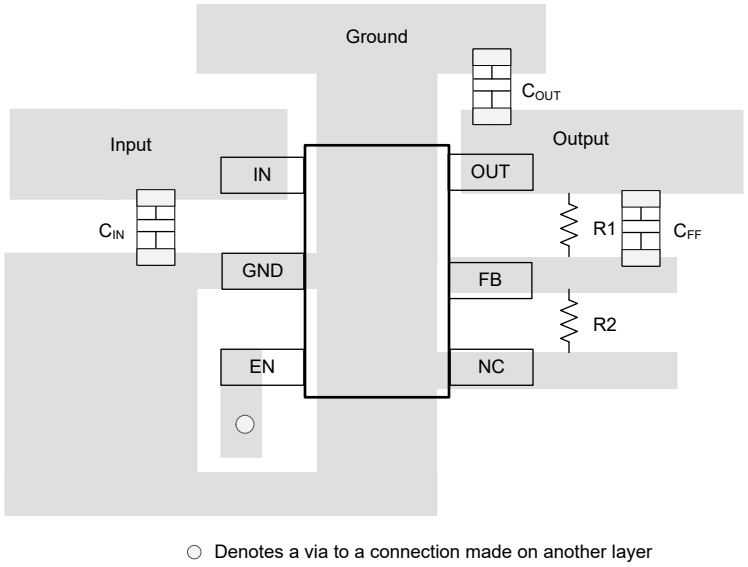


Figure 7-9. Layout Example (DBV Adjustable Package, New Chip)

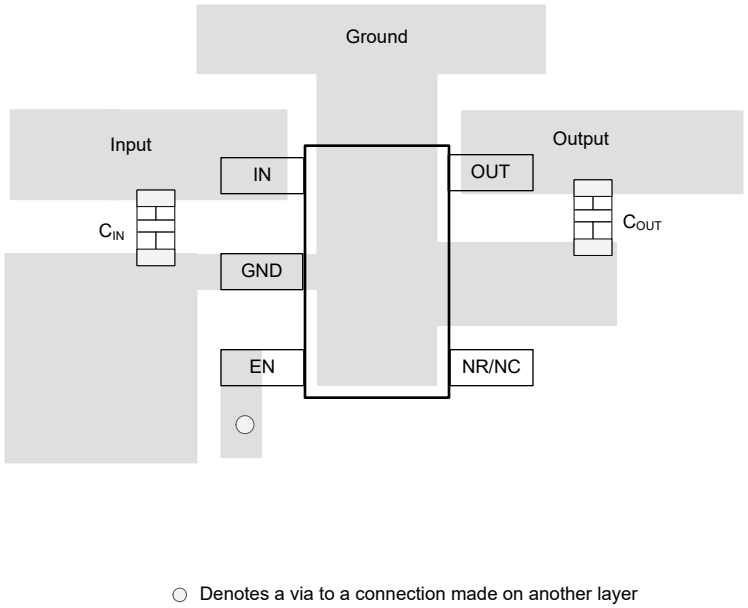


Figure 7-10. Layout Example (DBV Fixed Package, New Chip)

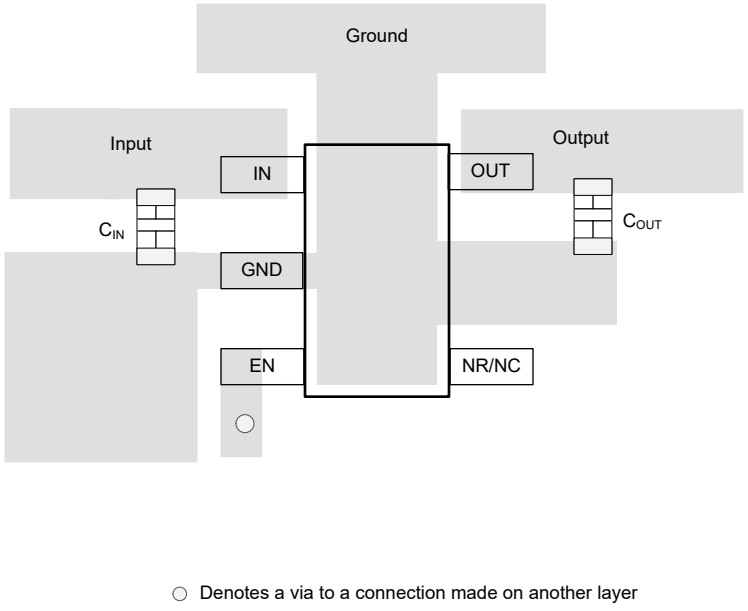


Figure 7-11. Layout Example (DBV Fixed Package, New Chip)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS730 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Ordering Information

PRODUCT(1) (2)	DESCRIPTION
TPS730**xxyyy z *M3***	**xx** is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact the factory for details and availability.

8.2 Documentation Support

8.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (April 2015) to Revision K (June 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added new silicon (M3) devices to document..... 1
- Changed entire document to identify the features and differences of the legacy chip and new chip and the adjustable and fixed versions of the device..... 1
- Changed *Features*, *Applications*, and *Description* sections..... 1
- Changed front-page figure 1
- Changed *Pin Configuration and Functions* section: Changed DBV pinout NR pins to NC/NR, added NC/NR pin row with reference to TPS7A20 for lower noise performance to *Pin Functions* table..... 3
- Added new silicon curves to *Typical Characteristics* section..... 7
- Deleted *(170 µA, typically)* from quiescent current discussion in *Overview* section..... 12
- Changed *Functional Block Diagrams* section..... 12
- Changed *Shutdown* section..... 14
- Changed *Foldback Current Limit* section..... 14
- Changed *Input and Output Capacitor Requirements* section..... 18
- Changed *Reverse Current Operation* section..... 19
- Changed input capacitor value from *0.1µF* to *1µF* in *Detailed Design Procedure* section..... 20
- Changed *Application Curves* section..... 20
- Added new figures to *Layout Examples* section..... 24
- Added M3 information to *Ordering Information* table..... 26

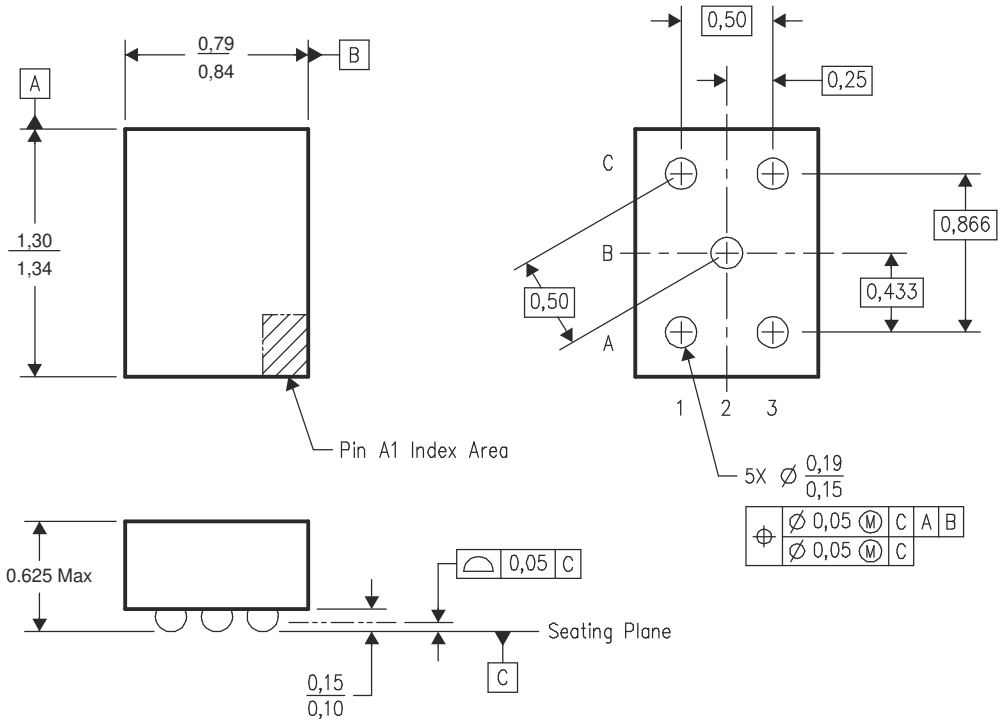
Changes from Revision I (February 2011) to Revision J (April 2015) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed fourth bullet of *Features* list to *low noise* 1
- Changed front-page figure 1
- Added *Pin Configuration and Functions* section..... 3
- Added condition statement to *Typical Characteristics* 7
- Moved *Ordering Information* to *Device Nomenclature* section 26

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 TPS730YZQ Nanostar™ Wafer Chip Scale Information



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

Figure 10-1. Nanostar™ Wafer Chip Scale Package

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73001DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVRM3	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73001DBVTG4	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI
TPS73018DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73018DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI
TPS73025DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS73025DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS73025DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS73025DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI
TPS73025DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PGWI
TPS730285DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII
TPS730285DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII
TPS730285DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PHII
TPS73028DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS73028DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS73028DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI
TPS73028DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PGXI
TPS73028YZQT	Obsolete	Production	DSBGA (YZQ) | 5	-	-	Call TI	Call TI	-40 to 125	E2
TPS73030DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73030DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS73030DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS73030DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI
TPS73033DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73033DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI
TPS73047DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI
TPS73047DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

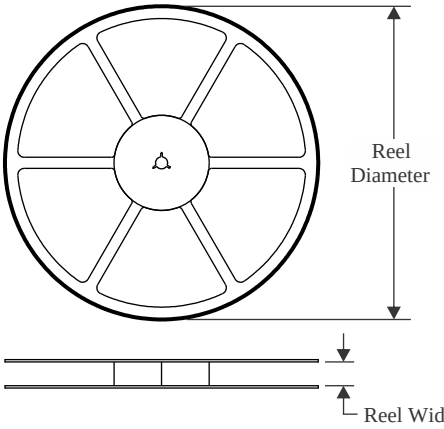
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

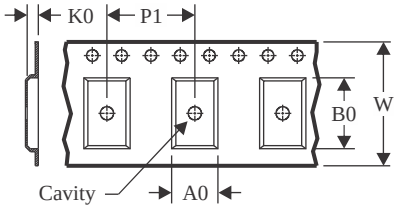
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

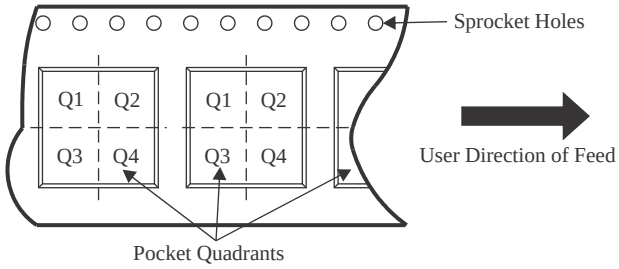


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

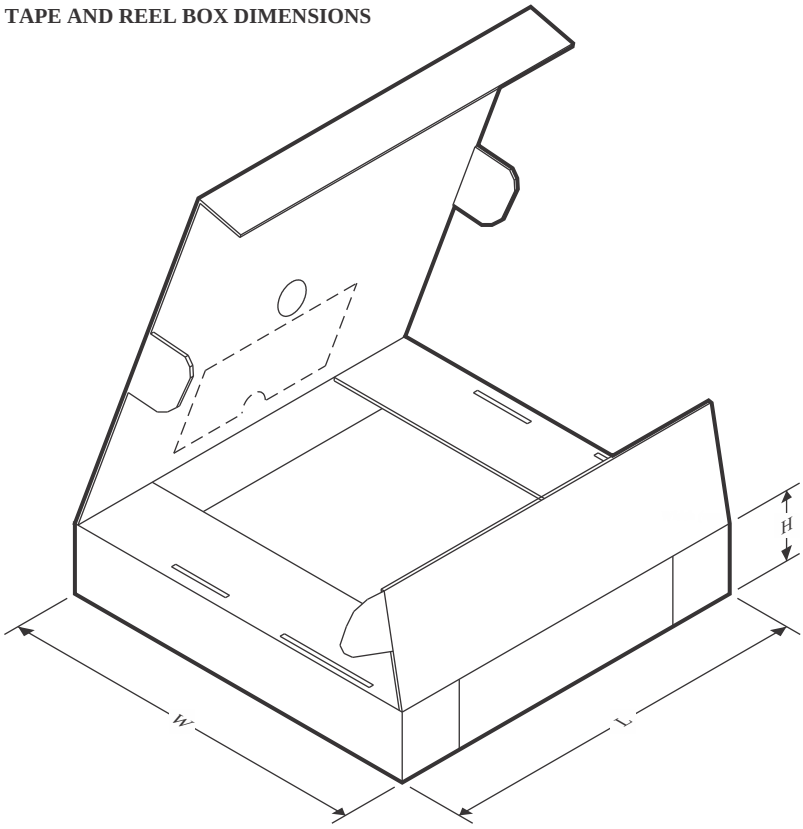


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73001DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73001DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73001DBVRG4	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73001DBVRM3	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73001DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73030DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73030DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73033DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73047DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

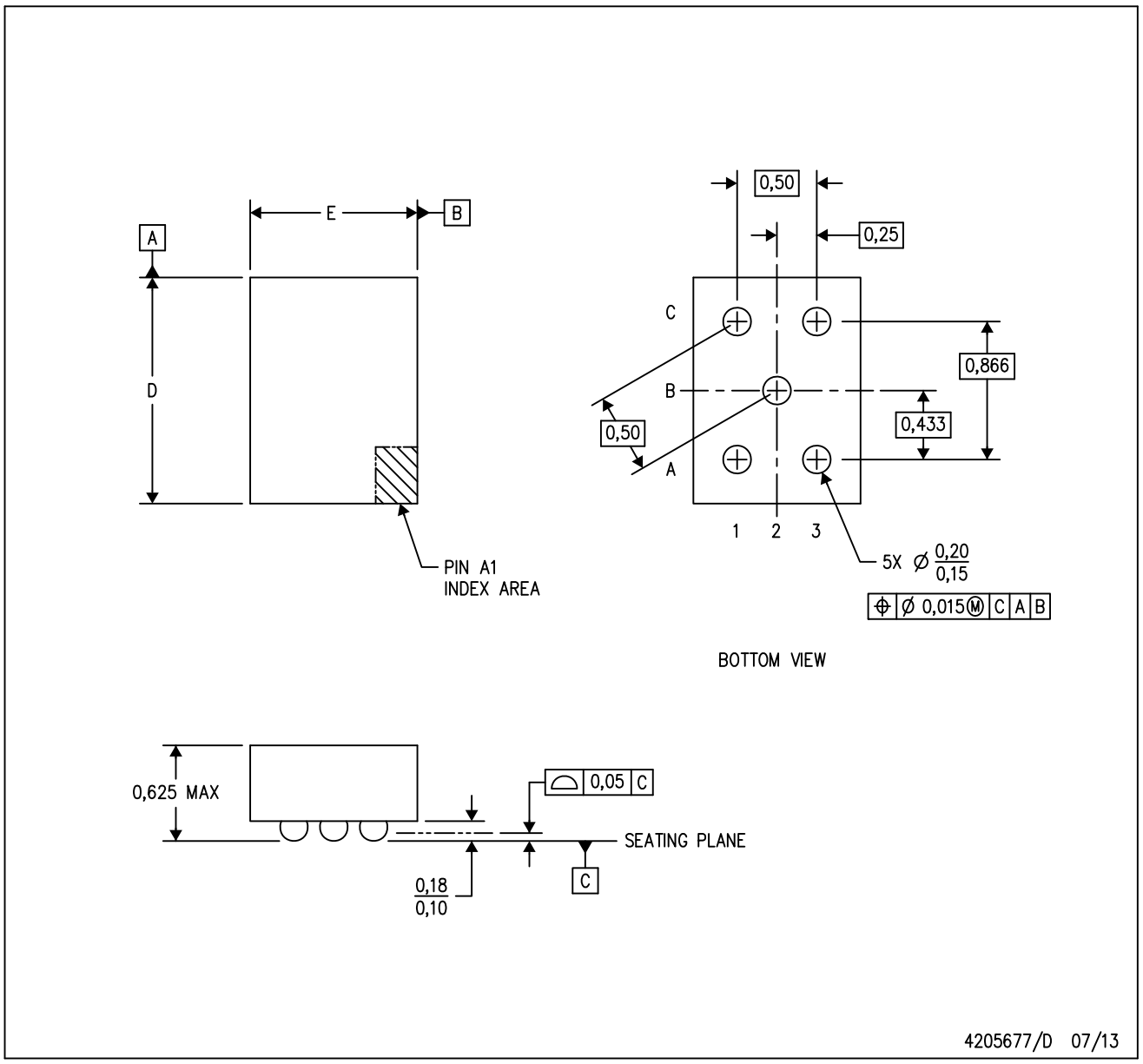


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73001DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS73001DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS73001DBVRG4	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS73001DBVRM3	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS73001DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS73018DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73018DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73018DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73018DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73025DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73025DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS730285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73028DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73030DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73030DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73047DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0

YZQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



Notes: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree ™ package configuration.

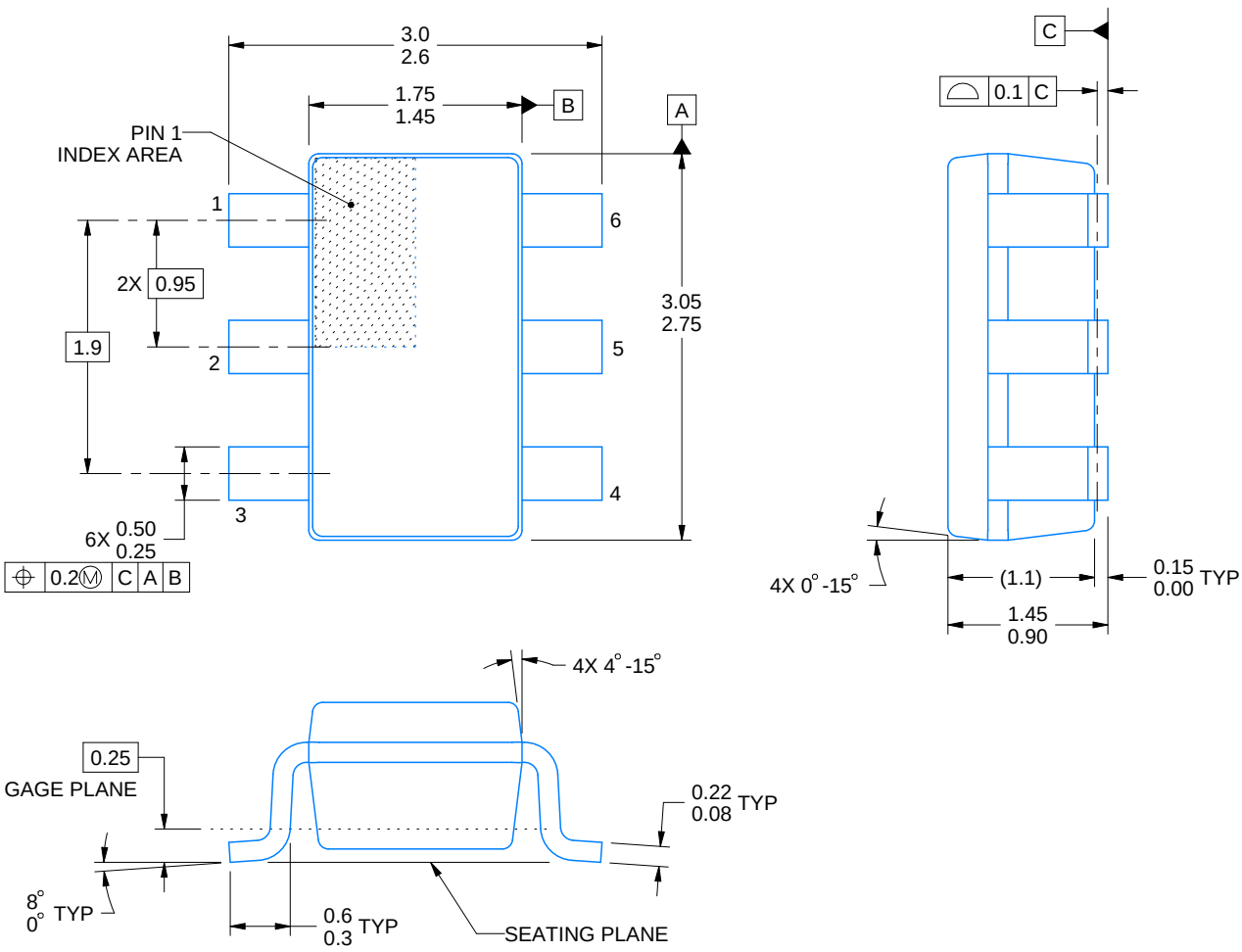
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

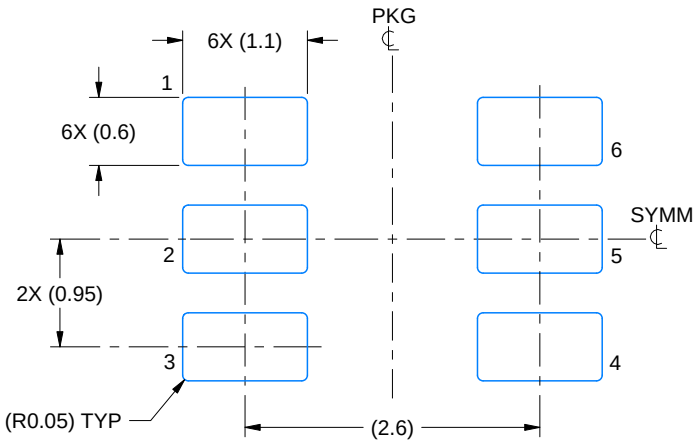
SMALL OUTLINE TRANSISTOR



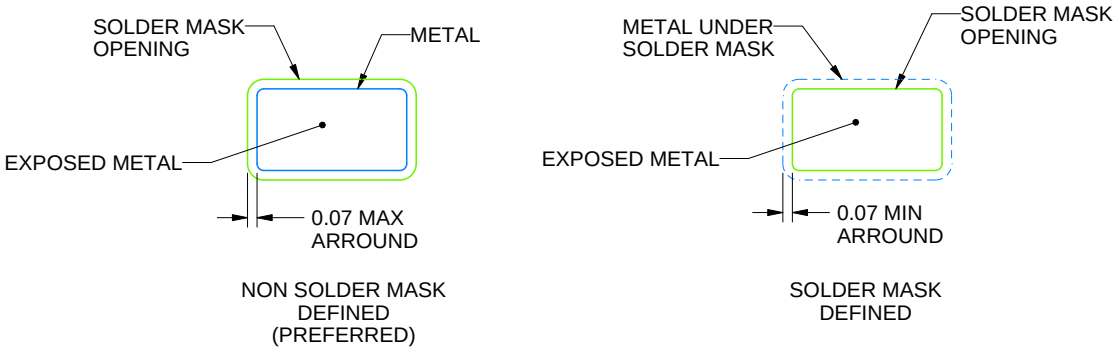
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

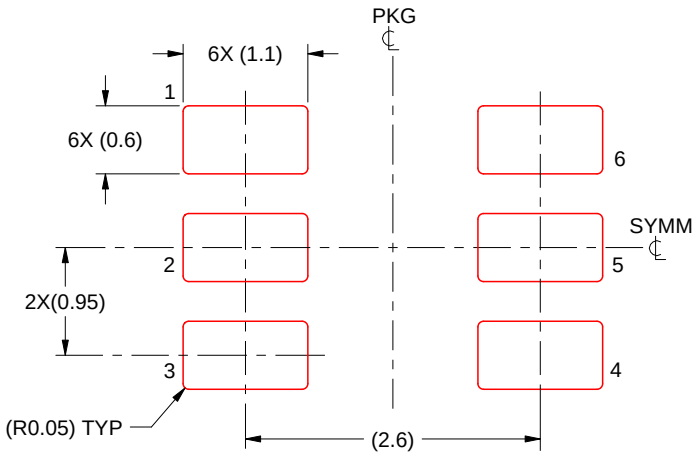


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

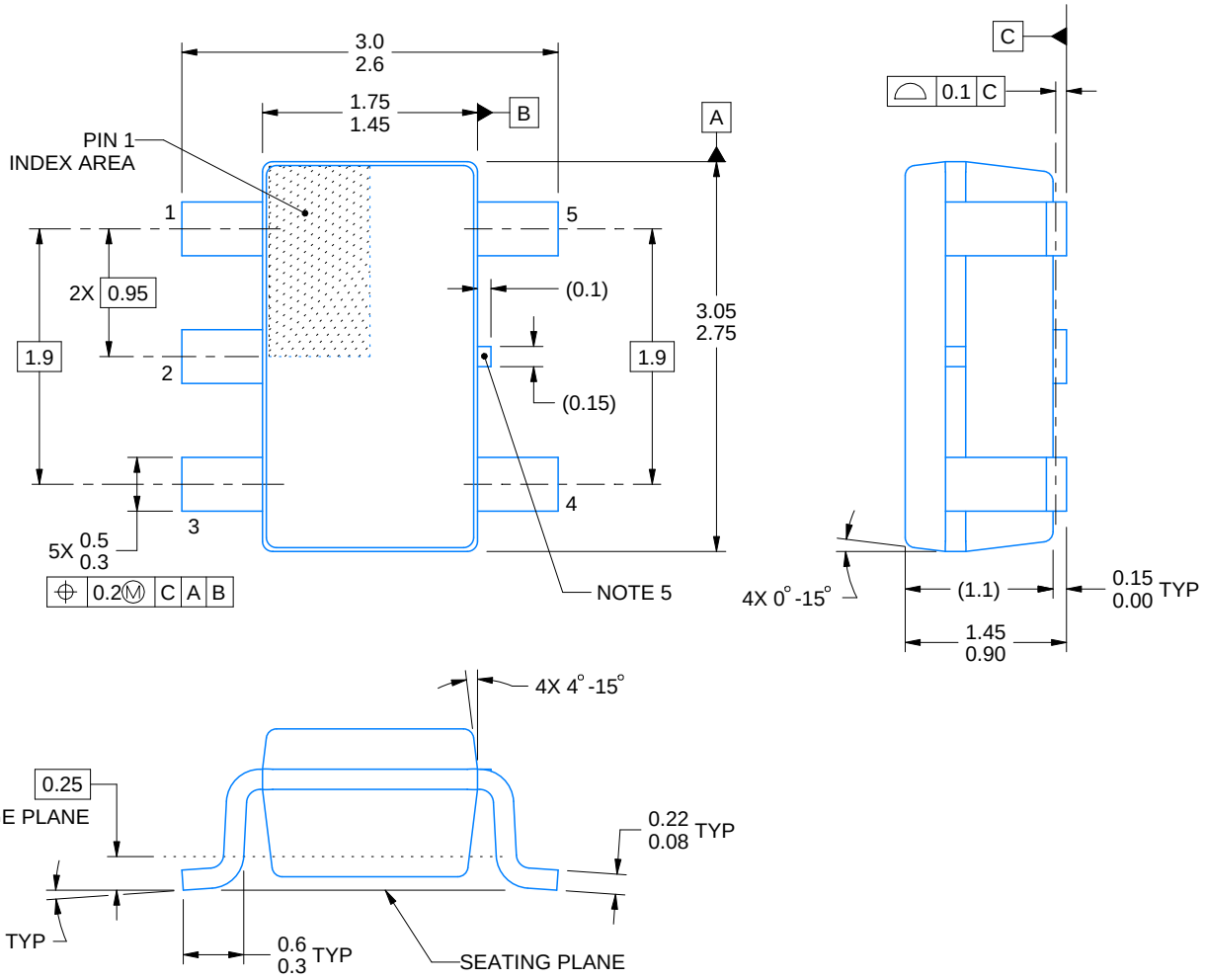
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

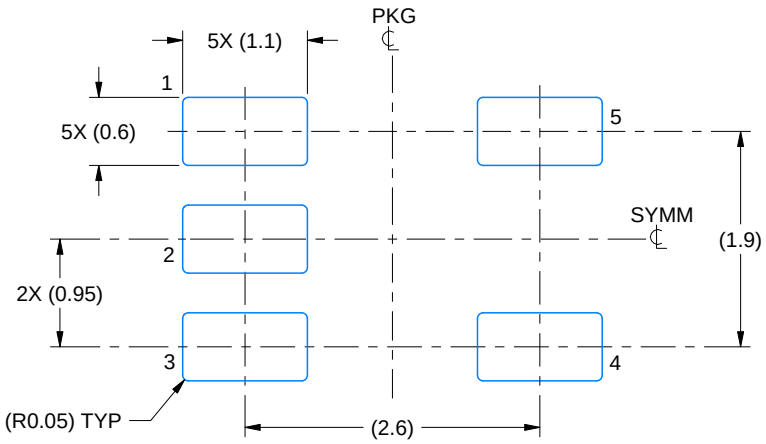
SMALL OUTLINE TRANSISTOR



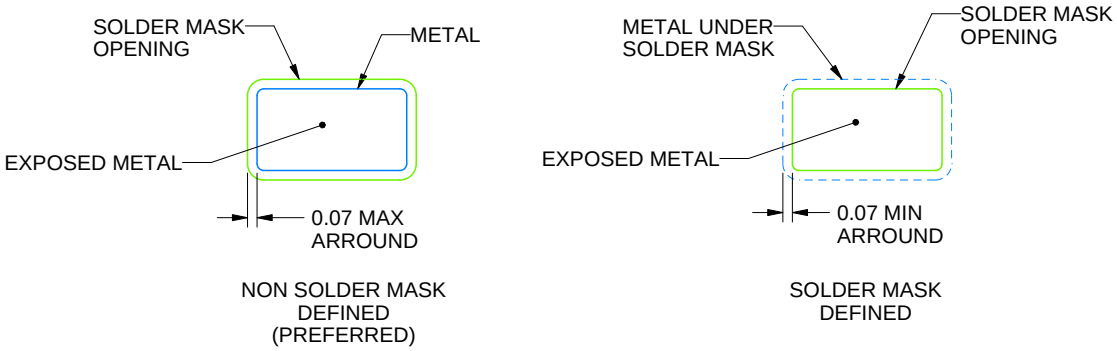
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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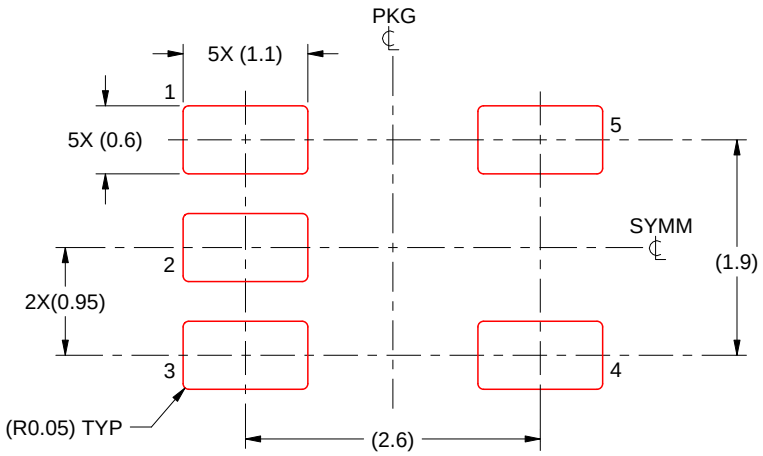
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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