

TPS732-Q1 車載、コンデンサ不要、NMOS、250mA、低ドロップアウト レギュレータ、逆電流保護機能搭載

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 0: $-40^{\circ}\text{C} \sim 150^{\circ}\text{C}$, T_A
 - デバイス HBM 分類レベル 2
 - デバイス CDM 分類レベル C4B
 - デバイス MM 分類レベル M2
- 出力コンデンサなし、または任意の値またはタイプのコンデンサで安定動作
- 入力電圧範囲: 1.7V~5.5V
- 非常に低いドロップアウト電圧: 250mA において 40mV (標準値)
- オプションの出力コンデンサの有無にかかわらず非常に優れた負荷過渡応答
- NMOS トポロジにより、低い逆リーク電流を実現
- 低ノイズ: $30\mu\text{V}_{\text{RMS}}$ (標準値、10kHz~100kHz)
- 初期精度: 0.5%
- 1% の総合精度 (ライン、負荷、温度)
- シャットダウン モードの最大 I_Q : 1 μA 未満
- サーマル シャットダウン、仕様規定された最小 / 最大電流制限保護
- 複数の出力電圧バージョンが利用可能:
 - 1.2V、1.5V、1.6V、1.8V、2.5V、3V、3.3V、5V の固定出力電圧
 - 可変出力: 1.2V~5.5V
 - カスタム出力品も提供

2 アプリケーション

- 携帯型およびバッテリー駆動の機器
- スイッチング電源のポストレギュレーション
- ノイズの影響を受けやすい回路 (VCO など)
- DSP、FPGA、ASIC、マイクロプロセッサのポイントオブロードレギュレーション

3 概要

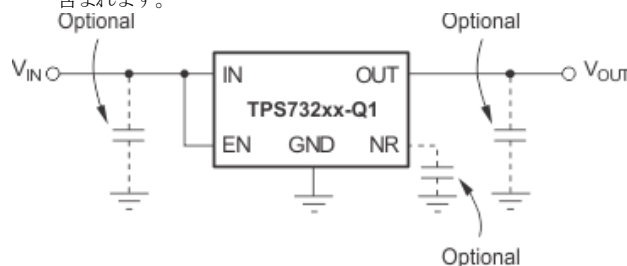
TPS732-Q1 低ドロップアウト (LDO) 電圧レギュレータは、NMOS パス過渡で構成される SAN NMOS トポロジを電圧フォロウ構成で使用します。このトポロジは、低 ESR の出力コンデンサで安定に動作し、コンデンサを使用しなくても動作できます。また、このトポロジは逆耐圧が高く (低逆電流)、グランド ピン電流が全出力電流値にわたってほぼ一定です。

TPS732-Q1 は、小さいドロップアウト電圧と小さなグランドピン電流を実現すると同時に、先進の BiCMOS プロセスを使用することで高い精度を達成しています。ディセーブル時の消費電流は 1 μA 未満であり、携帯型アプリケーション向けに設計されています。非常に小さい出力ノイズ (0.1 μF の C_{NR} で $30\mu\text{V}_{\text{RMS}}$) は、VCO への電力供給向けに設計されています。このデバイスは、サーマル シャットダウンとフォールドバック電流制限によって保護されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TPS732-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm
	DRB (VSON, 8)	3mm × 3mm

- 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



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代表的なアプリケーション回路 (固定電圧バージョン)



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4 Pin Configuration and Functions

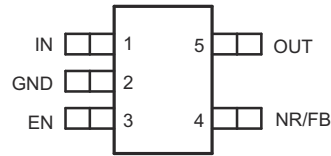


図 4-1. DBV Package 5-Pin SOT-23 Top View

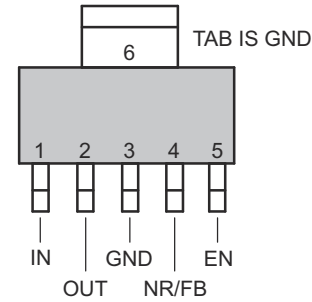
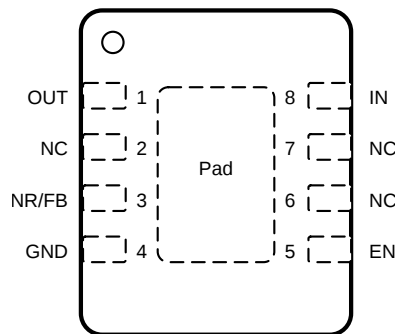


図 4-2. DCQ Package, 6-Pin SOT-223 (Top View)



NC: No internal connection

図 4-3. DRB Package 8-Pin VSON With Exposed Thermal Pad Top View

表 4-1. Pin Functions

PIN				TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.				
	SOT-2 3	SOT-2 23	VSON		
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See Shutdown for more details. EN can be connected to IN if not used.
FB ⁽²⁾	4	4	3	I	Input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	3, 6	4	—	Ground
IN	1	1	8	I	Unregulated input supply
NR ⁽³⁾	4	4	3	—	Connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This allows output noise to be reduced to low levels.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.
Pad	—	—	Pad	—	Ground
NC	—	—	2, 6, 7	—	No internal connection

(1) I = Input; O = Output.

(2) Adjustable voltage versions only.

(3) Fixed voltage versions only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR} , V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See Thermal Information		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{slg}	–65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM) (legacy silicon only)	±200	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS732-Q1 New silicon		UNIT
		DRB (VSON)	DCQ (SOT-223)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.9	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	8.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	17.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS732-Q1 Legacy silicon		UNIT
		DBV (SOT-23)	DRB (VSON)	
		5 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	180	47.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	64	83	°C/W
R _{θJB}	Junction-to-board thermal resistance	35	–	°C/W
ψ _{JT}	Junction-to-top characterization parameter	–	2.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	–	17.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	–	12.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.6 Electrical Characteristics

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 0.5\text{V}^{(1)}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{FB}	Internal reference (TPS73201-Q1)	T _J = 25°C		1.198	1.204	1.210	V
V _{OUT}	Output voltage range (TPS73201-Q1) ⁽²⁾			V _{FB}		5.5 - V _{DO}	V
	Accuracy ⁽¹⁾	Nominal	T _J = 25°C	−0.5		0.5	%
		V _{IN} , I _{OUT} , and T	V _{OUT} + 0.5V ≤ V _{IN} ≤ 5.5V; 10mA ≤ I _{OUT} ≤ 250mA	−1	±0.5	1	
ΔV _{OUT(ΔVIN)}	Line regulation	(V _{OUT(nom)} + 0.5V) ≤ V _{IN} ≤ 5.5V	(V _{OUT(nom)} + 0.5V) ≤ V _{IN} ≤ 5.5V	0.06			%/V
ΔV _{OUT(ΔIOUT)}	Load regulation	1mA ≤ I _{OUT} ≤ 250mA	1mA ≤ I _{OUT} ≤ 250mA	0.002			%/mA
ΔV _{OUT(ΔIOUT)}	Load regulation	10mA ≤ I _{OUT} ≤ 250mA	10mA ≤ I _{OUT} ≤ 250mA	0.0008			%/mA
V _{DO}	Dropout voltage ⁽³⁾ (V _{IN} = V _{OUT(NOM)} - 0.1V)	I _{OUT} = 250mA		40		150	mV
Z _{O(DO)}	Output impedance in dropout	1.7V ≤ V _{IN} ≤ V _{OUT} + V _{DO}		0.25			Ω
I _{CL}	Output current limit	V _{OUT} = 0.9 × V _{OUT(nom)}		250	425	600	mA
I _{SC}	Short-circuit current	V _{OUT} = 0V		300			mA
I _{REV}	Reverse leakage current ⁽⁴⁾ (-I _{IN})	V _{EN} ≤ 0.5V, 0V ≤ V _{IN} ≤ V _{OUT}		0.1		10	μA
I _{GND}	Ground pin current	I _{OUT} = 10mA (I _Q)		400		550	μA
I _{GND}	Ground pin current	I _{OUT} = 250mA		650		950	μA
I _{SHDN}	Shutdown current (I _{GND})	V _{EN} ≤ 0.5V, V _{OUT} ≤ V _{IN} ≤ 5.5V	V _{EN} ≤ 0.5V, V _{OUT} ≤ V _{IN} ≤ 5.5V	0.02		1	μA
I _{FB}	Feedback pin current (TPS73201)			0.1		0.45	μA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I _{OUT} = 250mA		58			dB
		f = 10kHz, I _{OUT} = 250mA		37			
V _N	Output noise voltage, BW = 10Hz to 100kHz	C _{OUT} = 10μF, no C _{NR}		27 x V _{OUT}			μV _{RMS}
		C _{OUT} = 10μF, C _{NR} =0.01μF		8.5 x V _{OUT}			
V _{EN(high)}	EN pin high (enabled)			1.7		V _{IN}	V
V _{EN(low)}	EN pin low (shutdown)			0		0.5	V
I _{EN(high)}	Enable pin current (enabled)	V _{EN} = 5.5V		0.02		0.1	μA
T _{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160			°C
		Reset, temperature decreasing		140			

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7V, whichever is greater.

(2) TPS73201-Q1 is tested at $V_{OUT} = 2.5\text{V}$.

(3) V_{DO} is not measured for output versions with $V_{OUT(nom)} < 1.8\text{V}$, because minimum $V_{IN} = 1.7\text{V}$.

(4) Fixed-voltage versions only; refer to *Application Information* section for more information.

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	$V_{OUT} = 3\text{V}$, $R_L = 30\Omega$, $C_{OUT} = 1\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$		600		μs

5.8 Typical Characteristics

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

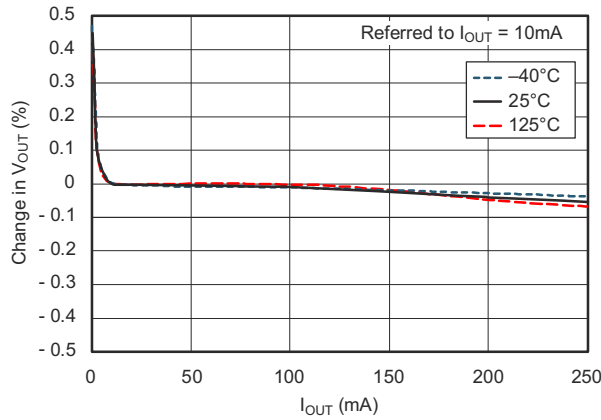


Figure 5-1. Load Regulation

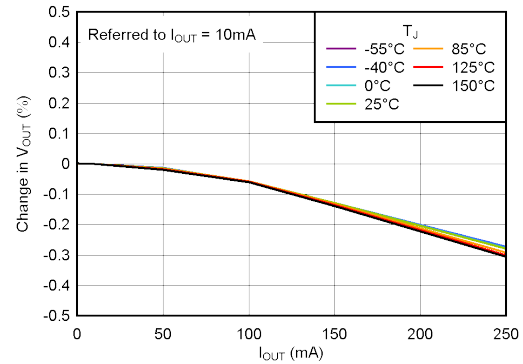


Figure 5-2. Load Regulation

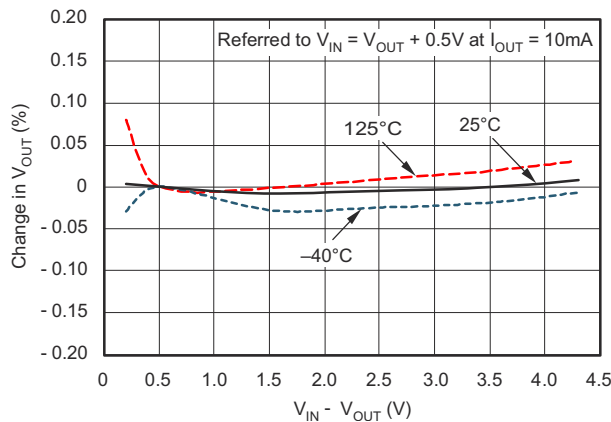


Figure 5-3. Line Regulation

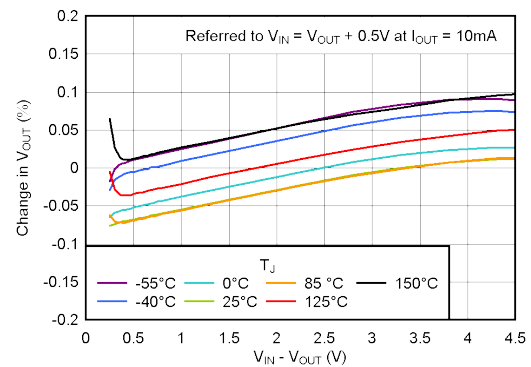


Figure 5-4. Line Regulation

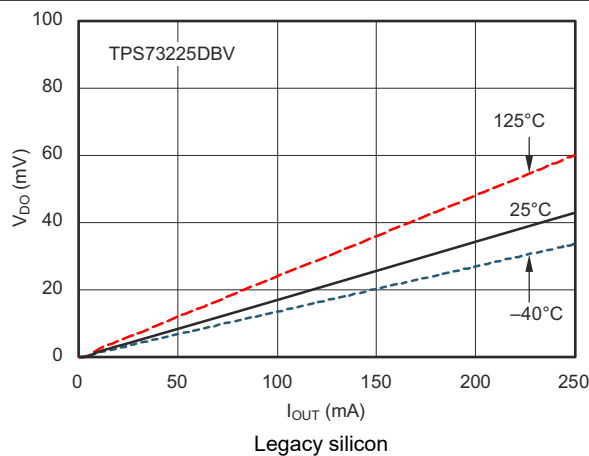


Figure 5-5. Dropout Voltage vs Output Current

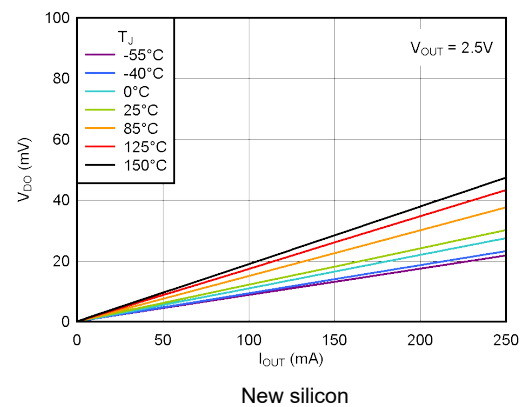


Figure 5-6. Dropout Voltage vs Output Current

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{nom})} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

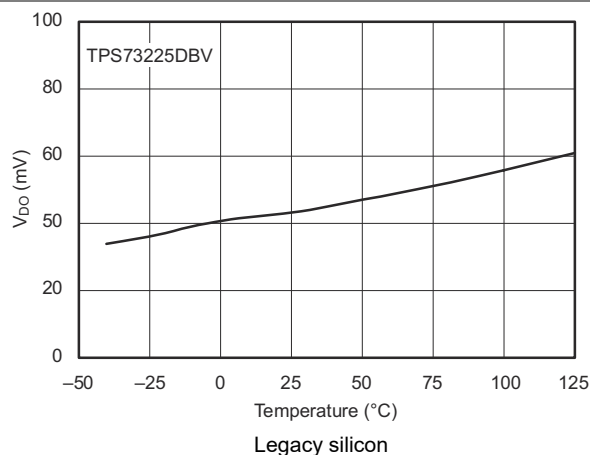


Figure 5-7. Dropout Voltage vs Temperature

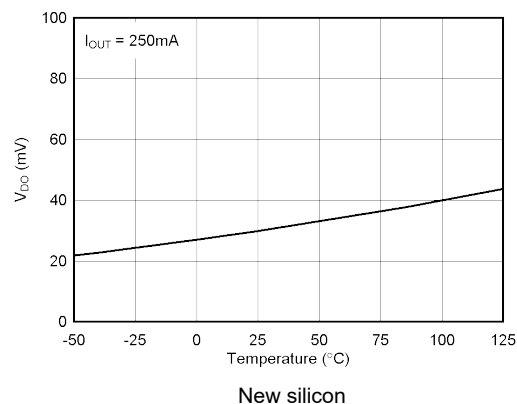


Figure 5-8. Dropout Voltage vs Temperature

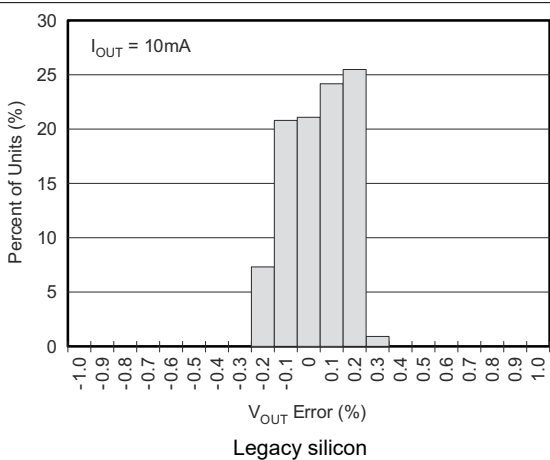


Figure 5-9. Output Voltage Accuracy Histogram

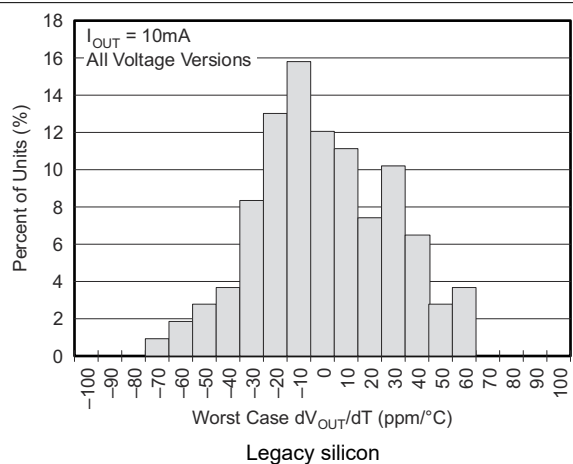


Figure 5-10. Output Voltage Drift Histogram

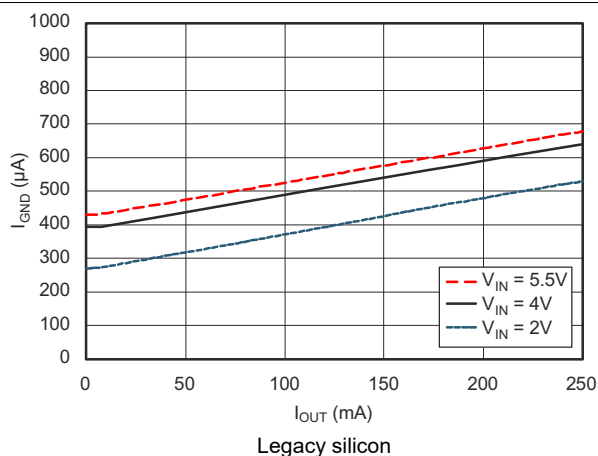


Figure 5-11. Ground Pin Current vs Output Current

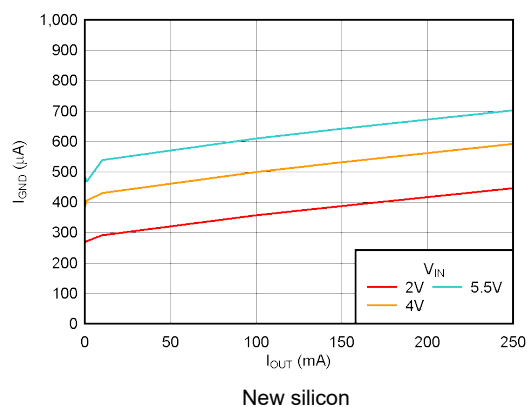


Figure 5-12. Ground Pin Current vs Output Current

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

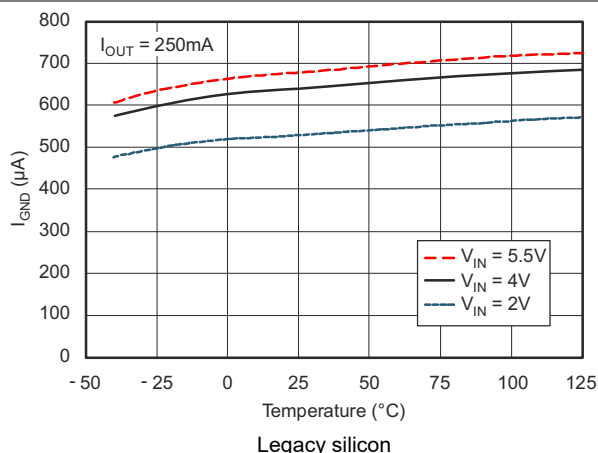


Figure 5-13. Ground Pin Current vs Temperature

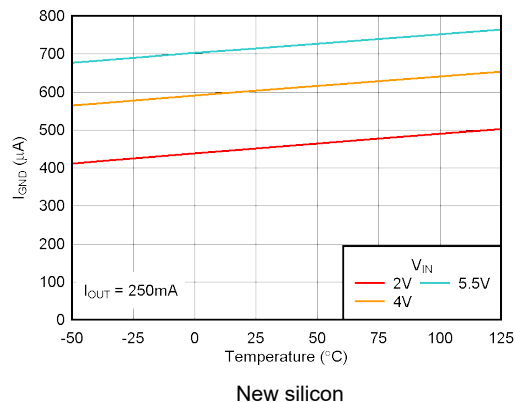


Figure 5-14. Ground Pin Current vs Temperature

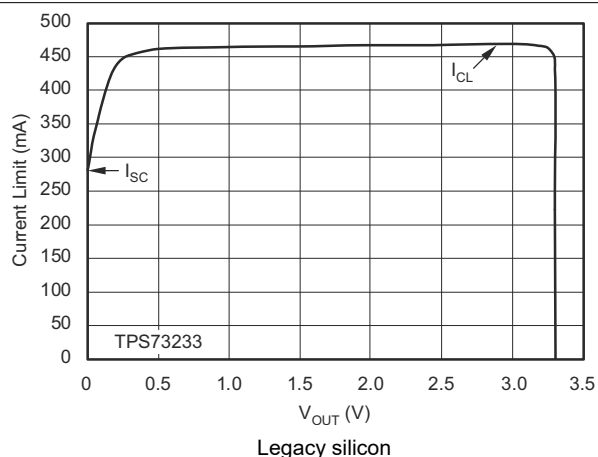


Figure 5-15. Current Limit vs V_{OUT} (FOLDBACK)

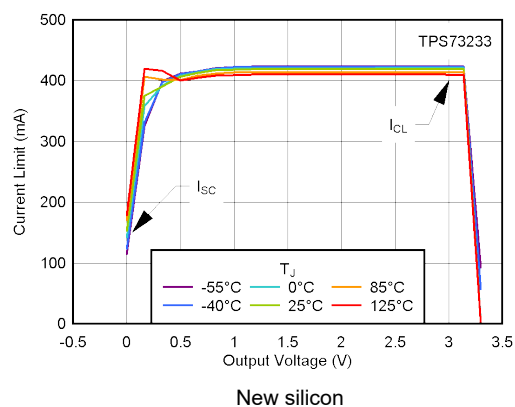


Figure 5-16. Current Limit vs V_{OUT} (Foldback)

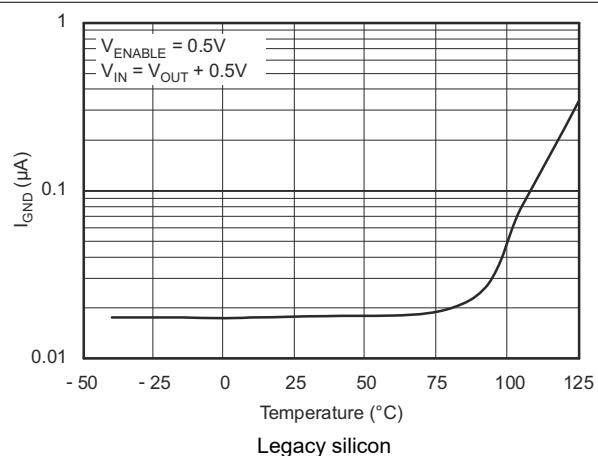


Figure 5-17. Ground Pin Current in Shutdown vs Temperature

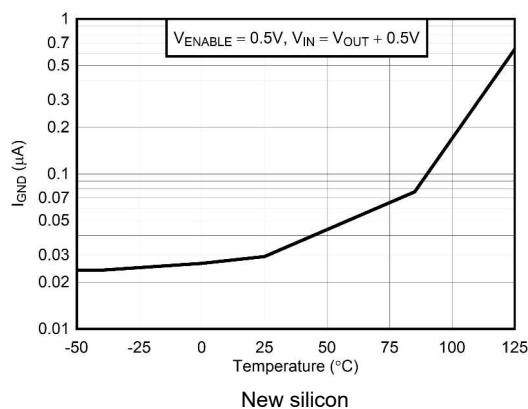


Figure 5-18. Ground Pin Current in Shutdown vs Temperature

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{nom})} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

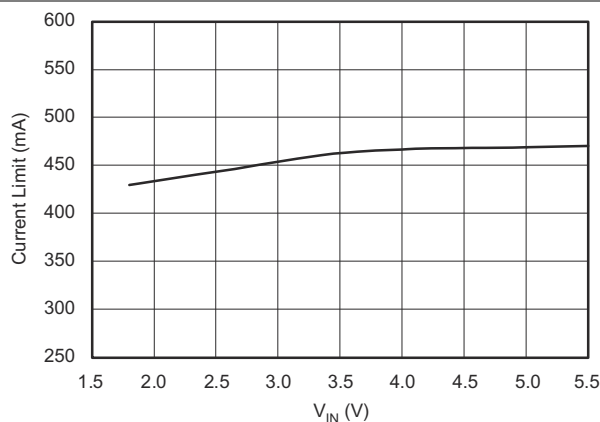


Figure 5-19. Current Limit vs V_{IN}

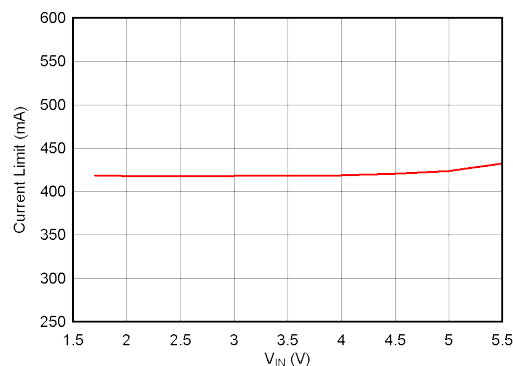


Figure 5-20. Current Limit vs V_{IN}

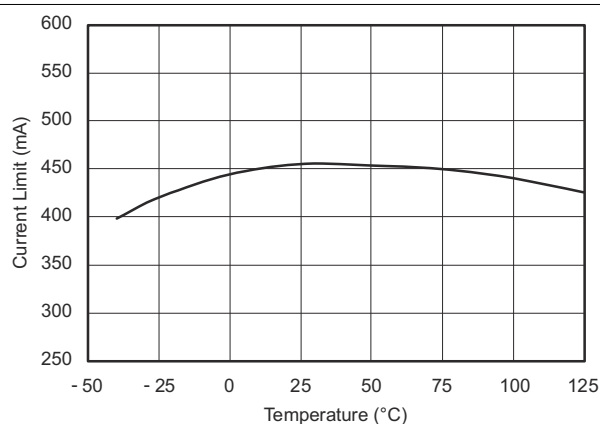


Figure 5-21. Current Limit vs Temperature

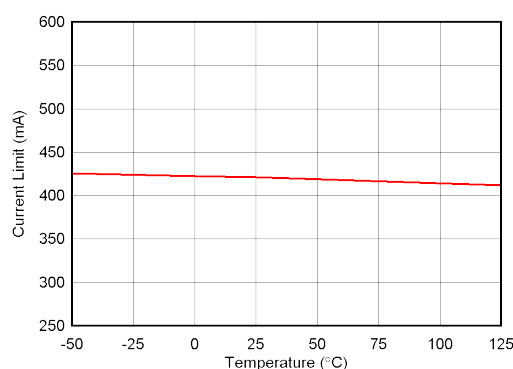


Figure 5-22. Current Limit vs Temperature

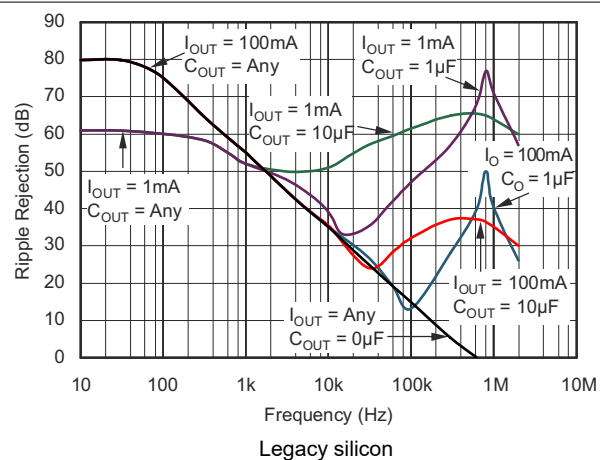


Figure 5-23. PSRR (Ripple Rejection) vs Frequency

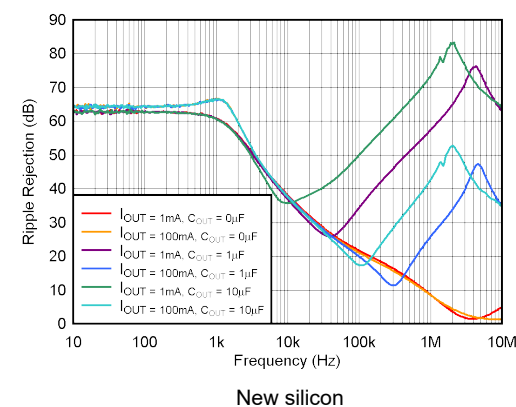


Figure 5-24. PSRR (Ripple Rejection) vs Frequency

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{nom})} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

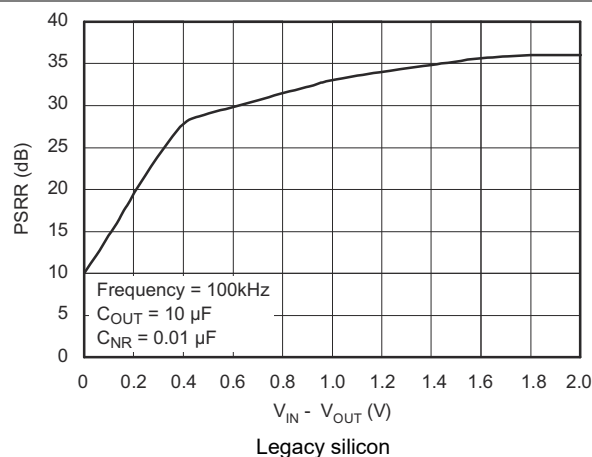


Figure 5-25. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

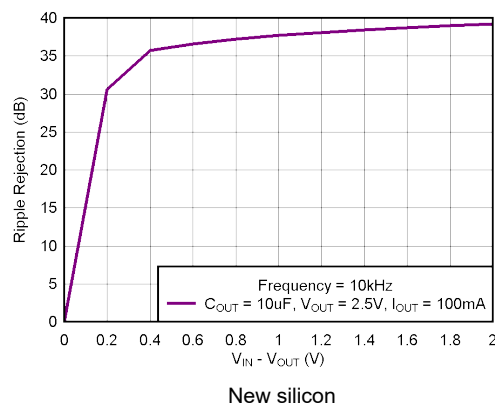


Figure 5-26. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

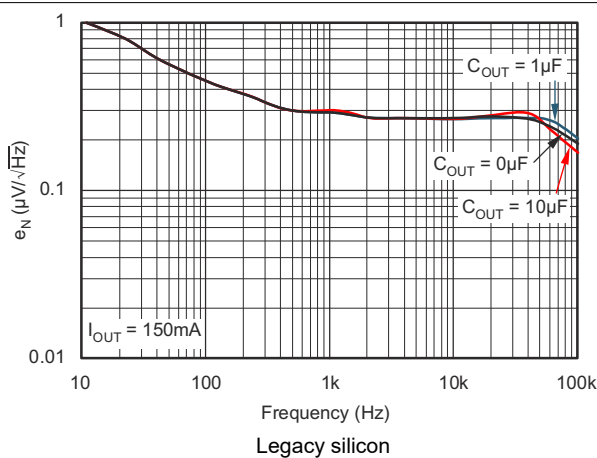


Figure 5-27. Noise Spectral Density vs $C_{NR} = 0\text{ }\mu\text{F}$

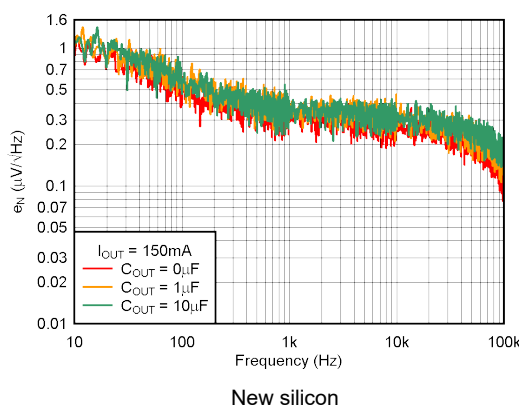


Figure 5-28. Noise Spectral Density $C_{NR} = 0\text{ }\mu\text{F}$

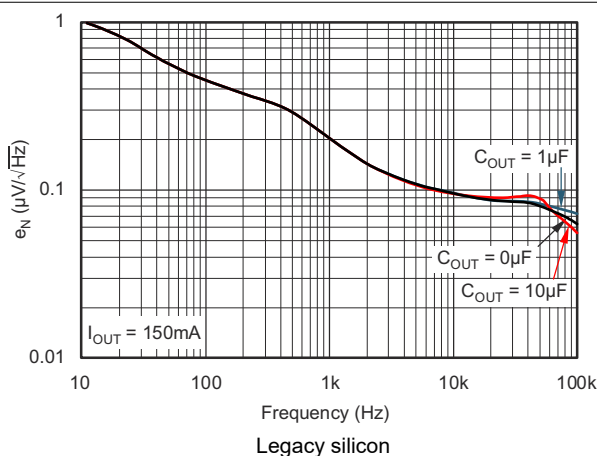


Figure 5-29. Noise Spectral Density vs $C_{NR} = 0.01\text{ }\mu\text{F}$

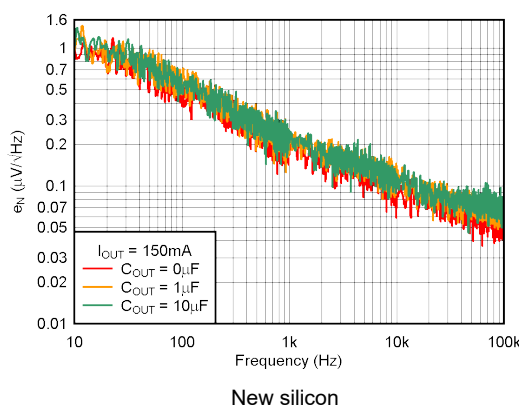


Figure 5-30. Noise Spectral Density $C_{NR} = 0.01\text{ }\mu\text{F}$

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

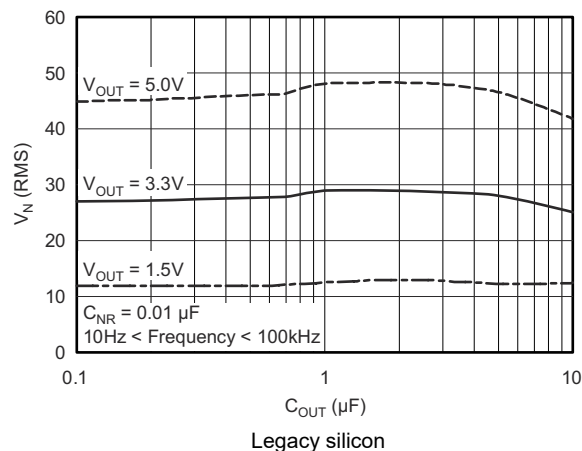


Figure 5-31. RMS Noise Voltage vs C_{OUT}

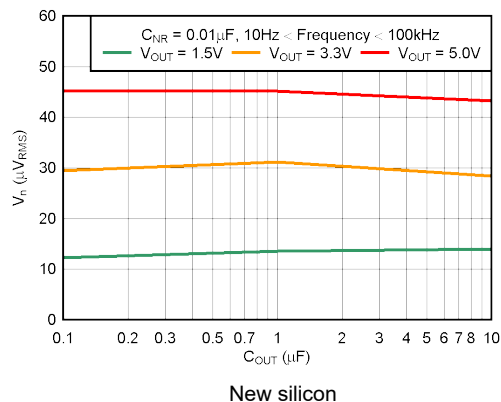


Figure 5-32. RMS Noise Voltage vs C_{OUT}

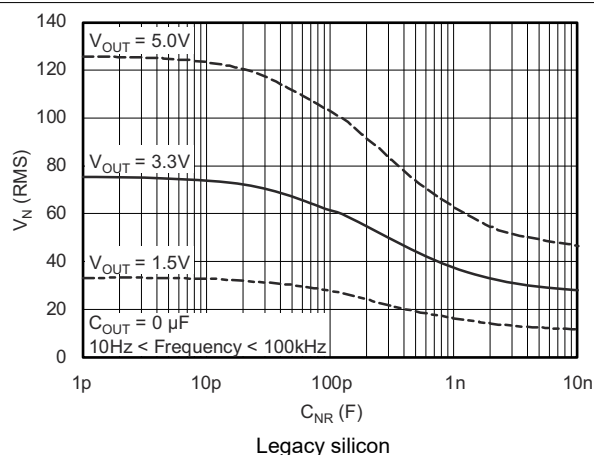


Figure 5-33. RMS Noise Voltage vs C_{NR}

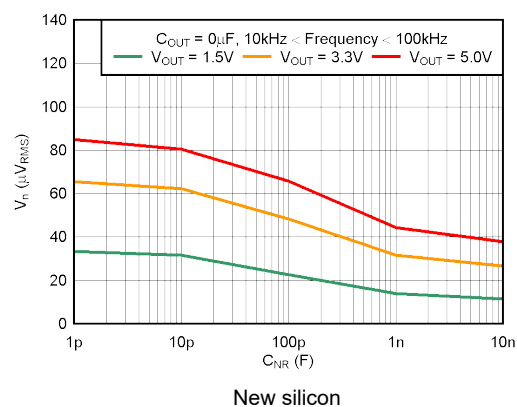


Figure 5-34. RMS Noise Voltage vs C_{NR}

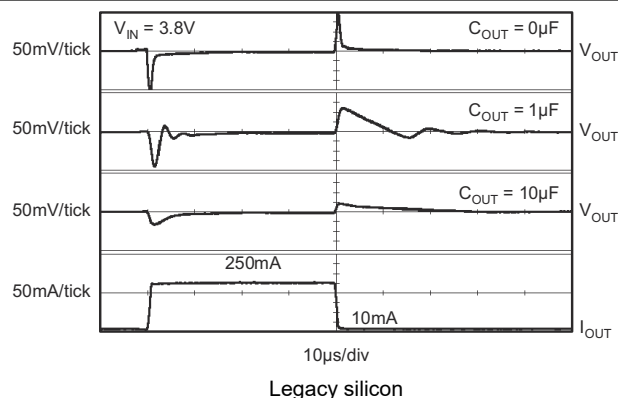


Figure 5-35. TPS73233-Q1 – Load Transient Response

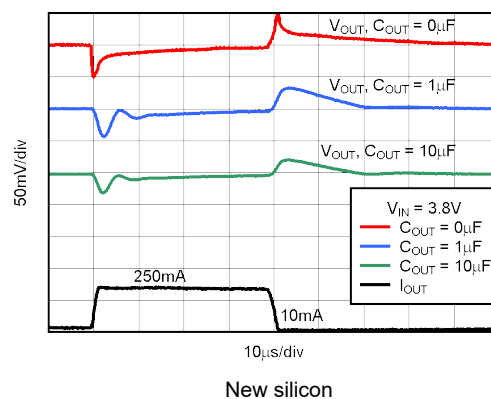


Figure 5-36. TPS73233-Q1 Load Transient Response

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

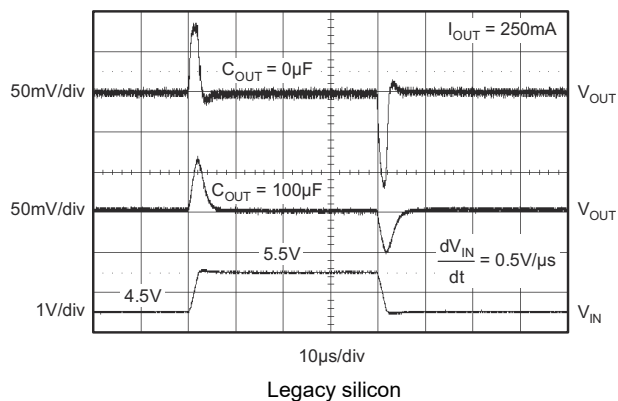


図 5-37. TPS73233-Q1 – Line Transient Response

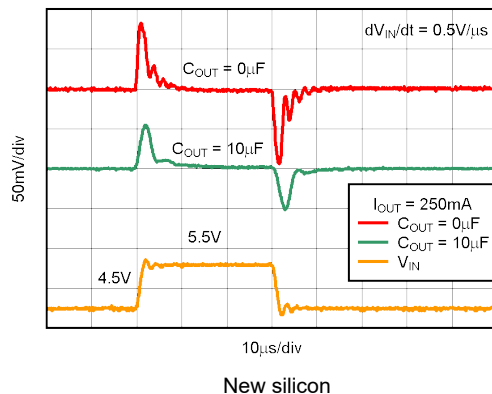


図 5-38. TPS73233-Q1 Line Transient Response

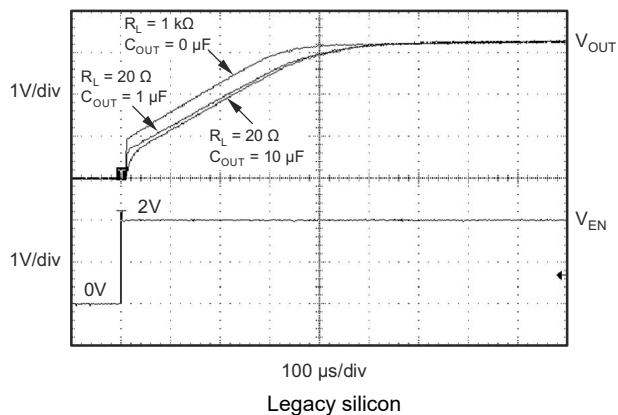


図 5-39. TPS73233-Q1 – Turnon Response

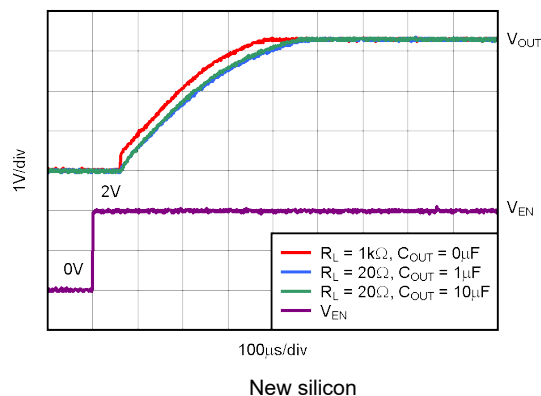


図 5-40. TPS73233-Q1 Turn-On Response

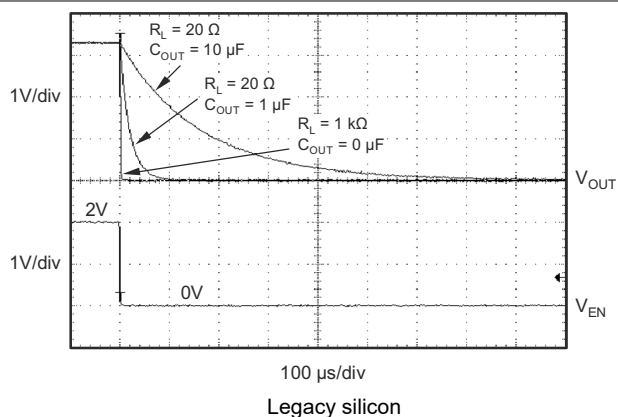


図 5-41. TPS73233-Q1 – Turnoff Response

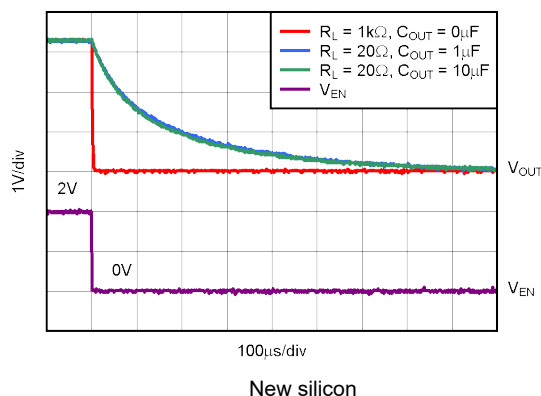


図 5-42. TPS73233-Q1 Turn-Off Response

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

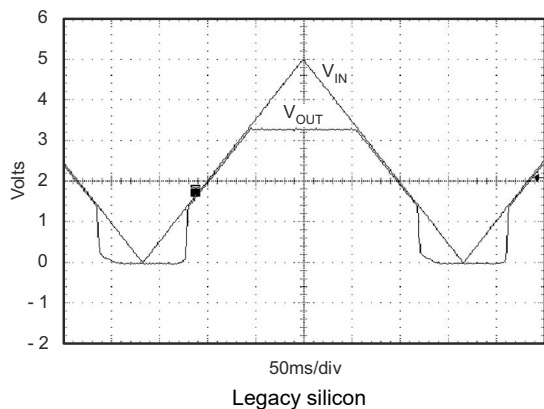


FIG 5-43. TPS73233-Q1 – Power Up and Power Down

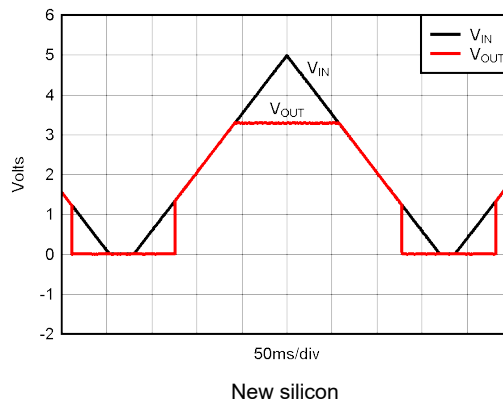


FIG 5-44. TPS73233-Q1 Power-Up and Power-Down

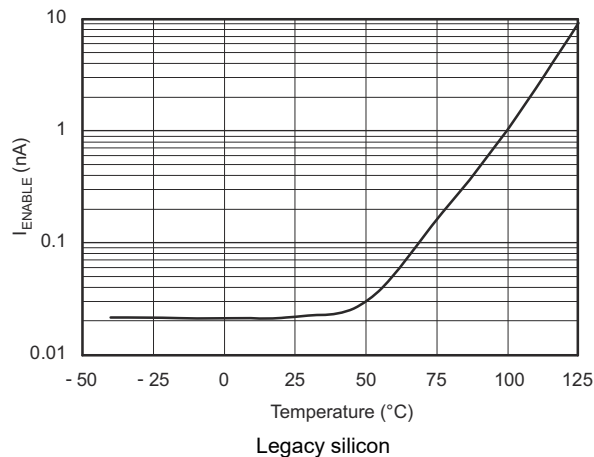


FIG 5-45. I_{ENABLE} vs Temperature

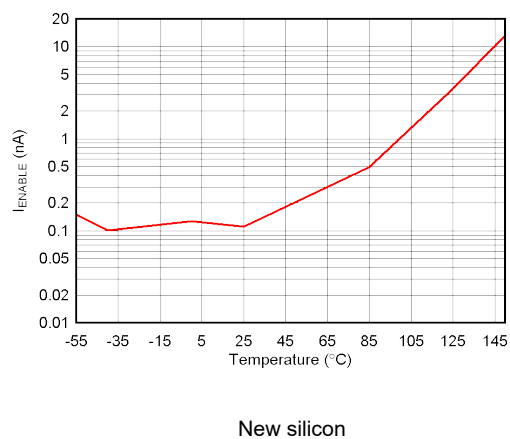


FIG 5-46. I_{ENABLE} vs Temperature

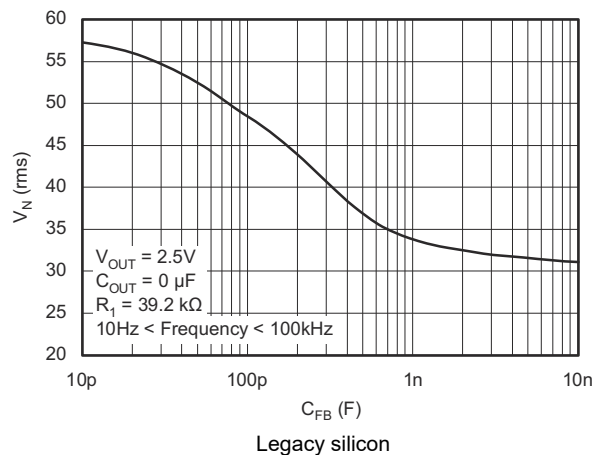


FIG 5-47. TPS73201-Q1 – RMS Noise Voltage vs C_{ADJ}

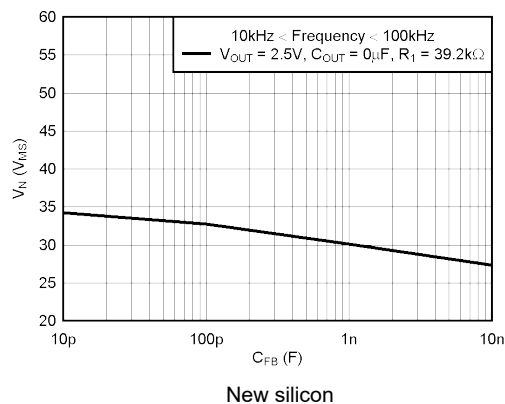


FIG 5-48. TPS73201-Q1 RMS Noise Voltage vs C_{FB}

5.8 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 1.7\text{ V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted)

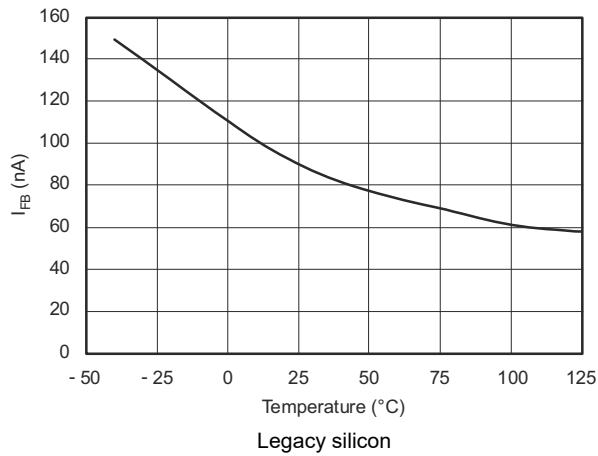


図 5-49. TPS73201-Q1 – I_{FB} vs Temperature

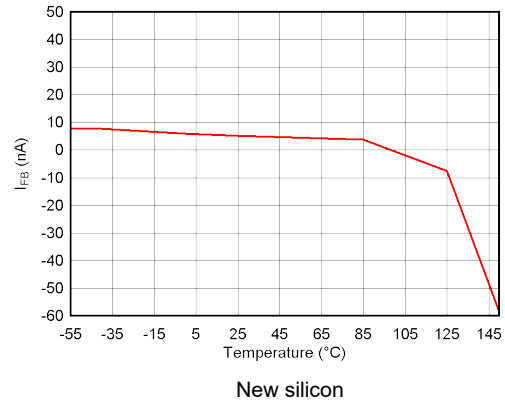


図 5-50. TPS73201-Q1 I_{FB} vs Temperature

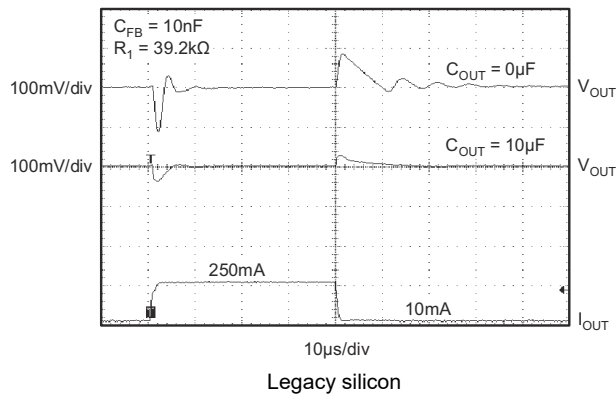


図 5-51. TPS73201-Q1 – Load Transient, Adjustable Version

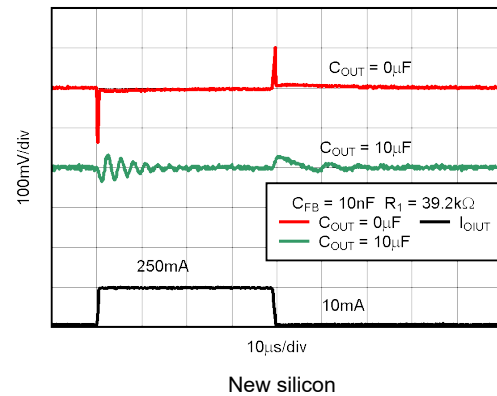


図 5-52. TPS73201-Q1 Load Transient, Adjustable Version

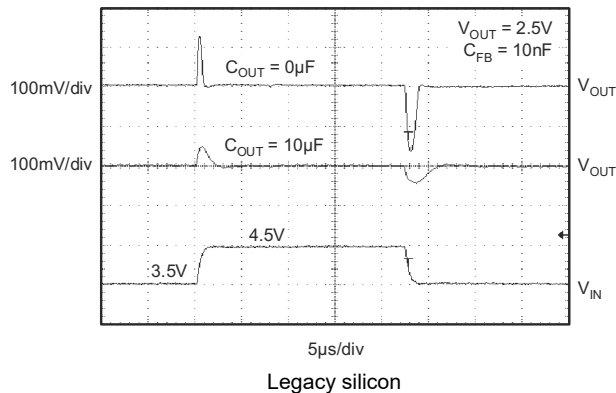


図 5-53. TPS73201-Q1 – Line Transient, Adjustable Version

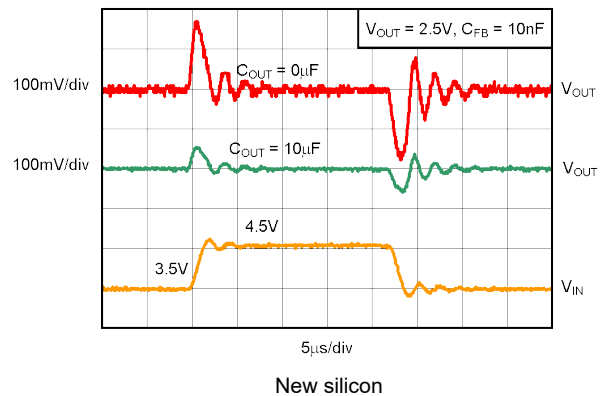


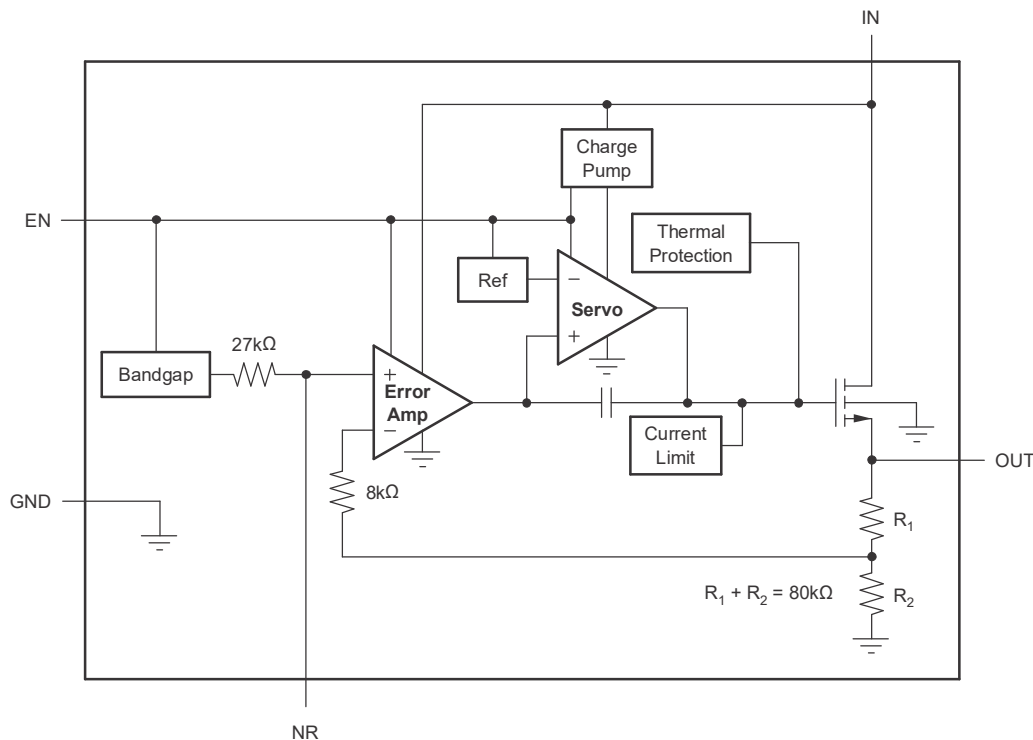
図 5-54. TPS73201-Q1 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS732-Q1 low-dropout linear regulator devices operate with an input voltage down to 1.7 V and support output voltages down to 1.2 V while sourcing up to 250 mA of load current. These linear regulators use an NMOS pass element with an integrated 4-MHz charge pump to provide a dropout voltage of less than 150 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS732-Q1 family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown. The TPS732-Q1 family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. The low noise output featured by the TPS732-Q1 family makes the device well-suited for powering VCOs or any other noise-sensitive load.

6.2 Functional Block Diagram



Fixed voltage version.

6.3 Feature Description

6.3.1 Internal Current Limit

The TPS732-Q1 internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See [Figure 5-15](#).

6.3.2 Shutdown

The enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (maximum) turns the regulator off and drops the ground pin current to approximately 10 nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN} . When a pullup resistor is used, and operation down to 1.8 V is required, use pullup resistor values below 50 kΩ.

6.3.3 Dropout Voltage

The TPS732-Q1 family of devices uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS732-Q1 family of devices requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN} - V_{OUT}$ above this line provide normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with $(V_{IN} - V_{OUT})$ close to dc dropout levels], the TPS732-Q1 family of devices can take a couple of hundred microseconds to return to the specified regulation accuracy.

6.3.4 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μ F) from the output pin to ground reduces undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB} , from the output to the adjust pin also improves the transient response.

The TPS732-Q1 family of devices does not have active pulldown when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by 式 1 and 式 2:

(Fixed voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80 \text{ k}\Omega} \quad (1)$$

(Adjustable voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80 \text{ k}\Omega \parallel (R_1 + R_2)} \quad (2)$$

6.3.5 Reverse Current

The NMOS pass element of the TPS732-Q1 family of devices provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element can be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-k Ω internal resistor divider to ground (see the [Functional Block Diagram](#) and [Figure 7-3](#)).

For the TPS73201-Q1, reverse current can flow when V_{FB} is more than 1 V above V_{IN} .

6.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, protecting the device from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732-Q1 family of devices is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS732-Q1 family of devices into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The TPS732-Q1 family of devices require an input voltage of at least 1.7V to function properly and attempt to maintain regulation.

When operating the device near 5.5V, take care to suppress any transient spikes that can exceed the 6V absolute maximum voltage rating. The device must never operate at a DC voltage greater than 5.5V.

7 Application and Implementation

注

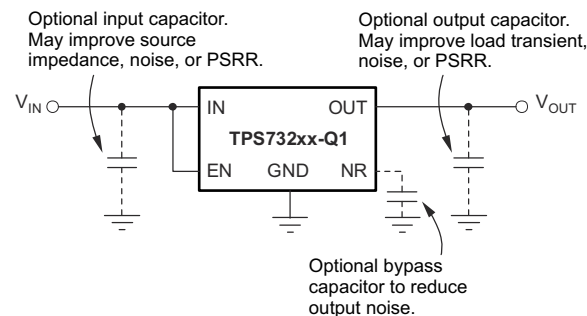
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7.1 Application Information

The TPS732-Q1 belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732-Q1 family of devices ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

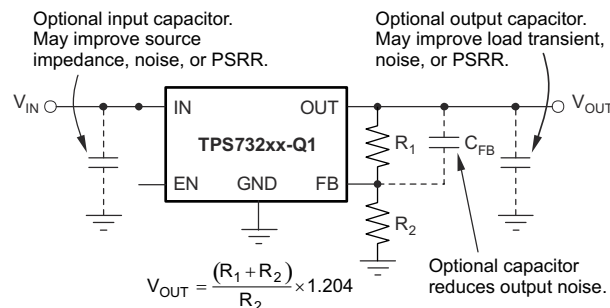
7.2 Typical Application

図 7-1 shows the basic circuit connections for the fixed voltage models. 図 7-2 gives the connections for the adjustable output version (TPS73201-Q1).



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図 7-1. Typical Application Circuit for Fixed-Voltage Versions

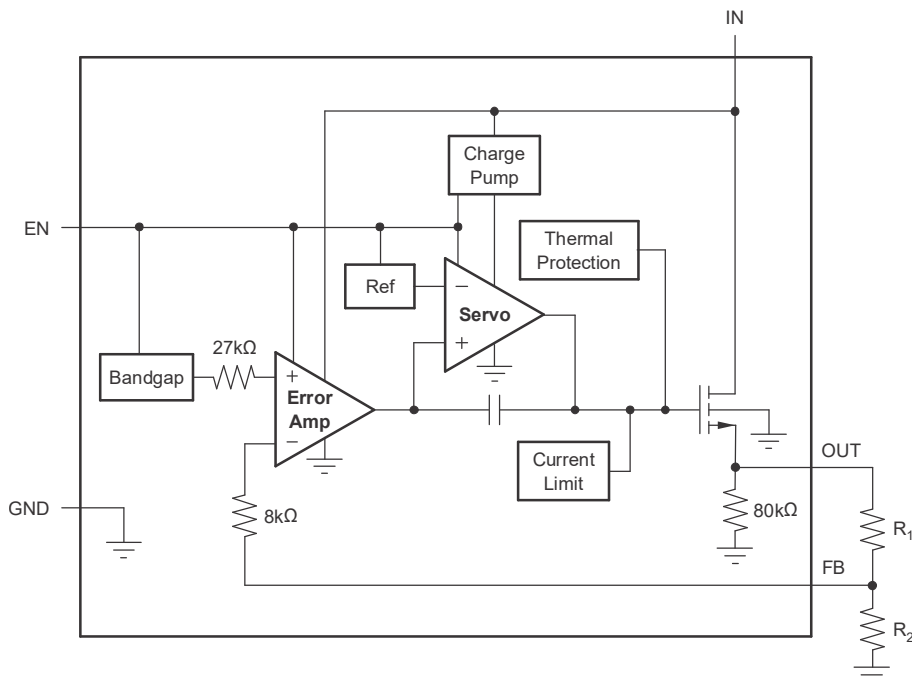


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図 7-2. Typical Application Circuit for Adjustable-Voltage Versions

7.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in [Figure 7-2](#). Sample resistor values for common output voltages are shown in [Table 7-1](#). For best accuracy, make the parallel combination of R_1 and R_2 approximately 19 k Ω .



$$V_{OUT} = (R_1 + R_2) / R_2 \times 1.204$$

$R_1 \parallel R_2 \cong 19 \text{ k}\Omega$ for best accuracy.

Figure 7-3. Adjustable Voltage Version

Table 7-1. Standard 1% Resistor Values for Common Output Voltages

V _{OUT}	R ₁	R ₂
1.2 V	Short	Open
1.5 V	23.2 k Ω	95.3 k Ω
1.8 V	28 k Ω	56.2 k Ω
2.5 V	39.2 k Ω	36.5 k Ω
2.8 V	44.2 k Ω	33.2 k Ω
3 V	46.4 k Ω	30.9 k Ω
3.3 V	52.3 k Ω	30.1 k Ω
5 V	78.7 k Ω	24.9 k Ω

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732-Q1 family of devices does not require an output capacitor for stability and has maximum phase margin with no capacitor. The devices are designed to be stable for all available types and values of capacitors. In applications where $V_{IN} - V_{OUT} < 0.5V$ and multiple low ESR capacitors are in parallel, ringing can occur when the product of C_{OUT} and total ESR drops below $50nF \times \Omega$. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the TPS732-Q1 family of devices and generates approximately $32 \mu V_{RMS}$ (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32 \mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32 \mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (3)$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (4)$$

where

- C_{NR} does not exist

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR} , is connected from NR to ground. For $C_{NR} = 10$ nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (5)$$

where

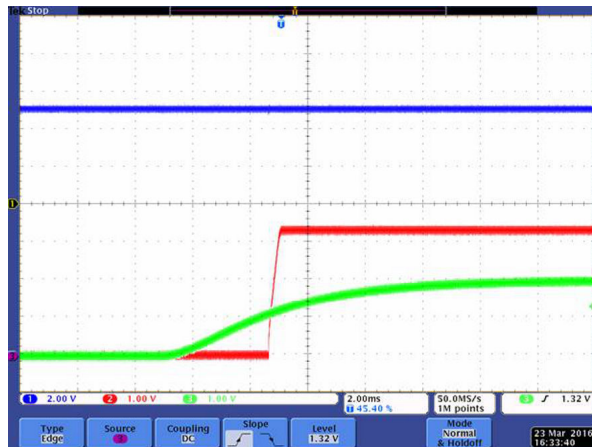
- $C_{NR} = 10$ nF

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in [Typical Characteristics](#).

The TPS73201-Q1 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB} , from the output to the FB pin reduces output noise and improve load transient performance.

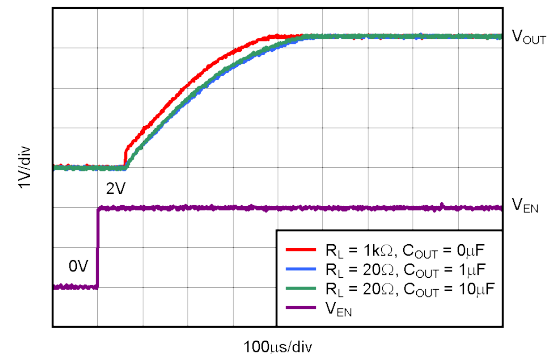
The TPS732-Q1 family of devices uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT} . The charge pump generates approximately 250 µV of switching noise at approximately 2 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

7.2.3 Application Curves



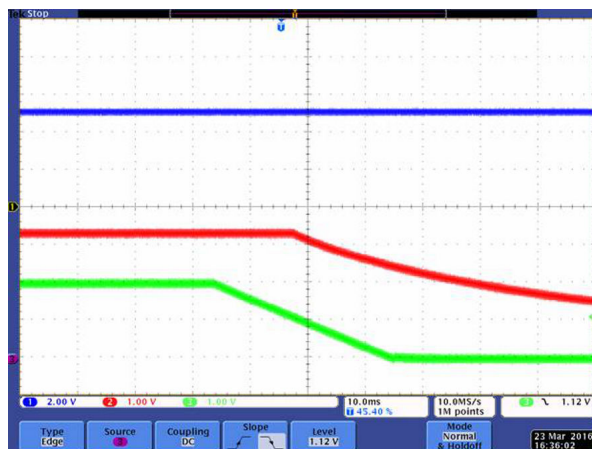
Legacy silicon

图 7-4. Start-Up



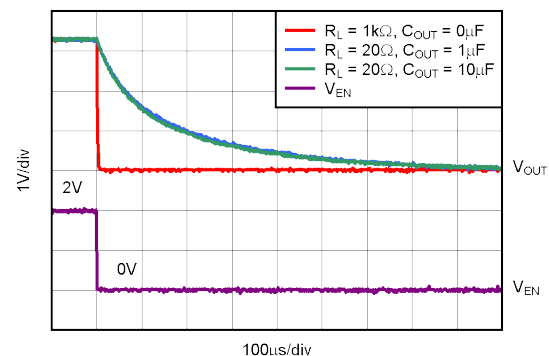
New silicon

図 7-5. Start-up



Legacy silicon

❌ 7-6. Shutdown



New silicon

7-7. Shutdown

7.3 Power Supply Recommendations

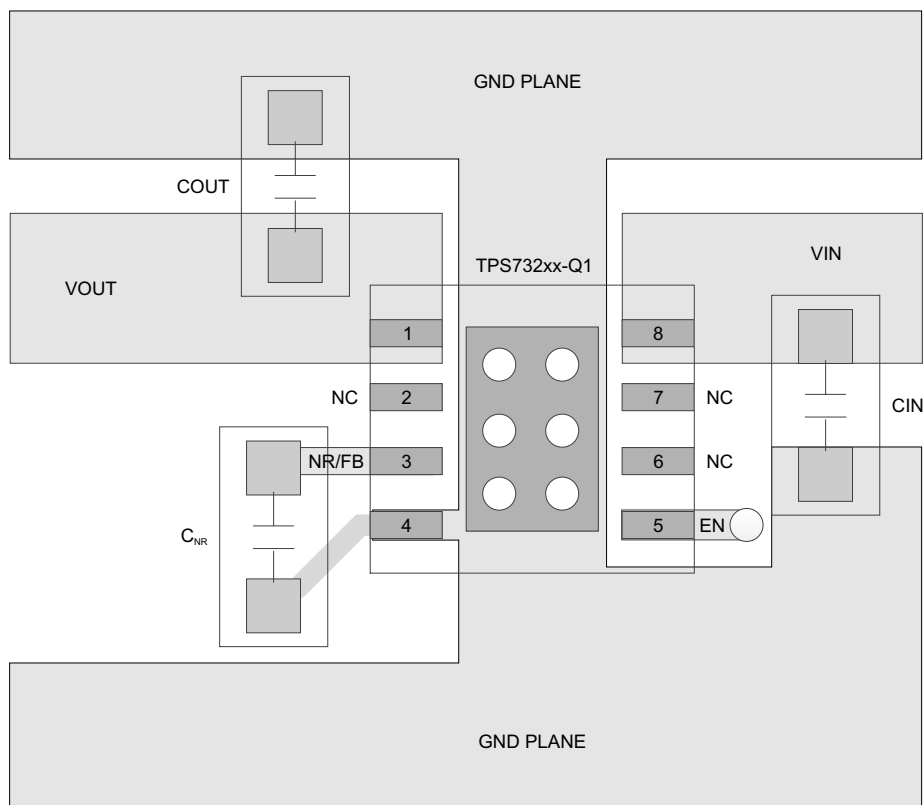
These devices are designed to operate from an input voltage supply range from 1.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, design the PCB with ground plane connections for V_{IN} and V_{OUT} capacitors, and the ground plane connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

7.4.2 Layout Example



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☒ 7-8. Fixed Output Voltage Option Layout (DRB Package)

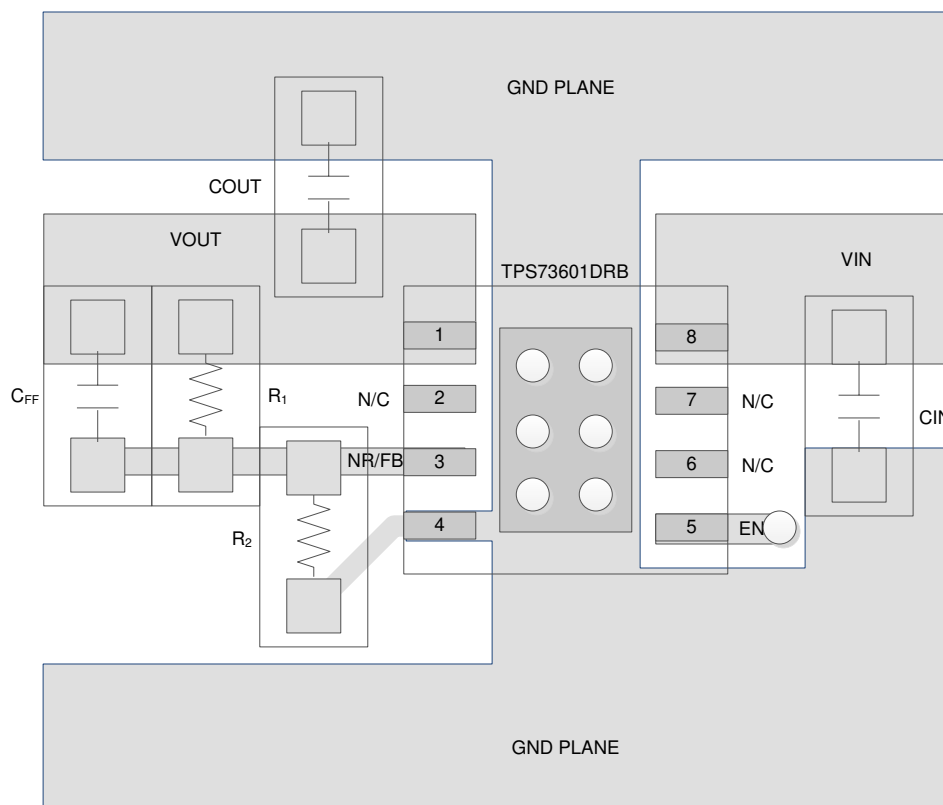


図 7-9. Adjustable Output Voltage Option Layout (DRB Package)

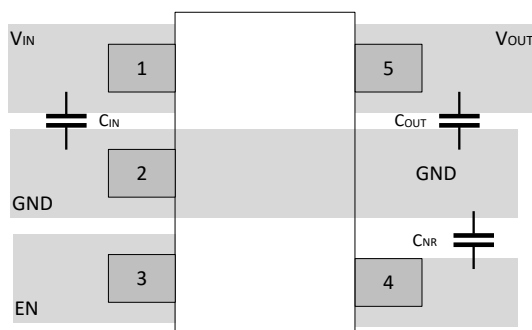
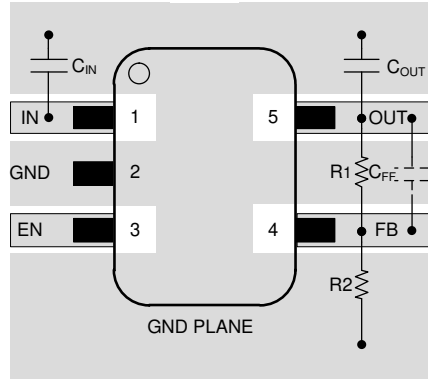
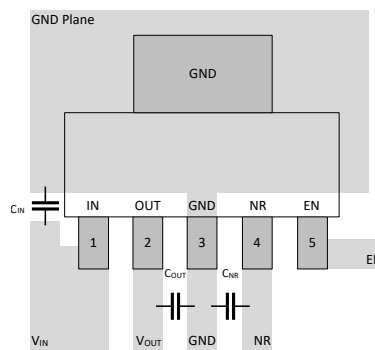


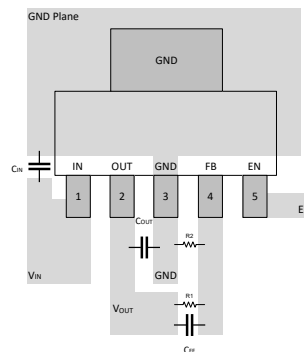
図 7-10. Layout Example for the DBV Package Fixed Version



7-11. Layout Example for the DBV Package Adjustable Version



7-12. Layout Example for the DCQ Package Fixed Version



7-13. Layout Example for the DCQ Package Adjustable Version

7.4.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.4 Package Mounting

Solder pad footprint recommendations for the TPS732-Q1 family of devices are presented in the *Solder Pad Recommendations for Surface-Mount Devices* ([SBFA015](#)) application bulletin.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Device Nomenclature

表 8-1. Ordering Information

PRODUCT	DESCRIPTION ⁽¹⁾
TPS732xxQyyy(M3)Q1	xx is the nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable ⁽²⁾). Q indicates that the device is a grade-1 device in accordance with the AEC-Q100 standard. yyy is the package designator. z is the package quantity. M3 is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the <i>legacy silicon</i> (CSO: DLN) or the <i>new silicon</i> (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document. Q1 indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

(2) For fixed 1.20V operation, tie FB to OUT.

8.1.2 Related Documentation

For related documentation see the following:

Solder Pad Recommendations for Surface-Mount Devices, [SBFA015](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (April 2016) to Revision G (December 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• 現在のファミリのフォーマットに合わせてドキュメント全体を変更.....	1
• ドキュメントに M3 デバイスを追加.....	1

Changes from Revision E (August 2013) to Revision F (April 2016)	Page
• 「製品情報」表、目次、「仕様」セクション、「ESD 定格」表、「推奨動作条件」表、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Changes from Revision D (March 2009) to Revision E (August 2013)	Page
• データシートから TPS73215-Q1、TPS73216-Q1、TPS73218-Q1、TPS73230-Q1、TPS73233-Q1、および TPS73250-Q1 を削除。.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73201QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJOQ
TPS73201QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJOQ
TPS73201QDRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PSAQ
TPS73201QDRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PSAQ
TPS73218QDCQRM3Q1	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	73218Q
TPS73218QDCQRM3Q1.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	73218Q
TPS73218QDCQRQ1	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73218Q
TPS73218QDCQRQ1.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73218Q
TPS73250QDCQRQ1	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73250Q
TPS73250QDCQRQ1.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	73250Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS732-Q1 :

- Catalog : [TPS732](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

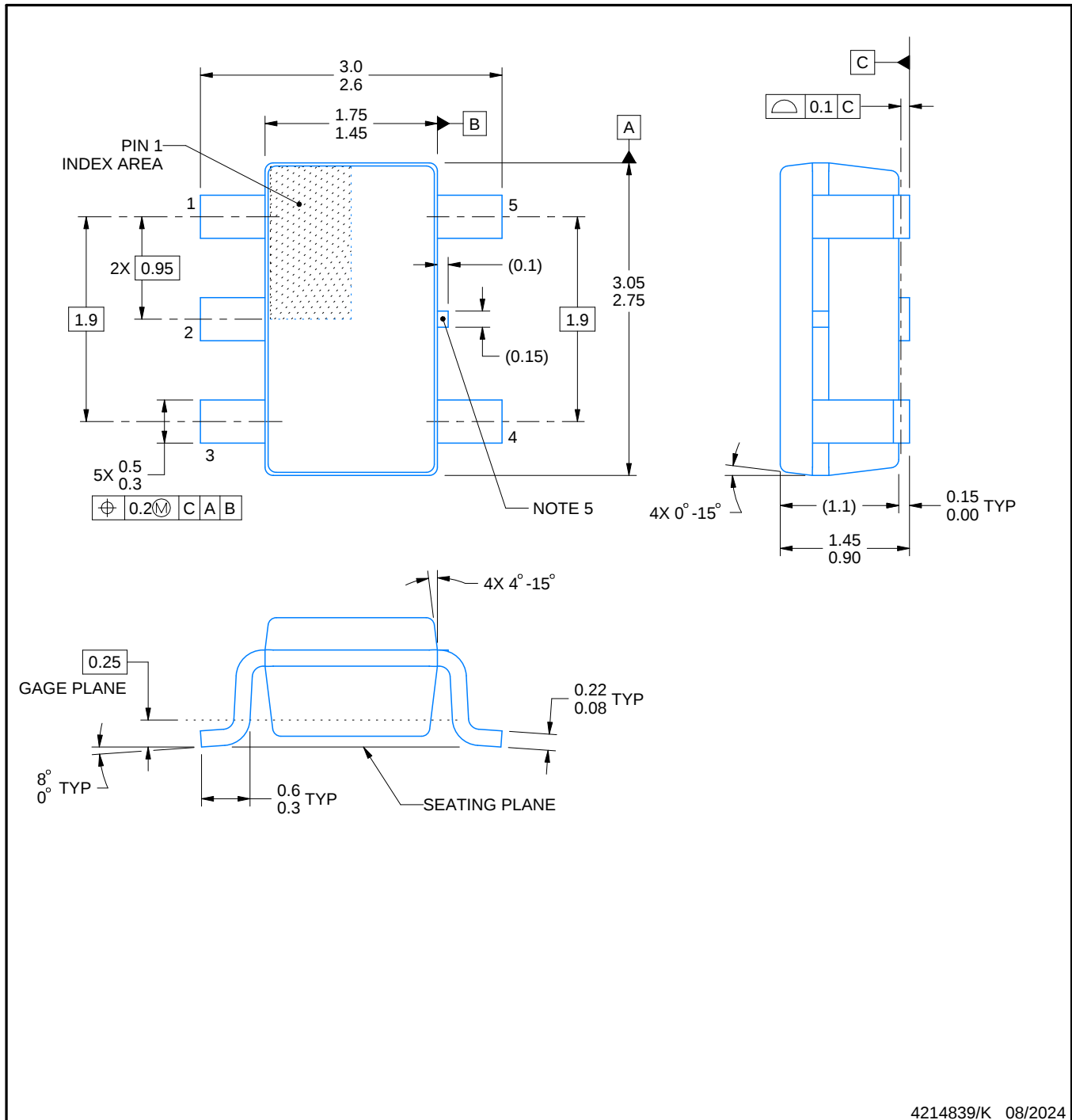


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73201QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

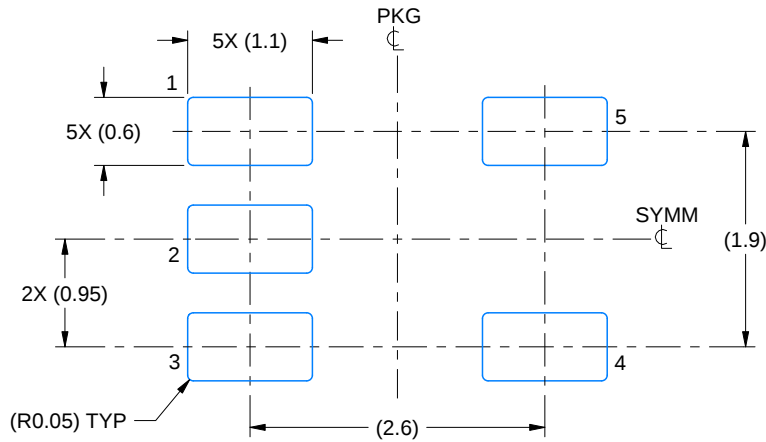
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

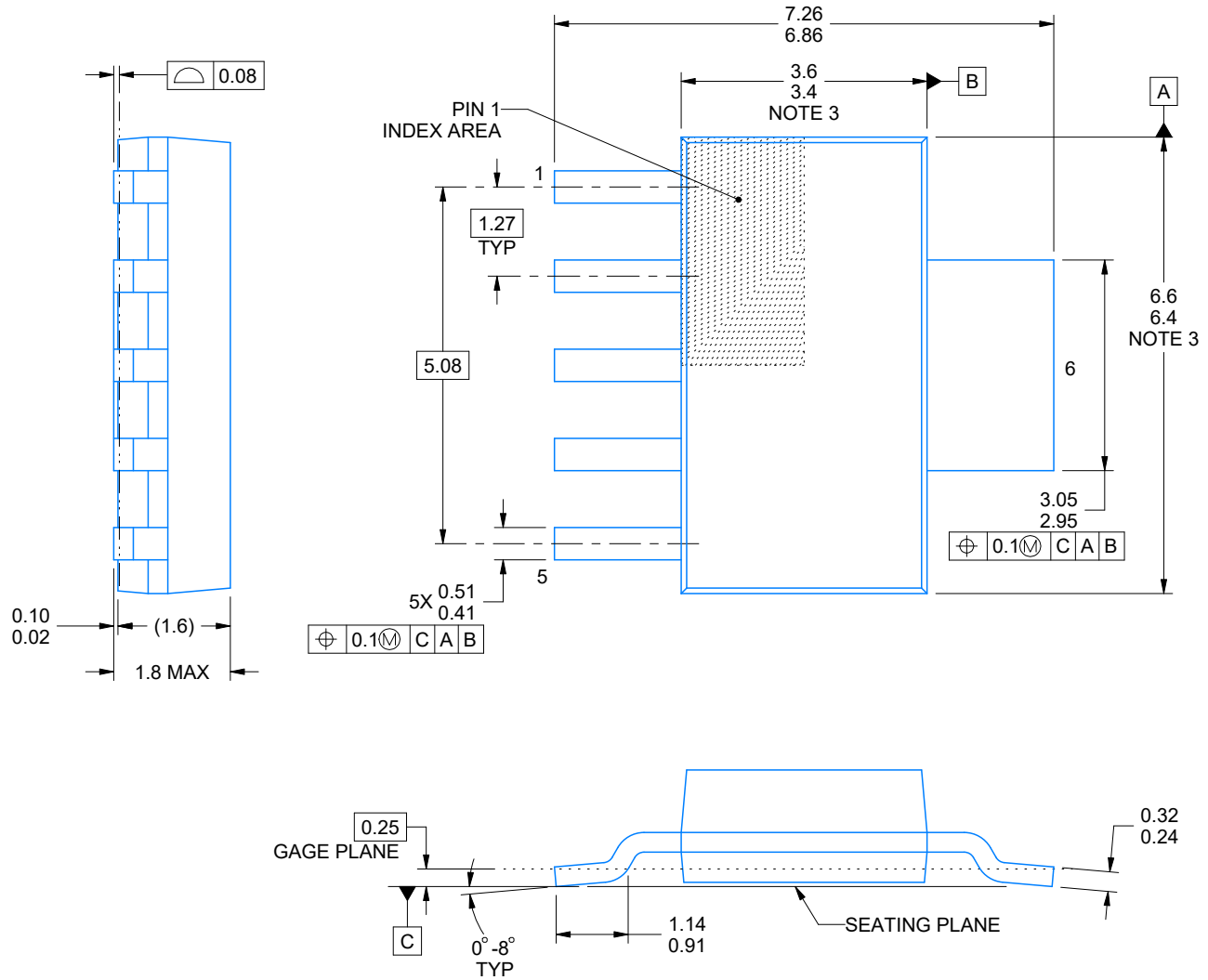
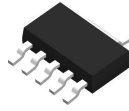


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

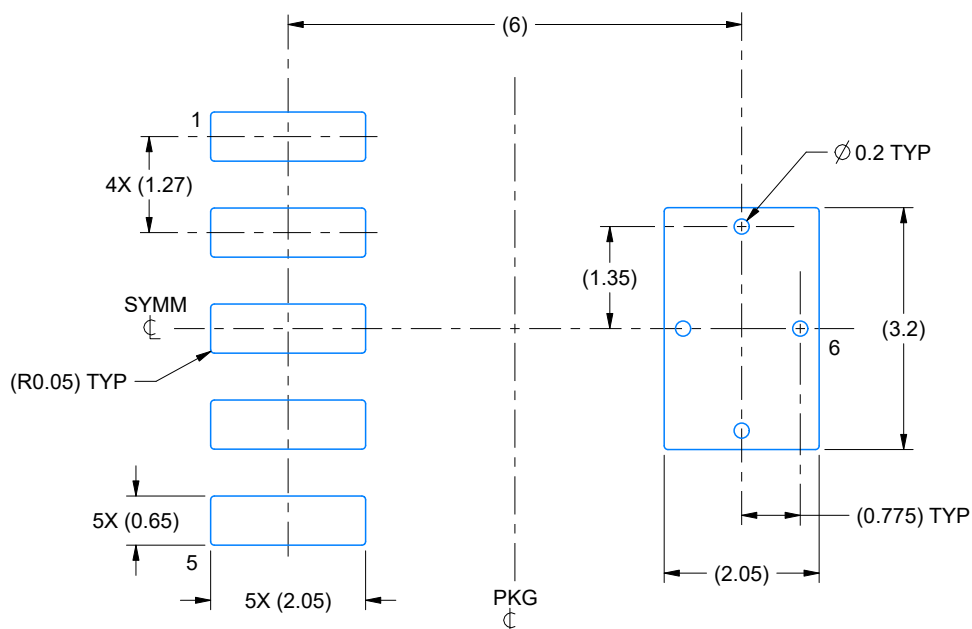
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



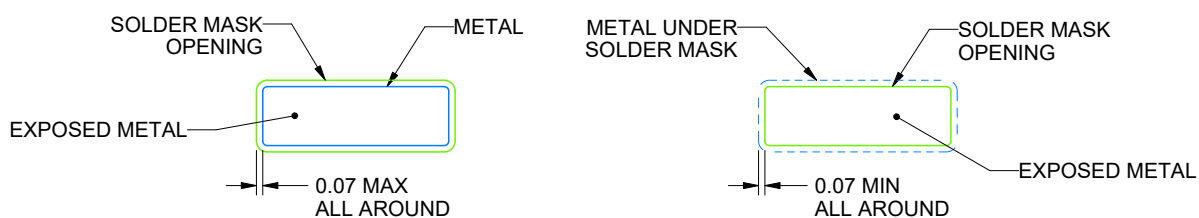
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

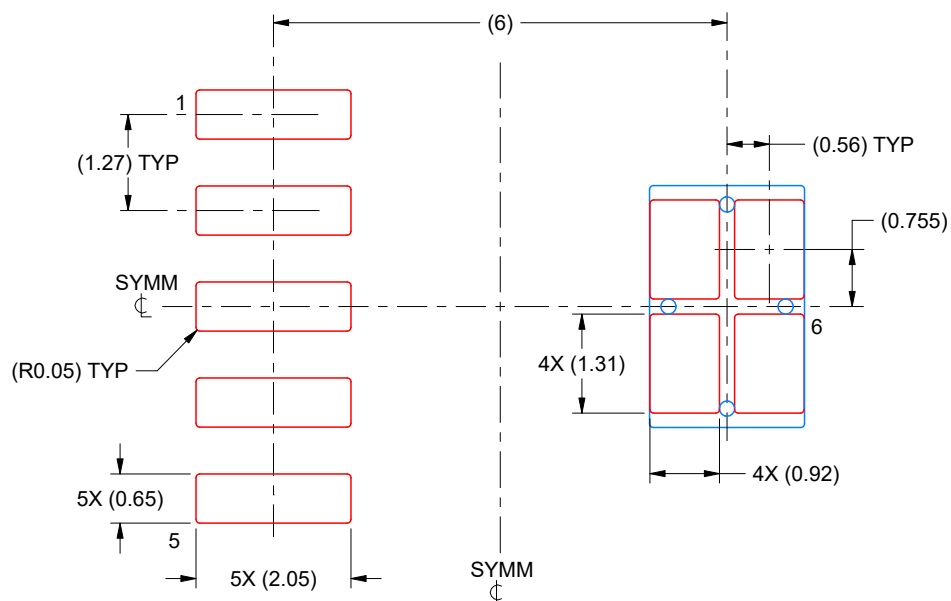
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

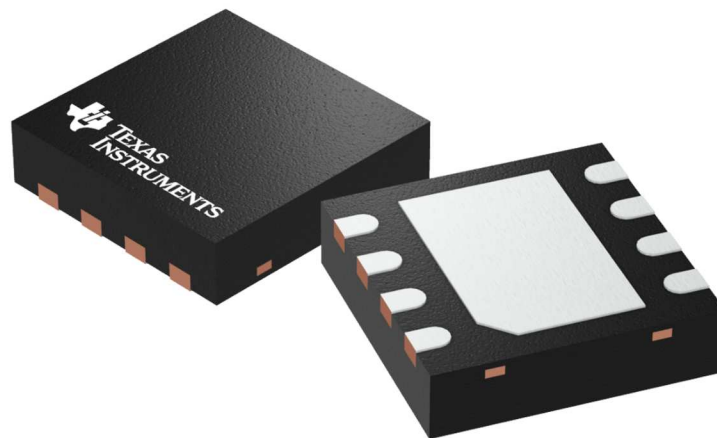
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRB 8

GENERIC PACKAGE VIEW

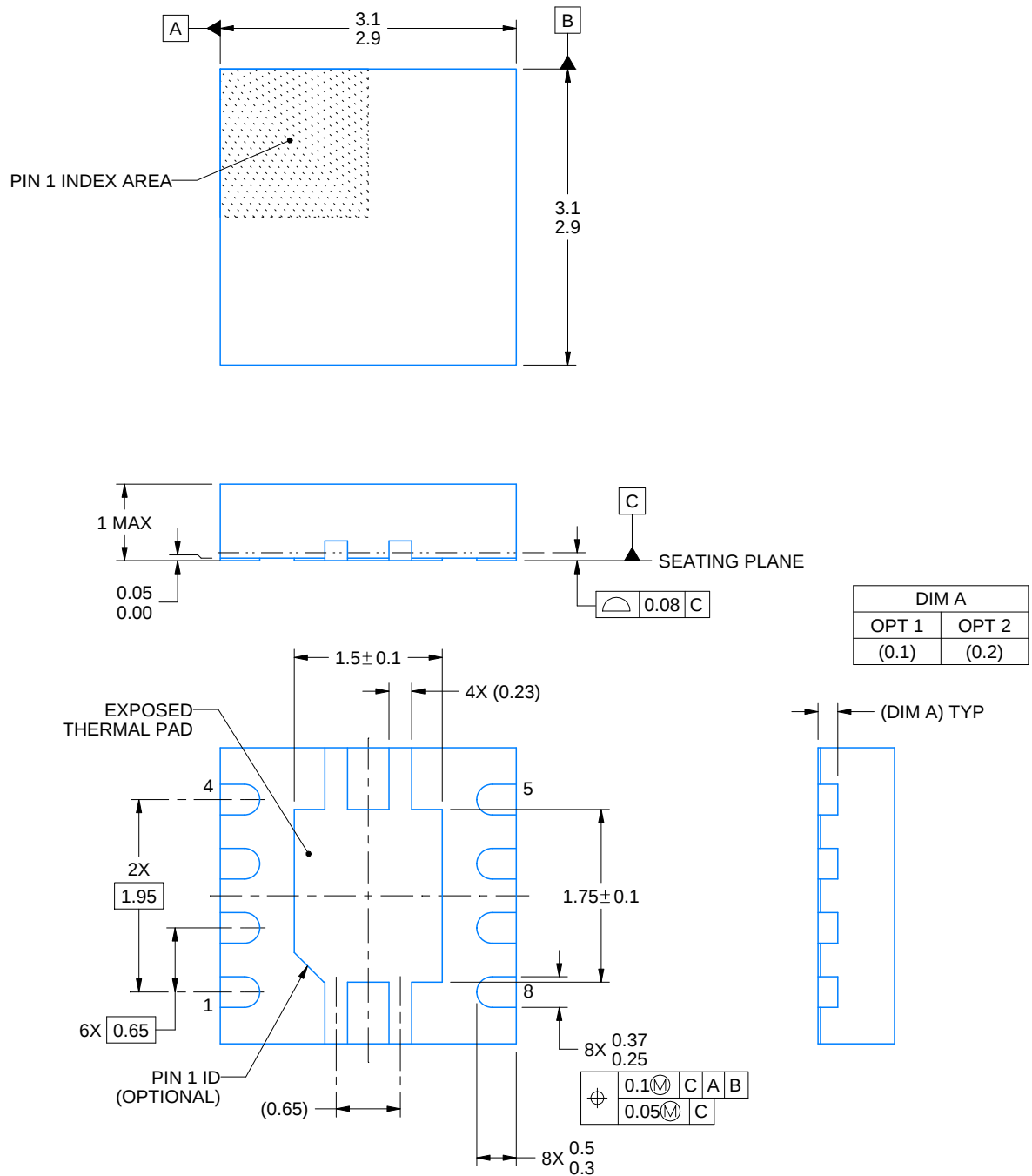
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



4218875/A 01/2018

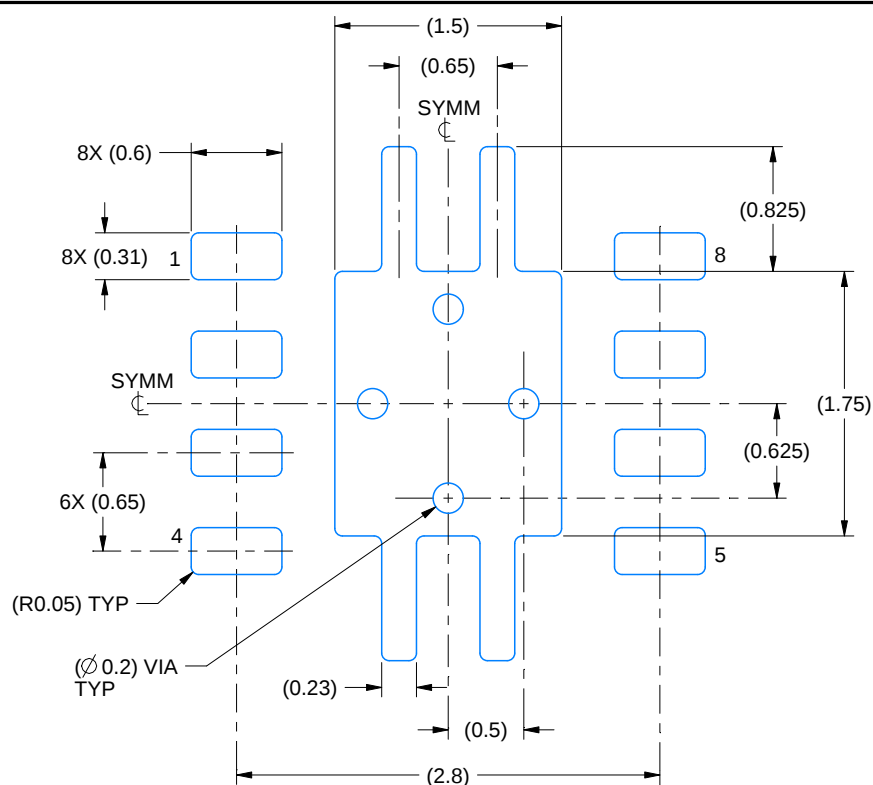
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

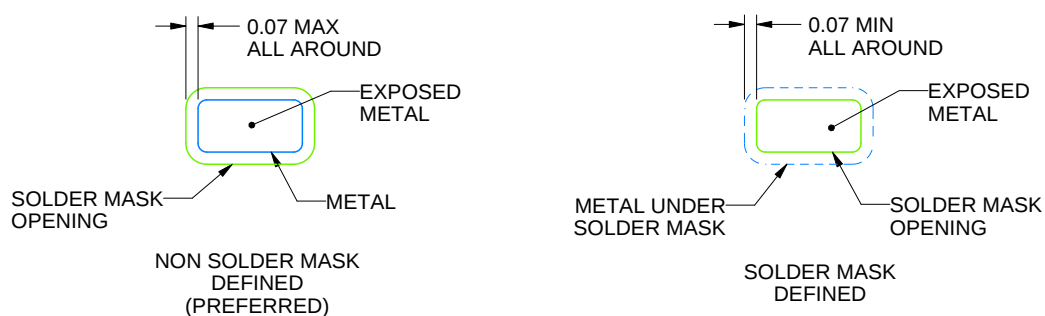
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

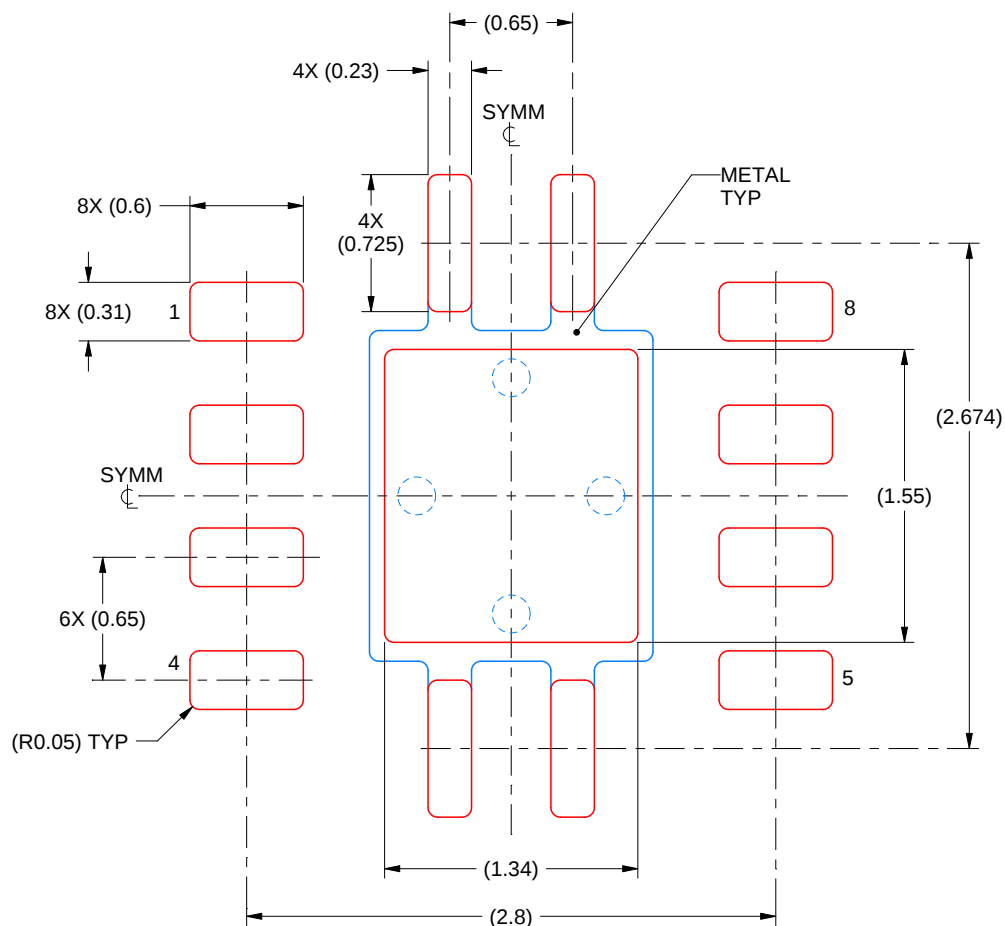
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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