TPS7H5001-SP Radiation-Hardness-Assured Si and GaN Dual Output Controller

1 Features

- Radiation performance:
  - Radiation hardness assured (RHA) up to TID 100 krads(Si)
    (RHA qualification in progress)
  - SEL, SEB, and SEGR immune to LET = 75 MeV-cm²/mg
  - SET and SEFI characterized up to LET = 75 MeV-cm²/mg
- Input voltage: 4 V to 14 V
- 0.613-V ±1% voltage reference over temperature, radiation, and line and load regulation
- Operating current of less than 10 mA at 1 MHz
- Switching frequency from 100 kHz to 2 MHz
- External clock synchronization capability
- Adjustable dead time and leading edge blank time
- Configurable duty cycle limit
- Adjustable slope compensation and soft start
- Adjustable undervoltage lockout (UVLO) using enable pin
- Input fault pin
- Supports buck and isolated topologies
- 22-pin, thermally-enhanced ceramic flatpack (HFT) for space applications

2 Applications

- Space satellite point of load supply for FPGAs, microcontrollers, data converters and ASICs
- Communications payload
- Command & data handling
- Optical imaging payload
- Satellite electrical power system

3 Description

The TPS7H5001-SP is a radiation-hardness-assured, current mode, dual output PWM controller optimized for both silicon (Si) and gallium nitride (GaN) power semiconductor based DC-DC converters in space applications. The high switching frequency capability of the TPS7H5001-SP, small footprint, and low-current consumption makes it ideal for fully exploiting the area reduction and high-efficiency benefits of GaN based DC-DC converters. The TPS7H5001-SP features integrated synchronous rectifier control outputs and dead-time programmability in order to target high-efficiency and high-performance topologies. In addition, the TPS7H5001-SP supports single-ended converter topologies by providing the user flexibility to control the maximum duty cycle. The 0.613 V ±1%-accurate internal reference allows design of high-current buck converters for FPGA core voltages.

The TPS7H5001-SP can be driven using an external clock through the SYNC pin or by using the internal oscillator at a frequency programmed by the user. Other programmable features include the UVLO threshold, soft start, and slope compensation. The TPS7H5001-SP is packaged in a small 22-pin ceramic dual flat package.

<table>
<thead>
<tr>
<th>PART NUMBER(1)</th>
<th>GRADE(2)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTPS7H5001HFT/EM</td>
<td>Engineering samples(3)</td>
<td>CDFP (22) 6.21 mm × 7.69 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 2021</td>
<td>*</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

![Figure 5-1. HFT Package 22-Pin CFP With Thermal Pad Top View](image)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT</td>
<td>I/O</td>
<td>1</td>
<td></td>
<td>In internal oscillation mode, the RT pin must be populated with a resistor to AVSS. When the RT pin is floating, a 200-kHz to 4-MHz external clock is required at the SYNC pin. The frequency of the external clock must be twice the desired switching frequency.</td>
</tr>
<tr>
<td>PS</td>
<td>I/O</td>
<td>2</td>
<td></td>
<td>Primary off to synchronous rectifier on dead-time set. Programmable through an external resistor to AVSS.</td>
</tr>
<tr>
<td>SP</td>
<td>I/O</td>
<td>3</td>
<td></td>
<td>Synchronous rectifier off to primary on dead-time set. Programmable through an external resistor to AVSS.</td>
</tr>
<tr>
<td>LEB</td>
<td>I/O</td>
<td>4</td>
<td></td>
<td>Leading edge blank time set. Programmable through an external resistor to AVSS.</td>
</tr>
<tr>
<td>HICC</td>
<td>I/O</td>
<td>5</td>
<td></td>
<td>Cycle-by-cycle current limit time delay and hiccup time setting. Delay time and hiccup time determined by capacitor from HICC to AVSS. Connecting this pin to AVSS disables hiccup mode.</td>
</tr>
<tr>
<td>SYNC</td>
<td>I/O</td>
<td>6</td>
<td></td>
<td>When the RT pin is floating, SYNC is configured as an input for a 200-kHz to 4-MHz external clock. In this case, the external clock input gets inverted and the system clock will run at half the frequency of the external clock input. When the RT pin is populated with a resistor to AVSS, SYNC outputs a 200-kHz to 4-MHz clock signal in phase with the switching frequency of the device.</td>
</tr>
<tr>
<td>DCL</td>
<td>I/O</td>
<td>7</td>
<td></td>
<td>Duty cycle limit configurability. This pin can be connected to AVSS, left floating, or VLDO to set the maximum duty cycle to 50%, 75%, and 100% respectively.</td>
</tr>
<tr>
<td>EN</td>
<td>I</td>
<td>8</td>
<td></td>
<td>Connecting the EN pin to the VLDO pin or external source greater than 0.6 V enables the device. In addition, input undervoltage lockout (UVLO) can be adjusted with two resistors.</td>
</tr>
<tr>
<td>VIN</td>
<td>I</td>
<td>9</td>
<td></td>
<td>Input supply to the device. Input voltage range is from 4 V to 14 V.</td>
</tr>
<tr>
<td>OUTA</td>
<td>O</td>
<td>10</td>
<td></td>
<td>Primary switching output A.</td>
</tr>
<tr>
<td>PIN</td>
<td>NO.</td>
<td>I/O</td>
<td>DESCRIPTION</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>-----</td>
<td>-----</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>OUTB</td>
<td>11</td>
<td>O</td>
<td>Primary switching output B. Active only when DCL = AVSS.</td>
<td></td>
</tr>
<tr>
<td>SRB</td>
<td>12</td>
<td>O</td>
<td>Synchronous rectifier output B. Active only when DCL = AVSS.</td>
<td></td>
</tr>
<tr>
<td>SRA</td>
<td>13</td>
<td>O</td>
<td>Synchronous rectifier output A.</td>
<td></td>
</tr>
<tr>
<td>AVSS</td>
<td>14</td>
<td>—</td>
<td>Ground of the device. The thermal pad, lid, and seal ring of the device are connected to ground.</td>
<td></td>
</tr>
<tr>
<td>VLDO</td>
<td>15</td>
<td>O</td>
<td>Output of internal regulator. Requires at least 1-μF external capacitor to AVSS.</td>
<td></td>
</tr>
<tr>
<td>CS_ILIM</td>
<td>16</td>
<td>I/O</td>
<td>Current sense for PWM control and cycle-by-cycle overcurrent protection. An input voltage over 1.05 V on CS_ILIM will trigger an overcurrent in the PWM controller.</td>
<td></td>
</tr>
<tr>
<td>FAULT</td>
<td>17</td>
<td>I</td>
<td>Fault protection pin. When the rising threshold of the FAULT pin is exceeded, the outputs will stop switching. After the external voltage drops below the falling threshold, the device will restart after a set delay. Connect this pin to AVSS to disable FAULT.</td>
<td></td>
</tr>
<tr>
<td>REFCAP</td>
<td>18</td>
<td>O</td>
<td>1.2-V internal reference. Requires a 470-nF external capacitor to AVSS.</td>
<td></td>
</tr>
<tr>
<td>RSC</td>
<td>19</td>
<td>I/O</td>
<td>A resistor from RSC to AVSS sets the desired slope compensation.</td>
<td></td>
</tr>
<tr>
<td>SS</td>
<td>20</td>
<td>I/O</td>
<td>Soft start. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.</td>
<td></td>
</tr>
<tr>
<td>VSENSE</td>
<td>21</td>
<td>I</td>
<td>Inverting input of the error amplifier.</td>
<td></td>
</tr>
<tr>
<td>COMP</td>
<td>22</td>
<td>I/O</td>
<td>Error amplifier output. Connect frequency compensation to this pin.</td>
<td></td>
</tr>
</tbody>
</table>
### 6 Specifications

#### 6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Input</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>–0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>RT, VSENSE, SS, RSC, COMP, PS, SP, HICC, LEB</td>
<td>–0.3</td>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td>SYNC</td>
<td>–0.3</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>EN, FAULT</td>
<td>–0.3</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>DCL, CS_ILIM</td>
<td>–0.3</td>
<td>7.5</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTA, OUTB, SRA and SRB</td>
<td>–0.3</td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>VLD0</td>
<td>–0.3</td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>REFSCAP</td>
<td>–0.3</td>
<td>3.3</td>
<td></td>
</tr>
</tbody>
</table>

| T<sub>J</sub>  | –55   | 150   | °C   |
| T<sub>stg</sub>| –65   | 150   | °C   |

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>V&lt;sub&gt;ESD&lt;/sub&gt;</th>
<th>ELECTROSTATIC DISCHARGE</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>±1000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 JESD22-C101, all pins&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>±250</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Supply voltage</td>
<td>4</td>
<td>14</td>
</tr>
<tr>
<td>SR&lt;sub&gt;VIN&lt;/sub&gt;</td>
<td>Input voltage slew rate</td>
<td>0.03</td>
<td>V/µs</td>
</tr>
<tr>
<td>T&lt;sub&gt;J&lt;/sub&gt;</td>
<td>Junction temperature</td>
<td>–55</td>
<td>125</td>
</tr>
</tbody>
</table>

#### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>TP7H5001-SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;θJA&lt;/sub&gt;</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>R&lt;sub&gt;θJC(bot)&lt;/sub&gt;</td>
<td>Junction-to-case (bottom) thermal resistance</td>
</tr>
<tr>
<td>R&lt;sub&gt;θJB&lt;/sub&gt;</td>
<td>Junction-to-board thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
## 6.5 Electrical Characteristics

over ambient temperature range \( T_A = -55^\circ C \) to 125°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY VOLTAGES AND CURRENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Operating input voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDD</td>
<td>Operating supply current</td>
<td>( f_{SW} = 500 \text{ kHz} ), No load for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SW} = 1 \text{ MHz} ), No load for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SW} = 2 \text{ MHz} ), No load for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SW} = 500 \text{ kHz}, C_{LOAD} = 100\text{pF} ) for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SW} = 1 \text{ MHz}, C_{LOAD} = 100\text{pF} ) for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SW} = 2 \text{ MHz}, C_{LOAD} = 100\text{pF} ) for OUTA, OUTB, SRA, and SRB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{DD(dis)}</td>
<td>Standby current</td>
<td>EN = 0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLDO</td>
<td>Internal linear regulator output voltage</td>
<td>5 V ≤ VIN ≤ 14 V, ( f_{SW} \leq 1 \text{ MHz} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLDO</td>
<td>Internal linear regulator output voltage</td>
<td>5 V ≤ VIN ≤ 14 V, ( f_{SW} = 2 \text{ MHz} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ENABLE AND UNDERVOLTAGE LOCKOUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ENR} )</td>
<td>EN threshold rising</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ENF} )</td>
<td>EN threshold falling</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ENH} )</td>
<td>EN hysteresis voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{EN}</td>
<td>EN pin input leakage current</td>
<td>VIN = 14 V, EN = 5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLDO_{UVLOR}</td>
<td>VLDO UVLO rising</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLDO_{UVLOF}</td>
<td>VLDO UVLO falling</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLDO_{UVLOH}</td>
<td>VLDO UVLO hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SOFT START</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{SS}</td>
<td>Soft-start current</td>
<td>SS = 0.3 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{yn}} )</td>
<td>Transconductance</td>
<td>(-2 \mu A &lt; I_{COMP} &lt; 2 \mu A, V_{(COMP)} = 1 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{DC}} )</td>
<td>DC gain</td>
<td>( V_{SENSE} = 0.6 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{SRC}} )</td>
<td>Error amplifier source current</td>
<td>( V_{(COMP)} = 1 \text{ V}, 100\text{-mV input overdrive} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{SNK}} )</td>
<td>Error amplifier sink current</td>
<td>( V_{(COMP)} = 1 \text{ V}, 100\text{-mV input overdrive} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{R0}} )</td>
<td>Error amplifier output resistance</td>
<td></td>
<td>7</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( E_{A_{OG}} )</td>
<td>Error amplifier input offset voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{IB}} )</td>
<td>Error amplifier input bias current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_{A_{BW}} )</td>
<td>Bandwidth</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNClIL</td>
<td>SYNC in low-level</td>
<td>VIN ≤ 5 V</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SYNClIL</td>
<td>SYNClIL in low-level</td>
<td>VIN ≥ 5 V</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNCHIL</td>
<td>SYNCHIL in high-level</td>
<td>VIN ≤ 5 V</td>
<td>3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SYNCHIL</td>
<td>SYNCHIL in high-level</td>
<td>VIN ≥ 5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSYNC</td>
<td>SYNC in frequency range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSYNC</td>
<td>SYNC in duty cycle</td>
<td>Duty cycle of external clock</td>
<td>40</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>SYNCRT</td>
<td>SYNC out low-to-high rise time (10%/90%)</td>
<td>( C_{LOAD} = 25 \text{pF} )</td>
<td>6</td>
<td>15</td>
<td>ns</td>
</tr>
</tbody>
</table>
6.5 Electrical Characteristics (continued)

over ambient temperature range $T_A = -55°C$ to $125°C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC&lt;sub&gt;FT&lt;/sub&gt;</td>
<td>SYNC out high-to-low fall time (10%/90%)</td>
<td>6</td>
<td>17</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>LOAD = 25 pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>SYNC out low level</td>
<td>10 mA</td>
<td>500</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>VLD&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>SYNC out high level (2)</td>
<td>10 mA</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EX&lt;sub&gt;DT&lt;/sub&gt;</td>
<td>Externally set frequency detection time</td>
<td>RT = Open, $f = 200$ kHz</td>
<td></td>
<td>20</td>
<td>µs</td>
</tr>
<tr>
<td>FSW&lt;sub&gt;EXT&lt;/sub&gt;</td>
<td>Externally set frequency</td>
<td>RT = 1.07 MΩ</td>
<td>95</td>
<td>105</td>
<td>115</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RT = 511 kΩ</td>
<td>190</td>
<td>210</td>
<td>230</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RT = 90.9 kΩ</td>
<td>900</td>
<td>1000</td>
<td>1100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RT = 34.8 kΩ</td>
<td>1700</td>
<td>2000</td>
<td>2300</td>
</tr>
</tbody>
</table>

**VOLTAGE REFERENCE**

| VREF | Internal voltage reference initial tolerance (1) | Measured at COMP, $25°C$ | 0.609 | 0.613 | 0.615 | V |
| | Internal voltage reference (1) | Measured at COMP, $-55°C$ | 0.607 | 0.609 | 0.612 | |
| | | Measured at COMP, $+125°C$ | 0.611 | 0.614 | 0.617 | |

| REFCAP | REFCAP voltage | REFCAP = 470 nF | 1.213 | 1.225 | 1.237 | V |

**CURRENT SENSE, CURRENT LIMIT AND HICCUP**

| CCSR | COMP to CS_LIM ratio | 2.00 | 2.06 | 2.12 | |
| | Current limit (over-current) threshold | 1.05 | 1.09 | | V |
| | | | | | |
| CS<sub>ILIM</sub> | Hiccup delay current | CS<sub>ILIM</sub> = 1.3 V, COMP = 3 V, VSENSE = REFCAP/2 V, C<sub>HICC</sub> = 3 nF, LEB = 49.9 kΩ, $f_{sw}$ = 100 kHz | 80 | | µA |
| | Hiccup restart current | | 1 | | µA |
| | Hiccup pull-up threshold | | 1.0 | | V |
| | Hiccup shut-down threshold | | 0.6 | | V |
| | Hiccup restart threshold | | 0.3 | | V |

**SLOPE COMPENSATION**

| Slope compensation | $f_{sw}$ = 100 kHz, RSC = 1.18 MΩ | 0.033 | V/µs |
| | $f_{sw}$ = 200 kHz, RSC = 562 kΩ | 0.066 | |
| | $f_{sw}$ = 1000 kHz, RSC = 100 kΩ | 0.333 | |
| | $f_{sw}$ = 2000 kHz, RSC = 49.9 kΩ | 0.666 | |

**FAULT**

| V<sub>FLTR</sub> | FLT threshold rising | | 0.57 | 0.6 | 0.63 | V |
| V<sub>FLTF</sub> | FLT threshold falling | | 0.47 | 0.5 | 0.53 | V |
| V<sub>FLTH</sub> | FLT hysteresis voltage | | 90 | 100 | 110 | mV |
| T<sub>FLT</sub> | FLT minimum pulse width | $V_{FLT} = 1$ V | 0.4 | 1.4 | | µs |
| | | | | | |
| I<sub>FLT</sub> | FLT delay duration | $f_{sw}$ = 100 kHz | 140 | 152 | 169 | µs |
| | | $f_{sw}$ = 200 kHz | 66 | 78 | 86 | |
| | | $f_{sw}$ = 1 MHz | 14 | 17 | 21 | |
| | | $f_{sw}$ = 2 MHz | 7 | 11 | 14 | |

**THERMAL SHUTDOWN**

| Thermal shutdown | | | 165 | 175 | 185 | °C |
| Thermal shutdown hysteresis | | | 10 | 15 | 20 | °C |

**PRIMARY AND SYNCHRONOUS RECTIFIER OUTPUTS**

| Low-level threshold | VIN = 5 V, IS<sub>SINK</sub> = 10 mA | 0.5 | | | V |
| | | | | | |
| High-level threshold | VIN = 5 V, IS<sub>SOURCE</sub> = 10 mA | 4.5 | | | V |
### 6.5 Electrical Characteristics (continued)

over ambient temperature range $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise/fall time</td>
<td>$R_{LOAD} = 50 , \text{kΩ}, C_{LOAD} = 100 , \text{pF}, 10%$ to $90%$</td>
<td></td>
<td></td>
<td>10</td>
<td>17 ns</td>
</tr>
<tr>
<td>$R_{\text{SRC}_P}$</td>
<td>$I_{OUT} = 20 , \text{mA}$</td>
<td>15</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{\text{SINK}_P}$</td>
<td>$I_{OUT} = 20 , \text{mA}$</td>
<td>15</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$v_{\text{MIN}}$</td>
<td>Minimum on-time $LEB = 10 , \text{kΩ}, 5 , \text{V} \leq \text{VIN} \leq 14 , \text{V}$</td>
<td>85</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{\text{DPS}}$</td>
<td>Primary off to secondary on dead time $PS = \text{floating}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of OUTx falling to $10%$ of SRx rising, OUTx and SRx floating</td>
<td>5</td>
<td>8</td>
<td>11</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$PS = 49.9 , \text{kΩ}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of OUTx falling to $10%$ of SRx rising, OUTx and SRx floating</td>
<td>43</td>
<td>50</td>
<td>55</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$PS = 107 , \text{kΩ}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of OUTx falling to $10%$ of SRx rising, OUTx and SRx floating</td>
<td>85</td>
<td>100</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>$T_{\text{DSP}}$</td>
<td>Secondary off to primary on dead time $SP = \text{floating}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of SRx falling to $10%$ of OUTx rising, OUTx and SRx floating</td>
<td>5</td>
<td>8</td>
<td>11</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$SP = 49.9 , \text{kΩ}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of SRx falling to $10%$ of OUTx rising edge, OUTx and SRx floating</td>
<td>43</td>
<td>50</td>
<td>55</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$SP = 107 , \text{kΩ}, 5 , \text{V} &lt; \text{VIN} &lt; 14 , \text{V}, 90%$ of SRx falling to $10%$ of OUTx rising, OUTx and SRx floating</td>
<td>85</td>
<td>100</td>
<td>110</td>
<td></td>
</tr>
</tbody>
</table>

### LEADING EDGE BLANK TIME AND DUTY CYCLE

| $T_{\text{LEB}}$ | Leading edge blank time $LEB = 10 \, \text{kΩ}, 5 \, \text{V} < \text{VIN} < 14 \, \text{V}$ | 12  | 15 | 19 | ns   |
|                 | $LEB = 49.9 \, \text{kΩ}, 5 \, \text{V} < \text{VIN} < 14 \, \text{V}$ | 45  | 50 | 55 |      |
|                 | $LEB = 110 \, \text{kΩ}, 5 \, \text{V} < \text{VIN} < 14 \, \text{V}$ | 85  | 100| 110|      |
| $D_{\text{MAX}}$ | Maximum duty cycle $DCL = \text{AVSS}$ | 45  | 48 | 50 |      |
|                 | $DCL = \text{floating, clock duty cycle = 50\%}$ | 70  | 75 | 80 | %    |
|                 | $DCL = \text{VLDO}$ | 100 |     |    |      |

(1) Measured at COMP pin to include error amplifier offset
(2) Bench verified. Not tested in production.
6.6 Typical Characteristics

**Figure 6-1. Operating Current Variation**

**Figure 6-2. Operating Current Variation**

**Figure 6-3. Standby Current Variation**

**Figure 6-4. Standby Current Variation**

**Figure 6-5. VLO UVLO Rising Variation**

**Figure 6-6. VLO UVLO Falling Variation**
6.6 Typical Characteristics (continued)

Figure 6-7. Enable Threshold Rising Variation

Figure 6-8. Enable Threshold Falling Variation

Figure 6-9. Soft-Start Current Variation

Figure 6-10. Soft-Start Current Variation

Figure 6-11. Voltage Reference Variation

Figure 6-12. Voltage Reference Variation
6.6 Typical Characteristics (continued)

- **Figure 6-13. Voltage Reference Variation**
  
  VIN = 4 V to 5 V  
  Temp. = 25°C

- **Figure 6-14. Voltage Reference Variation**
  
  VIN = 5 V to 14 V  
  Temp. = 25°C

- **Figure 6-15. Voltage Reference Variation**
  
  VIN = 4 V to 5 V  
  Temp. = 125°C

- **Figure 6-16. Voltage Reference Variation**
  
  VIN = 5 V to 14 V  
  Temp. = 125°C

- **Figure 6-17. Current Limit Threshold Variation**
  
  VIN = 4 V to 5 V

- **Figure 6-18. Current Limit Threshold Variation**
  
  VIN = 5 V to 14 V
6.6 Typical Characteristics (continued)

- **Figure 6-19.** Externally Set Frequency Variation
  
  VIN = 4 V to 5 V  
  RT = 1.07 MΩ

- **Figure 6-20.** Externally Set Frequency Variation
  
  VIN = 5 V to 14 V  
  RT = 1.07 MΩ

- **Figure 6-21.** Externally Set Frequency Variation
  
  VIN = 4 V to 5 V  
  RT = 511 kΩ

- **Figure 6-22.** Externally Set Frequency Variation
  
  VIN = 5 V to 14 V  
  RT = 511 kΩ

- **Figure 6-23.** Externally Set Frequency Variation
  
  VIN = 4 V to 5 V  
  RT = 90.9 kΩ

- **Figure 6-24.** Externally Set Frequency Variation
  
  VIN = 5 V to 14 V  
  RT = 90.9 kΩ
6.6 Typical Characteristics (continued)

VIN = 4 V to 5 V
RT = 34.8 kΩ

VIN = 5 V to 14 V
RT = 34.8 kΩ

Figure 6-25. Externally Set Frequency Variation

Figure 6-26. Externally Set Frequency Variation

Figure 6-27. Hiccup Delay Current Variation

Figure 6-28. Hiccup Delay Current Variation

Figure 6-29. Hiccup Restart Current Variation

Figure 6-30. Hiccup Restart Current Variation
6.6 Typical Characteristics (continued)

Figure 6-31. FAULT Threshold Rising Variation

Figure 6-32. FAULT Threshold Falling Variation

Figure 6-33. Leading Edge Blank Time Variation

Figure 6-34. Leading Edge Blank Time Variation

Figure 6-35. Leading Edge Blank Time Variation

Figure 6-36. Leading Edge Blank Time Variation
6.6 Typical Characteristics (continued)

Figure 6-37. Leading Edge Blank Time Variation

Figure 6-38. Leading Edge Blank Time Variation

Figure 6-39. PS Dead Time Variation

Figure 6-40. PS Dead Time Variation

Figure 6-41. PS Dead Time Variation

Figure 6-42. PS Dead Time Variation
6.6 Typical Characteristics (continued)

**Figure 6-43. PS Dead Time Variation**

VIN = 4 V to 5 V
RT = 100 kΩ

**Figure 6-44. PS Dead Time Variation**

VIN = 5 V to 14 V
RT = 100 kΩ

**Figure 6-45. SP Dead Time Variation**

VIN = 4 V to 5 V
RT = Floating

**Figure 6-46. SP Dead Time Variation**

VIN = 5 V to 14 V
RT = Floating

**Figure 6-47. SP Dead Time Variation**

VIN = 4 V to 5 V
RT = 49.9 kΩ

**Figure 6-48. SP Dead Time Variation**

VIN = 5 V to 14 V
RT = 49.9 kΩ
6.6 Typical Characteristics (continued)

Figure 6-49. SP Dead Time Variation

Figure 6-50. SP Dead Time Variation

Figure 6-51. Output Rise Time Variation

Figure 6-52. Output Rise Time Variation

Figure 6-53. Output Fall Time Variation

Figure 6-54. Output Fall Time Variation
6.6 Typical Characteristics (continued)

VIN (V) vs. OUTx/SRx Source Resistance (ohms)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>OUTx/SRx Source Resistance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4.2</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>12.5</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>17.5</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>22.5</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 4 V to 5 V

Figure 6-55. Output Source Resistance Variation

VIN (V) vs. OUTx/SRx Sink Resistance (ohms)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>OUTx/SRx Sink Resistance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>15</td>
<td>17.5</td>
</tr>
<tr>
<td>20</td>
<td>22.5</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 4 V to 5 V

Figure 6-57. Output Sink Resistance Variation

Slope Compensation (V/µs)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>Slope Compensation (V/µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.03</td>
</tr>
<tr>
<td>5</td>
<td>0.032</td>
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<tr>
<td>10</td>
<td>0.034</td>
</tr>
<tr>
<td>12.5</td>
<td>0.036</td>
</tr>
<tr>
<td>15</td>
<td>0.038</td>
</tr>
<tr>
<td>20</td>
<td>0.04</td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 4 V to 5 V

RT = 1.18 MΩ

Figure 6-59. Slope Compensation Variation

VIN (V) vs. OUTx/SRx Source Resistance (ohms)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>OUTx/SRx Source Resistance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>15</td>
<td>17.5</td>
</tr>
<tr>
<td>20</td>
<td>22.5</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 5 V to 14 V

Figure 6-56. Output Source Resistance Variation

VIN (V) vs. OUTx/SRx Sink Resistance (ohms)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>OUTx/SRx Sink Resistance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>15</td>
<td>17.5</td>
</tr>
<tr>
<td>20</td>
<td>22.5</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>OUTx/SRx Sink Resistance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>15</td>
<td>17.5</td>
</tr>
<tr>
<td>20</td>
<td>22.5</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 5 V to 14 V

RT = 1.18 MΩ

Figure 6-58. Output Sink Resistance Variation

Slope Compensation (V/µs)

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>Slope Compensation (V/µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.03</td>
</tr>
<tr>
<td>6</td>
<td>0.032</td>
</tr>
<tr>
<td>7</td>
<td>0.034</td>
</tr>
<tr>
<td>8</td>
<td>0.036</td>
</tr>
<tr>
<td>9</td>
<td>0.038</td>
</tr>
<tr>
<td>10</td>
<td>0.04</td>
</tr>
</tbody>
</table>

-55°C  25°C  125°C

VIN = 5 V to 14 V

RT = 1.18 MΩ

Figure 6-60. Slope Compensation Variation
6.6 Typical Characteristics (continued)

**Figure 6-61. Slope Compensation Variation**

VIN = 4 V to 5 V  
RT = 562 kΩ

**Figure 6-62. Slope Compensation Variation**

VIN = 5 V to 14 V  
RT = 562 kΩ

**Figure 6-63. Slope Compensation Variation**

VIN = 4 V to 5 V  
RT = 100 kΩ

**Figure 6-64. Slope Compensation Variation**

VIN = 5 V to 14 V  
RT = 100 kΩ

**Figure 6-65. Slope Compensation Variation**

VIN = 4 V to 5 V  
RT = 49.9 kΩ

**Figure 6-66. Slope Compensation Variation**

VIN = 5 V to 14 V  
RT = 49.9 kΩ
7 Detailed Description

7.1 Overview

The TPS7H5001-SP is a radiation-hardness-assured, current mode, dual output PWM controller optimized for silicon (Si) and gallium nitride (GaN) based DC-DC converters in space applications. The switching frequency of the TPS7H5001-SP can be configured from 100 kHz to 2 MHz while still maintaining a very low current consumption, which makes it ideal for fully exploiting the area reduction and high efficiency benefits of GaN based DC-DC converters. The device features integrated synchronous rectifier control outputs and dead-time programmability in order to target high efficiency and high performance topologies. In addition, the TPS7H5001-SP supports single-ended converter topologies by providing the user flexibility to control the maximum duty cycle. The 0.613-V ±1% accurate internal reference allows design of high-current buck converters for FPGA core voltages.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 VIN and VLDO

During steady state operation, the input voltage of the TPS7H5001-SP must be between 4 V and 14 V. A minimum bypass capacitance of at least 0.1 \( \mu \text{F} \) is needed between VIN and AVSS. The input bypass capacitors should be placed as close to the controller as possible.

The voltage applied at VIN serves as the input for the internal regulator that generates the VLDO voltage (5 V). At input voltages less than 5 V, the VLDO voltage will follow the voltage at VIN. Recommended capacitance for VLDO is 1 \( \mu \text{F} \). The EN and/or DCL pin can be tied to VLDO, but otherwise it is recommended to not externally load this pin due to limited output current capability.

A voltage divider connected between VIN and the EN pin can adjust the input voltage UVLO appropriately.

7.3.2 Startup

Before the primary outputs of the controller will start switching, the following conditions must be met:

- VLDO exceeds the rising UVLO threshold of 3.55 V (typical)
- The internal 0.613 V reference voltage is available
- The enable signal EN is above the rising voltage threshold of 0.6 V (typical)
- The FAULT pin voltage is below the rising voltage threshold of 0.6 V (typical)
- The device junction temperature is below the thermal shutdown threshold of 175°C (typical)

Once all of the aforementioned conditions are satisfied, the soft-start process will be initiated.

7.3.3 Enable and Undervoltage Lockout (UVLO)

There are several methods for enabling the TPS7H5001-SP through the EN pin. The pin can be tied directly to VLDO, which would allow for the device to be enabled as soon as the voltage on VLDO surpasses the rising edge voltage threshold of the EN pin. The pin can also be driven with an externally generated signal or a compatible PGOOD signal for instances in which sequencing is desired. Lastly, two resistors can be used to program the controller to enable when VIN surpasses a user determined threshold, as shown in Figure 7-1. The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AVSS.

![Figure 7-1. Enable Pin Configuration Using Two External Resistors](image)

Using Equation 1, the user can calculate the value for \( R_{UVLO\_TOP} \) for a chosen value of \( R_{UVLO\_BOT} \) based on the desired maximum startup voltage for the device. With these selected resistors Equation 2 can be used to determine the minimum startup voltage.
In the two-resistor configuration of Figure 7-1, the controller will also shut down due to undervoltage lockout when the input voltage falls below a particular threshold. This is due to the hysteresis of the EN pin. In order to determine the voltages at which shutdown is expected to occur, use Equation 3 and Equation 4.

\[
R_{UVLO\_TOP} = R_{UVLO\_BOT} \times \left( \frac{V_{START\_MAX}}{V_{EN\_RISING\_MAX}} - 1 \right)
\]  
(1)

\[
V_{START\_MIN} = V_{EN\_RISING\_MIN} \times \left( \frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right)
\]  
(2)

\[
V_{STOP\_MAX} = V_{EN\_FALLING\_MAX} \times \left( \frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right)
\]  
(3)

\[
V_{STOP\_MIN} = V_{EN\_FALLING\_MIN} \times \left( \frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right)
\]  
(4)

It is important to note that the user should take care when selecting the values for \(R_{UVLO\_TOP}\) and \(R_{UVLO\_BOT}\). It is recommended to optimize the selection of these resistors for startup in order to ensure proper operation. The UVLO value must be approximately 75% or less of the input voltage in order to ensure that the device turns on as expected under all circumstances. Setting the UVLO any higher may cause issues with the turn-on of the device. Figure 7-2 shows the expected startup and UVLO voltages on a 12 V rail where the maximum startup voltage is 90% of the nominal input voltage. In this instance, turn-off will occur when the input voltage falls to between 75% and 67% of its nominal value.

![Figure 7-2. Startup and UVLO Values for Two-Resistor Configuration with VIN = 12 V](image)

### 7.3.4 Voltage Reference

The device generates an internal 1.23-V bandgap reference that is utilized throughout the various control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to 0.613 V to produce the reference for the error amplifier. The error amplifier reference is measured at the COMP pin to account for offsets in the error amplifier and maintains regulation within ±1% across line, load, temperature, and TID as shown in Section 6. This tight reference tolerance allows for the user to design a highly accurate power converter. A 470-nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.
7.3.5 Error Amplifier

The TPS7H5001-SP uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS pin voltage or the internal 0.613-V voltage reference. The transconductance of the error amplifier is 1800 µA/V during normal operation. The frequency compensation network is connected between COMP pin and AVSS. The error amplifier DC gain is typically 10,000 V/V.

7.3.6 Output Voltage Programming

The output voltage of the power converter is set by using a resistor divider from \( V_{OUT} \) of the converter to the VSENSE pin. The output voltage must be divided down to nominal voltage reference of 0.613 V. Equation 5 can be used to select \( R_{BOTTOM} \).

\[
R_{BOTTOM} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP}
\]  

(5)

where:

- \( V_{REF} \) is 0.613 V (typical)
- \( V_{OUT} \) is the desired output voltage
- \( R_{TOP} \) is the value of the top resistor, selected by the user (i.e. 10 kΩ)

The recommendation is to use high tolerance resistors (1% or less) for \( R_{BOTTOM} \) and \( R_{TOP} \) for improved output voltage setpoint accuracy.

7.3.7 Soft-Start (SS)

The soft-start circuit increases the output voltage of the converter gradually until the steady-state programmed output is reached. During soft-start, the error amplifier uses the voltage on the soft-start pin as its reference until the SS pin voltage rises above \( V_{REF} \). Once the voltage at SS pin is above \( V_{REF} \), the soft-start period is complete. Note that the voltage at SS pin will continue to rise and once it reaches 1 V, the synchronous rectifier outputs of the controller will become active.

A capacitor between the SS pin and AVSS controls the soft-start time of the PWM controller. The following equation can be used to select the capacitor for the desired soft-start time:

\[
C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}}
\]  

(6)

where:

- \( t_{SS} \) is the desired soft-start time
- \( V_{REF} \) is voltage reference of 0.613 V (typical)
- \( I_{SS} \) is the soft-start charging current of 2.7 µA (typical)

7.3.8 Switching Frequency and External Synchronization

The TPS7H5001-SP has three modes for setting the switching frequency of the device: internal oscillator, external synchronization, and primary-secondary. The device is placed on one of these modes through unique configurations of the RT and SYNC pins. Primary-secondary mode can be used when it is desired for two controllers to have synchronized switching without the use of the external clock.

7.3.8.1 Internal Oscillator Mode

A resistor from the RT pin to AVSS sets the switching frequency of the device. The TPS7H5001-SP controller has a switching frequency range of 100 kHz to 2 MHz. In internal oscillator mode, the RT pin must be populated or the controller will not perform any switching. Equation 7 shows the calculation determining the RT value for a desired switching frequency. The curve in Figure 7-3 shows the RT value that corresponds to a given switching frequency for the TPS7H5001-SP.
\[
RT = \frac{112000}{f_{sw}} - 19.7
\]  

(7)

where:
- \(RT\) is in kΩ
- \(f_{sw}\) is in kHz

In this mode, the SYNC pin is configured as an output and produces a clock signal with a frequency that is twice that of the switching frequency set by \(RT\). As such, this clock signal has a range of 200 kHz to 4 MHz. This SYNC output clock signal is in phase with the switching frequency of the device. Figure 7-4 shows typical waveforms for the controller in this mode of operation.

7.3.8.2 External Synchronization Mode

The controller can be used in external synchronization mode by leaving the RT pin floating and applying a clock to the SYNC pin. Note than the RT pin configuration sets the oscillator mode of the controller and must be left floating for this mode of operation. The external clock that is applied must be set to twice the desired switching frequency (i.e. a 1-MHz applied clock is needed for 500-kHz switching frequency). The external clock must be in the range of 200 kHz to 4 MHz with a duty cycle between 40% and 60%. It is recommended to use an external clock with 50% duty cycle. The controller will internally invert the clock signal that is applied at the SYNC pin during this mode. Since the controller does not perform any switching with RT floating, the applied clock must be present before OUTA and OUTB will become active for external synchronization mode. Figure 7-5 shows the switching waveforms for the controller in external synchronization mode.
7.3.8.3 Primary-Secondary Mode

Two TPS7H5001-SP controllers can be operated in a primary-secondary mode by utilizing the SYNC pin. As mentioned in the *Internal Oscillator* section, when RT is selected to provide the desired switching frequency, SYNC outputs a clock signal at twice the switching frequency. As such, the clock input generated by the primary device be used as the clock input at SYNC for the secondary controller, which would operate in external synchronization mode. This means that the RT pin of the primary device should be populated while the corresponding pin of the secondary device would be left floating.

The primary-secondary mode would be useful in a couple of scenarios. The first is for two independent converters that need to be synchronized to the same switching frequency. In this instance, the converters can be two converters can have different operating conditions or topologies. Besides the shared SYNC signal, there are no connections between the two converters.
In a second scenario, two controllers can be used to design a single interleaved converter with phases in parallel. In this design, the VSENSE, COMP, SS, and HICC pins would need to be connected in addition to the shared SYNC connection.
When using two controllers in primary-secondary mode, it is important to note that secondary controller will invert the clock signal that it receives from the primary controller. As such, there will be phase shift between the switching outputs of the primary and secondary controllers. This phase shift from an output (i.e. OUTA) on the primary controller to the corresponding output on the secondary controller will be 90° or 270°, depending on when the secondary device synchronizes to its clock input.
The three operational modes for the controller are summarized in Table 7-1.

### Table 7-1. Oscillator Modes and Configurations

<table>
<thead>
<tr>
<th>Mode</th>
<th>RT</th>
<th>SYNC</th>
<th>Switching Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal oscillator</td>
<td>Populated with resistor to AVSS.</td>
<td>Configured as output. Generates in-phase clock at twice the switching frequency.</td>
<td>Configurable from 100 kHz to 2 MHz depending on RT value.</td>
</tr>
<tr>
<td>External synchronization</td>
<td>Floating.</td>
<td>Configured as input. Accepts 200-kHz to 4-MHz external clock that is inverted internally.</td>
<td>Synchronized to SYNC input clock at ½ of the clock frequency. Switching is out-of-phase with external clock.</td>
</tr>
<tr>
<td>Primary-secondary</td>
<td>Populated with resistor to AVSS on primary device. Floating on secondary device.</td>
<td>Configured as output on primary device. Configured as input on secondary device. The SYNC pins of primary and secondary devices are connected.</td>
<td>Configurable from 100 kHz to 2 MHz depending on RT value of primary device. Secondary device switching is either 90° or 270° out-of-phase with primary device.</td>
</tr>
</tbody>
</table>
7.3.9 Primary Switching Outputs (OUTA and OUTB)

OUTA and OUTB are the primary switching outputs of the controller. Due to the roughly 150-mA peak current capability of these outputs, an external gate drive solution will be needed. For buck and single ended isolated converter applications, OUTA provides the gate control signal for the main switch in the topology. For push-pull applications, OUTA and OUTB are both used to provide control signals to the main primary signals. Note that OUTB is only active when the duty cycle limit is set to 50% by connecting DCL pin to AVSS. OUTA and OUTB are not perfectly matched and will vary based on the COMP voltage in a given switching cycle.

7.3.10 Synchronous Rectifier Outputs (SRA and SRB)

In applications where synchronous rectification (SR) is desired in order to increase overall efficiency, SRA and SRB can be utilized to provide control signals for the SR switches. Also, in an active clamp topology where OUTA is used to control the main FET, SRA can be utilized to control the clamping FET. Similar to the primary switching outputs, the peak current capability is roughly 150 mA and an external gate drive solution is required. SRB is only active when the duty cycle limit is set to 50% connecting the DCL pin to AVSS. The synchronous rectifier outputs are off during the soft-start period and start switching when the voltage on SS exceeds 1 V. A small voltage transient may appear on the converter output at the moment when the synchronous rectifier outputs start switching.

7.3.11 Dead Time and Leading Edge Blank Time Programmability (PS, SP, and LEB)

The TPS7H5001-SP allows for the user to program two independent dead times, TD_{SP} and TD_{PS}, as shown in Figure 7-9. This allows for the dead times to be optimized by the user in order to prevent shoot-through between the primary and synchronous switches while attaining the best possible converter efficiency. The dead time TD_{PS} between primary output (OUTA and OUTB) turn-off to synchronous rectifier (SRA and SRB) turn-on, can be programmed using a resistor from PS to AVSS. Likewise, the dead time TD_{SP} between synchronous rectifier turn-off and primary output turn-on is set using a resistor from SP to AVSS. The equation for determining the values of R_{PS} and R_{SP} required for a desired dead time is shown in Equation 8.

\[ R_{PS} = R_{SP} = 1.207 \times DT - 8.858 \]  

where:
- DT is the desired dead time in ns
- \( R_{PS} \) and \( R_{SP} \) are in kΩ

If the PS and SP pins are left floating, the dead time will be set to a minimum value of 8 ns (typical). When these pins are populated, it is recommended to use a minimum resistor value of 10 kΩ for \( R_{PS} \) and \( R_{SP} \). The maximum resistor value to be used is 300 kΩ. As mentioned in Soft-Start (SS) and Synchronous Rectifier Outputs (SRA and SRB), the SRA and SRB outputs will be disabled during soft-start, so the dead time is observed only after this sequence is complete.

After OUTA or OUTB goes high, a leading edge blank time is implemented to remove any transient noise from the current sensing loop. Like the dead time, the leading edge blank time is programmable by placing an external resistor from LEB to AVSS. This pin cannot be left floating and a minimum resistor value of 10 kΩ is required from LEB to AVSS. The maximum resistor value that should be used is 300 kΩ. The equation for determining the value of \( R_{LEB} \) for a desired leading edge blank time is shown in Equation 9.

\[ R_{LEB} = 1.212 \times LEB - 9.484 \]  

where:
- LEB is the desired leading edge blank time in ns
- \( R_{LEB} \) is in kΩ

In Figure 7-9, the dead times and leading edge blank times are shown for the switching waveforms. This figure also illustrates the minimum on-time of the device, which is comprised of the programmed blank time \( T_{LEB} \) and an internal logic delay \( t_d \).
7.3.12 Pulse Skipping

In order to prevent converter operational issues related to the minimum on-time of the controller, specifically during high frequency operation, a pulse skipping mode has been implemented for the TPS7H5001-SP. During this mode, the primary outputs (OUTA and OUTB) will stop switching periodically. If the soft-start sequence of the converter has ended and the synchronous rectifier outputs are active, SRA and SRB will remain on during this period. If the device enters into pulse skipping during the soft-start sequence, SRA and SRB are not yet active and remain off. Having a minimum on-time that is too long in duration during high frequency operation can lead to an issue such as inductor current runaway during the soft-start period. Pulse skipping allows for overcoming this issue by reducing the peak inductor current during the startup period. In high frequency converter designs where the $\text{V}_{\text{IN}}$ to $\text{V}_{\text{OUT}}$ ratio of the converter may lead to required duty cycles that are less than the minimum on-time, the controller outputs will skip pulses in order to maintain the required output voltage. Pulse skipping will occur when both of the following conditions are present:

- The voltage at the COMP pin is less than 0.3 V at the rising edge of the system clock
- The previous duty cycle was less than 25%

When the duty cycle limit of the controller is set to 50% and both OUTA and OUTB are active, the number of pulses skipped by each of the primary outputs will be equal. This will ensure the volt-second balance is maintained across the transformer and that flux-walking that leads to transformer saturation is avoided in isolated topologies such as the push-pull.

7.3.13 Duty Cycle Programmability

The TPS7H5001-SP can be configured to support different DC-DC converter topologies by programming its maximum duty cycle using the DCL pin. For applications such as the buck converter where 100% duty cycle is needed, the DCL pin should be connected to VLDO. For other applications, such as active-clamp forward, the DCL could be connected to AVSS for 50% duty cycle limit or left floating for 75% maximum duty cycle. Note that OUTB and SRB are only active for the case when the duty cycle limit is set to 50% (DCL = AVSS).
This configuration is intended to support applications such as the push-pull converter that require two primary switching outputs and two synchronous rectification outputs. If the controller is being operated in external synchronization mode, the most precise results are obtained when the applied system clock has a 50% duty cycle. Specifically, for the case when the duty cycle limit is set to 75% (DCL = floating), there may be some variation of the duty cycle limit that is dependent on the duty cycle of the external clock applied at SYNC.

Table 7-2. DCL Pin Configurations

<table>
<thead>
<tr>
<th>Maximum Duty Cycle (Nominal)</th>
<th>DCL Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>VLDO</td>
</tr>
<tr>
<td>75%</td>
<td>Floating</td>
</tr>
<tr>
<td>50%</td>
<td>AVSS</td>
</tr>
</tbody>
</table>

7.3.14 Current Sense and PWM Generation (CS_ILIM)

The CS_ILIM pin is driven by a signal representative of the transformer primary-side current. The current signal has to have compatible input range of the COMP pin. As shown in Figure 7-10, the COMP pin voltage is used as the reference for the peak current. The primary side signals, OUTA and OUTB, are turned on by the internal clock signal and turned off when sensed peak current reaches the COMP/2 pin voltage. The CS_ILIM pin is also used to configure the current limit for the controller.

Figure 7-10. Peak Current Mode Control and PWM Generation

A resistor is needed from CS_ILIM to AVSS is used to detect current for both proper PWM operation and overcurrent protection. The current limit threshold $V_{CS\_ILIM}$ is specified as 1.05 V (nominal) in the electrical specifications. This indicates that when the voltage on this pin reaches this threshold, the device will go into hiccup mode. Equation 10 shows the calculation for determining the value of the sense resistor for a selected current limit.

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}}$$  \hspace{1cm} (10)

Note that the value of $I_{LIM}$ has to account for where and how the current is being sensed. For a forward converter with sense resistor between source of primary FET to AVSS, $I_{LIM}$ will be referred to the primary side of the converter.
$$I_{\text{LIM}} = I_{\text{L,PEAK}} \times \frac{N_S}{N_P}$$  \hspace{1cm} (11)

Equation 11 shows the calculation for determining $I_{\text{LIM}}$ in the design of a forward converter, where:
- $I_{\text{L,PEAK}}$ is the peak output inductor current desired to activate the overcurrent protection
- $N_S$ is the number of secondary turns for the power transformer
- $N_P$ is the number of primary turns for the power transformer

In the design of a buck converter which senses the high side current via a current sense transformer, Equation 12 can be used for determining $I_{\text{LIM}}$ for this instance.

$$I_{\text{LIM}} = I_{\text{L,PEAK}} \times \frac{N_{\text{CSP}}}{N_{\text{CSS}}}$$  \hspace{1cm} (12)

In this equation:
- $I_{\text{L,PEAK}}$ is the peak output inductor current desired to activate the overcurrent protection
- $N_{\text{CSP}}$ is the number of primary turns of the current sense transformer
- $N_{\text{CSS}}$ is the number of secondary turns of the current sense transformer

Regardless of the topology, the user should ensure that there is sufficient margin between the peak current during normal operation and the overcurrent trip point when determining the value of $R_{\text{CS}}$.

7.3.15 Hiccup Mode Operation (HICC)

Once the voltage at $\text{CS}_{\text{ILIM}}$ exceeds 1.05 V, the device will execute cycle-by-cycle current limiting. The controller output is turned on at the beginning of each cycle until such point that $\text{CS}_{\text{ILIM}}$ voltage reaches the current sense threshold $V_{\text{CS}_{\text{ILIM}}}$, when the output is turned off. At the same time, each time the voltage at $\text{CS}_{\text{ILIM}}$ reaches 1.05 V, the capacitor at $C_{\text{HICC}}$ is charged via a 80-µA current (hiccup delay current). This hiccup delay current is terminated at the end of the clock cycle. As long as there is still an overcurrent being detected, the cycle-by-cycle limiting will continue until the voltage on $C_{\text{HICC}}$ reaches 0.6 V. This cycle-by-cycle limiting period is referred to as the delay mode. As such, the capacitor $C_{\text{HICC}}$ can be chosen to dictate the amount of time that the controller will spend in delay mode.

$$C_{\text{HICC}} = \frac{t_{\text{delay}} \times 80 \mu\text{A}}{0.6 \text{ V}}$$  \hspace{1cm} (13)

Note that this equation is an approximation since:
- depending on the system behavior and if $C_{\text{HICC}}$ has been charged previously, $C_{\text{HICC}}$ may not start at 0 V as assumed by the equation
- the 80-µA charging current is a pulsed current, the duration of which will be dictated by the nature of the overcurrent (that is, when the current sense threshold is reached during each clock cycle)

After the voltage on HICC pin reaches 0.6 V, the SS pin of the controller is discharged and switching stops. The voltage on HICC is then quickly pulled up to 1 V with the pull-up current limited to approximately 1 mA. Once HICC voltage reaches 1 V, the 1-µA hiccup restart current begins to discharge $C_{\text{HICC}}$. The controller will not switch until HICC voltage falls to 0.3 V. Once the voltage falls to 0.3 V, the controller will initiate its soft-start sequence again. If the overcurrent has disappeared, normal operation will resume. The hiccup time, which is the entire non-switching period, can be calculated using Equation 14.

$$t_{\text{HICC}} = \frac{C_{\text{HICC}} \times (1 \text{ V} - 0.3 \text{ V})}{1 \mu\text{A}}$$  \hspace{1cm} (14)

In summary, the capacitor $C_{\text{HICC}}$ on the HICC pin controls the amount of time the controller spends performing cycle-by-cycle limiting before switching stops, and also controls the amount of time switching is disabled before re-start is attempted again. It is recommended to use a minimum of 3.3 nF for $C_{\text{HICC}}$. 

7.3.16 External Fault Protection (FAULT)

The FAULT pin provides the user with flexibility to implement additional protections for the converter, such as input overcurrent protection or overvoltage protection, if desired. This pin can also be utilized in the event that the user desires more stringent protections than what is offered by the controller (i.e. thermal shutdown). The user can design external logic circuitry to generate the signal necessary to drive this pin based on the protection function. If the voltage on the FAULT pin exceeds 0.6 V (typical) for a duration specified by the FAULT minimum pulse width, a fault shutdown will occur. This FAULT minimum pulse width duration, which is between 0.4 µs and 1.4 µs, is intended to prevent any spurious triggering due to short-term transients. Since any short-term transient event detected on this pin that is less than 1.4 µs in duration may not activate the FAULT pin, these events should be properly evaluated by the user in order to determine the impact to the overall system. Once the fault is detected, the SS pin is discharged and the controller outputs stop switching and stay low as long as the rising threshold is exceeded on the pin. Once the fault has subsided and the voltage of FAULT falls below the falling threshold of 0.5 V (typical), the TPS7H5001-SP enters a delay period that is dependent on the switching frequency. This delay is approximately equal to 15 switching frequency cycles in addition to an internal logic delay. The soft-start sequence is again initiated after the delay period has finished. Equation 15 can be used to determine the length of the fault delay.
\[ t_{d\text{FLT}} = \frac{14700}{f_{\text{sw}}} + 2 \quad (15) \]

In this equation:
- \( t_{d\text{FLT}} \) is the fault delay duration in μs
- \( f_{\text{sw}} \) is the switching frequency in kHz

If the FAULT threshold is exceeded during the delay, the entire sequence is started again. Figure 7-12 shows the switching waveforms when the fault mode has been activated in the controller.

![Switching Waveforms During Fault Mode](image)

**Figure 7-12. Switching Waveforms During Fault Mode**

### 7.3.17 Slope Compensation (RSC)

When utilizing peak current mode control in switching power converter design, the converter can enter into an unstable state when the duty cycle for the main power switch rises above 50 percent. Essentially, the converter will be in a state where the error between the peak current and average current increases with each subsequent switching cycle. This instability, known as subharmonic oscillation, can be mitigated by adding slope compensation. For the TPS7H5001-SP, the slope compensation is in the form of a voltage ramp that is subtracted from the error amplifier output divided down by the parameter CCSR (COMP to CS_LIM ratio). The minimum slope compensation for stability over the entire duty cycle range is equal to 0.5 × \( m \), where \( m \) is the inductor falling current slope. The recommended slope compensation is 1 × \( m \), as any increase above this value will not improve stability.

For a typical buck converter, setting the slope compensation equal to the downward slope of the sensed current waveform yields the calculation in Equation 16.
where:
• \( SC \) is the slope compensation value in V/μs
• \( L \) is the output inductor value in μH
• \( N_{CSP} \) is the number of primary turns of the current sense transformer
• \( N_{CSS} \) is the number of secondary turns on the current sense transformer
• \( R_{CS} \) is the value of the current sense resistor in Ω

If no current sense transformer is used, set \( N_{CSP}/N_{CSS} \) to 1.

The slope compensation for the forward converter will be similar with the note that the sensed current waveform would also need to take into account the turns ratio of the main power transformer.

\[
SC = \frac{V_{OUT}}{L} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS}
\]

(16)

where:
• \( N_S \) is the number of secondary turns of the power transformer
• \( N_P \) is the number of primary turns of the power transformer

For the TPS7H5001-SP, a resistor from the RSC pin to AVSS can be used to set the desired slope compensation of the controller. Equation 18 shows the calculation for determining the proper resistor value for RSC.

\[
R_{SC} = \frac{28.3}{SC^{1.1}}
\]

(18)

where:
• \( SC \) is the desired slope compensation is V/μs
• \( R_{SC} \) is in kΩ

7.3.18 Frequency Compensation

Since the TPS7H5001-SP uses a transconductance error amplifier (OTA), either Type 2A or Type 2B frequency compensation can be applied. The primary difference between the two compensation schemes is that Type 2A has an additional capacitor \( C_{HF} \) in parallel with \( R_{COMP} \) and \( C_{COMP} \) in order to provide high-frequency noise attenuation. These components will be connected between the COMP pin of the controller, which is the OTA output, and AVSS.
For any of the topologies supported by the TPS7H5001-SP, the following procedure and equations can be used to select the compensation components. All parameters in the equations are in standard units unless otherwise indicated (that is, H for inductance, F for capacitance, Hz for frequency, and so on).

1. Select the desired crossover frequency ($f_c$) for the converter.
2. Calculate $R_{COMP}$ based on the selected crossover frequency $f_c$.

$$R_{COMP} = \frac{2 \pi \times f_c \times V_{OUT} \times C_{OUT}}{g_{m\text{ea}} \times V_{REF} \times g_{mPS}}$$

(19)

where:
- $g_{m\text{ea}}$ is the error amplifier transconductance of $1800 \times 10^{-6} \text{ A/V}$ (typical)
- $V_{REF}$ is the 0.613 V reference voltage (typical)
- $g_{mPS}$ is the power stage transconductance (see Equation 23)

2. Calculate $C_{COMP}$ to place compensation zero at the location of the power stage dominant pole.

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}}$$

(20)

3. Determine the output capacitor ESR zero location (optional).

$$f_{ESR} = \frac{1}{2 \pi \times C_{OUT} \times \text{ESR}}$$

(21)

4. Select the capacitor $C_{HF}$ to provide a high frequency pole to compensate for the ESR zero (optional).

$$C_{HF} = \frac{1}{2 \pi \times R_{COMP} \times f_{ESR}}$$

(22)
For different power converter topologies, the primary change to the compensation selection procedure will be the
determination of the power stage transconductance $g_{mPS}$. The power stage transconductance can be calculated
as shown in Equation 23.

\[
g_{mPS} = \frac{N_P \times N_{CSS}}{CCSR \times R_{CS} \times N_S \times N_{CSP}}
\]  

(23)

where:

- $N_P$ is the number of primary turns on the main power transformer (set to 1 if no transformer is used)
- $N_S$ is the number of secondary turns on the main power transformer (set to 1 if no transformer is used)
- $N_{CSP}$ is the number of primary turns on the current sense transformer (set to 1 if no transformer is used)
- $N_{CSS}$ is the number of secondary turns of the current sense transformer (set to 1 if no transformer is used)
- $R_{CS}$ is the selected value of the current sense resistor
- $CCSR$ is the ratio to COMP of $CS_{ILIM}$

Note that for the TPS7H5001-SP, the sensed current waveform is compared to the voltage at COMP divided
down by the factor $CCSR$ at the PWM comparator, which is accounted for in the denominator of the equation.
For buck converters, all turns for the main power transformer can be set equal to 1 and the equation still applies.

7.3.19 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds
175°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 160°C (typical).

7.4 Device Functional Modes

The TPS7H5001-SP uses fixed frequency, peak current mode control. The controller regulates the peak current
and duty cycle of the converter. The internal oscillator initiates the turn-on of the primary output used as the
gate driver input for the power switch. The external power switch current is sensed through an external resistor
and compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal
resistors. When the sensed current reaches the stepped down COMP voltage, the power switch is then turned
off.
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H5001-SP is a radiation-hardness-assured dual output current mode PWM controller that can be utilized for designing space-grade DC-DC converters. The device should be paired with external gate drivers in order to provide control of the power semiconductor switching device(s) of the converter power stage. By allowing for switching frequencies up to 2 MHz and providing the capability to configure the leading edge blank time using a resistor, the controller provides many advantages for GaN power semiconductor based converter designs. The TPS7H5001-SP can be used for the design of a number of common DC-DC converter topologies, including but not limited to: buck, flyback, forward, active-clamp forward, push-pull, and full-bridge. The duty cycle limit of the device can be configured to be compatible with the selected topology using the DCL pin. With integrated synchronous rectification outputs for both of the main switching outputs, the controller enables the design of fully synchronous versions of each of the supported topologies. As such, the dead time can also be adjusted with an external resistor using the controller in order to optimize the overall converter efficiency.

8.2 Typical Application

![Typical Application Schematic](Figure 8-1)

8.2.1 Design Requirements

The example provided here is to demonstrate how to design a synchronous push-pull converter using GaN power semiconductor devices. This design example is to show how to determine the component selection for the TPS7H5001-SP as well as key components of the converter power stage.
Table 8-1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>20 A</td>
</tr>
<tr>
<td>Output current pre-load</td>
<td>0.5 mA</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>25°C</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Peak input current limit</td>
<td>14 A</td>
</tr>
<tr>
<td>Target bandwidth</td>
<td>~10 kHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The synchronous push-pull converter was designed to operate at a switching frequency of 500 kHz. For space-grade converter designs, the benefits of GaN power devices over silicon counterparts are readily apparent at this switching frequency. Using Equation 7, the required RT resistor for the desired frequency can be determined as shown in Equation 24.

\[
RT = \frac{112000}{500} - 19.7 = 204.3 \text{ kΩ}
\]  

(24)

A standard resistor value of 205 kΩ is selected for the design.

8.2.2.2 Output Voltage Programming Resistors

The converter has an output voltage of 5 V. The feedback resistor divider connected to VSENSE should be selected to correspond to the selected \( V_{\text{OUT}} \). With a resistor of 10 kΩ selected for \( R_{\text{TOP}} \), the value of the bottom resistor in the divider can be calculated.

\[
R_{\text{BOTTOM}} = \frac{V_{\text{REF}}}{V_{\text{OUT}} - V_{\text{REF}}} \times R_{\text{TOP}}
\]

(25)

\[
R_{\text{BOTTOM}} = \frac{0.613 \text{ V}}{5 \text{ V} - 0.613 \text{ V}} \times 10 \text{ kΩ} = 1.397 \text{ kΩ}
\]

(26)

The values for \( R_{\text{TOP}} \) and \( R_{\text{BOT}} \) needed are 10 kΩ and 1.4 kΩ, respectively.

8.2.2.3 Dead Time

For GaN power semiconductor devices, a key characteristic that has to be taken into consideration is the voltage drop of the GaN FET while it is operating in reverse conduction mode. While the GaN FET does not have a body diode that is inherent in the silicon FET, it does still have the ability to conduct current in the reverse direction with behavior that is similar to a diode. When conducting in the reverse direction, the source-drain voltage of the GaN FET can be quite large. Thus, to reduce the dead-time losses and maximize efficiency, the dead time was set to a value of approximately 25 ns. Based on the selected value, Equation 8 can be used to calculate the resistors needed to attain the desired dead time.

\[
R_{\text{PS}} = R_{\text{SP}} = 1.207 \times 25 - 8.858 = 21.3 \text{ kΩ}
\]

(27)

The standard resistor value of 20.5 kΩ was selected for both \( R_{\text{PS}} \) and \( R_{\text{SP}} \).
8.2.2.4 Leading Edge Blank Time

The leading edge blank time was initially chosen to be roughly 50 ns. This value was the initial approximation based on any ringing or transient spikes that were expected to be seen on the sensed current waveform at the CS_ILIM pin. Using Equation 9, the value of R_{LEB} was calculated from this desired value.

\[
R_{LEB} = 1.212 \times 50 - 9.484 = 51.1 \text{ k}\Omega
\]

The value of R_{LEB} selected was 49.9 kΩ. Note that the ringing and transient spikes on the sensed current waveform will depend heavily on component placement and parastics in the PCB layout. The leading edge blank time should also account for any propagation delay that is inherent to the gate driver being used in the application. As such, the value of R_{LEB} may need to be optimized as the design is tested to accommodate for these factors. Recall that the leading edge blank time is also correlated to the minimum on-time of the device, and extending this value significantly may become a limiting factor for the maximum switching frequency that can be achieved in the design.

8.2.2.5 Soft-Start Capacitor

For this design, the soft-start time is arbitrary. The value of the soft-start capacitor selected was 33 nF. Based on this value, the soft-start time can be calculated.

\[
t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}}
\]

\[
t_{SS} = \frac{33 \text{ nF} \times 0.613 \text{ V}}{2.7 \text{ mA}} = 7.49 \text{ ms}
\]

The soft-start time is ~7.5 ms for the design.

8.2.2.6 Transformer

The turns ratio and primary inductance of the transformer will be determined based on the target specifications of the converter. In order to calculate the maximum allowable turns ratio, a duty cycle limit must be selected for the design. Even though DCL will be connected to AVSS to impose a 50% duty cycle limit from the controller to ensure there is no overlap of the primary switching outputs, a maximum duty cycle of approximately 35% is targeted for the design in order to provide sufficient margin to the controller limit. This is due to the fact that the actual duty cycle is greater than calculated duty cycle when accounting for the converter efficiency, and to allow for duty cycle increases during load transient events. Equation 31 provides the formulate needed to calculate the maximum turns ratio for this design.

\[
N_{PS\_MAX} = \frac{2 \times V_{IN\_MIN} \times D_{LIM}}{V_{OUT} + V_{SR}}
\]

\[
N_{PS\_MAX} = \frac{2 \times 22 \text{ V} \times 0.35}{5 \text{ V} + 0.5 \text{ V}} = 2.8
\]

A value of 2.5 is selected for the turns ratio for the design.

In order to design for the primary inductance of the transformer, the magnetizing current must be selected. The value of the magnetizing current is a trade-off between transformer size and efficiency, with larger magnetizing current leading to a smaller size due to lower required inductance, but also leading to lower efficiency. A magnetizing current equal to 6% of the output current was initially targeted for this design. With this value, the primary inductance can be calculated using Equation 36. The minimum duty cycle expected is needed for this
calculation can be determined using Equation 34, where the estimated efficiency $\eta$ for the converter used in the calculation is 85%.

$$D_{\text{MIN}} = \frac{V_{\text{OUT}} + V_{\text{SR}}}{2 \times V_{\text{IN_MAX}} \times N_{\text{SP}} \times \eta}$$  

(33)

$$D_{\text{MIN}} = \frac{5 \text{ V} + 0.5 \text{ V}}{2 \times 36 \text{ V} \times 0.4 \times 0.85} = 0.22$$  

(34)

$$L_P = \frac{N_{PS} \times V_{\text{IN_MAX}} \times D_{\text{MIN}}}{f_{sw} \times I_{\text{MAG}}}$$  

(35)

$$L_P = \frac{2.5 \times 36 \text{ V} \times 0.22}{500 \text{ kHz} \times 0.06 \times 20 \text{ A}} = 33 \mu\text{H}$$  

(36)

Though the calculated value of $L_P$ is 33 $\mu$H, it may often be challenging to find the exact primary inductance value needed for the transformer design. As such, an inductance of 40 $\mu$H was used in the actual design.

The following equations detail the how to calculate transformer primary and secondary currents that are critical for proper design of the transformer. These equations are useful for defining the physical structure of the transformer. Note that these are ideal equations, and the final design should be optimized depending on the application.

$$I_{\text{SEC_MAX}} = I_{\text{OUT}} + \frac{\Delta I_l}{2}$$  

(37)

$$I_{\text{SEC_MAX}} = 20 + \frac{8.51 \text{ A}}{2} = 24.25 \text{ A}$$  

(38)

$$I_{\text{PRI_MAX}} = \frac{I_{\text{SEC_MAX}} + (0.5 \times I_{\text{MAG}})}{N_{PS}}$$  

(39)

$$I_{\text{PRI_MAX}} = \frac{24.25 \text{ A} + (0.5 \times 0.06 \times 20 \text{ A})}{2.5} = 9.94 \text{ A}$$  

(40)

$$I_{\text{SEC_MAX}} (\text{VIN_MIN}) = \frac{I_{\text{OUT}} + \left( D_{\text{MIN}} \times \left( \frac{V_{\text{IN_MIN}}}{N_{PS}} - V_{\text{OUT}} - V_{\text{SR}} \right) \right)}{2 \times f_{sw} \times L_{\text{OUT}}}$$  

(41)

$$I_{\text{SEC_MAX}} (\text{VIN_MIN}) = \frac{20 \text{ A} + \left( 0.37 \times \frac{22 \text{ V}}{2.5} - 5 \text{ V} - 0.5 \text{ V} \right)}{2 \times 500 \text{ kHz} \times 0.47 \mu\text{H}} = 22.58 \text{ A}$$  

(42)

$$I_{\text{PRI_MAX}} (\text{VIN_MIN}) = \frac{I_{\text{SEC_MAX}} (\text{VIN_MIN}) + (0.5 \times I_{\text{MAG}})}{N_{PS}}$$  

(43)
\[ I_{PRI\_MAX}(VIN\_MIN) = \frac{17.42 A + (0.5 \times 0.06 \times 20 A)}{2.5} = 9.27 A \]  

(44)

\[ I_{OUT} - \left( D_{MAX} \times \frac{V_{IN\_MIN} - V_{OUT} - V_{SR}}{N_{PS}} \right) \]

(45)

\[ I_{SEC\_MIN}(VIN\_MIN) = \frac{20 A - \left( 0.37 \times \frac{22 V}{2.5} - 5 V - 0.5 V \right)}{2 \times 500 \text{ kHz} \times 0.47 \mu H} = 17.42 A \]  

(46)

\[ I_{PRI\_MIN}(VIN\_MIN) = \frac{I_{SEC\_MIN}(VIN\_MIN) - (0.5 \times I_{MA.G})}{N_{PS}} \]

(47)

\[ I_{PRI\_MIN}(VIN\_MIN) = \frac{17.42 A - (0.5 \times 0.06 \times 20 A)}{2.5} = 6.73 A \]  

(48)

\[ t_{ON\_MAX} = \frac{(V_{OUT} + V_{SR}) \times N_{PS}}{2 \times f_{sw} \times V_{IN\_MIN}} \]

(49)

\[ t_{ON\_MAX} = \frac{(5 V + 0.5 V) \times 2.5}{2 \times 500 \text{ kHz} \times 22 V} = 0.63 \mu s \]  

(50)

\[ m_{PRI} = \frac{I_{PRI\_MAX}(VIN\_MIN) - I_{PRI\_MIN}(VIN\_MIN)}{t_{ON\_MAX}} \]

(51)

\[ m_{PRI} = \frac{9.27 A - 6.73 A}{0.63 \mu s} = 4072130.16 \frac{A}{s} = 4.07 \frac{A}{\mu s} \]  

(52)

\[ I_{PRI\_RMS} = \sqrt{D_{MIN} \times \left( \frac{m_{PRI} \times t_{ON\_MAX}}{3} \right)^2 + \left( \frac{m_{PRI}}{2} \times I_{PRI\_MIN}(VIN\_MIN) \times t_{ON\_MAX} \right) + I_{PRI\_MIN}(VIN\_MIN)^2} \]

(53)

\[ I_{PRI\_RMS} = \sqrt{0.22 \times \left( \frac{4072130.16 A}{3} \times 0.63 \mu s \right)^2 + \left( \frac{4072130.16 A}{2} \times 6.73 A \times 0.63 \mu s \right) + 6.73 A^2} \]

(54)

\[ = 3.55 A \]
8.2.2.7 Main Switching FETs

In the push-pull topology, the switching devices on the primary side will see a voltage that is equal to twice that of the input when the devices are off. As such, the GaN FETs selected should have a voltage rating that 3 times higher than the input voltage. The voltage rating for the GaN FETs was conservatively chosen for the primary side as 170 V for this application based on maximum input voltage of 36 V. This was to account for any transient spikes that were seen during operation. Also ensure that the GaN FETs are properly sized based on the primary current calculations in Section 8.2.2.6.

8.2.2.8 Synchronous Rectifier FETs

The maximum voltage stress that will be seen by the synchronous rectifier switch on the secondary side can be calculated using Equation 55.

\[ V_{SR\_STRESS} = V_{OUT} + \frac{V_{IN\_MAX}}{NPS} \]  

(55)

\[ V_{SR\_STRESS} = 5 \, V + \frac{36 \, V}{2.5} = 19.4 \, V \]  

(56)

Note that the maximum expected voltage is approximately 20 V, but a higher rating should be selected to allow for transient spikes. For the design, an 80-V rated GaN FET was conservatively chosen for the synchronous rectifier. The current rating should be sufficient to handle the maximum secondary current as calculated in Section 8.2.2.6. In order to reduce the current through GaN FET during the soft-start period, when the controller SRA and SRB signals are off, a Schottky diode can be used in parallel with the synchronous rectifier GaN FETs. This diode would also mitigate the reverse conduction losses attributed to the GaN FET during the dead time and boost the overall efficiency of the system.

8.2.2.9 RCD Clamp

A resistor-capacitor-diode clamp circuit can be used to limit the voltage at the switch node. The equations below can be used to determine initial values for the resistor and capacitor, but the circuit will need to be optimized through testing. First, calculate the clamp voltage by determining how much overshoot is allowable at the switch node.

\[ V_{CLAMP} = K_{CLAMP} \times NPS \times (V_{OUT} + V_{SR}) \]  

(57)

The parameter \( K_{CLAMP} \) defines the target overshoot value. For example, set \( K_{CLAMP} \) to 1.5 for 50% allowable overshoot.

Next, the leakage inductance \( L_L \) and peak primary current \( I_{PRI\_MAX} \) of the transformer can be used to approximate the clamp resistor. The clamp capacitor value can be determined thereafter. Note that \( \Delta V_{CLAMP} \) defines the allowable ripple for the clamp capacitor.

\[ R_{CLAMP} = \frac{V_{CLAMP}^2}{0.5 \times L_L \times I_{PRI\_MAX}^2 \times \frac{V_{CLAMP}}{V_{CLAMP}} \times \frac{V_{CLAMP}}{(NPS \times (V_{OUT} + V_{SR})) \times f_{sw}}} \]  

(58)

\[ C_{CLAMP} = \frac{V_{CLAMP}}{\Delta V_{CLAMP} \times V_{CLAMP} \times R_{CLAMP} \times f_{sw}} \]  

(59)
8.2.2.10 Output Inductor

For the output inductor, a ripple current of 40% was targeted for the design. Based on the selected ripple current, Equation 60 can be used to determine the output inductor value. $K_L$ is the current ripple factor, which will be set to 0.4 in this instance.

\[
L_{OUT} = \frac{(V_{IN\;MAX} - V_{OUT} - V_{SR}) \times D_{MIN}}{f_{sw} \times K_L \times I_{OUT}}
\]

\[L_{OUT} = \frac{(36 \;V - 5 \;V - 0.5 \;V) \times 0.22}{500 \;kHz \times 0.4 \times 20 \;A} = 0.5 \;\mu H
\]

The value of the inductor selected for the design is 0.47 $\mu$H.

8.2.2.11 Output Capacitance and Filter

Generally, there are two different calculations that can be used to determine the output capacitance required for the converter. The first calculates the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient as shown in Equation 62. The second, shown in Equation 64, determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design. Once the two different calculations are performed, the maximum of these should be chosen as the output capacitance for the design. The calculations are shown for target voltage ripple of 2% of the output voltage and maximum allowable voltage deviation of 2.5% of the output voltage.

\[
C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_c}
\]

\[C_{OUT} > \frac{10 \;A}{2\pi \times 0.025 \times 5 \;V \times 10 \;kHz} = 1.27 \;mF
\]

\[
C_{OUT} > I_{OUT} \times 2 \times D_{MAX}
\]

\[C_{OUT} > \frac{I_{OUT} \times 2 \times 0.37}{V_{RIPPLE} \times f_{sw}} = 294.12 \;\mu F
\]

Based on the calculations, at least 1.3 mF of output capacitance is required. When selecting capacitors, consider any derating of capacitance that is needed to account for aging, temperature, and DC bias.

For space-grade converter designs, there is another consideration when selecting the output capacitance. This is the impact of radiation induced single event transients (SETs). Single energetic particle strikes can lead to momentary variation in the PWM variation of the controller, which in turn can lead to output voltage transients in the converter. Thus, even though the value above provides a minimum value to account for voltage ripple and/or load transients, additional capacitance is likely needed to for adequate SET mitigation. For the design example, approximately 2.3 mF of total output capacitance was used.

An additional output filter can be used to further reduce the noise of the output stage if deemed necessary. This output filter consists of an additional inductor and a small amount of ceramic capacitance. This ceramic capacitance is placed immediately downstream of the main output inductor that was determined in Section 8.2.2.10. The filter inductance is then located between the added ceramic capacitance and the bulk output capacitance that was determined to be required for the design. This approach can drastically reduce the output voltage ripple without significantly increasing the size and/or number of components required. The key for the
secondary filter design is to choose the resonant frequency such that it is higher than the targeted crossover frequency yet well below the switching frequency and ESR zero of the bulk output capacitance. Equation 66, Equation 67, and Equation 68 can be used to determine the ESR zero as well as the resonant frequency and attenuation of the additional output filter.

\[
f_{\text{zero}} = \frac{1}{2\pi \times C_{\text{OUT}_\text{BULK}} \times \text{ESR}_{\text{BULK}}} \quad (66)
\]

\[
f_{\text{resonant}} = \frac{1}{2\pi \times L_f \times C_{\text{OUT}_\text{BULK}}} \quad (67)
\]

\[
\text{Att}_{\text{sw}} = 40\log_{10}\left(\frac{f_{\text{sw}}}{f_{\text{resonant}}}\right) - 20\log_{10}\left(\frac{f_{\text{sw}}}{f_{\text{zero}}}\right) \quad (68)
\]

In the event that there is peaking at high frequencies due to the output filter, a resistor can be used to dampen this peaking effect. Equation 69 and Equation 70 can be used to determine the frequency of the peaking and the value of the resistor needed to provide adequate damping.

\[
\omega_o = \frac{2 \times (C_{\text{OUT}_\text{SER}} + C_{\text{OUT}_\text{BULK}})}{L_f \times C_{\text{OUT}_\text{SER}} \times C_{\text{OUT}_\text{BULK}}} \quad (69)
\]

\[
R_f = \frac{R_{\text{OUT}} \times L_f \times (C_{\text{OUT}_\text{SER}} + C_{\text{OUT}_\text{BULK}}) - \frac{L_f}{\omega_o}}{R_{\text{OUT}} \times (C_{\text{OUT}_\text{SER}} + C_{\text{OUT}_\text{BULK}}) - (L_f \times C_{\text{OUT}_\text{SER}})} \quad (70)
\]

### 8.2.2.12 Sense Resistor

The converter was designed such that the cycle-by-cycle limiting will begin once the output current reaches roughly 35 A. Given that the peak inductor current at maximum load current is 24.25 A, this provides about 45% margin before an overcurrent event is detected by the controller. The primary side current is being sensed at CS_ILIM, so the turns ratio must be accounted for when calculating the necessary value of the sense resistor. Likewise, a current sense transformer with turns ratio of 1:100 is used to step down the primary current. The following calculations are used to arrive at the value of \(R_{\text{CS}}\) that translates to the desired output overcurrent level.

\[
I_{\text{LIM}} = I_{\text{L,PEAK}} \times \frac{N_S}{N_P} \times \frac{N_{\text{CSP}}}{N_{\text{CSS}}} \quad (71)
\]

\[
I_{\text{LIM}} = 35 \text{ A} \times \frac{1}{2.5} \times \frac{1}{100} = 0.14 \text{ A} \quad (72)
\]

\[
R_{\text{CS}} = \frac{V_{\text{CS-ILIM}}}{I_{\text{LIM}}} \quad (73)
\]

\[
R_{\text{CS}} = \frac{1.05 \text{ V}}{0.14 \text{ A}} = 7.73 \Omega \quad (74)
\]

Based on the calculation, a 7.5-Ω resistor was selected for \(R_{\text{CS}}\).
8.2.2.13 Hiccup Capacitor

For the design, the value of the hiccup capacitor used is the minimum recommended value of 3.3 nF. Based on this value, the delay and hiccup times of the converter after an overcurrent are detected can be calculated.

\[
t_{\text{delay}} = \frac{C_{\text{HICC}} \times 0.6 \text{ V}}{80 \mu\text{A}}
\]

(75)

\[
t_{\text{delay}} = \frac{3.3 \text{ nF} \times 0.6 \text{ V}}{80 \mu\text{A}} = 24.75 \mu\text{s}
\]

(76)

\[
t_{\text{HICC}} = \frac{C_{\text{HICC}} \times (1 \text{ V} - 0.3 \text{ V})}{1 \mu\text{A}}
\]

(77)

\[
t_{\text{HICC}} = \frac{3.3 \text{ nF} \times (1 \text{ V} - 0.3 \text{ V})}{1 \mu\text{A}} = 2.31 \text{ ms}
\]

(78)

Note that as mentioned in Section 7.3.15, the delay time calculation is an approximation and the actual time depends on the nature of the overcurrent.

8.2.2.14 Frequency Compensation Components

For this design, Type 2A compensation was used. With a target crossover frequency of 10 kHz, the guidelines shown in Section 7.3.18 are used here to determine the compensation values needed for the compensation network. The power stage transconductance is first needed in order to calculate the frequency compensation component values.

\[
\text{gm}_{\text{PS}} = \frac{N_P \times N_{\text{CSS}}}{C_{\text{CSR}} \times R_{\text{CS}} \times N_S \times N_{\text{CSP}}}
\]

(79)

\[
\text{gm}_{\text{PS}} = \frac{2.5 \times 100}{2.06 \times 7.5 \Omega \times 1 \times 1} = 16.2 \text{ A} / \text{V}
\]

(80)

With the power stage transconductance calculated as 16.2 A/V, the values of the external components needed at the COMP pin can be resolved.

\[
R_{\text{COMP}} = \frac{2\pi \times f_c \times V_{\text{OUT}} \times C_{\text{OUT}}}{\text{gm}_{\text{eA}} \times V_{\text{REF}} \times \text{gm}_{\text{PS}}}
\]

(81)

\[
R_{\text{COMP}} = \frac{2\pi \times 10 \text{ kHz} \times 5 \text{ V} \times 2.3 \text{ mF}}{1800 \times 10^{-6} \text{ A} \times 0.613 \text{ V} \times 16.2 \text{ A} / \text{V}} = 40.4 \text{ k\Omega}
\]

(82)

\[
C_{\text{COMP}} = \frac{V_{\text{OUT}} \times C_{\text{OUT}}}{I_{\text{OUT}} \times R_{\text{COMP}}}
\]

(83)

\[
C_{\text{COMP}} = \frac{5 \text{ V} \times 2.3 \text{ mF}}{20 \text{ A} \times 40.2 \text{ k\Omega}} = 14.3 \text{ nF}
\]

(84)

For the output capacitance 7 × 330-μF polymer tantalum capacitors were used to meet the 2.3-mF value that was needed for the design. At the selected switching frequency and output voltage, each of these capacitors had an ESR of roughly 6 mΩ. As such, the equivalent ESR used to determine the frequency of the ESR zero in the
frequency response is equivalent the parallel resistance of these seven capacitors, which is 0.86 mΩ. The ESR zero frequency is then used in the calculation of $C_{HF}$.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$  \hspace{1cm} (85)

$$f_{ESR} = \frac{1}{2\pi \times 2.3\text{ mF} \times 0.86\text{ mΩ}} = 80.73\text{ kHz}$$  \hspace{1cm} (86)

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{ESR}}$$  \hspace{1cm} (87)

$$C_{HF} = \frac{1}{2\pi \times 40.2\text{ kΩ} \times 80.73\text{ kHz}} = 49.04\text{ pF}$$  \hspace{1cm} (88)

The values of $R_{COMP}$, $C_{COMP}$, and $C_{HF}$ selected were 40.2 kΩ, 15 nF, and 47 pF, respectively. Note that like many other aspects of the design, the frequency compensation is often tuned during testing in order to obtain the best possible performance.

### 8.2.2.15 Slope Compensation Resistor

The slope compensation for the converter should be tailored by using the RSC pin of the TPS7H5001-SP. As recommended in Section 7.3.17, the slope compensation should be set to be equal to the falling slope of the output inductor in order to optimize sub-harmonic damping. The slope compensation that is calculated is dependent on the transformer turns ratio, current sense turns ratio, output inductor and current sense resistor that have been selected for the push-pull design.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS}$$  \hspace{1cm} (89)

$$SC = \frac{5\text{ V}}{0.47\text{ µH}} \times \frac{1}{2.5} \times \frac{1}{100} \times 7.5\Omega = 319148.94\frac{V}{s} = 0.319\text{ V/µs}$$  \hspace{1cm} (90)

$$RSC = \frac{28.3}{SC^{1.1}}$$  \hspace{1cm} (91)

$$RSC = \frac{28.3}{0.319^{1.1}} = 99.4\text{ kΩ}$$  \hspace{1cm} (92)

A resistor value of 102 kΩ is connected between RSC and AVSS for the design.
8.2.3 Application Curves

Figure 8-2. $V_{OUT}$ Soft-Start of Push-Pull Converter With $I_{OUT} = 10 \ A$

Figure 8-3. 5-A Load Step Response for Push Pull Converter
9 Power Supply Recommendations

The TPS7H5001-SP is designed to operate from an input voltage supply range between 4 V and 14 V. The input voltage supply for the controller should be well regulated and properly bypassed for best electrical performance. A minimum input bypass capacitor of 0.1 µF is required from VIN to AVSS, but additional capacitance can be used to help improve the noise and radiation performance of the controller. It is recommended to use ceramic capacitors (X5R or better) for bypassing, and these capacitors should be placed as close as possible to the controller with a low impedance path to AVSS. Additional bulk capacitors should be used if the input supply is more than a few inches from TPS7H5001-SP.
10 Layout

10.1 Layout Guidelines

In order to increase the reliability of the converter design using the TPS7H5001-SP, the following layout guidelines should be followed.

- Route the feedback trace as far away as possible from power magnetics components (inductor and/or power transformer) and other noise inducting traces on the printed circuit board (PCB) such as the switch node. If the feedback trace is routed beneath the power magnetic component, ensure that this trace is on another layer of the PCB with at least one ground layer separating the trace from the inductor or transformer.

- Minimize the copper area of the converter switch node for the best noise performance and reduction of parasitic capacitance to reduce switching losses. Ensure that any noise sensitive signals, such as the feedback trace, are routed away from this node as it contains a high dv/dt switching signal.

- All high di/dt and dv/dt switching loops in the power stage should have the paths minimized. This will help to reduce EMI, lower stresses on the power devices, and reduce any noise coupling into the control loop.

- Keep the analog ground of the controller (AVSS) separate from the power ground of the power stage that contains high frequency, high di/dt currents. These two grounds should be connected at a single point in the PCB layout. The sources of power semiconductor switches, the returns for bulk input capacitors of the power stage, and the output capacitor return should all be connected to the PCB power ground.

- All high current traces on the PCB should be short, direct, and as wide as possible. A good rule is to make the traces a minimum of 15 mils (0.381 mm) per ampere.

- Place all filtering and bypass capacitors for VIN, REFCAP, and VLDO as close as possible to the controller. Surface mount ceramic capacitors with lower ESR and ESL are recommended as these reduce the potential for noise coupling compared to through-hole capacitors. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the respective pin, and AVSS. Each bypass capacitor should have a good, low impedance connection to AVSS.

- External compensation components should be placed near the COMP pin of the controller. Surface mount components are recommended here as well.

- Attempt to keep the resistor divider used to generate the voltage at VSENSE close to the device in order to reduce noise coupling. Minimize stray capacitance to the VSENSE pin.

- OUTA, OUTB, SRA, and SRB are used to drive the inputs of a gate driver, isolator, or gate drive transformer. The PCB traces connected to these pins carry high dv/dt signals. Reduce noise coupling by routing these PCB traces away from any traces connected to VSENSE, COMP, RT, CS_ILIM, HICC, LEB, RSC, PS, and SP.

- In addition to utilizing the leading edge blank time programmability of the controller, RC filtering may be required for the sensed current signal input to CS_ILIM. Keep the resistor and capacitor in close vicinity to CS_ILIM to filter any ringing and/or spikes that may be present on the sensed current signal.

- When operating in internal oscillator mode with SYNC as an output, route the SYNC signal away from noise sensitive signals/pins such as VSENSE, COMP, RT, CS_ILIM, LEB, RSC, PS, and SP. Special care should be taken to eliminate noise from SYNC to HICC since these pins are adjacent to one another. It is recommended that the capacitor from HICC to AVSS be at least 3.3 nF to help with the reduction of the noise.

- Connect the backside metallization of the TPS7H5001-SP to the AVSS plane of the PCB using multiple vias. It is recommended to avoid putting solder paste directly on top of the vias unless these vias are tented or filled.
10.2 Layout Example

Connect backside metallization of device to AVSS using multiple vias

Keep compensation components as close to COMP pin as possible

Keep feedback trace away from noise inducing signals and components

Keep current sense filter close to the device

Keep output signals to gate drivers away from noise sensitive signals

Figure 10-1. PCB Layout Example
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H5001-SP Evaluation Module user's guide*
- Texas Instruments, *TPS7H5001-SP Lookahead Total Ionizing Dose (TID) radiation report*
- Texas Instruments, *TPS7H5001-SP Single-Event Effects (SEE) radiation report*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

**TI Glossary**  
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metallization
EXAMPLE BOARD LAYOUT

HFT0022A

CFP - 2.428mm max height

CERAMIC FLATPACK

HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

PKG

PKG

(R0.05) TYP

(0.605)

(0.955) TYP

(1.14) TYP

(1.115)

(7.29)

(3.62)

(\(\varnothing 0.2\)) TYP

4225791/C 01/2021
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<td>2192775</td>
<td>01/28/2021</td>
<td>R. RAZAK / ANIS FAUZI</td>
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## PACKAGING INFORMATION

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<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>PTPS7H5001HFT EVAL ONLY</td>
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(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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