TPS8268x 1600-mA High-Efficiency MicroSiP™ Step-Down Converter Module (Profile < 1.0mm)

1 Features

- Wide V_{IN} Range From 2.5V to 5.5V
- Total Solution Size < 6.7 mm^2
- Sub 1-mm Profile Solution
- ±1.5% DC Voltage Accuracy
- Up to 1600-mA Load Current
- Up to 90% Efficiency
- Fixed Output Voltage:
  - TPS8268180: 1.80V
  - TPS8268150: 1.50V
  - TPS8268120: 1.20V
  - TPS8268105: 1.05V
  - TPS8268090: 0.90V
- Low EMI by Spread Spectrum PWM Frequency Dithering
- *Best in Class* Load and Line Transient Response
- Internal Soft Start
- Current Overload and Thermal Shutdown Protection

2 Applications

- Optical Modules
- Cell Phones, Smart-Phones
- Solid State Disk Drive Applications
- Space constrained applications

3 Description

The TPS8268x device is a complete DC/DC step-down power supply optimized for small solution size. Included in the package are the switching regulator, inductor and input/output capacitors. Integration of all passive components enables a tiny solution size of only 6.7mm^2.

The TPS8268x is based on a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications in which high load currents in a very small solution size and height are required. The TPS8268x is optimized for high efficiency and low output voltage ripple and supports up to 1600-mA load current. With an input voltage range of 2.5-V to 5.5-V, the device supports applications powered by Li-Ion batteries as well as 5-V and 3.3-V rails.

The TPS8268x operates at a 5.5-MHz switching frequency with spread spectrum capability. For noise-sensitive applications, this provides a lower noise regulated output, as well as low noise at the input. The device supports a fixed output voltage, requiring no external feedback network.

These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency with the same size.

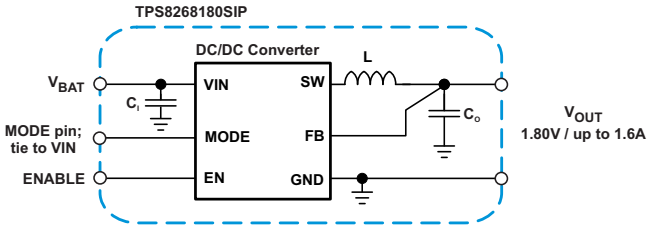
The TPS8268x is packaged in a compact (2.3mm x 2.9mm) and low profile BGA package suitable for automated assembly by standard surface mount equipment.

Device Information(1)

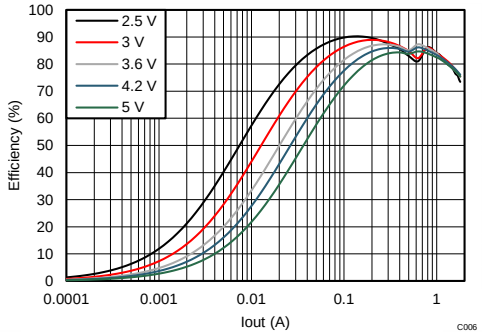
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS8268180	µSIP	2.30 mm × 2.90 mm
TPS8268150	µSIP	2.30 mm × 2.90 mm
TPS8268120	µSIP	2.30 mm × 2.90 mm
TPS8268105	µSIP	2.30 mm × 2.90 mm
TPS8268090	µSIP	2.30 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Efficiency vs Load Current for TPS8268180



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision B (June 2015) to Revision C — **Page**

- Deleted "Preview" from Device Comparison Table and Electrical Characteristics table for TPS8268120 and TPS8268180 devices ... 3

Changes from Revision A (November 2014) to Revision B — **Page**

- Added Preview devices TPS8268180 and TPS8268120 specifications and typical application curves to the data sheet. ... 1
- Moved timing specs from Electrical Characteristics table to Timing Requirements table ... 6

Changes from Original (October 2014) to Revision A — **Page**

- Changed from Product Preview to Production Data ... 1

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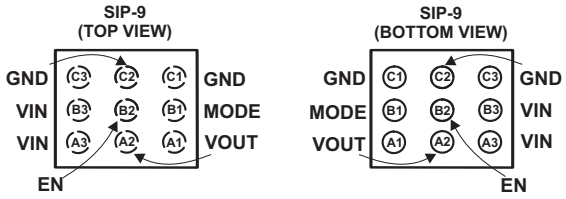
5 Device Comparison Table (1)

DEVICE NUMBER	FEATURES	OUTPUT VOLTAGE	Marking
TPS8268180	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.80V	HK
TPS8268150	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.50V	YR
TPS8268120	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.20V	HJ
TPS8268105	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.05V	YO
TPS8268090	PWM Spread Spectrum Modulation Output Capacitor Discharge	0.90V	YP

(1) For other voltage options please contact a TI sales representative.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1, A2	O	Power output pin. Apply output load between this pin and GND.
VIN	A3, B3	I	Supply voltage connection
EN	B2	I	This is the enable pin of the device. Connecting this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
MODE	B1	I	This pin must be tied to the input supply voltage VIN.
GND	C1, C2, C3	–	Ground pin.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Voltage at VIN(2)	–0.3	6	V
	Voltage at VOUT(2)	–0.3	3.6	
	Voltage at EN, MODE(2)	–0.3	V_{IN} + 0.3	
	Peak output current		1600	mA
T_J	Operating internal junction temperature range	–40	125	°C
T_{stg}	Storage temperature range	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1) (2)	Human body model	±2000	V
		Charge device model	±500	V
		Machine model	±100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VIN	Input voltage range		2.5		5.5	V
I_{OUT}	Peak output current for TPS8268090, TPS8268105, TPS8268120	VIN ≥ 2.8V	0		1600(1)	mA
	Peak output current for TPS8268150, TPS8268180	VIN ≥ 3.2V				
I_{OUT}	Average output current for TPS8268090, TPS8268105, TPS8268120	VIN ≥ 2.7V	0		1200(1)	mA
	Average output current for TPS8268150, TPS8268180	VIN ≥ 2.9V				
I_{OUT}	Average output current during soft-start	Vout ≤ 0.9 x $V_{OUT,nom}$	0		1000(2)	mA
	Additional effective input capacitance		0			µF
	Additional effective output capacitance		0		30(3)	µF
T_A	Operating ambient temperature range		–40		85	°C

(1) See *Thermal and Reliability Information* for additional details
(2) See *Soft Start* for additional details
(3) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied.

7.4 Thermal Information

THERMAL METRIC(1)		TPS8268x SIP 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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Thermal Information (continued)

THERMAL METRIC[1]		TPS8268x SIP 9 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

7.5 Electrical Characteristics

Minimum and maximum values are at VIN = 2.5 V to 5.5 V, EN = VIN and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at VIN = 3.6 V, EN = VIN and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current		I_{OUT} = 0mA		7		mA
I_{SD}	Shutdown current		EN = low		0.5	5	µA
UVLO	Undervoltage lockout threshold		VIN rising		2.1	2.3	V
			VIN falling		1.95	2.25	V
ENABLE, MODE							
V_{IH}	High-level input voltage			0.9			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN; T_J = –40°C to 85°C		0.01	1.5	µA
PROTECTION							
	Thermal shutdown		Temperature rising		140		°C
	Thermal shutdown hysteresis		Temperature falling		10		°C
I_{LIM}	Average output current limit				2100		mA
I_{SC}	Input current limit under short-circuit condition		V_{OUT} shorted to ground		150		mA
OUTPUT							
$V_{OUT,NOM}$	Nominal output voltage	TPS8268180			1.80		V
		TPS8268150			1.50		V
		TPS8268120			1.20		V
		TPS8268105			1.05		V
		TPS8268090			0.90		V
	Output voltage accuracy	TPS8268120, TPS8268105, TPS8268090	2.8V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1600 mA T_J = –40°C to 85°C	0.985×$V_{OUT,NOM}$	$V_{OUT,NOM}$	1.015×$V_{OUT,NOM}$	V
		TPS8268180, TPS8268150	3.2V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1600 mA T_J = –40°C to 85°C				
		TPS8268120, TPS8268105, TPS8268090	2.7V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1200 mA T_J = –40°C to 125°C	0.98×$V_{OUT,NOM}$	$V_{OUT,NOM}$	1.025×$V_{OUT,NOM}$	V
		TPS8268180, TPS8268150	2.9V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1200 mA T_J = –40°C to 125°C				
	Line regulation		VIN = 2.5V to 5.5V, I_{OUT} = 200 mA		0.2		%/V
	Load regulation		I_{OUT} = 0mA to 1600 mA		–0.85		%/A
f_{SW}	Nominal oscillator frequency		I_{OUT} = 0mA		5.5		MHz
R_{DIS}	VOUT discharge resistor				12		Ω

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7.6 Timing Requirements

Minimum and maximum values are at VIN = 2.5 V to 5.5 V, EN = VIN and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at VIN = 3.6 V, EN = VIN and T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Start-up delay time	Time from EN = high to start switching		120	300	µs
t_{RAMP}	Ramp time	I_{OUT} = 0mA, Time from start switching until 95% of nominal output voltage		150		µs

7.7 Typical Characteristics

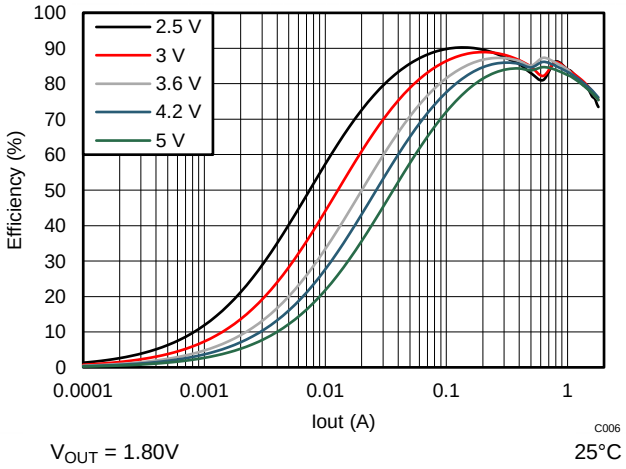

Figure 1. Efficiency vs Output Current

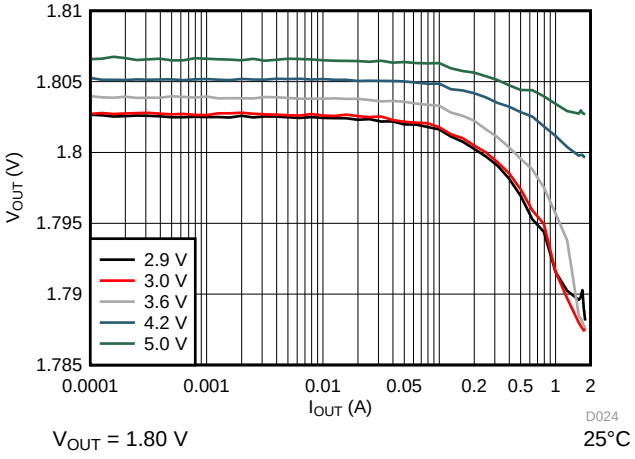

Figure 2. Output Voltage vs Output Current

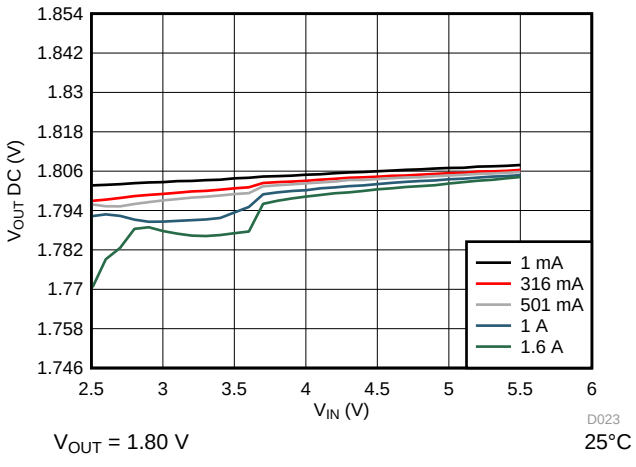

Figure 3. Output Voltage vs Input Voltage

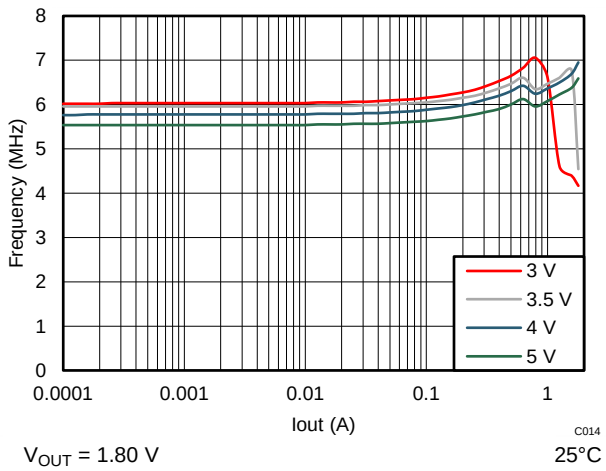

Figure 4. Switching Frequency vs Output Current

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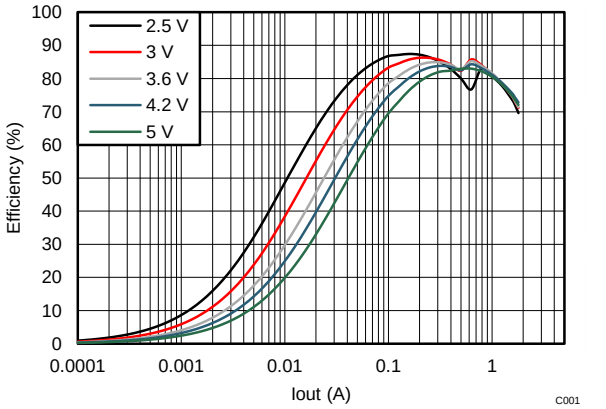
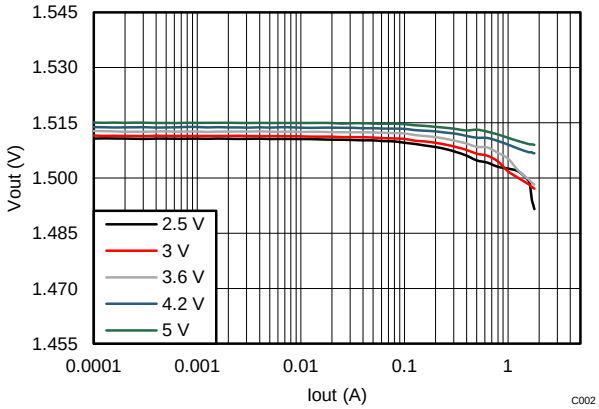
Typical Characteristics (continued)



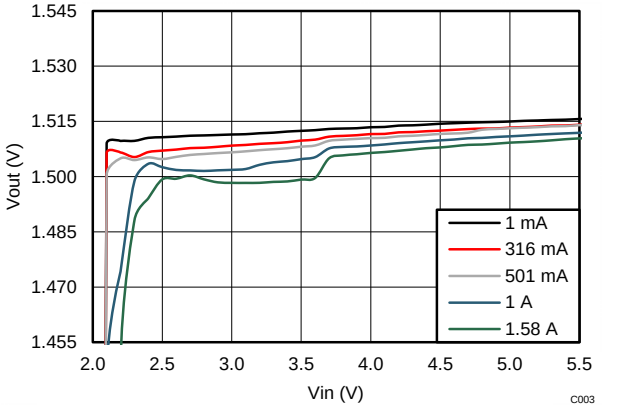
V_{OUT} = 1.50V 25°C

Figure 5. Efficiency vs Output Current



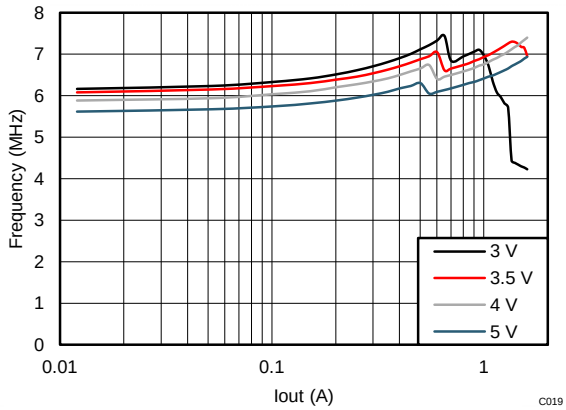
V_{OUT} = 1.50 V 25°C

Figure 6. Output Voltage vs Output Current



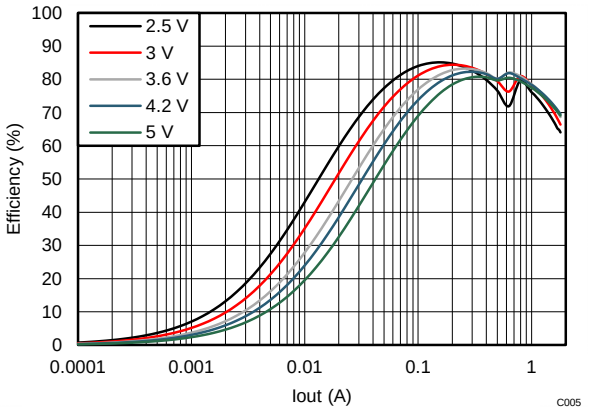
V_{OUT} = 1.50 V 25°C

Figure 7. Output Voltage vs Input Voltage



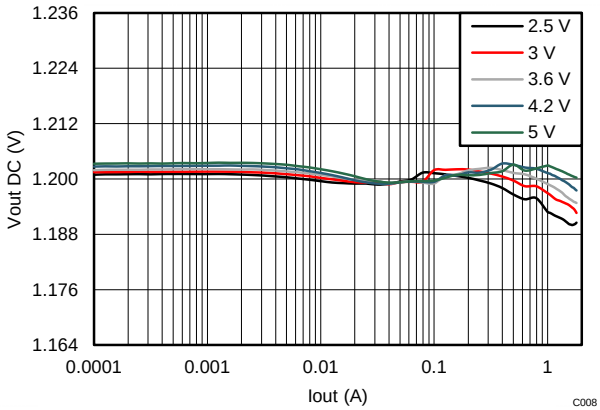
V_{OUT} = 1.50 V 25°C

Figure 8. Switching Frequency vs Output Current



V_{OUT} = 1.20V 25°C

Figure 9. Efficiency vs Output Current



V_{OUT} = 1.20 V 25°C

Figure 10. Output Voltage vs Output Current

Typical Characteristics (continued)

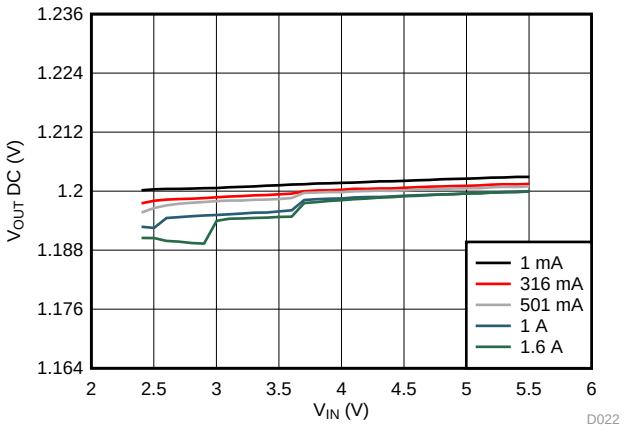


Figure 11. Output Voltage vs Input Voltage

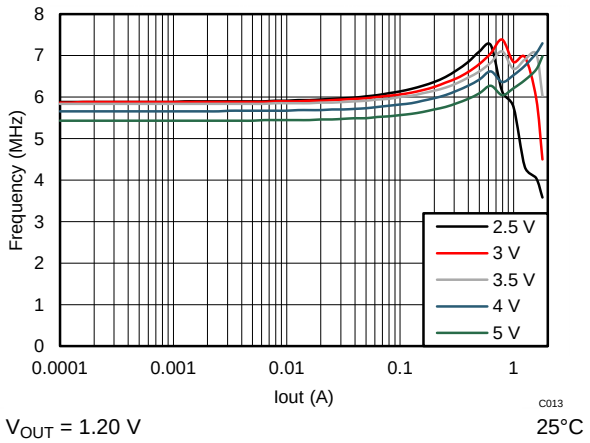


Figure 12. Switching Frequency vs Output Current

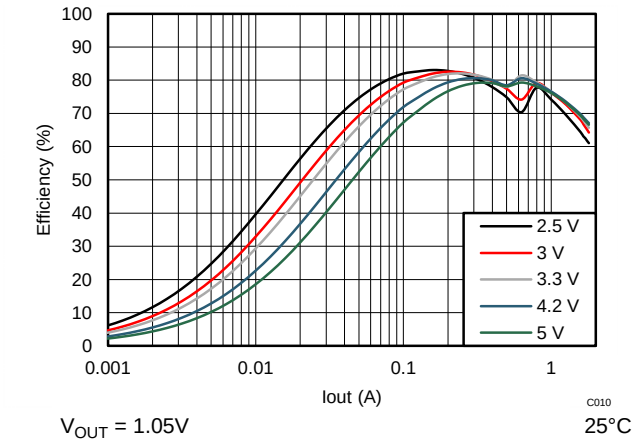


Figure 13. Efficiency vs Output Current

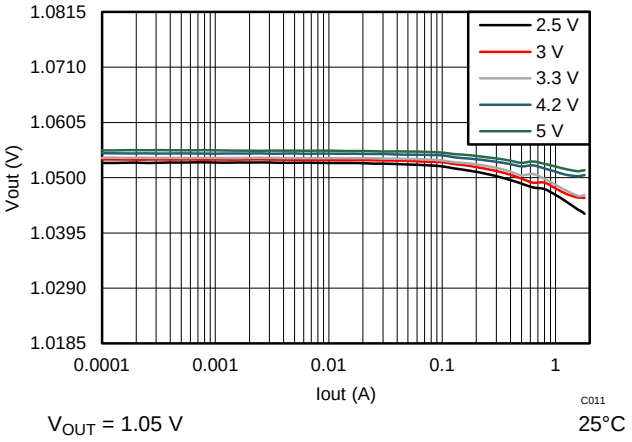


Figure 14. Output Voltage vs Output Current

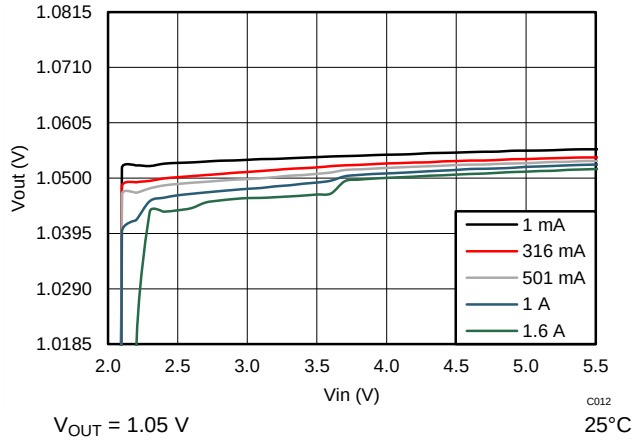


Figure 15. Output Voltage vs Input Voltage

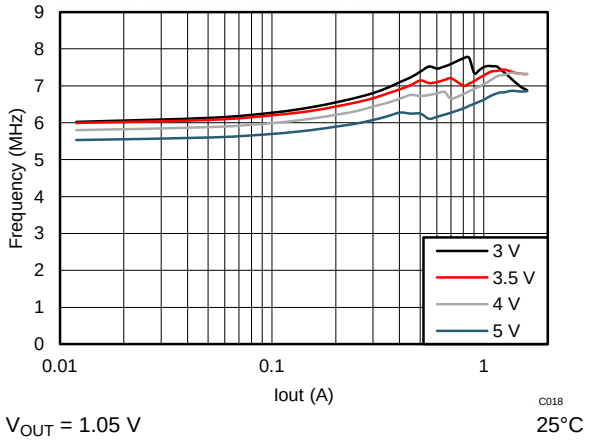


Figure 16. Switching Frequency vs Output Current

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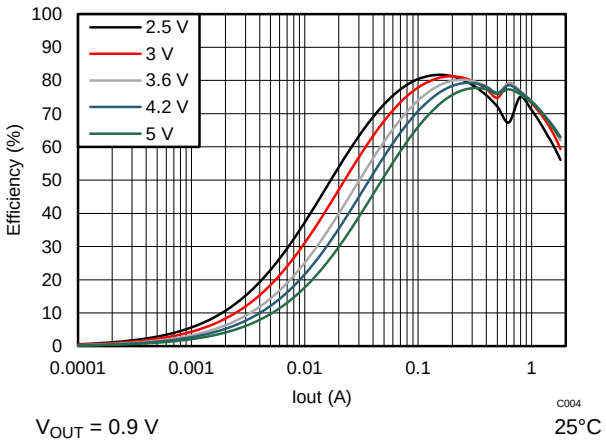
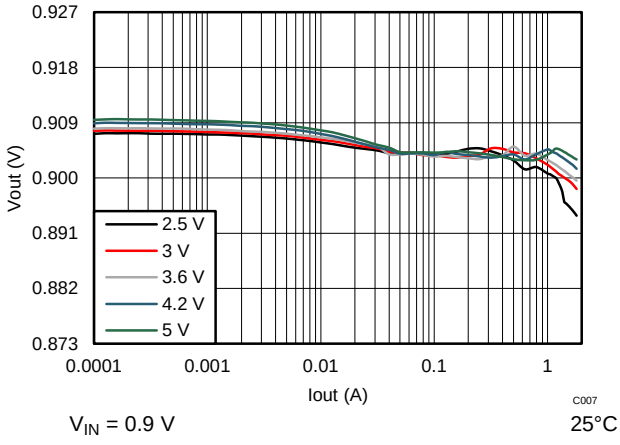
Typical Characteristics (continued)



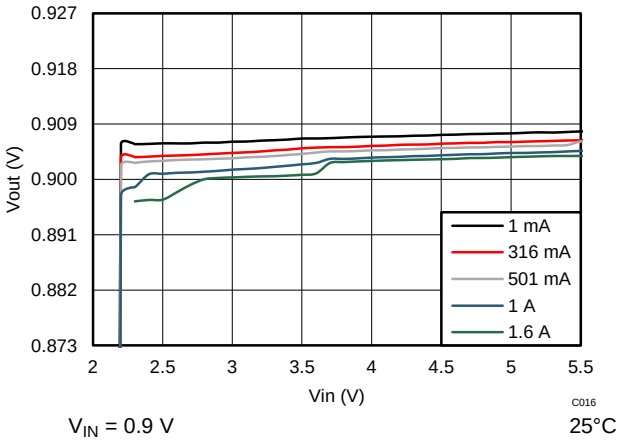
V_{OUT} = 0.9 V 25°C

Figure 17. Efficiency vs Output Current



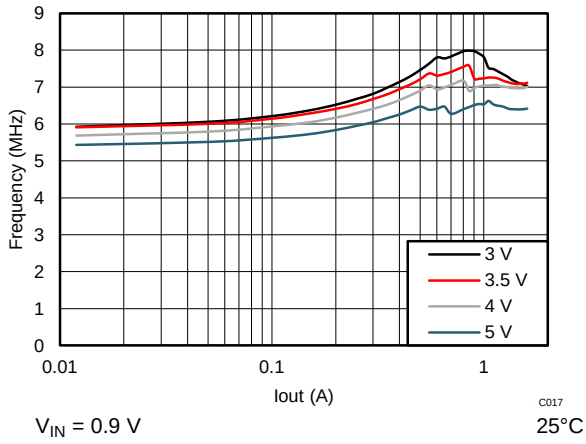
V_{IN} = 0.9 V 25°C

Figure 18. Output Voltage vs Output Current



V_{IN} = 0.9 V 25°C

Figure 19. Output Voltage vs Input Voltage



V_{IN} = 0.9 V 25°C

Figure 20. Switching Frequency vs Output Current

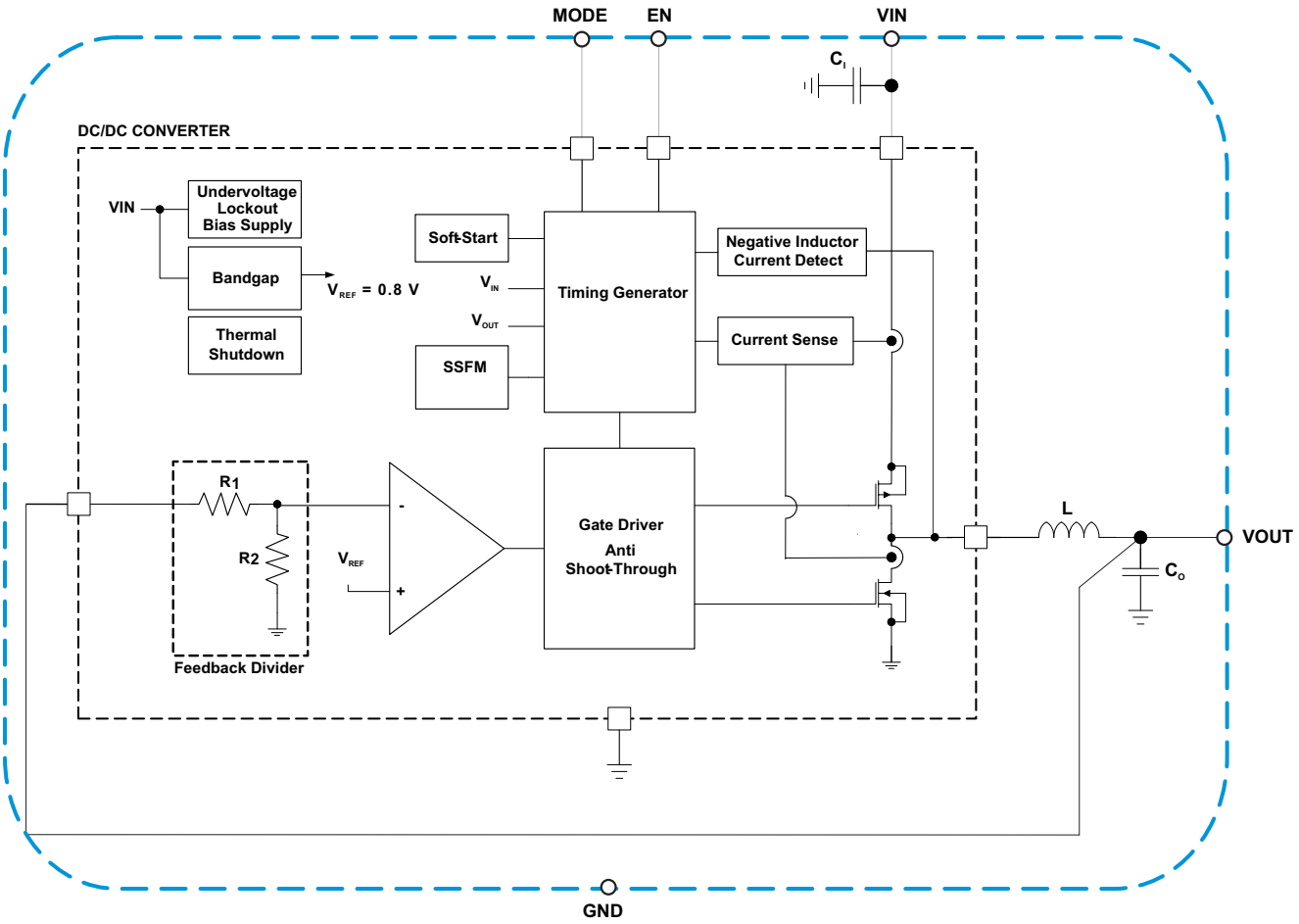
8 Detailed Description

8.1 Overview

The TPS8268x is a complete DC/DC step-down power supply intended for small size and low profile applications. Included in the package are the switching regulator, inductor and input/output capacitors. It is a complete Plug & Play Solution, meaning typically no additional components are required to finish the design. Integration of all required passive components enables a tiny solution size of only 6.7mm^2. The converter operates with fixed frequency pulse width modulation (PWM).

The TPS8268x integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft Start

The TPS8268x has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold V_{UVLO}, the output voltage ramps up to 95% of its nominal value within t_{Ramp} of typ. 150µs. This ensures a controlled ramp up of the output voltage and limits the input voltage drop when a battery or a high-impedance power source is connected to the input of the DC/DC converter.

The inrush current during start-up is directly related to the effective capacitance and load present at the output of the converter.

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Feature Description (continued)

During soft start, the current limit is reduced to 2/3 of its nominal value. The maximum load current during soft start should be less than 1A. Once the internal reference voltage has reached 90% of its target value, the current limit is set to its nominal target value.

8.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on either MOSFET under undefined conditions. The TPS8268x has a rising UVLO threshold of 2.1V (typical).

8.3.3 Short-Circuit Protection

The TPS8268x integrates current limit circuitry to protect the device against heavy load or short circuits. When the average current in the high-side MOSFET reaches its current limit, the high-side MOSFET is turned off and the low-side MOSFET is turned on ramping down the inductor current.

As soon as the converter detects a short circuit condition, it shuts down. After a delay of approximately 20 µs, the converter restarts. In case the short circuit condition remains, the converter shuts down again after hitting the current limit threshold. In case the short circuit condition remains present on the converters output, the converter periodically re-starts with a small duty cycle and shuts down again, thereby limiting the current drawn from the input.

8.3.4 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the power stage is turned off. The device continues its operation when the junction temperature falls below typically 130°C.

8.3.5 Enable

The TPS8268x device starts operation when EN is set high. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 0.5µA. In this mode, the internal high-side and low-side MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal control circuitry is switched off. The TPS8268x device actively discharges the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 12Ω. This internal discharge transistor is only turned on after the device had been enabled at least once. The required time to discharge the output capacitor at the output node depends on load current and the effective output capacitance.

The TPS8268x is designed such that it can start into a pre-biased output, in case the output discharge circuit was active for too short a time to fully discharge the output capacitor. In this case, the converter starts switching as soon as the internal reference has approximately reached the equivalent voltage to the output voltage present. It then ramps the output from that voltage level to its target value.

8.3.6 MODE Pin

This pin must be tied to the input voltage VIN and must not be left floating.

8.4 Device Functional Modes

8.4.1 Spread Spectrum, PWM Frequency Dithering

The goal is to spread out the emitted RF energy over a larger frequency range, so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

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Device Functional Modes (continued)

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to their output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by around ±10% of the nominal switching frequency, thereby significantly reducing the peak radiated and conducted noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

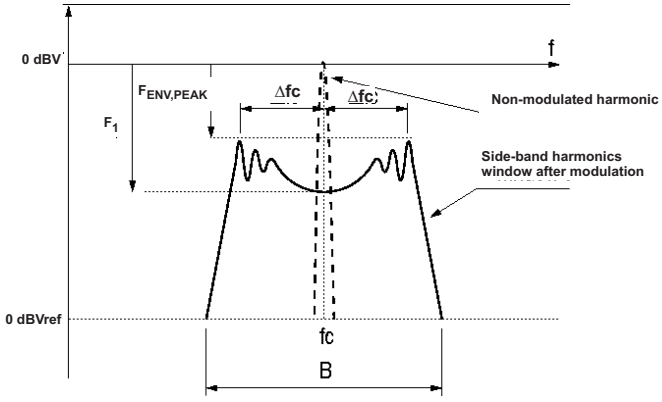

Figure 21. Spectrum Of A Frequency Modulated Sin. Wave With Sinusoidal Variation In Time

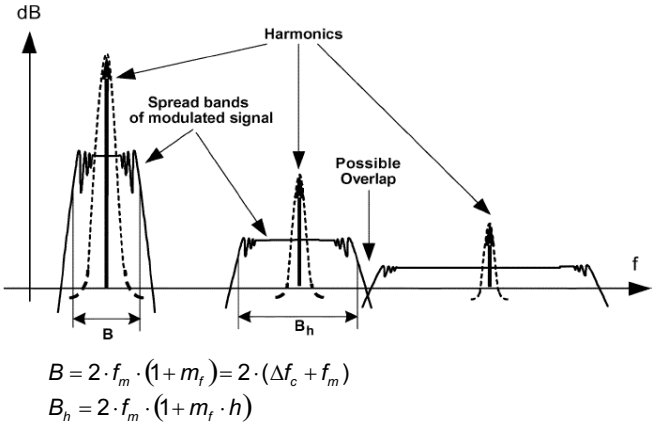

Figure 22. Spread Bands Of Harmonics In Modulated Square Signals (1)

The above figures show that after modulation the side-band harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (m_f), the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

where:

- f_c is the carrier frequency (5.5 MHz)
- f_m is the modulating frequency (approx. 0.008*f_c)
- δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency f_c is limited by the device and finally the parameter modulation ratio (δ), together with f_m , which is the side-band harmonic´s bandwidth around the carrier frequency f_c . The bandwidth of a frequency modulated waveform is approximately given by Carson's rule and is summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

f_m < RBW (resolution bandwidth): The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

(1) Spectrum illustrations and formulae (Figure 21 and Figure 22) copyright *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY*, VOL. 47, NO.3, AUGUST 2005. See *References* Section for full citation.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS8268x device is a complete DC/DC step-down power supply optimized for small solution size. Included in the package are the switching regulator, inductor and input/output capacitors. Integration of passive components enables a tiny solution size of only 6.7mm^2.

9.2 Typical Application

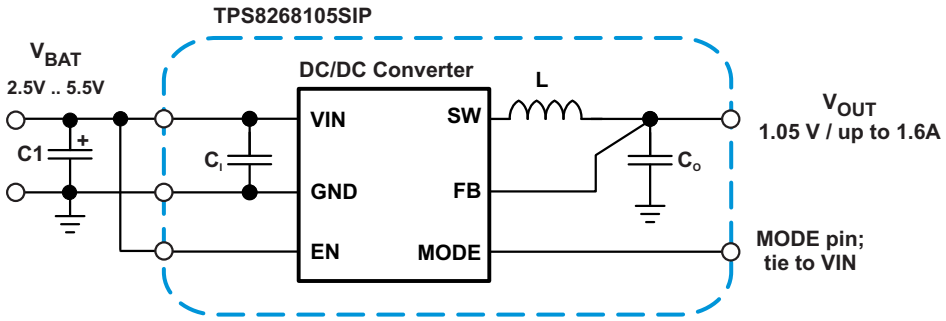

Figure 23. Typical Application Schematic

9.2.1 Design Requirements

Figure 23 shows the schematic of the typical application. The following design guidelines provide all information to operate the device within the recommended operating conditions. An external input capacitor may be required depending on the source impedance of the battery or pre-regulator used to power TPS8268x. See also *Power Supply Recommendations*.

Reference	Description	Manufacturer
IC1	MicroSIP Module TPS8268xSIP	Texas Instruments
C1	Tantalum Capacitor; T520B157M006ATE025; 150uF/6.3V	Kemet

9.2.2 Detailed Design Procedure

The TPS8268x allows the design of a complete power supply with no additional external components. The input capacitance can be increased in case the source impedance is large or if there are high load transients expected at the output. The dc bias effect of the input and output capacitors must be taken into account and the total capacitance on the output must not exceed the value given in the recommended operating conditions.

9.2.2.1 Input Capacitor Selection

Because the nature of the buck converter has a pulsating input current, a low ESR input capacitor is required.

For most applications, the input capacitor that is integrated into the TPS8268x is sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

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The TPS8268x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

9.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS8268x allows the use of tiny ceramic output capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For most applications, the output capacitor integrated in the TPS8268x is sufficient. An additional output capacitor may be used for the purpose of improving AC voltage accuracy during large load transients.

To further reduce the voltage drop during load transients, additional external output capacitance up to 30µF can be added. A low ESR multilayer ceramic capacitor (MLCC) is suitable for most applications. The total effective output capacitance must remain below 30µF.

As the device operates in PWM mode, the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor´s ESL and the ripple current that flows through the output capacitor´s impedance.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PCB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter´s small and large signal behavior should be checked over the input voltage range, load current range and temperature range.

The easiest test is to evaluate, directly at the converter's output, the following items:

- efficiency
- load transient response
- output voltage ripple

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop typically has more than 45° of phase margin.

9.2.3 Application Curves

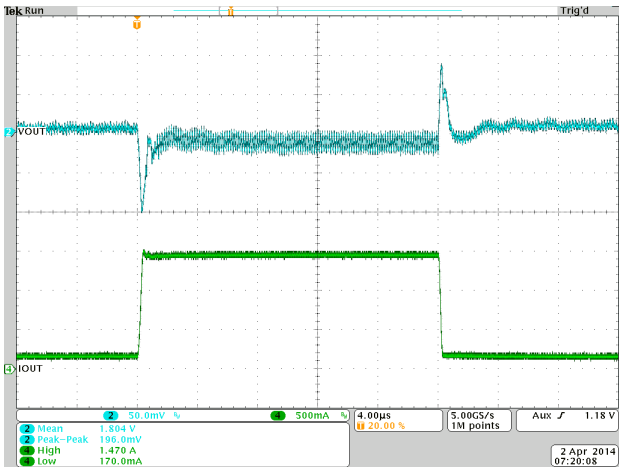

Figure 24. Load Transient Response for TPS8268180 (Vout = 1.80V, Iout = 170mA to 1.47A to 170mA, Vin = 5V)

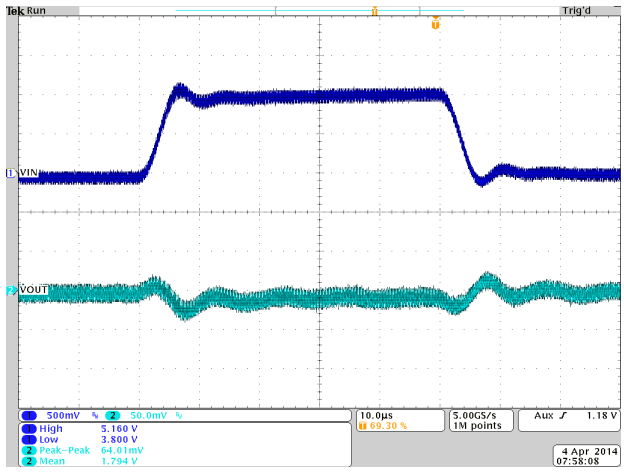

Figure 25. Line Transient Response for TPS8268180 (Vout = 1.80V; Iout = 800mA, Vin = 4V to 5V to 4V)

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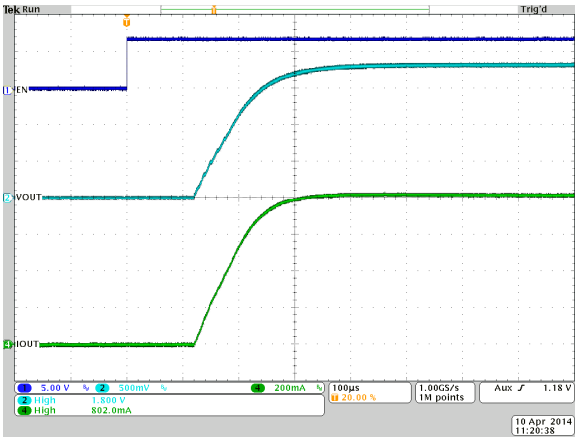

Figure 26. Startup for TPS8268180 (Vin = 5V, Vout = 1.80V)

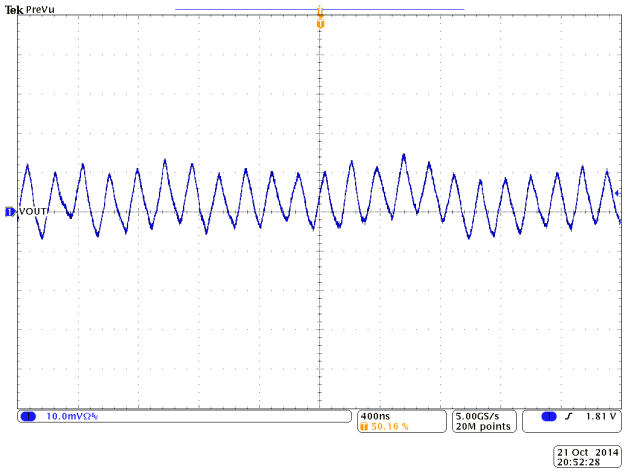

Figure 27. Output Voltage Ripple for TPS8268180 (Vin = 5V, Vout = 1.80V, Iout = 900mA)

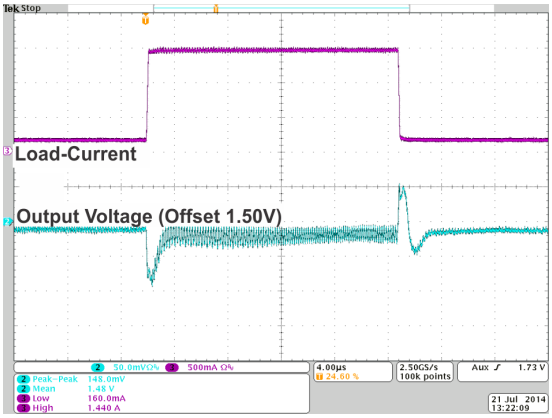

Figure 28. Load Transient Response for TPS8268150 (Vout = 1.5V, Iout = 160mA to 1.44A to 160mA, Vin = 5V)

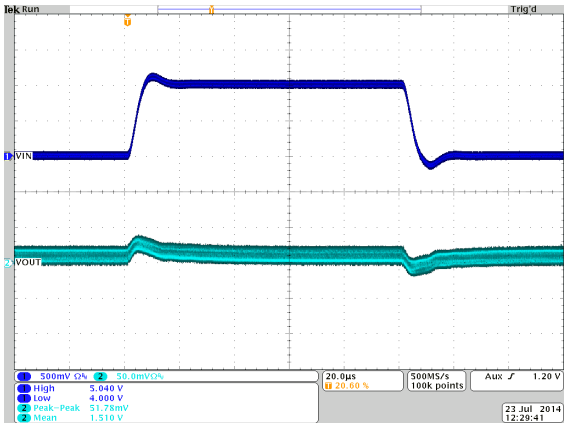

Figure 29. Line Transient Response for TPS8268150 (Vout = 1.5V, Iout = 800mA, Vin = 4V to 5V to 4V)

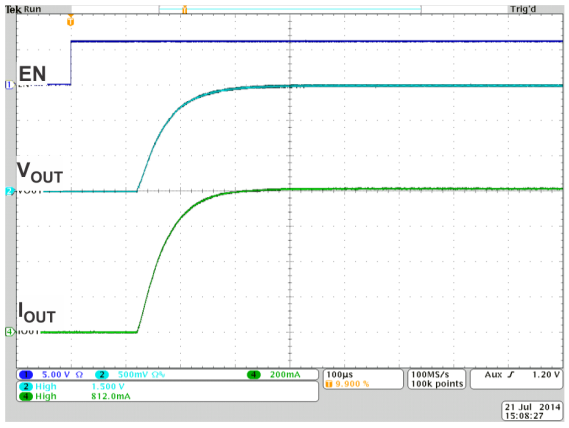

Figure 30. Startup for TPS8268150 (Vin = 5V, Vout = 1.5V)

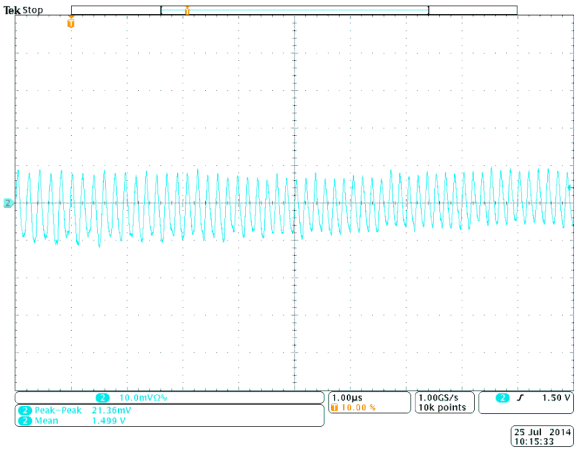

Figure 31. Output Voltage Ripple for TPS8268150 (Vin = 5V, Vout = 1.5V, Iout = 900mA)

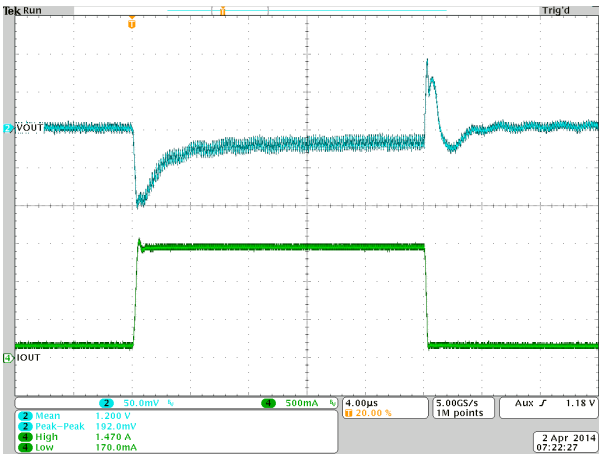

Figure 32. Load Transient Response for TPS8268120 (Vout = 1.20V, Iout = 170mA to 1.47A to 170mA, Vin = 5V)

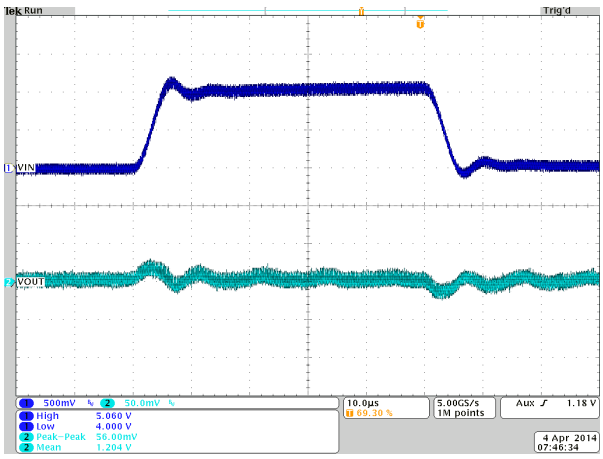

Figure 33. Line Transient Response for TPS8268120 (Vout = 1.20V; Iout = 800mA, Vin = 4V to 5V to 4V)

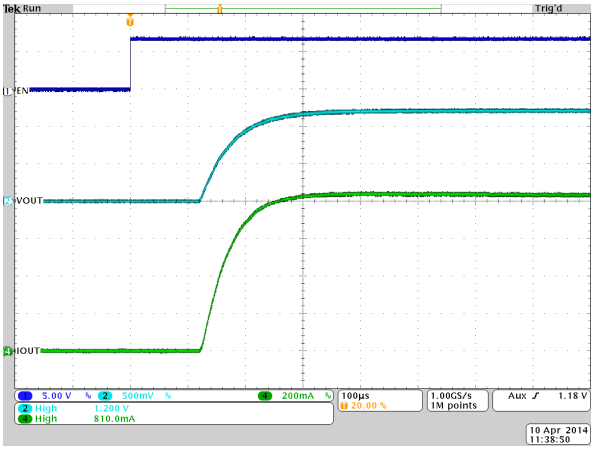

Figure 34. Startup for TPS8268120 (Vin = 5V, Vout = 1.20V)

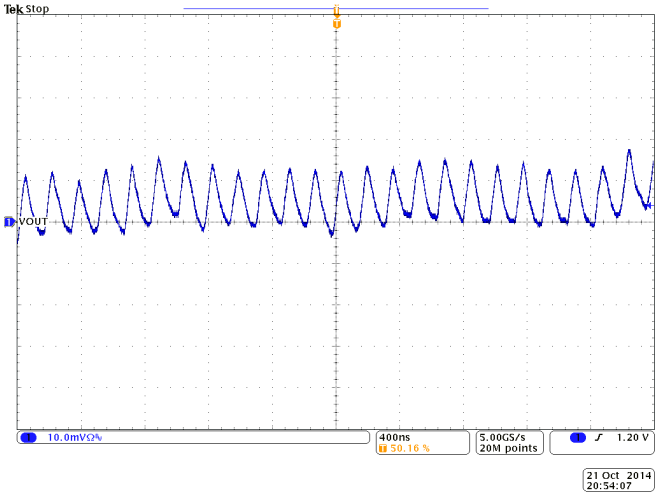

Figure 35. Output Voltage Ripple for TPS8268120 (Vin = 5V, Vout = 1.20V, Iout = 900mA)

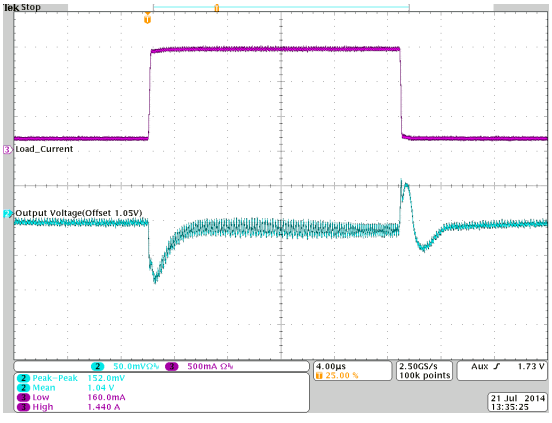

Figure 36. Load Transient Response for TPS8268105 (Vout = 1.05V, Iout = 160mA to 1.44A to 160mA, Vin = 5V)

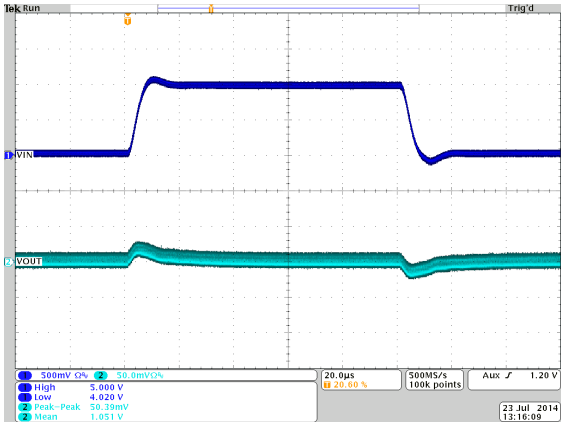

Figure 37. Line Transient Response for TPS8268105 (Vout = 1.05V; Iout = 900mA, Vin = 4V to 5V to 4V)

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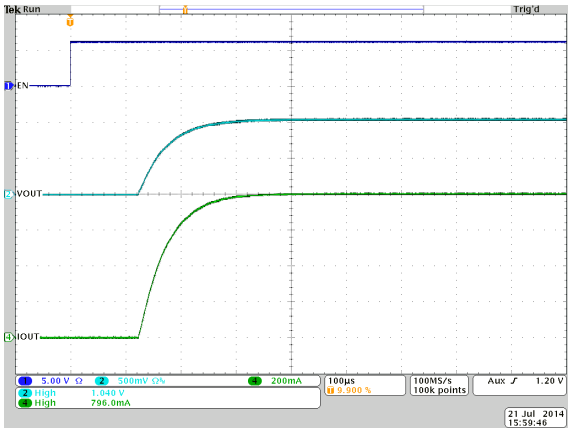

Figure 38. Startup for TPS8268105 (Vin = 5V, Vout = 1.05V)

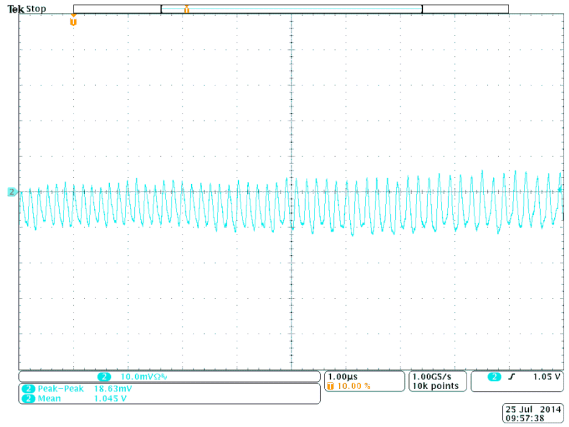

Figure 39. Output Voltage Ripple for TPS8268105 (Vin = 5V, Vout = 1.05V, Iout = 900mA)

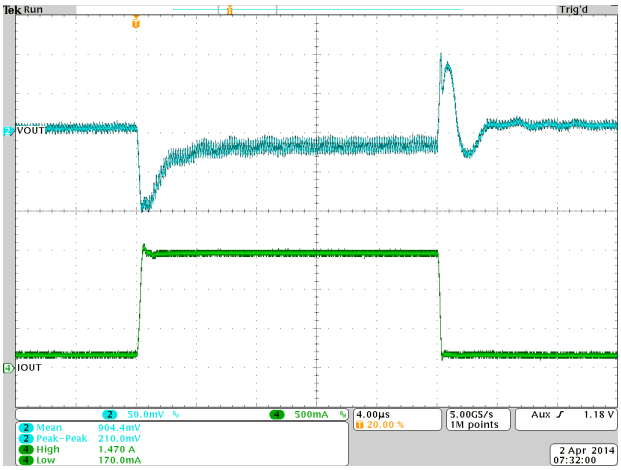

Figure 40. Load Transient Response for TPS8268090 (Vout = 0.9V, Iout = 170mA to 1.47A to 170mA, Vin = 5V)

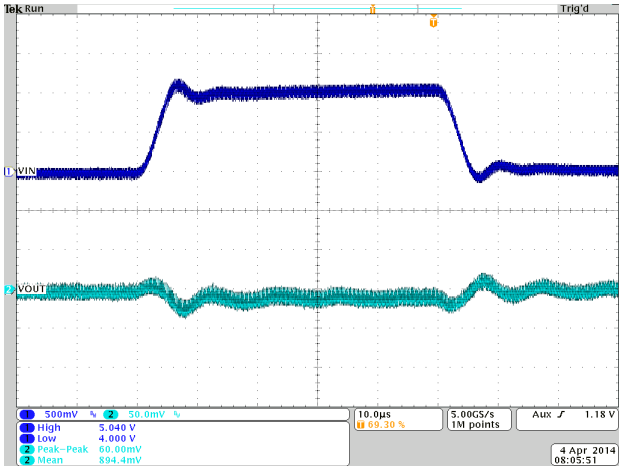

Figure 41. Line Transient Response for TPS8268090 (Vout = 0.90V; Iout = 900mA, Vin = 4V to 5V to 4V)

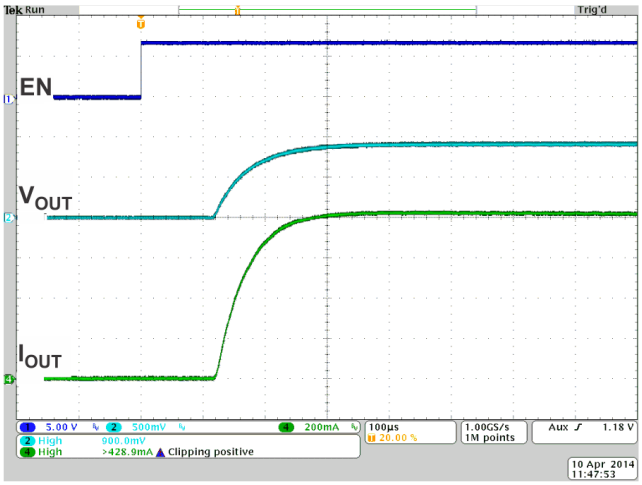

Figure 42. Startup for TPS8268090 (Vin = 5V, Vout = 0.9V)

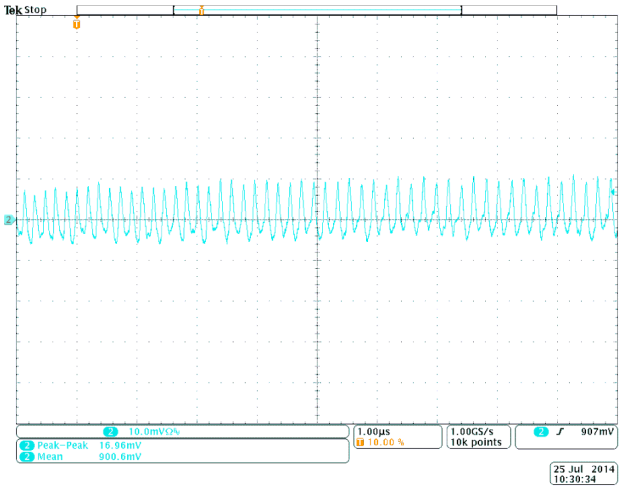

Figure 43. Output Voltage Ripple for TPS8268090 (Vin = 5V, Vout = 0.9V, Iout = 900mA)

10 Power Supply Recommendations

The input power supply to the TPS8268x must have a current rating according to the input voltage and output current of the TPS8268x. TPS8268x provides a fast transient response due to its high switching frequency and fast control loop. For highly dynamic loads, the device demands high inputs currents within a short time. The power supply to TPS8268x therefore needs to have a low output impedance in order to keep the input voltage stable during fast load changes. Make sure the input voltage to TPS8268x at any time is above the minimum voltage level required to supply the load at the output. See the electrical characteristics for the minimum input voltage for a given load current for the different output voltage versions. Additional input capacitance needs to be added if the input voltage dops below the minimum level required.

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11 Layout

11.1 Layout Guidelines

TPS8268x allows the design of a power supply with small solution size. In order to properly dissipate the heat, wide copper traces for the power connections should be used to distribute the heat across the PCB. If possible, a GND plane should be used as it provides a low impedance connection as well as serves as a heat sink.

In making the pad size for the SiP LGA balls, it is recommended that the layout use a non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 44 shows the appropriate diameters for a MicroSiP™ layout.

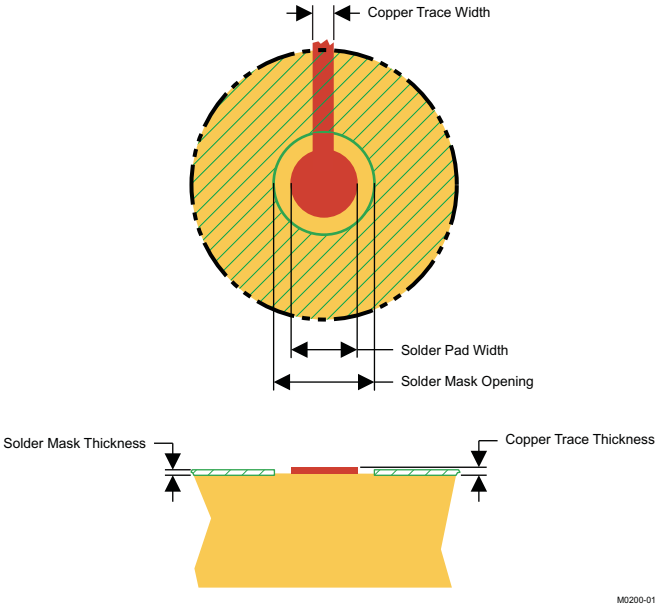

Figure 44. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PCB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and slightly reduce reliability. However, wider traces may be used to improve the thermal relief of the device as well as to provide sufficient current handling.
(2) Best reliability results are achieved when the PCB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PCB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

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11.2 Layout Example

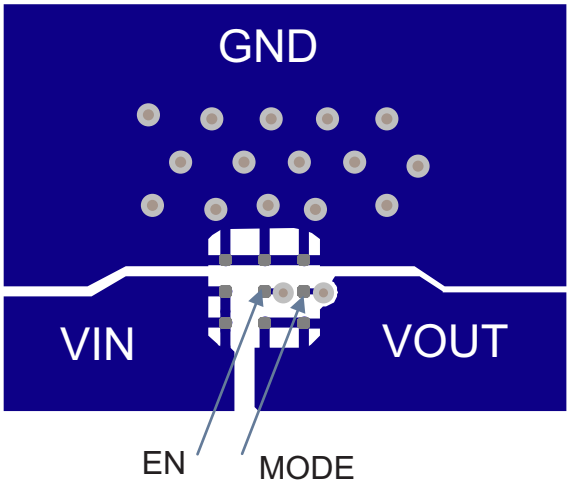

Figure 45. Recommended PCB Layout

11.3 Surface Mount Information

The TPS8268x MicroSiP™ DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum to allow the MicroSiP™ device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

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11.4 Thermal and Reliability Information

The TPS8268x´s output current may need to be de-rated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current de-rating is dependent upon the input voltage, output power and environmental thermal conditions. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS8268x die and inductor temperature should be kept lower than the maximum rating of 125°C, so care should be taken in the circuit layout to ensure good heat sinking. Sufficient cooling should be provided to ensure reliable operation.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the junction temperature, approximate the power dissipation within the TPS8268x by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking an actual power measurement. Then, calculate the internal temperature rise of the TPS8268x above the surface of the printed circuit board by multiplying the TPS8268x´s power dissipation by its thermal resistance.

The thermal resistance numbers listed in the Thermal Information table are based on modeling the MicroSiP™ package mounted on a high-K test board specified per the JEDEC standard. For increased accuracy and fidelity to the actual application, it is recommended to run a thermal image analysis of the actual system.

Thermal measurements have been taken on the EVM to give a guideline on what temperature can be expected when the device is operated in free air at 25°C ambient under a certain load. The temperatures have been checked at 4 different spots as listed below:

- Spot1: temperature of the input capacitor
- Spot2: temperature of the output capacitor
- Spot3: temperature of the inductor
- Spot4: temperature on the main pcb next to the module

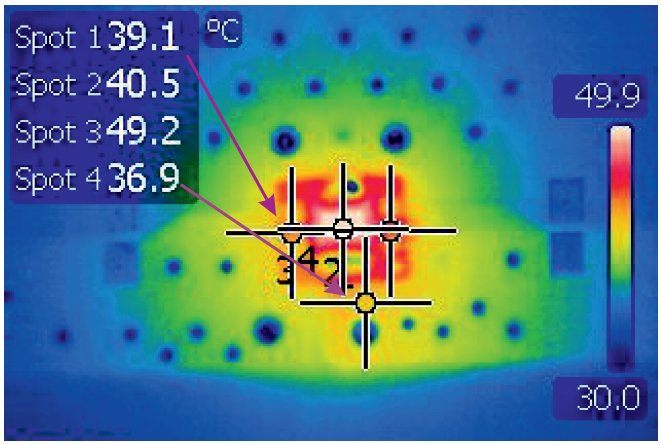

Figure 46. V_{IN}= 5V, V_{OUT}=1.05V, I_{OUT}= 1A 388mW Power Dissipation

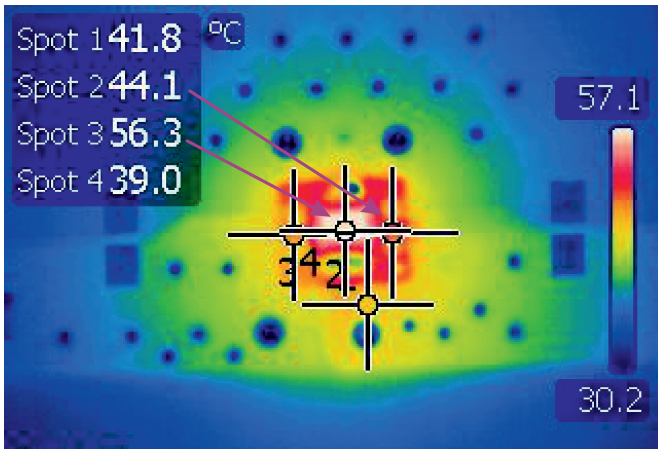

Figure 47. V_{IN}= 5V, V_{OUT}= 1.05V, I_{OUT}= 1.2A 466mW Power Dissipation

The TPS8268x contains a thermal shutdown that inhibits switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the components internal to the MicroSiP™ package are subjected to high temperatures for prolonged or repetitive intervals, which may decrease the reliability of the device.

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Thermal and Reliability Information (continued)

MLCC capacitor reliability/lifetime depends on temperature and applied voltage. At higher temperatures, MLCC capacitors are subject to stronger stress. On the basis of frequently evaluated failure rates determined with standardized test conditions, the reliability of all MLCC capacitors can be calculated for their actual operating temperature and voltage.

Failures caused by systematic degradation are described by the Arrhenius model. The most critical parameter (IR) is the Insulation Resistance (i.e. leakage current). The drop of IR below a lower limit (e.g. 1 MΩ) is used as the failure criterion. See Figure 48 and Figure 49. Note that the wear-out mechanisms occurring in the MLCC capacitors are not reversible but cumulative over time.

Input Capacitor Lifetime vs Temperature and Voltage

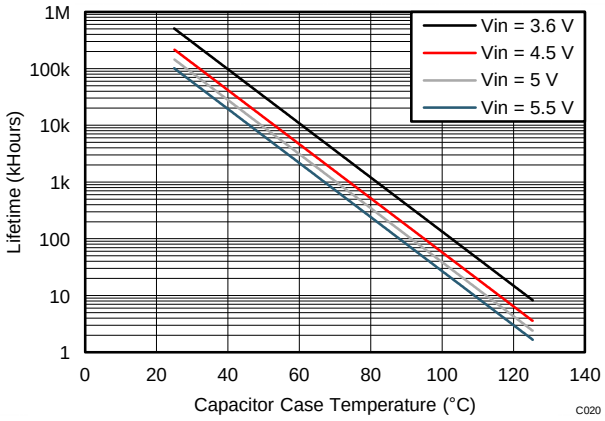

Figure 48. Input Capacitor Lifetime

Output Capacitor Lifetime vs Temperature and Voltage

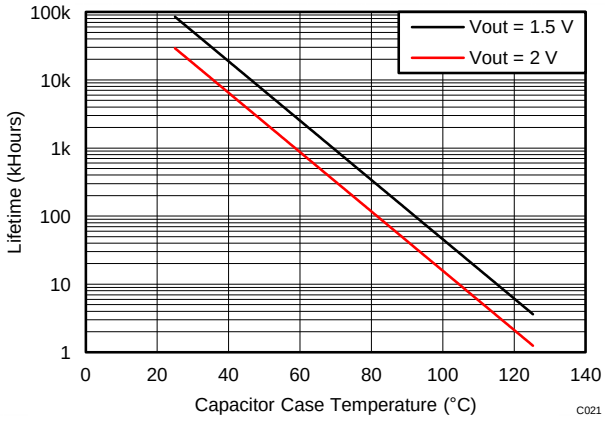

Figure 49. Output Capacitor Lifetime

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 References

"EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques", in *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 4, NO. 3, AUGUST 2005, pp 569-576* by Josep Balcells, Alfonso Santolaria, Antonio Orlandi, David González, Javier Gago.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS8268180	Click here	Click here	Click here	Click here	Click here
TPS8268150	Click here	Click here	Click here	Click here	Click here
TPS8268120	Click here	Click here	Click here	Click here	Click here
TPS8268105	Click here	Click here	Click here	Click here	Click here
TPS8268090	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

MicroSiP is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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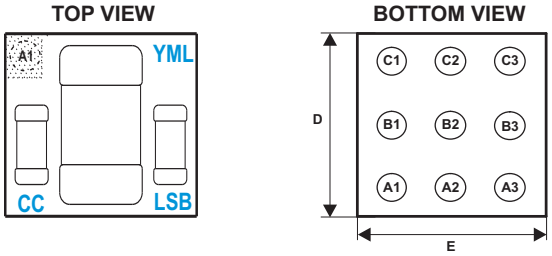
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Summary

SIP PACKAGE



Code:

- CC — Customer Code (device/voltage specific)
- YML — Y: Year, M: Month, L: Lot trace code
- LSB — L: Lot trace code, S: Site code, B: Board locator

13.2 MicroSiP™ DC/DC Module Package Dimensions

TheTPS8268x is available in an 9-bump ball grid array (BGA) package. The package dimensions are:

- D = 2.30 ±0.05 mm
- E = 2.90 ±0.05 mm

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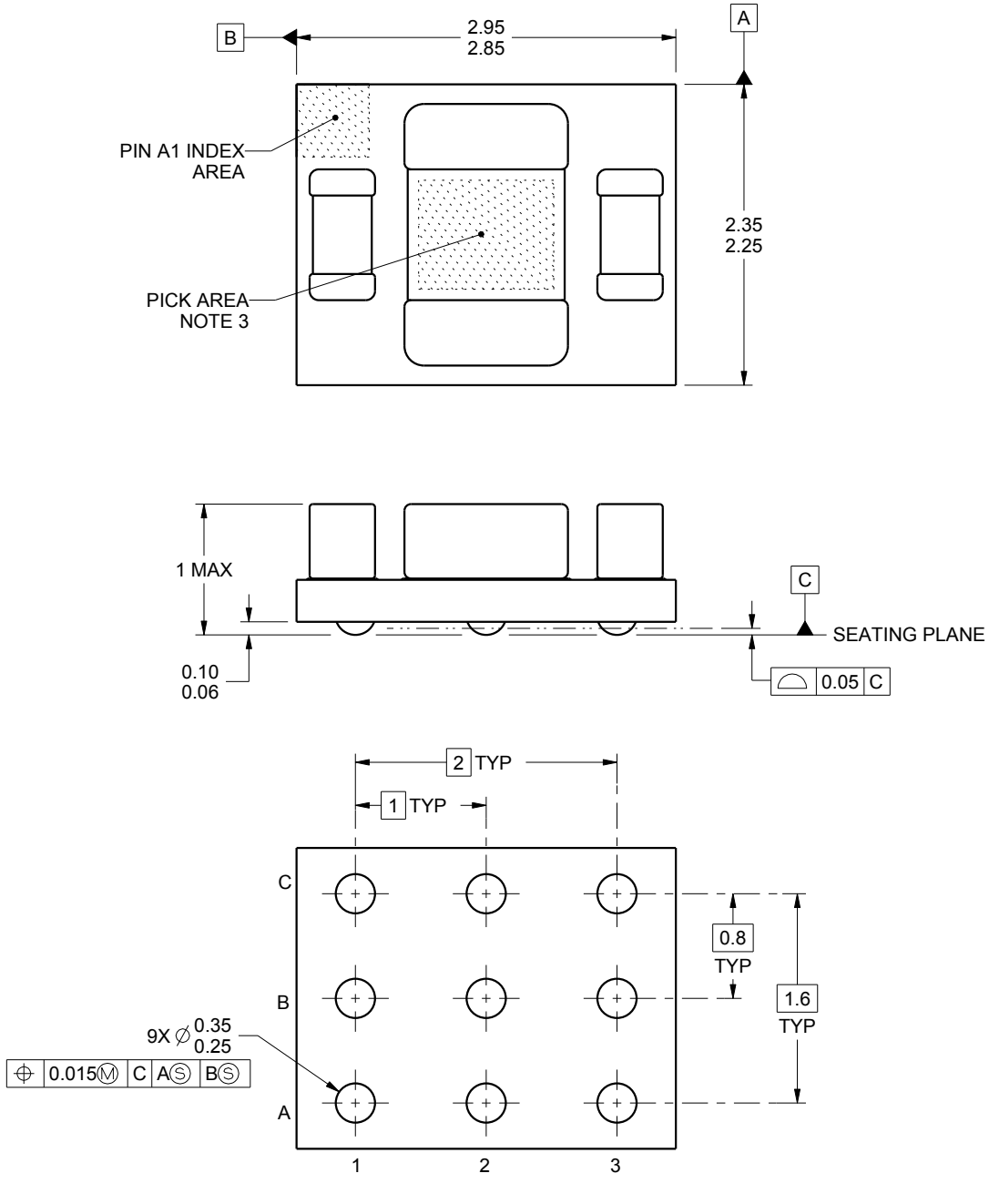
PACKAGE OUTLINE

SIP0009B

MicroSiP™- 1 mm max height

MICRO SYSTEM IN PACKAGE

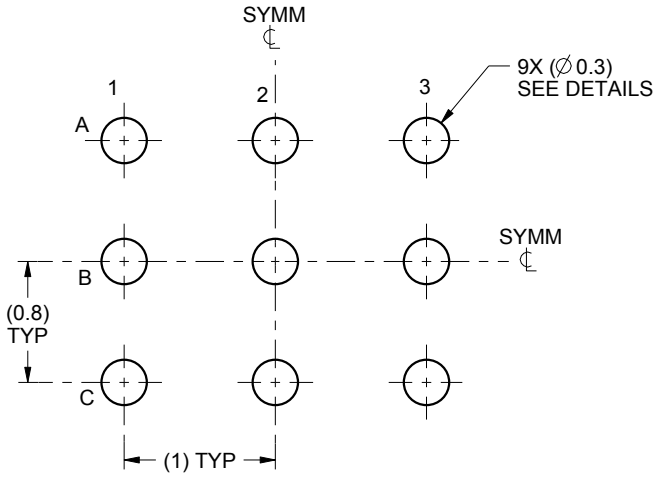


4218356/B 11/2014

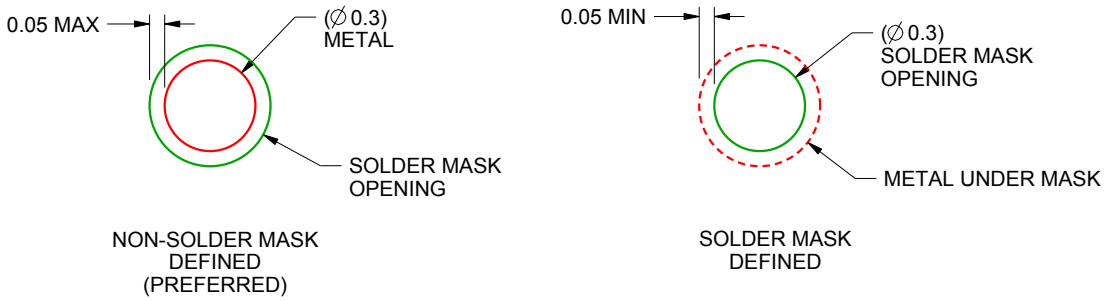
MicroSiP is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. For pick and place nozzle recommendation, see product datasheet.
4. Location, size and quantity of each component are for reference only and may vary.



LAND PATTERN EXAMPLE
SCALE:20X

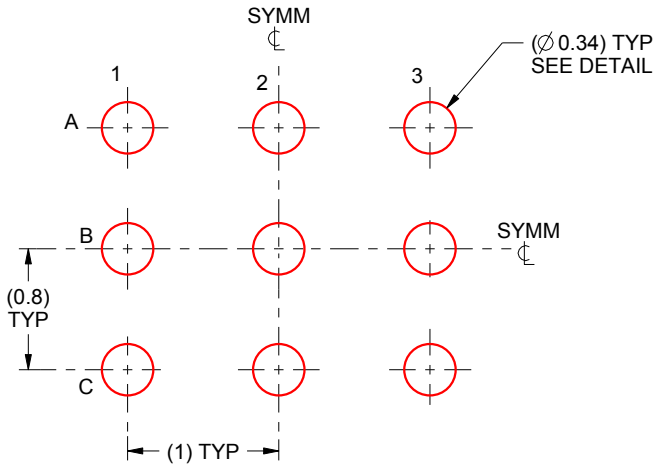


SOLDER MASK DETAILS
NOT TO SCALE

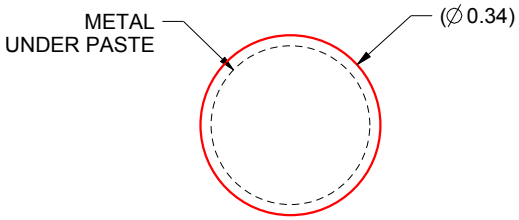
4218356/B 11/2014

NOTES: (continued)

5. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X



SOLDER PASTE DETAIL
TYPICAL

4218356/B 11/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS8268090SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268090SIPR.B	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268090SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268090SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268105SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268105SIPR.B	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268105SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268105SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268120SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HJ
TPS8268120SIPR.B	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HJ
TPS8268120SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HJ
TPS8268120SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HJ
TPS8268150SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR
TPS8268150SIPR.B	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR
TPS8268150SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR
TPS8268150SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR
TPS8268180SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HK
TPS8268180SIPR.B	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HK
TPS8268180SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HK
TPS8268180SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	HK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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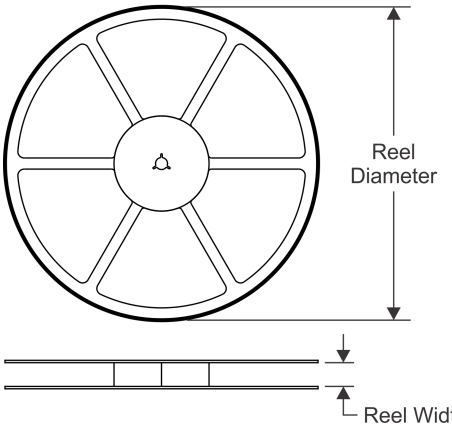
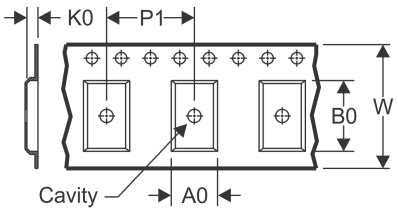
TAPE AND REEL INFORMATION

REEL DIMENSIONS

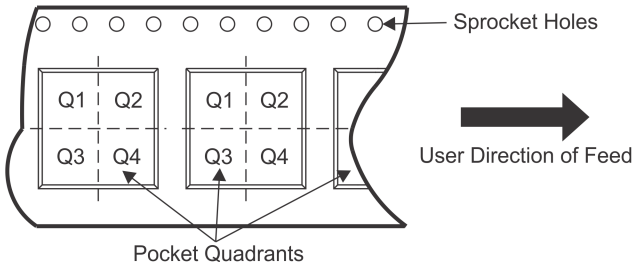


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

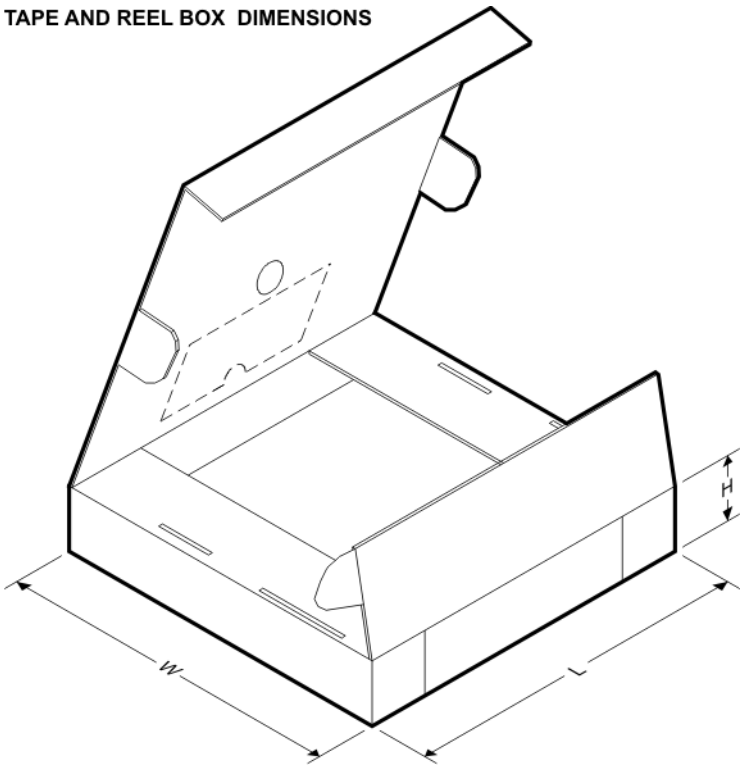
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS8268090SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268090SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268105SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268105SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268120SIPR	uSiP	SIP	9	3000	178.0	9.0	2.5	3.1	1.35	4.0	8.0	Q2
TPS8268120SIPT	uSiP	SIP	9	250	178.0	9.0	2.5	3.1	1.35	4.0	8.0	Q2
TPS8268150SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268150SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268180SIPR	uSiP	SIP	9	3000	178.0	9.0	2.5	3.1	1.35	4.0	8.0	Q2
TPS8268180SIPT	uSiP	SIP	9	250	178.0	9.0	2.5	3.1	1.35	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS8268090SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268090SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268105SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268105SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268120SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268120SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268150SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268150SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268180SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268180SIPT	uSiP	SIP	9	250	223.0	194.0	35.0

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