SBOS141C – JANUARY 1984 – REVISED SEPTEMBER 2009

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE-SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

APPLICATIONS

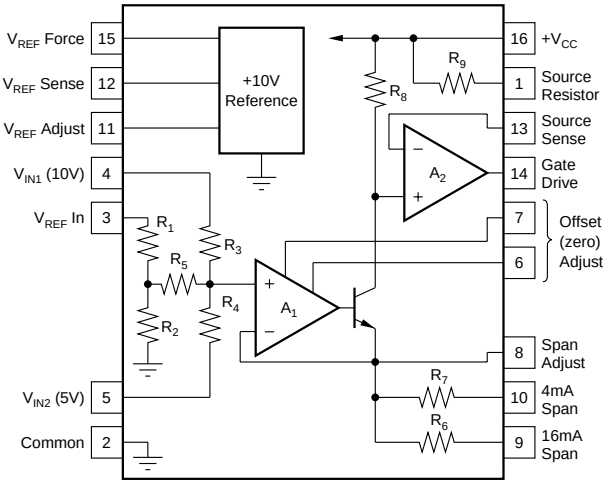
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4mA to 20mA, 0mA to 20mA, 5mA to 25mA, and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



ABSOLUTE MAXIMUM RATINGS(1)

Power Supply, $+V_{CC}$	40V
Input Voltage, V_{IN1}, V_{IN2}, $V_{REF\ IN}$	$+V_{CC}$
See text regarding safe negative input voltage range.	
Storage Temperature Range: A, B	–55°C to +125°C
K, U	–40°C to +85°C
Output Short-Circuit Duration, Gate Drive and V_{REF} Force	Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor	40mA

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

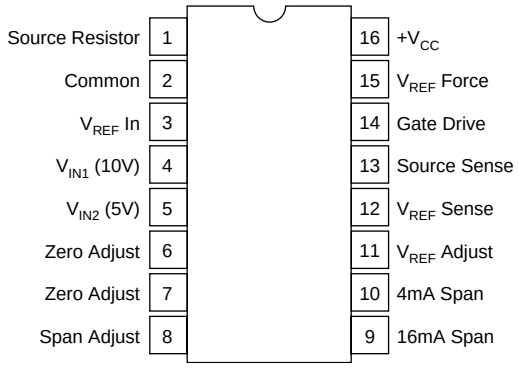
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE
XTR110AG	DIP-16 Ceramic	JD	–40°C to +85°C
XTR110BG	DIP-16 Ceramic	JD	–40°C to +85°C
XTR110KP	DIP-16 Plastic	N	0°C to +70°C
XTR110KU	SOL-16 Surface-Mount	DW	0°C to +70°C

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

TOP VIEW



ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω**, unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG, KP, KU			XTR110BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSMITTER								
Transfer Function			$I_O = 10\ [(V_{REF}In/16) + (V_{IN1}/4) + (V_{IN2}/2)]\ /R_{SPAN}$					
Input Range: V_{IN1}[5]	Specified Performance	0		+10	*		*	V
V_{IN2}	Specified Performance	0		+5	*		*	V
Current, I_O	Specified Performance[1]	4		20	*		*	mA
	Derated Performance[1]	0		40	*		*	mA
Nonlinearity	16mA/20mA Span[2]		0.01	0.025		0.002	0.005	% of Span
Offset Current, I_{OS}	I_O = 4mA[1]							
Initial	[1]		0.2	0.4		0.02	0.1	% of Span
vs Temperature	[1]		0.0003	0.005		*	0.003	% of Span/°C
vs Supply, V_{CC}	[1]		0.0005	0.005		*	*	% of Span/V
Span Error	I_O = 20mA							
Initial	[1]		0.3	0.6		0.05	0.2	% of Span
vs Temperature	[1]		0.0025	0.005		0.0009	0.003	% of Span/°C
vs Supply, V_{CC}	[1]		0.003	0.005		*	*	% of Span/V
Output Resistance	From Drain of FET (Q_{EXT})[3]		10×10^9			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} In		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of Span		15			*		µs
	To 0.01% of Span		20			*		µs
Slew Rate			1.3			*		mA/µs
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temperature			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line Regulation		0.0002	0.005		*	*	%/V
vs Output Current	Load Regulation		0.0005	0.01		*	*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range		–0.100		+0.25	*		*	V
Output Current	Specified Performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification: AG, BG		–40		+85	*		*	°C
KP, KU		0		+70				°C
Operating: AG, BG		–55		+125	*		*	°C
KP, KU		–25		+85				°C

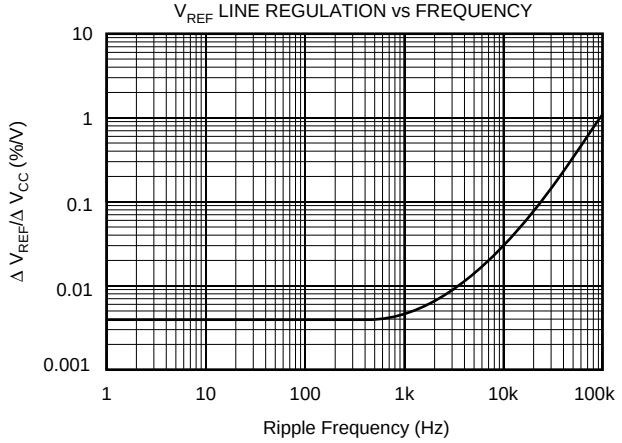
* Specifications same as AG/KP grades. ** Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by ($+V_{CC}$ – 2V) $+V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 3. (5) For extended I_{REF} drive circuit see Figure 4. (5) Unit may be damaged. See *Input Voltage Range* section.

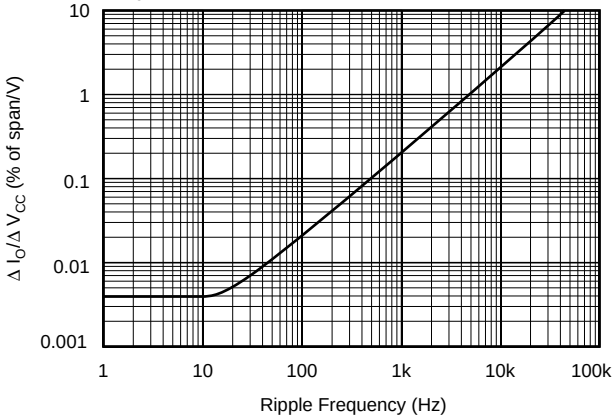
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω, unless otherwise noted.

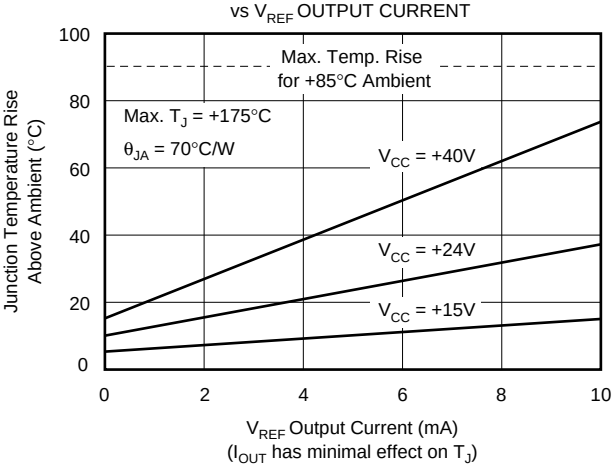
V_{REF} LINE REGULATION vs FREQUENCY



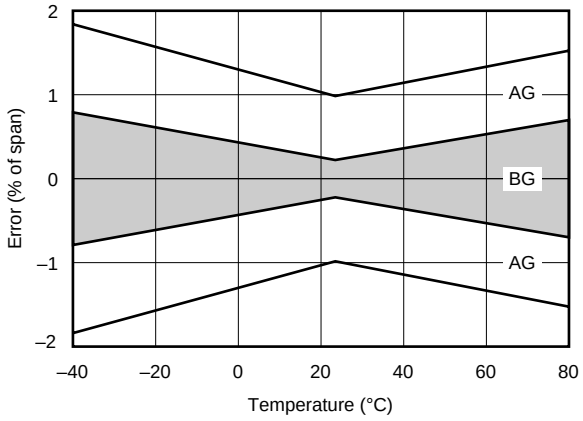
I_O POWER SUPPLY REGULATION vs FREQUENCY



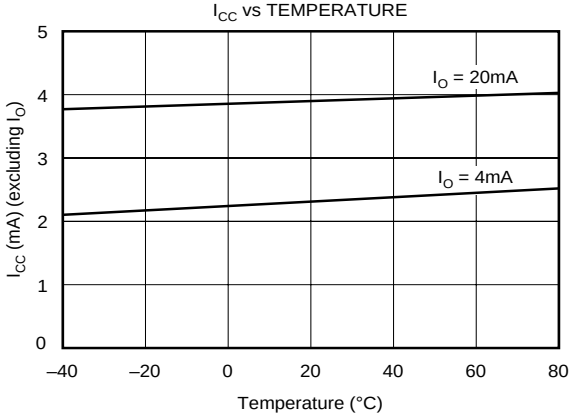
JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



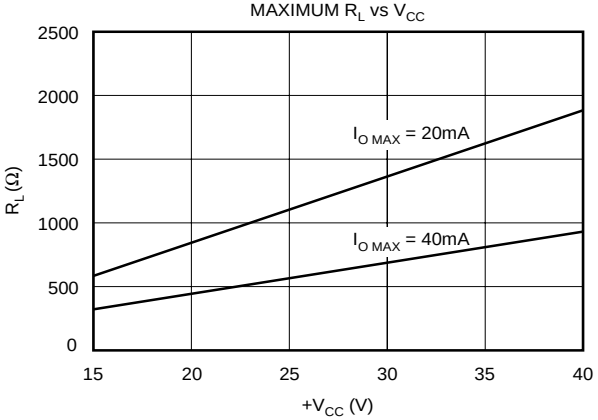
TOTAL OUTPUT ERROR vs TEMPERATURE



I_{CC} vs TEMPERATURE



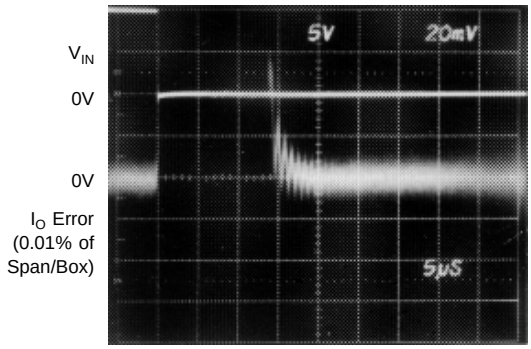
MAXIMUM R_L vs V_{CC}



TYPICAL PERFORMANCE CURVES (Continued)

At T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω, unless otherwise noted.

SETTLING TIME WITH NEG V_{IN} STEP



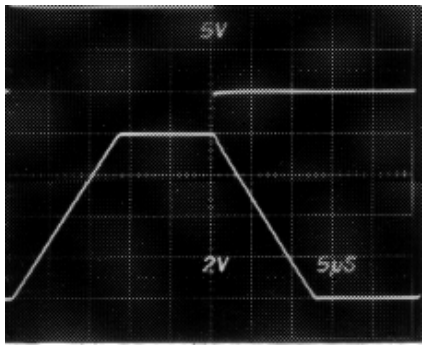
V_{IN}

0V

0V

I_O Error (0.01% of Span/Box)

PULSE RESPONSE



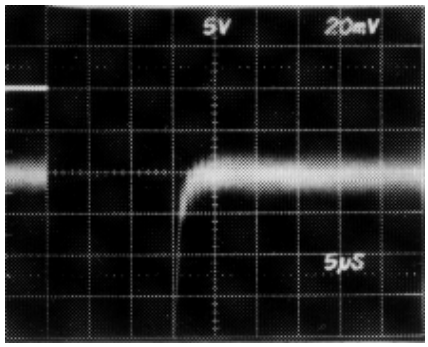
V_{IN}

0V

I_O into 500Ω

0V

SETTLING TIME WITH POS V_{IN} STEP



V_{IN}

0V

0V

I_O Error (0.01% of Span/Box)

APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0V to 10V input and 4ma to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_O = \frac{10\left[\frac{(V_{REF\ IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2}\right]}{R_{SPAN}} \qquad (1)$$

R_{SPAN} is the total impedance seen at the emitter of the internal NPN transistor. This impedance varies depending on how pins 8, 9 and 10 are configured. Typical operating region configurations are shown in Figure 1. An external R_{SPAN} can be connected for different output current ranges as described later.

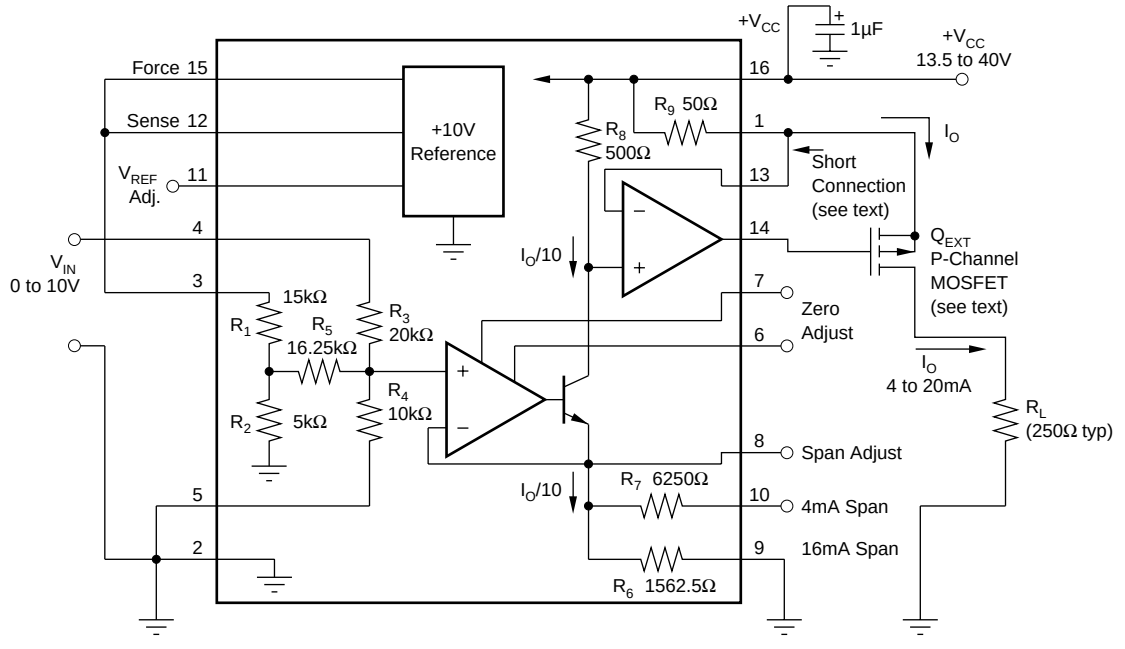
EXTERNAL TRANSISTOR

An external pass transistor, Q_{EXT}, is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

MANUFACTURER	PART NO.	BV_{DSS}(1)	BV_{GS}(1)	PACKAGE
Ferranti	ZVP1304A	40V	20V	TO-92
	ZVP1304B	40V	20V	TO-39
	ZVP1306A	60V	20V	TO-92
	ZVP1306B	60V	20V	TO-39
International Rectifier	IRF9513	60V	20V	TO-220
Motorola	MTP8P08	80V	20V	TO-220
RCA	RFL1P08	80V	20V	TO-39
	RFT2P08	80V	20V	TO-220
Siliconix (preferred)	VP0300B	30V	40V	TO-39
	VP0300L	30V	40V	TO-92
	VP0300M	30V	40V	TO-237
	VP0808B	80V	40V	TO-39
	VP0808L	80V	40V	TO-92
	VP0808M	80V	40V	TO-237
Supertex	VP1304N2	40V	20V	TO-220
	VP1304N3	40V	20V	TO-92
	VP1306N2	60V	20V	TO-220
	VP1306N3	60V	20V	TO-92

NOTE: (1) BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.



INPUT RANGE (V)	OUTPUT RANGE (mA)	PIN 3	PIN 4	PIN 5	PIN 9	PIN 10
0-10	0-20	Com	Input	Com	Com	Com
2-10	4-20	Com	Input	Com	Com	Com
0-10	4-20	+10V Ref	Input	Com	Com	Open
0-10	5-25	+10V Ref	Input	Com	Com	Com
0-5	0-20	Com	Com	Input	Com	Com
1-5	4-20	Com	Com	Input	Com	Com
0-5	4-20	+10V Ref	Com	Input	Com	Open
0-5	5-25	+10V Ref	Com	Input	Com	Com

FIGURE 1. Basic Circuit Connection.

If the supply voltage, $+V_{CC}$, exceeds the gate-to-source breakdown voltage of Q_{EXT}, and the output connection (drain of Q_{EXT}) is broken, Q_{EXT} could fail. If the gate-to-source breakdown voltage is lower than $+V_{CC}$, Q_{EXT} can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for Q_{EXT}—see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

TRANSISTOR DISSIPATION

Maximum power dissipation of Q_{EXT} depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by Q_{EXT} is:

$$P_{MAX} = (+V_{CC})\ I_{FS} \qquad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

PACKAGE TYPE	ALLOWABLE POWER DISSIPATION
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Use if hermetic package is required.

TABLE II. External Transistor Package Type and Dissipation.

INPUT VOLTAGE RANGE

The internal op amp A_1 can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of A_1 is:

$$V_{A1} = \frac{(V_{REF\ IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \qquad (3)$$

This voltage should not be allowed to go more negative than –0.5V. If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any point where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ($V_{REF\ SENSE}$). To preserve accuracy, any load including pin 3 should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

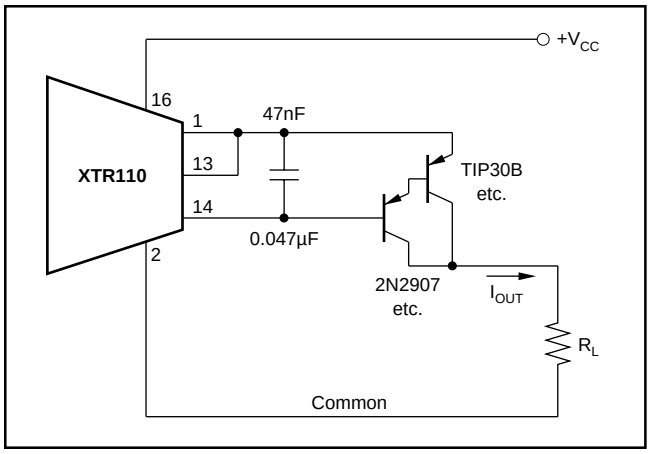


FIGURE 2. Q_{EXT} Using PNP Transistors.

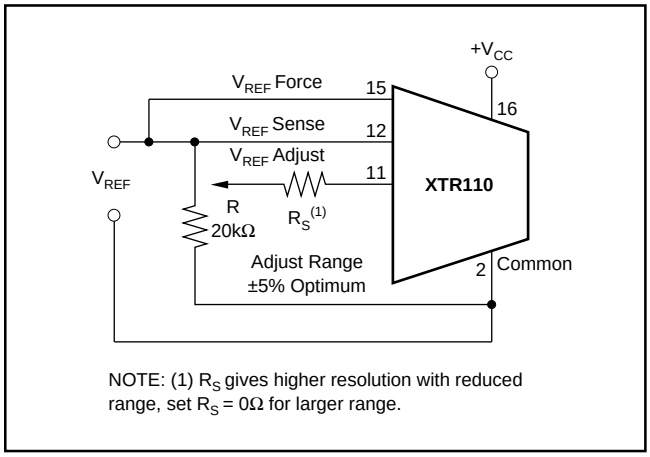


FIGURE 3. Optional Adjustment of Reference Voltage.

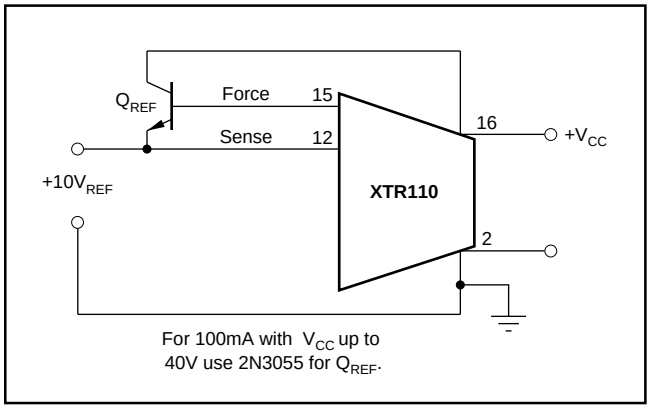


FIGURE 4. Increasing Reference Current Drive.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. Set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting

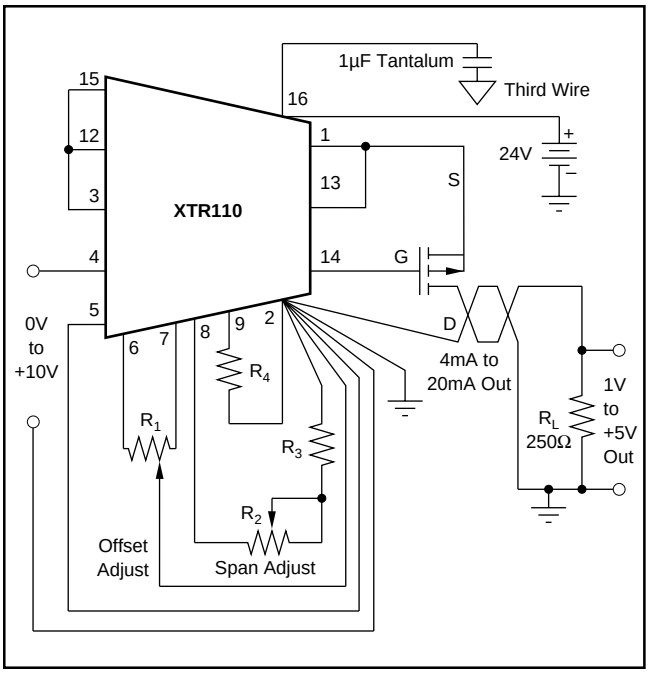


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

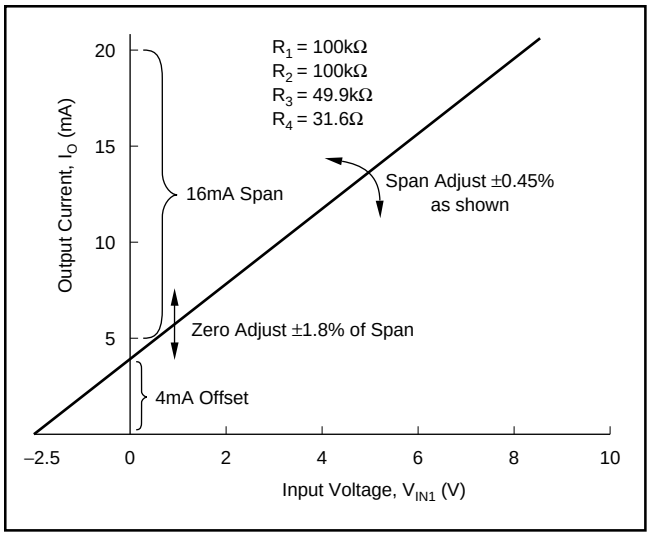


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

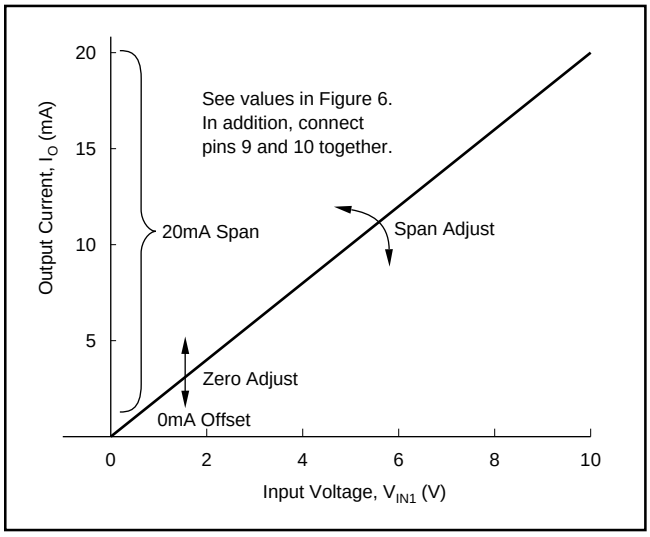


FIGURE 7. Zero and Span of 0V to +10V_{IN}, 0mA to 20mA Output Configuration (see Figure 5).

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9 \ (Span_{OLD}/Span_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.

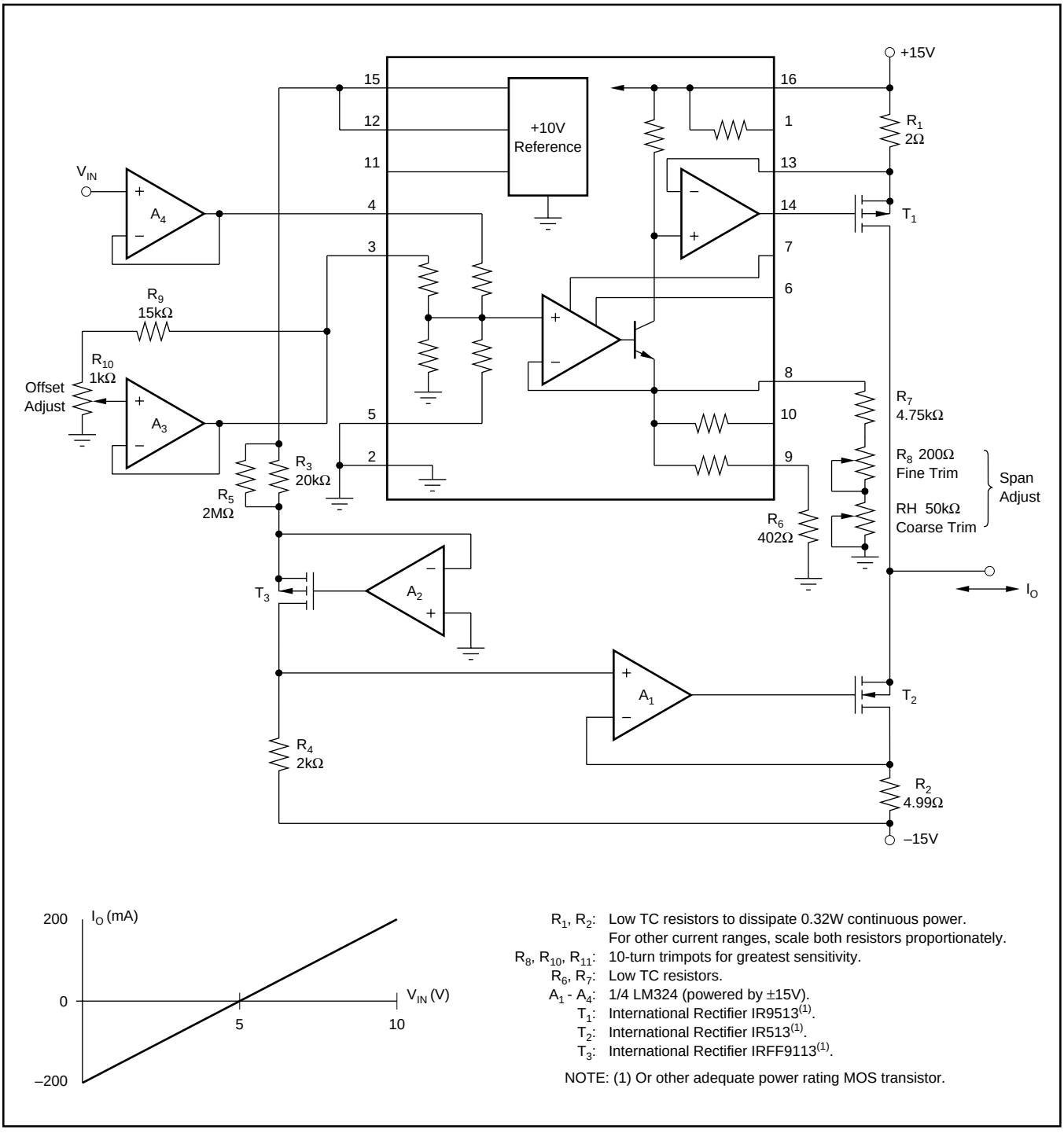


FIGURE 8. ±200mA Current Pump.

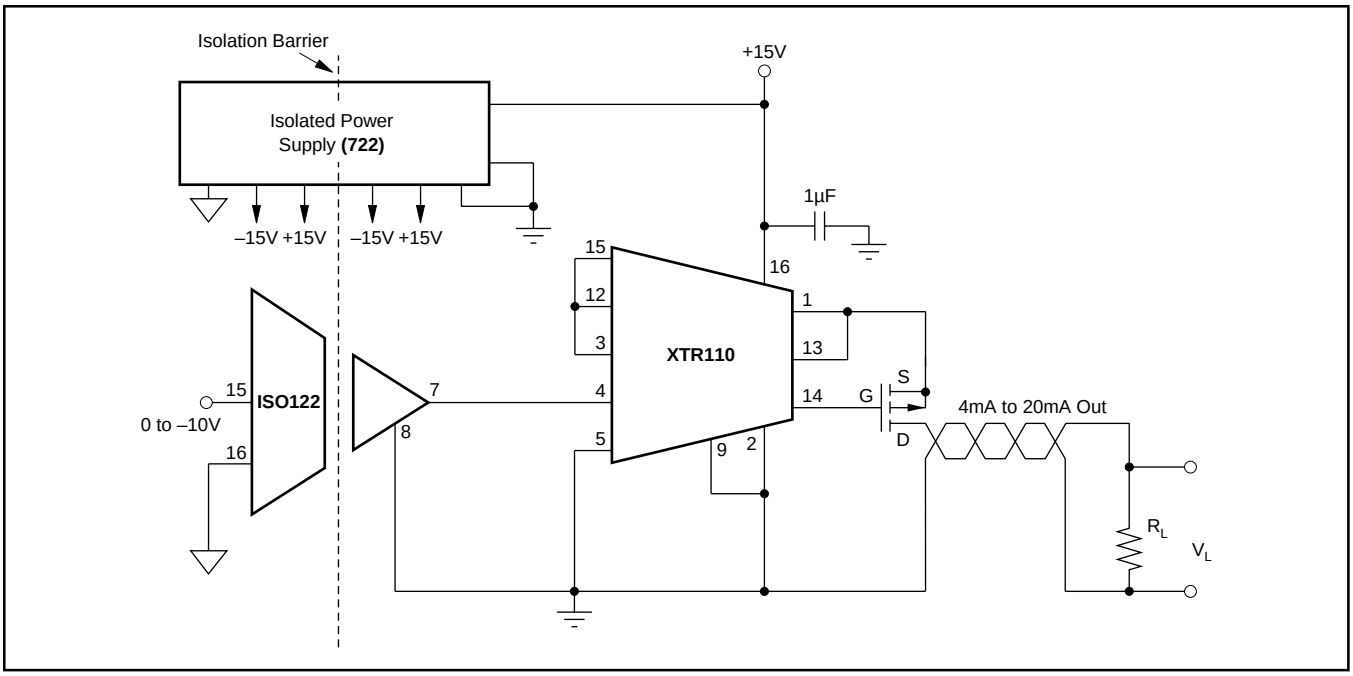


FIGURE 9. Isolated 4mA to 20mA Channel.

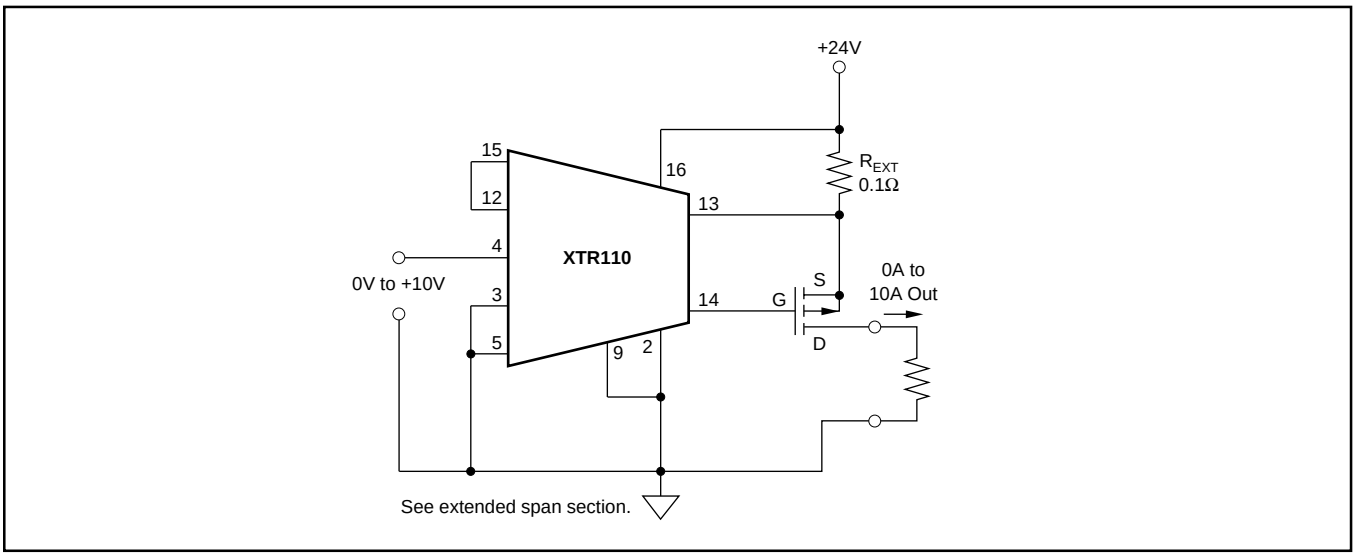


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
9/09	C	6	Front Page	Changed front page to standard format.
			Applications Information	Changed text in third paragraph.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTR110AG	Active	Production	CDIP SB (JD) | 16	24 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR110AG
XTR110AG.A	Active	Production	CDIP SB (JD) | 16	24 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR110AG
XTR110BG	Active	Production	CDIP SB (JD) | 16	24 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR110BG
XTR110BG.A	Active	Production	CDIP SB (JD) | 16	24 | TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 85	XTR110BG
XTR110KP	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	XTR110KP
XTR110KP.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	XTR110KP
XTR110KU	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR110KU
XTR110KU.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR110KU
XTR110KU/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR110KU
XTR110KU/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR110KU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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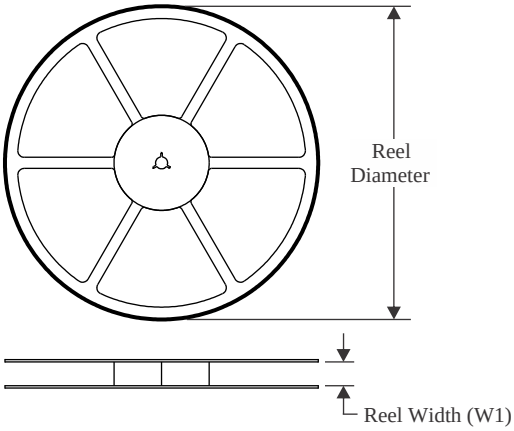
and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

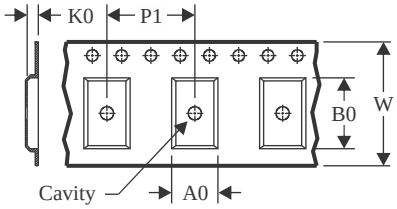
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

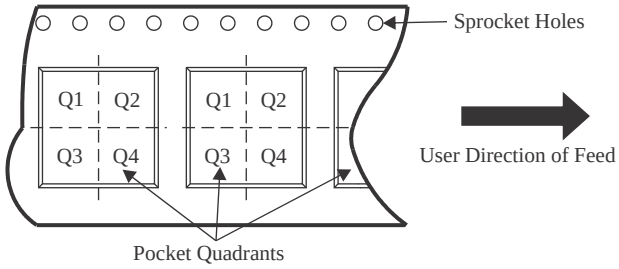


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

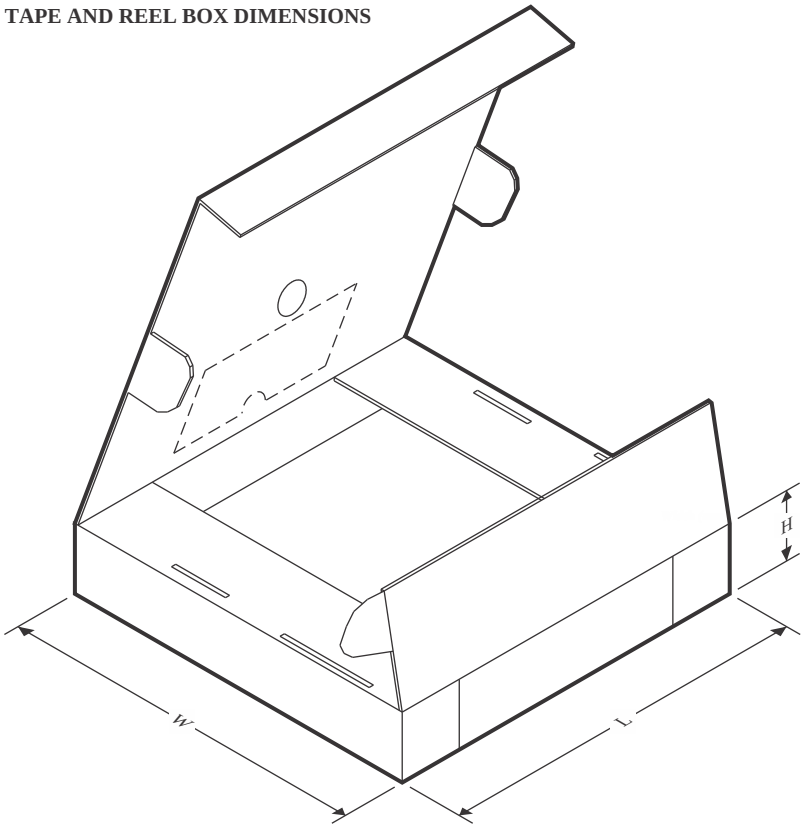
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR110KU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

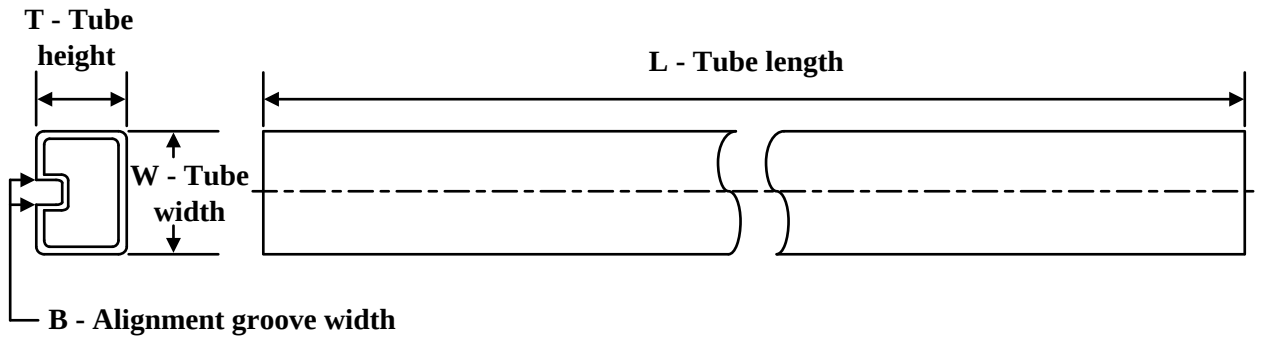
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR110KU/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE

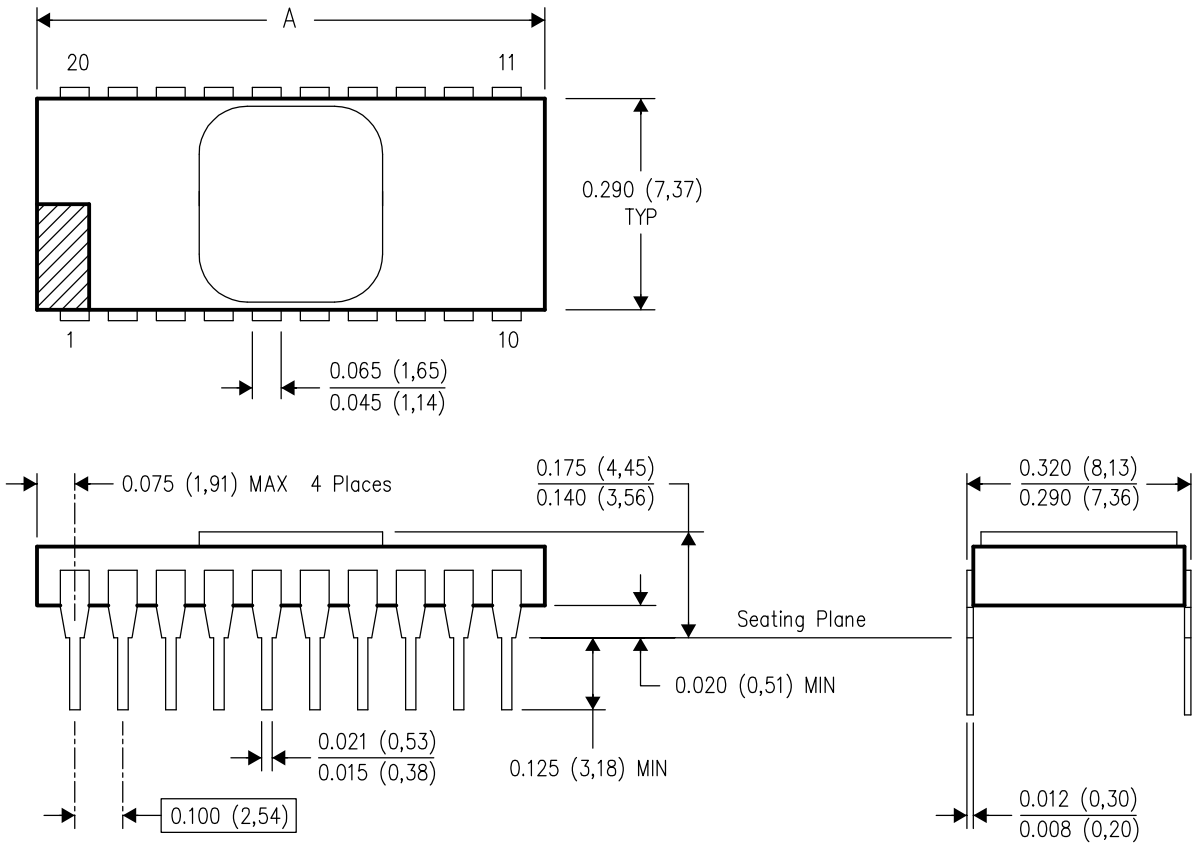


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
XTR110AG	JD	CDIP SB	16	24	506.98	15.24	12290	NA
XTR110AG.A	JD	CDIP SB	16	24	506.98	15.24	12290	NA
XTR110BG	JD	CDIP SB	16	24	506.98	15.24	12290	NA
XTR110BG.A	JD	CDIP SB	16	24	506.98	15.24	12290	NA
XTR110KP	N	PDIP	16	25	506	13.97	11230	4.32
XTR110KP.A	N	PDIP	16	25	506	13.97	11230	4.32
XTR110KU	DW	SOIC	16	40	507	12.83	5080	6.6
XTR110KU.A	DW	SOIC	16	40	507	12.83	5080	6.6

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

GENERIC PACKAGE VIEW

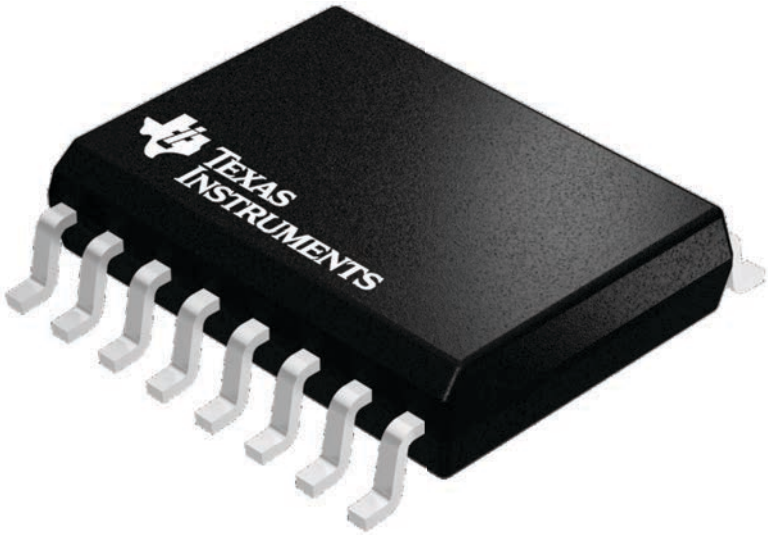
DW 16

SOIC - 2.65 mm max height

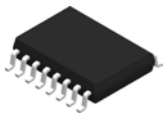
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

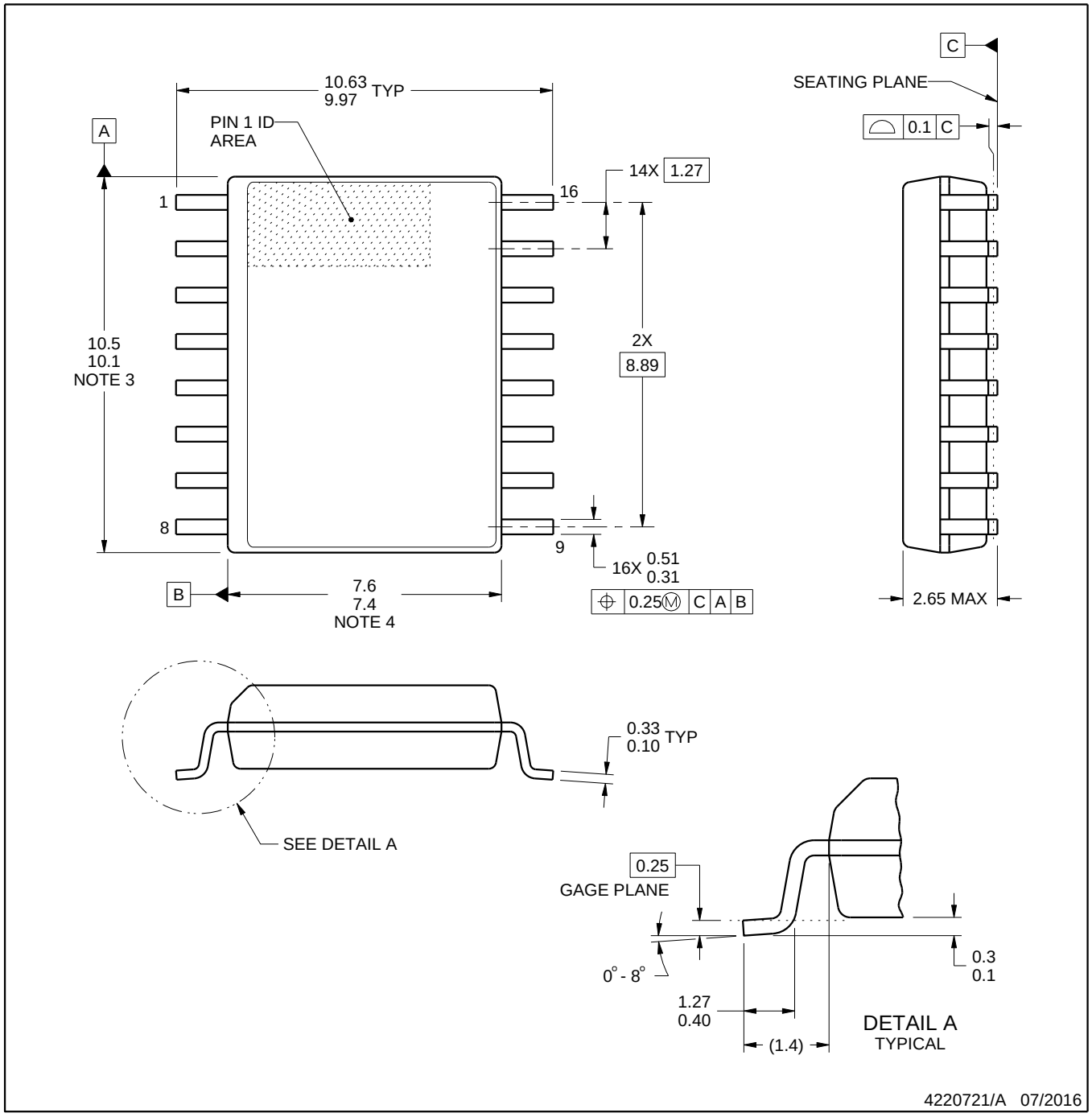


PACKAGE OUTLINE

DW0016A

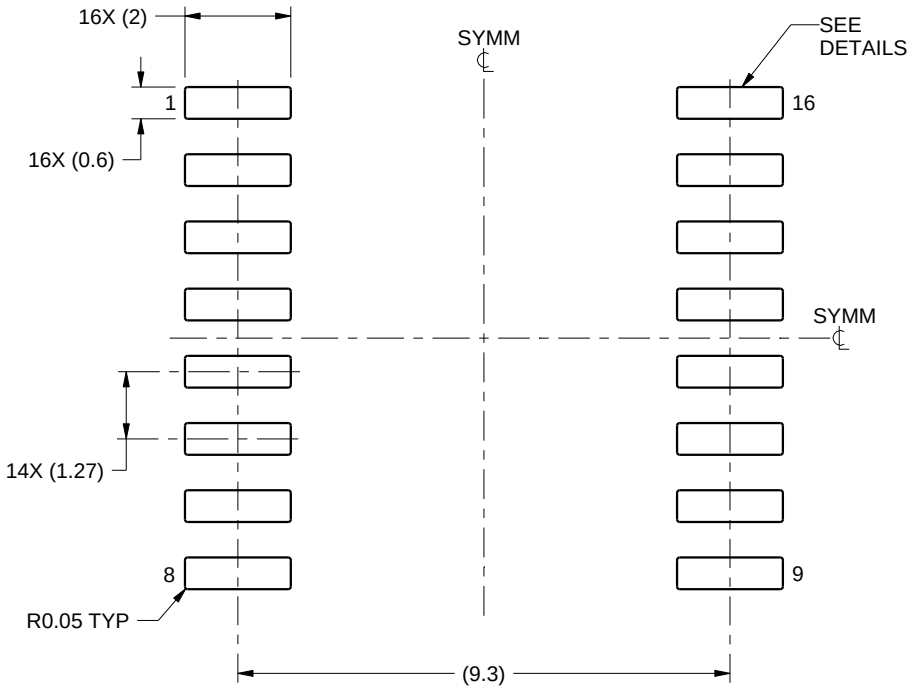
SOIC - 2.65 mm max height

SOIC

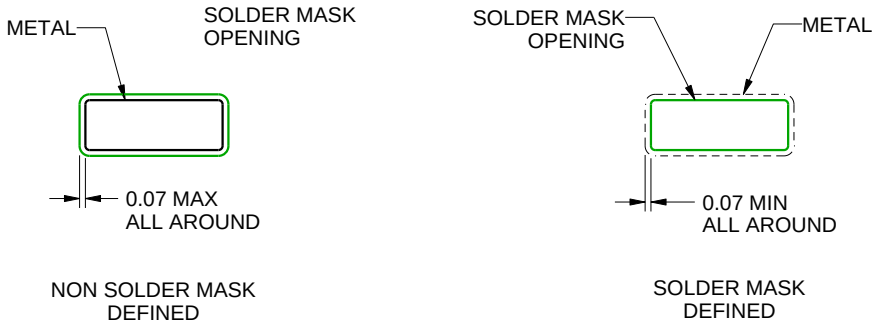


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

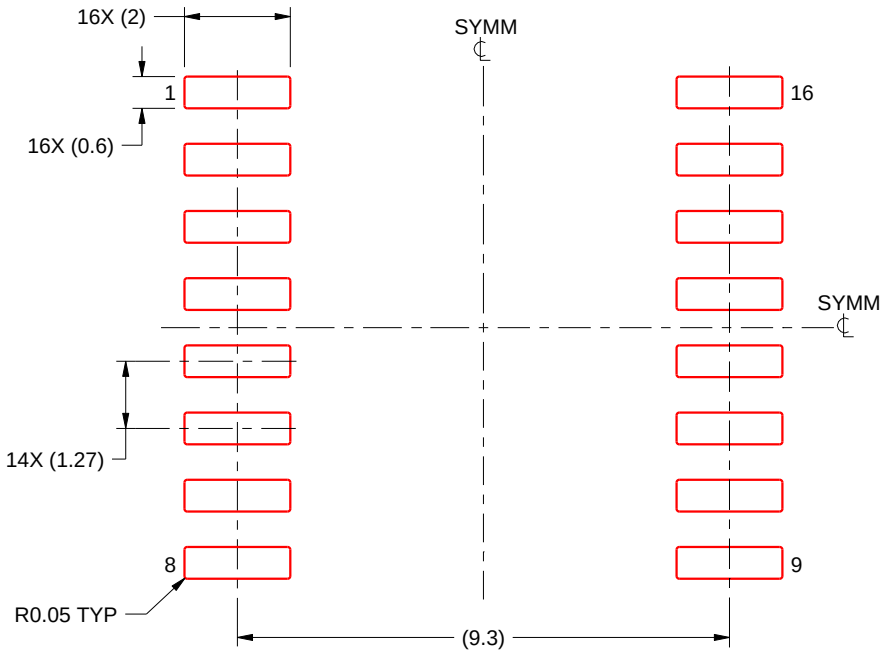


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

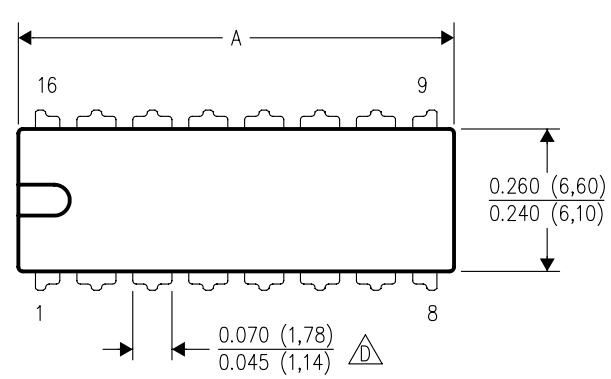
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

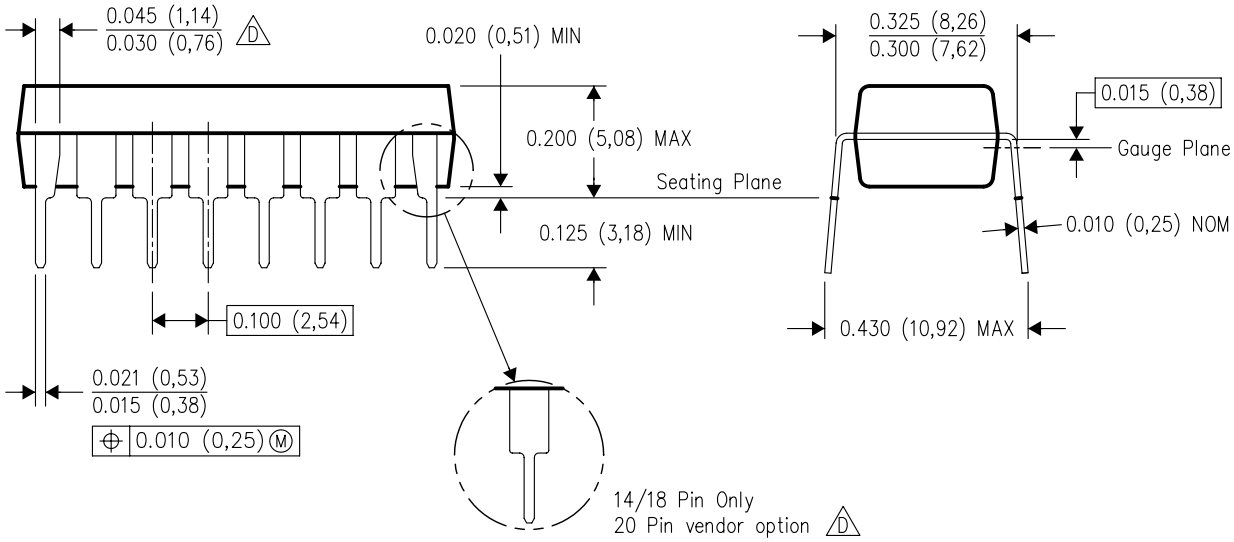
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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