



**Table of Contents**

<b>1 Overview</b> .....	<b>2</b>
<b>2 Failure Mode Distribution (FMD)</b> .....	<b>3</b>
<b>3 Functional Safety Failure In Time (FIT) Rates</b> .....	<b>4</b>
3.1 LMR33610 and LMR33620.....	4
3.2 LMR33630.....	5
3.3 LMR33640.....	6
<b>4 Pin Failure Mode Analysis (Pin FMA)</b> .....	<b>7</b>
4.1 LMR336x0 (VQFN Package).....	8
4.2 LMR336x0 (HSOIC Package).....	11
<b>5 Revision History</b> .....	<b>13</b>

**Trademarks**

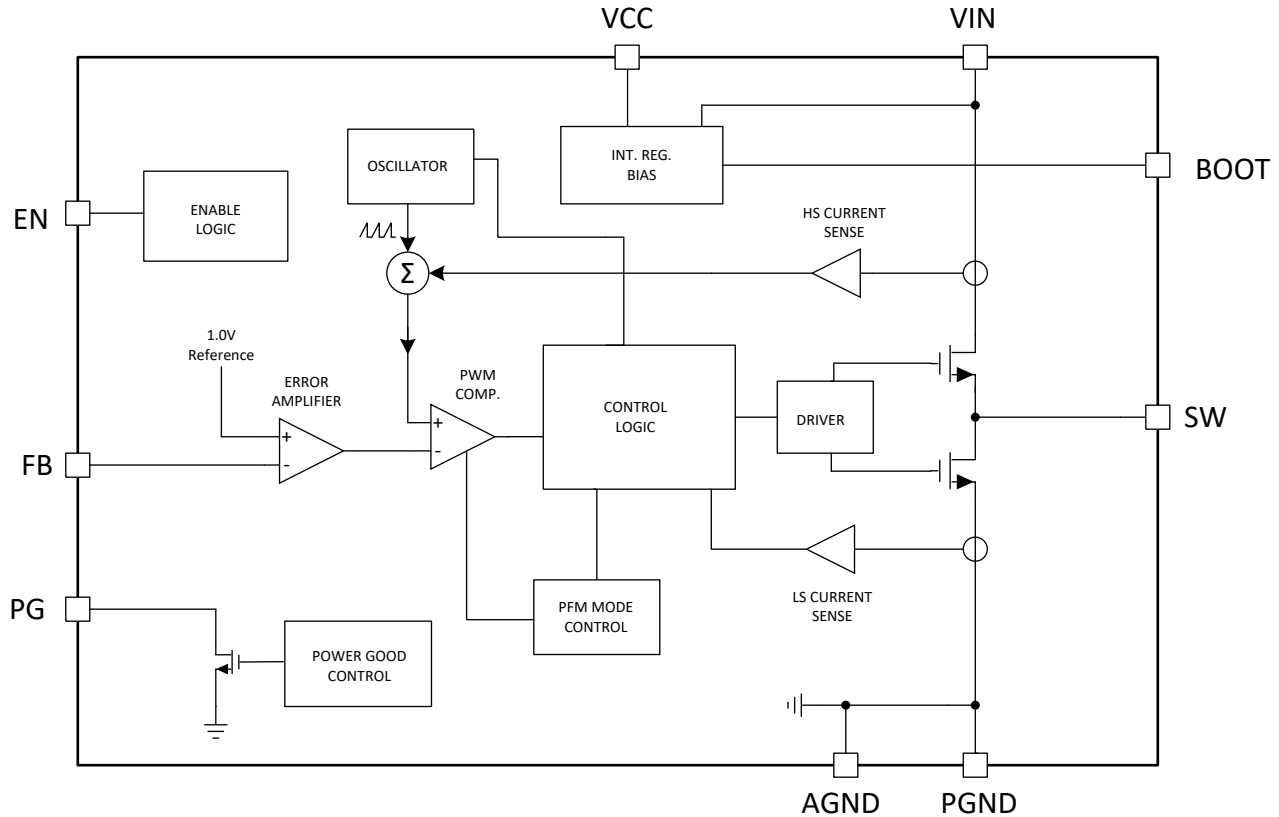
All trademarks are the property of their respective owners.

## 1 Overview

This document contains information for LMR336x0 in the VQFN-12 package (RNX designator) and HSOIC-8 package (DDA designator) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

LMR336x0 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR336x0 in [Table 2-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 2-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
SW Output	60%
SW output not in specification -- voltage or timing	25%
SW driver FET suck on	5%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in [Table 2-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

### 3 Functional Safety Failure In Time (FIT) Rates

#### 3.1 LMR33610 and LMR33620

This section provides Functional Safety Failure In Time (FIT) rates for the LMR33610 and LMR33620 are based on the following two different industry-wide used reliability standards:

- [Table 3-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 3-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	10
Die FIT Rate	5
Package FIT Rate	5

The failure rate and mission profile information in [Table 3-3](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 370 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

### 3.2 LMR33630

This section provides Functional Safety Failure In Time (FIT) rates for the LMR33630 based on the following industry-wide used reliability standards:

- [Table 3-2](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 3-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	13
Die FIT Rate	8
Package FIT Rate	5

The failure rate and mission profile information in [Table 3-2](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 555 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

### 3.3 LMR33640

This section provides Functional Safety Failure In Time (FIT) rates for the LMR33640 based on the following two different industry-wide used reliability standards:

- [Table 3-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 3-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 3-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	14
Die FIT Rate	6
Package FIT Rate	8

The failure rate and mission profile information in [Table 3-3](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 700 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 3-4. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 3-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR336x0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#) and [Table 4-6](#))
- Pin open-circuited (see [Table 4-3](#) and [Table 4-7](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#) and [Table 4-8](#))
- Pin short-circuited to VIN (see [Table 4-5](#) and [Table 4-9](#))

[Table 4-6](#) through [Table 4-9](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

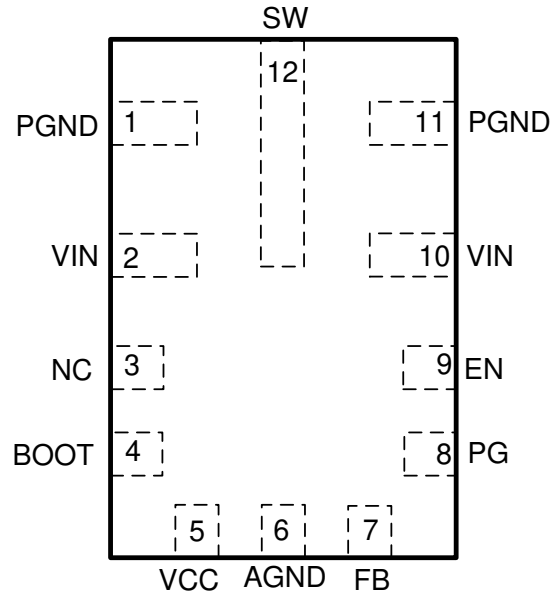
Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the '*Recommended Operating Conditions*' and the '*Absolute Maximum Ratings*' found in the appropriate device data sheet.
- Configuration as shown in the '*Example Application Circuit*' found in the appropriate device data sheet.

### 4.1 LMR336x0 (VQFN Package)

Figure 4-1 shows the LMR336x0 pin diagram for the VQFN-12 package (RNx designator). For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the appropriate device data sheet.



**Figure 4-1. Pin Diagram**



**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	No effect	D
VIN	2,10	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), damage to internal power FET(s) and/or other internal circuits.	A
BOOT	4	Damage to internal circuits	A
VCC	5	Fault mode will shut device off	B
AGND	6	No effect	D
FB	7	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
PG	8	Power good functionality will be lost.	B
EN	9	Loss of ENABLE functionality Device will remain in shut-down mode.	B
SW	12	Damage to internal power FET(s) and/or other internal circuits	A

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	With either one or both pins open, possible device damage.	A
VIN	2,10	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), the effect is the same as "open on pin 4"	B
BOOT	4	Loss of output voltage regulation; low or no output voltage.	B
VCC	5	VCC LDO will be unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
AGND	6	Loss of output voltage regulation. Possible damage to internal circuits.	A
FB	7	Loss of output voltage regulation. Output voltage may rise or fall outside of intended regulation window.	B
PG	8	PG functionality will be lost.	B
EN	9	Loss of ENABLE functionality. Erratic operation; probable loss of regulation.	B
SW	12	Loss of output voltage.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

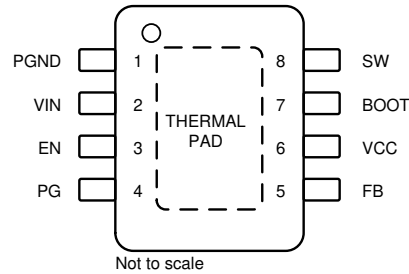
Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	VIN	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2	N/C	No effect if this pin is not used by customer.	D
			When used to route the SW node to connect CBOOT (as recommended), the output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
N/C	3	BOOT	No effect if this pin is not used by customer.	D
			When used to route the SW node to connect CBOOT (as recommended), damage to internal circuits. No output voltage will be produced.	A
BOOT	4	VCC	Loss of output regulation, possible damage to internal circuits	A
VCC	5	AGND	Fault mode will shut device off	B
AGND	6	FB	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
FB	7	PG	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load.	B
PG	8	EN	Erratic operation; probable loss of regulation.	B
EN	9	VIN	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain on.	B
VIN	10	PGND	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
PGND	11	SW	Damage to internal power FET(s) and/or other internal circuits	A

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2,10	No effect.	D
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), the output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
BOOT	4	Damage to internal circuits	A
VCC	5	Damage to internal circuits for VIN>5.5 V	A
AGND	6	Possible damage to internal circuits or package	A
FB	7	Damage to internal circuits will occur for VIN>5.5 V.	A
PG	8	Damage to internal circuits.	A
EN	9	No damage to device. Loss of ENABLE functionality.	B
SW	12	The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A

## 4.2 LMR336x0 (HSOIC Package)

Figure 4-2 shows the LMR336x0 pin diagram for the HSOIC-8 package (DDA designator). For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the appropriate device data sheet.



**Figure 4-2. Pin Diagram**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	No effect	D
VIN	2	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
N/C	3	Loss of ENABLE functionality Device will remain in shut-down mode.	B
BOOT	4	Power good functionality will be lost.	B
VCC	5	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
AGND	6	No effect	D
FB	7	Damage to internal circuits	A
PG	8	Damage to internal power FET(s) and/or other internal circuits	A

**Table 4-7. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Possible device damage.	A
VIN	2	Loss of output voltage.	B
EN	3	Loss of ENABLE functionality. Erratic operation; probable loss of regulation.	B
PG	4	PG functionality will be lost.	B
FB	5	Loss of output voltage regulation. Output voltage may rise or fall outside of intended regulation window.	B
VCC	6	VCC LDO will be unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
BOOT	7	Loss of output voltage regulation; low or no output voltage.	B
SW	8	Loss of output voltage.	B

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	VIN	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2	EN	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain on.	B
EN	3	PG	Erratic operation; probable loss of regulation.	B
FB	5	VCC	Output voltage will drop to near zero volts.	B
VCC	6	BOOT	Loss of output regulation, possible damage to internal circuits	A
BOOT	7	SW	Damage to internal circuits. No output voltage will be produced.	A

**Table 4-9. Pin FMA for Device Pins Short-Circuited to VIN**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2	No effect.	D
EN	3	No damage to device. Loss of ENABLE functionality.	B
PG	4	Damage to internal circuits.	A
FB	5	Damage to internal circuits will occur for VIN>5.5 V.	A
VCC	6	Damage to internal circuits for VIN>5.5 V	A
BOOT	7	Damage to internal circuits	A
SW	8	The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (March 2021)	Page
• Updated AGND in <a href="#">Table 4-6</a> .....	11

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated