DLP4710 0.47 1080p DMD

1 特長

- 対角 0.47 インチ (11.93mm) のマイクロミラー・アレイ
  - マイクロメートル・サイズのアルミ製ミラーを直交に配置した 1920 × 1080 アレイ
  - マイクロミラー・ピッチ:5.4µm
  - マイクロミラー傾斜角 (平面に対して):±17°
  - 底面照明による最良の効率と光学エンジン・サイズ
  - 偏波無依存のアルミニウム製マイクロミラー表面
- 32 ビット SubLVDS 入力データ・バス
- 専用 DLP3439 ディスプレイ・コントローラ
- 専用の DLPA3000 または DLPA3005 PMIC/LED ドライバによる信頼性の高い動作

2 アプリケーション

- スマート・フル HD プロジェクタ
- モバイル・アクセサリのフル HD プロジェクタ
- スクリーンレス・ディスプレイ
- 対話式ディスプレイ
- 低レイテンシのゲーム用ディスプレイ
- ヘッド・マウント・ディスプレイ

3 概要

DLP4710 デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御の MOEMS (micro-opto-electromechanical system) 空間光変調器 (SLM) です。適切な光学システムと結合することで、DLP4710LC DMD は非常に鮮明で高品質の画像や映像を表示できます。このデバイスは、DLP4710 DMD、DLPC3479 コントローラおよび DLPA3000/DLPA3005 PMIC/LED ドライバで構成されるチップセットの部品です。DLP4710LC は物理的なサイズが小さく、コントローラや PMIC/LED ドライバと組み合わせることにより、小さな外形と低消費電力で高解像度の HD 表示を可能にする、完全なシステム・ソリューションを実現します。

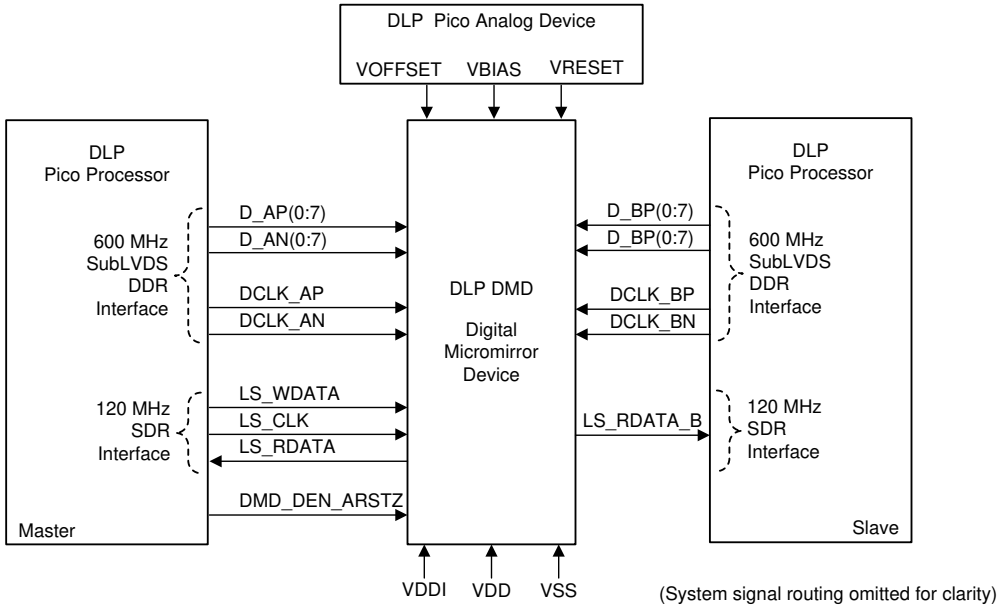
DLP4710 を使用して設計を開始する方法については、「TI DLP®Pico™ ディスプレイ・テクノロジーを使用した設計の開始」ページを参照してください。

DLP4710 のエコシステムには、設計期間の短縮に役立つ定評あるリソースが用意されており、これにはすぐに量産可能な光モジュール、光モジュール・メーカー、デザインハウスなどが含まれます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DLP4710	FQL (100)	24.50mm × 11mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



0.47 1080p チップセット

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

Changes from Revision A (November 2021) to Revision B (May 2022) — **Page**

- Updated Absolute Maximum Ratings disclosure to the latest TI standard ... 8
- Updated *Micromirror Array Optical Characteristics* ... 20
- Added *Third-Party Products Disclaimer* ... 37

Changes from Revision * (November 2018) to Revision A (November 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated $|T_{DELTA}|$ MAX from 30°C to 15°C ... 9

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5 Pin Configuration and Functions

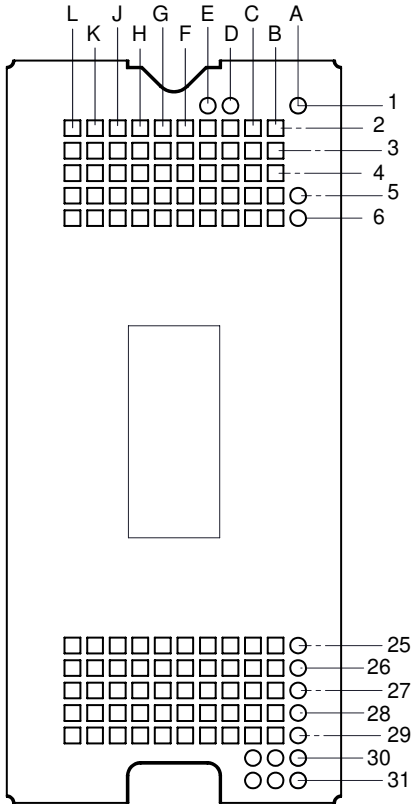


図 5-1. FQL Package. 100-Pin LGA. Bottom View.

表 5-1. Connector Pins

PIN[1]		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
DATA INPUTS						
D_AN(0)	G3	I	SubLVDS	Double	Data, Negative	5.01
D_AN(1)	F4	I	SubLVDS	Double	Data, Negative	2.03
D_AN(2)	E3	I	SubLVDS	Double	Data, Negative	2.41
D_AN(3)	E6	I	SubLVDS	Double	Data, Negative	4.71
D_AN(4)	J5	I	SubLVDS	Double	Data, Negative	3.23
D_AN(5)	L5	I	SubLVDS	Double	Data, Negative	3.87
D_AN(6)	G5	I	SubLVDS	Double	Data, Negative	6.32
D_AN(7)	L3	I	SubLVDS	Double	Data, Negative	1.84
D_AP(0)	H3	I	SubLVDS	Double	Data, Positive	5.01
D_AP(1)	G4	I	SubLVDS	Double	Data, Positive	2.03
D_AP(2)	E4	I	SubLVDS	Double	Data, Positive	2.41
D_AP(3)	E5	I	SubLVDS	Double	Data, Positive	4.71
D_AP(4)	J6	I	SubLVDS	Double	Data, Positive	3.23
D_AP(5)	L6	I	SubLVDS	Double	Data, Positive	3.87
D_AP(6)	G6	I	SubLVDS	Double	Data, Positive	6.32
D_AP(7)	L4	I	SubLVDS	Double	Data, Positive	1.84
D_BN(0)	G27	I	SubLVDS	Double	Data, Negative	2.51
D_BN(1)	E26	I	SubLVDS	Double	Data, Negative	4.43

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表 5-1. Connector Pins (continued)

PIN[1]		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
D_BN(2)	D28	I	SubLVDS	Double	Data, Negative	2.76
D_BN(3)	D26	I	SubLVDS	Double	Data, Negative	5.47
D_BN(4)	L25	I	SubLVDS	Double	Data, Negative	4.85
D_BN(5)	K25	I	SubLVDS	Double	Data, Negative	4.10
D_BN(6)	L28	I	SubLVDS	Double	Data, Negative	2.53
D_BN(7)	K27	I	SubLVDS	Double	Data, Negative	2.76
D_BP(0)	F27	I	SubLVDS	Double	Data, Positive	2.51
D_BP(1)	E27	I	SubLVDS	Double	Data, Positive	4.43
D_BP(2)	D27	I	SubLVDS	Double	Data, Positive	2.76
D_BP(3)	D25	I	SubLVDS	Double	Data, Positive	5.47
D_BP(4)	L26	I	SubLVDS	Double	Data, Positive	4.85
D_BP(5)	J25	I	SubLVDS	Double	Data, Positive	4.10
D_BP(6)	K28	I	SubLVDS	Double	Data, Positive	2.53
D_BP(7)	J27	I	SubLVDS	Double	Data, Positive	2.76
DCLK_AN	J3	I	SubLVDS	Double	Clock, Negative	3.77
DCLK_AP	K3	I	SubLVDS	Double	Clock, Positive	3.77
DCLK_BN	H26	I	SubLVDS	Double	Clock, Negative	2.98
DCLK_BP	H27	I	SubLVDS	Double	Clock, Positive	2.98
CONTROL INPUTS						
LS_WDATA	D3	I	LPSDR [1]	Single	Write data for low speed interface.	1.20
LS_CLK	C3	I	LPSDR	Single	Clock for low-speed interface	1.20
DMD_DEN_ARSTZ	B6	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	4.19
LS_RDATA_A	C6	O	LPSDR	Single	Read data for low-speed interface	3.93
LS_RDATA_B	C4	O	LPSDR	Single	Read data for low-speed interface	2.57
POWER [3]						
VBIAS	B27	Power			Supply voltage for positive bias level at micromirrors	24.51
VBIAS	B4	Power				24.51
VOFFSET	B2	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	49.56
VOFFSET	C29	Power				49.56
VRESET	B28	Power			Supply voltage for negative reset level at micromirrors.	24.82
VRESET	B3	Power				24.82

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表 5-1. Connector Pins (continued)

PIN[1]		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
VDD	C2	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
VDD	D2	Power				
VDD	D29	Power				
VDD	E2	Power				
VDD	E29	Power				
VDD	H2	Power				
VDD	H28	Power				
VDD	H29	Power				
VDD	J2	Power				
VDD	J28	Power				
VDD	J29	Power				
VDD	K2	Power				
VDD	K29	Power				
VDD	L2	Power				
VDD	L29	Power				
VDDI	E28	Power			Supply voltage for SubLVDS receivers.	
VDDI	F2	Power				
VDDI	F28	Power				
VDDI	F29	Power				
VDDI	F3	Power				
VDDI	G2	Power				
VDDI	G28	Power				
VDDI	G29	Power				

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表 5-1. Connector Pins (continued)

PIN(1)		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
VSS	B25	Ground			Common return. Ground for all power.	
VSS	B26	Ground				
VSS	B29	Ground				
VSS	B5	Ground				
VSS	C25	Ground				
VSS	C26	Ground				
VSS	C27	Ground				
VSS	C28	Ground				
VSS	C5	Ground				
VSS	D4	Ground				
VSS	D5	Ground				
VSS	D6	Ground				
VSS	E25	Ground				
VSS	F25	Ground				
VSS	F26	Ground				
VSS	F5	Ground				
VSS	F6	Ground				
VSS	G25	Ground				
VSS	G26	Ground				
VSS	H25	Ground				
VSS	H4	Ground				
VSS	H5	Ground				
VSS	H6	Ground				
VSS	J26	Ground				
VSS	J4	Ground				
VSS	K26	Ground				
VSS	K4	Ground				
VSS	K5	Ground				
VSS	K6	Ground				
VSS	L27	Ground				

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQL ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.
(3) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.

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表 5-2. Test Pads

NUMBER	SYSTEM BOARD
A1	Do not connect
A5	Do not connect
A6	Do not connect
A25	Do not connect
A26	Do not connect
A27	Do not connect
A28	Do not connect
A29	Do not connect
A30	Do not connect
A31	Do not connect
B30	Do not connect
B31	Do not connect
C30	Do not connect
C31	Do not connect
D1	Do not connect
E1	Do not connect

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic(2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers(2)	–0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode(2) (3)	–0.5	11	V
	VBIAS	Supply voltage for micromirror electrode(2)	–0.5	19	V
	VRESET	Supply voltage for micromirror electrode(2)	–15	0.5	V
	| VDDI–VDD |	Supply voltage delta (absolute value)(4)		0.3	V
	| VBIAS–VOFFSET |	Supply voltage delta (absolute value)(5)		11	V
	| VBIAS–VRESET |	Supply voltage delta (absolute value)(6)		34	V
Input voltage	Input voltage for other inputs LPSDR(2)		–0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS(2) (7)		–0.5	VDDI + 0.5	V
Input pins	| VID |	SubLVDS input differential voltage (absolute value)(7)		810	mV
	IID	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational (8)	–20	90	°C
		Temperature – non-operational(8)	–40	90	°C
	T_{DP}	Dew Point Temperature - operating and non-operating (non-condensing)		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(9)		30	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated by the *セクション 7.6*) or of any point along the Window Edge as defined in 図 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operational in a system

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		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing)(1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(4)					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.7	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.7	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(5)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\lvert V_{DDI}–V_{DD}\rvert$	Supply voltage delta (absolute value)(6)			0.3	V
$\lvert V_{BIAS}–V_{OFFSET}\rvert$	Supply voltage delta (absolute value)(7)			10.5	V
$\lvert V_{BIAS}–V_{RESET}\rvert$	Supply voltage delta (absolute value)(8)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(9)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(10)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(10)					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) 図 6-8, 図 6-9	150	250	350	mV
V_{CM}	Common mode voltage 図 6-8, 図 6-9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage 図 6-8, 図 6-9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance 図 6-10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(11) (12) (13) (14)	0		40 to 70(13)	°C
	Array Temperature - short-term operational, 25 hr max(12) (15)	–20		-10	
	Array Temperature - short-term operational, 500 hr max(12) (15)	–10		0	
	Array Temperature – short-term operational, 500 hr max(12) (15)	70		75	
$\lvert T_{DELTA}\rvert$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (16)			15	°C
T_{WINDOW}	Window Temperature – operational(11) (17)			90	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(18)			24	°C

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		MIN	NOM	MAX	UNIT
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	Months
ILL_{UV}	Illumination wavelengths < 420 nm (11)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 420 nm and 700 nm		Thermally limited		
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(20)			55	degrees

(1) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(2) *セクション 6.4* are applicable after the DMD is installed in the final product.
(3) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *セクション 6.4*. No level of performance is implied when operating the device above or below the *セクション 6.4* limits.
(4) All voltage values are with respect to the ground pins (VSS).
(5) VOFFSET supply transients must fall within specified max voltages.
(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(10) Refer to the SubLVDS timing requirements in *セクション 6.7*.
(11) Simultaneous exposure of the DMD to the maximum *セクション 6.4* for temperature and UV illumination will reduce device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-1 and the Package Thermal Resistance using *セクション 7.6*.
(13) Per 図 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *セクション 7.7* for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the usable life of the device
(15) Short-term is the total cumulative time over the useful life of the device.
(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(17) Window temperature is the highest temperature on the window edge shown in 図 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(20) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

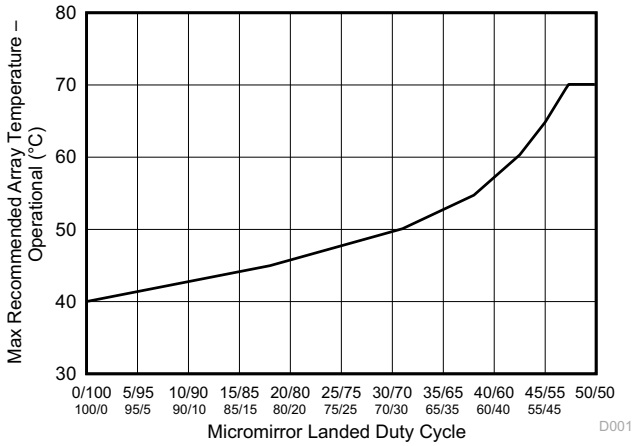


図 6-1. Max Recommended Array Temperature – Derating Curve

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6.5 Thermal Information

THERMAL METRIC[1]		DLP4710LC FQL (LGA) 100 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)[1]	1.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the セクション 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD[3] [4]	V_{DD} = 1.95 V			260	mA
		V_{DD} = 1.8 V		180		
I_{DDI}	Supply current: VDDI[3] [4]	V_{DDI} = 1.95 V			62	mA
		V_{DDI} = = 1.8 V		40		
I_{OFFSET}	Supply current: VOFFSET[5] [6]	V_{OFFSET} = 10.5 V			7.4	mA
		V_{OFFSET} = 10 V		6.3		
I_{BIAS}	Supply current: VBIAS[5] [6]	VBIAS = 18.5 V			1.1	mA
		VBIAS = 18 V		0.9		
I_{RESET}	Supply current: VRESET[6]	VRESET = –14.5 V			5.4	mA
		VRESET = –14 V		4.4		
POWER[7]						
P_{DD}	Supply power dissipation: VDD[3] [4]	VDD = 1.95 V			507	mW
		VDD = 1.8 V		324		
P_{DDI}	Supply power dissipation: VDDI[3] [4]	VDDI = 1.95 V			120.9	mW
		VDD = 1.8 V		72		
P_{OFFSET}	Supply power dissipation: VOFFSET[5] [6]	VOFFSET = 10.5 V			77.7	mW
		VOFFSET = 10 V		63		
P_{BIAS}	Supply power dissipation: VBIAS[5] [6]	VBIAS = 18.5 V			20.35	mW
		VBIAS = 18 V		16.2		
P_{RESET}	Supply power dissipation: VRESET[6]	VRESET = –14.5 V			78.3	mW
		VRESET = –14 V		61.6		
P_{TOTAL}	Supply power dissipation: Total			536.8	804.25	mW
LPSDR INPUT[8]						
$V_{IH(DC)}$	DC input high voltage[9]		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage[9]		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage[9]		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage[9]		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	図 6-10	0.1 × VDD		0.4 × VDD	V
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT[10]						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V

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PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (1080 × 240) micromirrors	400		450	pF

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) LPSDR specification is for pin LS_RDATA.

6.7 Timing Requirements

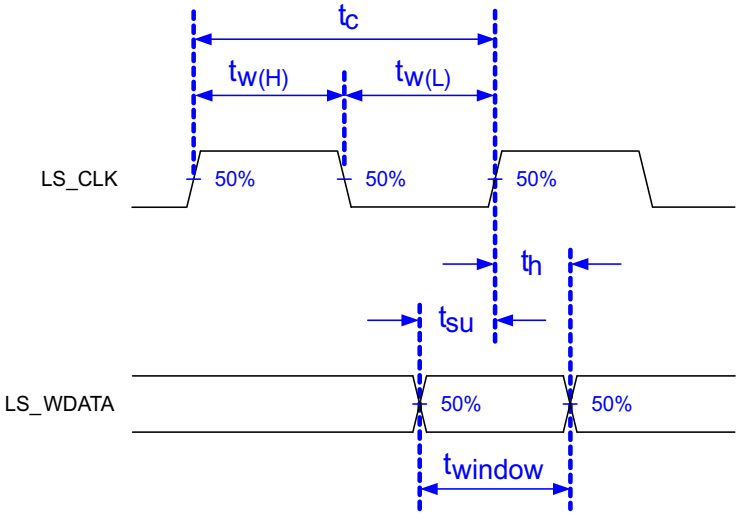
Device electrical characteristics are over *セクション 6.4* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × VDD, 図 6-3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × VDD, 図 6-3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × VDD, 図 6-3	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × VDD, 図 6-3	0.25			V/ns
t_c	Cycle time LS_CLK,	図 6-2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, 図 6-2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, 図 6-2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, 図 6-2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, 図 6-2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time, 図 6-2	3.0			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, 図 6-5		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, 図 6-4	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, 図 6-4	0.7	1		V/ns
t_c	Cycle time DCLK,	図 6-6	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, 図 6-6	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, 図 6-6	0.79			ns
t_{su}	Setup time	D(0:7) valid before DCLK ↑ or DCLK ↓, 図 6-6				
t_h	Hold time	D(0:7) valid after DCLK ↑ or DCLK ↓, 図 6-6				
t_{WINDOW}	Window time	Setup time + Hold time, 図 6-6, 図 6-7	3.0			ns

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			MIN	NOM	MAX	UNIT
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in 図 6-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 図 6-3 .
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to the *セクション 6.6* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

図 6-2. LPSDR Switching Parameters

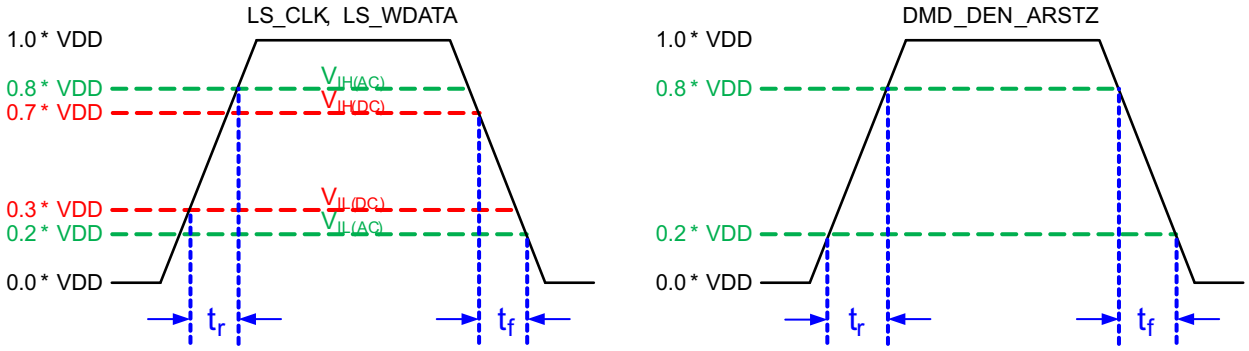


図 6-3. LPSDR Input Rise and Fall Slew Rate

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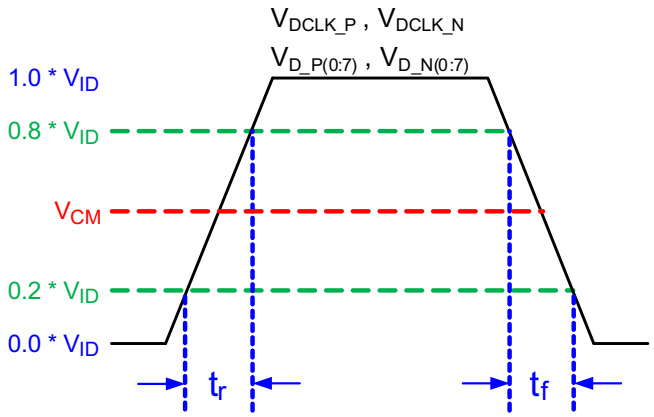


図 6-4. SubLVDS Input Rise and Fall Slew Rate

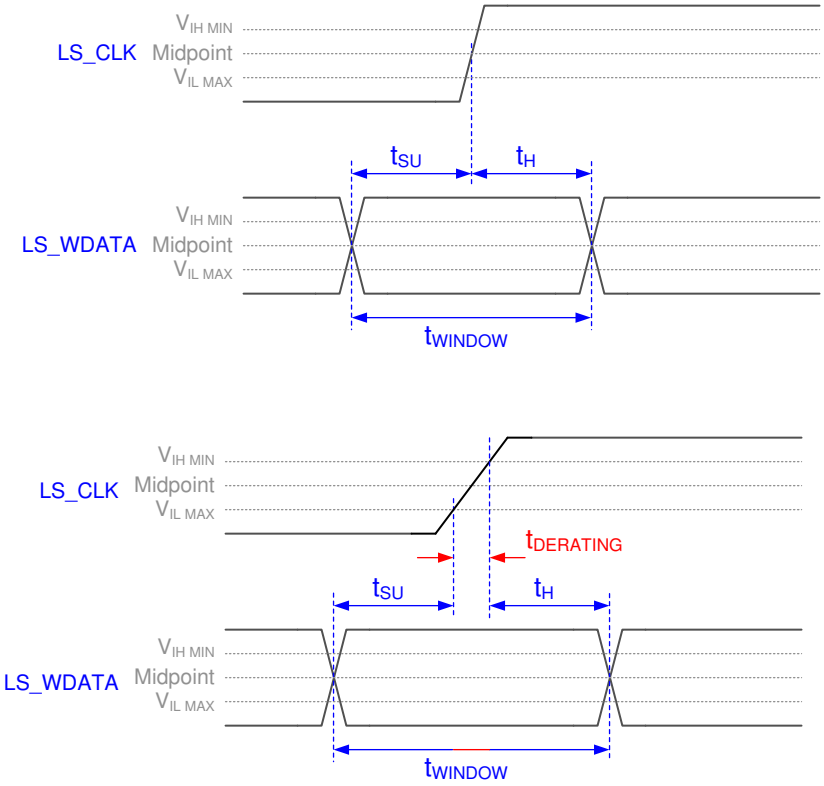


図 6-5. Window Time Derating Concept

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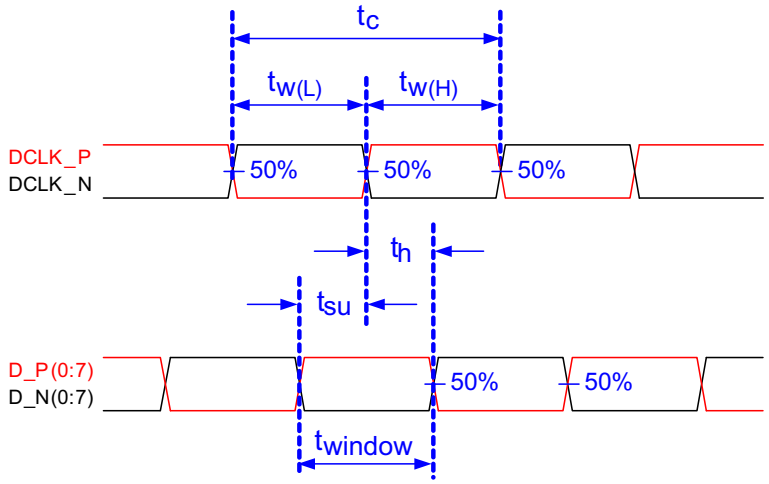
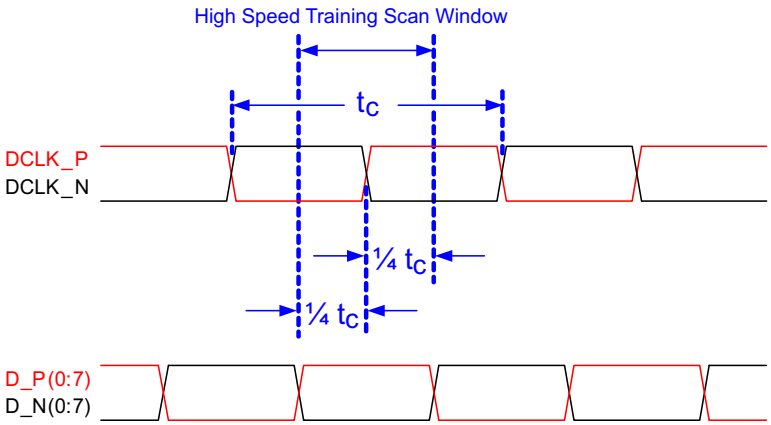


図 6-6. SubLVDS Switching Parameters



Note: Refer to *セクション 7.3.3* for details.

図 6-7. High-Speed Training Scan Window

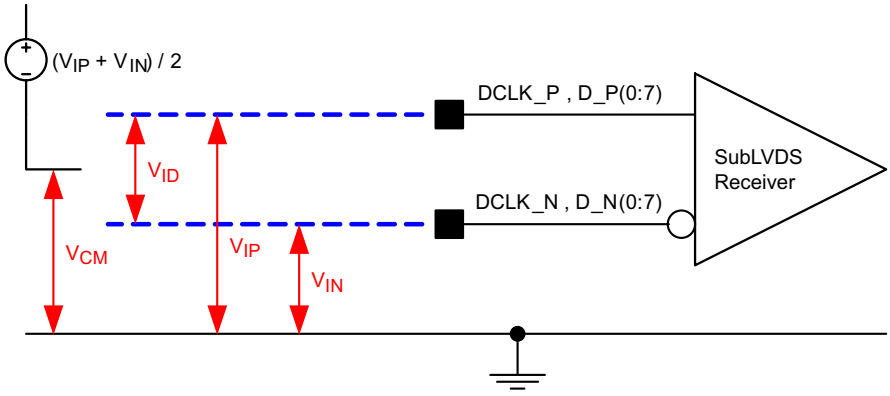


図 6-8. SubLVDS Voltage Parameters

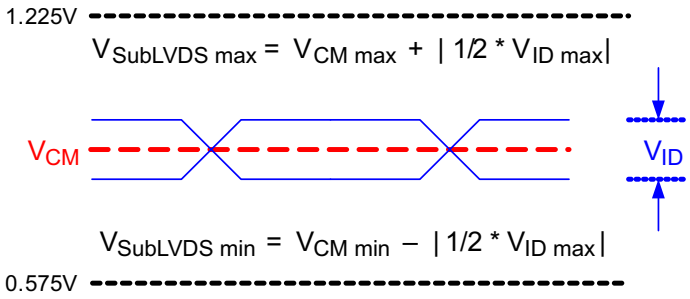


図 6-9. SubLVDS Waveform Parameters

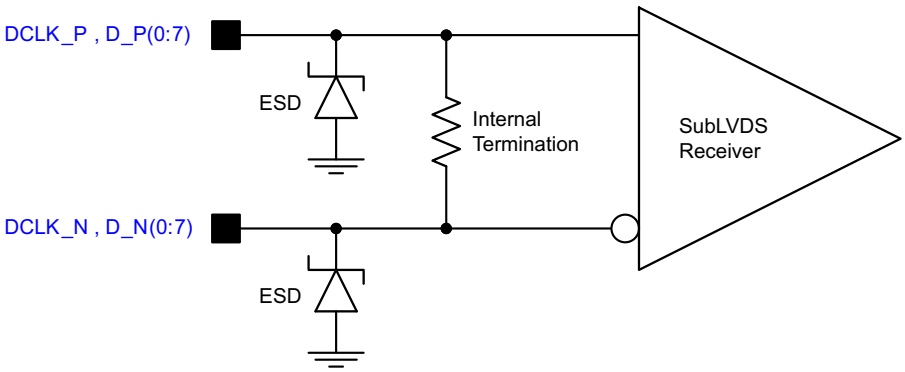


図 6-10. SubLVDS Equivalent Input Circuit

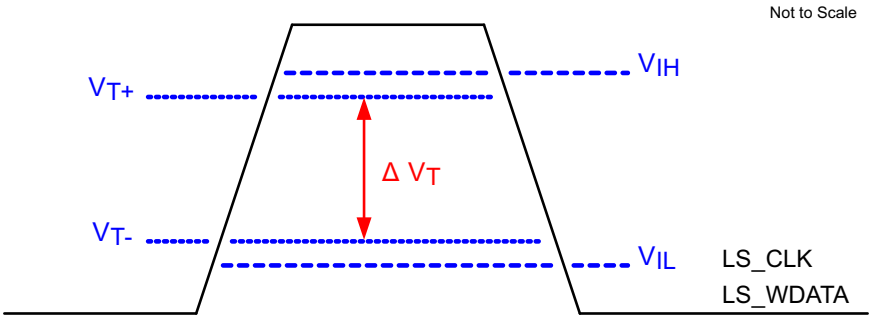


図 6-11. LPSDR Input Hysteresis

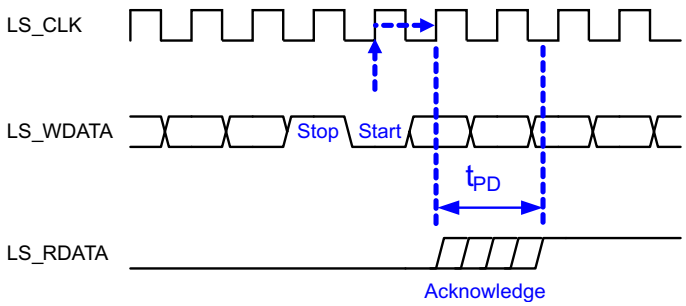
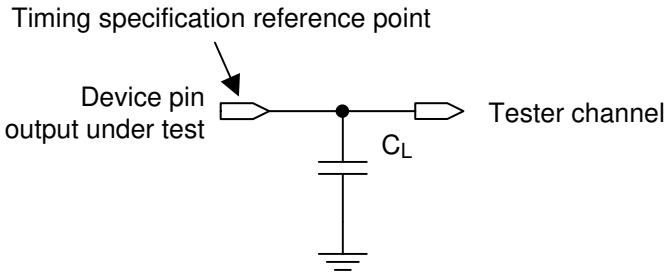


図 6-12. LPSDR Read Out

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See *Timing* for more information.

図 6-13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. (figure 12 xref)	C_L = 45 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal interface area (see 図 6-14)			62	N
	Clamping and electrical interface area (see 図 6-14)			110	N

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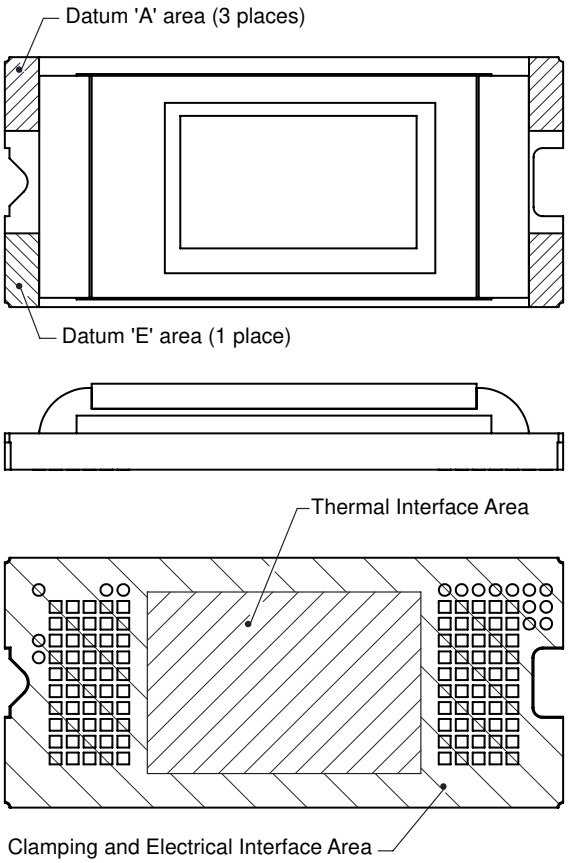


図 6-14. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

	PARAMETER		VALUE	UNIT
	Number of active columns	See 図 6-15	1920	micromirrors
	Number of active rows	See 図 6-15	1080	micromirrors
ε	Micromirror (pixel) pitch	See 図 6-16	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see 図 6-15	10.368	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see 図 6-15	5.832	mm
	Micromirror active border	Pond of micromirror (POM)(1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

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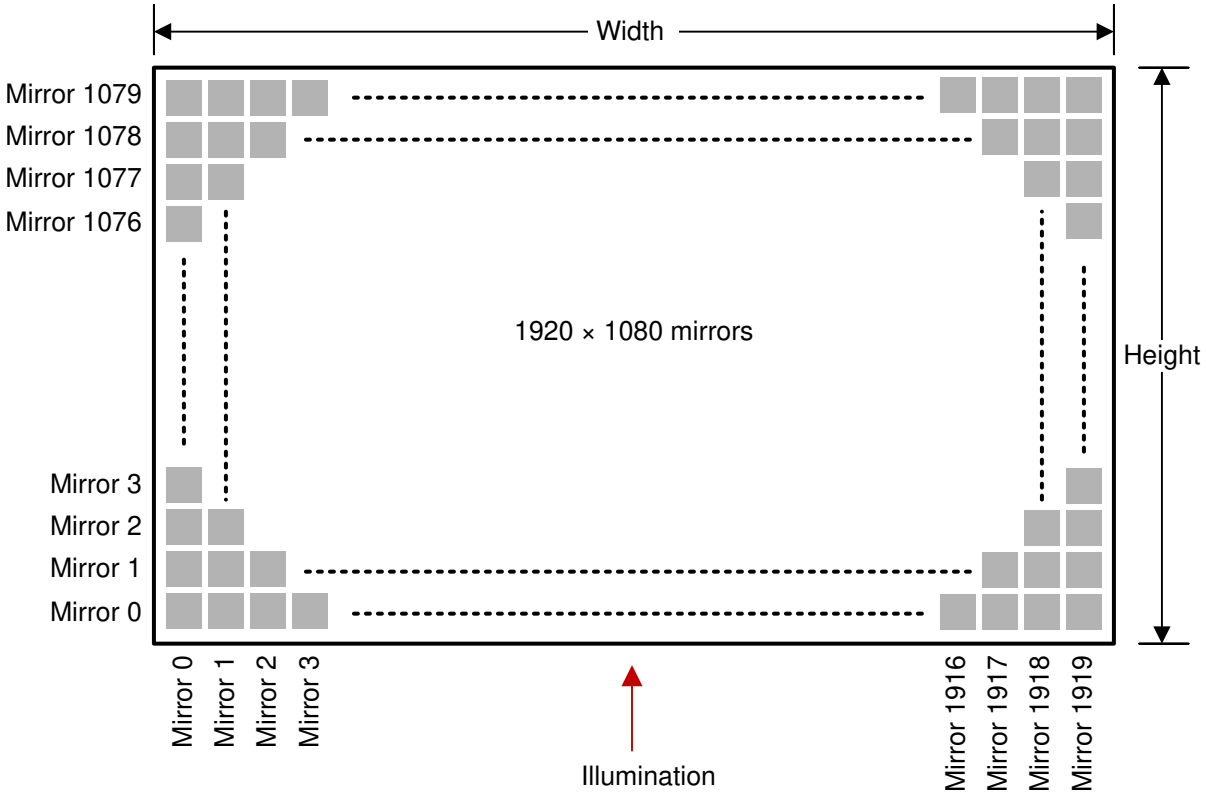


図 6-15. Micromirror Array Physical Characteristics

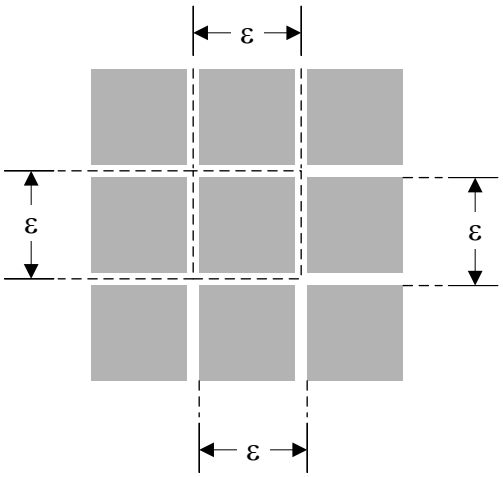


図 6-16. Mirror (Pixel) Pitch

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6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state(1)		17		degree
Micromirror tilt angle tolerance(2) (3) (4) (5)			–1.4		1.4	degree
Micromirror tilt direction (6) (7)		Landed ON state		180		degree
		Landed OFF state		270		
Micromirror crossover time(8)		Typical performance		1	3	µs
Micromirror switching time(9)		Typical performance	10			
Image performance(10)	Bright pixel(s) in active area (11)	Gray 10 Screen (12)			0	micromirrors
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
	Dark pixel(s) in the active area (14)	White Screen			4	
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See 図 6-17.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38 inch minimum viewing distance
The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

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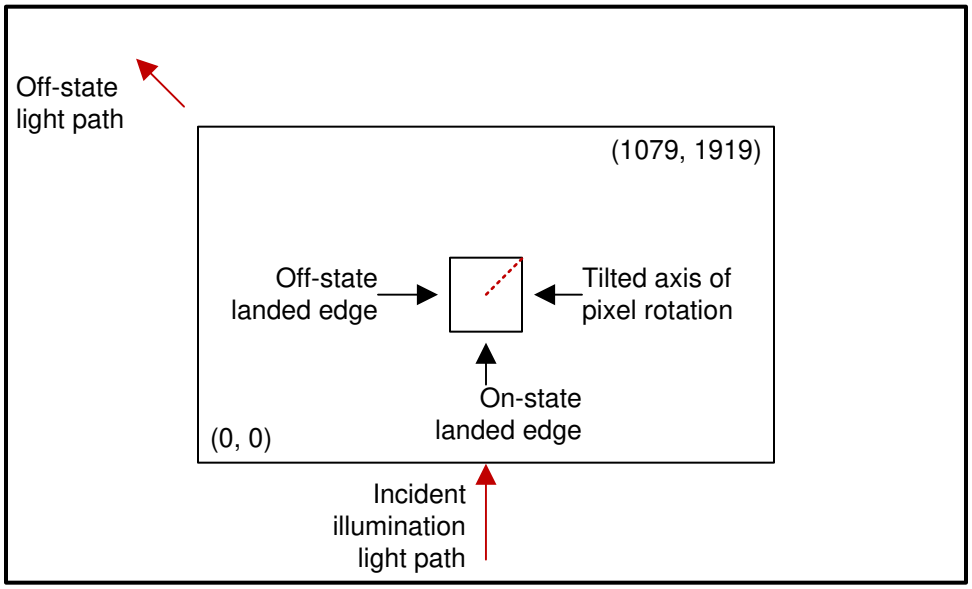


図 6-17. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER[1]		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture[2]				See [2]	
Illumination overfill[3]				See [3]	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Optical Interface and System Image Quality Considerations* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP4710LC device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

The DLP4710 is a component of one or more TI ®DLP chipsets. Reliable function and operation of the DLP4710 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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6.14 Software Requirements

Note

The DLP4710 DMD has mandatory software requirements. Refer to *Software Requirements for TI ®DLP ™Pico TRP Digital Micromirror Devices* application report for additional information. Failure to use the specified software will result in failure at power up.

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7 Detailed Description

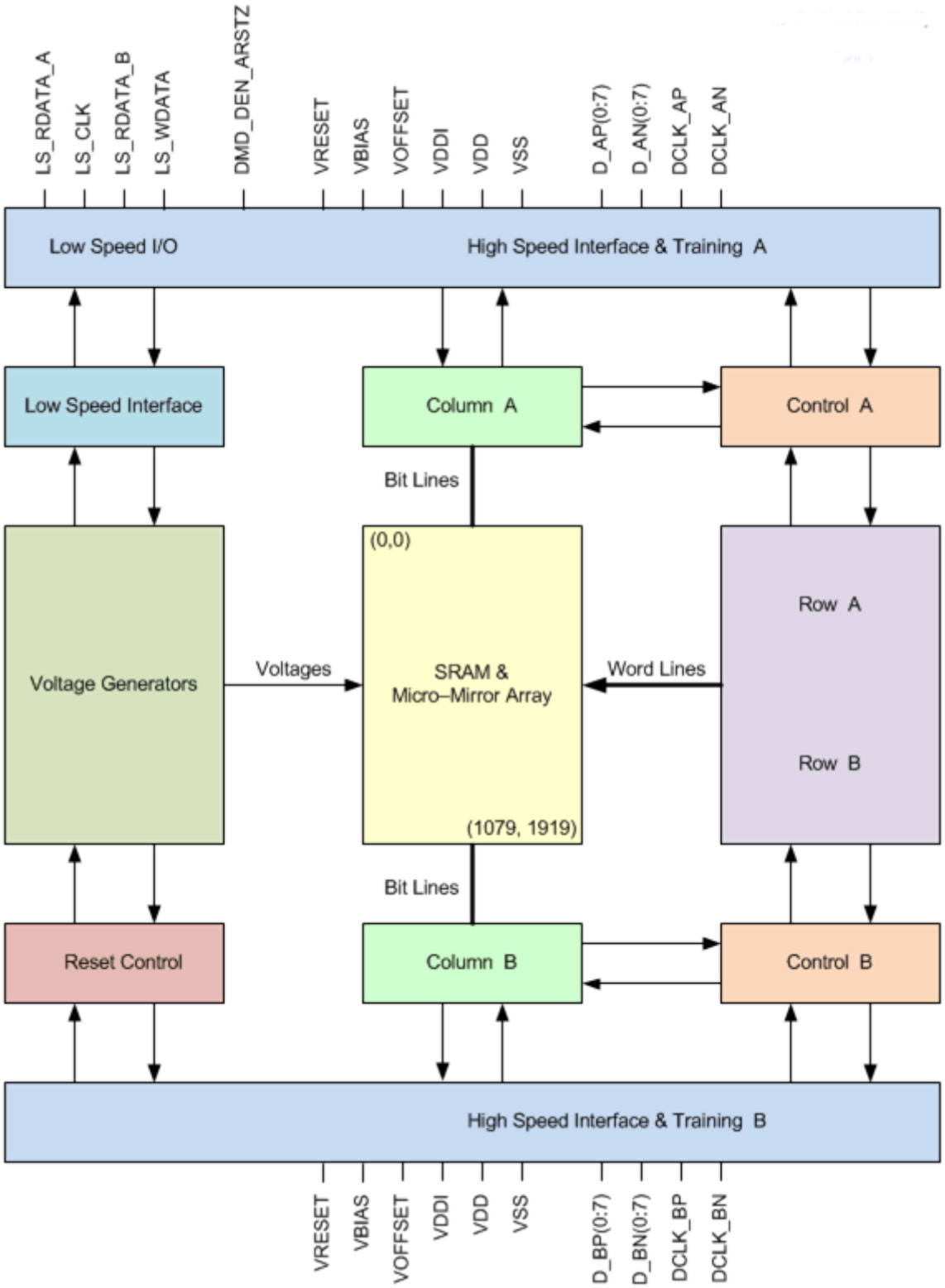
7.1 Overview

The DLP4710LC device is a 0.47 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1920 columns by 1080 rows in a square grid pixel arrangement. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

DLP4710LC device is part of the chipset comprising the DLP4710LC DMD, DLPC3479 controller, and DLPA3000 or DLPA3005 PMIC/LED driver. To ensure reliable operation, the DLP4710LC DMD must always be used with either the DLPC3479 controller and the DLPA3000 or DLPA3005 PMIC/LED drivers.

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7.2 Functional Block Diagram



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Note

Simplified for clarity.

7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA3000/DLPA3005, contains three regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC3479 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing test results at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. 図 6-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is intended for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3479 controller. See the DLPC3479 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area is typically the same. Ensure this angle does not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger

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than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area may occur.

7.5.1.2 Pupil Match

The optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Be sure to design an illumination optical system that limits light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular optical architecture, overfill light may require further reduction below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

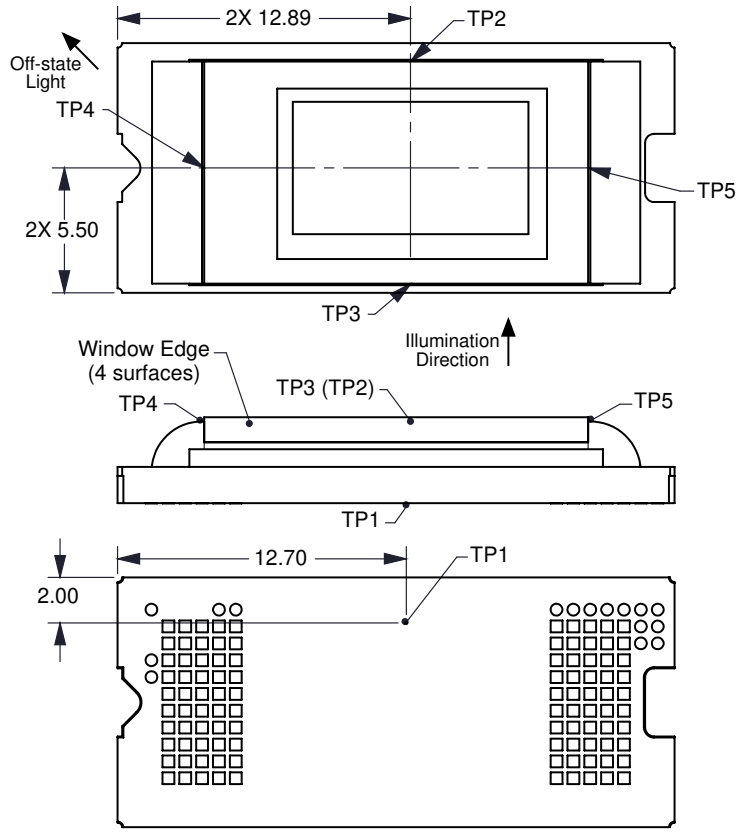


図 7-1. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

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$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

where

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in 図 7-1
- $R_{ARRAY–TO–CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in セクション 6.5
- Q_{ARRAY} = Total DMD power; electrical plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

The electrical power dissipation of the DMD varies and depends on the voltages, data rates and operating frequencies. Use a nominal electrical power dissipation of 0.25 W to calculate array temperature. Absorbed optical power from the illumination source varies and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. The conversion constant assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

The following is a sample calculation for typical projection application:

$T_{CERAMIC}$ = 55°C (measured)

SL = 1500 lm (measured)

$Q_{ELECTRICAL}$ = 0.25 W

CL2W = 0.00266 W/lm

Q_{ARRAY} = 0.25 W + (0.00266 W/lm × 1500 lm) = 4.24 W

T_{ARRAY} = 55°C + (4.24 W × 1.1°C/W) = 59.66°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On and Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time), whereas 25/75 indicates that the pixel is in the OFF state 75% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

When assessing landed duty cycle, the time spent switching from the current state to the opposite state is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.In practice, image processing algorithms in the DLP chipset can result a total of less that 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

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It is the symmetry or asymmetry of the landed duty cycle that is relevant. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD. This interaction can be used to reduce the impact that an asymmetrical landed duty cycle has on the useable life of the DMD. 図 6-1 describes this relationship. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a give long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel depends on the image content being displayed by that pixel.

In the simplest case for example, when the system displays pure-white on a given pixel for a given time period, that pixel operates very close to a 100/0 landed duty cycle during that time period. Likewise, when the system displays pure-black, the pixel operates very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Nominal Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

To account for color rendition (and continuing to ignore image processing for this example) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where *color cycle time* describes the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the nominal landed duty cycle of a given pixel can be calculated as shown in 式 4:

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_\%} \times \text{Red_Scale_Value}) + (\text{Green_Cycle_\%} \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_\%} \times \text{Blue_Scale_Value}) \quad (4)$$

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where

- Red_Cycle_% represents the percentage of the frame time that red displays to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green displays to achieve the desired white point
- Blue_Cycle_% represents the percentage of the frame time that blue displays to achieve the desired white point

For example, assume that the ratio of red, green and blue color cycle times are as listed in 表 7-2 (in order to achieve the desired white point) then the resulting nominal landed duty cycle for various combinations of red, green, blue color intensities are as shown in 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

表 7-3. Color Intensity Combinations

Red Scale Value	Green Scale Value	Blue Scale Value	Nominal Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to consider when estimating the landed duty cycle is any applied image processing. In the DLPC34xx controller family, the two functions which influence the actual landed duty cycle are Gamma and IntelliBright™, and bitplane sequencing rules.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC34xx controller family, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 7-2.

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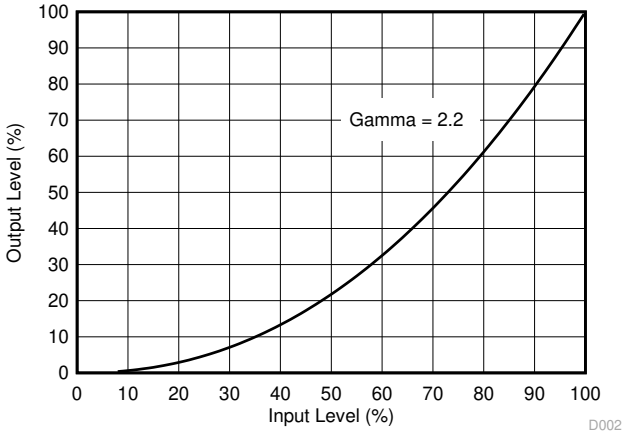


図 7-2. Example of Gamma = 2.2

As shown in 図 7-2, when the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Because gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3439 or DLPC3479 controller.

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8 Application and Implementation

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the dual DLPC3479 controllers. The new high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Applications of interest include

DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005. Refer to *Power Supply Recommendations* for power-up and power-down specifications. To ensure reliable operation, the DLP4710LC DMD must always be used with two DLPC3479 controllers and a DLPA3000 or DLPA3005 PMIC/LED driver.

8.2 Typical Application

A pico-projector that can be used as an accessory to a smartphone, tablet or a laptop is a common application when using a DLP4710LC DMD and two DLPC3479 devices. The two DLPC3479 devices in the pico-projector receive images from a multimedia front end within the product as shown in 図 8-1.

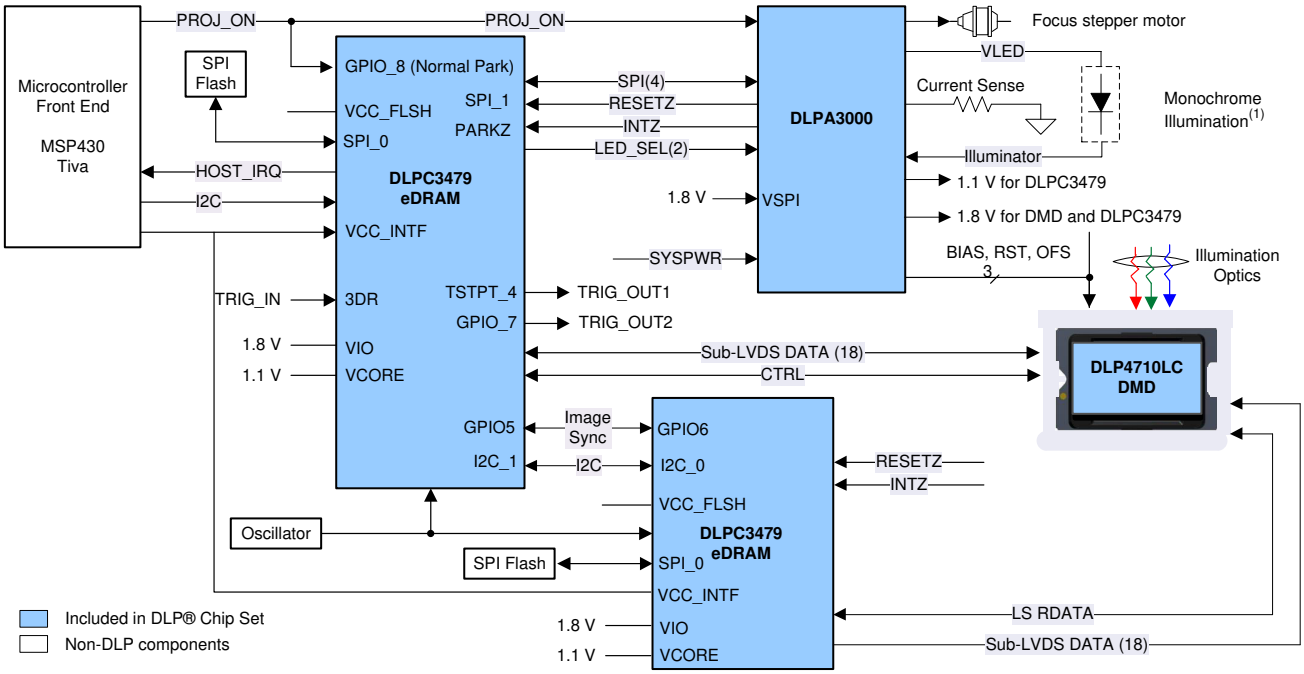


図 8-1. Typical Application Diagram

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of a DLP4710 DMD, two DLPC3439 controllers and a DLPA3000/DLPA3005 PMIC/LED driver. The DLPC3439 controllers do the digital image processing, the DLPA3000/DLPA3005 provides the needed analog functions for the projector, and the DLP4710 DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips are needed. At a minimum a Flash part is needed to store the software and firmware to control each DLPC3439 controller.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

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For connecting the DLPC3439 controllers to the multimedia front end for receiving images, a 24-bit parallel interface is used. An I2C interface should be connected to the multimedia front end for sending commands to one of the DLPC3439 controllers for configuring the DLPC3439 controller for different features.

8.2.2 Detailed Design Procedure

For connecting the two DLPC3439 controllers, the DLPA3000/DLPA3005, and the DLP4710 DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in 図 8-2. For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

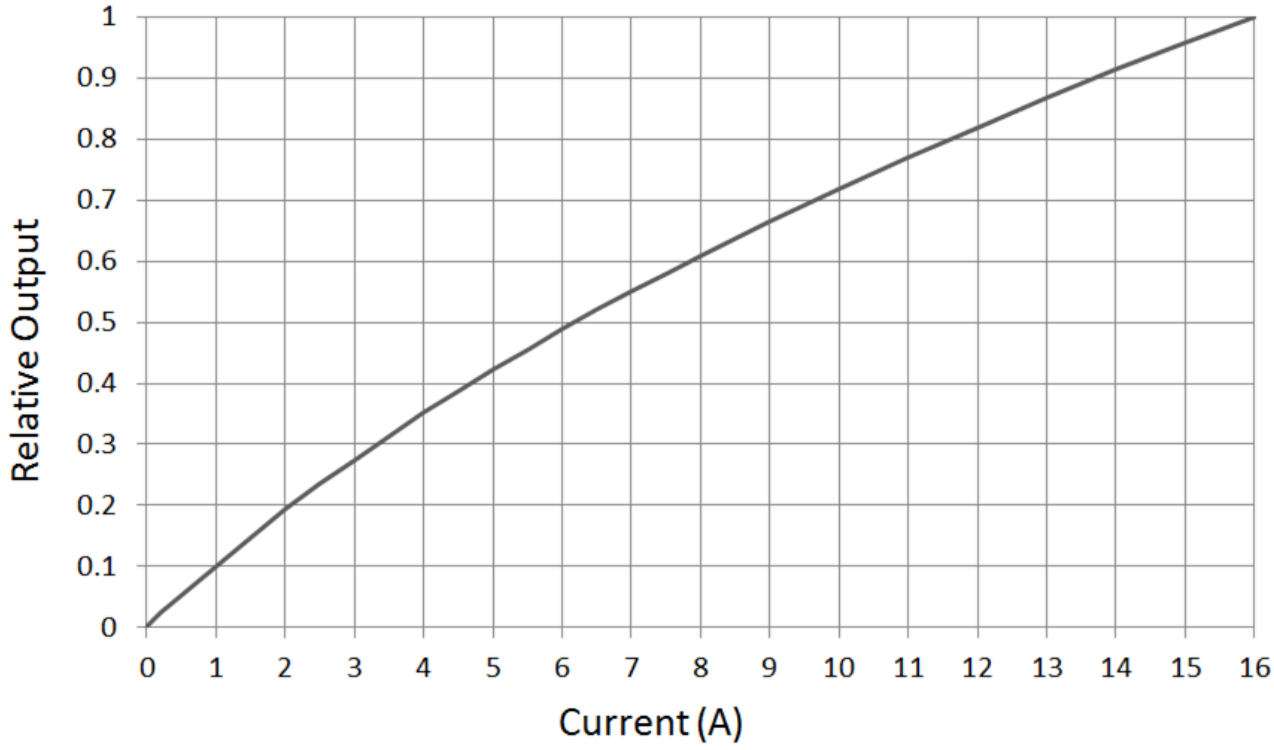


図 8-2. Luminance vs Current

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9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005 devices.

Note

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 23. VSS must also be connected.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 23. VSS must also be connected.

9.1 DMD Power Supply Power-Up Procedure

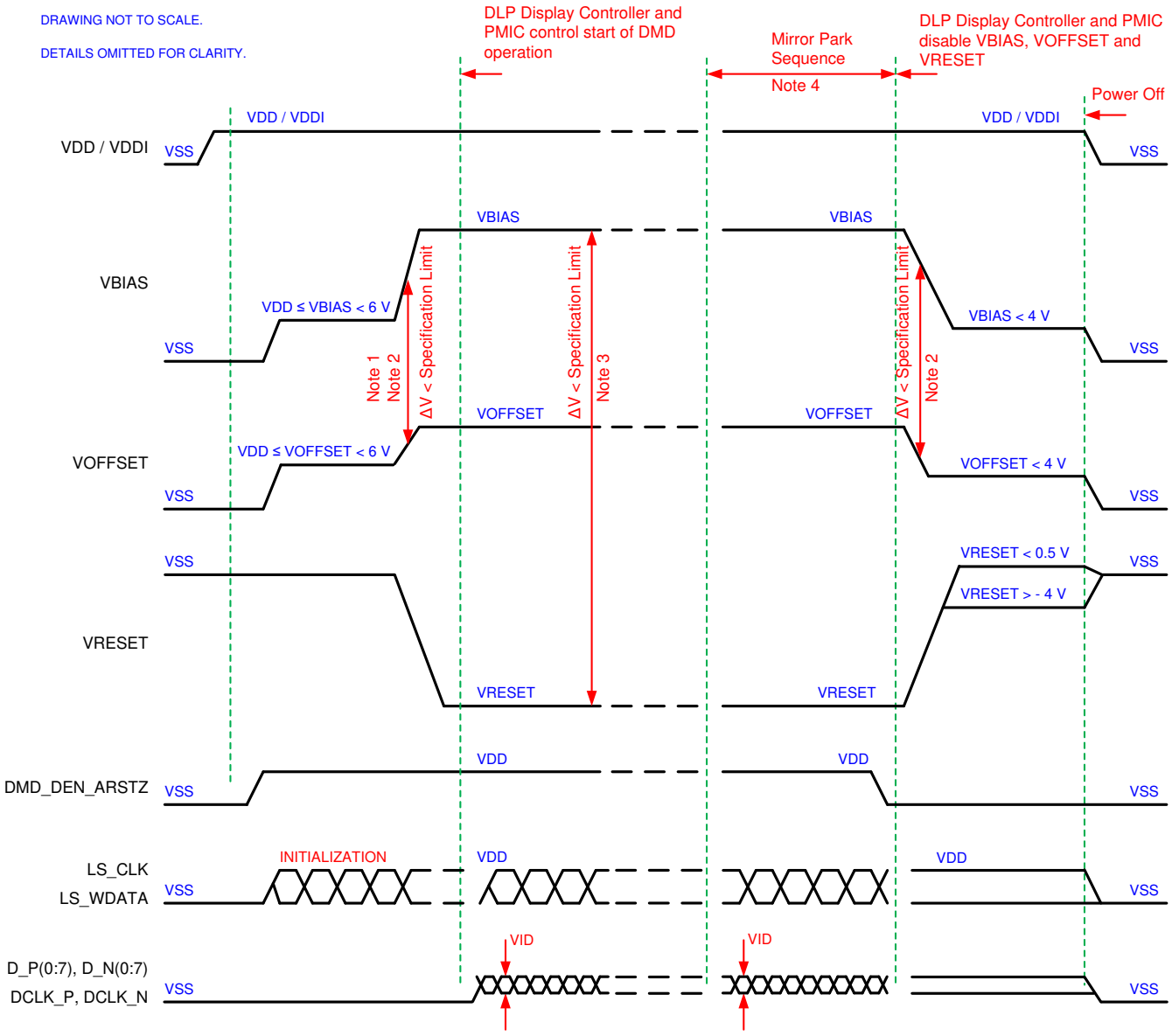
- During the power-up sequence, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During the power-up sequence, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in *セクション 6.4*. Refer to 表 9-1 for the power-up sequence, delay requirements.
- During the power-up sequence, there is no requirement for the relative timing of VRESET with respect to VBIAS and VOFFSET.
- Power supply slew rates during the power-up sequence are flexible, provided that the transient voltage levels follow the requirements specified in *セクション 6.1*, in *セクション 6.4*, and in セクション 9.3.
- During the power-up sequence, LPSDR input pins must not be driven high until after VDD/VDDI have settled at operating voltages listed in *セクション 6.4*.

9.2 DMD Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. During the power-down sequence, VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During the power-down sequence, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in *セクション 6.4*.
- During the power-down sequence, there is no requirement for the relative timing of VRESET with respect to VBIAS and VOFFSET.
- Power supply slew rates during the power-down sequence, are flexible, provided that the transient voltage levels follow the requirements specified in *セクション 6.1*, in *セクション 6.4*, and in セクション 9.3.
- During the power-down sequence, LPSDR input pins must be less than VDD/VDDI specified in *セクション 6.4*.

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9.3 Power Supply Sequencing Requirements



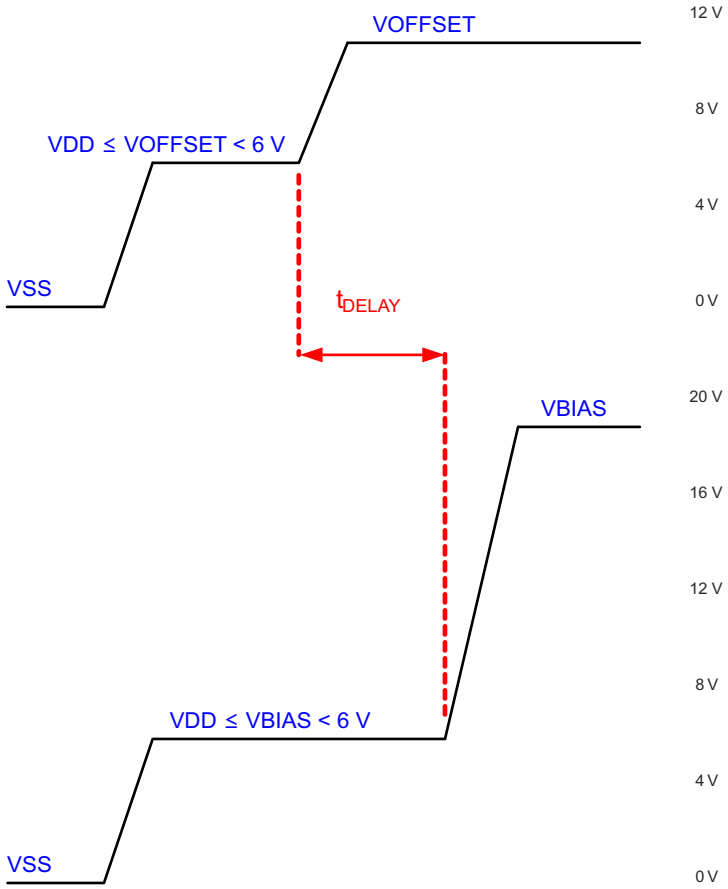
A. DLP controller and PMIC controls start of DMD operation
B. Mirror park sequence starts
C. Mirror park sequence ends. DLP controller and PMIC disables VBIAS, VOFFSET, and VRESET.
D. Power off.
E. Refer to 表 9-1 and 図 9-2 for critical power-up sequence delay requirements.
F. When system power is interrupted, the ASIC driver initiates hardware the power-down sequence, that disables VBIAS, VRESET and VOFFSET after the micromirror park sequence is complete. Software the power-down sequence, disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control.
G. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit shown in *セクション 6.4*.
H. Drawing is not to scale and details are omitted for clarity.

図 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

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表 9-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from VOFFSET power up to VBIAS power up	2		ms
VOFFSET	Supply voltage level during power–up sequence delay (see 図 9-2)		6	V
VBIAS	Supply voltage level during power–up sequence delay (see 図 9-2)		6	V



A. Refer to 表 9-1 for VOFFSET and VBIAS supply voltage levels during power-up sequence delay.

図 9-2. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and Ctrl signals between the DLPC3439 controller and the DLP4710 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer 図 10-1.
- Minimum of two 220-nF decoupling capacitor close to VBIAS. Capacitor C3 and C10 in 図 10-1.
- Minimum of two 220-nF decoupling capacitor close to VRST. Capacitor C1 and C9 in 図 10-1.
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C2 and C8 in 図 10-1.
- Minimum of four 220-nF decoupling capacitor close to VDDI and VDD. Capacitor C4, C5, C6 and C7 in 図 10-1.

10.2 Layout Example

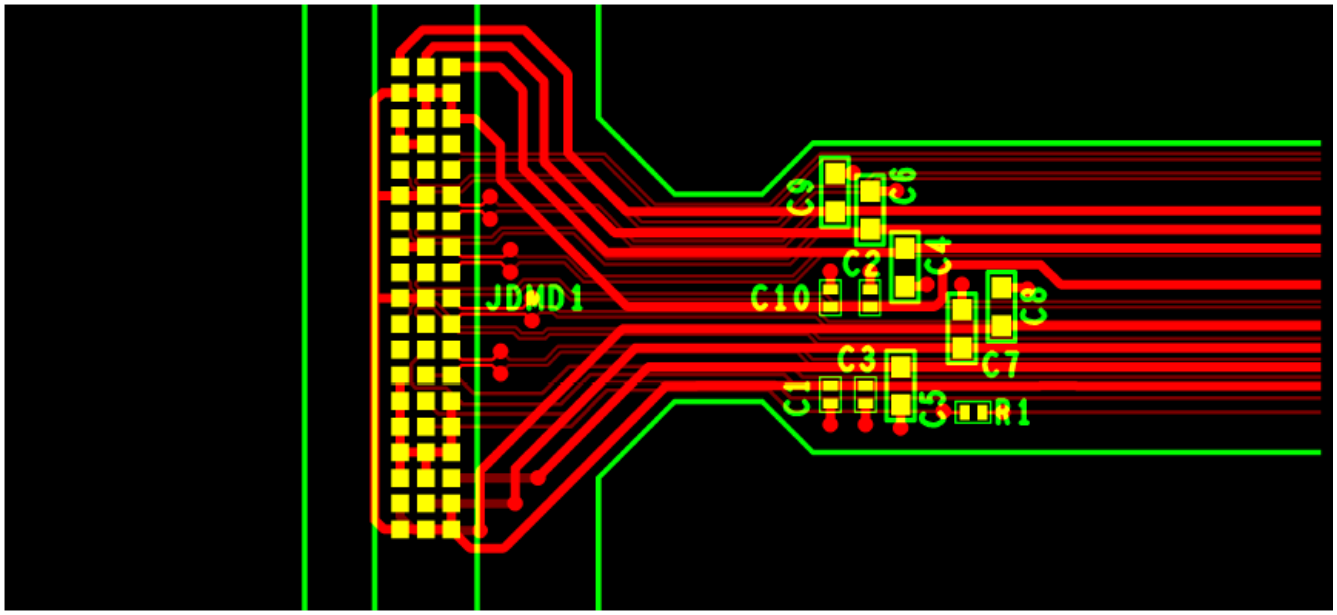


図 10-1. Power Supply Connections

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

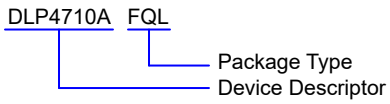


図 11-1. Part Number Description

11.1.3 Device Markings

The device marking includes the legible character string GHJJJJK DLP4710AFQL. GHJJJJK is the lot trace code. DLP4710AFQL is the device marking.

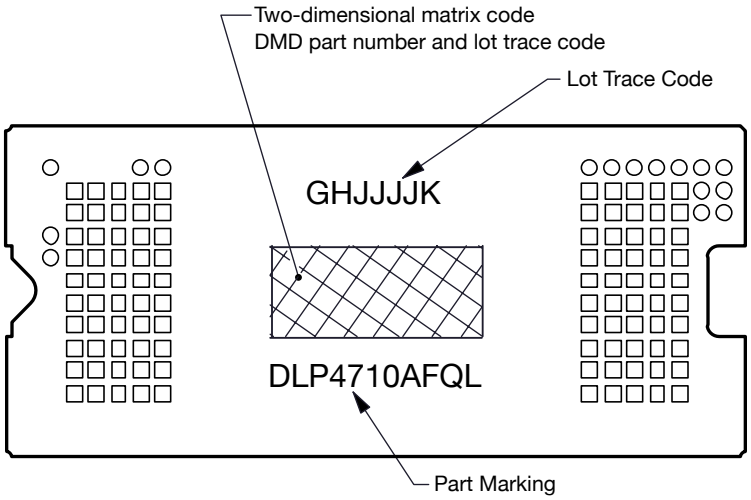


図 11-2. DMD Marking Locations

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP4710	Click here	Click here	Click here	Click here	Click here
DLPC3439	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here
DLPA3005	Click here	Click here	Click here	Click here	Click here

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11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP4710AFQL	ACTIVE	CLGA	FQL	100	80	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

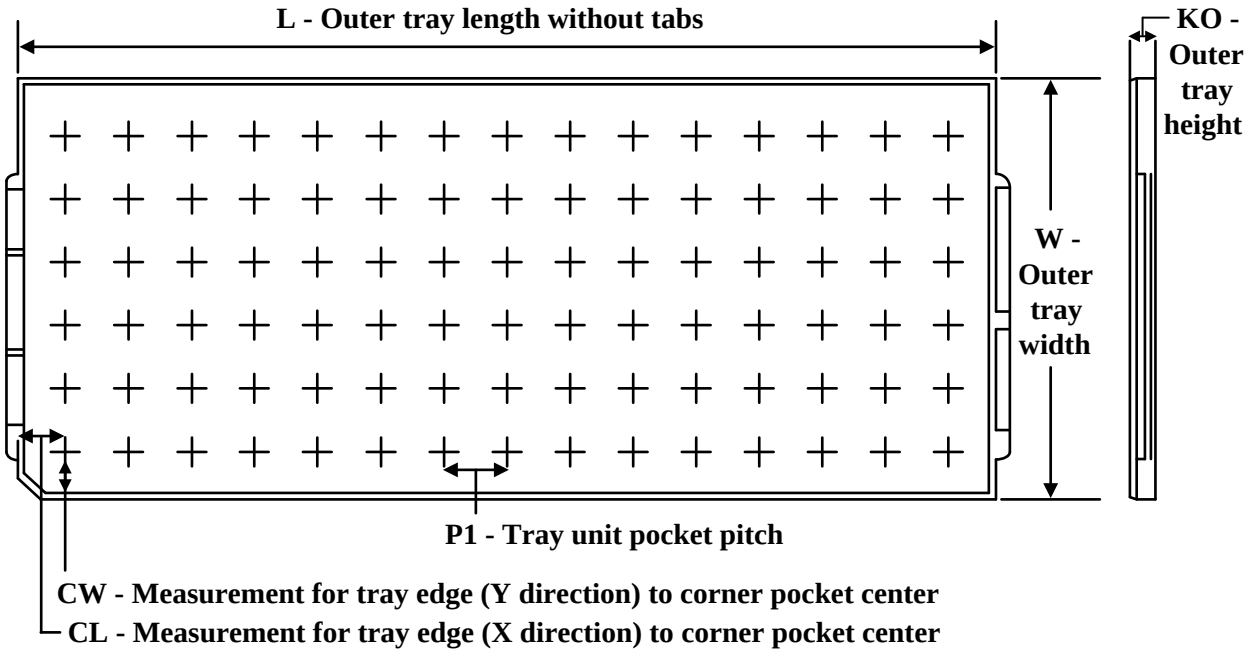
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

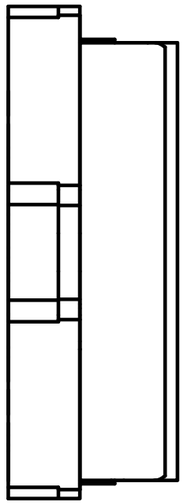
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP4710AFQL	FQL	CLGA	100	80	8 x 10	150	315	135.9	12190	28	31.5	15.45

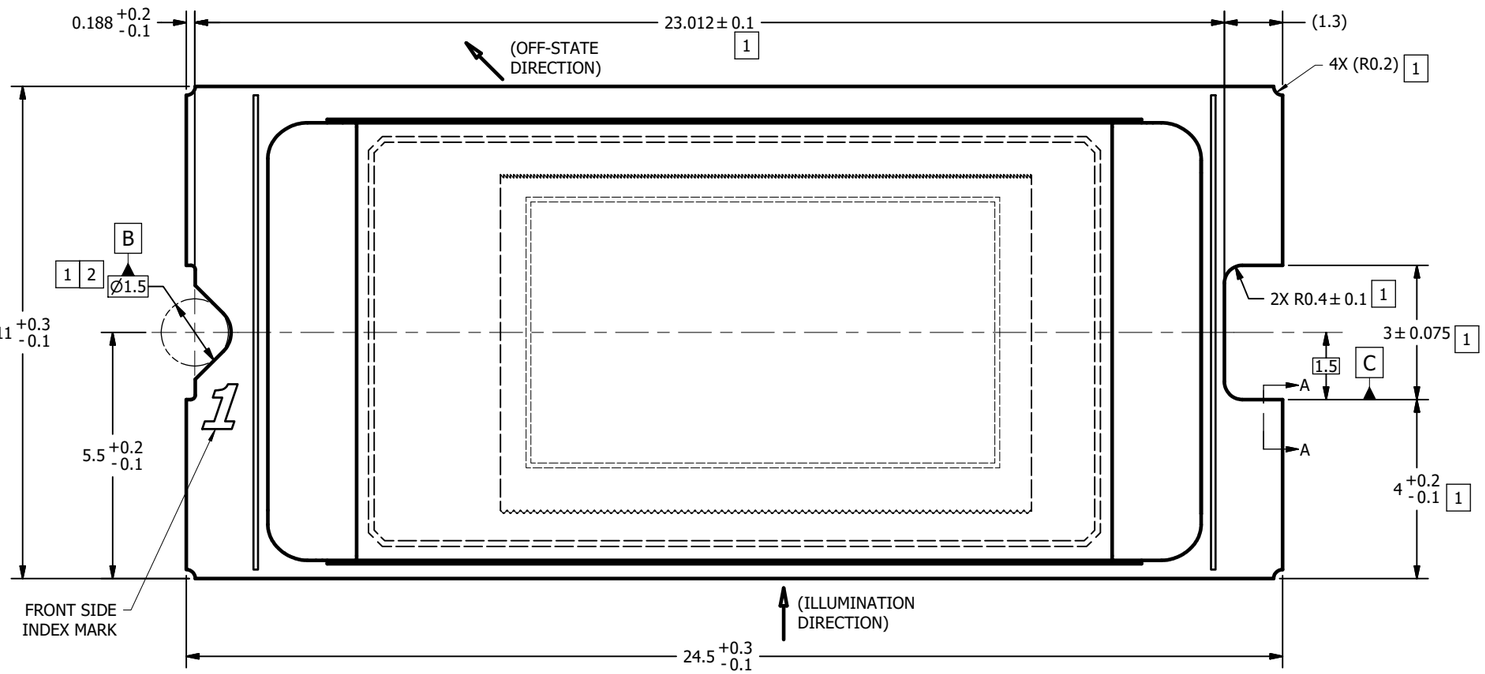
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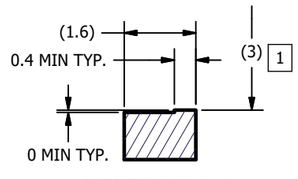
REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2140050: INITIAL RELEASE	2/20/2014	BMH
B	ECO 2140429: CORRECT DATUM C IN VIEW J-J, SH. 3	3/6/2014	BMH
C	ECO 2142093: DELETE BACK SIDE FLATNESS SPEC	5/22/2014	BMH
D	ECO 2145057: ADD "FQL PACKAGE" TO DRAWING TITLE	7/20/2016	BMH
E	ECO 2187241: ADD APERTURE SLOT PICTORIALLY	4/23/2020	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

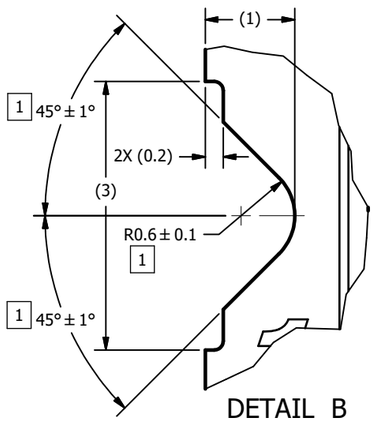
1. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
2. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
3. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
4. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
8. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.



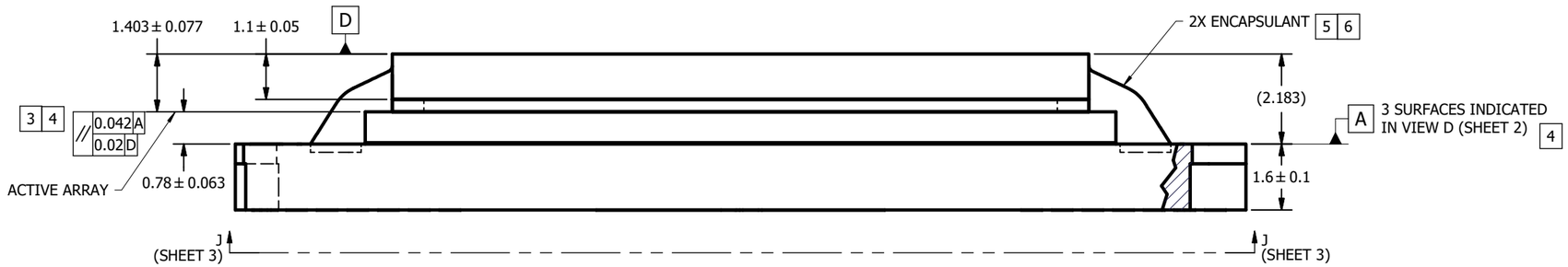




SECTION A-A
NOTCH OFFSETS



DETAIL B
V-NOTCH
SCALE 30 : 1



	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	2/20/2014
ENGINEER	B. HASKETT	2/20/2014
QA/CE	P. KONRAD	2/26/2014
CM	S. SUSI	2/25/2014
	M. DORAK	2/23/2014
APPROVED	R. LONG	2/26/2014

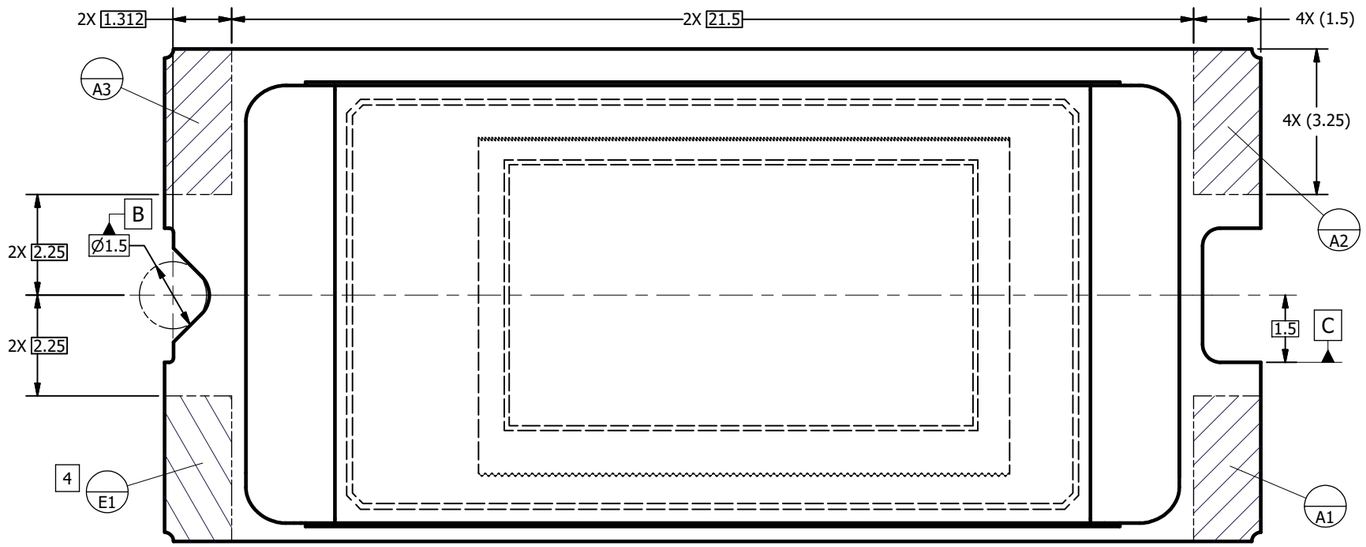
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .47 1080p SERIES 312 (FQL PACKAGE)

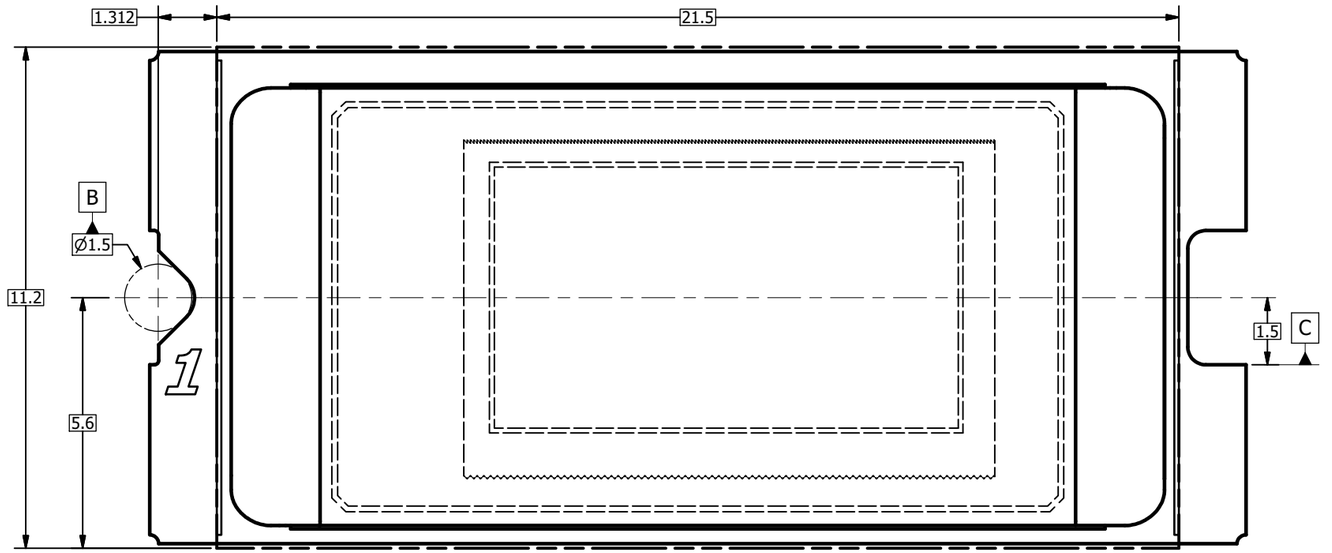
SIZE	DWG NO	REV
D	2513652	E

SCALE 15:1 SHEET 1 OF 3

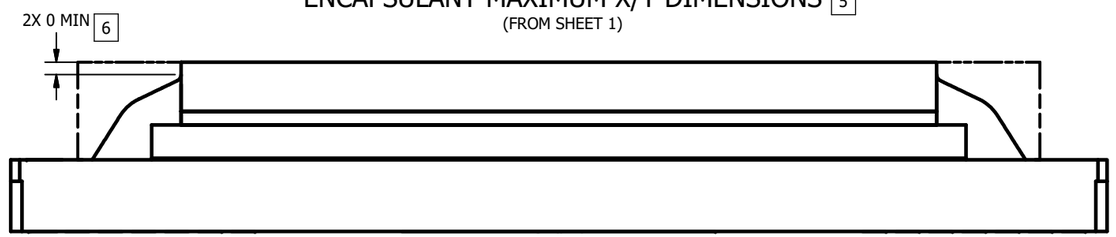
INV11-2006a



VIEW C
DATUMS A AND E
(SUBSTRATE METALLIZATION OMITTED FOR CLARITY)
(FROM SHEET 1)



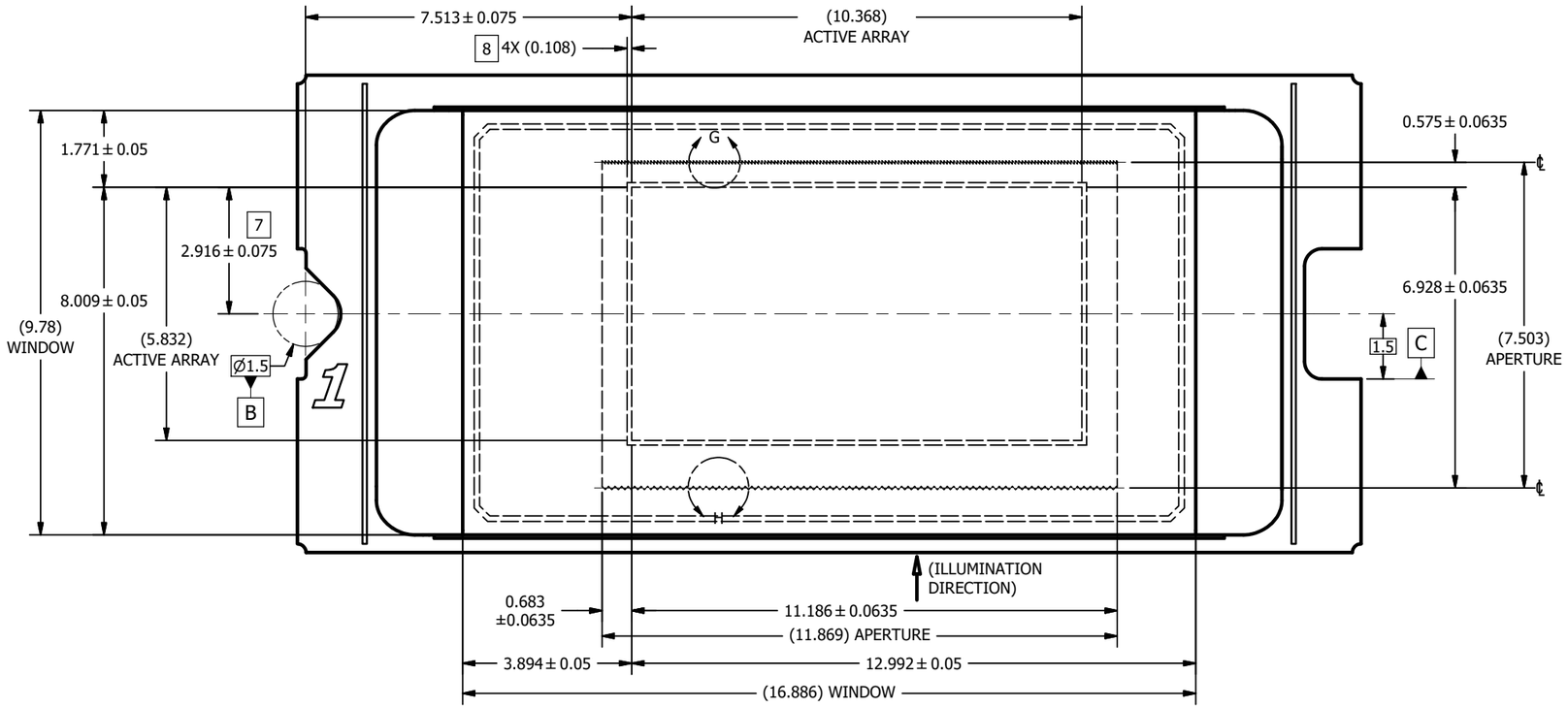
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



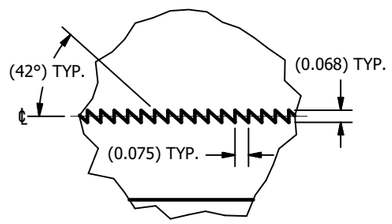
VIEW E
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 2/20/2014	SIZE D	DWG NO 2513652	REV E
			SCALE	SHEET 2 OF 3	

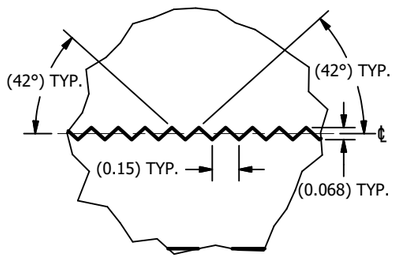
INV11-2006a



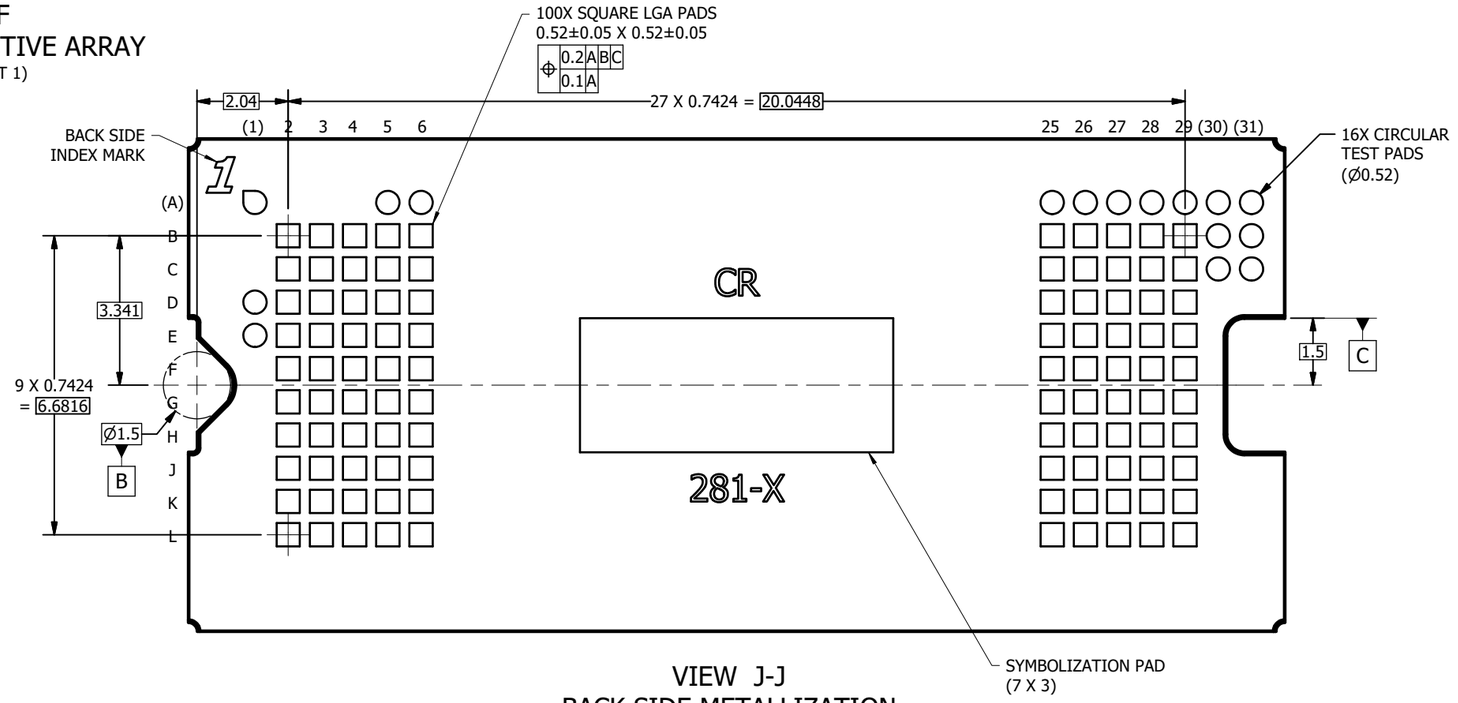
VIEW F
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL G
APERTURE TOP EDGE
SCALE 60 : 1



DETAIL H
APERTURE BOTTOM EDGE
SCALE 60 : 1



VIEW J-J
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 2/20/2014	SIZE D	DWG NO 2513652	REV E
			SCALE	SHEET 3 OF 3	

INV11-2006a

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