LM2903-Q1 および LM2903B-Q1 車載用デュアル・コンパレータ

特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 0:-40℃～150℃の動作時周囲温度範囲 (LM2903E-Q1)
  - デバイス温度グレード 1:-40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル H1C
  - デバイス CDM ESD 分類レベル C4B
- 「B」デバイスの HBM ESD を 2kV に改善
- 「B」デバイスでは 3 温度テストが利用可能
- シングル電源またはデュアル電源
- 電源電圧に依存しない低い消費電流、コンパレータあたり 200µA (標準値) (「B」バージョン)
- 低い入力バイアス電流、3.5nA (標準値) (「B」デバイス)
- 低い入力オフセット電流、0.5nA (標準値) (「B」デバイス)
- 低い入力オフセット電圧、±0.37mV (標準値) (「B」デバイス)
- 同相入力電圧範囲にはグランドを含む
- 差動入力電圧範囲は最大定格電源電圧と同じ ±36V
- TTL、MOS、CMOS 互換出力
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能

アプリケーション

- 車載用
  - HEV / EV およびパワートレイン
  - インフォテインメントとクラスタ
  - ボディ・コントロール・モジュール
- 産業用
- 家電製品

概要

LM2903B-Q1 デバイスは、業界標準の LM2903-Q1 コンパレータ・ファミリの次世代バージョンです。この次世代ファミリは、小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、小さい伝搬遅延、優れた 2kV の ESD 性能などの特長と、そのまま置き換えることができる利便性を兼ね備えており、コストの制約が厳しい用途で大きな価値を提供します。

すべてのデバイスは、広い電圧範囲にわたって動作するように設計された 2 つの独立した電圧コンパレータで構成されています。デュアル電源でも、2 つの電源間の差分が 2V～36V の範囲内であり、VCC が入力同相電圧より 1.5V 以上高ければ、動作可能です。出力は、他のオープン・コレクタ出力に接続できます。

LM2903-Q1 と LM2903B-Q1 は、AEC-Q100 グレード 1 の温度範囲 (-40℃～+125℃) で認定済みです。LM2903E-Q1 はグレード 0 の拡張温度範囲 (-40℃～+150℃) で認定済みです。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM2903B-Q1	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm
	SOT-23 (8)	1.60mm × 2.90mm
LM2903-Q1	SOIC (8)	4.90mm × 3.91mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
LM2903E-Q1	TSSOP (8)	3.00mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ファミリ比較表

仕様	LM2903B-Q1	LM2903-Q1	LM2903-Q1 「A」デバイス	LM2903-Q1 「AV」デバイス	LM2903E-Q1	単位
電源電圧仕様	2～36	2～30	2～30	2～32	2～30	V
総電源電流 (5V～V_S (最大値))	0.6～0.8	1～2.5	1～2.5	1～2.5	1～2.5	mA
温度範囲	-40～125	-40～125	-40～125	-40～125	-40～150	℃
ESD (HBM / CDM)	2k / 1k	1k / 750	1k / 750	1k / 750	1k / 750	V
オフセット電圧 (全温度範囲での最大値)	±4	±15	±4	±4	±15	mV
入力バイアス電流 (標準値 / 最大値)	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 250	nA
応答時間 (標準値)	1	1.3	1.3	1.3	1.3	µsec

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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1 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision K (August 2022) to Revision L (August 2023) **Page**

- Added reference to Application Note 17

Changes from Revision J (November 2020) to Revision K (August 2022) **Page**

- Added T, R and H Temp Test Options table 7

Changes from Revision I (June 2020) to Revision J (November 2020) **Page**

- データシート全体を通して、LM2903B-Q1 の最小推奨電源電圧を 2V に変更 1
- Added Operating Virtual Temp to Abs Max Table for both versions 5
- Updated Supply Voltage vs Supply Current graph for 2V 5

Changes from Revision H (January 2020) to Revision I (June 2020) **Page**

- 機能安全のテキストとリンクを追加 1
- 「B」の「製品情報」の一覧に VSSOP パッケージを追加 1
- Added DGK to "B" Thermal Table 6
- Added text to Apps Overview section for ESD 16

Changes from Revision G (November 2018) to Revision H (January 2020) **Page**

- データシートに LM2903B-Q1 を追加 1
- 「製品情報」表を追加 1
- Added "B" device graphs 10
- Changed incorrect input text in Feature Description in Apps Section 16

Changes from Revision F (May 2018) to Revision G (November 2018) **Page**

- Changed previous Q1 graphs to match new format 9
- Added LM2903E-Q1 specific graphs 9

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2 Pin Configuration and Functions

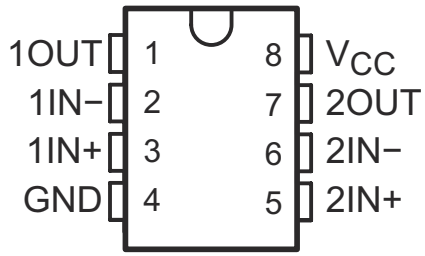
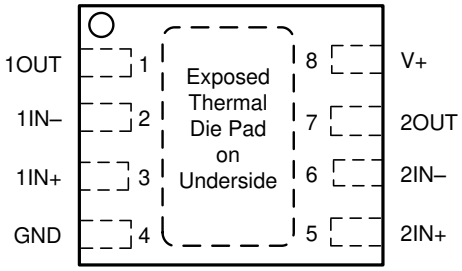


図 2-1. D, DGK, DDF OR PW PACKAGE
Top View



Connect thermal pad directly to GND pin.

図 2-2. DSG Package
8-Pin WSON With Exposed Pad
Top View

2.1 Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP, PDIP, SO, DDF and TSSOP	DSG		
1OUT	1	1	Output	Output pin of comparator 1
1IN–	2	2	Input	Negative input pin of comparator 1
1IN+	3	3	Input	Positive input pin of comparator 1
GND	4	4	—	Ground
2IN+	5	5	Input	Positive input pin of comparator 2
2IN-	6	6	Input	Negative input pin of comparator 2
2OUT	7	7	Output	Output pin of comparator 2
V_{CC}	8	8	—	Positive Supply
Thermal Pad	—	PAD	—	Connect directly to GND pin

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3 Specifications

3.1 Absolute Maximum Ratings, LM2903-Q1 and LM2903E-Q1

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		36	V
V_{CC}	Supply voltage, LM2903E-Q1 Only(2)		32	V
V_{ID}	Differential input voltage(3)	–36	36	V
V_I	Input voltage range (either input)	−0.3	36	V
V_O	Output voltage		36	V
I_O	Output current		20	mA
T_J	Operating virtual-junction temperature		150	°C
T_{SCG}	Duration of output short-circuit to ground		Unlimited	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Differential voltages are at IN+ with respect to IN−.

3.2 Absolute Maximum Ratings, LM2903B-Q1

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	-0.3	38	V
Differential input voltage : V_{ID} (2)		±38	V
Input pins (IN+, IN–)	-0.3	38	V
Current into input pins (IN+, IN–)		-50	mA
Output pin (OUT)	-0.3	38	V
Output sink current		25	mA
Operating virtual-junction temperature		150	°C
Output short-circuit duration(3)		Unlimited	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltages are at IN+ with respect to IN-
(3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

3.3 ESD Ratings, LM2903-Q1 and LM2903E-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range		LM2903-Q1 Only	–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		-1000	1000	V
		Charged device model (CDM), per AEC Q100-011	All pins	-750	750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

3.4 ESD Ratings, LM2903B-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		-2000	2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	-1000	1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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3.5 Recommended Operating Conditions, LM2903B-Q1

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	2	36	V
Ambient temperature, T_A, LM2903B	–40	125	°C
Input voltage range, V_{IVR}	–0.1	(V+) – 2	V

3.6 Recommended Operating Conditions, LM2903-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} (non-V devices)		2	30	V
V_{CC} (V devices)		2	32	V
T_J	Junction Temperature	-40	125	°C

3.7 Recommended Operating Conditions, LM2903E-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		2	30	V
T_J	Junction Temperature	-40	150	°C

3.8 Thermal Information, LM2903-Q1 and LM2903E-Q1

THERMAL METRIC(1)		LM2903E-Q1	LM2903-Q1			UNIT
		PW (TSSOP)	DGK (VSSOP)	PW (TSSOP)	D (SOIC)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.9	199.4	186.6	126.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	120.8	79.6	74.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	108.9	90.2	116.5	66.4	
ψ_{JT}	Junction-to-top characterization parameter	11.9	21.5	17.7	25.4	
ψ_{JB}	Junction-to-board characterization parameter	107.3	119.1	114.9	65.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

3.9 Thermal Information, LM2903B-Q1

THERMAL METRIC(1)		LM2903B-Q1					UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.5	193.7	200.6	96.9	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.2	82.9	89.6	119.0	119.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	91.8	115.5	131.3	63.1	115.4	
ψ_{JT}	Junction-to-top characterization parameter	38.5	20.8	22.1	12.4	19.4	
ψ_{JB}	Junction-to-board characterization parameter	91.1	113.9	129.6	63.0	113.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	38.7	-	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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3.10 Electrical Characteristics LM2903B - Q1

V_S = 5 V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–2.5	±0.37	2.5	mV
		V_S = 5 to 36V, T_A = –40°C to +125°C	–4		4	mV
V_{IO}	Input offset voltage, DGK package only	V_S = 5 to 36V	–3.5	±0.37	3.5	mV
		V_S = 5 to 36V, T_A = –40°C to +125°C	–5		5	mV
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +125°C			–50	nA
I_{OS}	Input offset current		–10	±0.5	10	nA
		T_A = –40°C to +125°C	–25		25	nA
V_{CM}	Common mode range(1)	V_S = 3 to 36V	(V–)		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = –40°C to +125°C	(V–)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
		I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5 V; V_{ID} = 1V		0.1	20	nA
		(V+) = V_O = 36V; V_{ID} = 1V		0.3	50	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)	V_S = 5 V, no load		400	600	µA
		V_S = 36 V, no load, T_A = –40°C to +125°C		550	800	µA

(1) The voltage at any input should not be allowed to go negative by more than 0.3 V. The upper end of the input voltage range is V_{CC} – 1.5 V for one input, and the other input can exceed the V_{CC} level; the comparator provides a proper output state. Either or both inputs can go to 36 V without damage.

3.11 Switching Characteristics LM2903B - Q1

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns

(1) High-to-low and low-to-high refers to the transition at the input.

3.12 LM2903B-Q1 "T", "R" and "H" Temperature Test Options

The following table describes the production temperature testing for the LM2903B-Q1 "H", "R" and "T" options. Specifications are the same as the LM2903B-Q1 above.

Test	LM2903B-Q1	LM2903BR-Q1	LM2903BH-Q1	LM2903BT-Q1
Probe (Wafer)	-	25°C	125°C	-40°C and 125°C
Final (Packaged)	25°C	25°C	25°C	25°C

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3.13 Electrical Characteristics, LM2903-Q1 and LM2903E-Q1

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = $V_{IC(min)}$, V_{CC} = 5 V to MAX(2)	Non-A devices	25°C		2	7	mV
				Full range			15	
			A-suffix devices	25°C		1	2	
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−250	nA
				Full range			−500	
V_{ICR}	Common-mode input voltage range(3)			25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = V_{CC} MAX(2)		Full range			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = −1 V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1	mA
			V_{CC} = MAX(2)	Full range			2.5	

(1) Full range (MIN or MAX) for LM2903-Q1 is −40°C to 125°C and −40°C to 150°C for the LM2903E-Q1 . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) V_{CC} MAX = 30 V for non-V devices and 32 V for V-suffix devices.
(3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is VCC+ − 1.5 V for the inverting input (−), and the non-inverting input (+) can exceed the VCC level; the comparator provides a proper output state. Either or both inputs can go to 30 V (32V for V-suffix devices) without damage.

3.14 Switching Characteristics, LM2903-Q1 and LM2903E-Q1

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive	1.3	µs
	C_L = 15 pF(1) (2)	TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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3.15 Typical Characteristics, LM2903-Q1 and LM2903E-Q1 Only

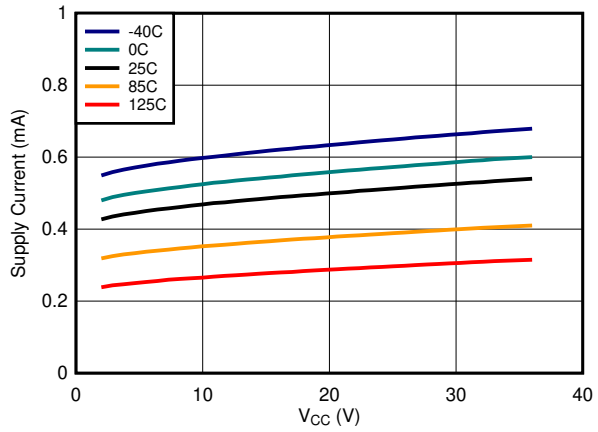


図 3-1. Supply Current vs. Supply Voltage

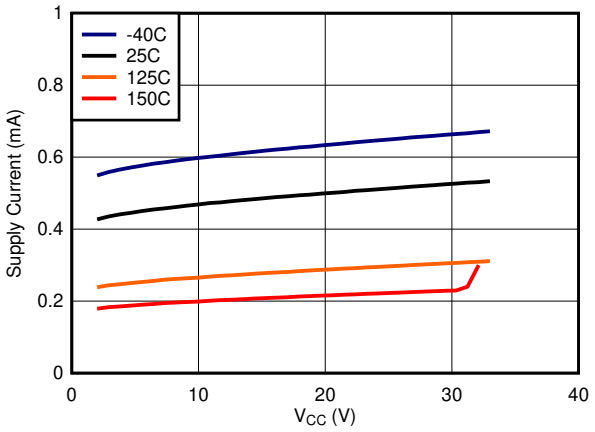


図 3-2. Supply Current vs. Supply Voltage LM2903E-Q1 Only

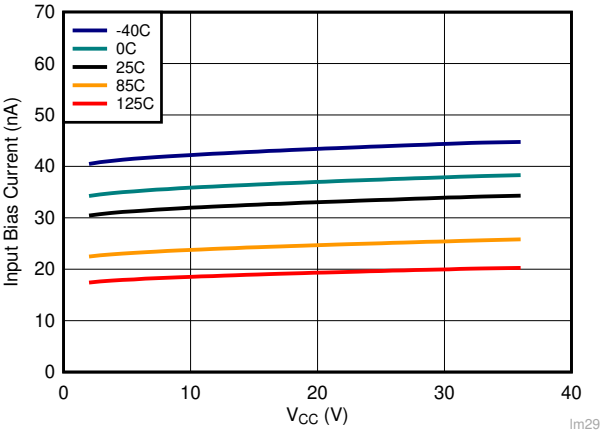


図 3-3. Input Bias Current vs. Supply Voltage

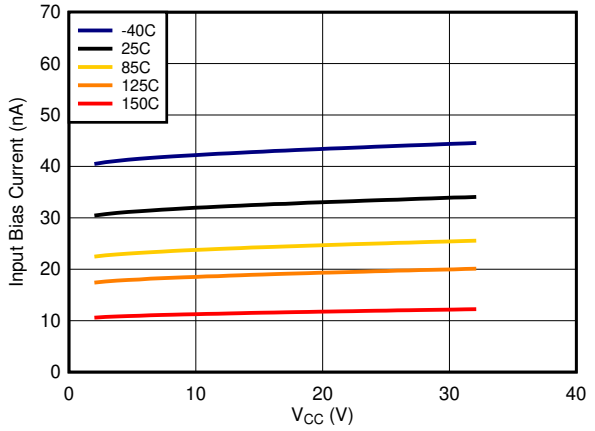


図 3-4. Input Bias Current vs. Supply Voltage LM2903E-Q1 Only

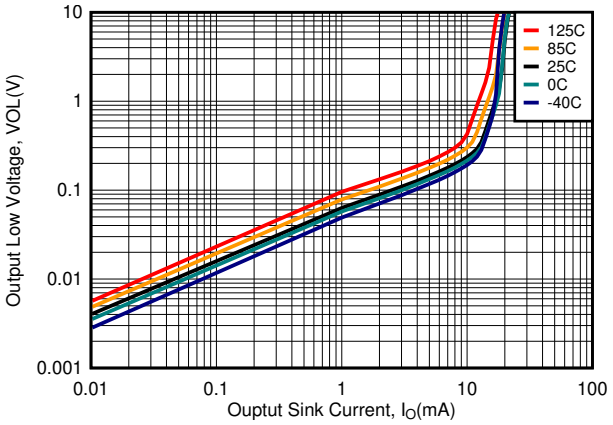


図 3-5. Output Low Voltage vs. Output Current

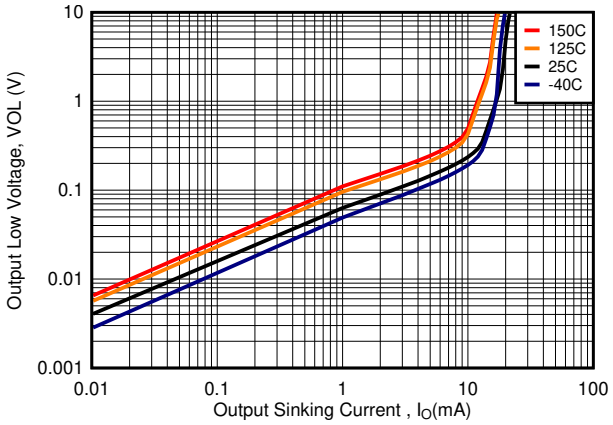


図 3-6. Output Low Voltage vs. Output Current LM2903E-Q1 Only

3.16 Typical Characteristics, LM2903B-Q1 Only

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

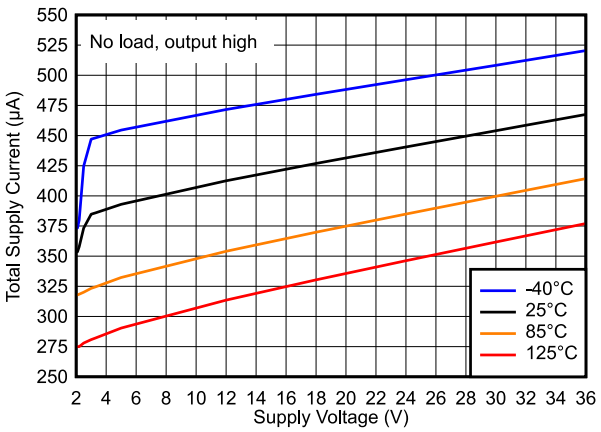


図 3-7. Total Supply Current vs. Supply Voltage

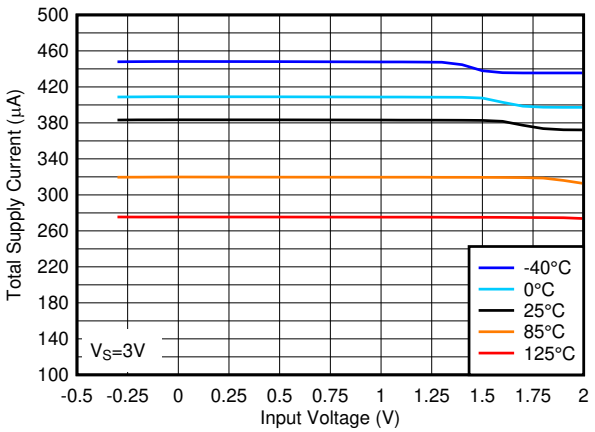


図 3-8. Total Supply Current vs. Input Voltage at 3V

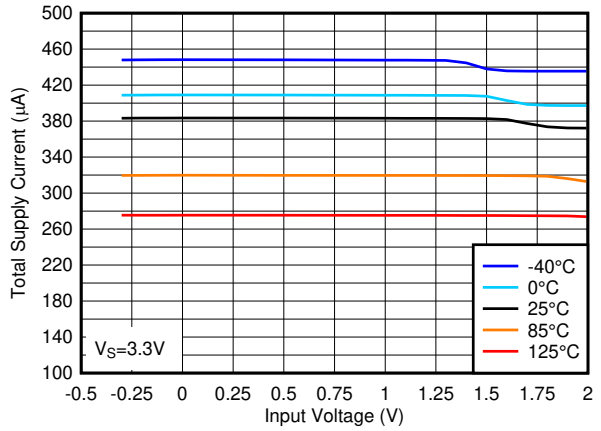


図 3-9. Total Supply Current vs. Input Voltage at 3.3V

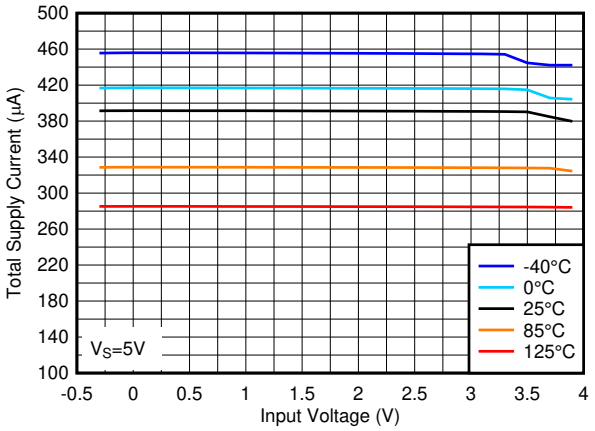


図 3-10. Total Supply Current vs. Input Voltage at 5V

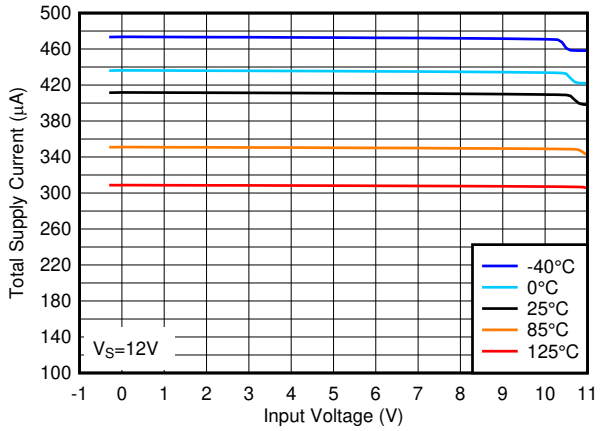


図 3-11. Total Supply Current vs. Input Voltage at 12V

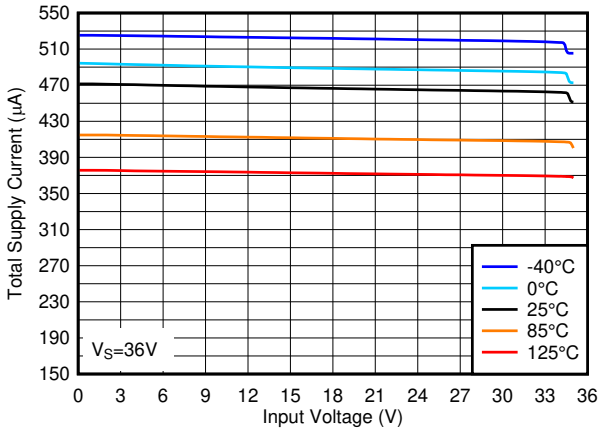


図 3-12. Total Supply Current vs. Input Voltage at 36V

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3.16 Typical Characteristics, LM2903B-Q1 Only (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

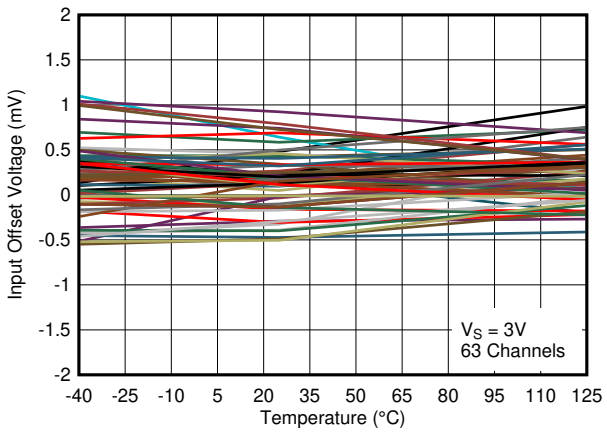


図 3-13. Input Offset Voltage vs. Temperature at 3V

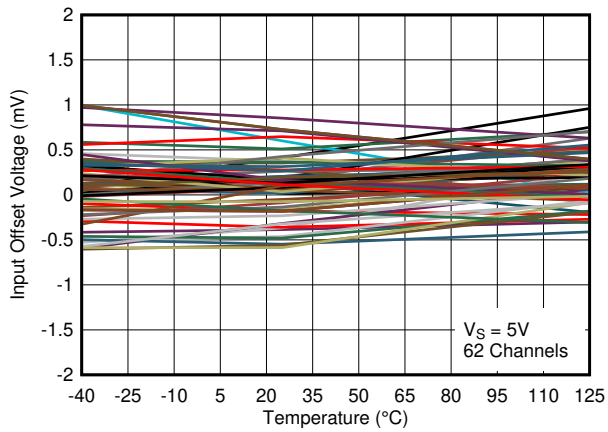


図 3-14. Input Offset Voltage vs. Temperature at 5V

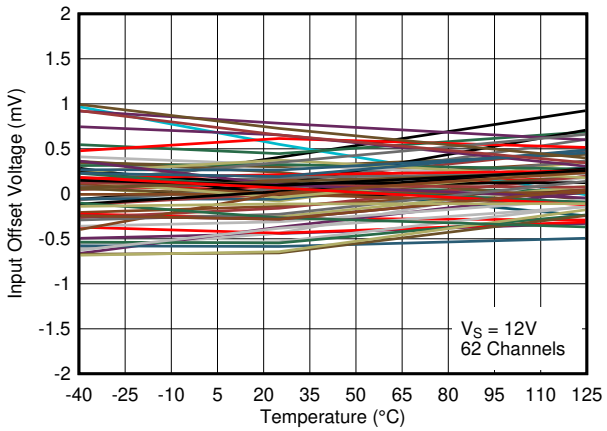


図 3-15. Input Offset Voltage vs. Temperature at 12V

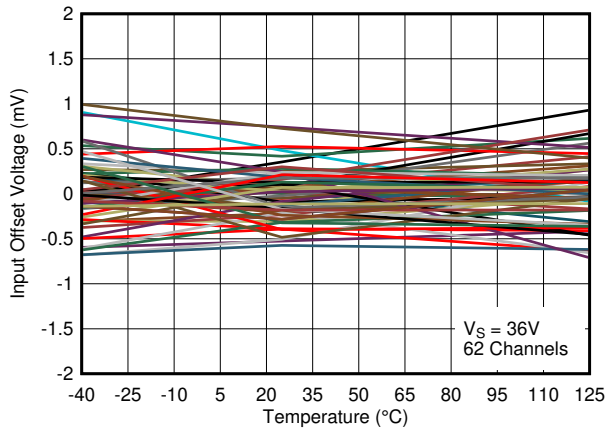


図 3-16. Input Offset Voltage vs. Temperature at 36

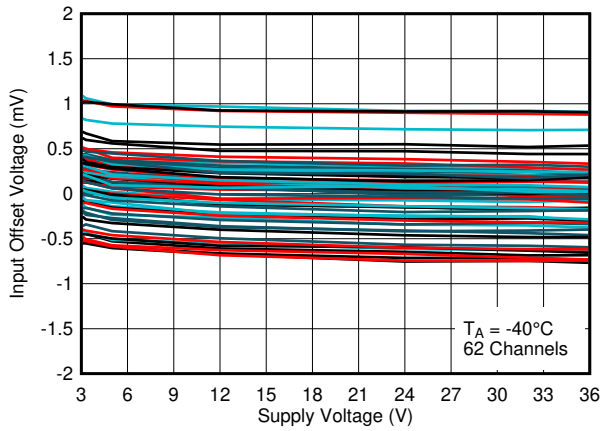


図 3-17. Input Offset Voltage vs. Supply Voltage at -40°C

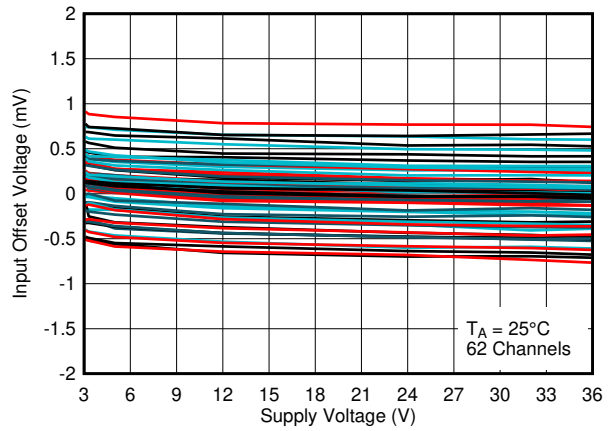


図 3-18. Input Offset Voltage vs. Supply Voltage at 25°C

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3.16 Typical Characteristics, LM2903B-Q1 Only (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

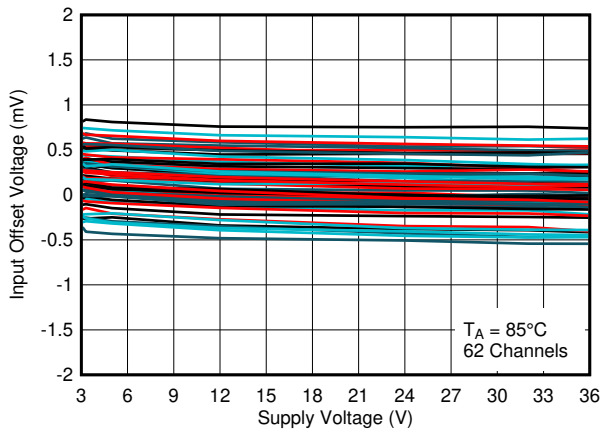


図 3-19. Input Offset Voltage vs. Supply Voltage at 85°C

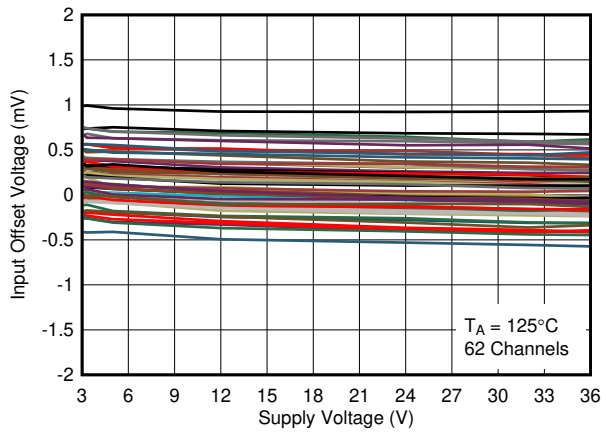


図 3-20. Input Offset Voltage vs. Supply Voltage at 125°C

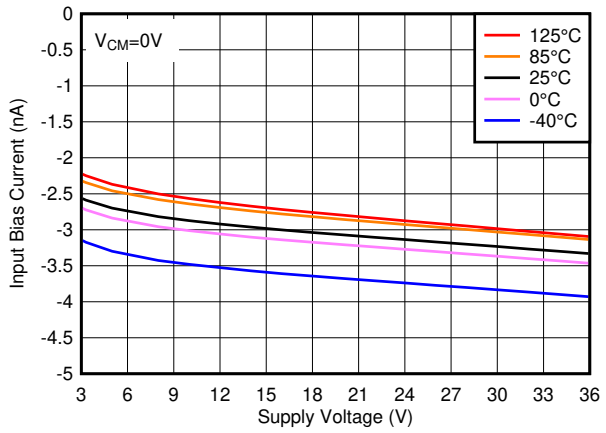


図 3-21. Input Bias Current vs. Supply Voltage

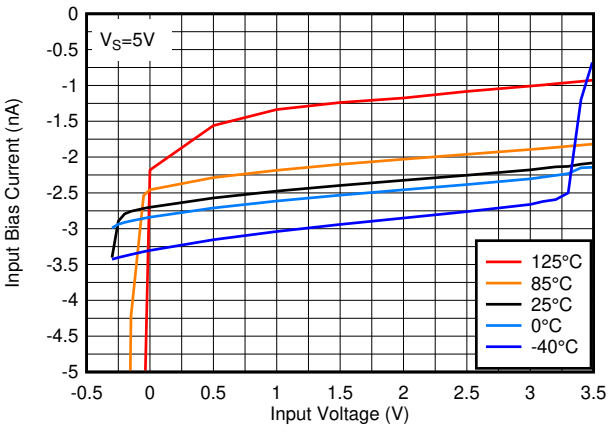


図 3-22. Input Bias Current vs. Input Voltage at 5V

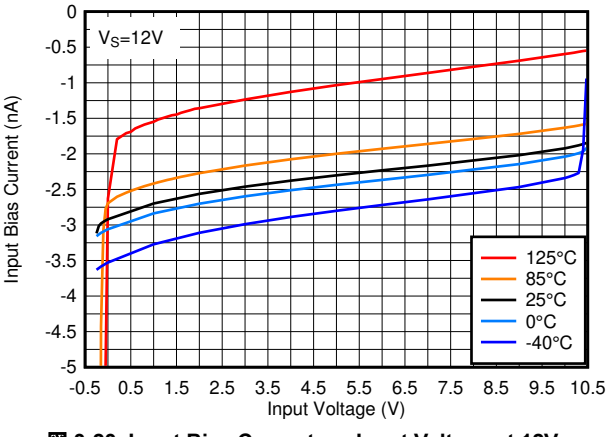


図 3-23. Input Bias Current vs. Input Voltage at 12V

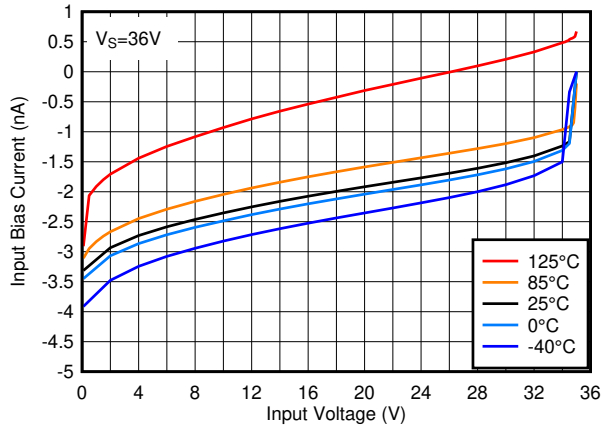


図 3-24. Input Bias Current vs. Input Voltage at 36V

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3.16 Typical Characteristics, LM2903B-Q1 Only (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

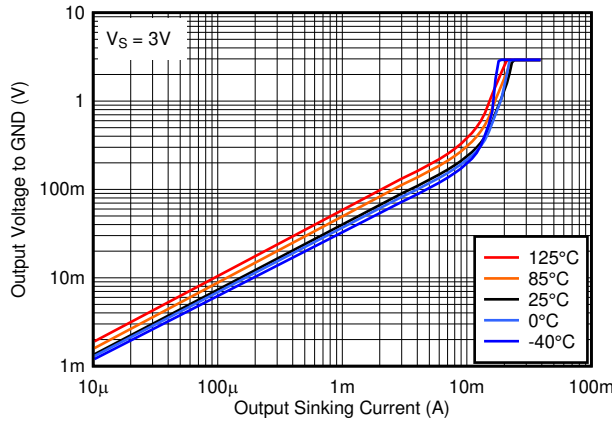


図 3-25. Output Low Voltage vs. Output Sinking Current at 3V

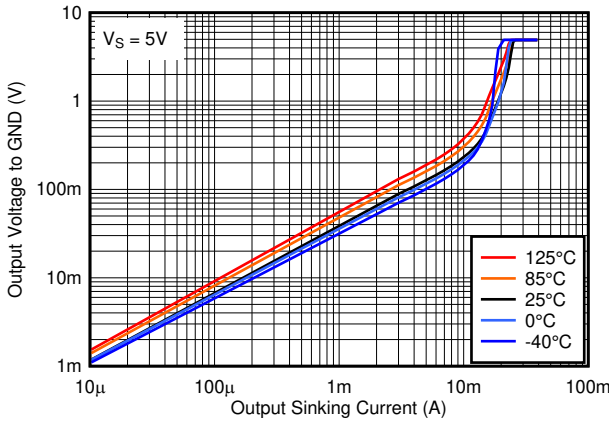


図 3-26. Output Low Voltage vs. Output Sinking Current at 5V

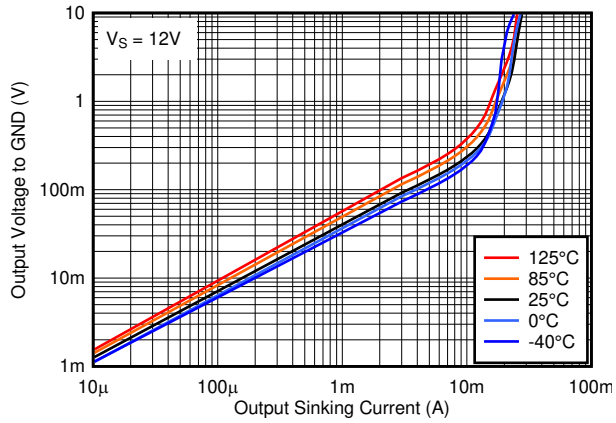


図 3-27. Output Low Voltage vs. Output Sinking Current at 12V

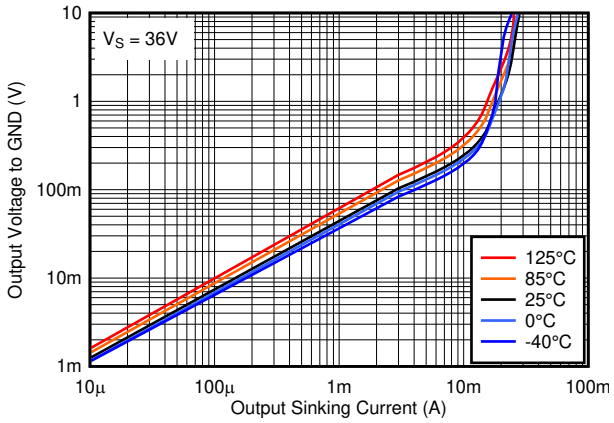


図 3-28. Output Low Voltage vs.Output Sinking Current at 36V

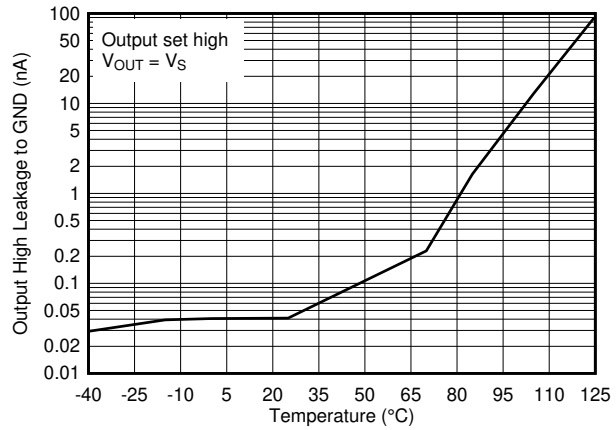


図 3-29. Output High Leakage Current vs.Temperature at 5V

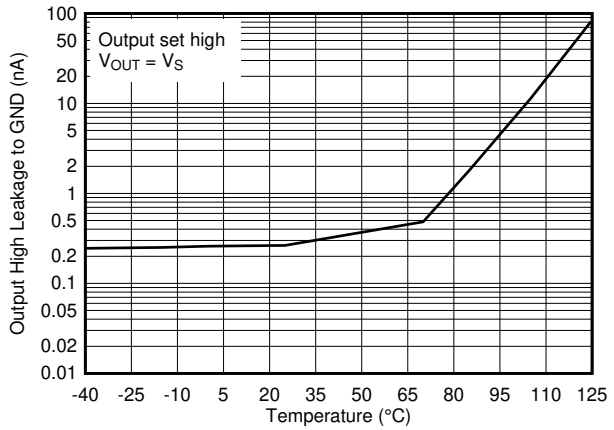


図 3-30. Output High Leakage Current vs. Temperature at 36V

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3.16 Typical Characteristics, LM2903B-Q1 Only (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

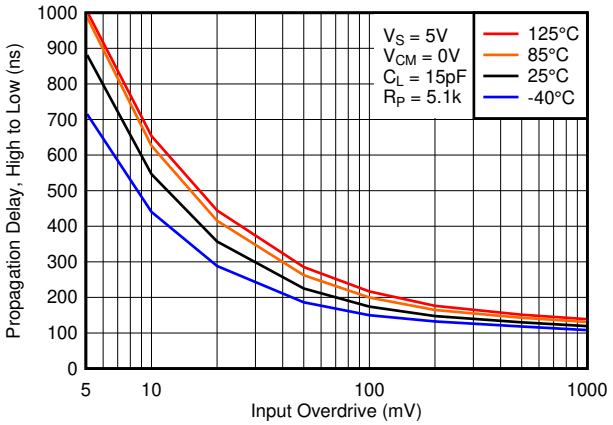


図 3-31. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

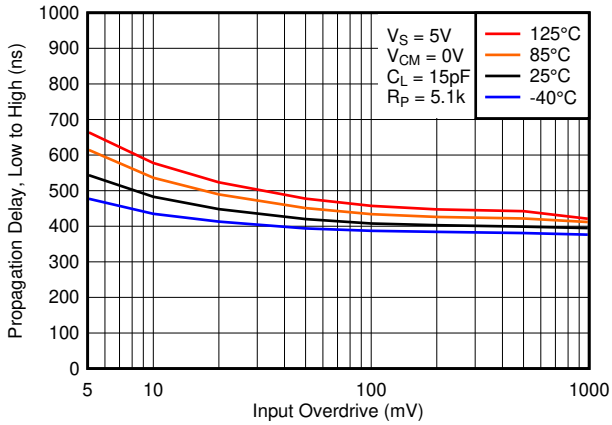


図 3-32. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

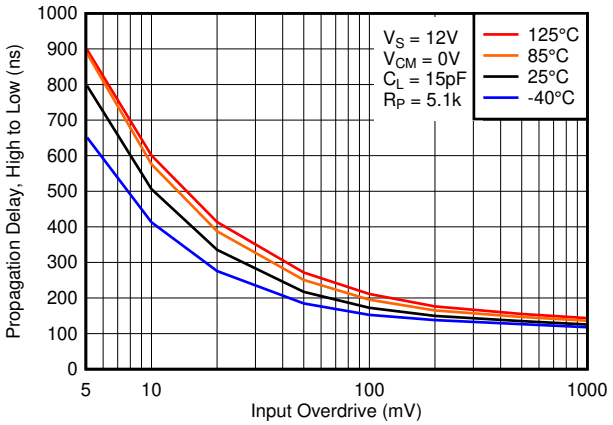


図 3-33. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

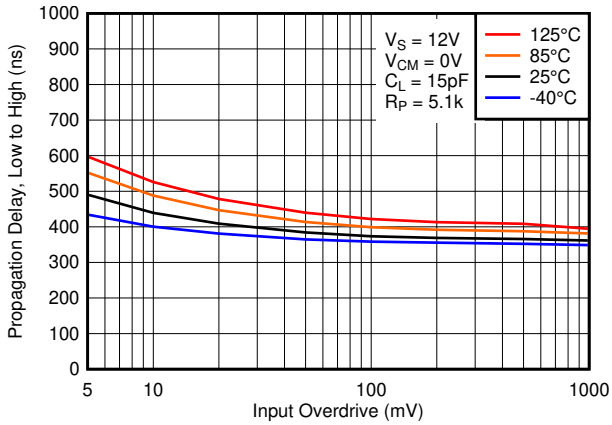


図 3-34. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

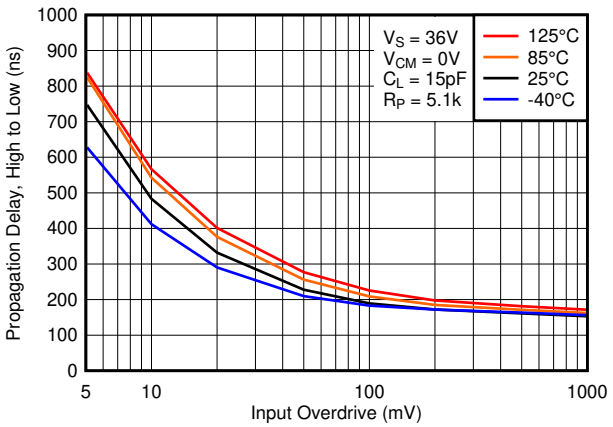


図 3-35. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

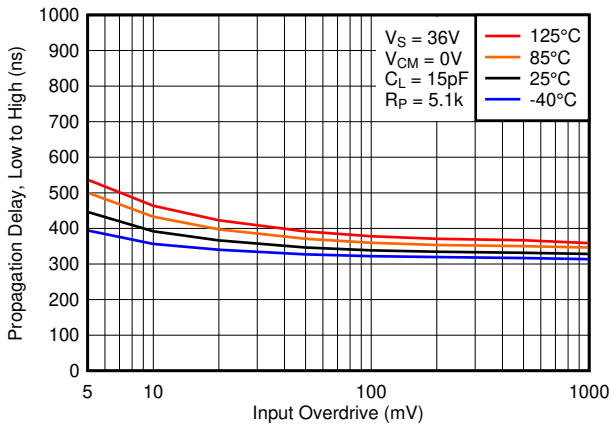


図 3-36. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

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3.16 Typical Characteristics, LM2903B-Q1 Only (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

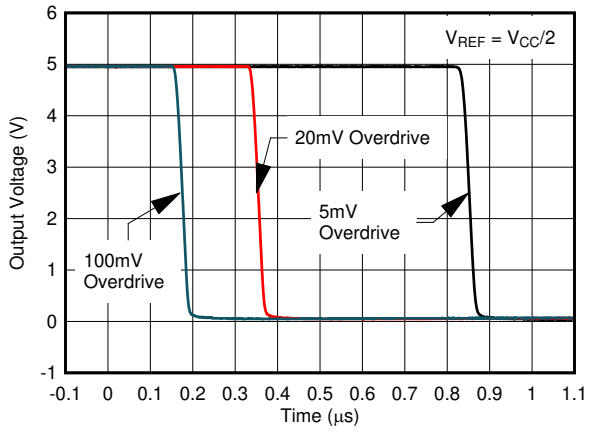


図 3-37. Response Time for Various Overdrives, High-to-Low Transition

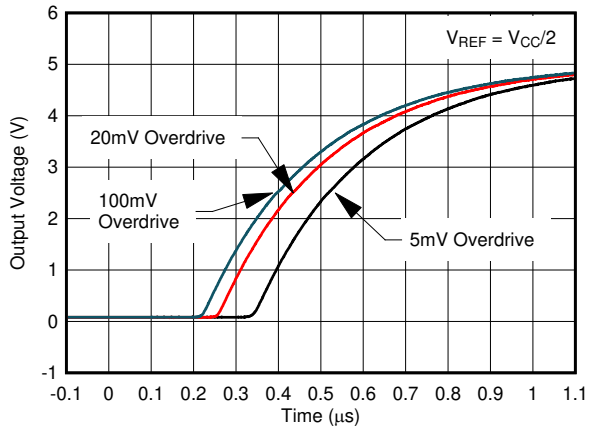


図 3-38. Response Time for Various Overdrives, Low-to-High Transition

4 Detailed Description

4.1 Overview

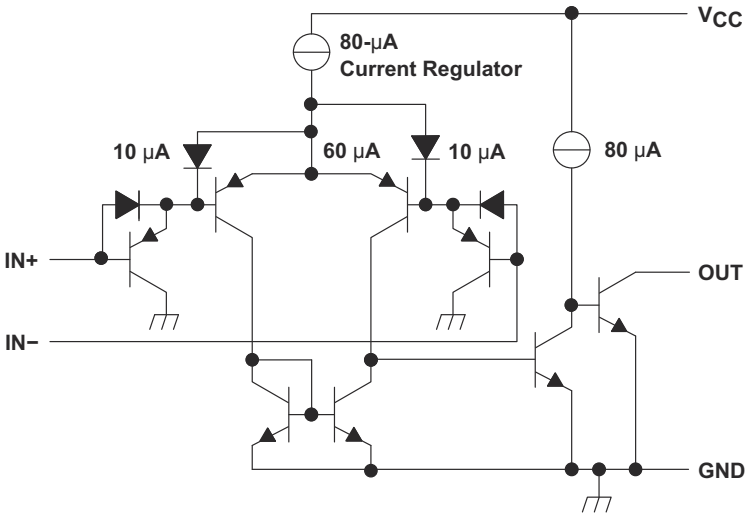
The LM2903-Q1 family is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's very wide supply voltages range (2 V to 36 V), low Iq and fast response.

This device is AEC-Q100 qualified and can operate over a wide temperature range of –40°C to 125°C (LM2903-Q1 and LM2903B-Q1) or –40°C to 150°C (LM2903E-Q1).

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note SNOAA35 for more information

4.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

図 4-1. Schematic (Each Comparator)

4.3 Feature Description

LM2903-Q1 family consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM2903-Q1 to accurately function from ground to V_{CC}–1.5V differential input. This is enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and will scale with the output current. Please see 図 3-3 in the *セクション 3.15* section for V_{OL} values with respect to the output current.

4.4 Device Functional Modes

4.4.1 Voltage Comparison

The LM2903-Q1 family operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

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5 Application and Implementation

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5.1 Application Information

LM2903-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2903Q1 optimal for level shifting to a higher or lower voltage.

5.2 Typical Application

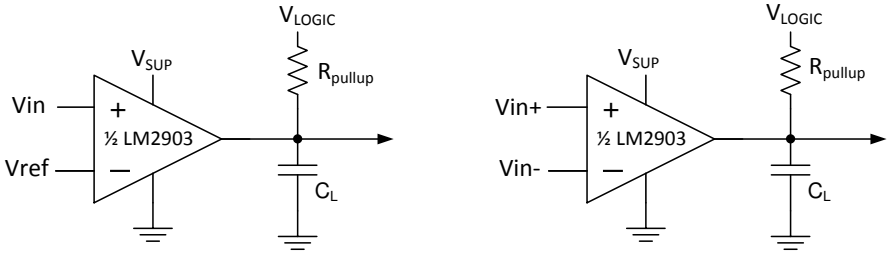


図 5-1. Single-ended and Differential Comparator Configurations

5.2.1 Design Requirements

For this design example, use the parameters listed in 表 5-1 as the input parameters.

表 5-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage	2 V to 36 V
Output Current (R_{PULLUP})	1 µA to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

5.2.2 Detailed Design Procedure

When using LM2903-Q1 family in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

5.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2.0 V. This limits the input voltage range to as high as V_{CC}– 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

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Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions

5.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 図 5-2 and 図 5-3 show positive and negative response times with respect to overdrive voltage.

5.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 図 3-5 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

5.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
  – R_{CE} can be determine by taking the slope of 図 3-5 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

5.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

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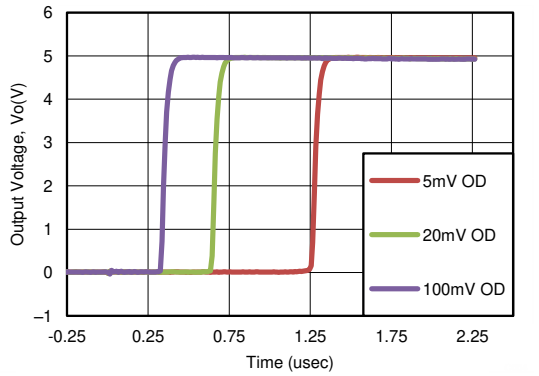


図 5-2. Response Time for Various Overdrives (Positive Transition)

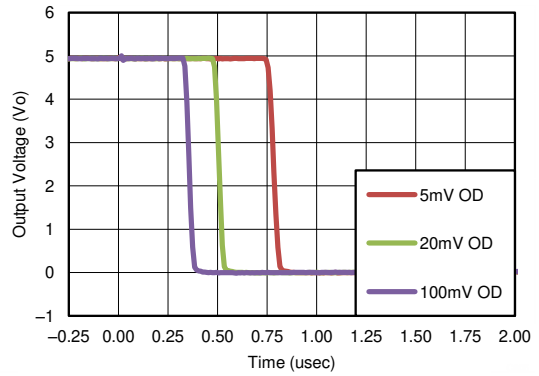


図 5-3. Response Time for Various Overdrives (Negative Transition)

5.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

5.4 Layout

5.4.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

5.4.2 Layout Example

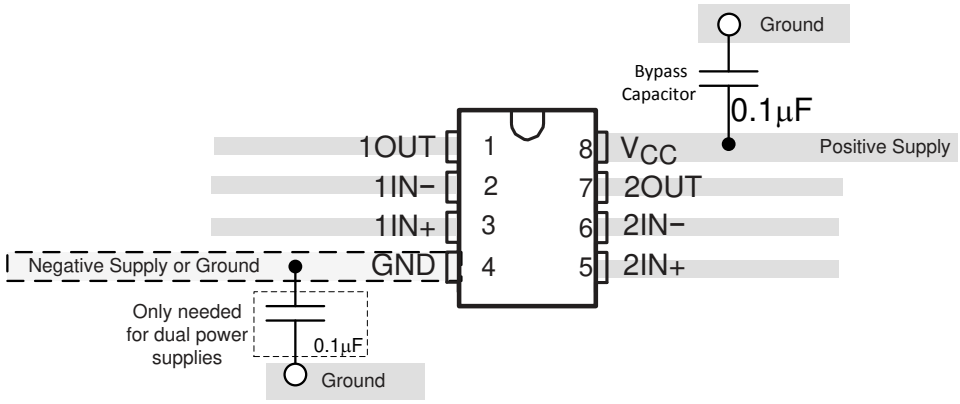


図 5-4. LM2903Q1 Layout Example

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

LM2903B-Q1 Functional Safety FIT Rate, FMD and Pin FMA - SLCA005

Application Design Guidelines for LM339, LM393, TL331 Family Comparators - SNOAA35

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 サポート・リソース

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6.4 Trademarks

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6.5 静電気放電に関する注意事項



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6.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	Samples
LM2903BHQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BHQ	Samples
LM2903BHQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BHQ	Samples
LM2903BHQPWRQ1	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BH	Samples
LM2903BQDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BQ	Samples
LM2903BQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	03BQ	Samples
LM2903BQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ	Samples
LM2903BQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BQ	Samples
LM2903BRQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BRQ	Samples
LM2903BRQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BRQ	Samples
LM2903BRQPWRQ1	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BR	Samples
LM2903BTQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BTQ	Samples
LM2903BTQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903BTQ	Samples
LM2903BTQPWRQ1	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903BT	Samples
LM2903BWDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 125	3BWQ	Samples
LM2903EPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2903Q0	Samples
LM2903QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	KACQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	Samples
LM2903VQDRG4Q1	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	
LM2903VQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	Samples
LM2903VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	Samples
LM2903VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM2903-Q1, LM2903B-Q1 :

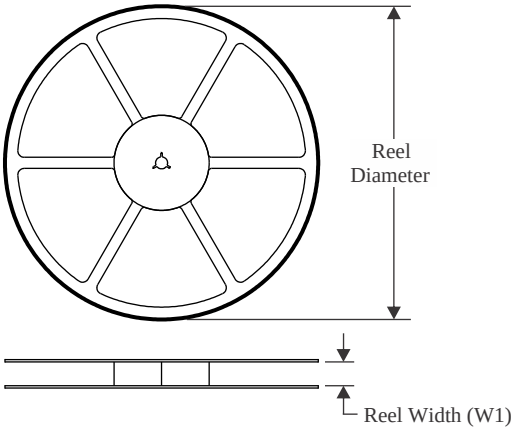
- Catalog : LM2903, LM2903B

NOTE: Qualified Version Definitions:

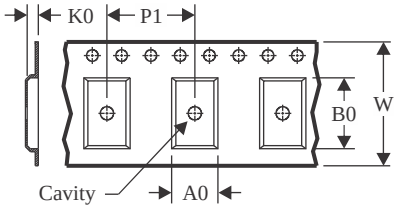
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

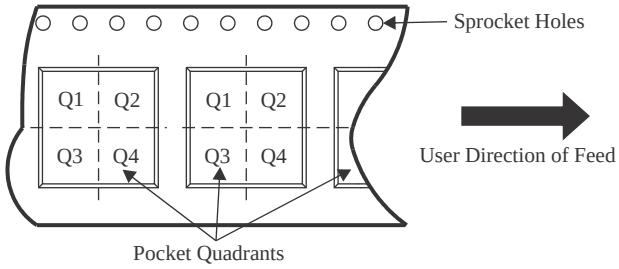


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

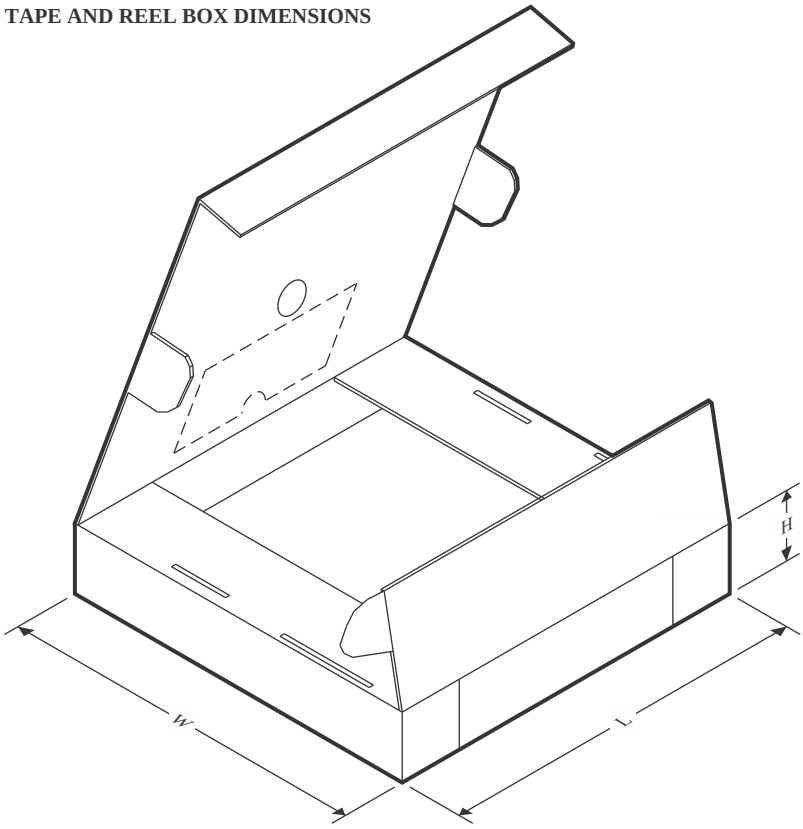


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903AVQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BHQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BHQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BHQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2903BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BRQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BRQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903BRQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BTQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BTQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BTQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BWDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LM2903EPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

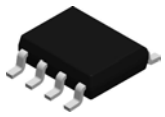
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903AVQDRG4Q1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903AVQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903BHQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BHQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2903BHQPWRQ1	TSSOP	PW	8	3000	356.0	356.0	35.0
LM2903BQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2903BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
LM2903BQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903BQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903BRQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BRQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2903BRQPWRQ1	TSSOP	PW	8	3000	356.0	356.0	35.0
LM2903BTQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BTQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903BTQPWRQ1	TSSOP	PW	8	3000	356.0	356.0	35.0
LM2903BWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
LM2903EPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903QDRG4Q1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903QPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQDRG4Q1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903VQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

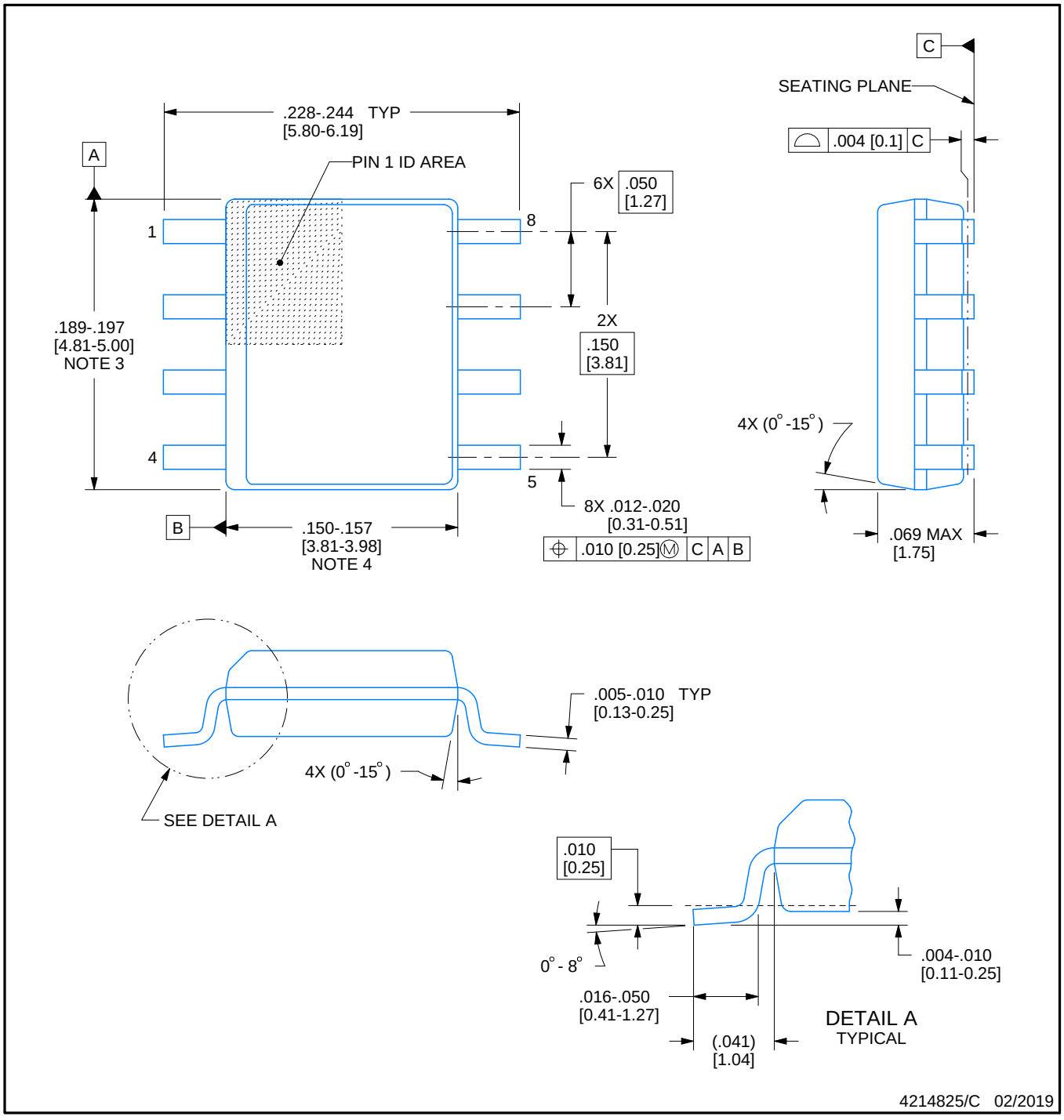


PACKAGE OUTLINE

D0008A

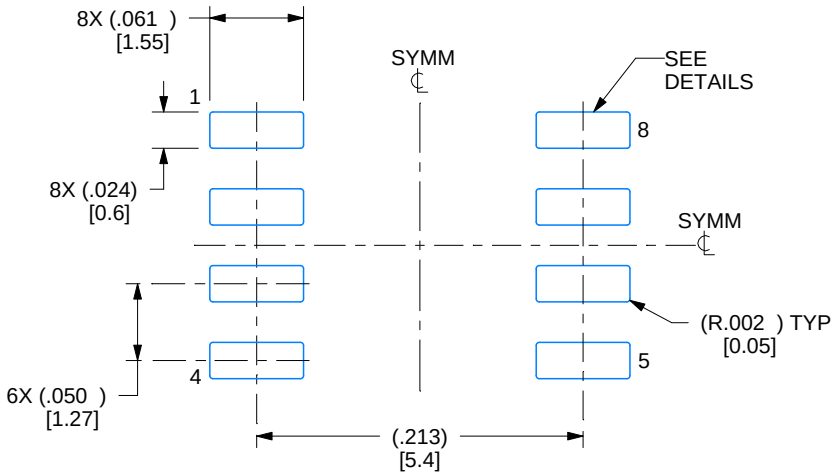
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

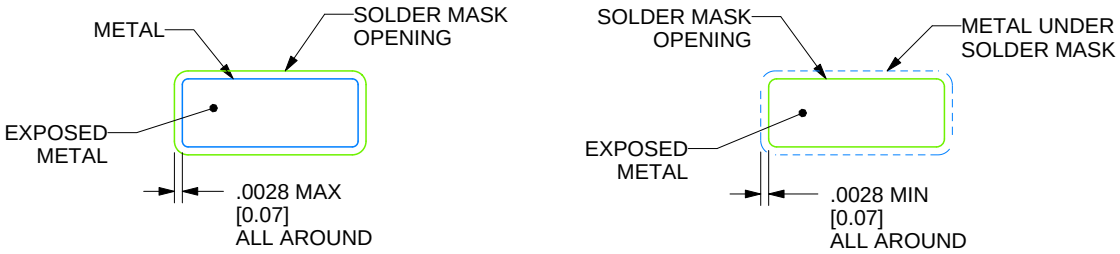


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

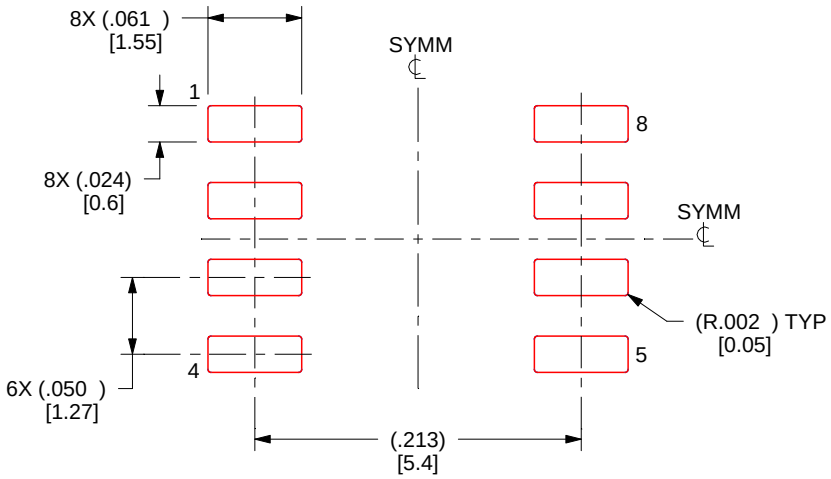
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



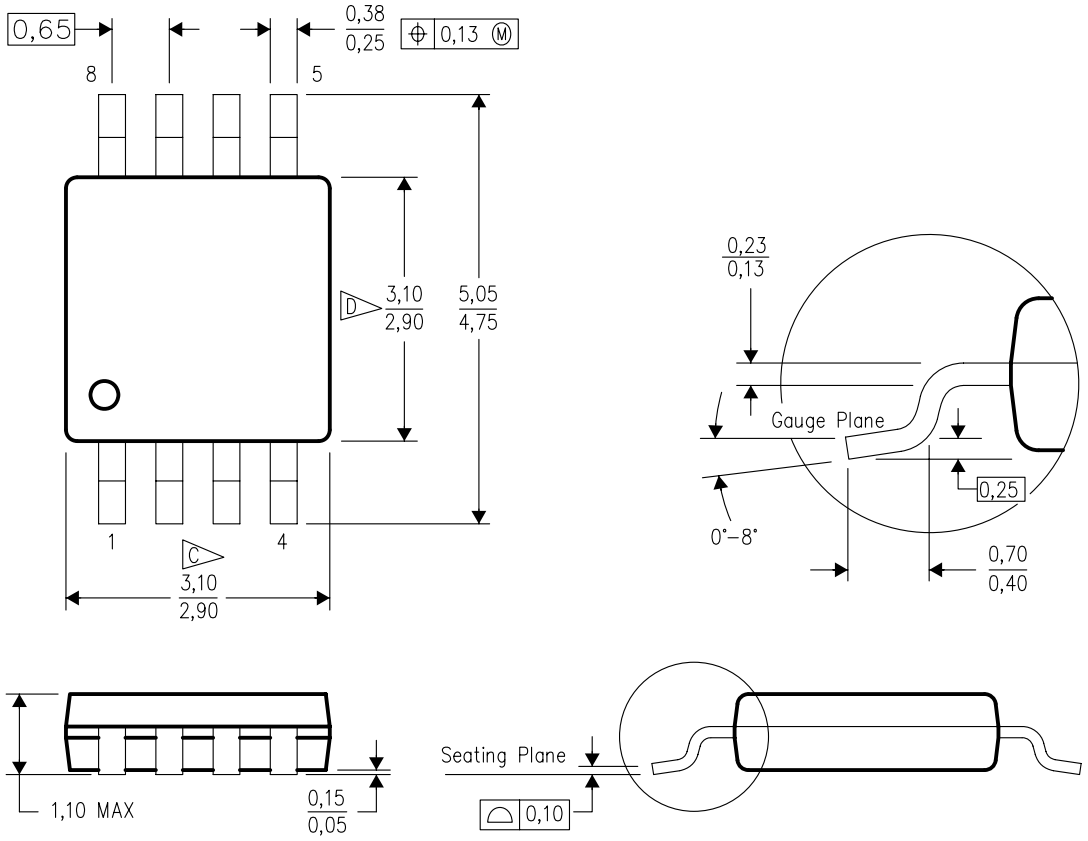
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

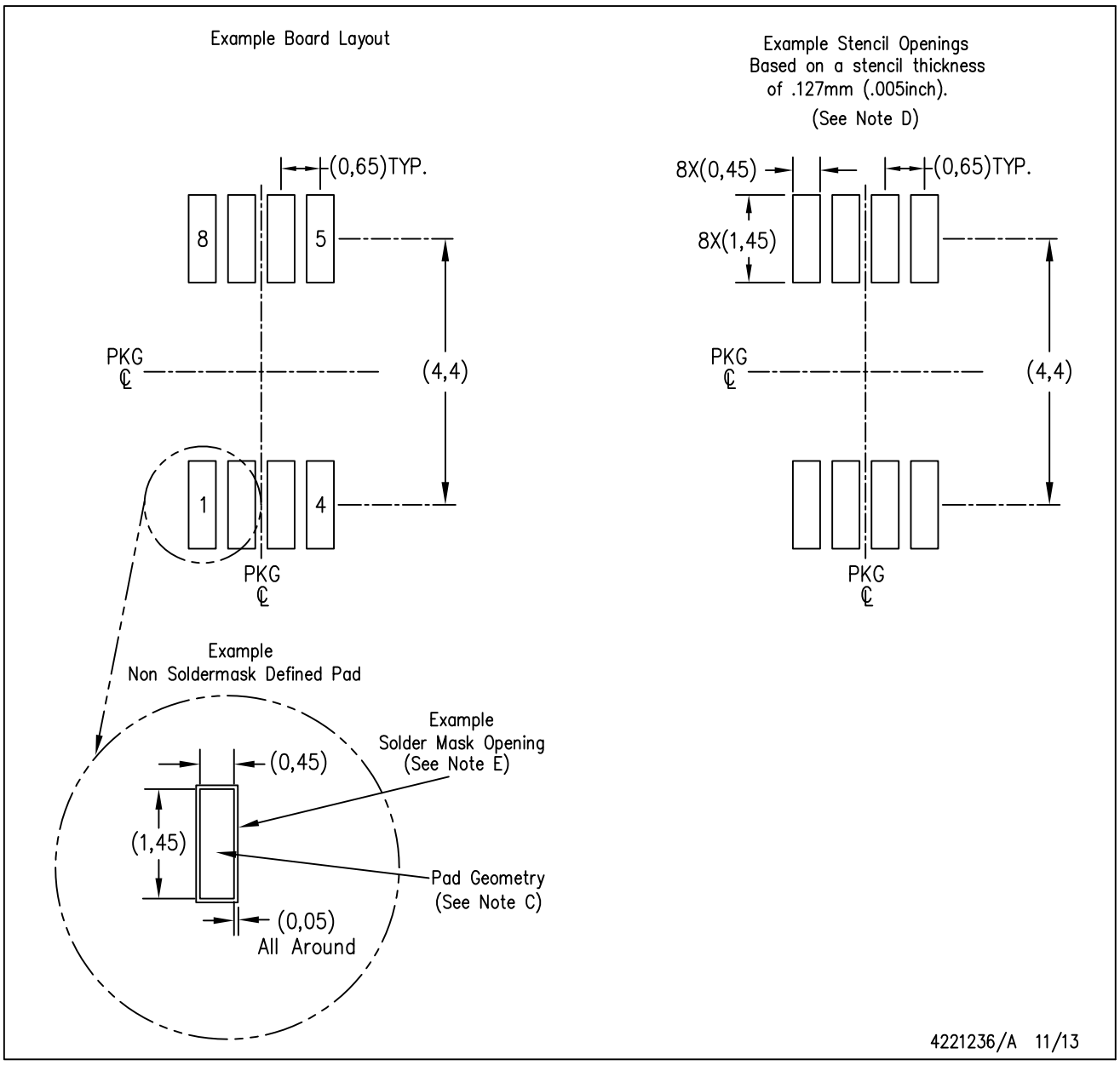
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

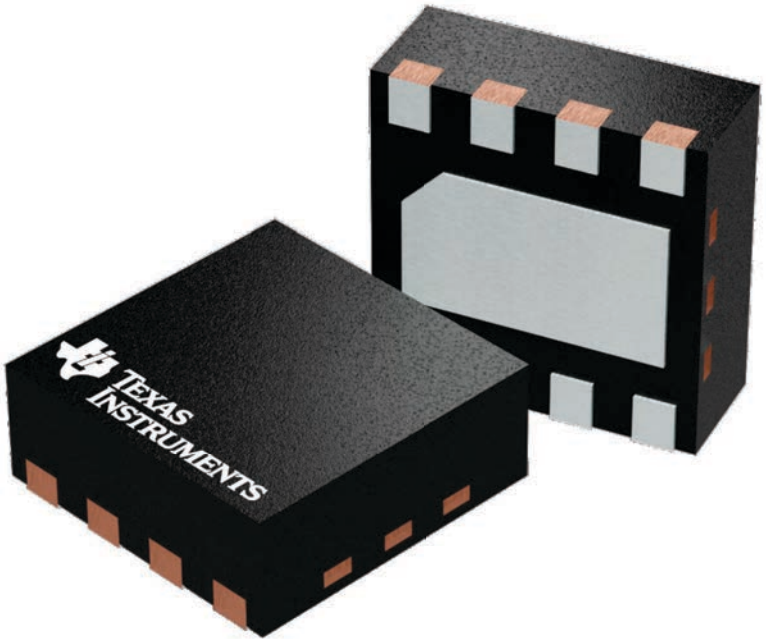
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



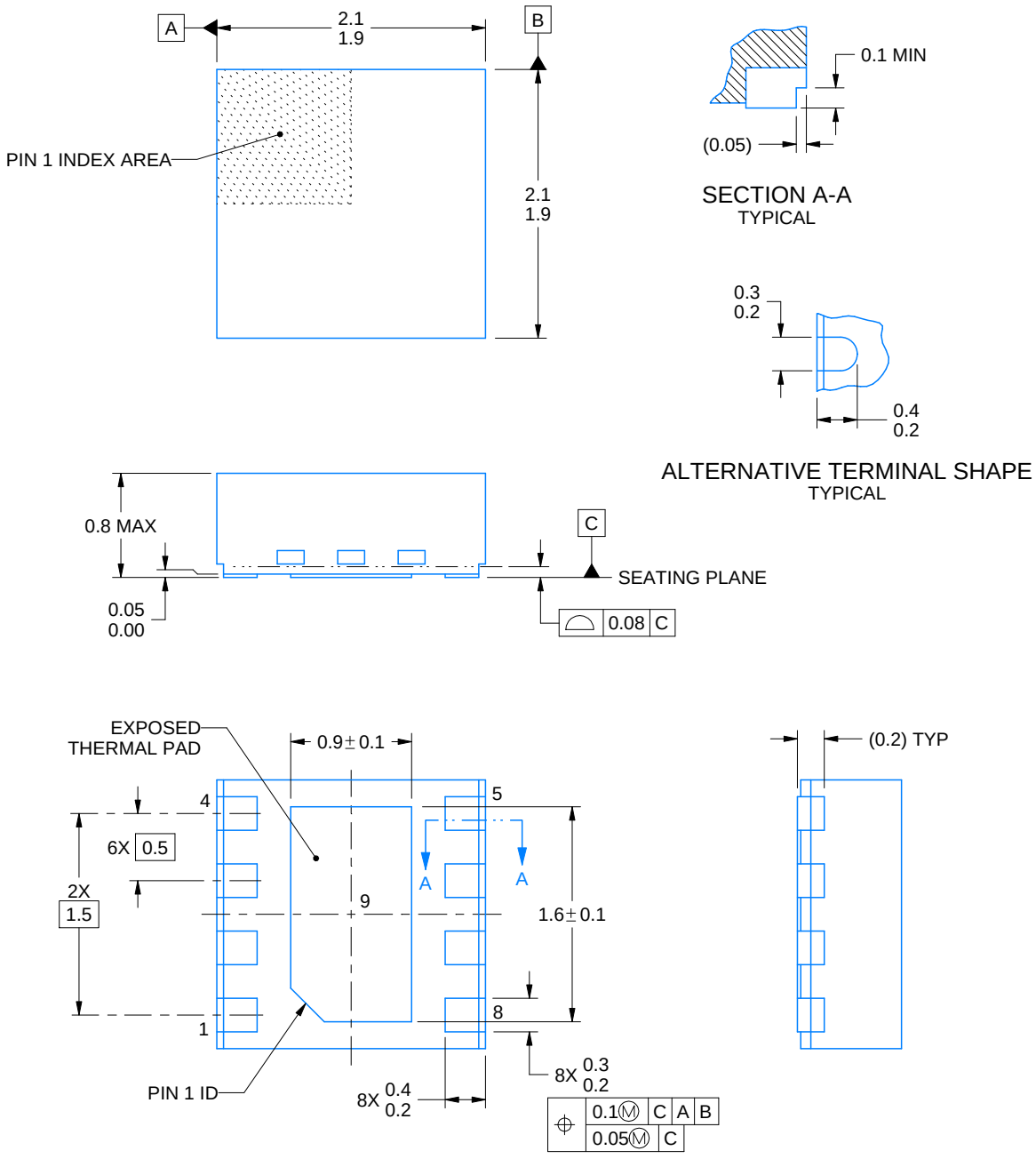
4224783/A

PACKAGE OUTLINE

DSG0008B

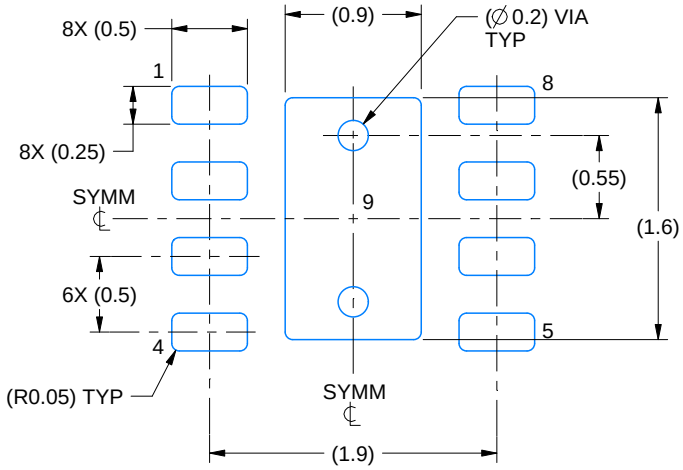
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

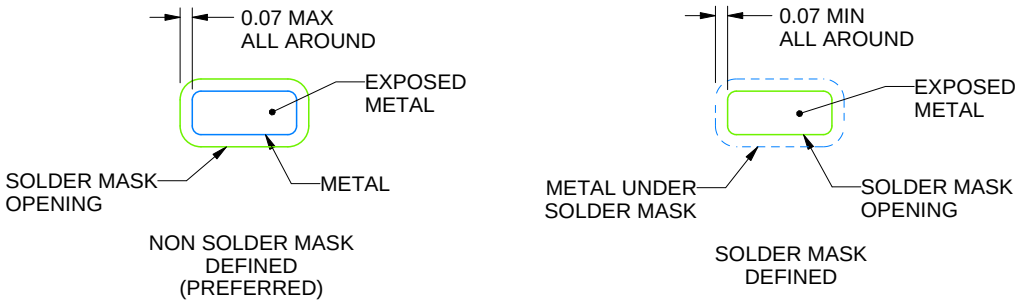


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

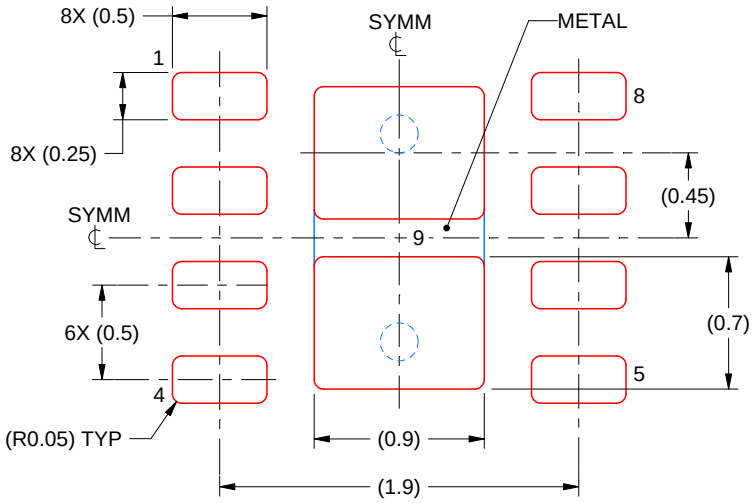
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

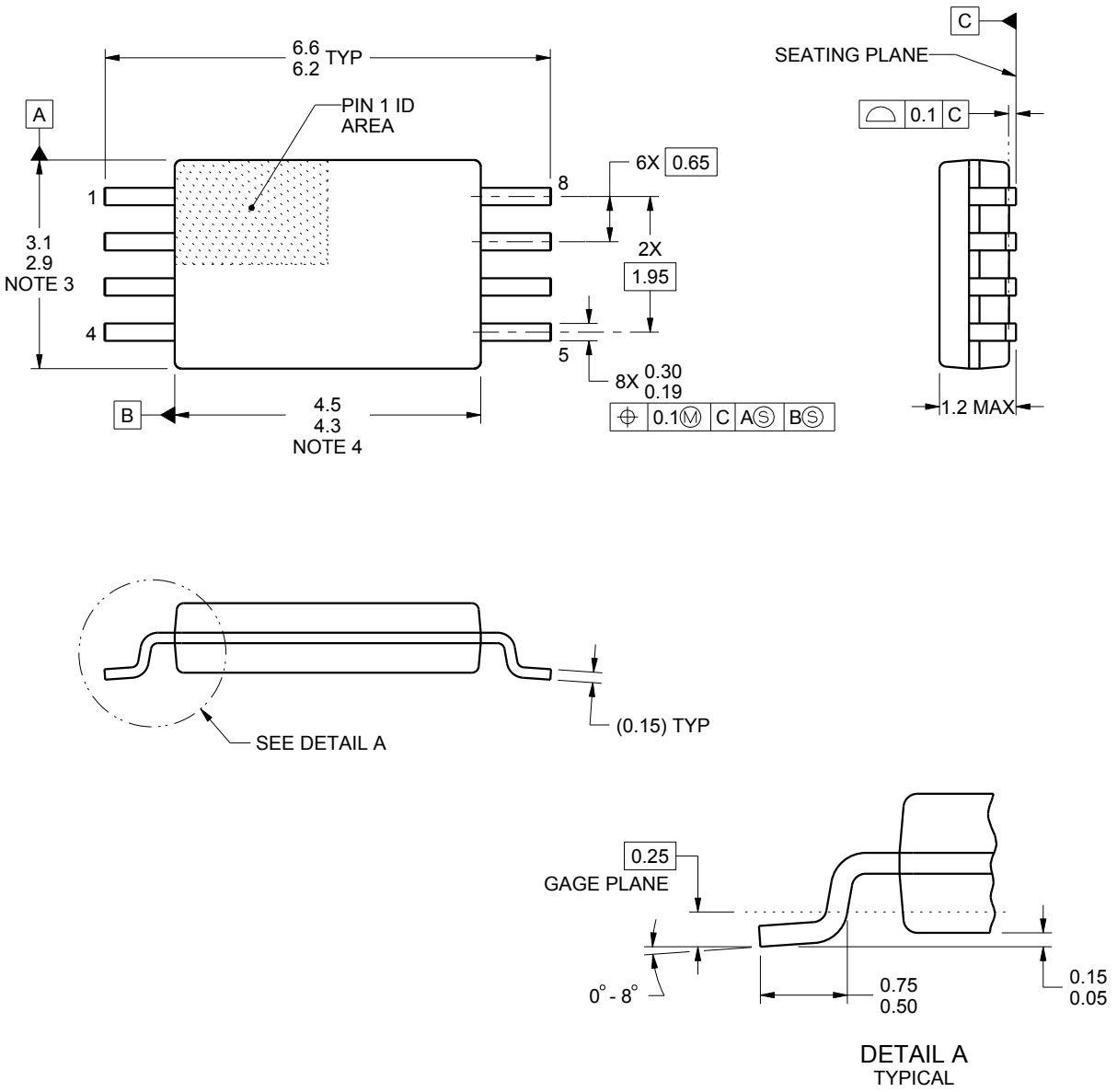
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

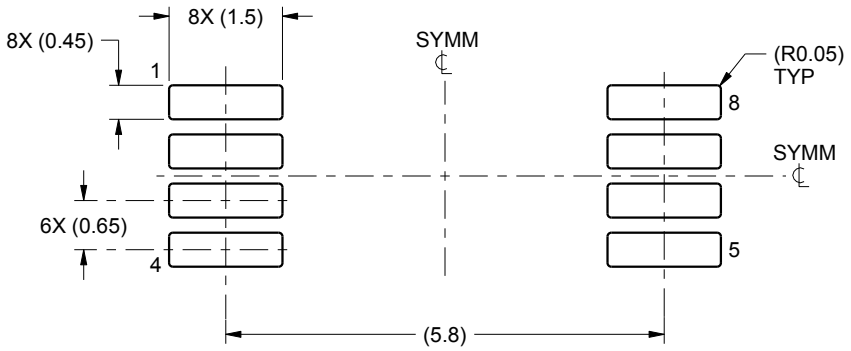
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

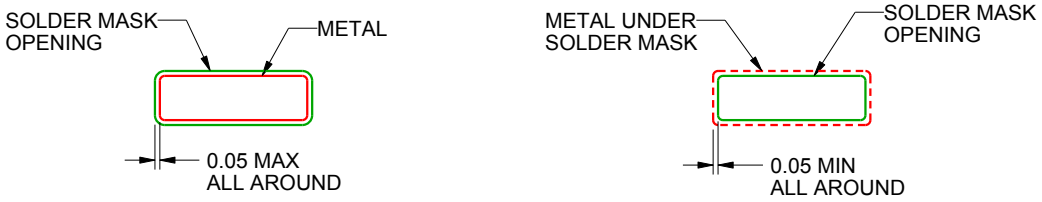


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

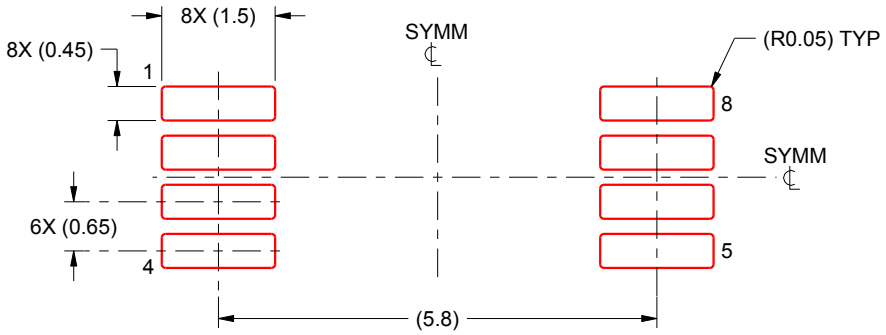


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

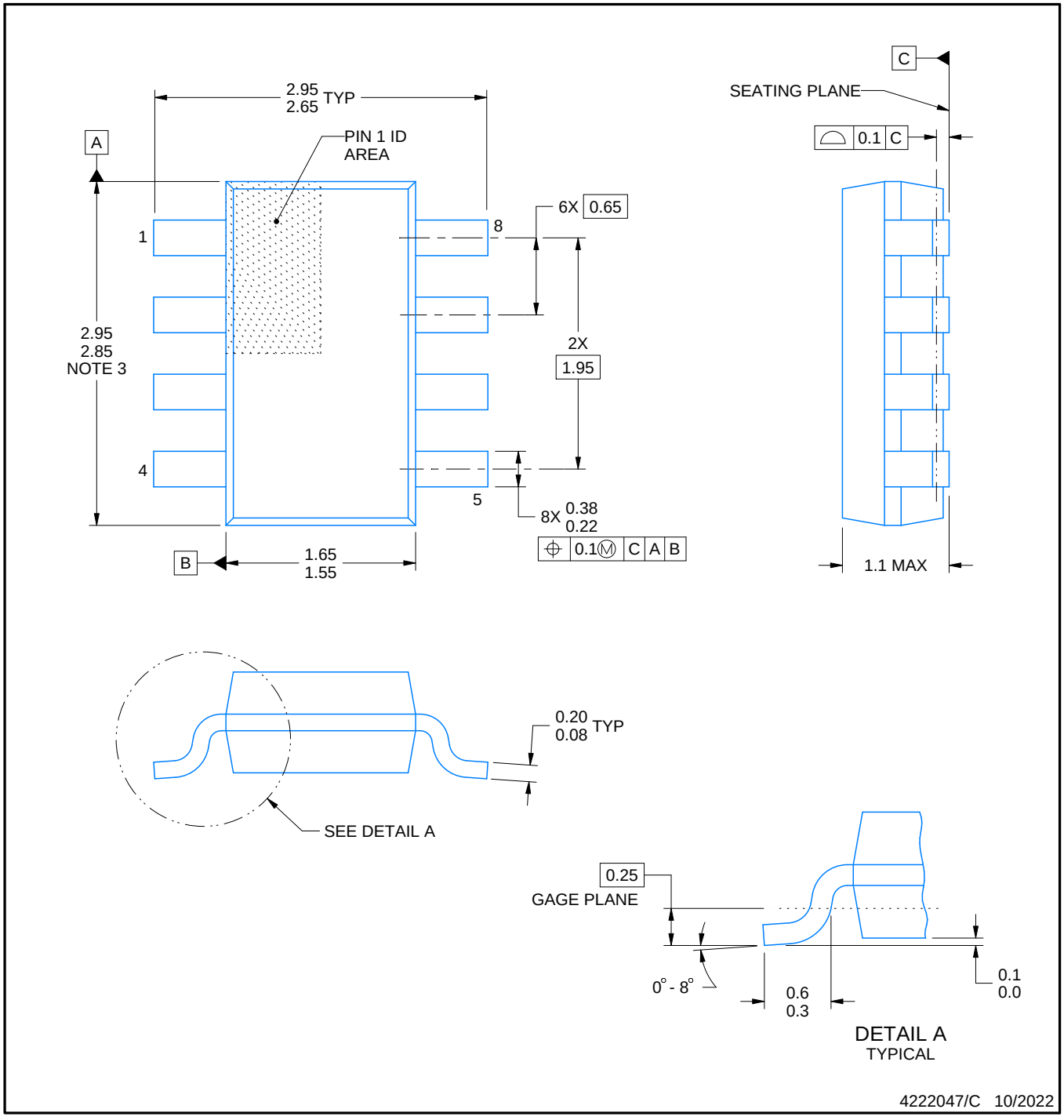
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

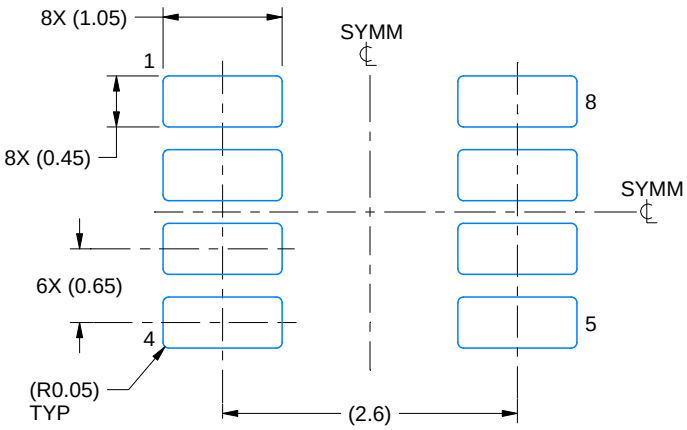
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

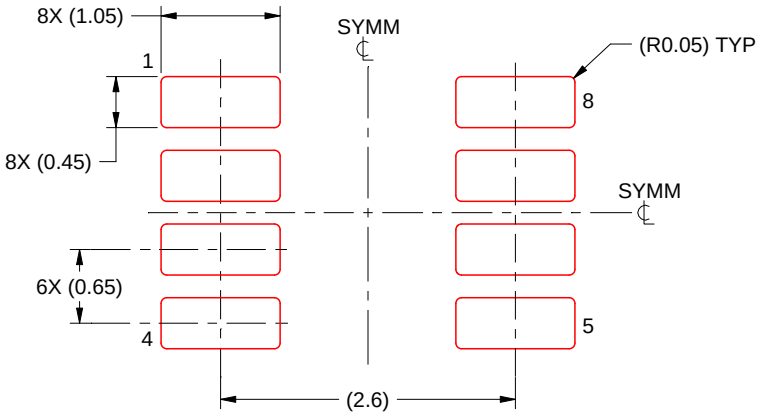
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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