

TPS3813-Q1 ウィンドウ・ウォッチドッグ搭載、車載用プロセッサ監視回路

1 特長

- 車載アプリケーションに対応
- 下記内容で AEC-Q100 認定済み:
 - デバイス温度グレード 1: -40°C ~ +125°C の動作時周囲温度範囲
 - デバイス HBM 分類レベル 2
 - デバイス CDM 分類レベル C4B
- 遅延とウィンドウ比率をプログラム可能なウィンドウ・ウォッチドッグ
- 6 ピン SOT-23 パッケージ
- 消費電流 9µA (標準値)
- 25ms の固定遅延時間を持つパワー・オン・リセット・ジェネレータ
- 高精度の電源電圧モニタ (V_{IT}): 2.5V、3V、3.3V、5V
- オープン・ドレイン・リセット出力

2 アプリケーション

- オンボード・チャージャ (OBC) およびワイヤレス・チャージャ
- ドライバー監視
- デジタル・コックピット処理装置
- ADAS ドメイン・コントローラ
- 車載テレマティクス制御ユニット

3 概要

TPS3813-Q1 監視回路は、主に DSP およびプロセッサ・ベースのシステムにおいて、回路の初期化とタイミングの監視を行います。

起動中に電源電圧 (V_{DD}) が 1.1V よりも高くなると、 $\overline{\text{RESET}}$ ピンがアサートされます。その後、監視回路は

V_{DD} を監視し、 V_{DD} がスレッシュホールド電圧 (V_{IT}) よりも低く保たれている間、 $\overline{\text{RESET}}$ ピンをアクティブに維持します。

内蔵のタイマは、システムが確実に正しくリセットするように、出力が非アクティブ状態 (HIGH) に戻るのを遅らせます。この遅延時間 ($t_d = 25\text{ms}$ (標準値)) は、 V_{DD} がスレッシュホールド電圧 (V_{IT}) を上回ったときにカウントを開始します。電源電圧がスレッシュホールド電圧 (V_{IT}) を下回ると、出力は再びアクティブ (LOW) になります。外付け部品は不要です。このファミリの全デバイスには、内蔵分圧器で設定される固定検出スレッシュホールド電圧 (V_{IT}) があります。

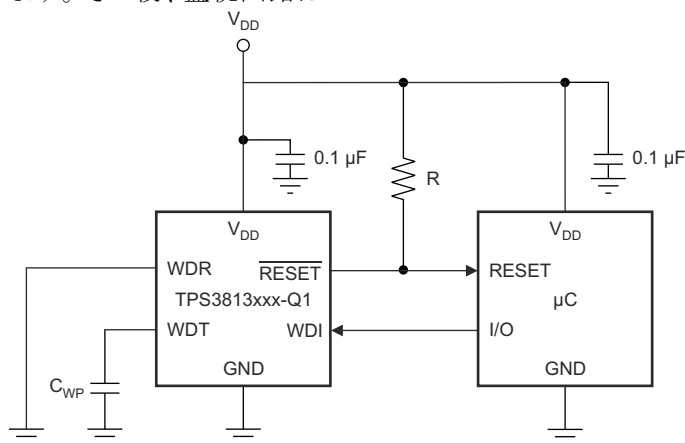
安全が要求されるアプリケーション向けに、TPS3813-Q1 ファミリのデバイスは、遅延とウィンドウ比率をプログラム可能なウィンドウ・ウォッチドッグを内蔵しています。ウォッチドッグのタイムアウトの上限は、WDT ピンを GND または V_{DD} に接続するか、外付けコンデンサを使用することで設定できます。下限、すなわちウィンドウ比率は、WDR ピンを GND または V_{DD} に接続することで設定されます。ウォッチドッグが正常に対応できなかった場合、 $\overline{\text{RESET}}$ ピンは、マイクロコントローラにリセットをアサートします。

この製品ファミリは、2.5V、3V、3.3V、5V 電源電圧用に設計されています。これらのデバイスは 6 ピンの SOT-23 パッケージで供給されます。これらのデバイスは、-40°C ~ 125°C の温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TPS3813K33-Q1	SOT-23 (6)	2.90mm × 1.60mm
TPS3813I50-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的な動作回路



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (October 2019) to Revision H (October 2021)	Page
• Changed t_w parameter name to t_{GL_VIT} in 7.6 <i>Timing Requirements</i> section and added <i>Glitch immunity V_{IT}</i> in parameter definition.	6
• Added timing diagram.....	7
• Added Input Voltage (VDD), VDD Hysteresis, and VDD Glitch Immunity sections into datasheet.....	10

Changes from Revision F (December 2016) to Revision G (October 2019)	Page
• Updated text for device conditions on start-up.	9
• Added information to further clarify shaded areas in the Upper and Lower Boundary Visualization.....	11

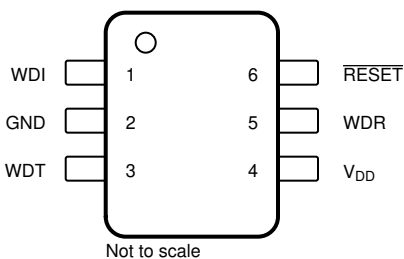
Changes from Revision E (October 2016) to Revision F (December 2016)	Page
• Changed the part numbers in the <i>Electrical Characteristics</i> table and deleted references to TPS3813-Q1J25 and TPS3813-Q1L30.....	6

Changes from Revision D (June 2015) to Revision E (October 2016)	Page
• Added + 1 back to the $t_{window,typ}$ equation in the <i>Programming Window-Watchdog Using an External Capacitor</i> section.....	14

Changes from Revision C (September 2013) to Revision D (June 2015)	Page
• データシートから TPS38131J25-Q1 および TPS3813L30-Q1 デバイスを削除.....	1
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• Deleted the <i>Dissipation Ratings</i> table	6
• Changed the voltage on the V_{DD} pin from 0.6 V to 1.1 V in the <i>Timing Diagram</i> figure.....	12

Changes from Revision B (May 2012) to Revision C (August 2013)	Page
• Deleted banner stating that TPS3813K33-Q1 is <i>Not Recommended for New Designs</i>	8
Changes from Revision A (November 2008) to Revision B (April 2012)	Page
• Changed value from 47 pF to 155 pF.....	14

5 Pin Configuration and Functions



**图 5-1. DBV Package
6-Pin SOT-23
Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	WDI	I	Watchdog timer input. This input must be driven at all times and not left floating.
2	GND	I	Ground
3	WDT	I	Programmable watchdog delay input
4	V _{DD}	I	Supply voltage and supervising input
5	WDR	I	Selectable watchdog window ratio input. This input must be tied to V _{DD} or GND and not left floating.
6	RESET	O	Open-drain reset output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage ⁽²⁾		7	V
	RESET	−0.3	V _{DD} + 0.3	
	All other pins ⁽²⁾	−0.3	7	
I _{OL}	Maximum low output current		5	mA
I _{OH}	Maximum high output current		−5	mA
I _{IK}	Input clamp current (V _I < 0 or V _I > V _{DD})		±20	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{DD})		±20	mA
	Continuous total power dissipation	See セクション 6.4		
T _A	Operating free-air temperature	−40	125	°C
	Soldering temperature		260°C	
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±500	
	Corner pins (1, 3, 4, and 6)	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

at specified temperature range

		MIN	MAX	UNIT
V _{DD}	Supply voltage	2	6	V
V _I	Input voltage	0	V _{DD} + 0.3	V
V _{IH}	High-level input voltage	0.7 × V _{DD}		V
V _{IL}	Low-level input voltage		0.3 × V _{DD}	V
Δt/ΔV	Input transition rise and fall rate		100	ns/V
t _w	Pulse width of WDI trigger pulse	50		ns
T _A	Operating free-air temperature range	−40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3813-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	202.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	164.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	54.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	44.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage		V _{DD} = 2 V to 6 V, I _{OL} = 500 μA			0.2	V
			V _{DD} = 3.3 V I _{OL} = 2 mA			0.4	
			V _{DD} = 6 V, I _{OL} = 4 mA			0.4	
Power up reset voltage ⁽¹⁾			V _{DD} ≥ 1.1 V, I _{OL} = 50 μA			0.2	V
V _{IT}	Negative-going input threshold voltage ⁽²⁾	TPS3813K33-Q1		2.87	2.93	3	V
		TPS3813I50-Q1		4.45	4.55	4.65	
V _{HYS}	Hysteresis	TPS3813K33-Q1			40		mV
		TPS3813I50-Q1			60		
I _{IH}	High-level input current	WDI, WDR	WDI = V _{DD} = 6 V, WDR = V _{DD} = 6 V	−125		125	nA
		WDT	WDT = V _{DD} = 6 V, V _{DD} > V _{IT} , RESET = High	−125		125	
I _{IL}	Low-level input current	WDI, WDR	WDI = 0 V, WDR = 0 V, V _{DD} = 6 V	−125		125	
		WDT	WDT = 0 V, V _{DD} > V _{IT} , RESET = High	−125		125	
I _{OH}	High-level output current	V _{DD} = V _{IT} + 0.2 V, V _{OH} = V _{DD}				25	nA
I _{DD}	Supply current	V _{DD} = 2 V output unconnected			9	13	μA
		V _{DD} = 5 V output unconnected			20	25	
C _i	Input capacitance	V _I = 0 V to V _{DD}			5		pF

(1) The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.

6.6 Timing Requirements

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to +125°C.

		MIN	TYP	MAX	UNIT
t _{GL_VIT}	Glitch immunity V _{IT} (Pulse width at V _{DD})	V _{DD} = V _{IT} + 0.2 V, V _{DD} = V _{IT} – 0.2 V		3	μs

6.7 Switching Characteristics

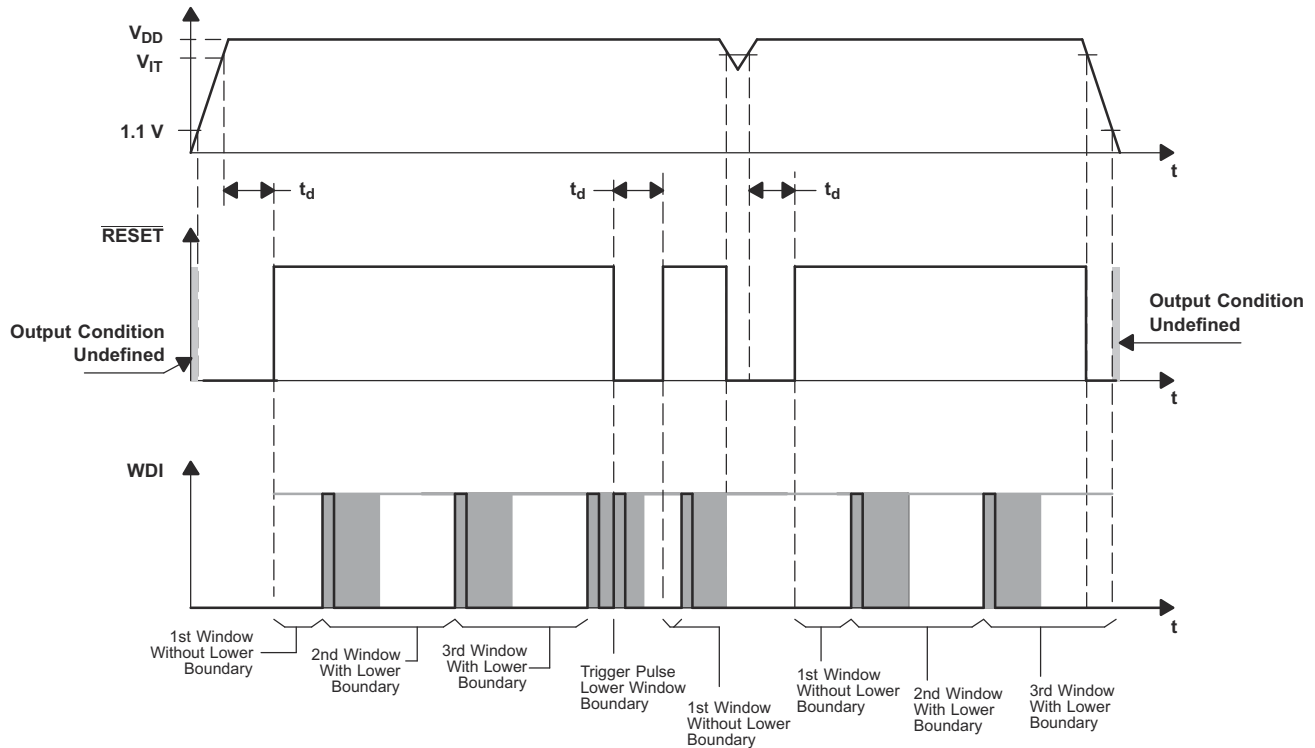
$R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _d	Delay time		V _{DD} ≥ V _{IT} + 0.2 V (see FIG 7-3)	20	25	30	ms
t _{t(out)}	Watchdog time-out	Upper limit	WDT = 0 V	0.2	0.25	0.3	s
			WDT = V _{DD}	2	2.5	3	
			WDT = programmable ⁽¹⁾	See ⁽²⁾			ms
Watchdog window ratio			WDR = 0 V, WDT = 0 V	1:31.8			
			WDR = 0 V, WDT = V _{DD}	1:32			
			WDR = 0 V, WDT = programmable	1:25.8			
			WDR = V _{DD} , WDT = 0 V	1:124.9			
			WDR = V _{DD} , WDT = V _{DD}	1:127.7			
			WDR = V _{DD} , WDT = programmable	1:64.5			
t _{PHL}	Propagation (delay) time, high-to-low-level output	V _{DD} to RESET delay	V _{IL} = V _{IT} – 0.2 V, V _{IH} = V _{IT} + 0.2 V		30	50	μs

(1) $155\text{ pF} < C_{(ext)} < 63\text{ nF}$

(2) $(C_{(ext)} / 15.55\text{ pF} + 1) \times 6.25\text{ ms}$

6.8 Timing Diagrams



6-1. Timing Diagram

6.9 Typical Characteristics

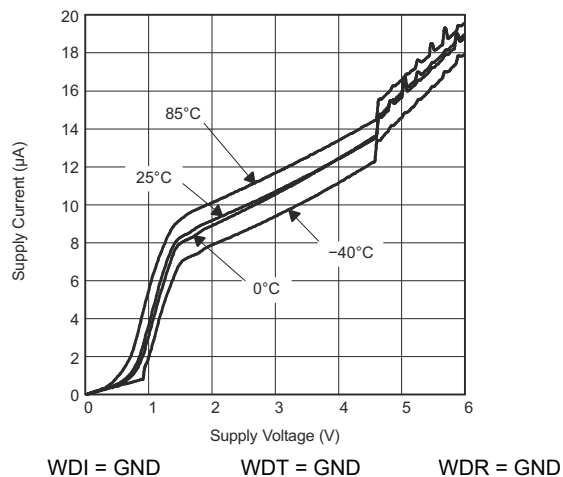


Figure 6-2. Supply Current vs Supply Voltage

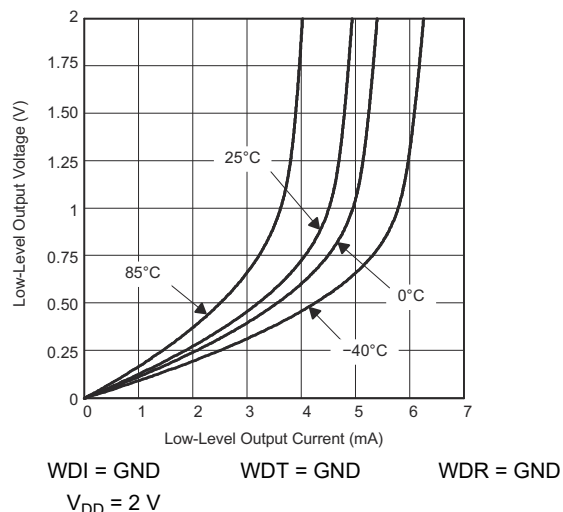


Figure 6-3. Low-Level Output Voltage vs Low-Level Output Current

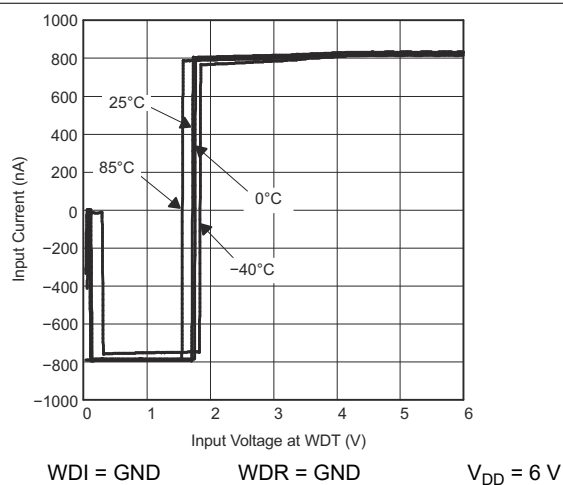


Figure 6-4. Input Current vs Input Voltage at WDT

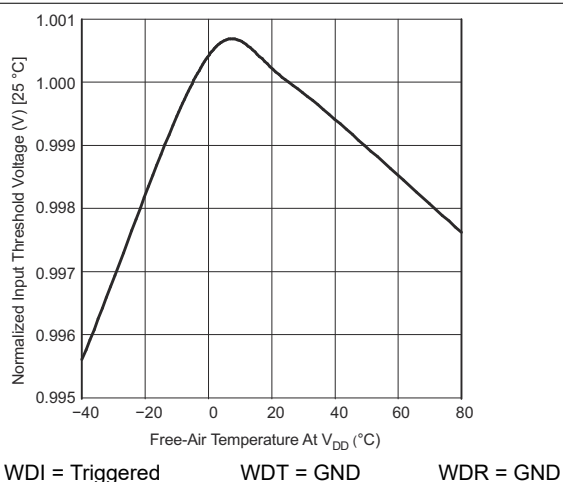


Figure 6-5. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

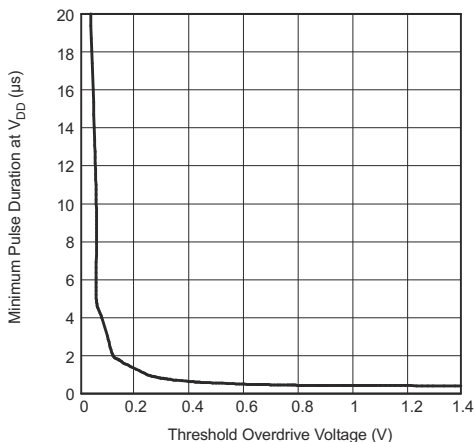


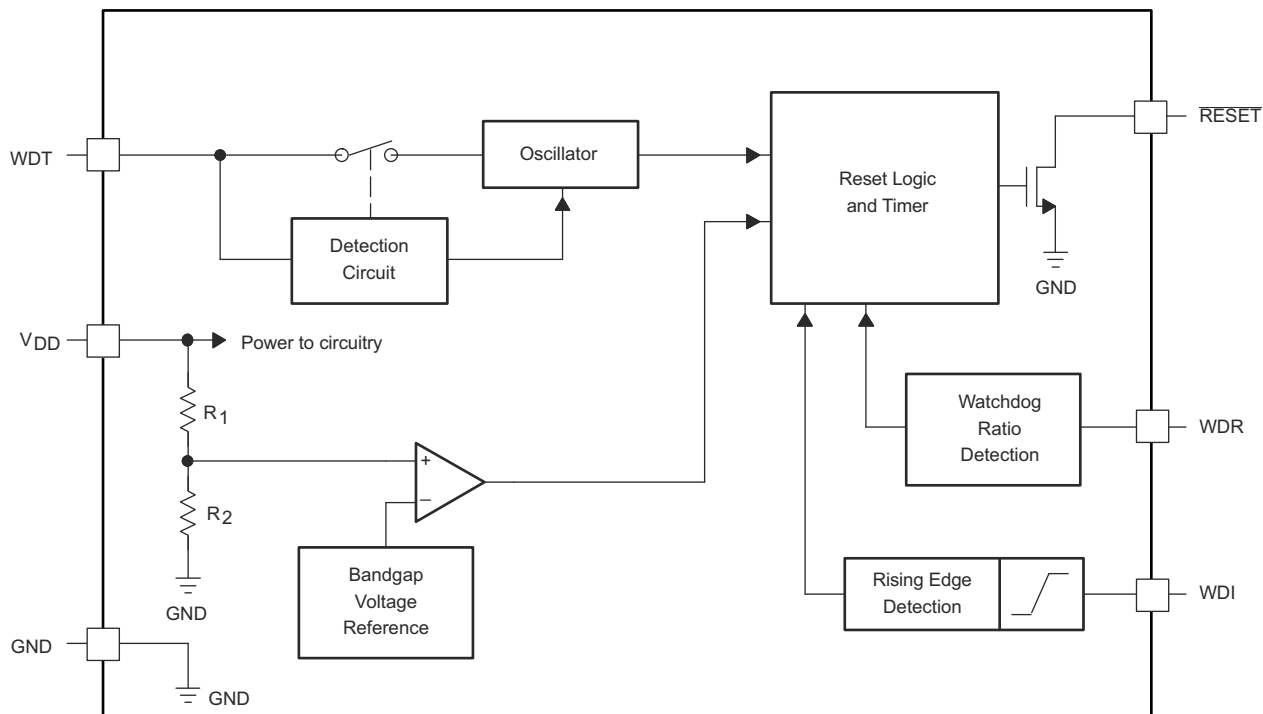
FIG 6-6. Minimum Pulse Duration At V_{DD} vs V_{DD} Threshold Overdrive Voltage

7 Detailed Description

7.1 Overview

The TPS3813-Q1 devices (TPS3813K33-Q1 and TPS3813I50-Q1) are a family of supervisory circuits with watchdog functionality. The TPS3813-Q1 family of devices is designed to assert a reset on the **RESET** pin when the supply (V_{DD}) drops below the threshold voltage (V_{IT}) which varies depending on which device is used. When the V_{DD} supply rises above 1.1 V, the **RESET** pin output state becomes valid and is active in logic low state until the V_{DD} supply crosses the voltage threshold ($V_{IT} + V_{HYS}$). The watchdog window can be programmed using the **WDT** and **WDR** pins with several different configurations, all of which are explained in the following sections.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator with integrated reference to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the following:

- Internal bandgap (reference voltage)
- Internal regulator
- State machine
- Buffers
- Other control logic blocks

Good design practice involves placing a 0.1 μF to 1 μF bypass capacitor at VDD input for noisy applications and to ensure enough charge is available for the device to power up correctly. The reset output is undefined when VDD is below V_{POR} .

7.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below the falling voltage threshold V_{IT} , the output reset is asserted. When the voltage at the VDD pin rises above the rising voltage threshold ($V_{\text{IT}+} = V_{\text{IT}} + V_{\text{HYS}}$), the output reset is deasserted after t_{D} reset time delay.

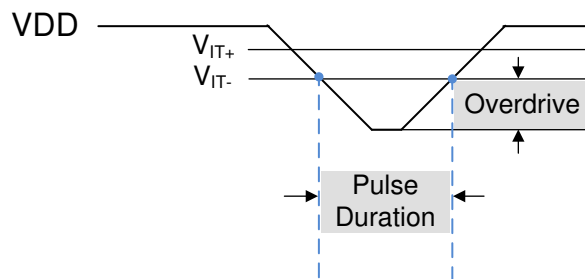
7.3.1.2 VDD Glitch Immunity

These devices are immune to quick voltage transient or excursion on VDD. Sensitivity to transients depends on both pulse duration ($t_{\text{GL_VIT}}$) found in [セクション 6.6](#) and transient overdrive. Overdrive is defined by how much VDD exceeds the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in [式 1](#).

$$\text{Overdrive} = |((V_{\text{DD}} / V_{\text{IT}}) - 1) \times 100\%| \quad (1)$$

where

- $V_{\text{IT}} = V_{\text{IT-}}$ is the threshold voltage
- $V_{\text{IT}+} = V_{\text{IT}} + V_{\text{HYS}}$ is the rising threshold voltage
- VDD is the input voltage crossing V_{IT}



☒ 7-1. Overdrive Versus Pulse Duration

TPS3813-Q1 devices have built-in glitch immunity ($t_{\text{GL_VIT-}}$) as shown in [セクション 6.6](#). ☒ 7-1 shows that VDD must fall below V_{IT} for $t_{\text{GL_VIT-}}$, otherwise the falling transistion is ignored. When VDD falls below V_{IT} for $t_{\text{GL_VIT-}}$, RESET transitions low to indicate a fault condition after the propagation delay high-to-low (t_{PHL}). When VDD rises above $V_{\text{IT}+} = V_{\text{IT}} + V_{\text{HYS}}$, RESET deasserts to a logic high indicating there is no more fault condition only if VDD remains above $V_{\text{IT}+}$ for longer than the reset delay (t_{D}).

7.3.2 Implemented Window-Watchdog Settings

The watchdog window can be set up in two different ways. The first way is to use the implemented timing, which is a default setting. The other way is to activate the default settings by wiring the WDT and WDR pin to V_{DD} or GND. Four different timings available with these settings which are listed in 表 7-1.

表 7-1. Window-Watchdog Configuration Settings

SELECTED OPERATION MODE		t_{window}	t_{boundary}
WDT = 0 V	WDR = 0 V	Max = 0.3 s	Max = 9.46 ms
		Typ = 0.25 s	Typ = 7.86 ms
		Min = 0.2 s	Min = 6.27 ms
	WDR = V _{DD}	Max = 0.3 s	Max = 2.43 ms
		Typ = 0.25 s	Typ = 2 ms
		Min = 0.2 s	Min = 1.58 ms
WDT = V _{DD}	WDR = 0 V	Max = 3 s	Max = 93.8 ms
		Typ = 2.5 s	Typ = 78.2 ms
		Min = 2 s	Min = 62.5 ms
	WDR = V _{DD}	Max = 3 s	Max = 23.5 ms
		Typ = 2.5 s	Typ = 19.6 ms
		Min = 2 s	Min = 15.6 ms

See 図 7-2 to visualize the values named in the table. The upper boundary of the window frame is defined by t_{window} and the lower boundary of the window frame is defined by t_{boundary} . 表 7-1 describes the upper and lower boundary settings. The device must detect a rising edge at the WDI pin between $t_{\text{boundary,max}}$ and $t_{\text{window,min}}$ to prevent asserting a reset. The values in 表 7-1 are typical and worst case conditions and are valid over the whole temperature range of -40°C to $+125^{\circ}\text{C}$.

The shaded areas shown in 図 7-2 are cases where undefined operation may happen. This device may not detect a violation if a WDI pulse occurs within these three shaded areas. The first shaded area addresses the situation of two consecutive rising edges occur within a quick amount of time. The typical time between rising edges should be more than 500 μs . The second and third shaded areas are defined by the min and max variance of the lower boundary (t_{boundary}) and upper boundary (t_{window}). Set the WDI rising edge within the $t_{\text{boundary,max}}$ and $t_{\text{window,min}}$ for correct operation.

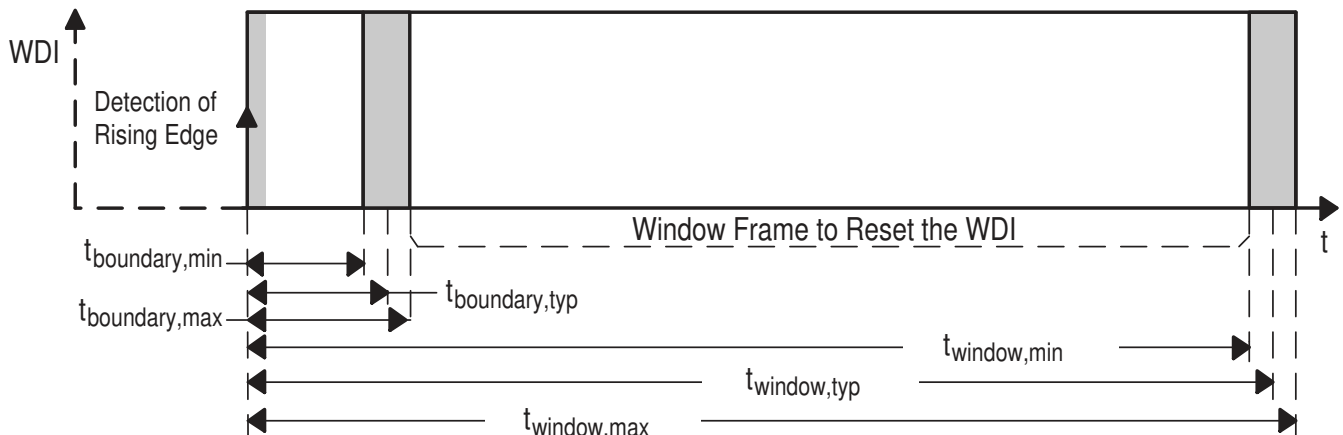


図 7-2. Upper and Lower Boundary Visualization

7.3.2.1 Timing Rules of Window-Watchdog

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses must fit into the configured window frame.

The lower boundary of the watchdog window begins with the rising edge of the WDI trigger pulse. At the same time, all internal timers are reset. If an external capacitor is used, the lower boundary is impacted because of the different oscillator frequency. See the [セクション 8.2.2.1](#) section for additional details. [図 7-3](#), especially the shaded boundary area, was prepared in a nonreal ratio scale to better visualize the description.

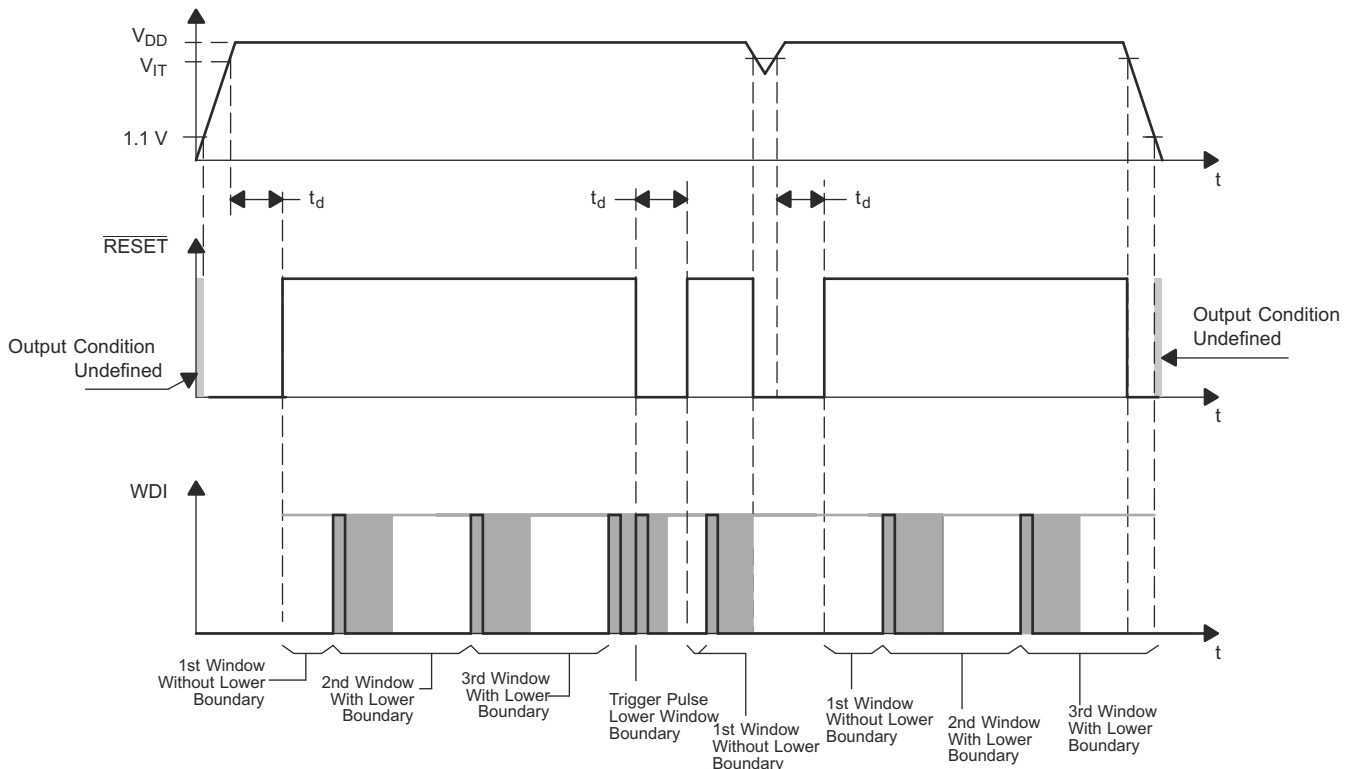


図 7-3. Timing Diagram

7.3.3 Watchdog Software Considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, TI recommends that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses should be set to different timings inside the window frame to release a defined reset if the program should hang in any subroutine. This setting allows the window watchdog to detect timeouts of the trigger pulse as well as pulses that distort the lower boundary.

7.4 Device Functional Modes

The functional mode for the TPS3813-Q1 family of devices is either on or reset. [表 7-2](#) lists the device truth table.

表 7-2. Device States

CONDITION	STATE	RESET
$V_{DD} > V_{IT}$	On	H
$V_{DD} < V_{IT}$	Reset	L
Watchdog fault		

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Lower-Boundary Calculation

The lower boundary can be calculated based on the values listed in the [セクション 6.7](#) table. Additionally, facts must be taken into account to verify that the lower boundary is where it is expected. Because the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin is taken into account at the next internal clock cycle. Accounting for any rising edge at the WDI pin occurs regardless of the external source. Because the shift between internal and external clock is not known, consider the worst-case condition when calculating this value.

表 8-1. Watchdog Lower-Boundary Calculation

SELECTED OPERATION MODE		LOWER BOUNDARY OF FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V	$t_{boundary,max} = t_{window,max} / 23.5$
		$t_{boundary,typ} = t_{window,typ} / 25.8$
		$t_{boundary,min} = t_{window,min} / 28.7$
	WDR = V_{DD}	$t_{boundary,max} = t_{window,max} / 51.6$
		$t_{boundary,typ} = t_{window,typ} / 64.5$
		$t_{boundary,min} = t_{window,min} / 92.7$

8.2 Typical Application

A typical application example (see [図 8-1](#)) is used to describe the function of the watchdog in more detail.

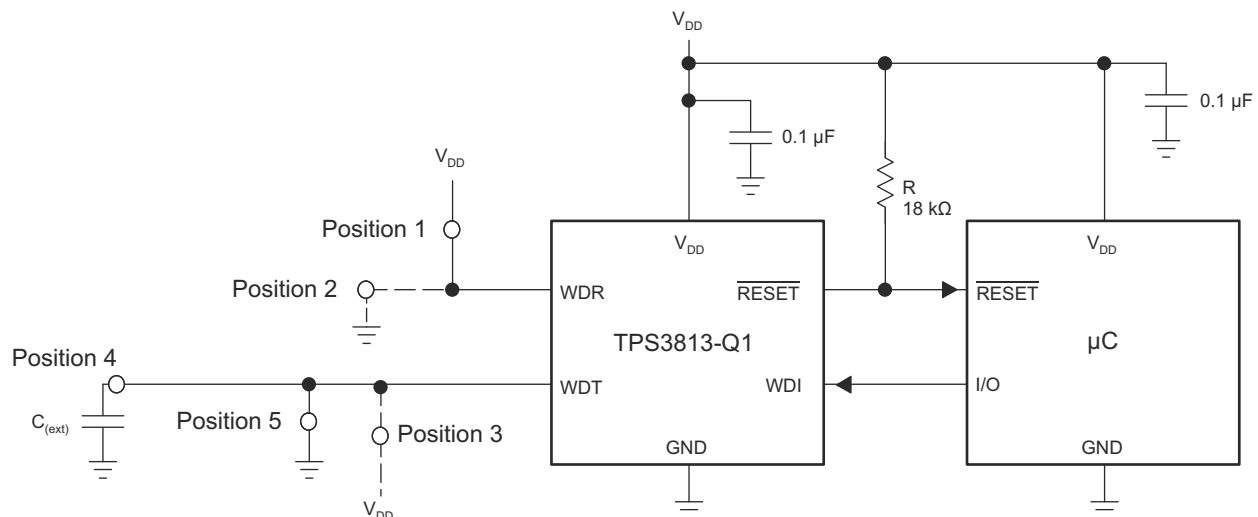


図 8-1. Application Example

8.2.1 Design Requirements

Design requirements include any design parameters that are solely based on the watchdog timing desired by the user. The [セクション 7.3.2](#) and [セクション 8.2.2](#) sections describe these timings. Select the TPS3813-Q1 device option based on desired threshold voltage of either 2.5 V, 3 V, 3.3 V, or 5 V.

8.2.2 Detailed Design Procedure

To configure the window watchdog function, two pins are provided by the TPS3813-Q1 family of devices. These pins set the window timeout and ratio.

The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. This ratio can be configured in two different frame sizes.

If the window watchdog ratio pin (WDR) is set to V_{DD} (Position 1 in [図 8-1](#)) then the lower boundary frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:124.9, for WDT connected to V_{DD} , the value is a ratio of 1:127.7, and for an external capacitor connected to WDT, the value is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND (Position 2) the lower boundary frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:31.8, for WDT connected to V_{DD} the value is a ratio 1:32, and for an external capacitor connected to WDT the value is a ratio of 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 s and 2.5 s for the window or can be programmed by connecting an external capacitor with a low leakage current at WDT.

For example, if the watchdog timeout pin (WDT) is connected to V_{DD} , the timeout is 2.5 s. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD} , the lower boundary is 19.6 ms.

8.2.2.1 Programming Window-Watchdog Using an External Capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. The capacitors that are used should have low ESR and low tolerances because the tolerances must be considered to perform the calculations. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{\text{boundary,max}}$ and $t_{\text{window,min}}$. The trigger pulse must fit into this window frame.

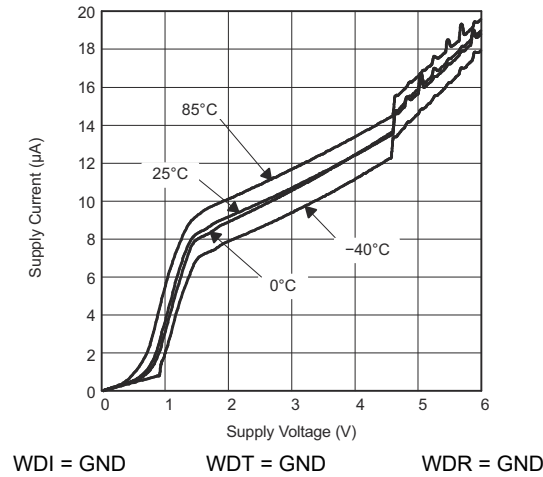
The external capacitor should have a value between a minimum of 155 pF and a maximum of 63 nF.

$$t_{\text{window,typ}} = \left(\frac{C_{(\text{ext})}}{15.55 \text{ pF}} + 1 \right) \times 6.25 \text{ ms} \quad (2)$$

表 8-2. Watchdog Upper-Boundary Capacitor Programming

SELECTED OPERATION MODE		WINDOW FRAME
WDT = external capacitor $C_{(\text{ext})}$	WDR = 0 V and WDR = V_{DD}	$t_{\text{window,max}} = 1.25 \times t_{\text{window,typ}}$
		$t_{\text{window,min}} = 0.75 \times t_{\text{window,typ}}$

8.2.3 Application Curve



8-2. Supply Current vs Supply Voltage

9 Power Supply Recommendations

TPS3813-Q1 family of devices are designed to operate from an input supply with a voltage range from 2 V to 6 V. Although not required, placing a 0.1-µF ceramic capacitor close to the V_{DD} pin is good analog design practice.

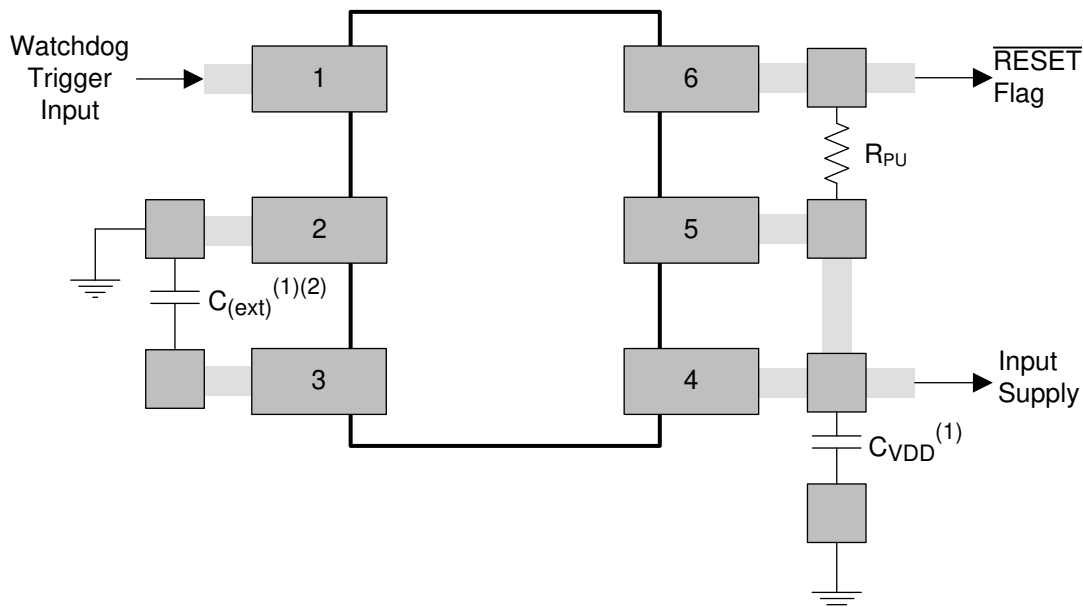
10 Layout

10.1 Layout Guidelines

Use the following guidelines for proper layout design of the device:

- Place the V_{DD} decoupling capacitor as close to the device as possible.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor, along with the parasitic inductance from the supply to the capacitor, can cause ringing if the traces are excessive.
- If using a capacitor between the WDT pin and GND pin to program the upper boundary of the window-watchdog, the capacitor must be placed as close to the device as possible.
- Traces for WDR and WDT pins must be short and tight to avoid building up excessive parasitics.

10.2 Layout Example



- A. In this layout example, the WDR pin is tied to V_{DD} and the WDT pin is tied to GND through an external capacitor.
- B. The overall window timeout in this configuration is based on the external capacitor connected to the WDT pin. The formula used to calculate this value can be found in the [セクション 8.2.2](#) section.
- In this configuration, the ratio of the frame lower boundary is 1:64.5 (typical) of the overall window timeout size. The maximum and minimum ratios are 1:51.6 and 1:92.7 of the overall window timeout size, respectively.

図 10-1. Device Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

図 11-1 shows a legend for reading the complete device name for and TPS3813-Q1 device.

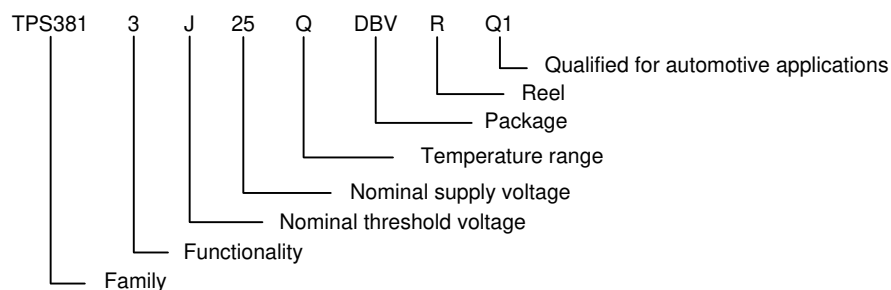


図 11-1. Device Nomenclature

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [All Window-Watchdog Supervisors](#) (SLVA365)
- [Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs](#) (SLVA485)
- [Disabling the Watchdog Timer for TI's Family of Supervisors](#) (SLVA145)
- [Window Watchdog Calculator for TPS3813 Voltage Supervisors](#) (SPRCAG1)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3813I50QDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBI
TPS3813K33QDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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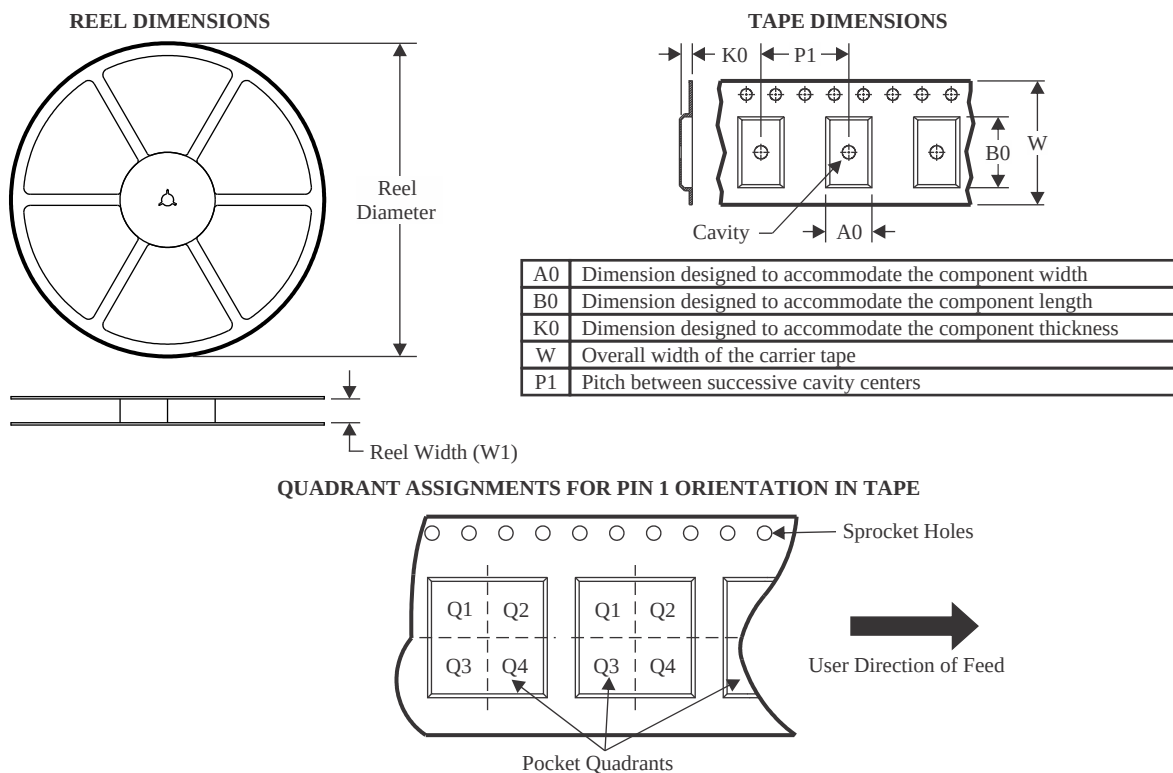
OTHER QUALIFIED VERSIONS OF TPS3813-Q1 :

- Catalog : [TPS3813](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

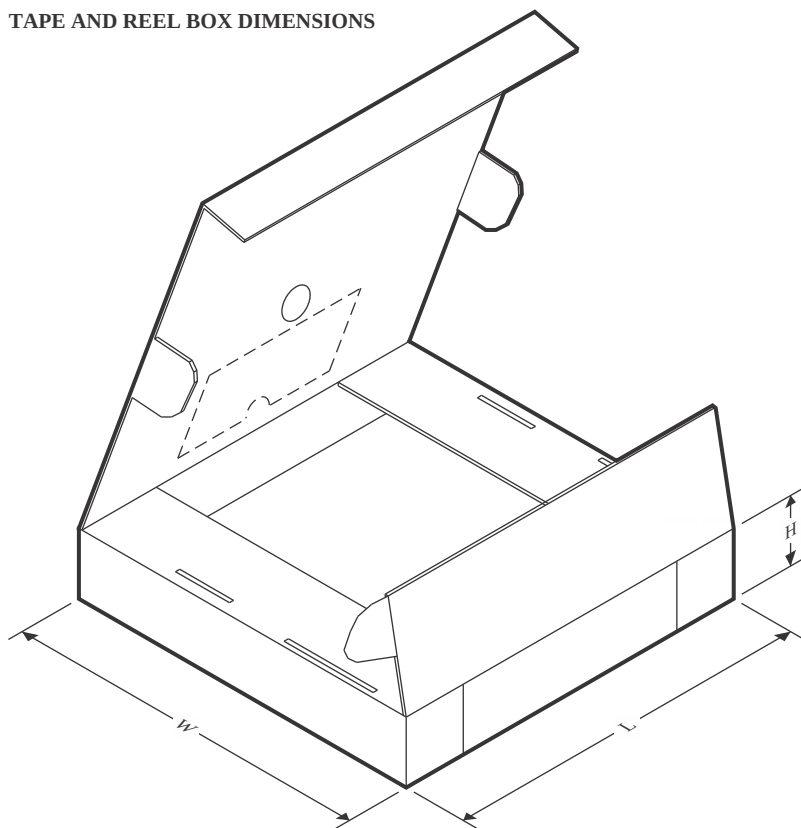
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

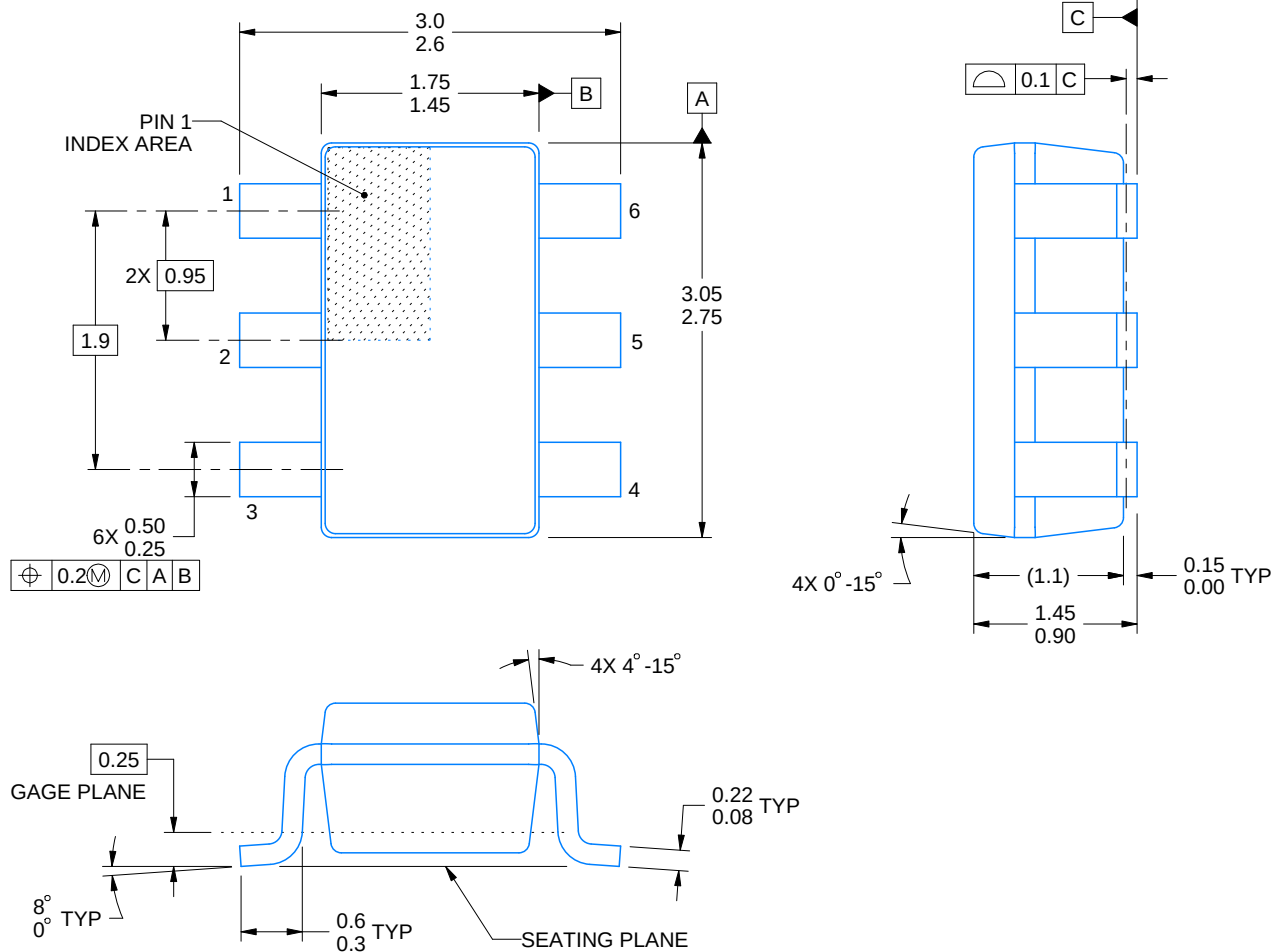


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

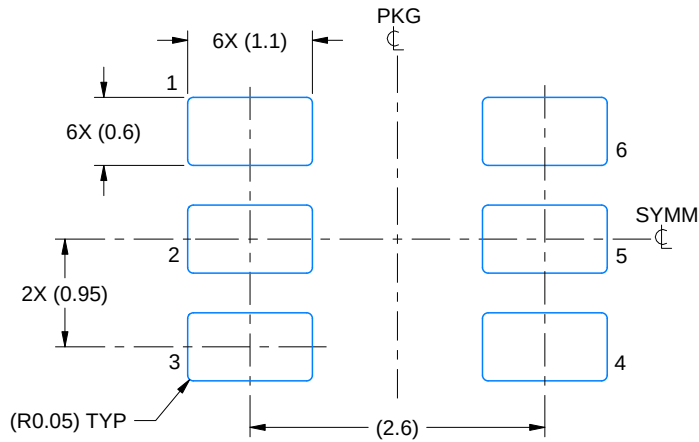
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

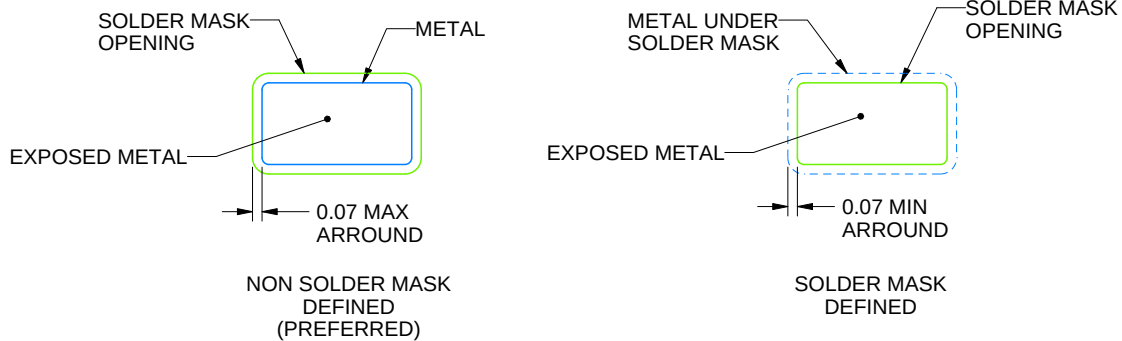
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

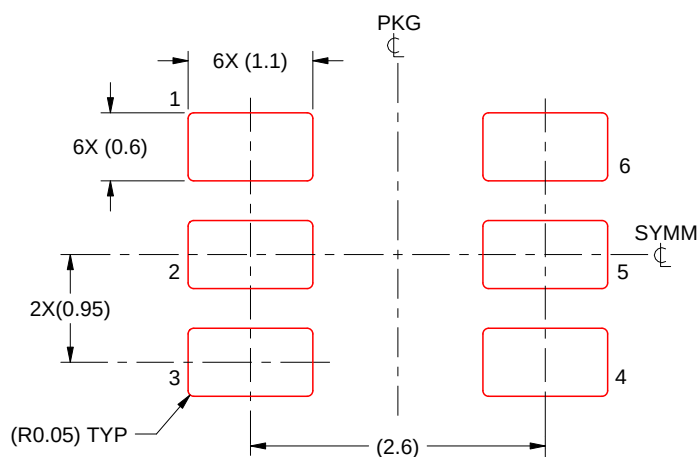
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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