12GSPS DAC と 3GSPS ADC、400MHz IBW 搭載、AFE7903 2T2R 5MHz～7.4GHz RF サンプリング AFE

1 特長

- データシート全体のご請求
- デュアル RF サンプリング 12GSPS 送信 DAC
- デュアル RF サンプリング 3GSPS 受信 ADC
- TX または RX ごとの最大信号帯域幅：400MHz
- RF 周波数範囲：5MHz～7.4GHz
- デジタル・ステップ・アッテネータ (DSA)：
  – TX：40dB レンジ、0.125dB ステップ
  – RX：25dB レンジ、0.5dB ステップ
- TX と RX 向けにシングルバンドまたはデュアルバンド DUC / DDC を搭載
- TX / RX に対応する 16 個の NCO
- DAC / ADC クロック用の内部 PLL / VCO、または DAC もしくは ADC サンプル・レートでの外部クロックを選択可能
- Sysref アライメント検出器
- SerDes データ・インターフェイス：
  – JESD204B、JESD204C 適合
  – 8 つの SerDes トランシーバ (最高 29.5Gbps)
  – サブクラス 1 のマルチデバイス同期
- パッケージ：17mm × 17mm (0.35mm ピッチ)

2 アプリケーション

- レーダー
- シーカー・フロント・エンド
- 防衛無線
- 技術通信インフラストラクチャ
- ワイヤレス通信テスト

3 概要

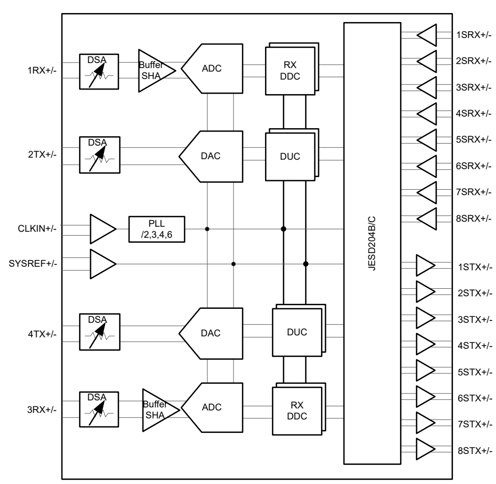
AFE7903 は、高性能で広帯域のマルチチャネル・トランシーバで、2 つの RF サンプリング・トランスミッタ・チェーンと 2 つの RF サンプリング・レシーバ・チェーンを内蔵しています。このデバイスは、最大 7.4GHz で動作するため、追加の周波数変換段を必要とせず、HF、VHF、UHF、L、S、C バンドの周波数範囲について直接 RF サンプリングが可能です。この密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

TX 信号パスは、最大 400MHz の信号帯域幅を実現する補間およびデジタル・アップ・コンバージョン・オプションをサポートしています。DUC の出力は、2 次ナイキスト動作を拡張する混在モード出力方式で 12GSPS の DAC (D/A コンバータ) を駆動します。DAC 出力は、40dB レンジ、1dB アナログ・ステップ、0.125dB デジタル・ステップの可変ゲイン・アンプ (TX DSA) を内蔵しています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AFE7903	FC-BGA	17mm × 17mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 概要 (続き)

各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。各レシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションによりデータ帯域幅を 2 つの RX では最高 400MHz で最適化できます。

SYSREF タイミング検出器を搭載しているため、デバイス・クロックを基準とした SYSREF 入力タイミングの最適化が可能です。

5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from July 14, 2022 to June 5, 2023 (from Revision A (July 2022) to Revision B (June 2023)) **Page**

- 「製品情報」を「パッケージ情報」表に変更 1
- Changed I_{IH} and I_{IL} units to µA..... 22
- Removed TX Clock Dither Enabled from TX Typical characteristics and specification headers..... 72
- Changed 1st Nyquist zone output to 2nf Nyquist zone output in セクション 6.12.14 header..... 132

Changes from March 1, 2022 to July 14, 2022 (from Revision * (March 2022) to Revision A (July 2022)) **Page**

- DSA および NCO の特長から FB を削除..... 1
- ADC sample rate divider..... 20
- Changed 2.6 to 1.8 GHz matching..... 47
- Removed Dither = 1 from the conditions and dither plot..... 72
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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/3}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	{1/3}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110(1)	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

6.4 Thermal Information

THERMAL METRIC(1)		17x17mm FC-BGA	UNIT
		400 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC_{RES}	DAC resolution			14		bits
f_{RFout}	RF output frequency range	f_{DAC} = 12 GSPS, 1st Nyquist	5		6000	MHz
		f_{DAC} = 9 GSPS, 1st Nyquist	5		4500	
		f_{DAC} = 9 GSPS, 2nd Nyquist	4500		7400	
		f_{DAC} = 6 GSPS, 1st Nyquist	5		3000	
		f_{DAC} = 6 GSPS, 2nd Nyquist	3000		6000	
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 10 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 30 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 400 MHz, f_{DAC} = 6GSPS, -0.1dBFS		5.6		dBm
		f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f_{out} = 3500 MHz, -0.5dBFS		2.9		dBm
		f_{out} = 4900 MHz, -0.5dBFS		-0.6		dBm
		f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R_{TERM}	Output termination resistor	Default setting		100		Ω
ATT_{range}	DSA Attenuation range			40		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (1)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration		±0.2		
ATT_{step}	DSA Gain Steps Phase accuracy, any 8dB range(1)	f_{out} = 30MHz		±1		deg
		f_{out} = 400MHz		±1		deg
		f_{out} = 850MHz		±1		deg
		f_{out} = 1800MHz		±1		deg
		f_{out} =2600MHz		±1		deg
		f_{out} = 3500MHz		±1		
		f_{out} = 4900MHz		±1		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	f_{DAC} =6 GSPS, f_{out} = 5MHz ±1MHz, -7dBFS each tone		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -7dBFS each tone		-47		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -7dBFS each tone		-51		dBc
		f_{out} = 850MHz ±10MHz, -7dBFS each tone		-61		dBc
		f_{out} = 1800MHz ±10MHz, -7dBFS each tone		-62		dBc
		f_{out} = 2600MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 3500MHz ±10MHz, -7dBFS each tone		-63		dBc
		f_{out} = 4900MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 5MHz ±1MHz, -13dBFS each tone		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -13dBFS each tone		-71		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -13dBFS each tone		-72		dBc
		f_{out} = 850MHz ±10MHz, -13dBFS each tone		-73		dBc
		f_{out} = 1800MHz ±10MHz, -13dBFS each tone		-75		dBc
		f_{out} = 2600MHz ±10MHz, -13dBFS each tone		-79		dBc
		f_{out} = 3500MHz ±10MHz, -13dBFS each tone		-77		dBc
		f_{out} = 4900MHz ±10MHz, -13dBFS each tone		-77		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 30 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		45		dBc
		f_{out} = 400 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		48		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		62		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		56		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		39		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		42		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		60		dBc

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_S/2$ - f_{OUT}	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-47		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-43		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-43		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-75		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-73		dBc
		f_{out} = 400 MHz		-46		dBc
		f_{out} = 850 MHz		-65		dBc
		f_{out} = 1800 MHz		-68		dBc
		f_{out} = 2600 MHz		-47		dBc
		f_{out} = 3500 MHz		-59		dBc
		f_{out}= 4900 MHz		-48		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-74		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-67		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-58		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-69		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-59		dBc
HD3	3rd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-46		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-49		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-49		dBc
		f_{out} = 850 MHz		-56		dBc
		f_{out} = 1800 MHz		-58		dBc
		f_{out} = 2600 MHz		-60		dBc
		f_{out} = 3500 MHz		-63		dBc
		f_{out}= 4900 MHz		-66		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-82		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-88		dBc

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-58		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-60		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-61		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-50		dBc
		f_{out} = 850 MHz		-85		dBc
		f_{out} = 1800 MHz		-90		dBc
		f_{out} = 2600 MHz		-84		dBc
		f_{out} = 3500 MHz		-86		dBc
		f_{out}= 4900 MHz		-87		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-94		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-93		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-85		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-89		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-88		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-89		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{DAC} =6 GSPS, f_{out} = 400 MHz		87		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		84		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		78		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		80		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		81		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		74		dBc
f_S/4	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/4-50MHz		-95		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/4-50MHz		-88		dBFS
		f_{DAC} = 11796.48MSPS, f_{OUT}=f_{DAC}/4-50MHz		-76		dBFS
f_S/2	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/2-50MHz		-52		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/2-50MHz		-45		dBFS
		f_{DAC} = 11796.48 MSPS, f_{OUT}=f_{DAC}/2-50MHz		-49		dBFS

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_S/4$	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-82		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-75		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS, f_{OUT}=3*f_{DAC}/4-50MHz		-49		dBFS
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-70		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-62		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-61		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-50		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-72		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-60		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-69		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-64		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-59		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-53		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-38		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.16		%
		F_{out} =1.8425 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.21		%
		F_{out} =2.6 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.24		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.27		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.38		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 5 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-148		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-143		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-129		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 30 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-154		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-142		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-132		dBFS/Hz

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 100 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-158		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-136		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 400 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-160		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-153		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.8		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.7		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-148.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-137.9		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-157.9		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-151.3		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.8		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-158.3		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151.6		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144.9		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-134.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-158.2		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-150.9		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-144.4		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-133.4		dBFS/Hz

6.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 500MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and 9GSPS above 6GHz; PLL clock mode below 6GHz and External clock mode above 6GHz; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-154.6		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-147.0		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-140.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-129.9		dBFS/Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-12		dB
Isolation	Far Channel: 2TXOUT to 4TXOUT	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(2)		-104		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(2)		-100		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(2)		-105		dB
		f_{out} = 400 MH, f_{DAC} = 6000MSPS, straight mode(3)		-97		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-91		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83.2		dB
PN_{TXADD}	Additive Phase Noise External Clock Mode (4)	f_{out} = 3.7GHz, f_{OFFSET} = 100Hz		-97		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1kHz		-106		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10kHz		-117		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 100kHz		-128		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1MHz		-138		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10MHz		-144		dBc/Hz

(1) After DSA calibration procedure
(2) measured with 1µH DC feed inductor
(3) measured with 0.39µH DC feed inductor
(4) Input clock phase noise subtracted.

6.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		5		7400	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 5 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-0.4		dBm
		f_{IN} = 30 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-2.2		dBm
		f_{IN} = 410 MHz, DSA=0dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 12		-2.5		dBm
		f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
$P_{FS\_CW,MAX}$	MAX Full scale input power - reliability limited, at device pins	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		19.7		dBm
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		17.8		dBm
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		17.6		dBm
		f_{IN} = 830 MHz		16.7		dBm
		f_{IN} = 1760 MHz		17.0		dBm
		f_{IN} = 2610 MHz		18		dBm
		f_{IN} = 3610 MHz		18.5		dBm
		f_{IN} = 4910 MHz		19.3		dBm
R_{TERM}	Input reference impedance			100.0		Ω
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		1.8		deg
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

6.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density [3] (small signal = -30dBFS)	f_{IN} = 5 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-147.1		dBFS/Hz
		f_{IN} = 30 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-150.7		dBFS/Hz
		f_{IN} = 410 MHz, DSA = 3dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-155.4		dBFS/Hz
		f_{IN} = 830 MHz, DSA = 3dB		-156.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 3dB		-156.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 3dB		-155.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48, 3<=Atten<=22		-147.8		dBFS/Hz
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24, 3<=Atten<=22		-151.5		dBFS/Hz
		f_{IN} = 410 MHz, 3<=Atten<=22, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-156.6		dBFS/Hz
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		29.4		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		24.5		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		19.3		dB
		f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB

6.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure(4) DSA Atten=4dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		30.6		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		25.1		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		20.1		dB
		f_{IN} = 830 MHz		20.0		dB
		f_{IN} = 1760 MHz		20.6		dB
		f_{IN} = 2610 MHz		21.9		dB
		f_{IN} = 3610 MHz		23.5		dB
		f_{IN} = 4910 MHz		22.3		dB
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		45.9		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		40.2		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		35.0		dB
		f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
IMD3	3^{rd} order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 30±1 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-82		dBc
		f_{IN} = 400MHz and 405MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-75		dBc
		f_{IN} = 840 MHz		-82		dBc
		f_{IN} = 1770 MHz		-84		dBc
		f_{IN} = 2610 MHz		-74		dBc
		f_{IN} = 3610 MHz		-77		dBc
		f_{IN} = 4920 MHz		-76		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		100		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		94		dBFS
		f_{IN} = 830 MHz		88		dBFS
		f_{IN} = 1760 MHz		81		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		79		dBFS

6.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(2)	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-84		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-90		dBFS
		f_{IN} = 830 MHz		-86		dBFS
		f_{IN} = 1760 MHz		-90		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-87		dBFS
		f_{IN} = 4910 MHz		-84		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-96		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-94		dBFS
		f_{IN} = 830 MHz		-80		dBFS
		f_{IN} = 1760 MHz		-85		dBFS
		f_{IN} = 2610 MHz		-86		dBFS
		f_{IN} = 3610 MHz		-78		dBFS
		f_{IN} = 4910 MHz		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-94		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-94		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-94		dBFS
		f_{IN} = 830 MHz		-88		dBFS
		f_{IN} = 1760 MHz		-81		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-82		dBFS
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		101		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		95		dBFS
		f_{IN} = 830 MHz		89		dBFS
		f_{IN} = 1760 MHz		89		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		87		dBFS
		f_{IN} = 4910 MHz		90		dBFS

6.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS and 500MSPS above 6GHz, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 9GHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion(2) A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-104		dBFS
		f_{IN} = 830 MHz, with board trim		-79		dBFS
		f_{IN} = 1760 MHz, with board trim		-102		dBFS
		f_{IN} = 2610 MHz, with board trim		-100		dBFS
		f_{IN} = 3610 MHz, with board trim		-101		dBFS
		f_{IN} = 4910 MHz, with board trim		-99		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-103		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-84		dBFS
		f_{IN} = 381 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 830 MHz		-95		dBFS
		f_{IN} = 1760 MHz		-95		dBFS
		f_{IN} = 2610 MHz		-98		dBFS
		f_{IN} = 3610 MHz		-97		dBFS
		f_{IN} = 4910 MHz		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-95		dBFS
		f_{IN} = 830 MHz		-89		dBFS
		f_{IN} = 1760 MHz		-89		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90		dBFS
TX-RX Isolation	2TXOUT to 1RXIN 4TXOUT to 3RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-105		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-101		dB
		f_{IN} = 400 MHz		-99		dB
		f_{IN} = 830 MHz		-86		dB
		f_{IN} = 1760 MHz		-87		dB
		f_{IN} = 2610 MHz		-84		dB
		f_{IN} = 3610 MHz		-82		dB
		f_{IN} = 4910 MHz		-82		dB

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.

(2) After HD2 trim on specific printed circuit board.
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB

6.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f_{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
DIV_{RXADC}				1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error(1)	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff

6.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance[2]	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

6.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode			400		mV
Z_{SRdiff}	SerDes Internal Differential Termination(1)			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	
		Quarter rate mode	4.75		8.125	
		1/8th	2.375		4.062	
		1/16th	1.1875		2.031	
	Insertion Loss Tolerance(2)	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Input Voltage		VDD1P8GPIO–0.2			V
V_{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff(3)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff(3)
Z_T	Input termination	differential		100		Ω

6.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff(3)
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

6.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1a: 2T2R - TDD, 50%/50% duty cycle TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		260		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			297		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			70		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			89		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			288		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			536		mA
P_{diss}	Power Dissipation			2166		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1b: 2T2R - TX active, RX in standby, TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		205		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			282		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			71		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			21		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			365		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			499		mA
P_{diss}	Power Dissipation			2014		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1c: 2T2R - RX active, TX in standby TX: 125 MSPS input, 24x Int, f_{DAC} = 3 GSPS RX: f_{ADC} = 1.5 GSPS, 12x Dec, 125 MSPS output f_{OUT}=f_{IN}= 400 MHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		315		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			313		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			70		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			211		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			76		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			573		mA
P_{diss}	Power Dissipation			2318		mW

6.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 2T2R - FDD TX: 125MSPS input, 24x Int, f_{DAC} = 3GSPS RX: f_{ADC} = 1.5GSPS, 12x Dec, 125MSPS output f_{OUT} = 400 MHz, f_{IN} = 500 MHz Serdes: 8b/10b, 10Gbps TX/RX LMFS: 1-4-8-1		458		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			335		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			71		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			158		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			386		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			77		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			728		mA
P_{diss}	Power Dissipation			2974		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3a: 2T2R - TDD, 50%/50% duty cycle TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		307		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			321		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			397		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1108		mA
P_{diss}	Power Dissipation			3047		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3b: 2T2R - TX active, RX in standby TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		266		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			293		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			26		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			545		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1061		mA
P_{diss}	Power Dissipation			2899		mW

6.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3c: 2T2R - RX active, TX in standby TX: 500 MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		349		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			350		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			287		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			248		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1155		mA
P_{diss}	Power Dissipation			3195		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 2T2R - FDD TX: 500MSPS input, 24x Int, f_{DAC} = 12 GSPS RX: f_{ADC} = 3 GSPS, 6x Dec, 500MSPS output f_{OUT}= 3.5GHz, f_{IN}= 3.7 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		550		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			371		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			288		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			567		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1568		mA
P_{diss}	Power Dissipation			4354		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5a: 2T2R - TDD, 50%/50% duty cycle TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		307		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			312		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			157		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			370		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1051		mA
P_{diss}	Power Dissipation			2948		mW

6.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5b: 2T2R - TX active, RX in Standby TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		265		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			284		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			26		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			507		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			969		mA
P_{diss}	Power Dissipation			2749		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5c: 2T2R - RX active, TX in standby TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		348		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			341		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			287		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			234		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			88		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1133		mA
P_{diss}	Power Dissipation			3146		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6: 2T2R FDD TX: dual 125 MSPS input, 48x Int, f_{DAC} = 6 GSPS, MixMode RX: dual f_{ADC} = 3 GSPS, 24x Dec, 125 MSPS output f_{OUT}=f_{IN}= 3.5 GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-8-16-1		550		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			362		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			289		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			530		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			89		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1518		mA
P_{diss}	Power Dissipation			4253		mW

6.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.		16		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			174		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			33		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			37		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			155		mA
P_{diss}	Power Dissipation			596		mW

6.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(\overline{SDEN})}$	Setup Time, $\overline{SDEN}$ to Rising Edge of SCLK		15		ns
$t_{h(\overline{SDEN})}$	Hold Time, $\overline{SDEN}$ after last Rising Edge of SCLK (1)		5 + t_{SCLK}		ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(SCLK)\_W}$	Minimum SCLK period: registers write		25		ns
$t_{(SCLK)\_R}$	Minimum SCLK period: registers read		50		ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) $\overline{SDEN}$ need to be held one more extra clock cycle with the last SCLK edge

6.11 Switching Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

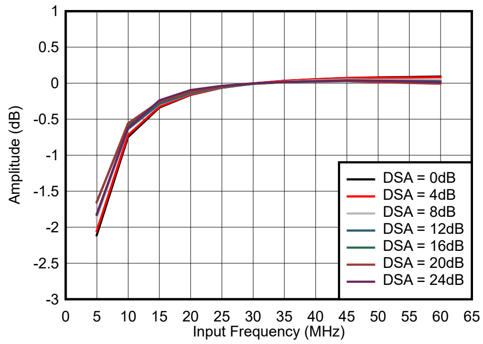
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t_{JESDTX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles(1)
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
t_{JESDRX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles(1)
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
	SerDes Transmitter Analog Delay			3.6		ns

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

6.12 Typical Characteristics

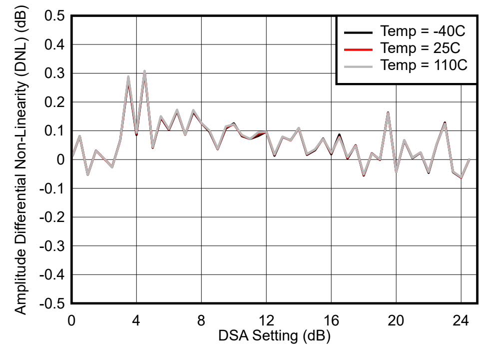
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



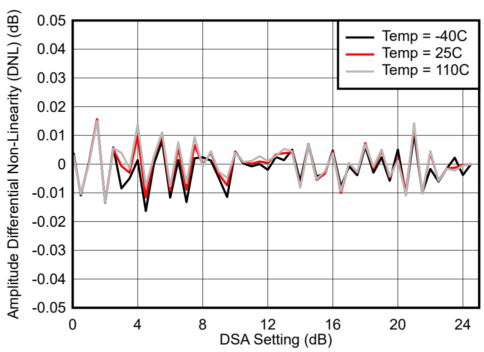
Normalized to 30 MHz

図 6-1. RX In-Band Gain Flatness, f_{IN} = 30 MHz



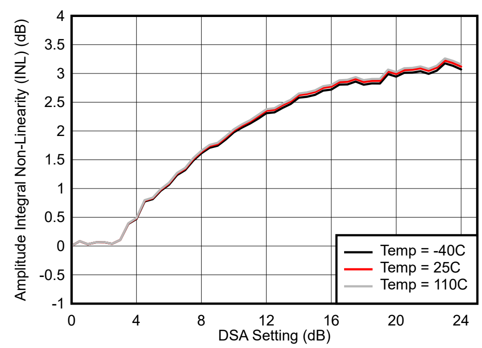
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



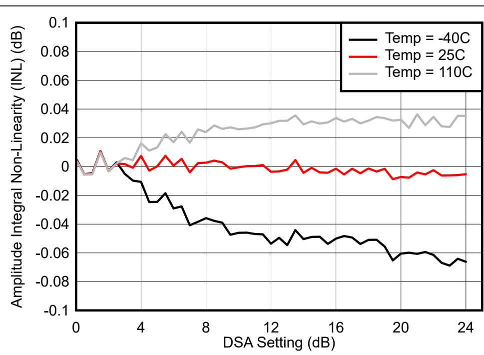
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz



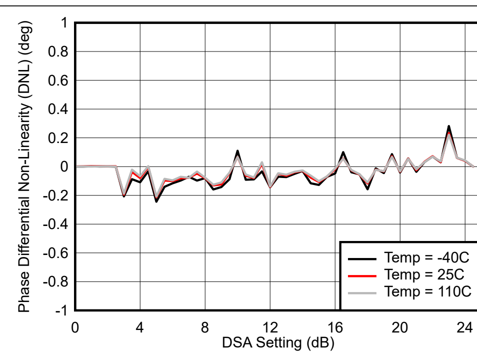
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz

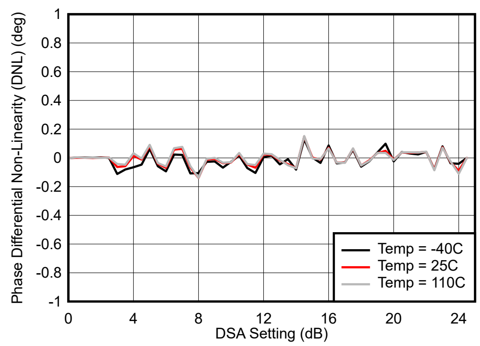


Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz

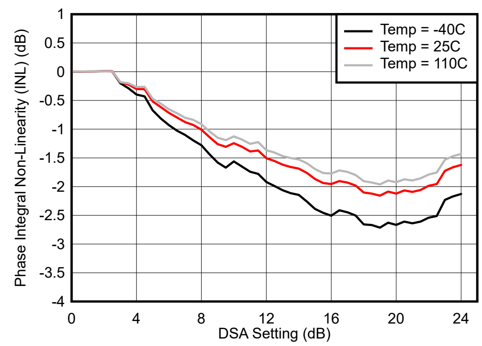
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



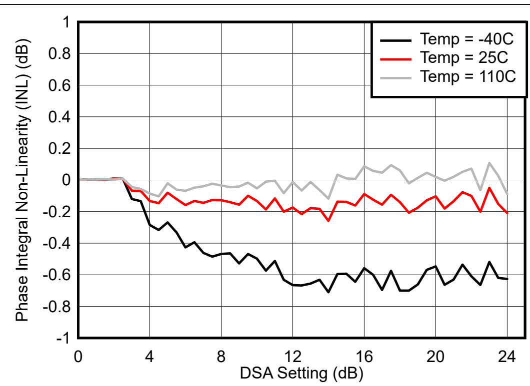
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

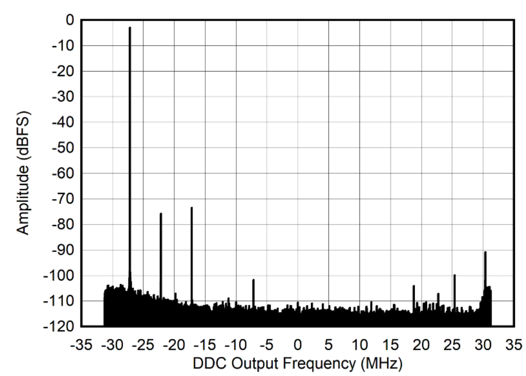
図 6-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz



With 0.8 GHz matching

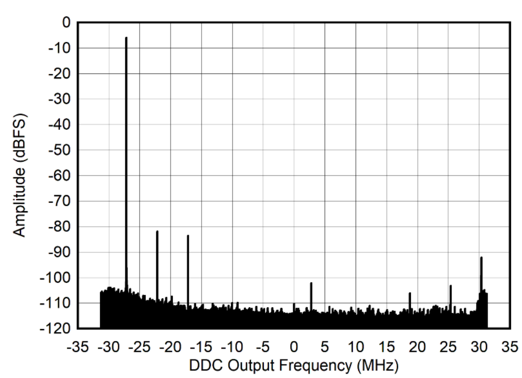
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz



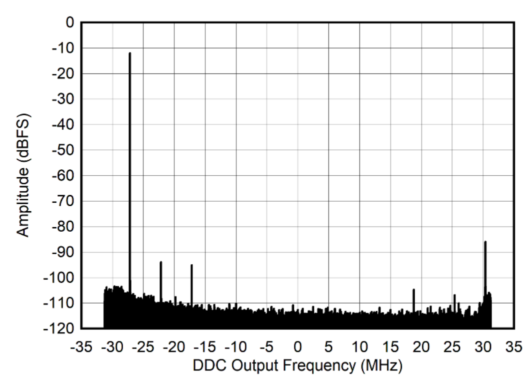
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-10. RX Output FFT at 5 MHz



A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 6-11. RX Output FFT at 5 MHz

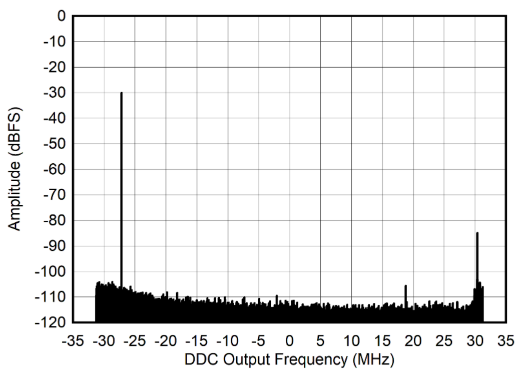


A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-12. RX Output FFT at 5 MHz

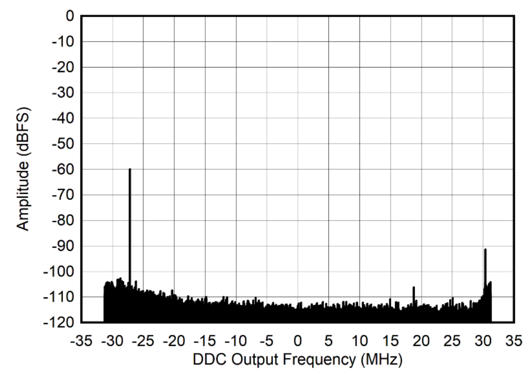
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



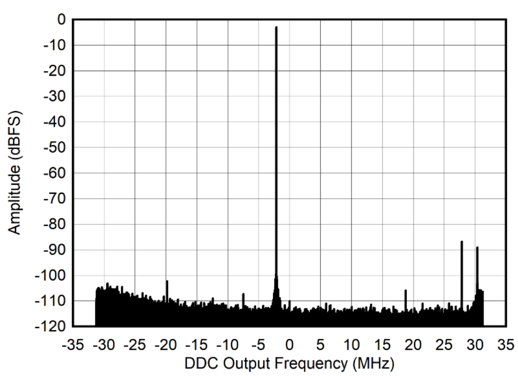
A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-13. RX Output FFT at 5 MHz



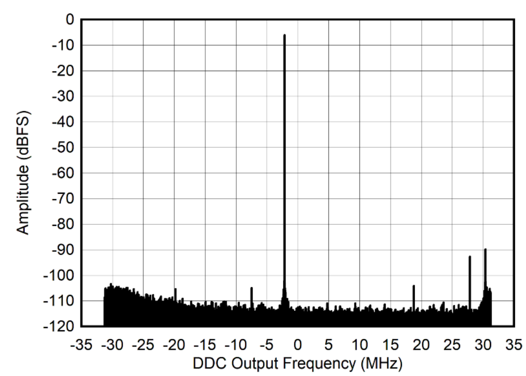
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-14. RX Output FFT at 5 MHz



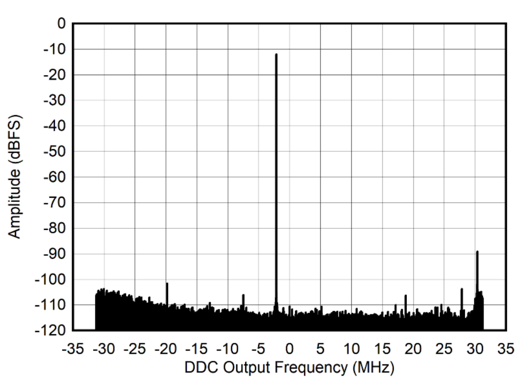
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-15. RX Output FFT at 30 MHz



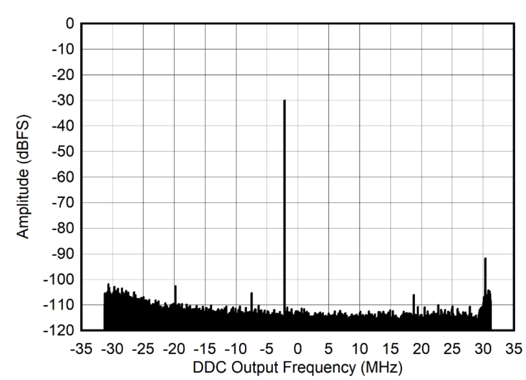
A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-16. RX Output FFT at 30 MHz



A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-17. RX Output FFT at 30 MHz

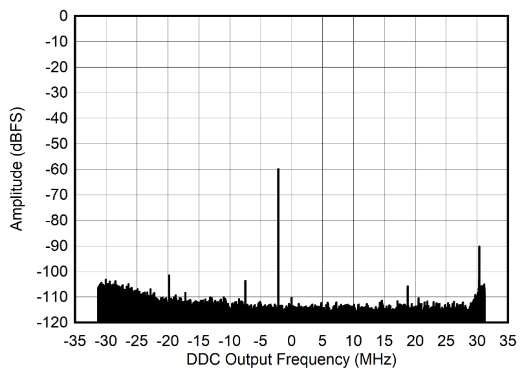


A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-18. RX Output FFT at 30 MHz

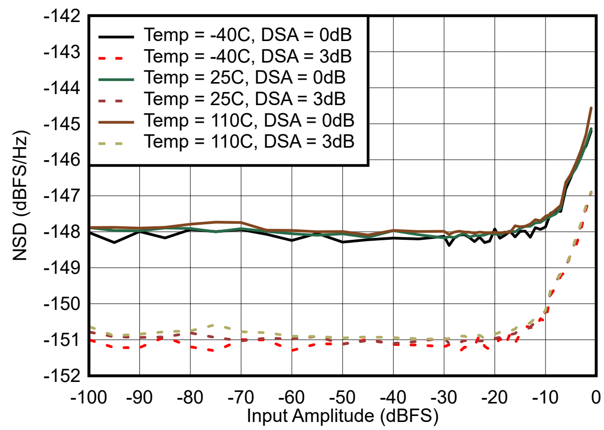
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



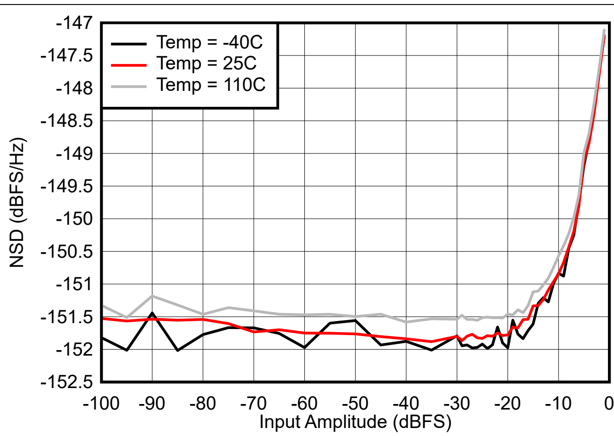
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-19. RX Output FFT at 30 MHz



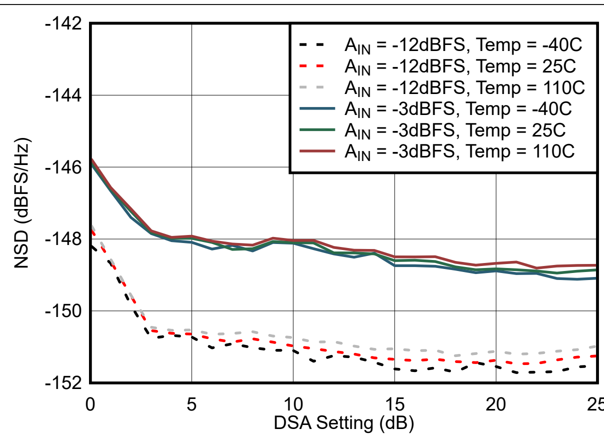
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

図 6-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-21. NSD vs Input Amplitude at 30 MHz with DSA = 12

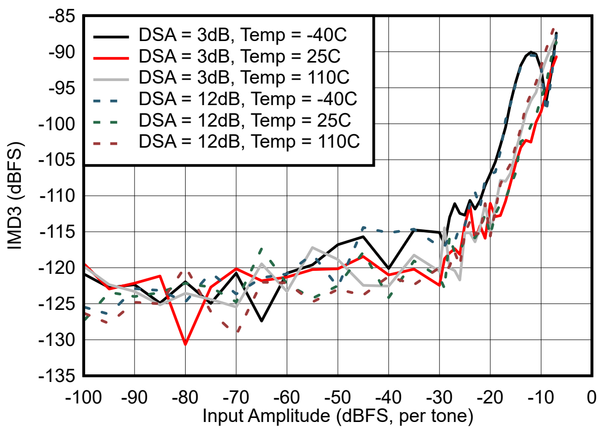


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-22. NSD vs DSA Attenuation at 30 MHz

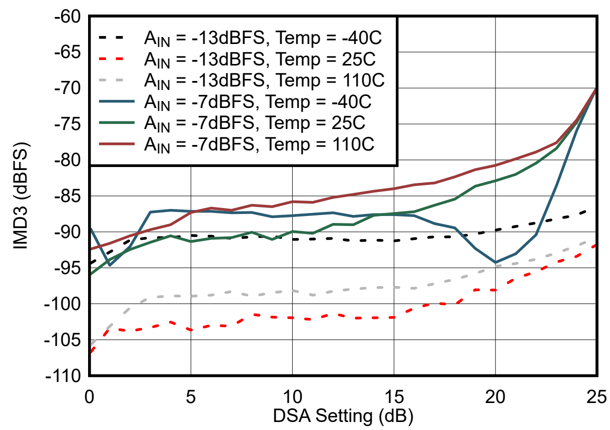
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



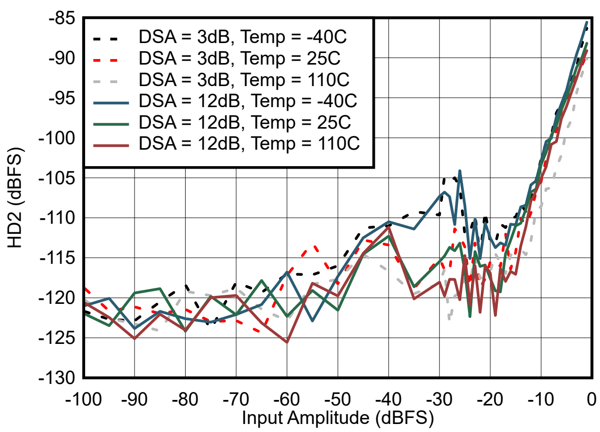
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-23. IMD3 vs Input Amplitude at 30 MHz



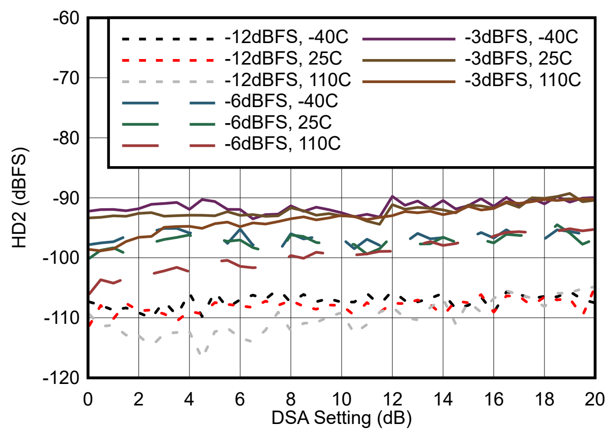
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-24. IMD3 vs DSA Setting at 30 MHz



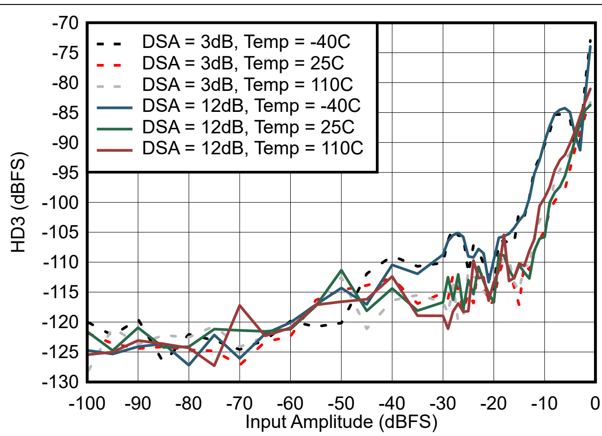
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-25. HD2 vs Input Amplitude at 30 MHz



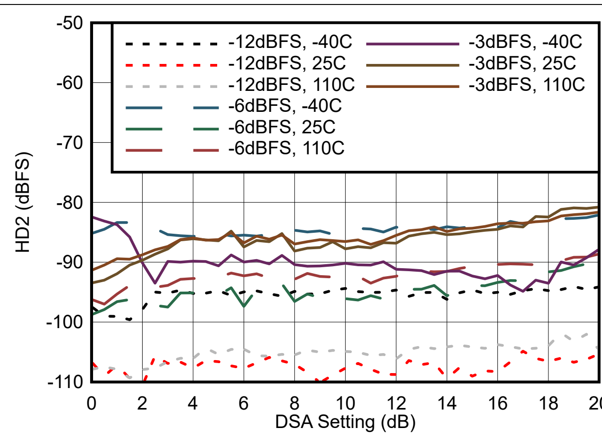
f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 6-26. HD2 vs DSA Setting at 30 MHz



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-27. HD3 vs Input Amplitude at 30 MHz

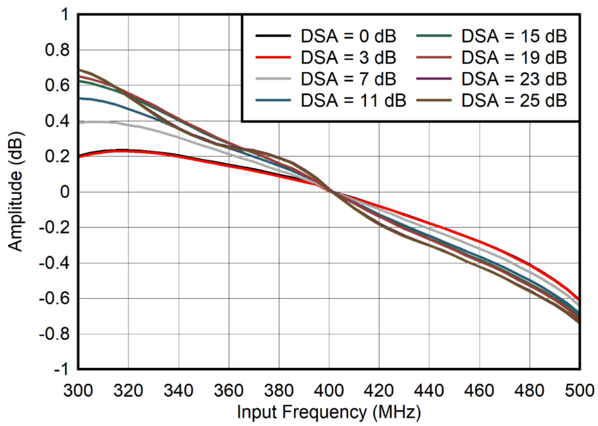


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-28. HD3 vs DSA Setting at 30 MHz

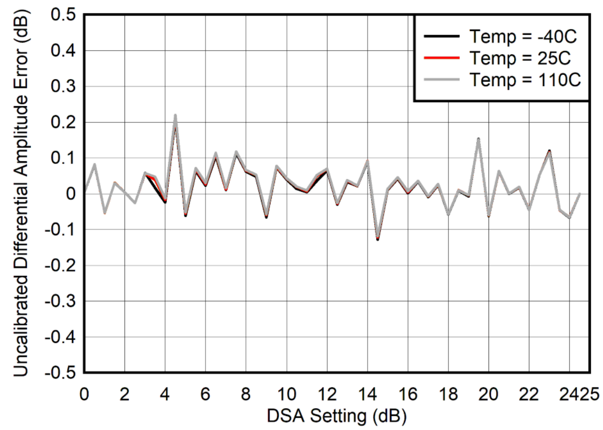
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



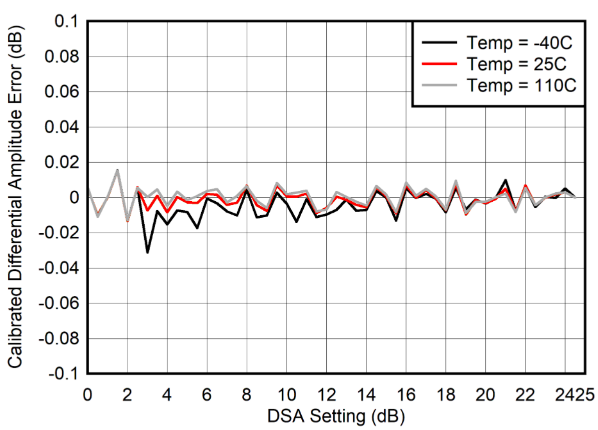
Normalized to 400 MHz

図 6-29. RX In-Band Gain Flatness, f_{IN} = 400 MHz



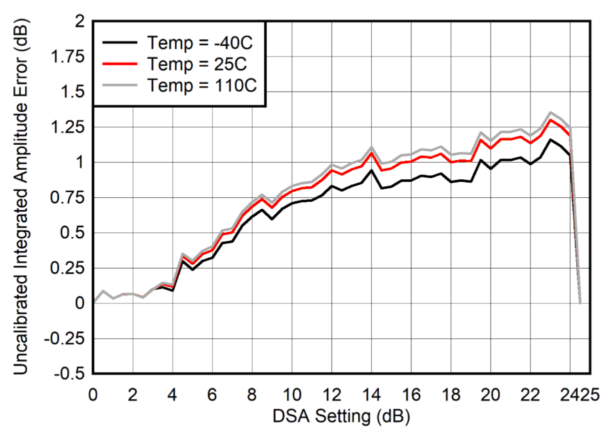
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz

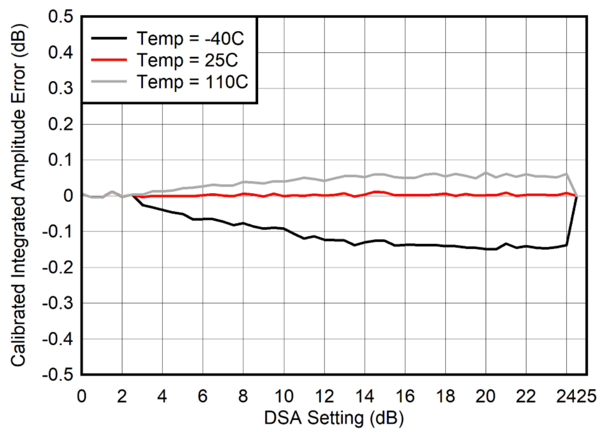


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

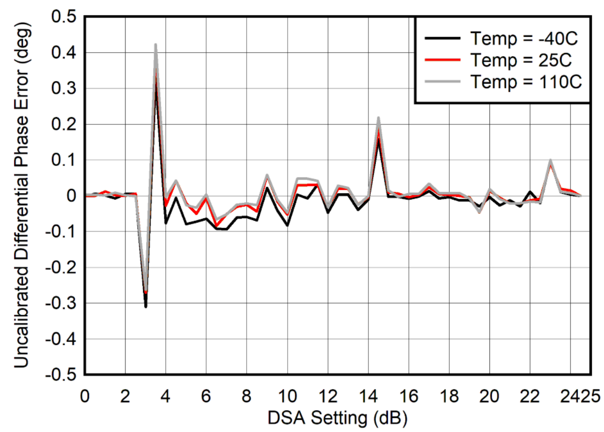
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



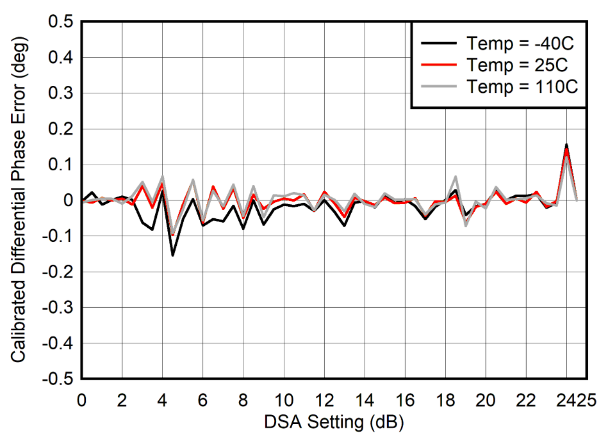
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



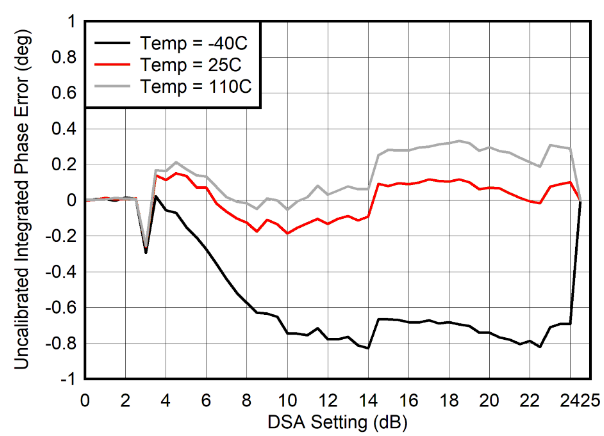
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz

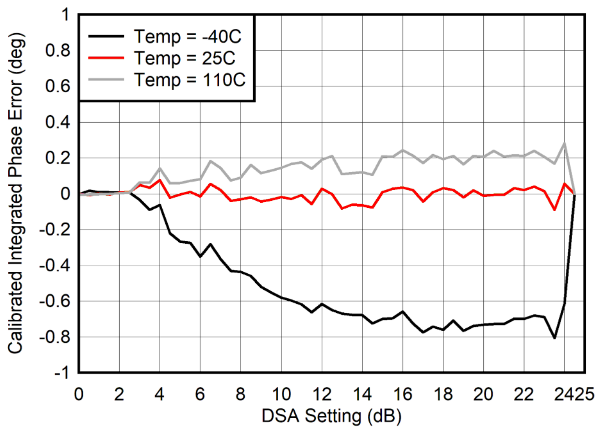


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz

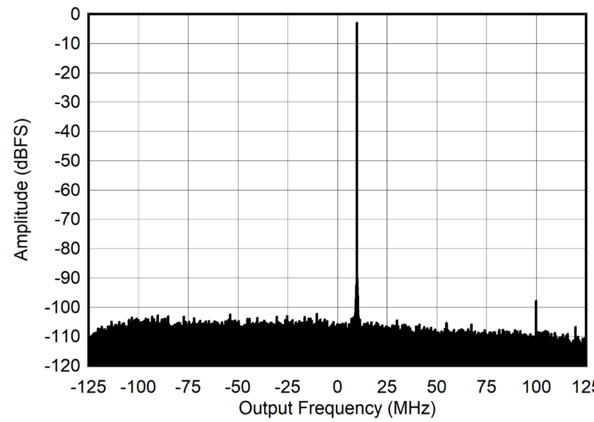
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



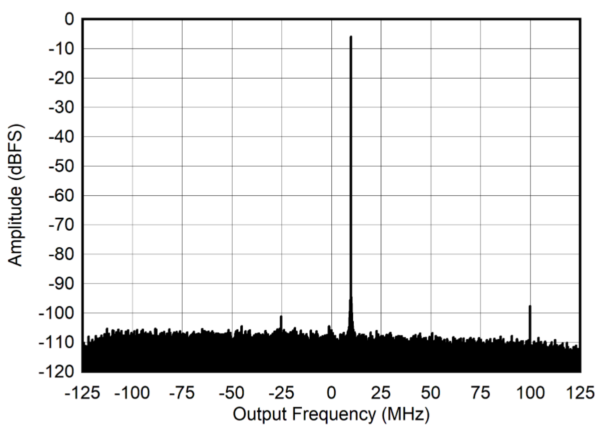
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz



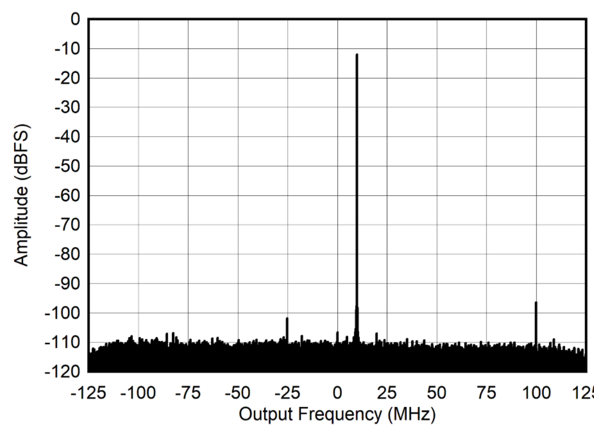
f_{NCO} = 400MHz

図 6-38. RX Output FFT at 405 MHz and -3dBFS



f_{NCO} = 400MHz

図 6-39. RX Output FFT at 405 MHz and -6dBFS

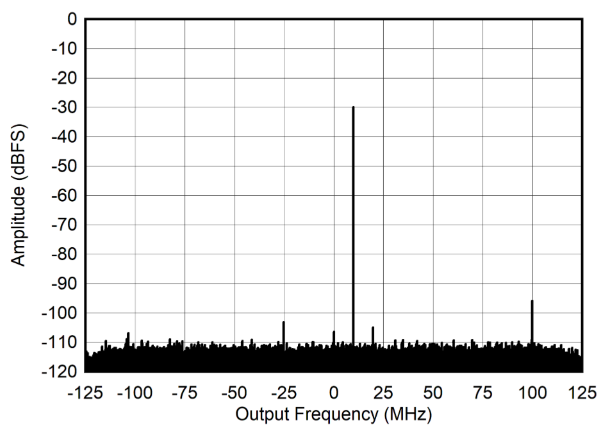


f_{NCO} = 400MHz

図 6-40. RX Output FFT at 405 MHz and -12dBFS

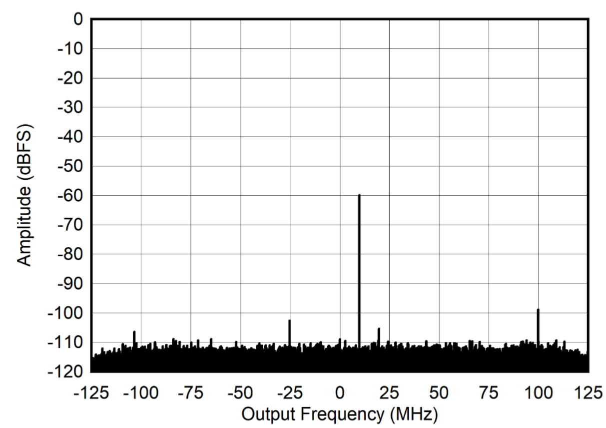
6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



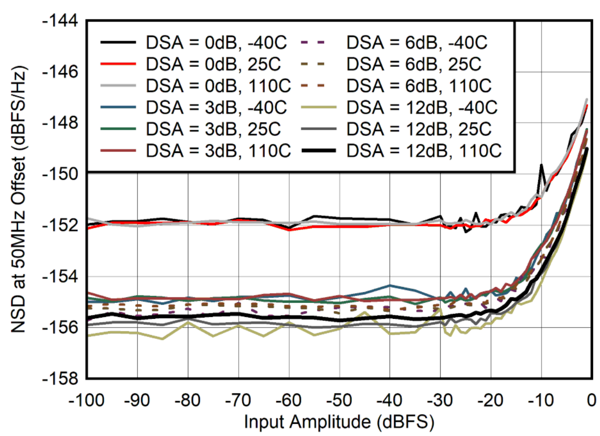
f_{NCO} = 400MHz

図 6-41. RX Output FFT at 405 MHz and -30dBFS



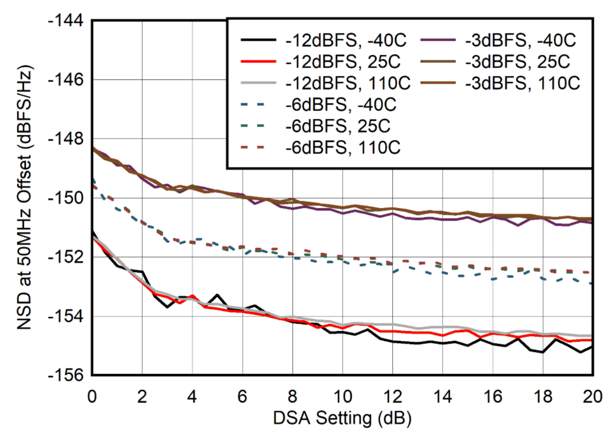
f_{NCO} = 400MHz

図 6-42. RX Output FFT at 405 MHz and -60dBFS



f_{OFFSET} = 50MHz

図 6-43. NSD vs Input Amplitude at 400MHz



f_{OFFSET} = 50MHz

図 6-44. NSD vs DSA Setting at 400MHz

6.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.

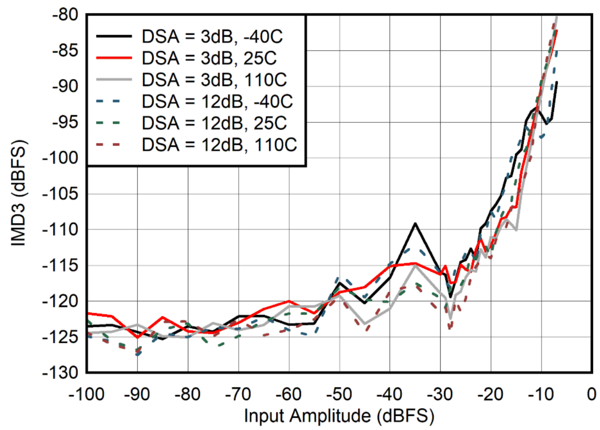


図 6-45. IMD3 vs Input Amplitude at 400MHz

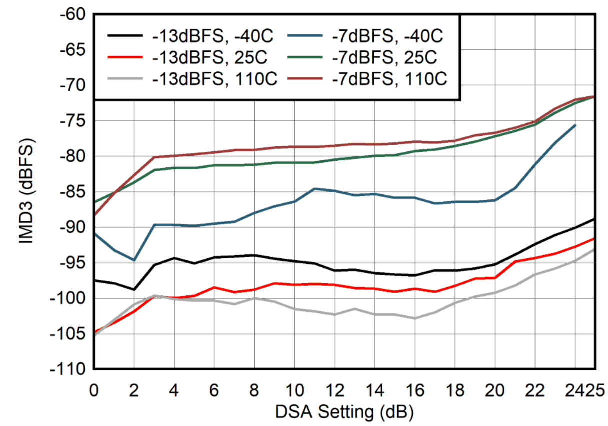


図 6-46. IMD3 vs DSA Setting at 400MHz

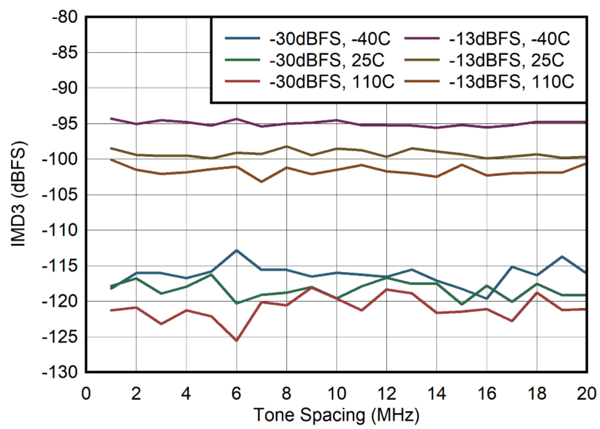


図 6-47. IMD3 vs Tone Spacing at 400MHz

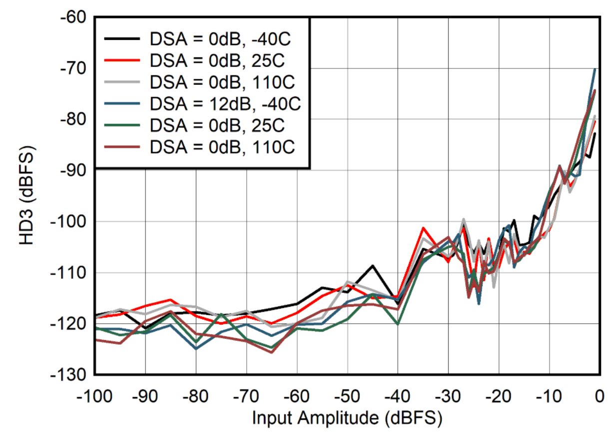


図 6-48. HD3 vs Input Amplitude at 400MHz

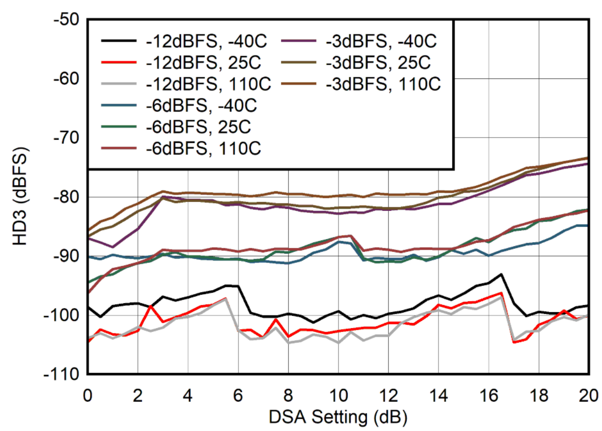
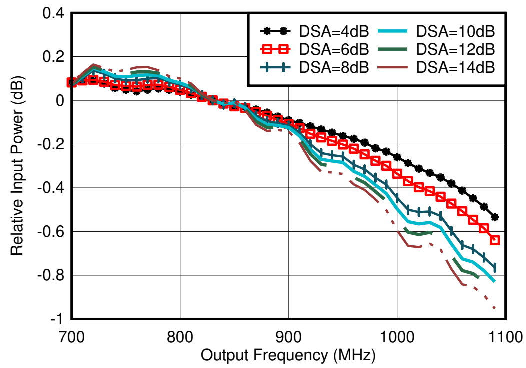


図 6-49. HD3 vs DSA Setting at 400MHz

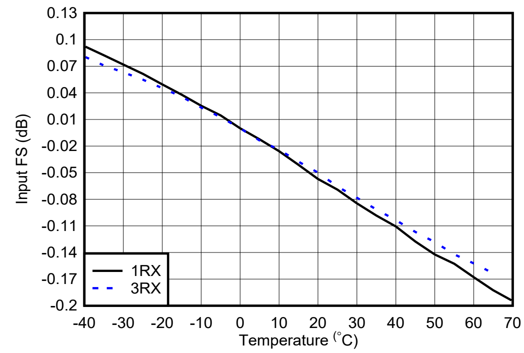
6.12.2 RX Typical Characteristics at 800 MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



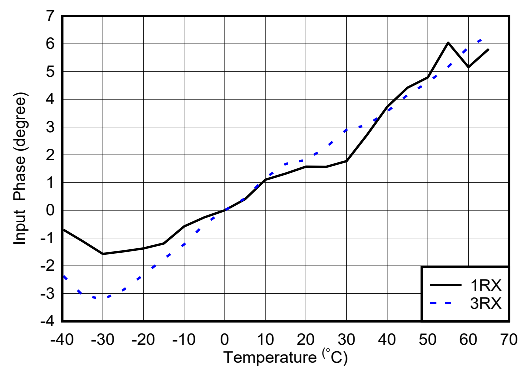
With 0.8 GHz matching, normalized to 830 MHz

図 6-50. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz



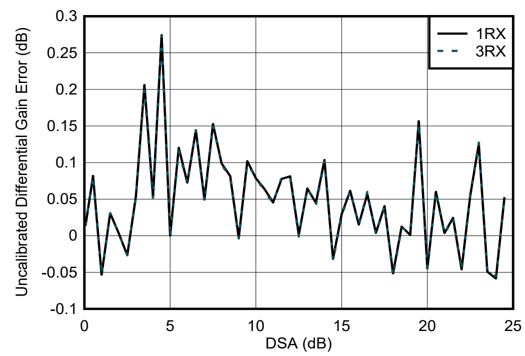
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

図 6-51. RX Input Fullscale vs Temperature and Channel at 800 MHz



With 0.8 GHz matching, normalized to phase at 25°C

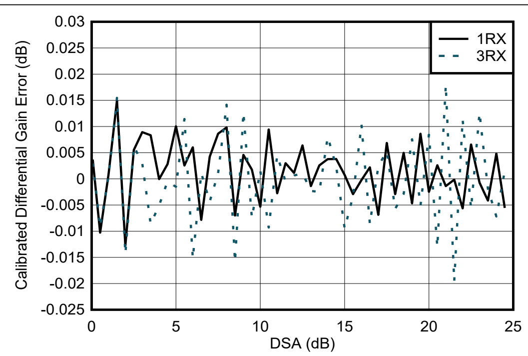
図 6-52. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

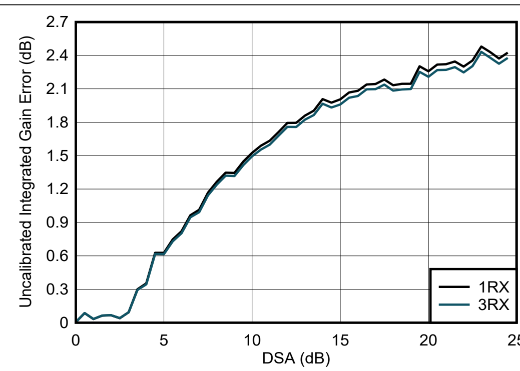
図 6-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



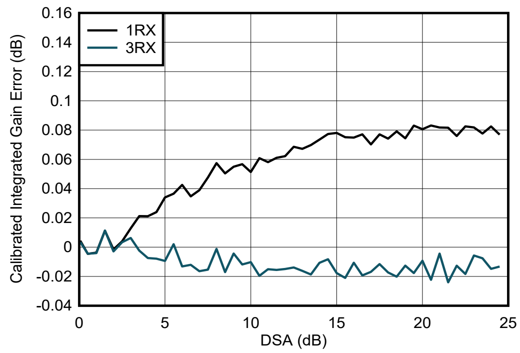
With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

6.12.2 RX Typical Characteristics at 800 MHz (continued)

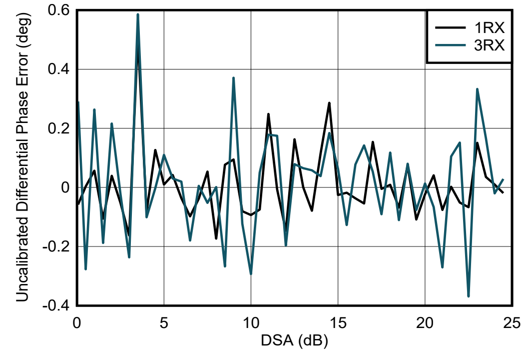
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

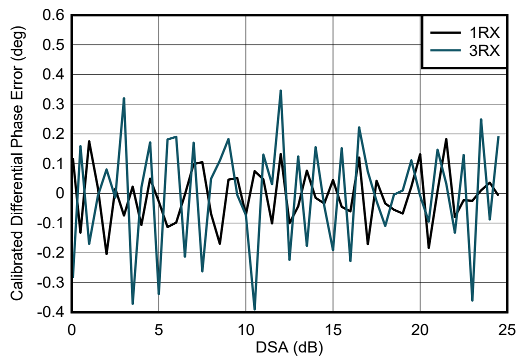
図 6-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

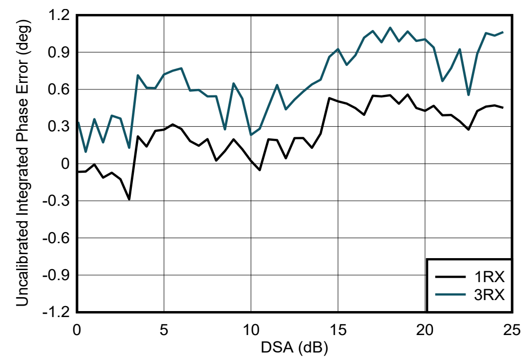
図 6-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

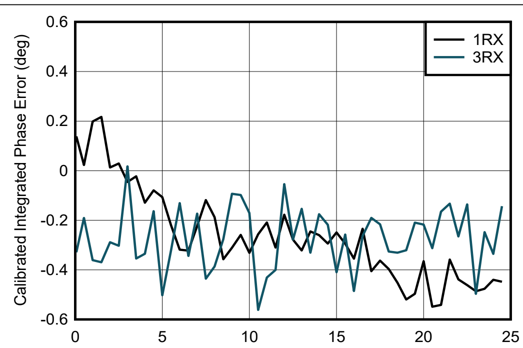
図 6-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

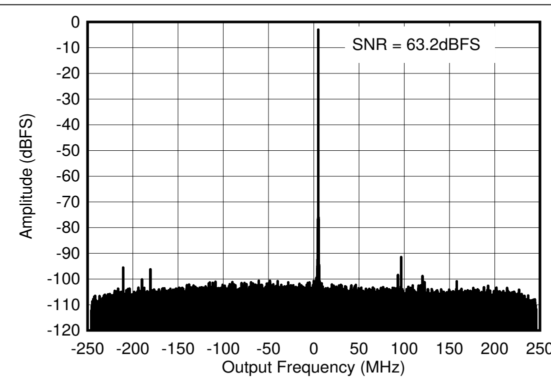
図 6-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

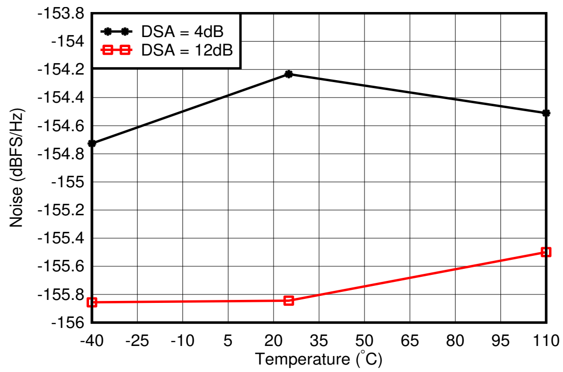


With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

図 6-61. RX Output FFT at 0.8 GHz

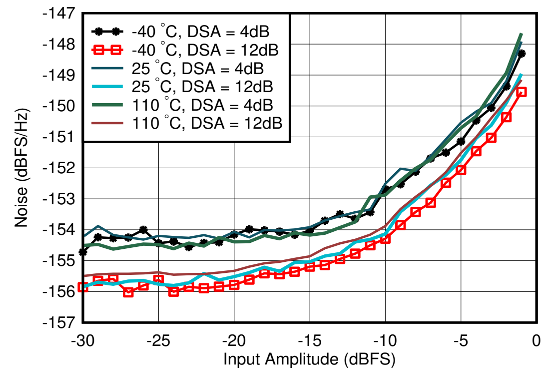
6.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



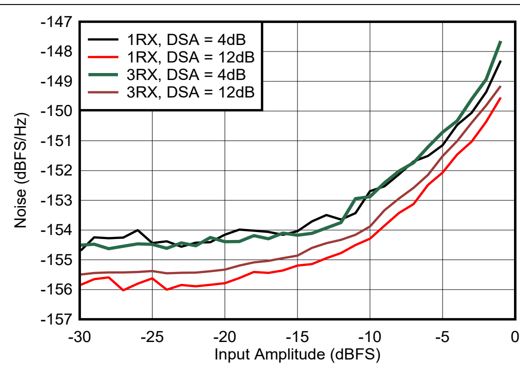
With 0.8 GHz matching, 12.5-MHz offset from tone

図 6-62. RX Noise Spectral Density vs Temperature at 0.8 GHz



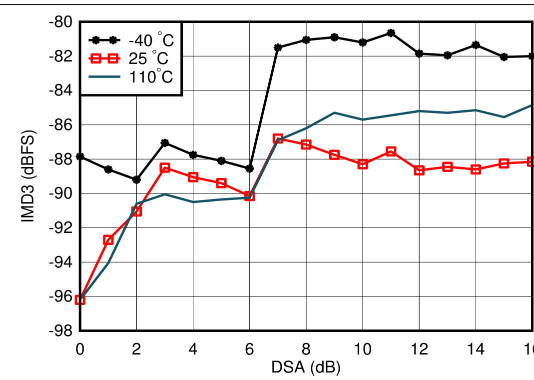
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



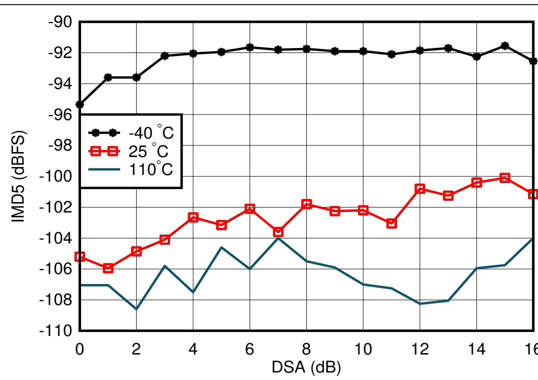
With 0.8 GHz matching, 12.5-MHz offset from tone

図 6-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



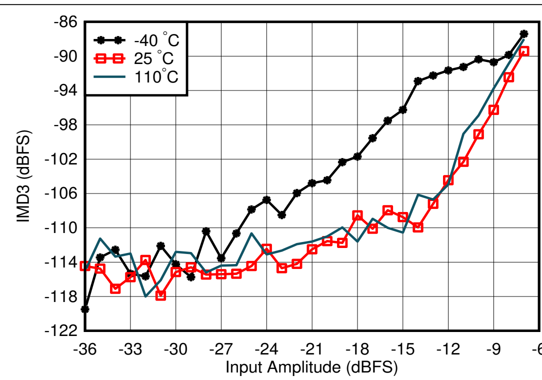
A. With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz

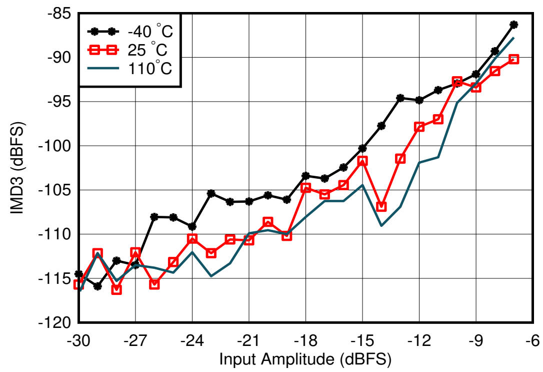


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz

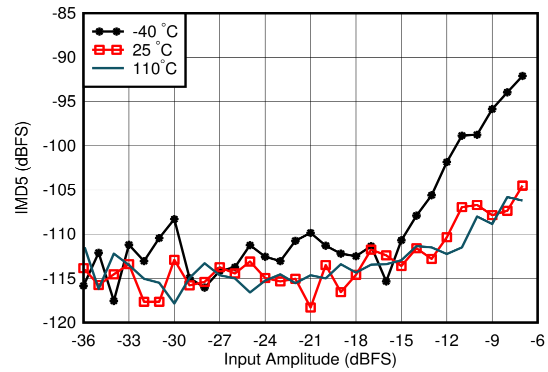
6.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



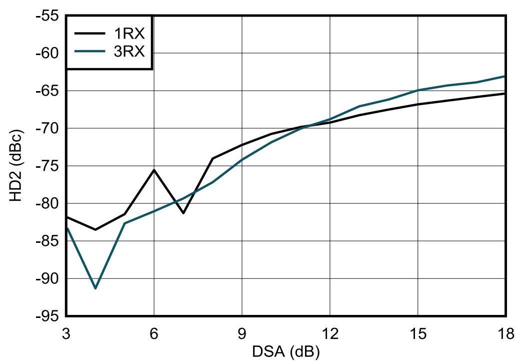
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



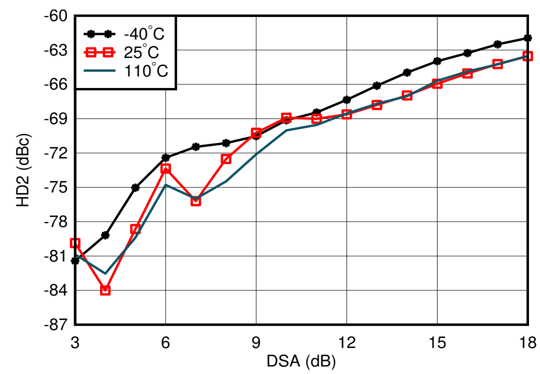
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



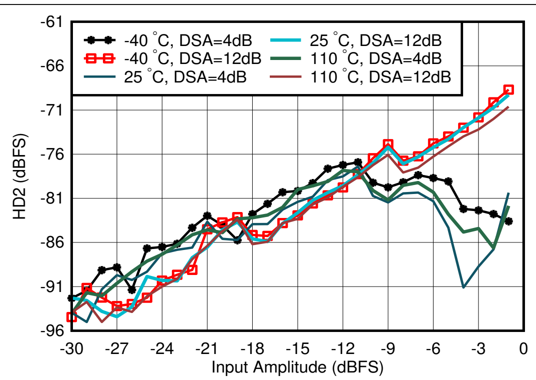
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz



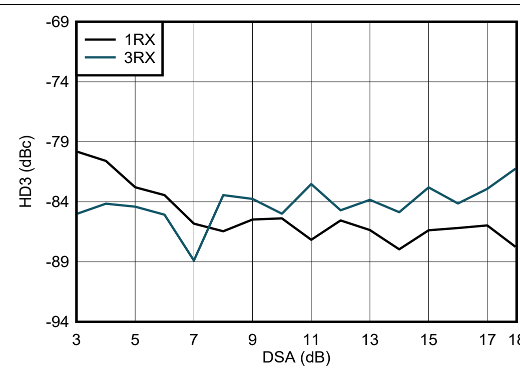
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-72. RX HD2 vs Input Level and Temperature at 0.8 GHz

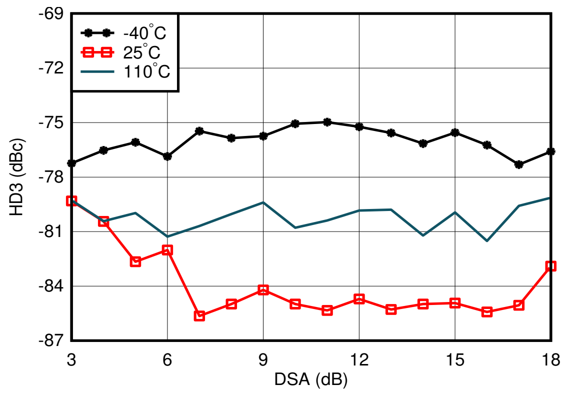


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz

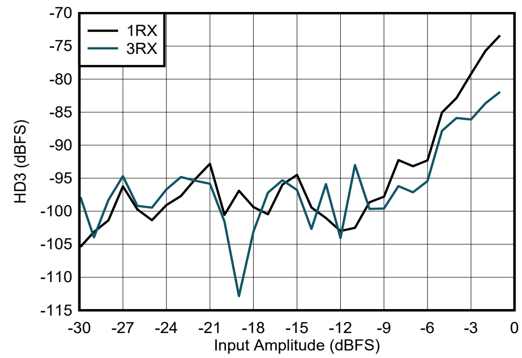
6.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



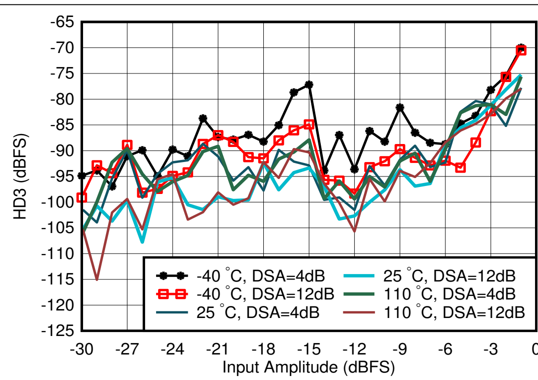
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



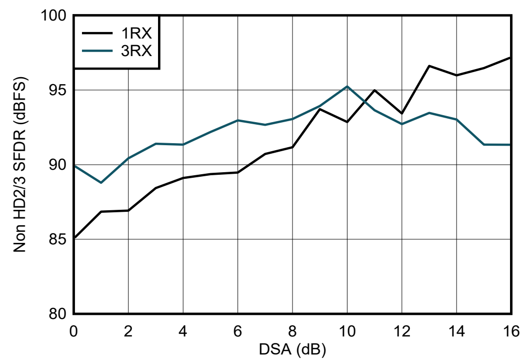
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-75. RX HD3 vs Input Level and Channel at 0.8 GHz



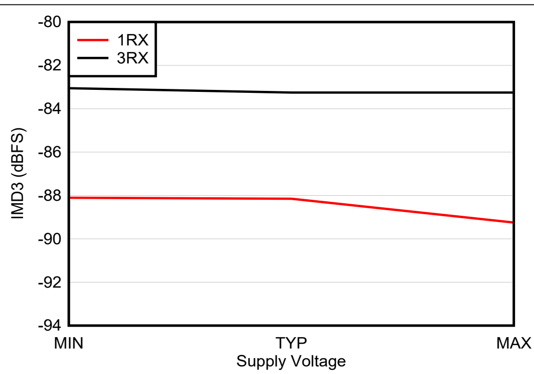
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-76. RX HD3 vs Input Level and Temperature at 0.8 GHz



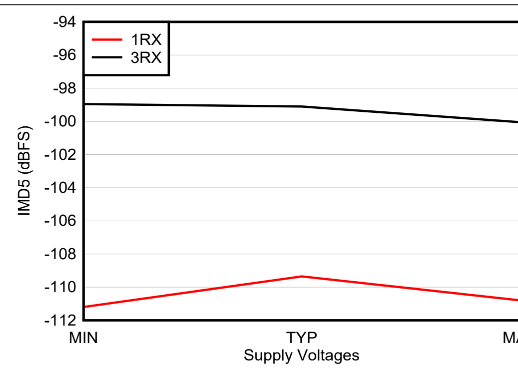
With 0.8 GHz matching

図 6-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-78. RX IMD3 vs Supply and Channel at 0.8 GHz

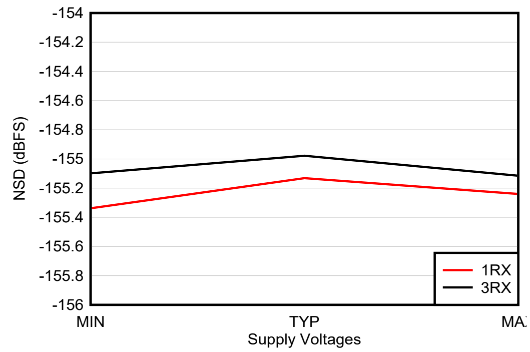


With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-79. RX IMD5 vs Supply and Channel at 0.8 GHz

6.12.2 RX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.

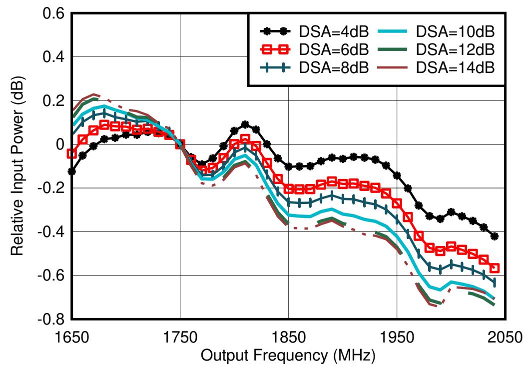


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

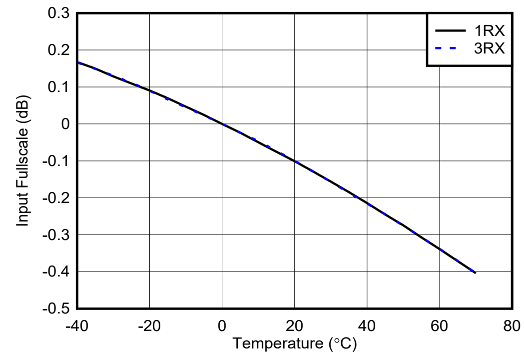
6.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



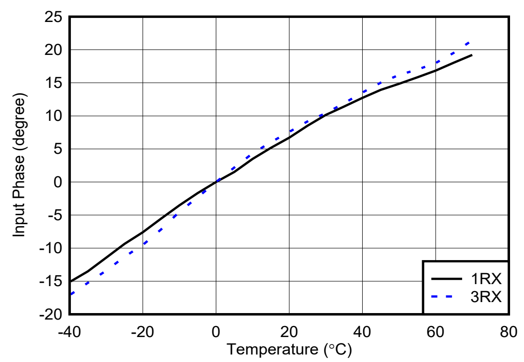
With 1.8 GHz matching, normalized to 1.75 GHz

図 6-81. RX In-Band Gain Flatness, f_{IN} = 1750 MHz



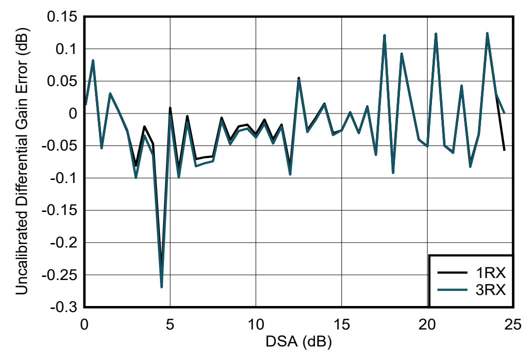
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

図 6-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 1.8 GHz matching, normalized to phase at 25°C

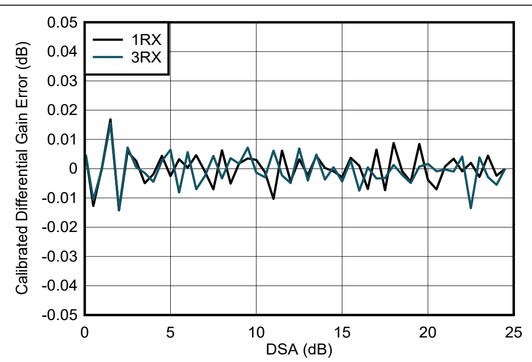
図 6-83. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

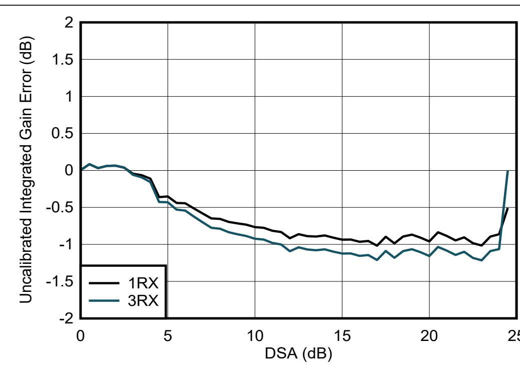
図 6-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

図 6-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



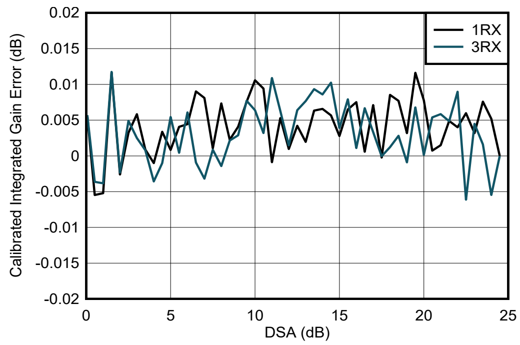
With 1.8 GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

図 6-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

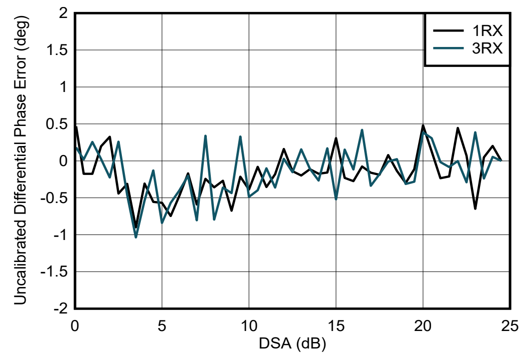
6.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



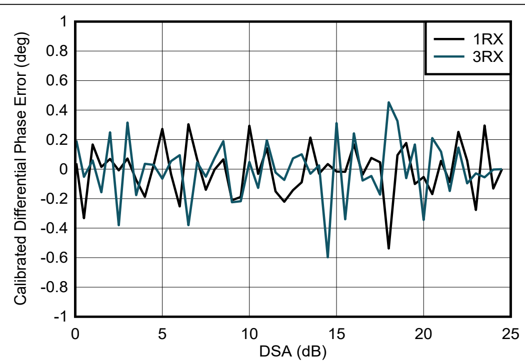
With 1.8 GHz matching
Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

図 6-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



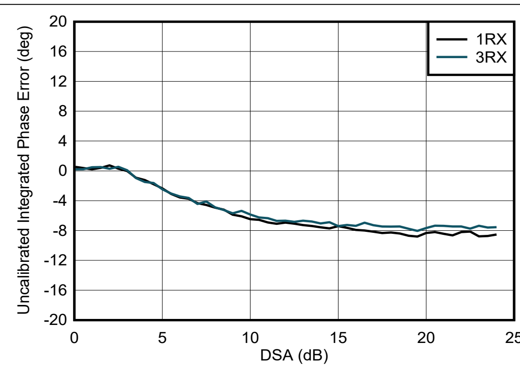
With 1.8 GHz matching
Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

図 6-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



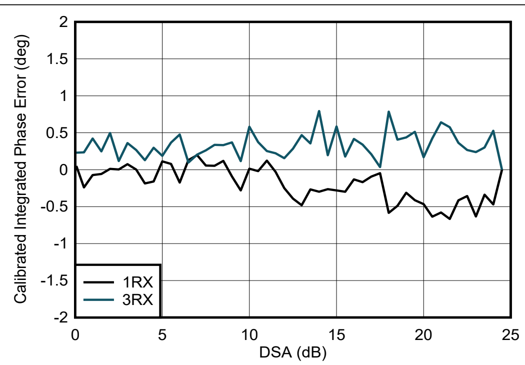
With 1.8 GHz matching
Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

図 6-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



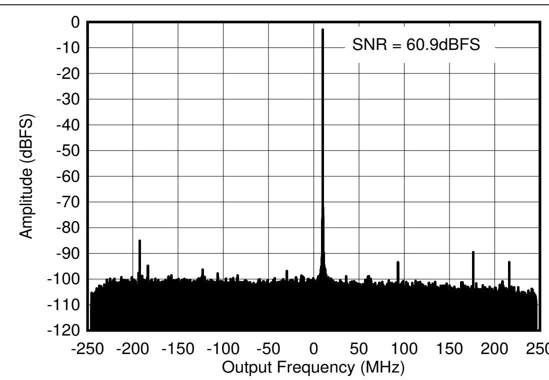
With 1.8 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching
Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

図 6-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

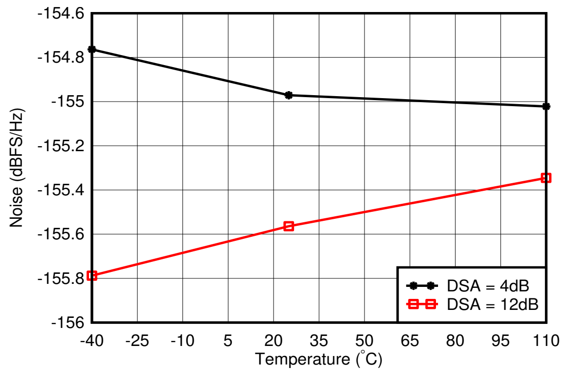


With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 6-92. RX Output FFT at 1.75 GHz

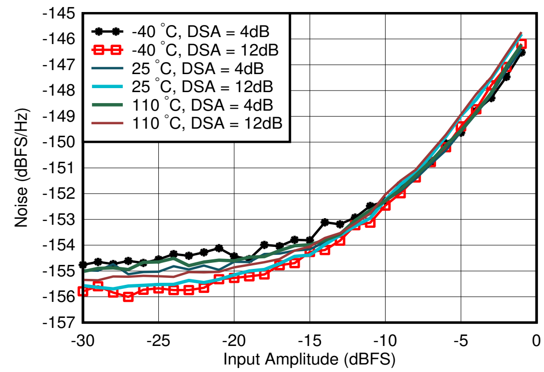
6.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



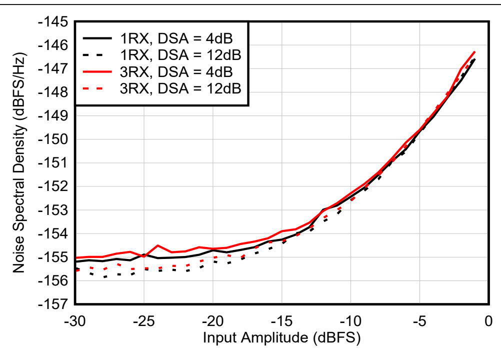
With 1.8 GHz matching, 12.5-MHz offset from tone

図 6-93. RX Noise Spectral Density vs Temperature at 1.75 GHz



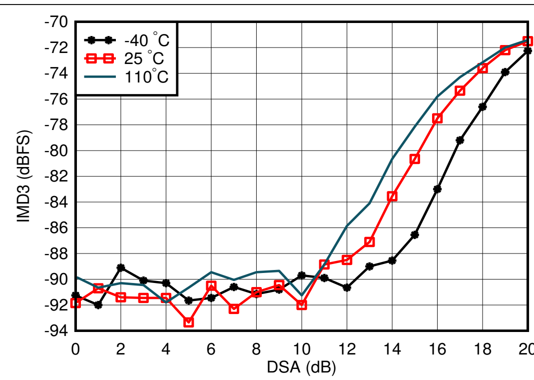
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



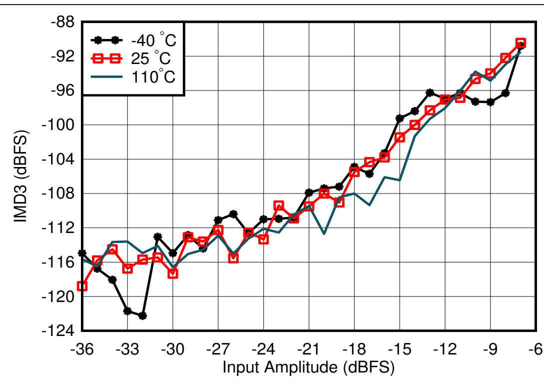
With 1.8 GHz matching, 12.5-MHz offset from tone

図 6-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



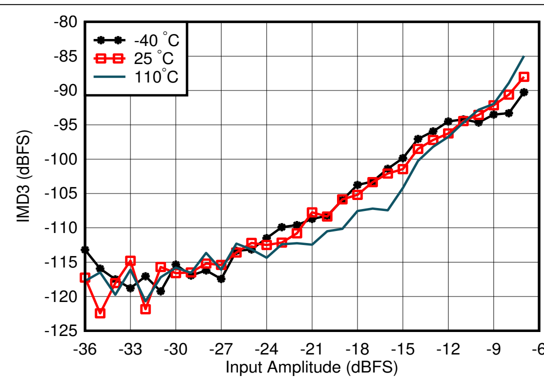
With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz

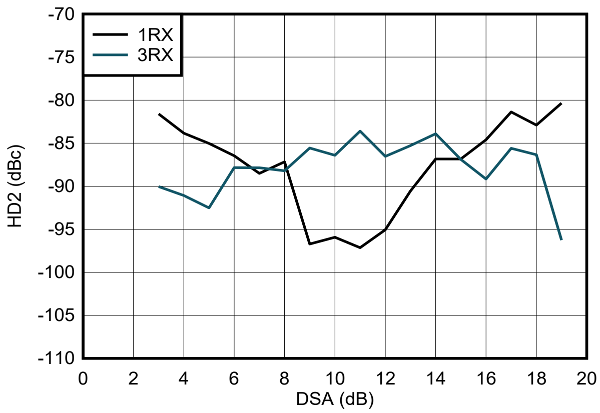


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz

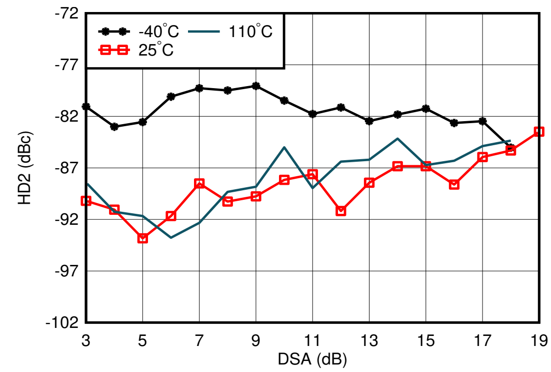
6.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



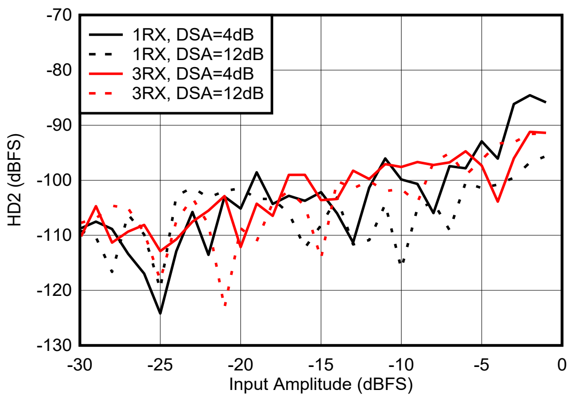
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



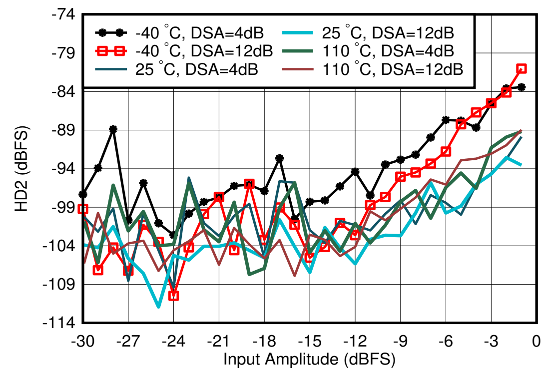
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



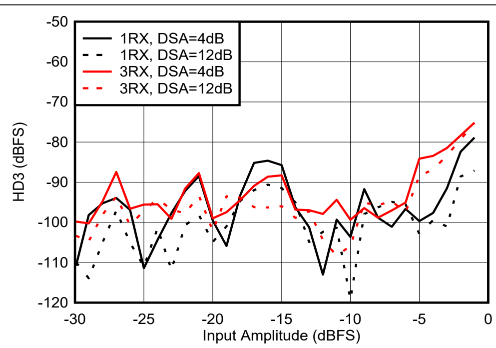
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



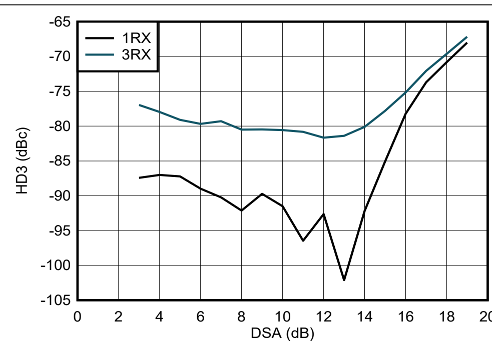
With 1.8 GHz matching, f_{in} = 1900 MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 6-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz

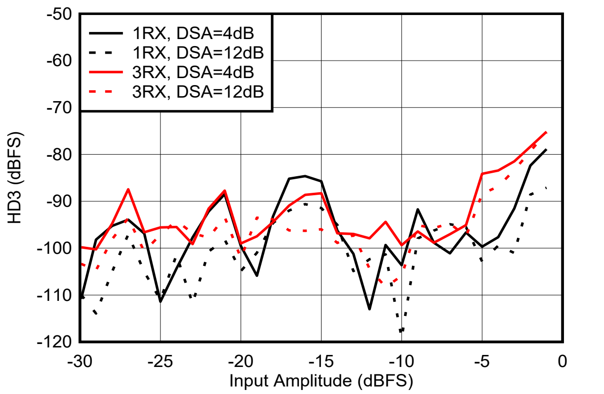


With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 6-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

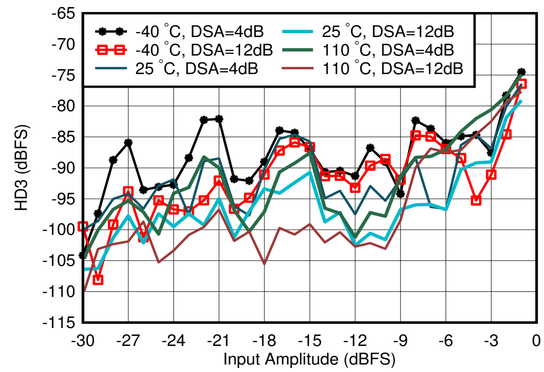
6.12.3 RX Typical Characteristics 1.75 GHz to 1.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



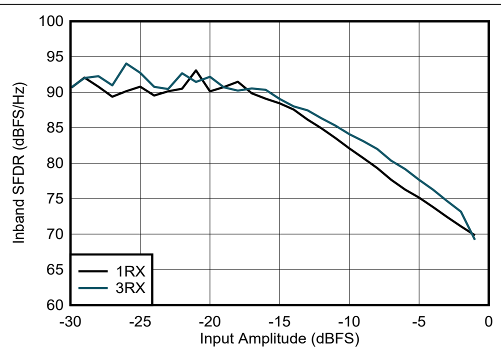
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 6-105. RX HD3 vs Input Level and Channel at 1.9 GHz



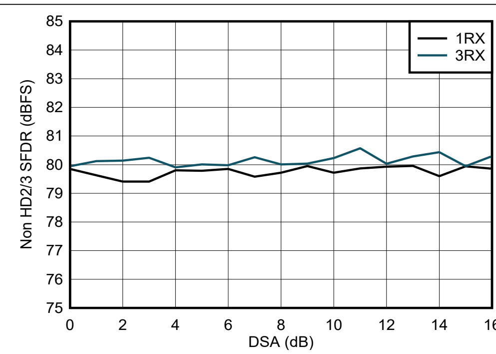
With 1.8 GHz matching, f_{in} = 1900 MHz, DDC bypass mode (TI only mode for characterization)

図 6-106. RX HD3 vs Input Level and Temperature at 1.9 GHz



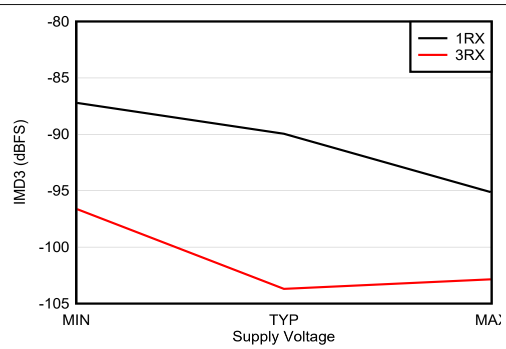
With 1.8 GHz matching, decimated by 3

図 6-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz



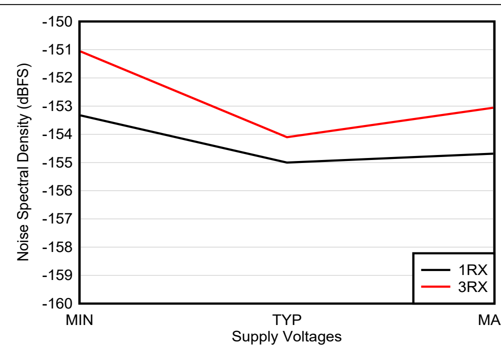
With 1.8 GHz matching

図 6-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-109. RX IMD3 vs Supply and Channel at 1.75 GHz

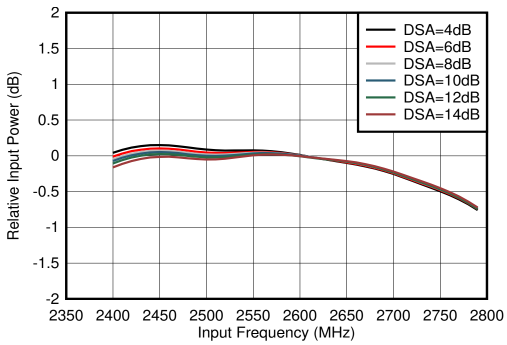


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

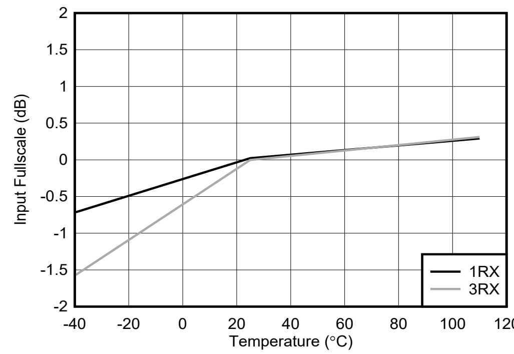
6.12.4 RX Typical Characteristics 2.6 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



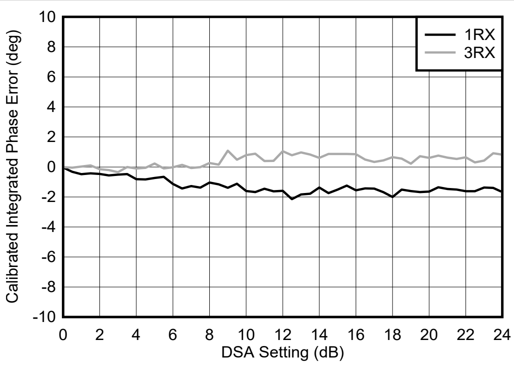
With matching, normalized to power at 2.6 GHz for each DSA setting

図 6-111. RX Inband Gain Flatness, f_{IN} = 2600 MHz



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

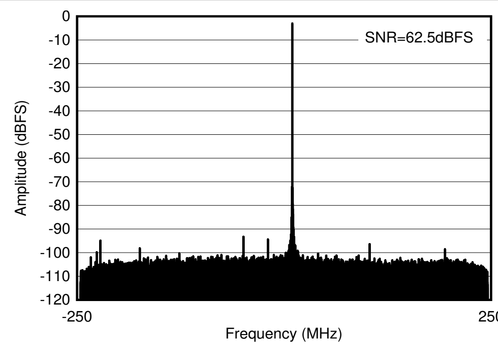
図 6-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

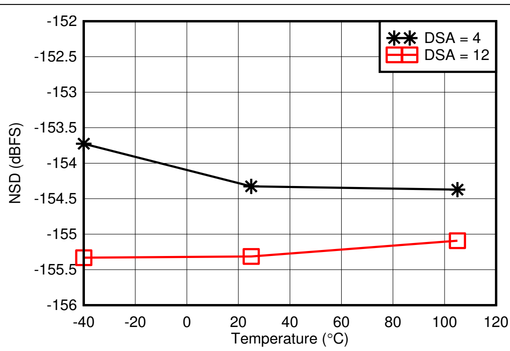
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



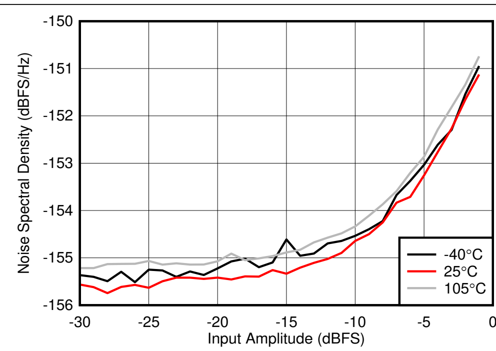
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 6-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

図 6-115. RX Noise Spectral Density vs Temperature at 2.6 GHz

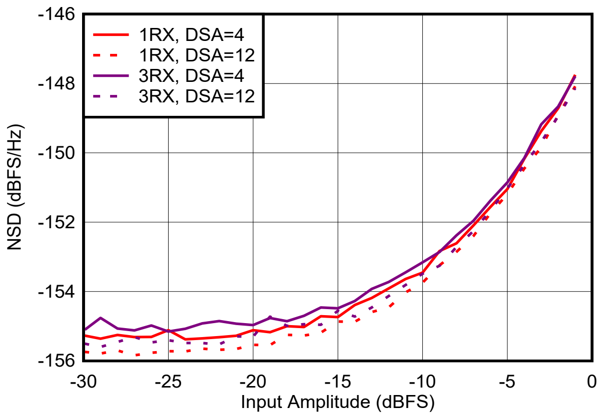


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

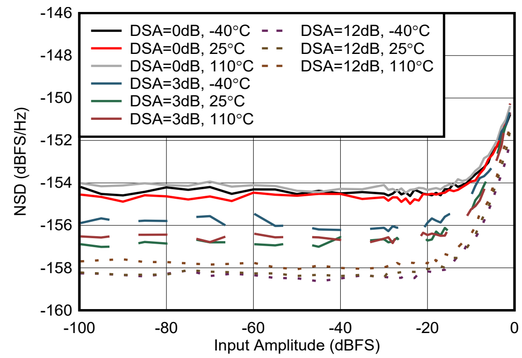
6.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



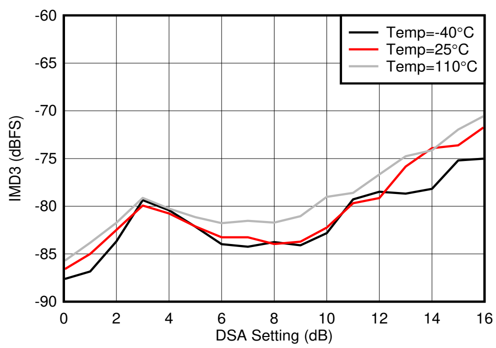
With 2.6 GHz matching, 12.5-MHz offset from tone

図 6-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



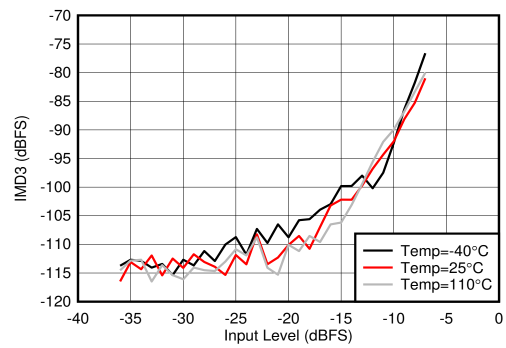
50-MHz offset from tone, external clock mode

図 6-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)



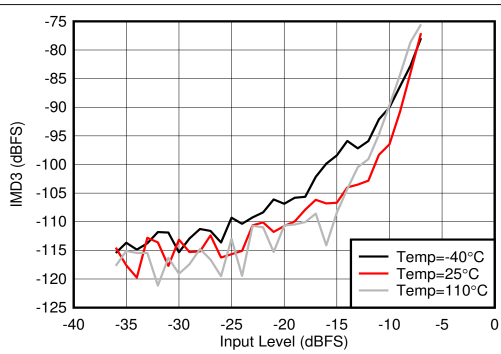
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



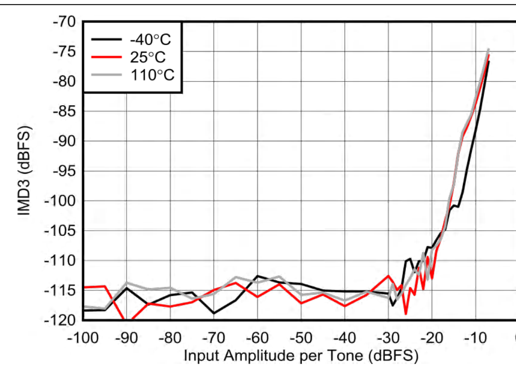
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz

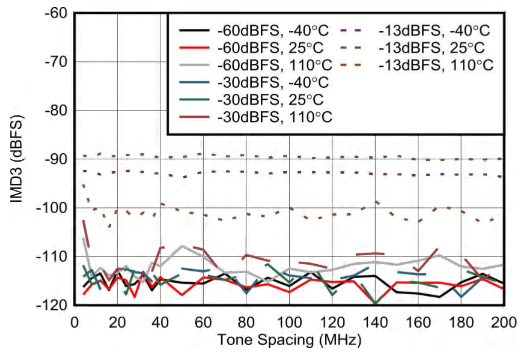


Tone spacing = 50 MHz, External clock mode

図 6-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

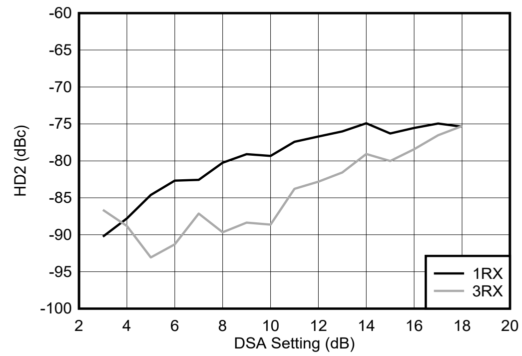
6.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



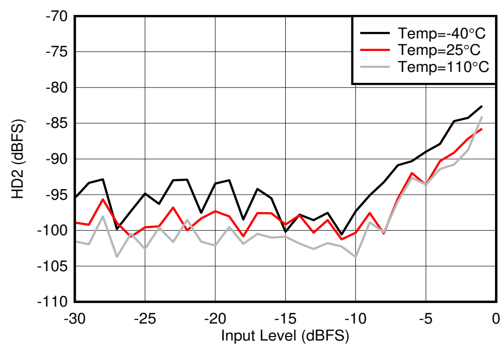
External clock mode

図 6-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



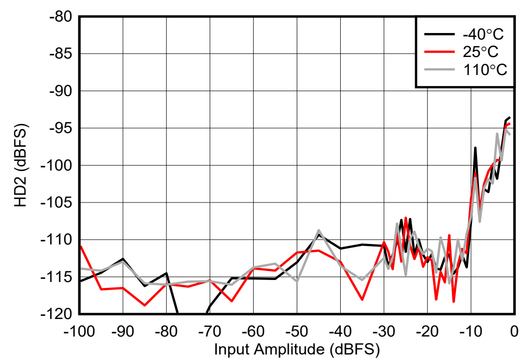
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



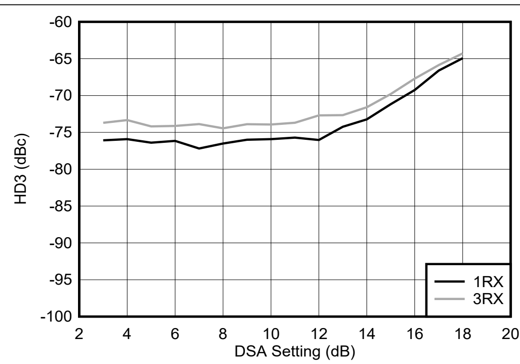
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



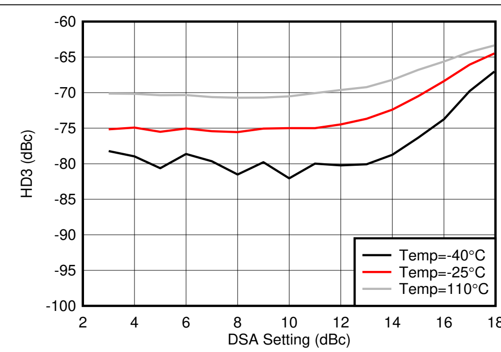
External clock mode

図 6-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz

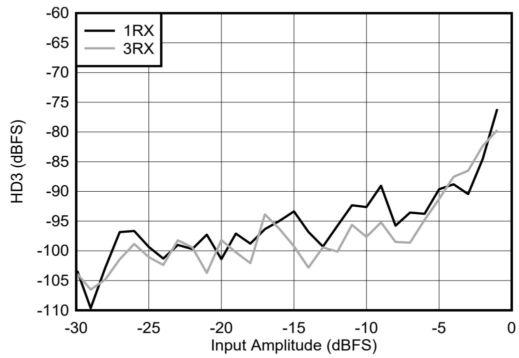


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

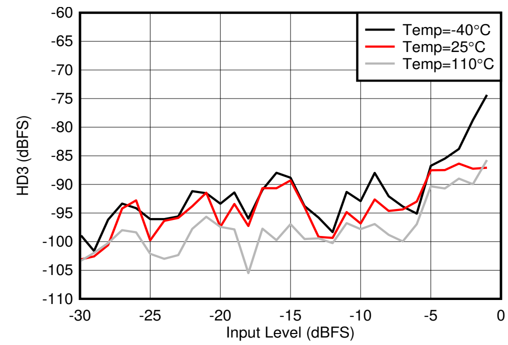
6.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



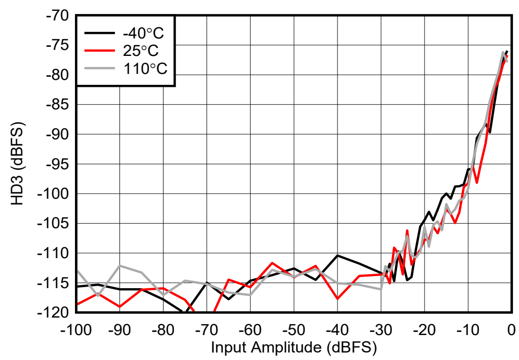
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-129. RX HD3 vs Input Level and Channel at 2.6 GHz



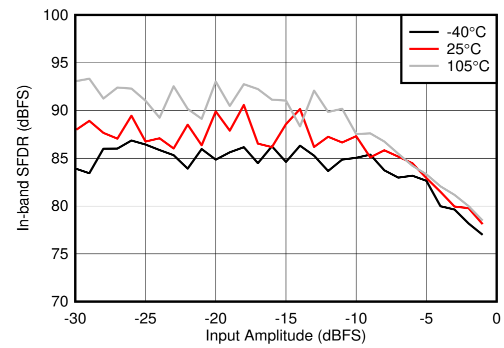
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-130. RX HD3 vs Input Level and Temperature at 2.6 GHz



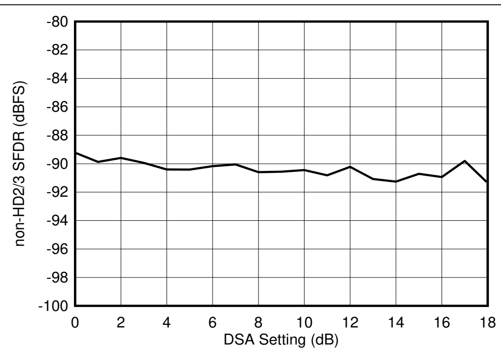
External clock mode

図 6-131. RX HD3 vs Input Level and Temperature at 2.6 GHz



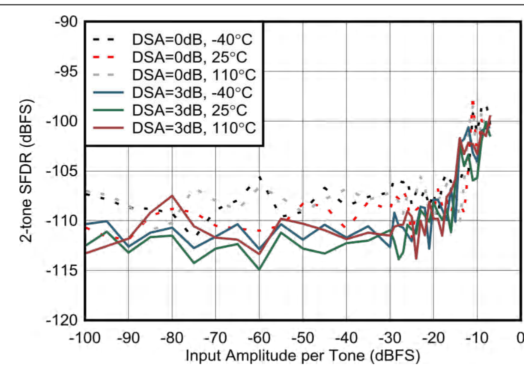
With 2.6 GHz matching, decimate by 4

図 6-132. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



With 2.6 GHz matching

図 6-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

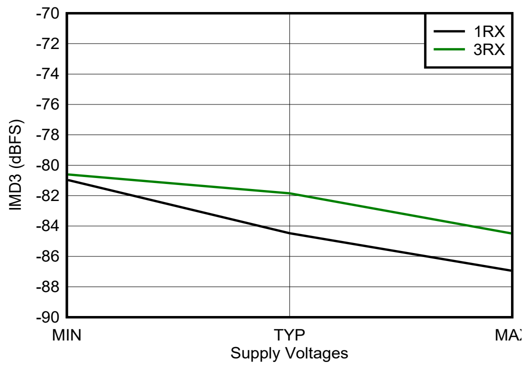


External clock mode, 50MHz tone spacing, excluding 3rd order distortion

図 6-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

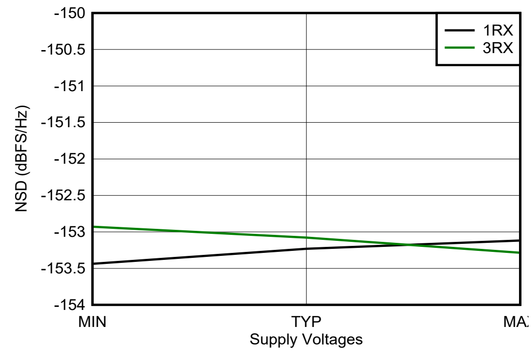
6.12.4 RX Typical Characteristics 2.6 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-135. RX IMD3 vs Supply and Channel at 2.6 GHz

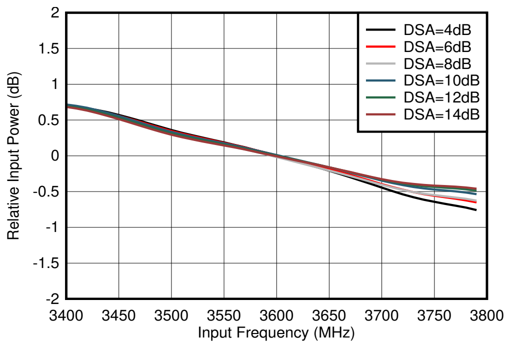


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

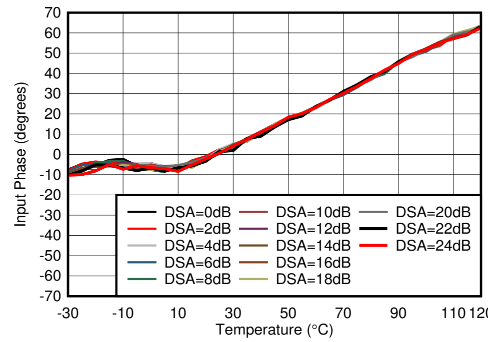
6.12.5 RX Typical Characteristics 3.5 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



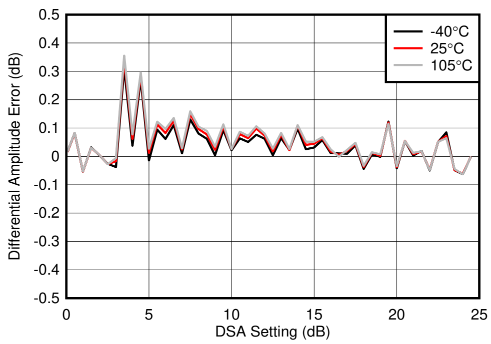
With 3.6 GHz matching, normalized to 3.6 GHz

図 6-137. RX In-Band Gain Flatness, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

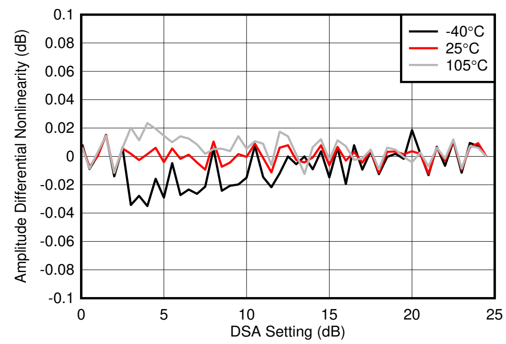
図 6-138. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

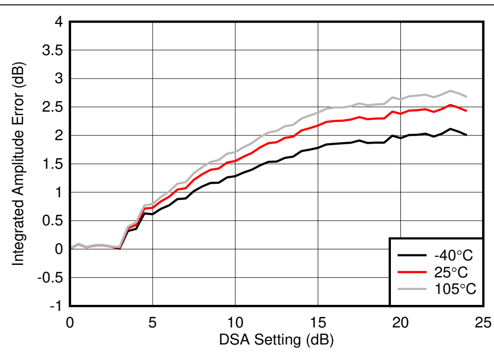
図 6-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

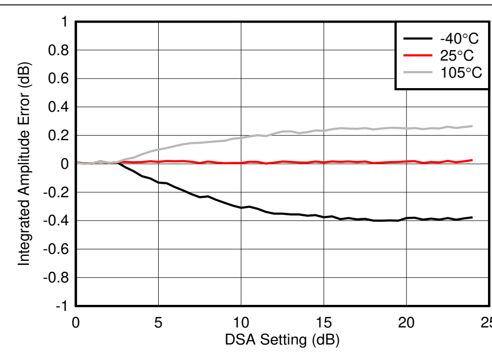
図 6-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



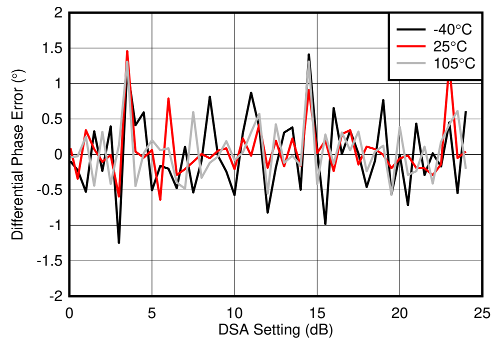
With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

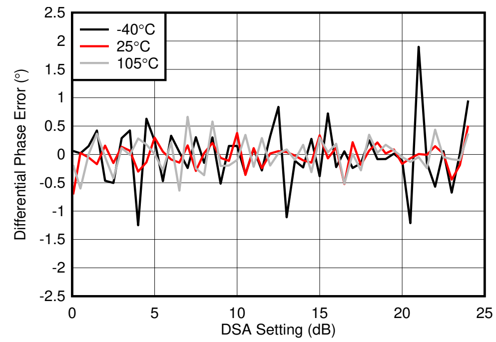
6.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



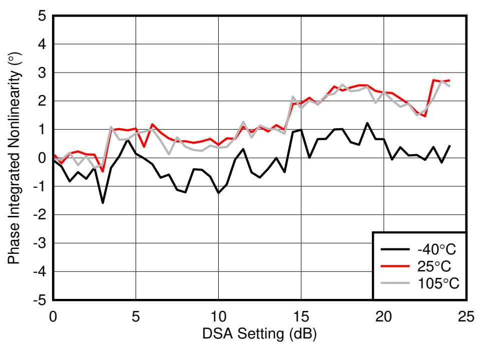
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



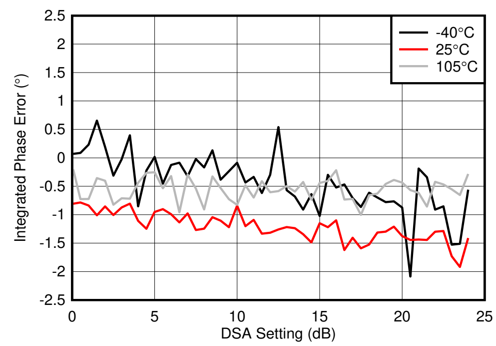
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



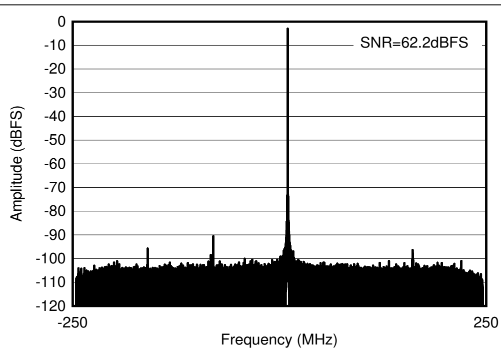
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



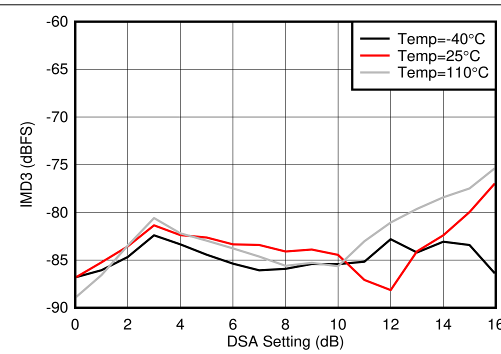
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

図 6-147. RX Output FFT at 3.6 GHz

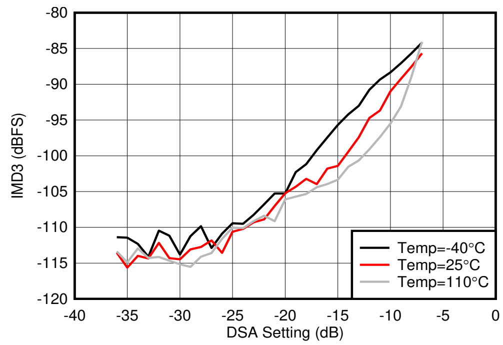


With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

図 6-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

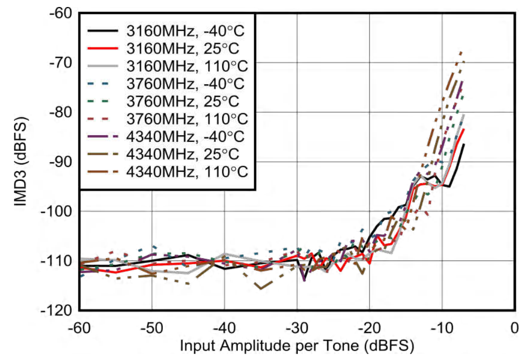
6.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



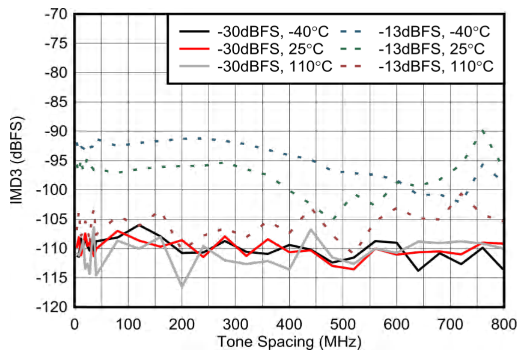
With 3.5 GHz matching, 20-MHz tone spacing

図 6-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



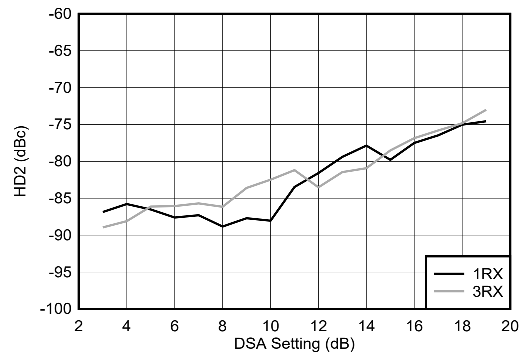
External clock mode, 20-MHz tone spacing, 2x Decimation

図 6-150. RX IMD3 vs Input Level



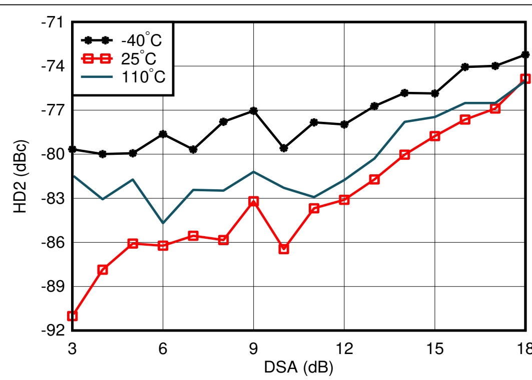
External clock mode, 2x Decimation

図 6-151. RX IMD3 vs Tone Spacing at 3.76 GHz



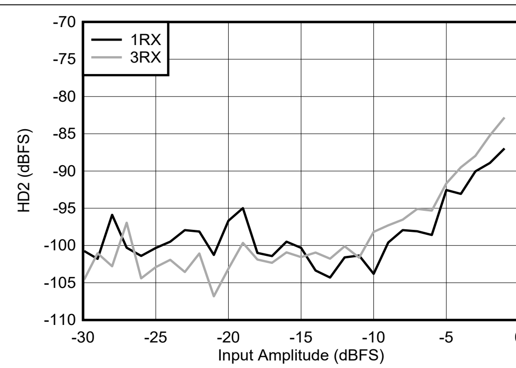
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

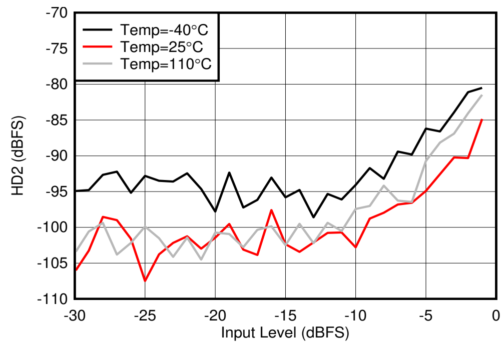


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-154. RX HD2 vs Input Level and Channel at 3.6 GHz

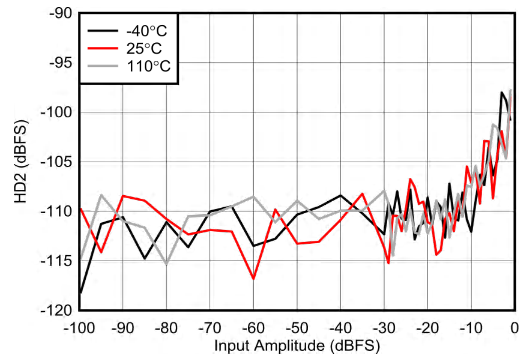
6.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



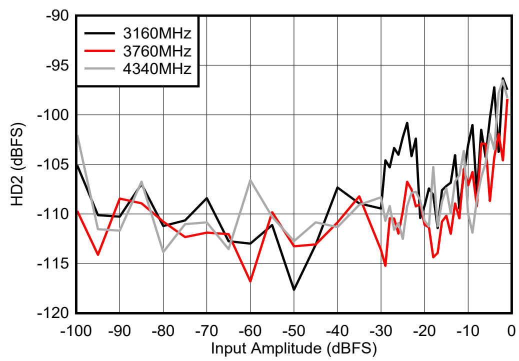
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



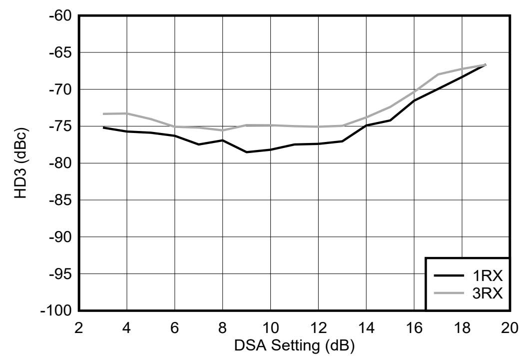
External clock mode, 2x Decimation

図 6-156. RX HD2 vs Input Level at 3.76 GHz



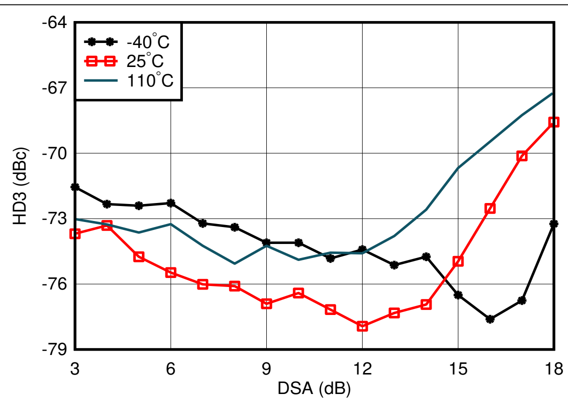
External clock mode, 25°C, 2x Decimation

図 6-157. RX HD2 vs Input Level



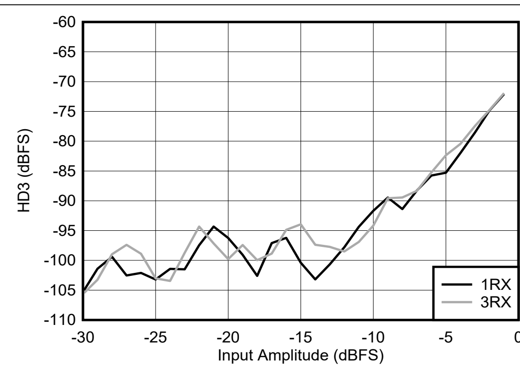
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz

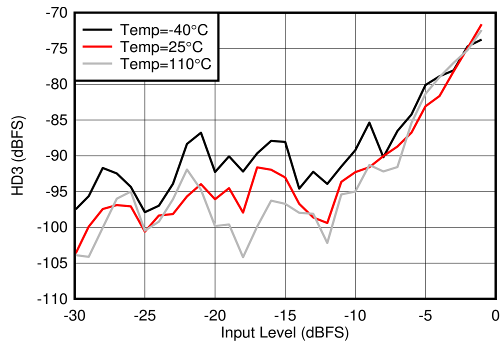


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-160. RX HD3 vs Input Level and Channel at 3.6 GHz

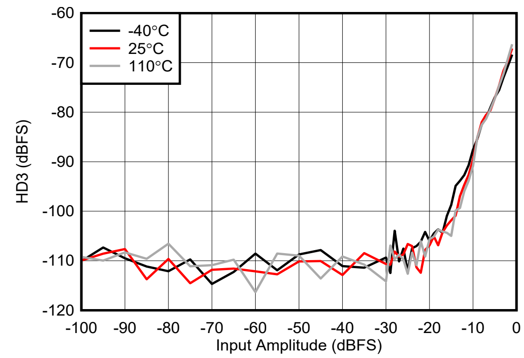
6.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



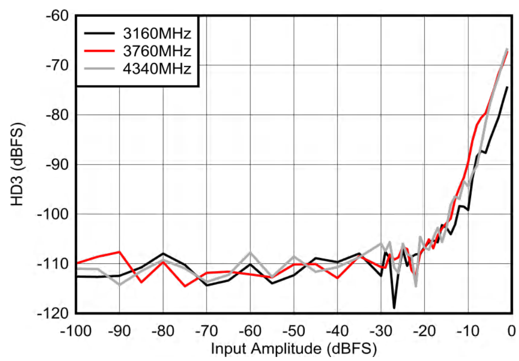
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



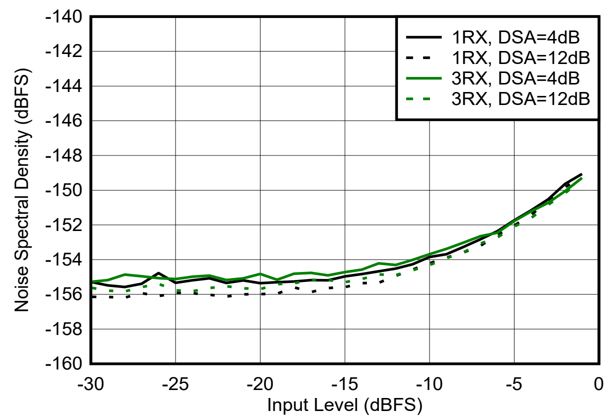
External clock mode, 2x Decimation

図 6-162. RX HD3 vs Input Level at 3.76GHz



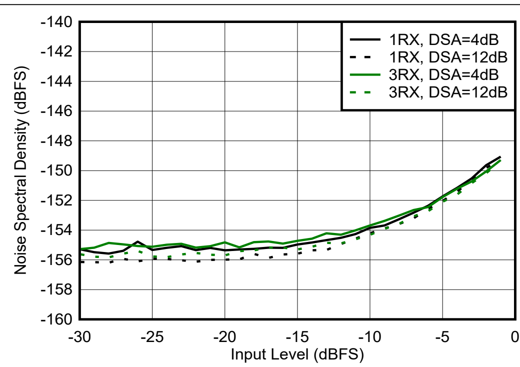
External clock mode, 25°C, 2x Decimation

図 6-163. RX HD3 vs Input Level



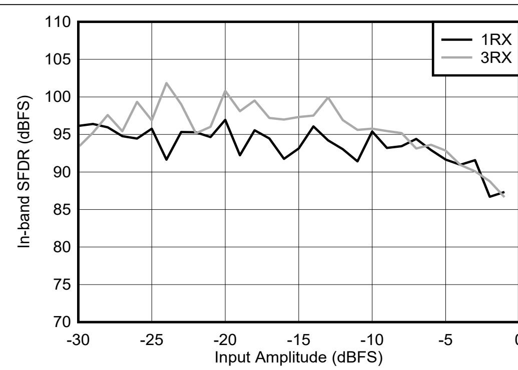
With 3.5 GHz matching, 12.5-MHz offset from tone

図 6-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

図 6-165. RX Noise Spectral Density vs Input Level at 3.76 GHz

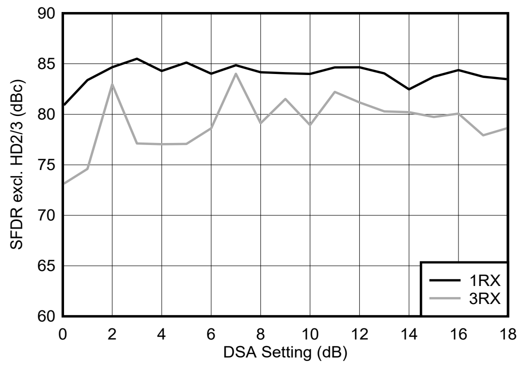


With 3.5 GHz matching

図 6-166. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

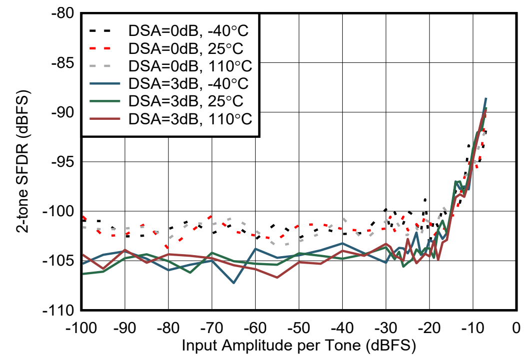
6.12.5 RX Typical Characteristics 3.5 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



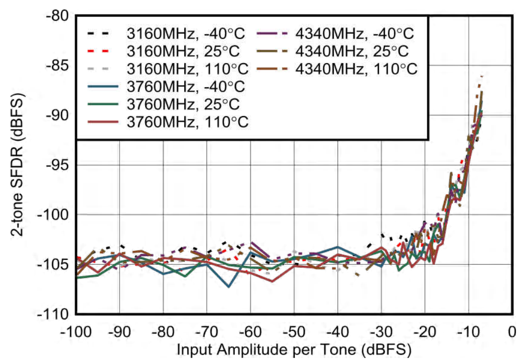
With 3.5 GHz matching

図 6-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



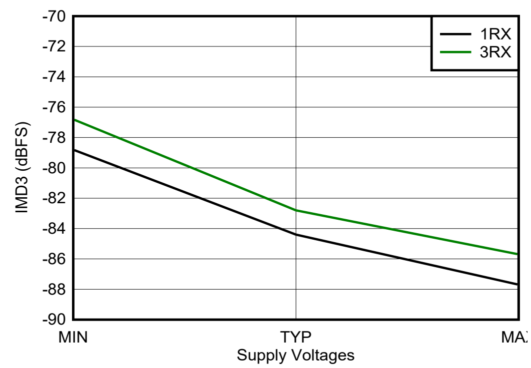
External clock mode, 20 MHz tone spacing, excluding 3rd order distortion

図 6-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



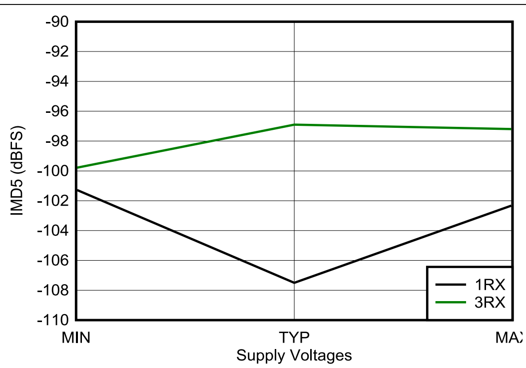
External clock mode, 20 MHz tone spacing, excluding 3rd order distortion

図 6-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz



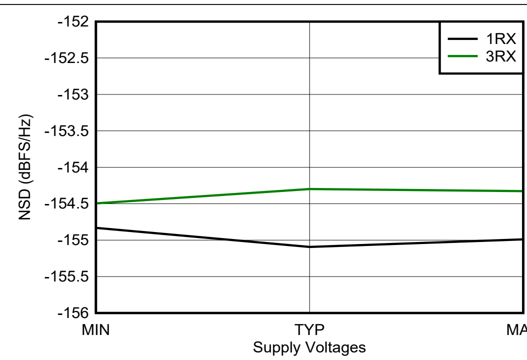
With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

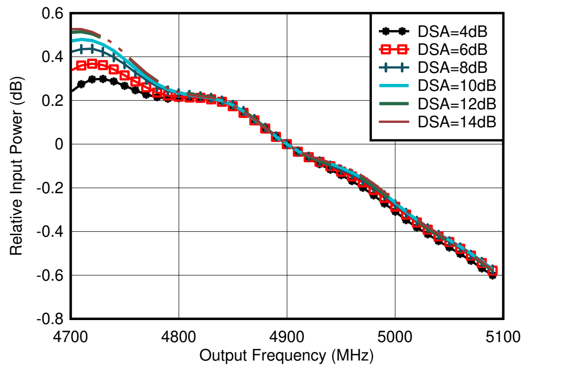


With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

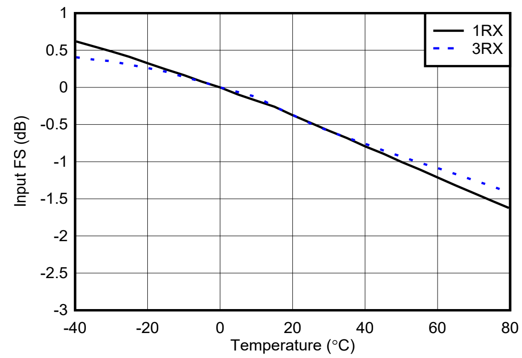
6.12.6 RX Typical Characteristics 4.9 GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



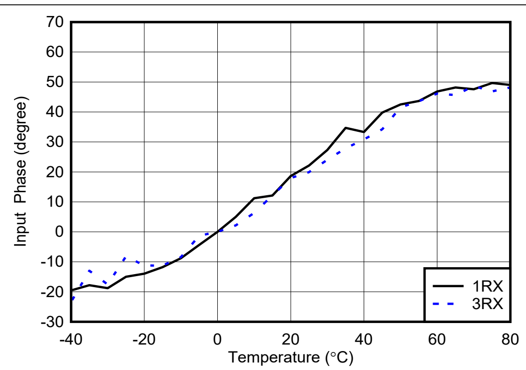
With matching, normalized to power at 4.9GHz for each DSA setting

図 6-173. RX Inband Gain Flatness, f_{IN} = 4900 MHz



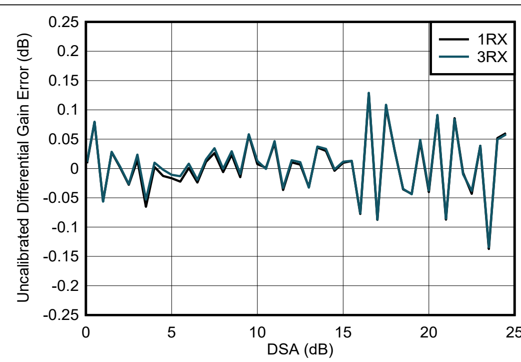
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

図 6-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

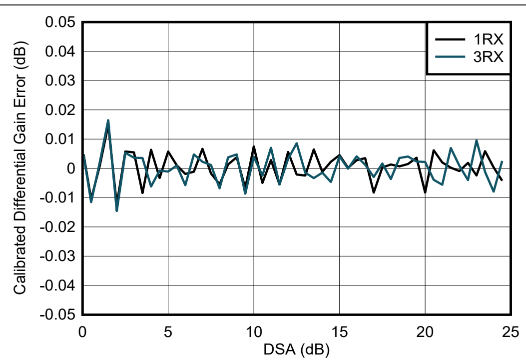
図 6-175. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

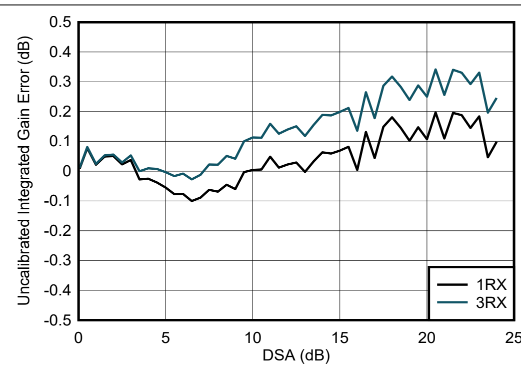
図 6-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN} (DSA Setting – 1) – P_{IN} (DSA Setting) + 1

図 6-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



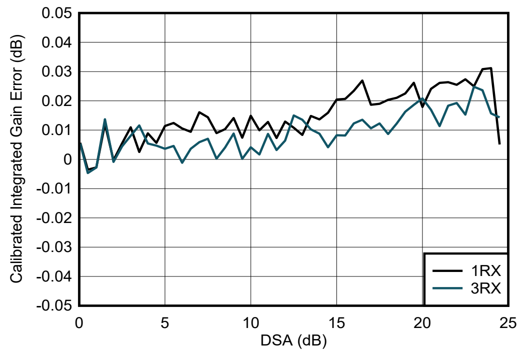
With 4.9 GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

図 6-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

6.12.6 RX Typical Characteristics 4.9 GHz (continued)

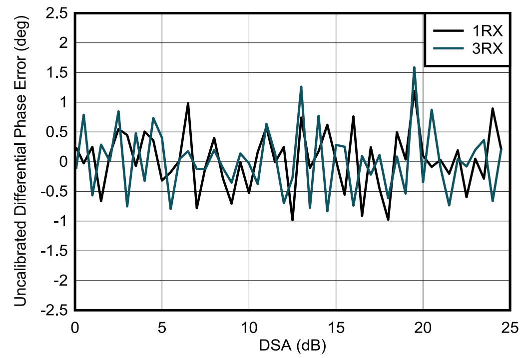
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN} (DSA Setting) – P_{IN} (DSA Setting = 0) + (DSA Setting)

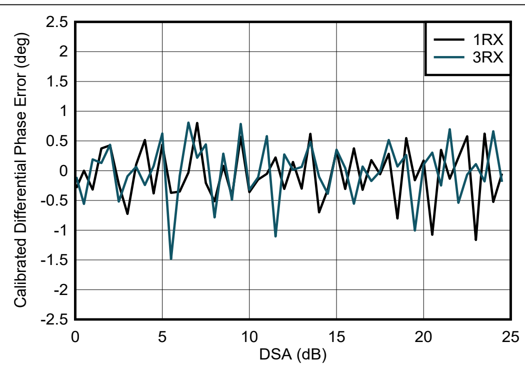
図 6-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

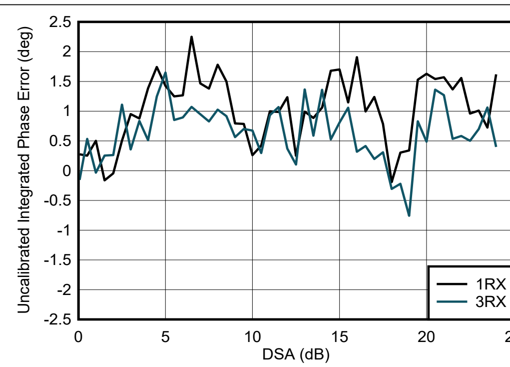
図 6-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$ (DSA Setting – 1) – $Phase_{IN}$ (DSA Setting)

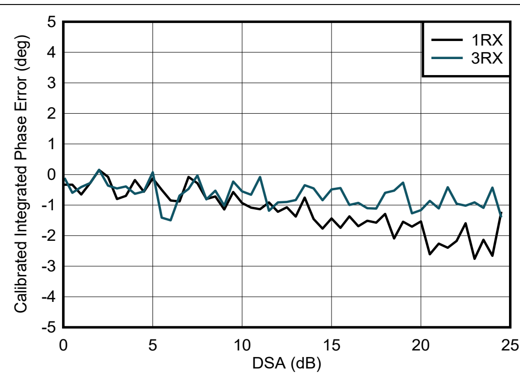
図 6-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

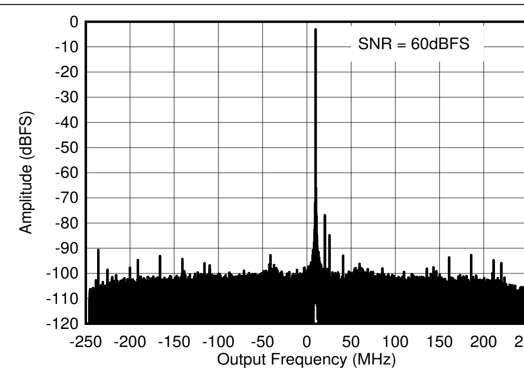
図 6-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = Phase (DSA Setting) – Phase (DSA Setting = 0)

図 6-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

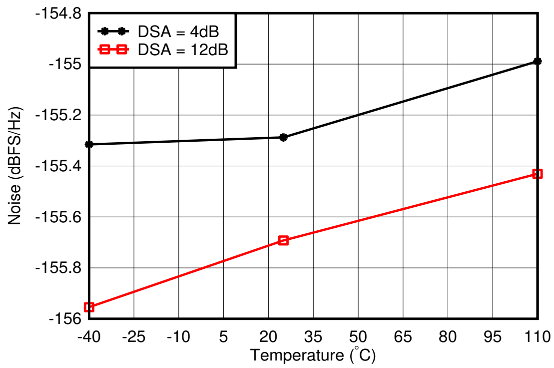


With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

図 6-184. RX Output FFT at 4.9 GHz

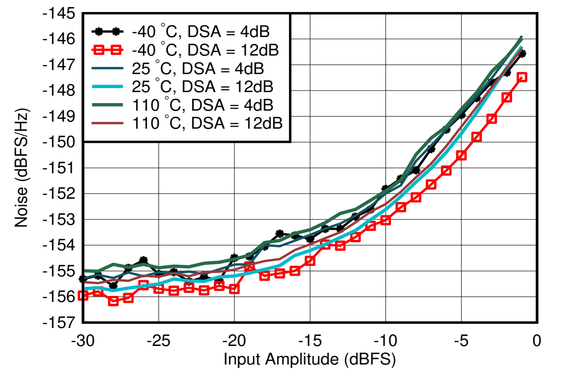
6.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



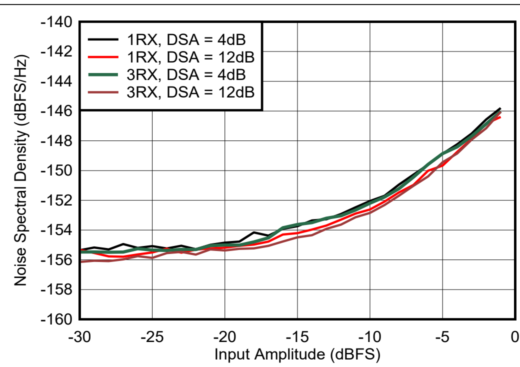
With 4.9 GHz matching, 12.5-MHz offset from tone

図 6-185. RX Noise Spectral Density vs Temperature at 4.9 GHz



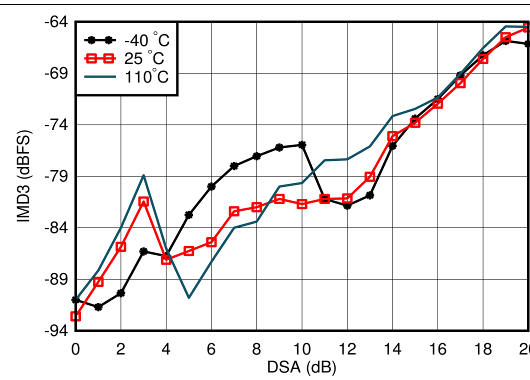
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



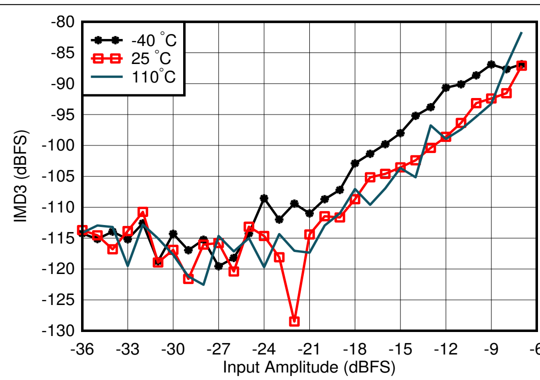
With 4.9 GHz matching, 12.5-MHz offset from tone

図 6-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



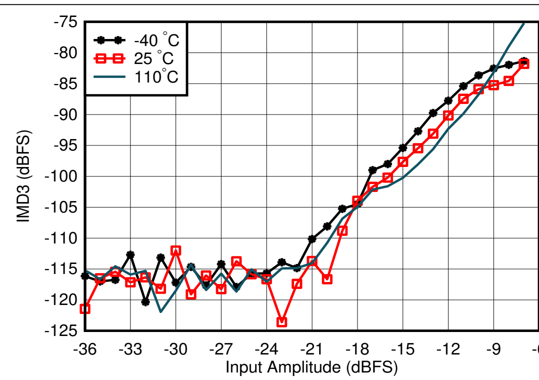
With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz

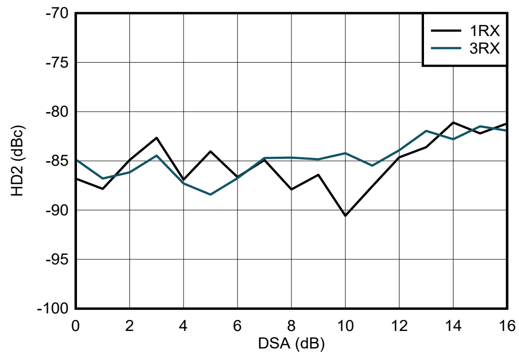


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz

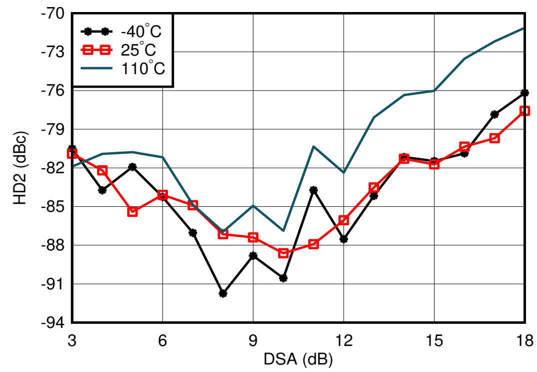
6.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



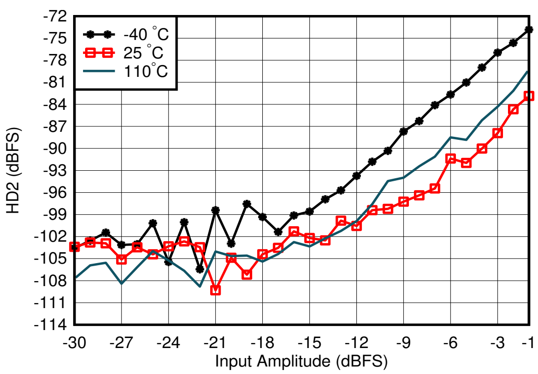
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



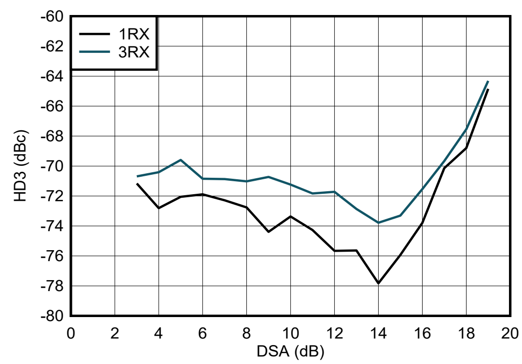
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-192. RX HD2 vs DSA and Temperature at 4.9 GHz



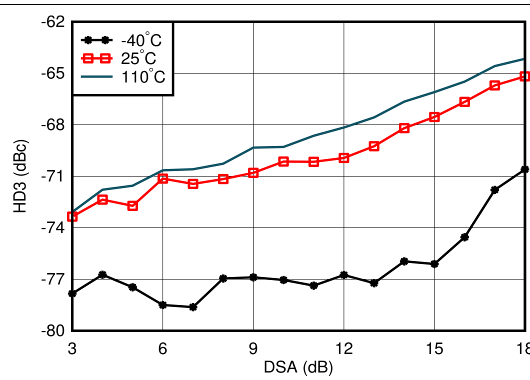
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-193. RX HD2 vs Input Level and Temperature at 4.9 GHz



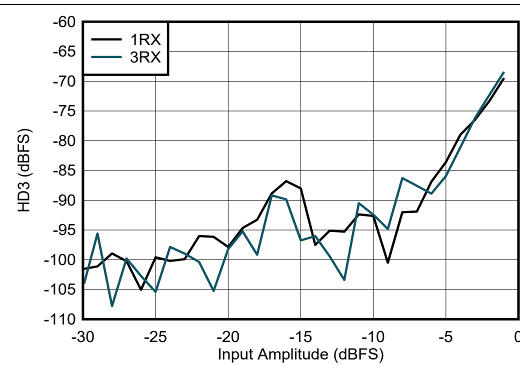
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz

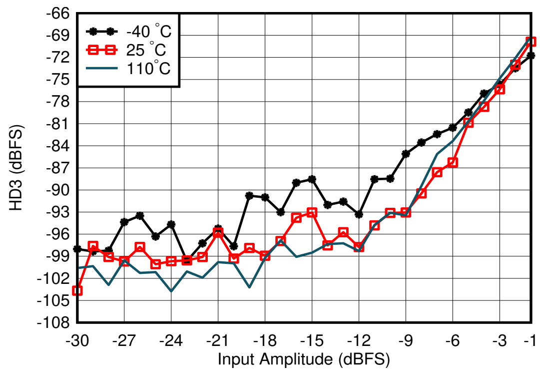


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-196. RX HD3 vs Input Level and Channel at 4.9 GHz

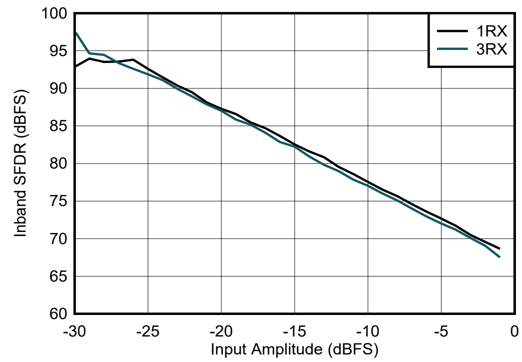
6.12.6 RX Typical Characteristics 4.9 GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52 MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



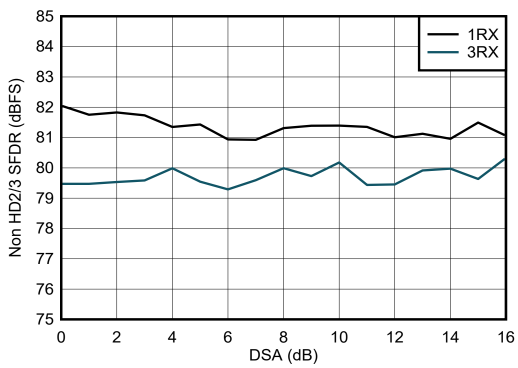
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



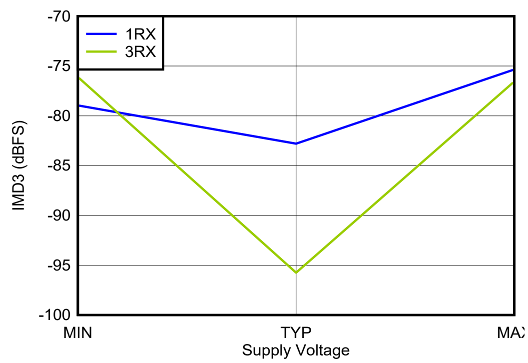
With 4.9 GHz matching, decimate by 3

図 6-198. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



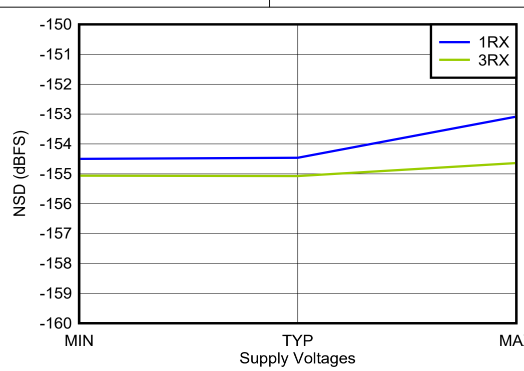
With 4.9 GHz matching

図 6-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-200. RX IMD3 vs Supply and Channel at 4.9 GHz

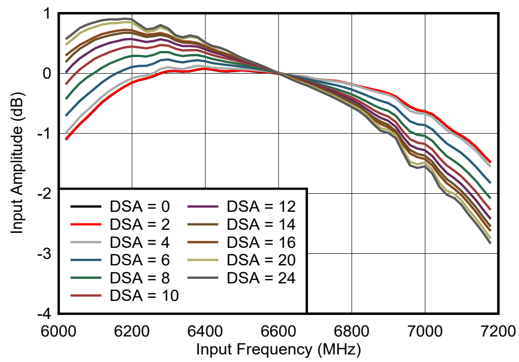


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

6.12.7 RX Typical Characteristics 6.8 GHz

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000 MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Normalized to 6.6 GHz

図 6-202. RX In-Band Gain Flatness

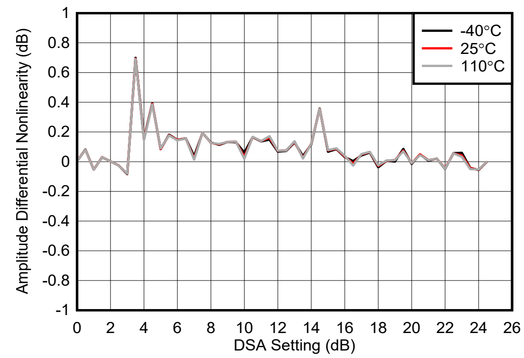
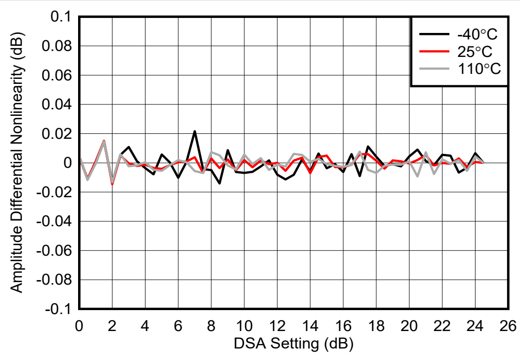


図 6-203. RX Uncalibrated Differential Amplitude Error at 6.851 GHz



Calibrated at 25°C, held at -40 and 110°C

図 6-204. RX Calibrated Differential Amplitude Error at 6.851 GHz

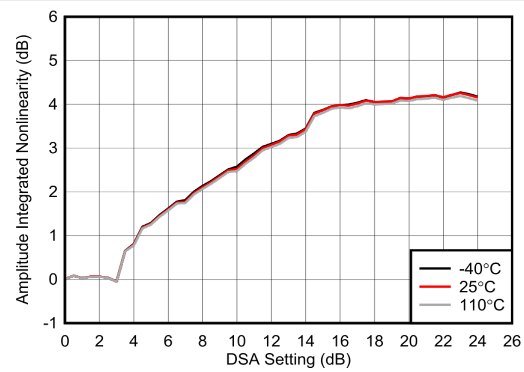
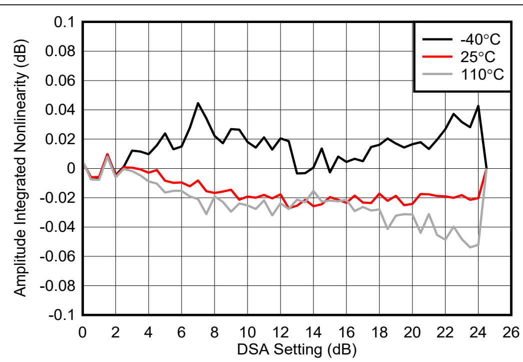


図 6-205. RX Uncalibrated Integrated Amplitude Error at 6.851 GHz



Calibrated at 25°C, held at -40 and 110°C

図 6-206. RX Calibrated Integrated Amplitude Error at 6.851 GHz

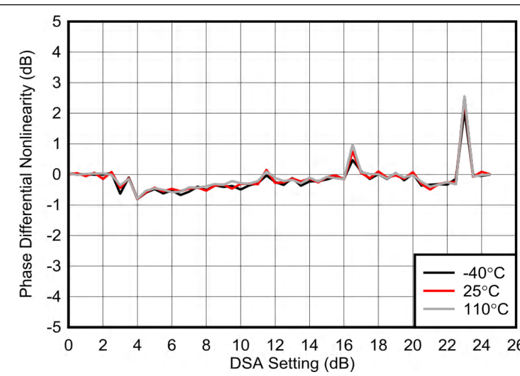
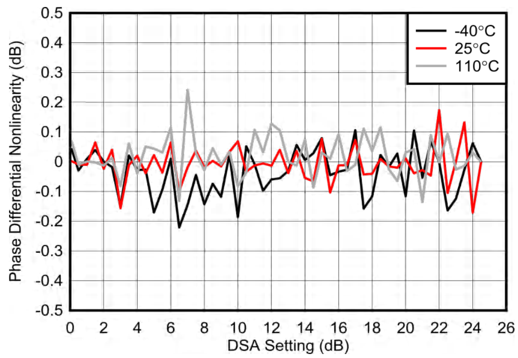


図 6-207. RX Uncalibrated Differential Phase Error at 6.851 GHz

6.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000 MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Calibrated at 25°C, held at -40 and 110°C

図 6-208. RX Calibrated Differential Phase Error at 6.851 GHz

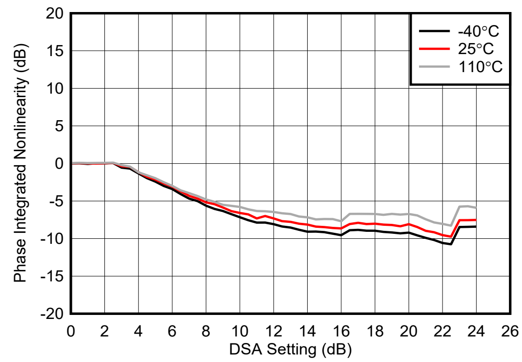
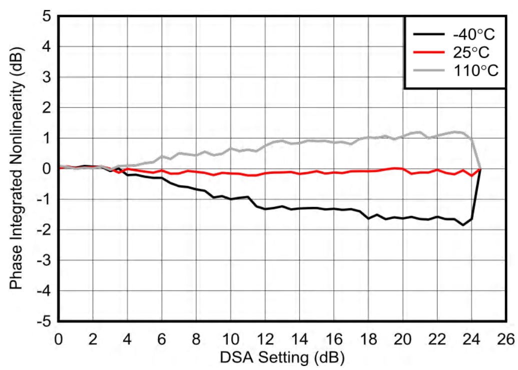
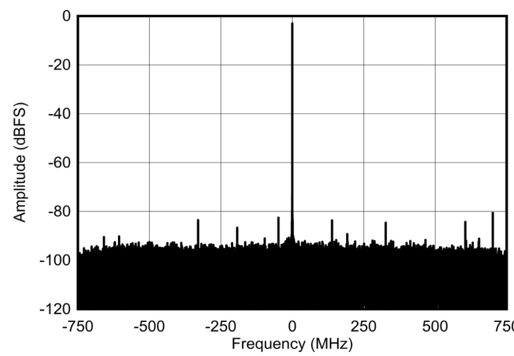


図 6-209. RX Uncalibrated Integrated Phase Error at 6.851 GHz



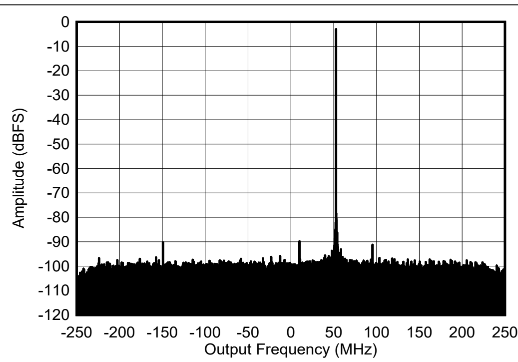
Calibrated at 25°C, held at -40 and 110°C

図 6-210. RX Calibrated Integrated Phase Error at 6.851 GHz



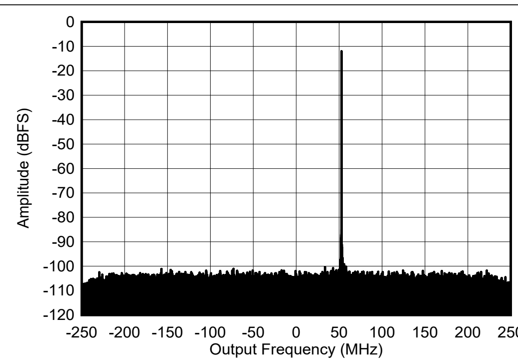
F_{IN} = 6.851 GHz, F_{NCO} = 6.85GHz

図 6-211. RX Output FFT at 6.851 GHz and -3 dBFS



F_{IN} = 6.851 GHz, F_{NCO} = 6.85GHz

図 6-212. RX Output FFT at 6.851GHz and -6dBFS

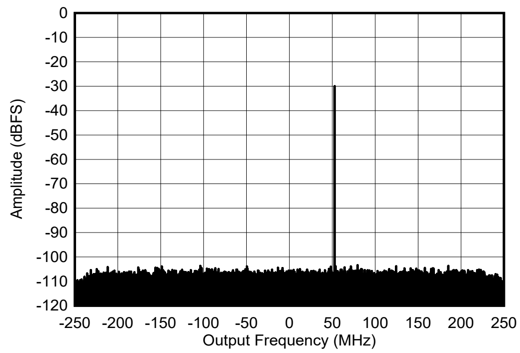


F_{IN} = 6.851 GHz, F_{NCO} = 6.85GHz

図 6-213. RX Output FFT at 6.851 GHz and -12 dBFS

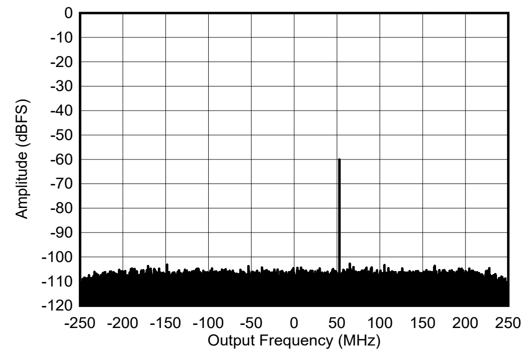
6.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000 MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



F_{IN} = 6.851 GHz, F_{NCO} = 6.85GHz

図 6-214. RX Output FFT at 6.851 GHz and -30 dBFS



F_{IN} = 6.851 GHz, F_{NCO} = 6.85GHz

図 6-215. RX Output FFT at 6.851 GHz and -60 dBFS

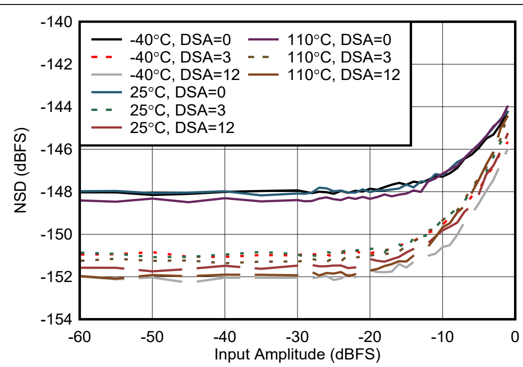
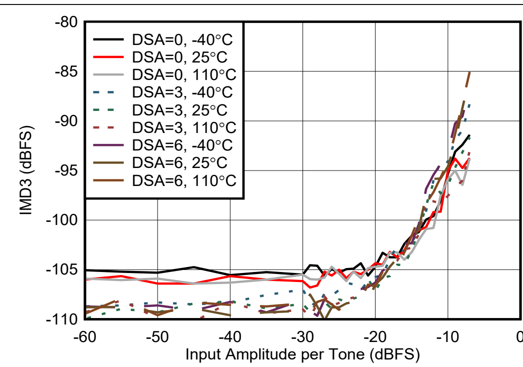
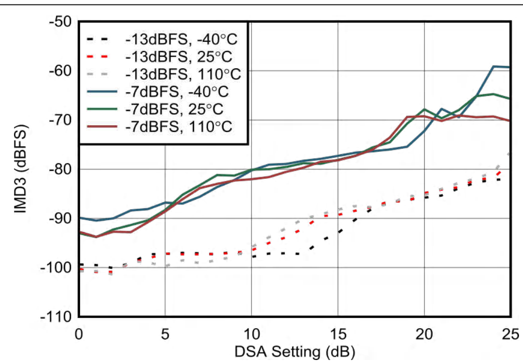


図 6-216. RX NSD vs Input Amplitude at 6.851 GHz



100 MHz Tone Spacing

図 6-217. RX IMD3 vs Input Amplitude at 6.851 GHz



100 MHz Tone Spacing

図 6-218. RX IMD3 vs DSA Setting at 6.851 GHz

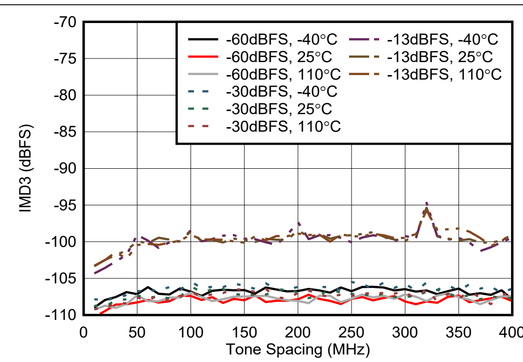


図 6-219. RX IMD3 vs Tone Spacing at 6.851 GHz

6.12.7 RX Typical Characteristics 6.8 GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30 MHz: ADC Sampling Rate = 3000 MSPS, output sample rate = 500 MSPS (decimate by 6x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.

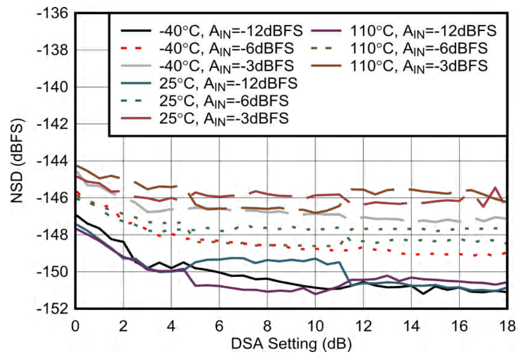
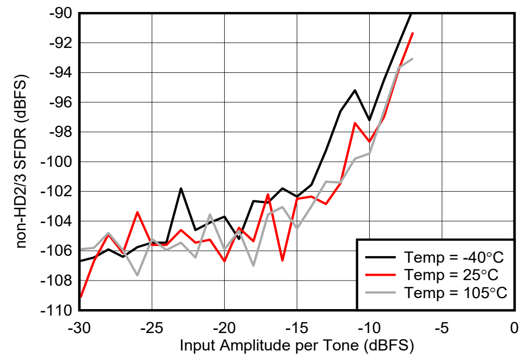


図 6-220. RX NSD vs DSA Setting at 6.851 GHz



50 MHz tone spacing, excluding 3rd order distortion

図 6-221. RX 2-tone SFDR vs Input Amplitude at 6.85 GHz

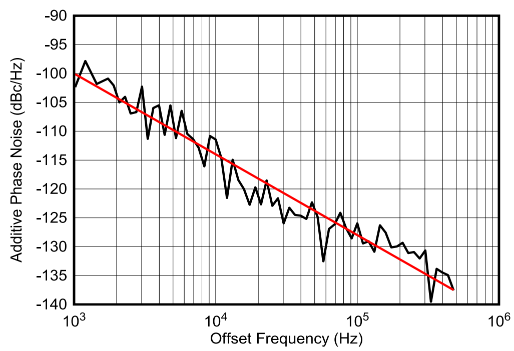
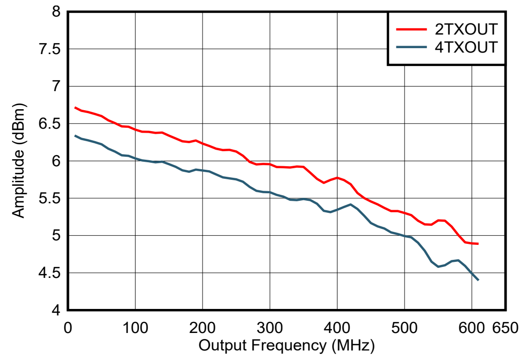


図 6-222. RX Additive Phase Noise at 6.85 GHz

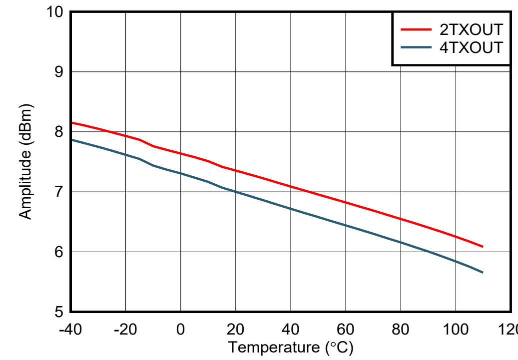
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



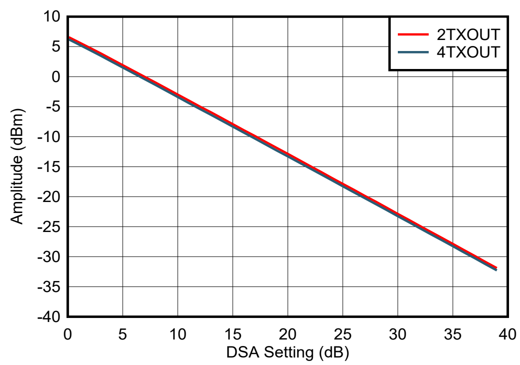
including PCB and cable losses

図 6-223. TX Output Fullscale vs Output Frequency: 5 MHz - 600 MHz



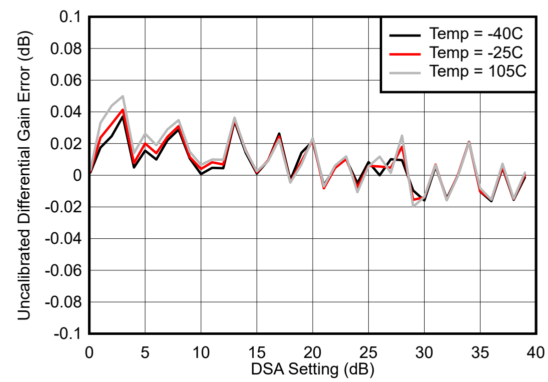
including PCB and cable losses

図 6-224. TX Output Fullscale vs Temperature at 30 MHz



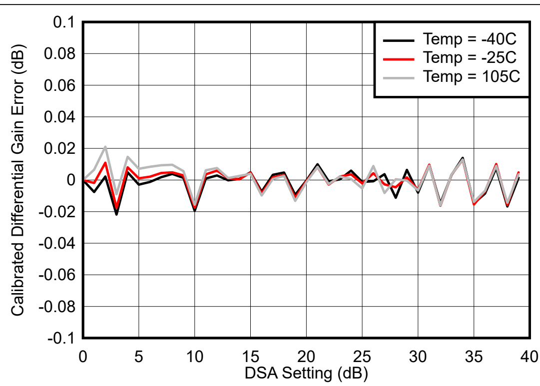
including PCB and cable losses

図 6-225. TX Output Fullscale vs DSA Setting at 30 MHz



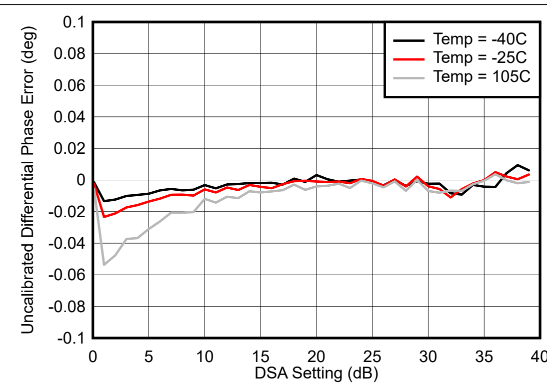
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-226. Uncalibrated TX Differential Gain Error (DNL) at 30 MHz



Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-227. Calibrated TX Differential Gain Error (DNL) at 30 MHz

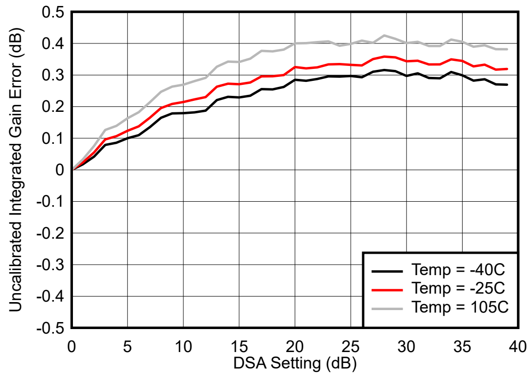


Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-228. Calibrated TX Differential Gain Error (DNL) at 30 MHz

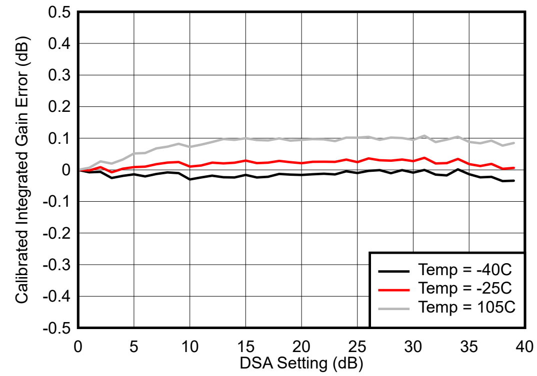
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



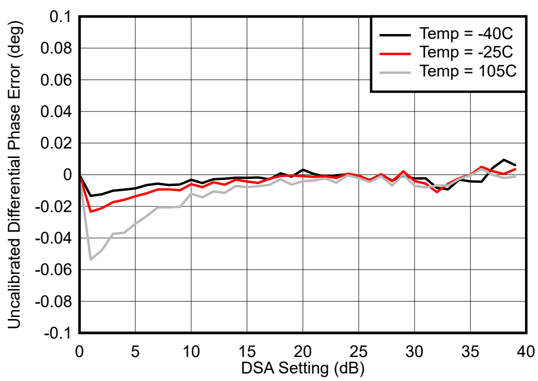
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 6-229. Uncalibrated TX Integrated Gain Error (INL) at 30 MHz



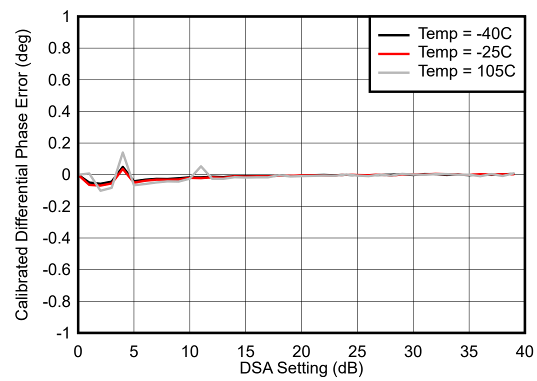
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 6-230. Calibrated TX Integrated Gain Error (INL) at 30 MHz



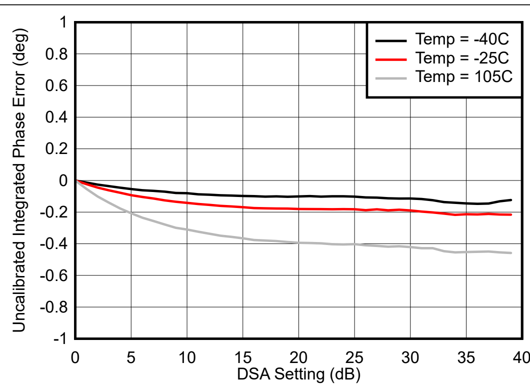
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-231. Uncalibrated TX Differential Phase Error (DNL) at 30 MHz



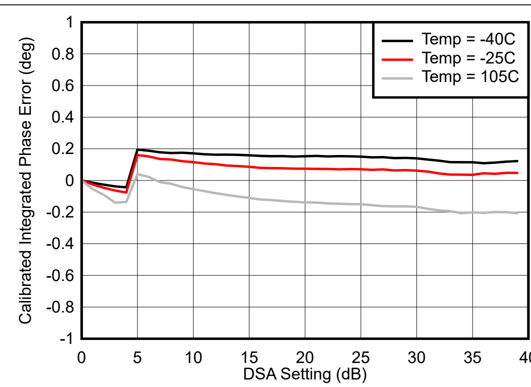
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-232. Calibrated TX Differential Phase Error (DNL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 6-233. Uncalibrated TX Integrated Phase Error (INL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 6-234. Calibrated TX Integrated Phase Error (INL) at 30 MHz

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

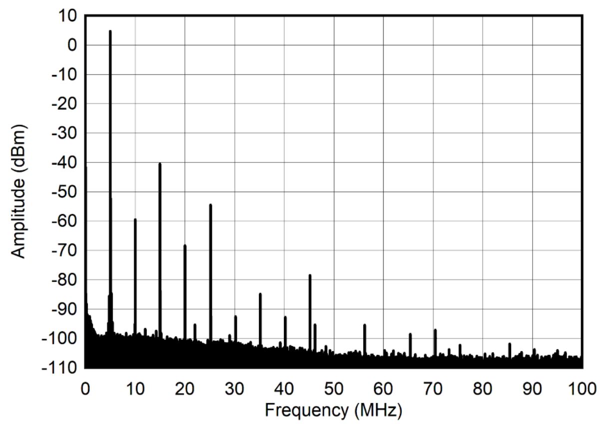


図 6-235. Single Tone Spectrum at 5 MHz and -1 dBFS (0 - 100 MHz)

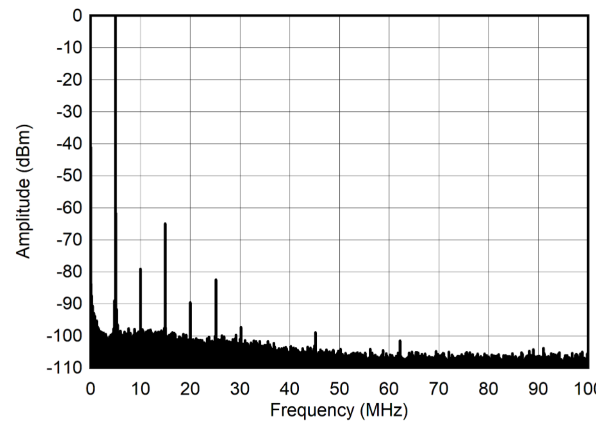


図 6-236. Single Tone Spectrum at 5 MHz and -6d BFS (0 - 100 MHz)

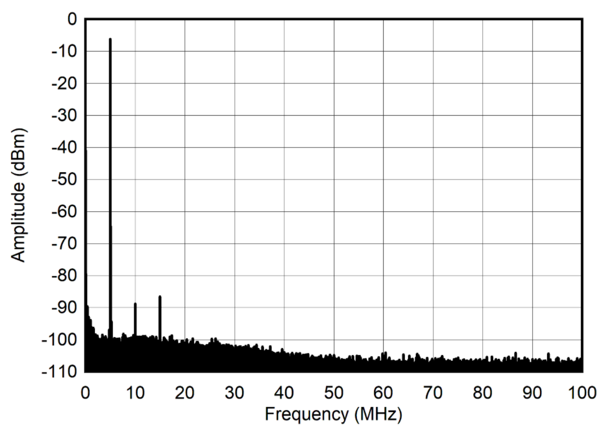


図 6-237. Single Tone Spectrum at 5 MHz and -12 dBFS (0 - 100 MHz)

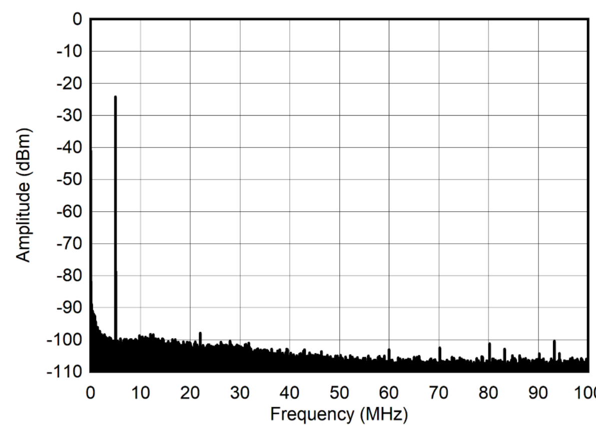


図 6-238. Single Tone Spectrum at 5 MHz and -30 dBFS (0 - 100 MHz)

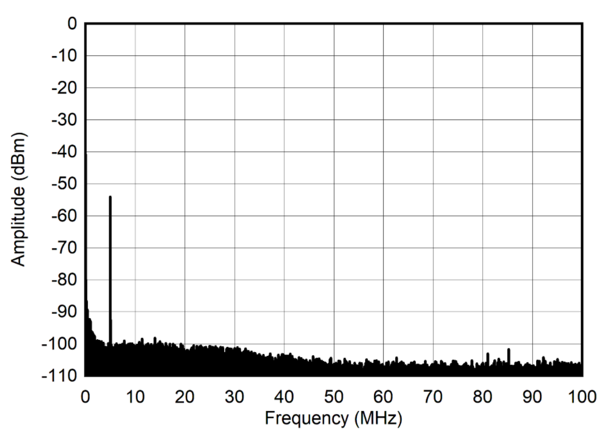


図 6-239. Single Tone Spectrum at 5 MHz and -60 dBFS (0 - 100 MHz)

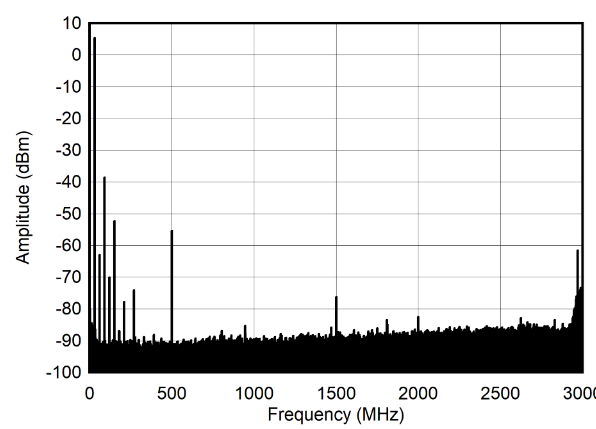


図 6-240. Single Tone Spectrum at 30 MHz and -1 dBFS (Nyquist)

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

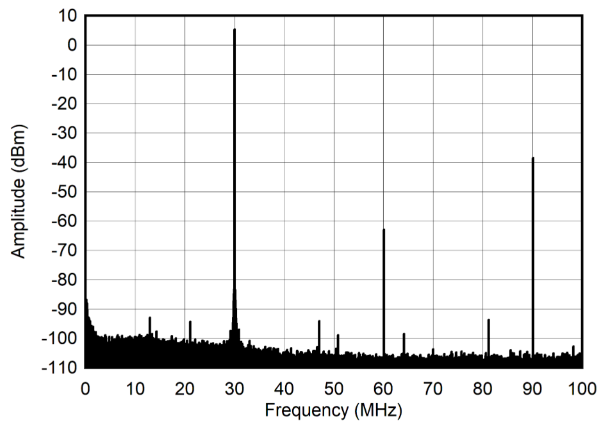


図 6-241. Single Tone Spectrum at 30 MHz and -1 dBFS (0 - 100 MHz)

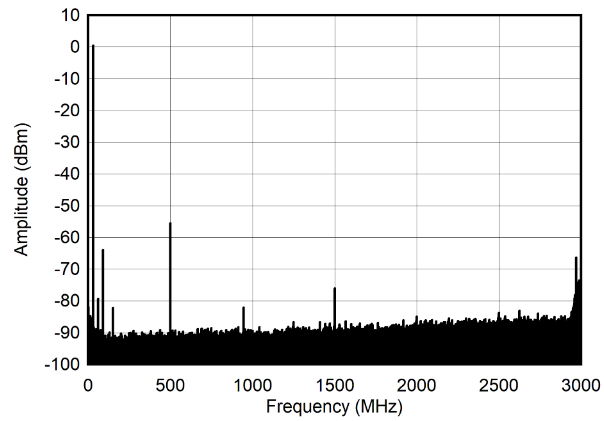


図 6-242. Single Tone Spectrum at 30 MHz and -6 dBFS (Nyquist)

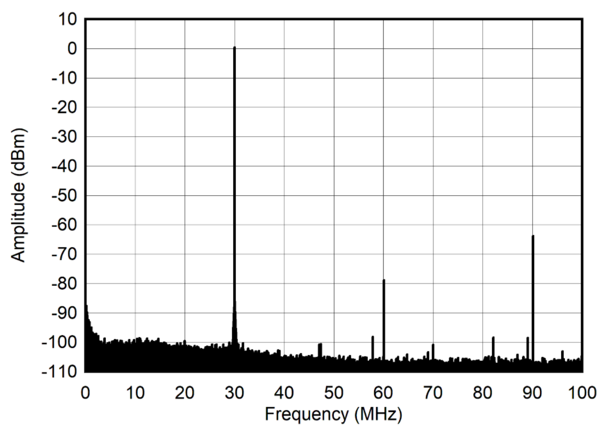


図 6-243. Single Tone Spectrum at 30 MHz and -6 dBFS (0 - 100 MHz)

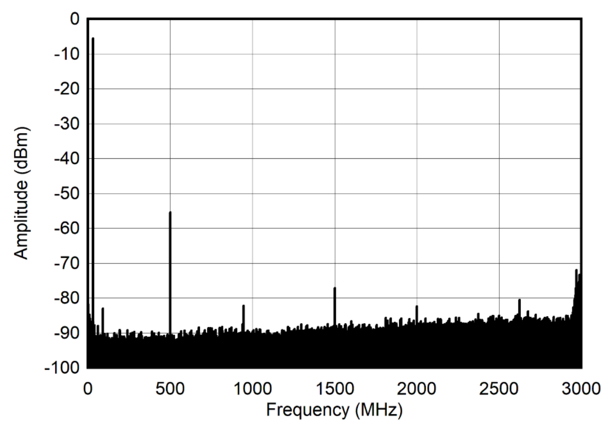


図 6-244. Single Tone Spectrum at 30 MHz and -12 dBFS (Nyquist)

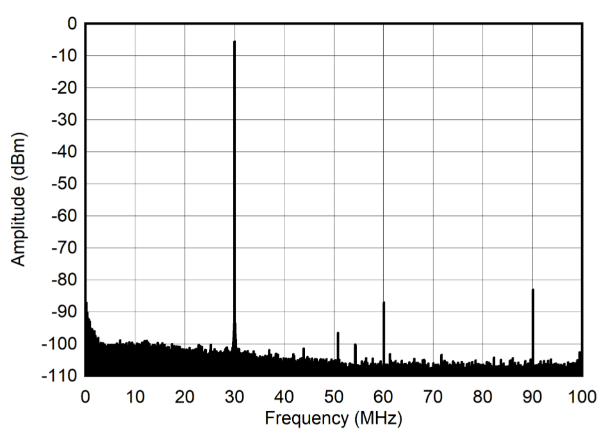


図 6-245. Single Tone Spectrum at 30 MHz and -12 dBFS (0 - 100 MHz)

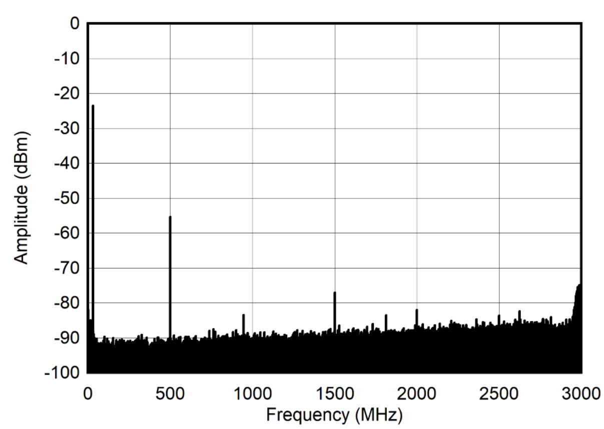


図 6-246. Single Tone Spectrum at 30 MHz and -30 dBFS (Nyquist)

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

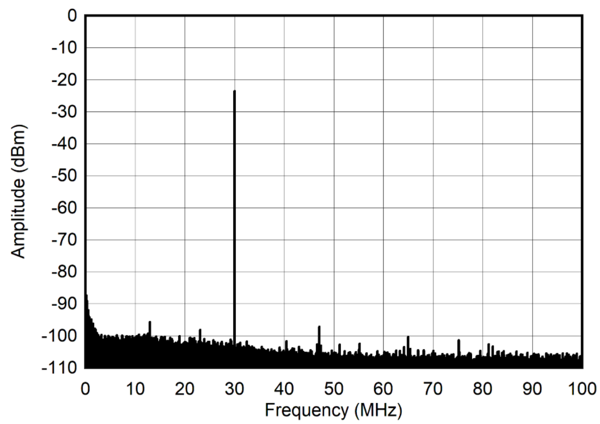


図 6-247. Single Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

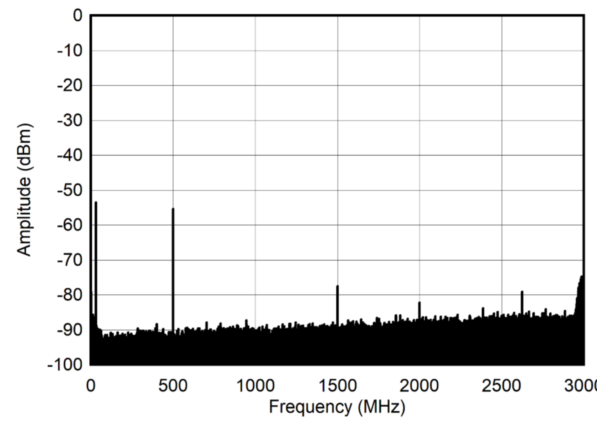


図 6-248. Single Tone Spectrum at 30 MHz and -60 dBFS (Nyquist)

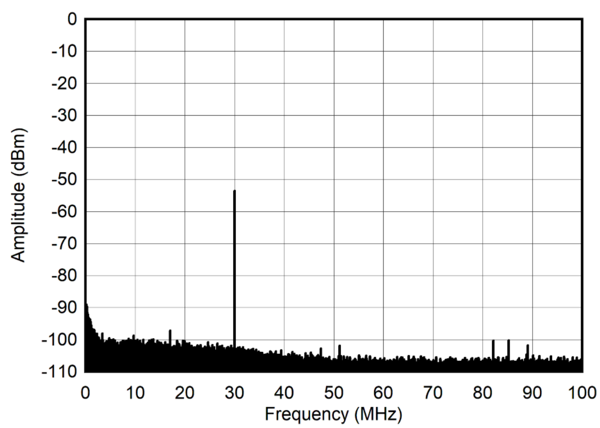


図 6-249. Single Tone Spectrum at 30 MHz and -60 dBFS (0 - 100 MHz)

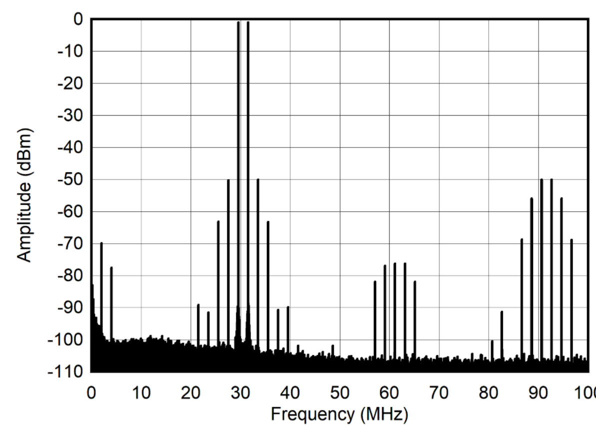


図 6-250. Dual Tone Spectrum at 30 MHz and -7 dBFS (0 - 100 MHz)

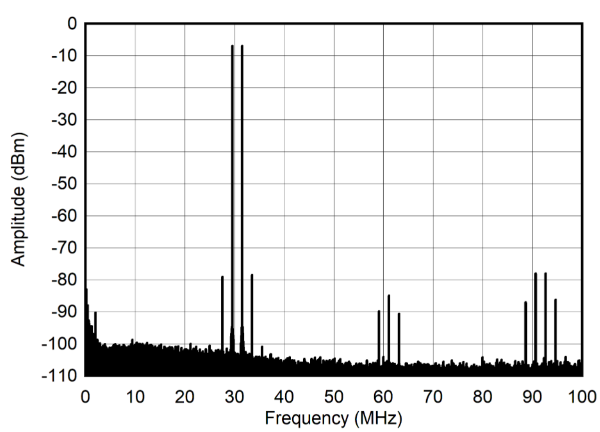


図 6-251. Dual Tone Spectrum at 30 MHz and -13 dBFS (0 - 100 MHz)

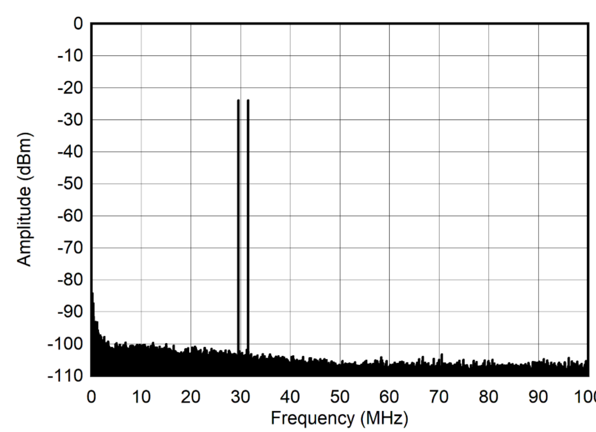


図 6-252. Dual Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

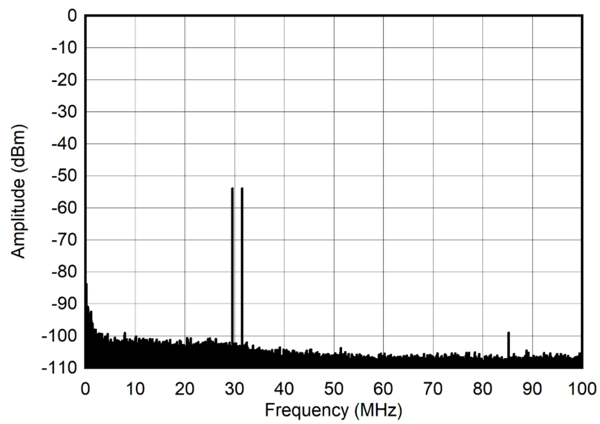
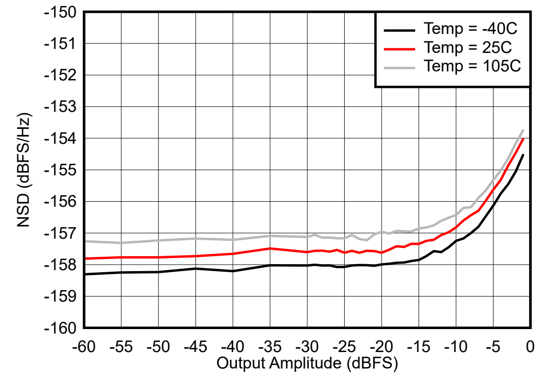
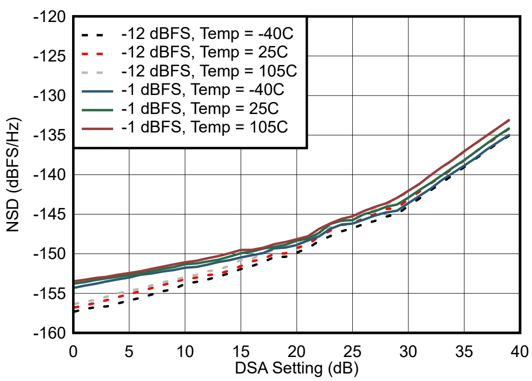


図 6-253. Dual Tone Spectrum at 30 MHz and -60d BFS (0 - 100 MHz)



measured at +50 MHz offset

図 6-254. Noise Spectral Density vs Digital Amplitude at 30 MHz



measured at +50 MHz offset

図 6-255. Noise Spectral Density vs DSA Setting at 30 MHz

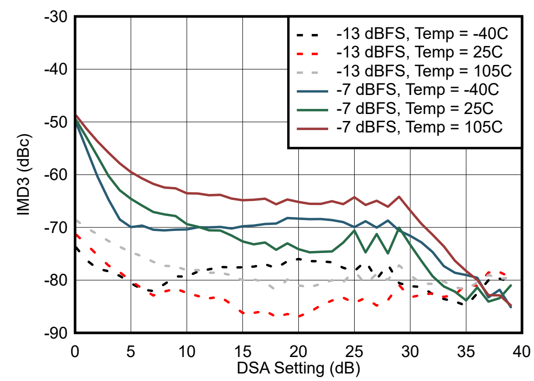


図 6-256. IMD3 vs DSA Setting at 30 MHz

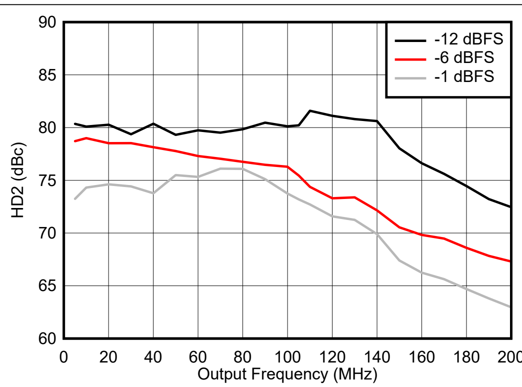


図 6-257. HD2 vs Frequency 0 - 200 MHz

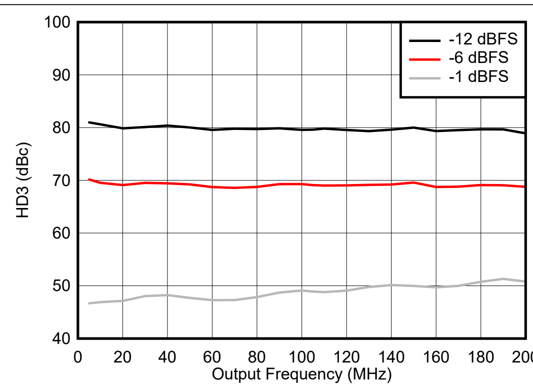
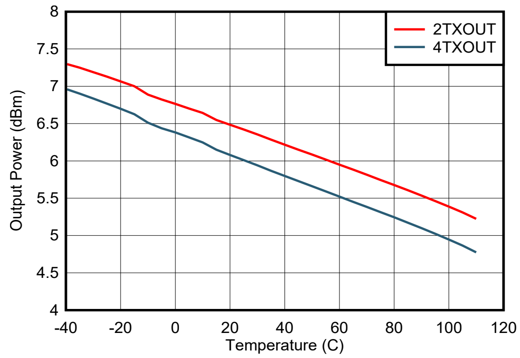


図 6-258. HD3 vs Frequency 0 - 200 MHz

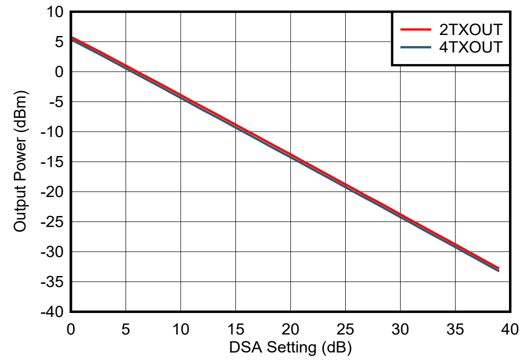
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



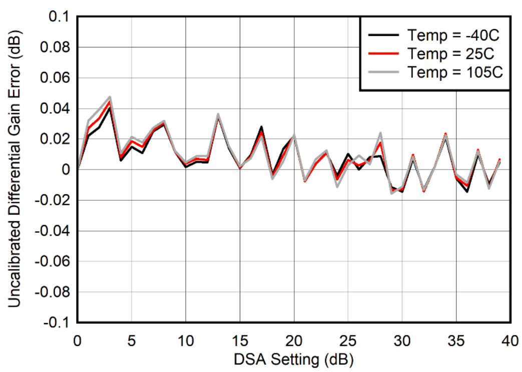
including PCB and cable losses

図 6-259. TX Output Fullscale vs Temperature at 400 MHz



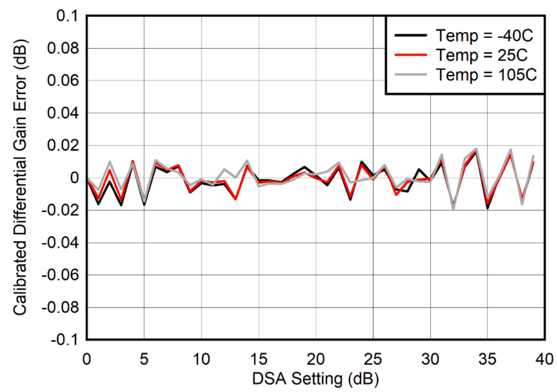
including PCB and cable losses

図 6-260. TX Output Fullscale vs DSA Setting at 400 MHz



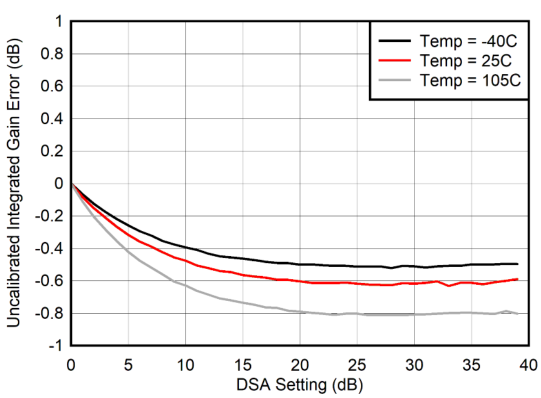
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-261. Uncalibrated TX Differential Gain Error (DNL) at 400 MHz



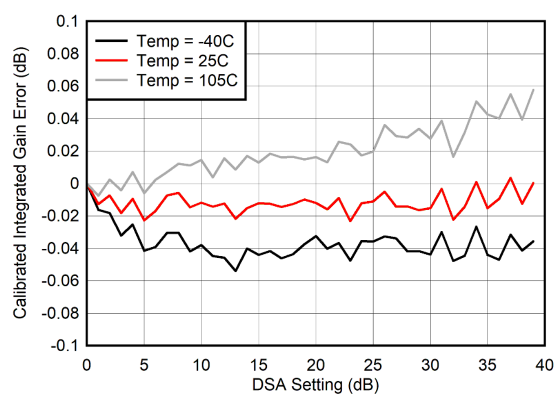
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-262. Calibrated TX Differential Gain Error (DNL) at 400 MHz



Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 6-263. Uncalibrated TX Integrated Gain Error (INL) at 400 MHz

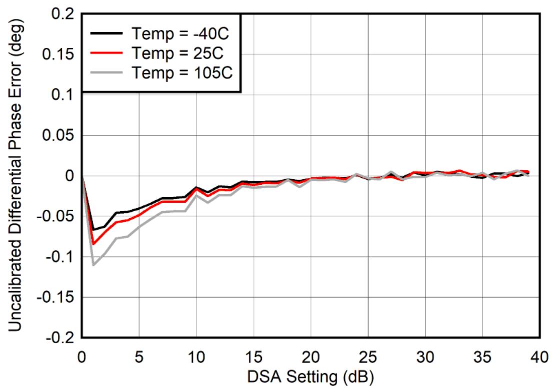


Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 6-264. Calibrated TX Integrated Gain Error (INL) at 400 MHz

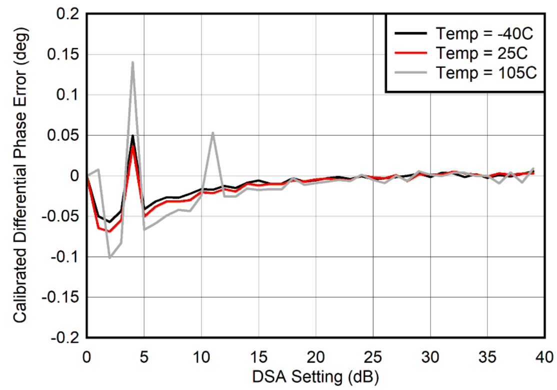
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



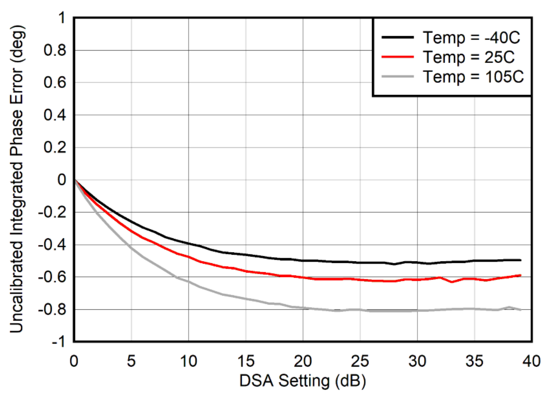
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-265. Uncalibrated TX Differential Phase Error (DNL) at 400 MHz



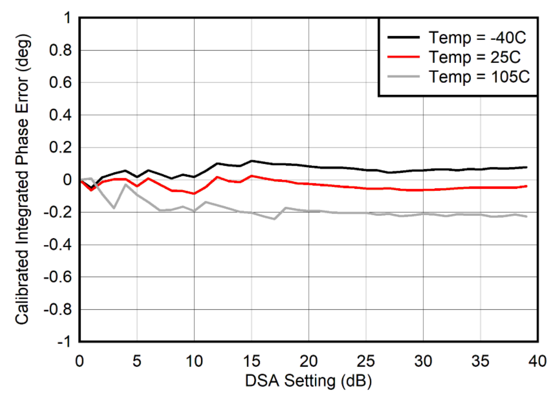
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-266. Calibrated TX Differential Phase Error (DNL) at 400 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 6-267. Uncalibrated TX Integrated Phase Error (INL) at 400 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 6-268. Calibrated TX Integrated Phase Error (INL) at 400 MHz

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

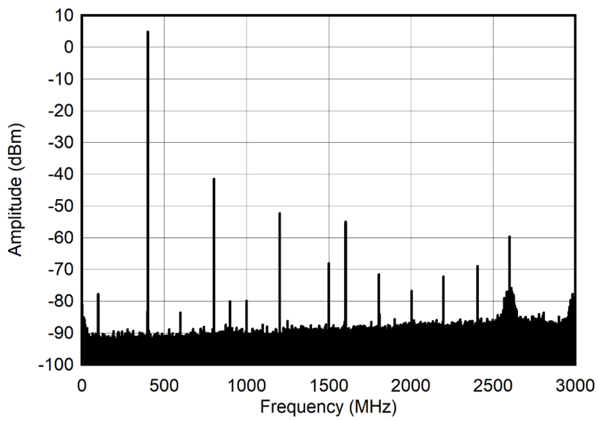


図 6-269. Single Tone Spectrum at 400 MHz and -1 dBFS (Nyquist)

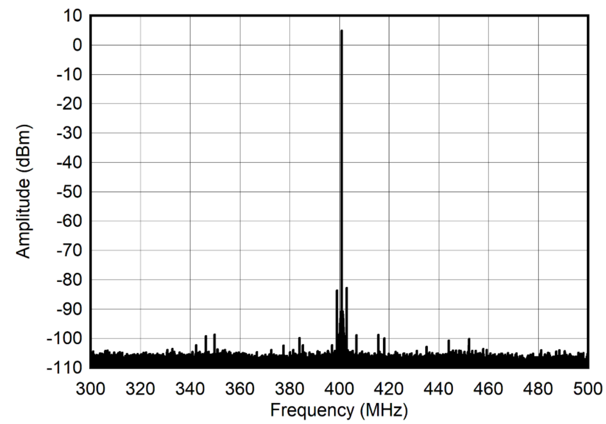


図 6-270. Single Tone Spectrum at 400 MHz and -1 dBFS (±100MHz)

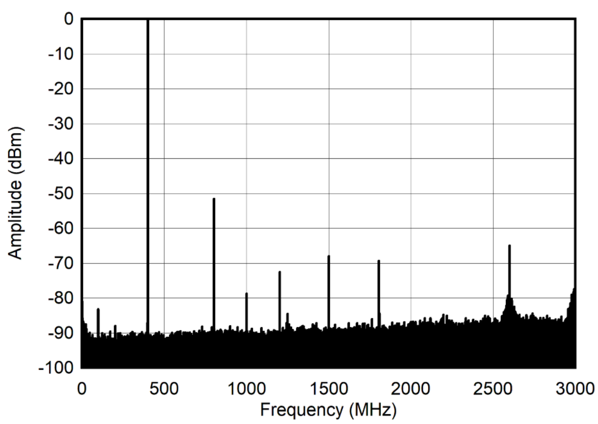


図 6-271. Single Tone Spectrum at 400 MHz and -6 dBFS (Nyquist)

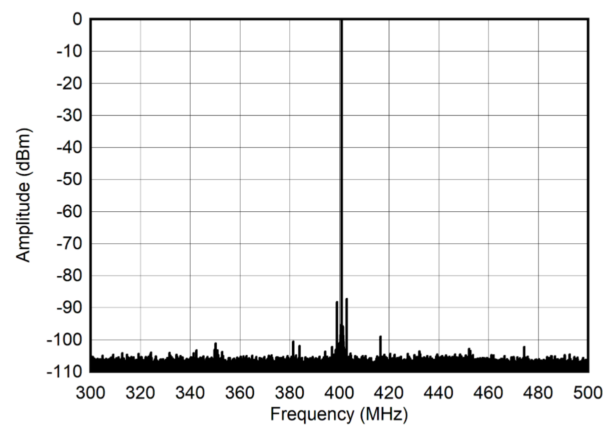


図 6-272. Single Tone Spectrum at 400 MHz and -6 dBFS (±100MHz)

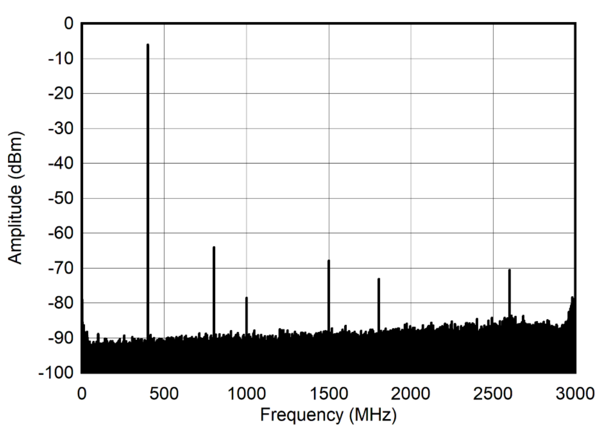


図 6-273. Single Tone Spectrum at 400 MHz and -12 dBFS (Nyquist)

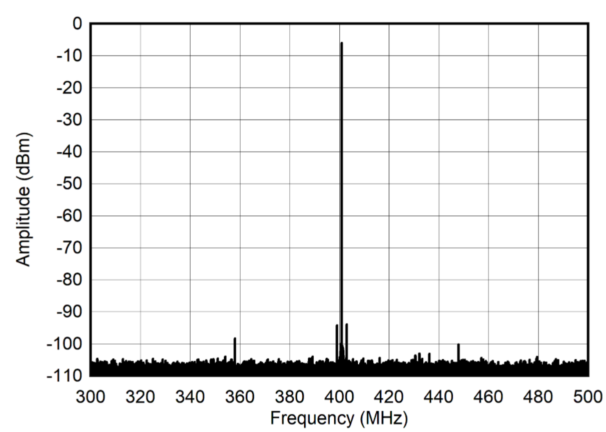


図 6-274. Single Tone Spectrum at 400 MHz and -12 dBFS (±100MHz)

6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

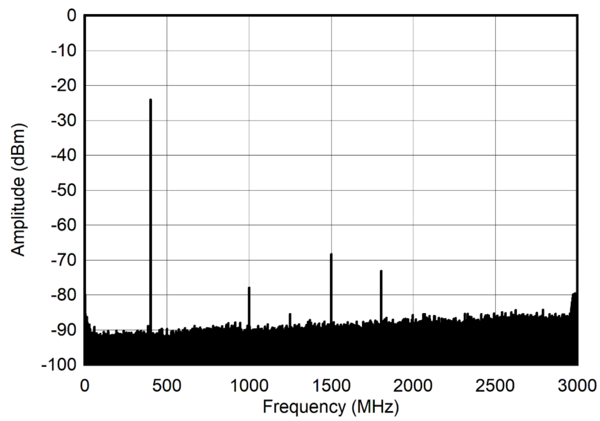


図 6-275. Single Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)

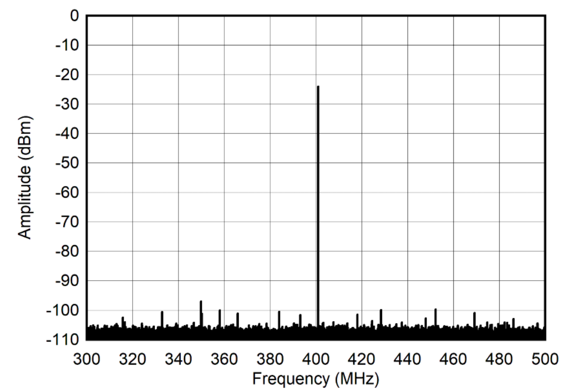


図 6-276. Single Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)

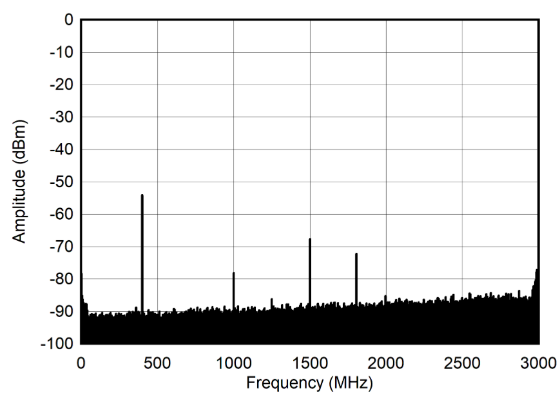


図 6-277. Single Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

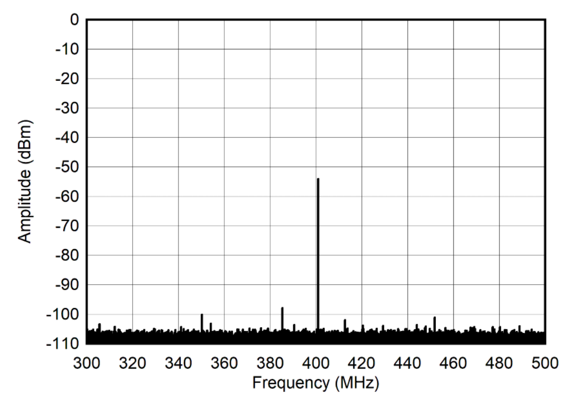
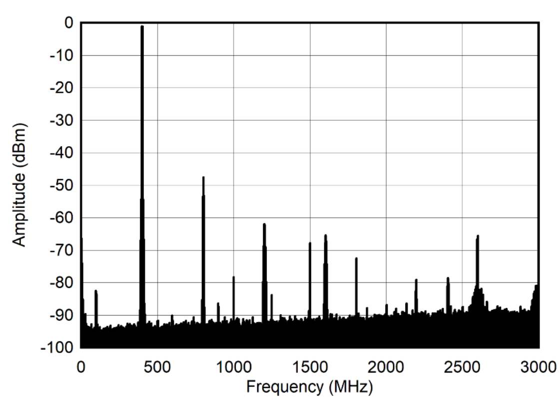
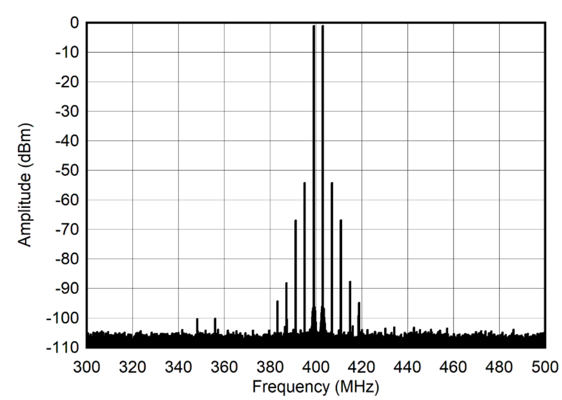


図 6-278. Single Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)



Tone Spacing = 4 MHz

図 6-279. Dual Tone Spectrum at 400 MHz and -7 dBFS (Nyquist)

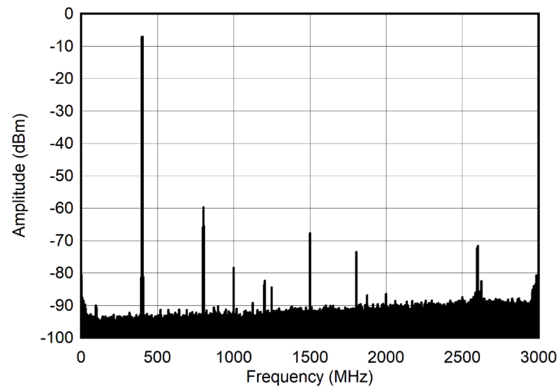


Tone Spacing = 4 MHz

図 6-280. Dual Tone Spectrum at 400 MHz and -7 dBFS (±100MHz)

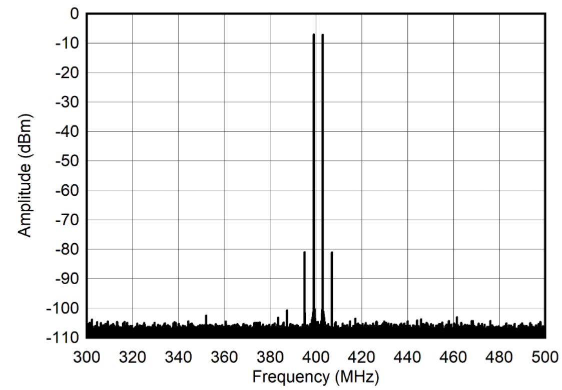
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



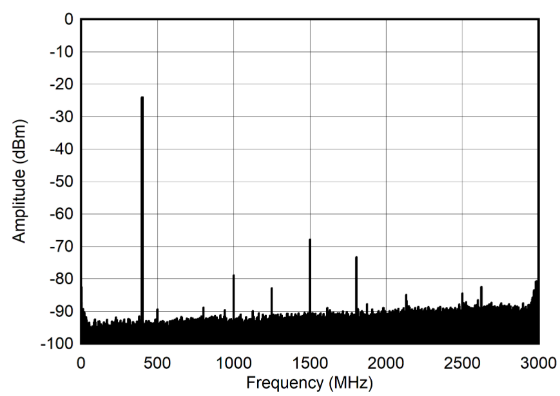
Tone Spacing = 4 MHz

図 6-281. Dual Tone Spectrum at 400 MHz and -13 dBFS (Nyquist)



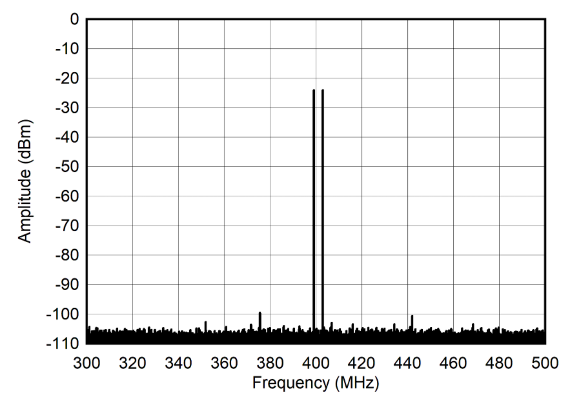
Tone Spacing = 4 MHz

図 6-282. Dual Tone Spectrum at 400 MHz and -13 dBFS (±100MHz)



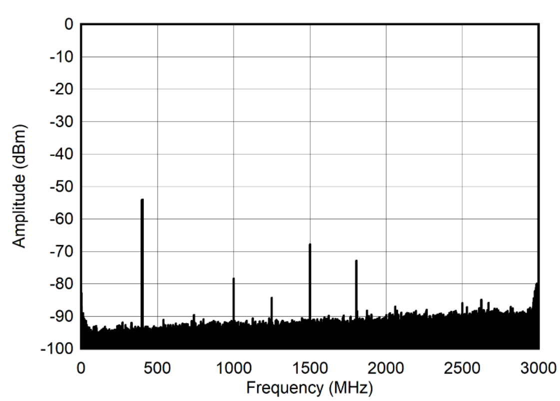
Tone Spacing = 4 MHz

図 6-283. Dual Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)



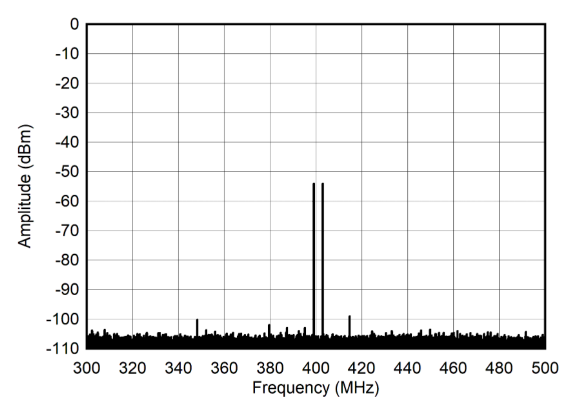
Tone Spacing = 4 MHz

図 6-284. Dual Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)



Tone Spacing = 4 MHz

図 6-285. Dual Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

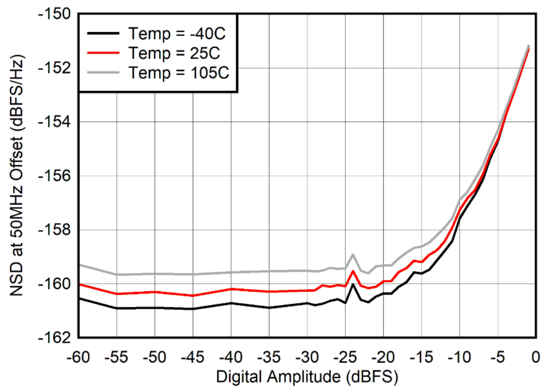


Tone Spacing = 4 MHz

図 6-286. Dual Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)

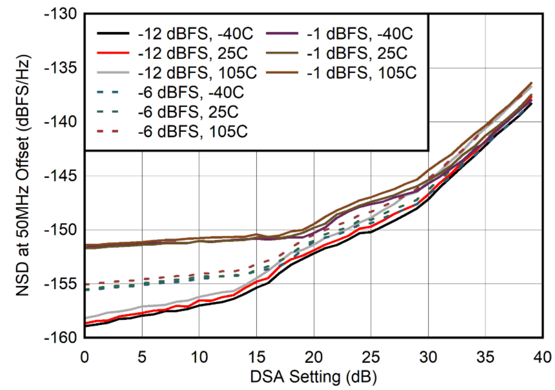
6.12.8 TX Typical Characteristics at 30 MHz and 600 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



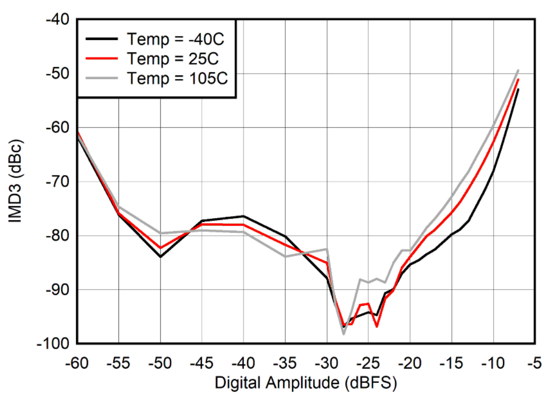
measured at 50 MHz offset

図 6-287. Noise Spectral Density vs Digital Amplitude at 400 MHz



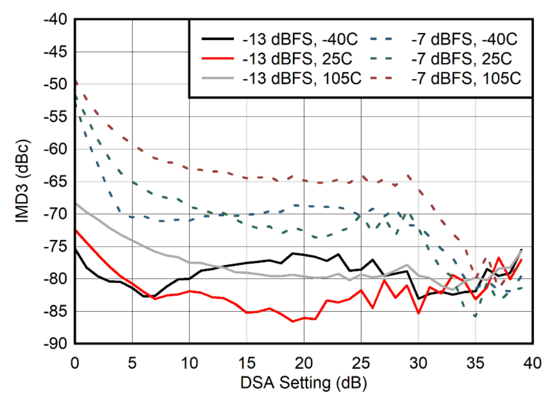
measured at 50 MHz offset

図 6-288. Noise Spectral Density vs DSA Setting at 400 MHz



Tone Spacing = 4 MHz

図 6-289. IMD3 vs Digital Amplitude at 400 MHz



Tone Spacing = 4 MHz

図 6-290. IMD3 vs DSA Setting at 400 MHz

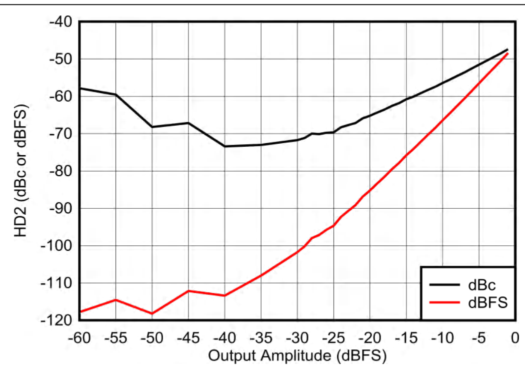


図 6-291. HD2 vs Amplitude at 400 MHz

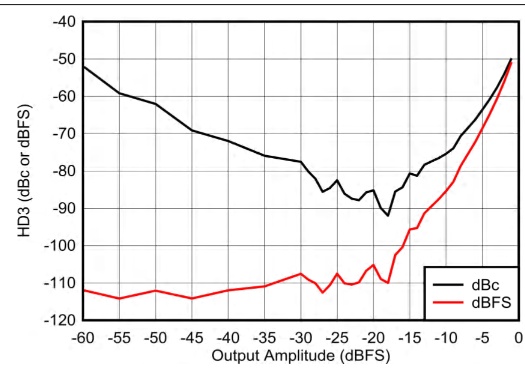
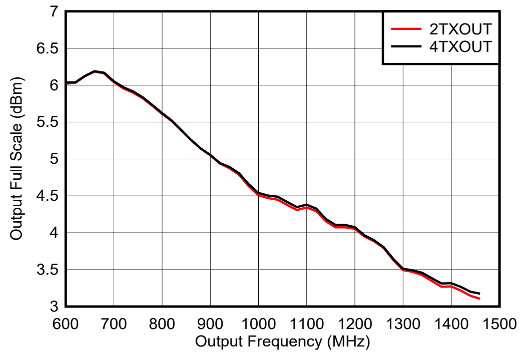


図 6-292. HD3 vs Amplitude at 400 MHz

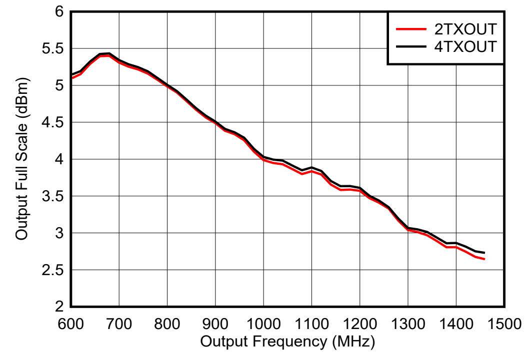
6.12.9 TX Typical Characteristics at 800 MHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



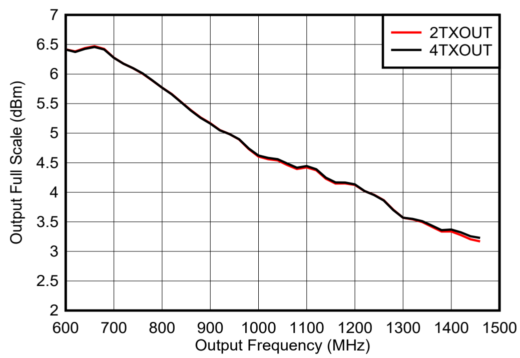
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-293. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode



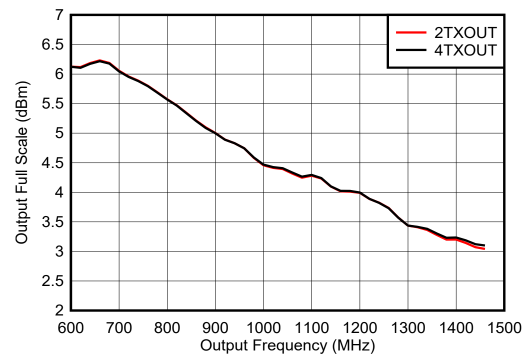
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHzmatching

図 6-294. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Straight Mode



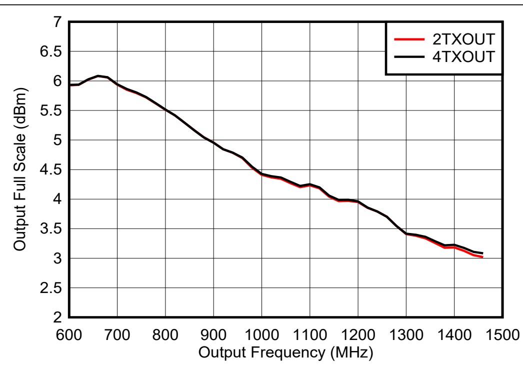
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-295. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Interleave Mode



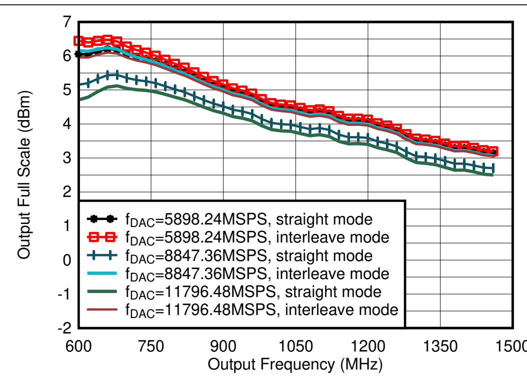
Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-296. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Interleave Mode



Including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-297. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS, Interleave Mode

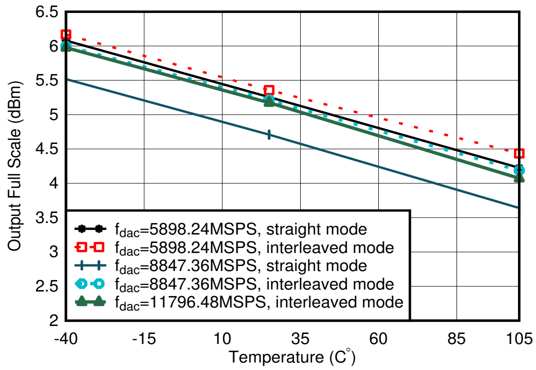


including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-298. TX Output Fullscale vs Output Frequency

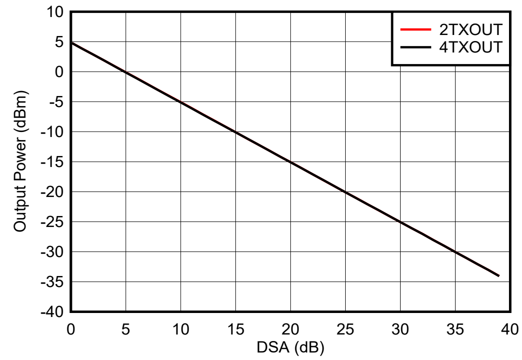
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



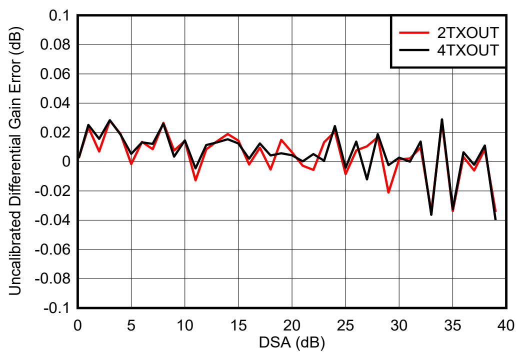
including PCB and cable losses, A_{out} = -0.5 dFBS, DSA = 0, 0.8 GHz matching

図 6-299. TX Output Fullscale vs Temperature



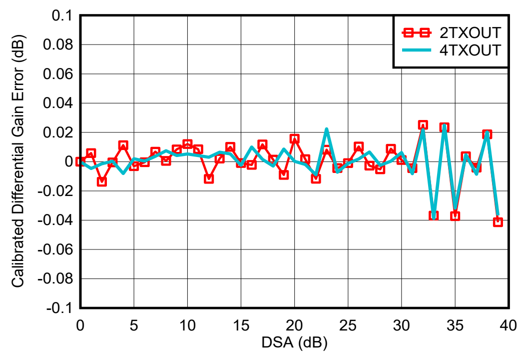
f_{DAC} = 11796.48 MSPS, interleave mode, A_{out} = -0.5 dFBS, matching 0.8 GHz

図 6-300. TX Output Power vs DSA Setting and Channel at 0.85 GHz



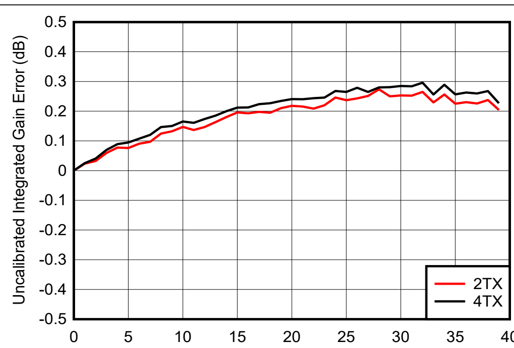
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-301. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



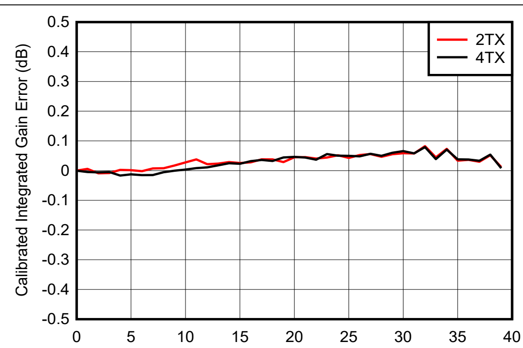
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-302. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

図 6-303. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

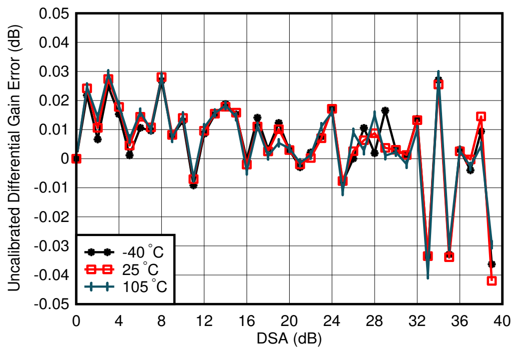


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 6-304. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

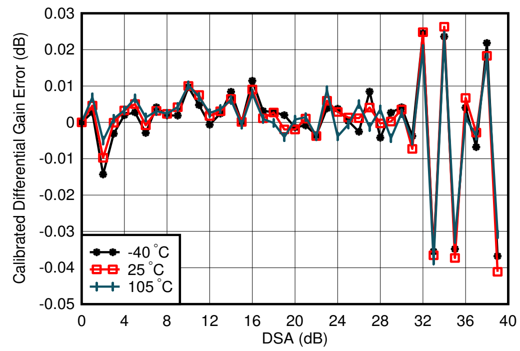
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



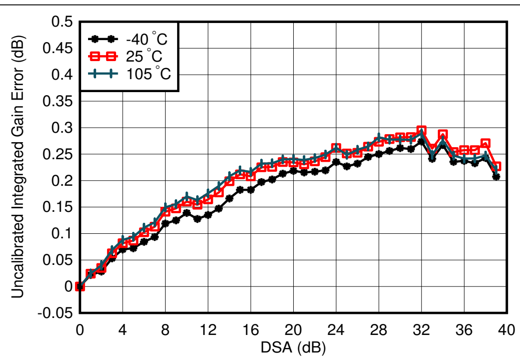
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-305. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



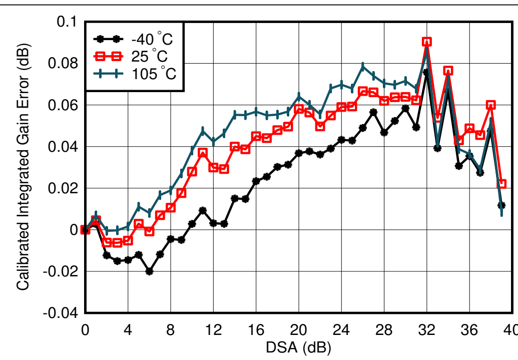
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-306. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 6-307. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

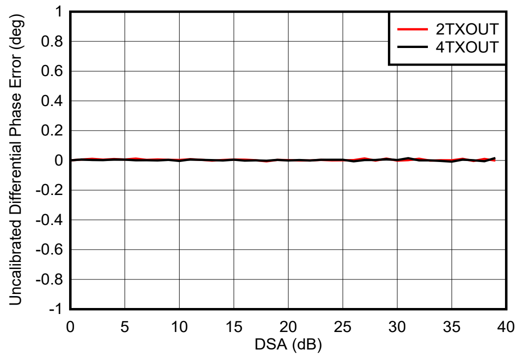


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 6-308. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

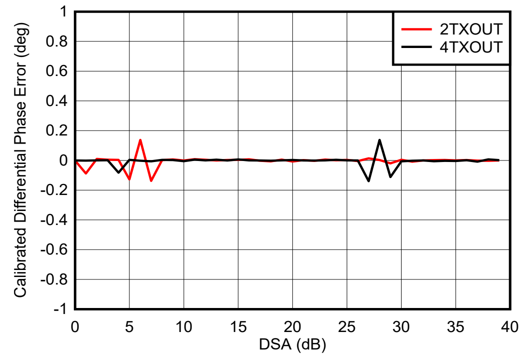
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



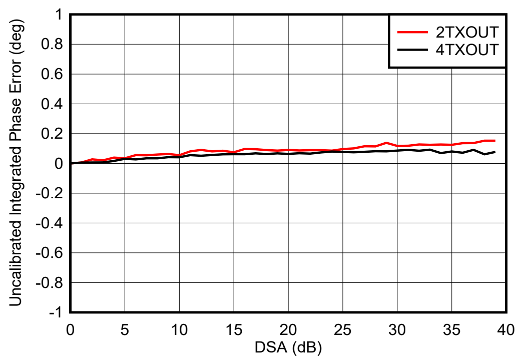
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-309. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



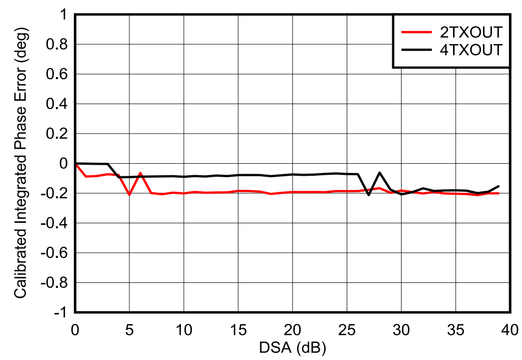
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 6-310. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 6-311. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

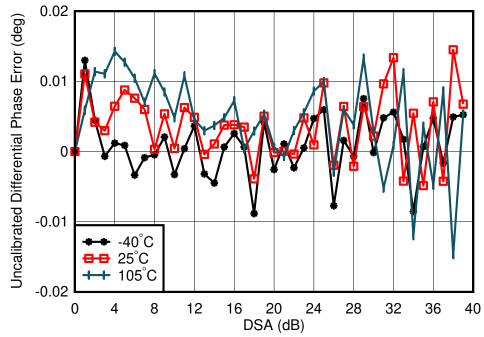


f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 6-312. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

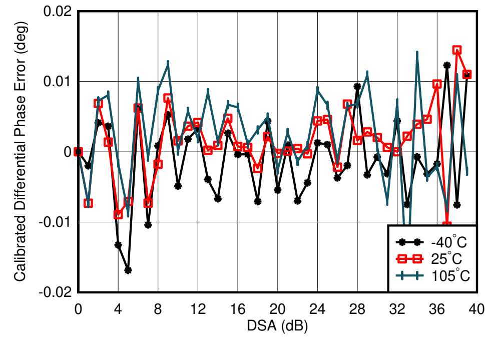
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



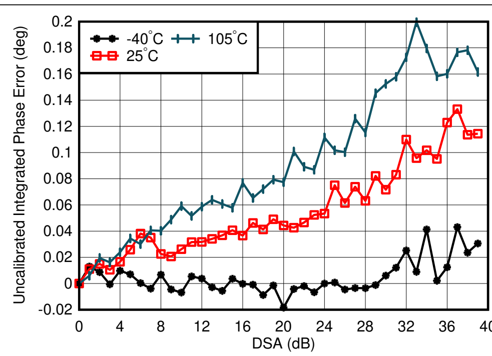
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 6-313. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



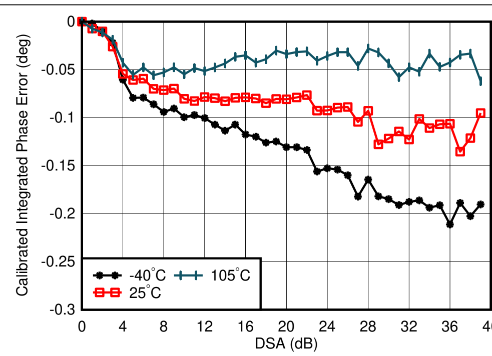
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 6-314. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



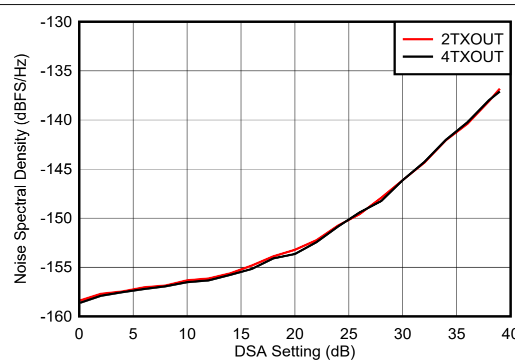
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 6-315. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



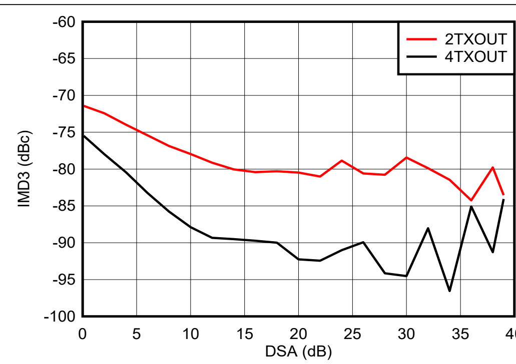
f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 6-316. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, matching at 0.8 GHz, P_{OUT} = –13 dBFS

図 6-317. TX Output Noise vs Channel and Attenuation at 0.85 GHz

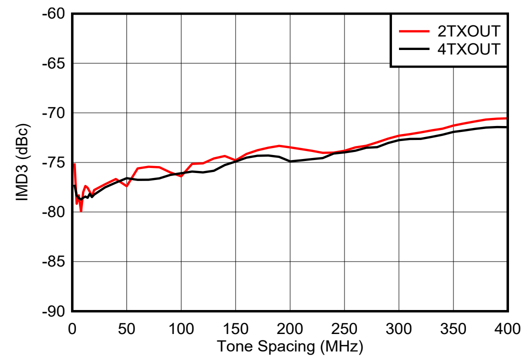


f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 6-318. TX IMD3 vs DSA Setting at 0.85 GHz

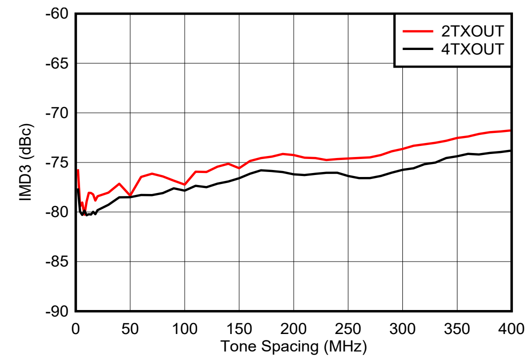
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



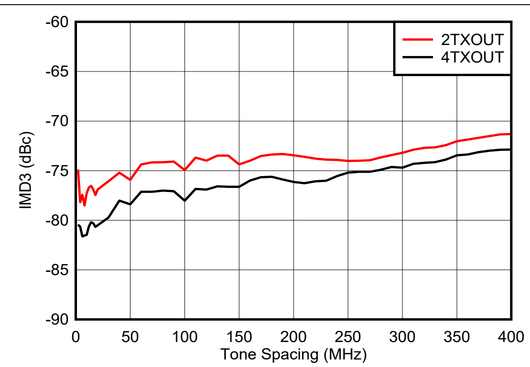
f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 6-319. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



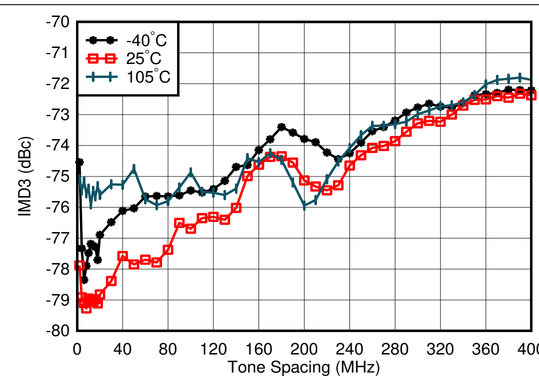
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 6-320. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



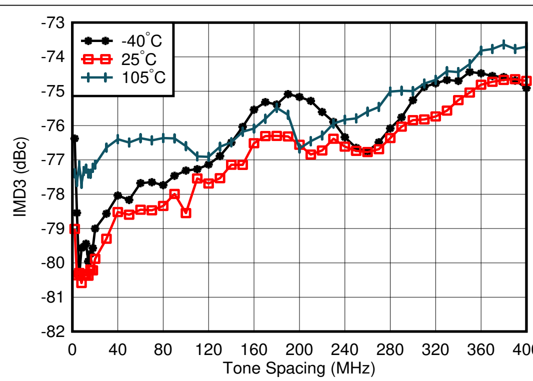
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 6-321. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



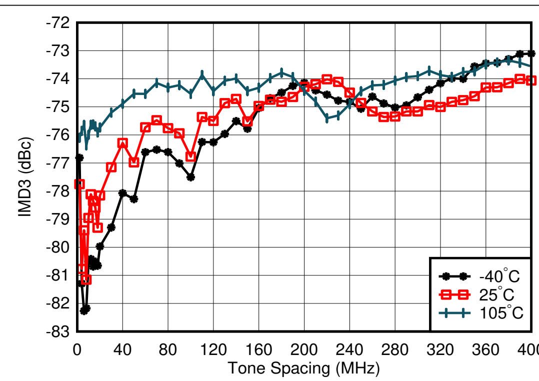
f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 6-322. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 6-323. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

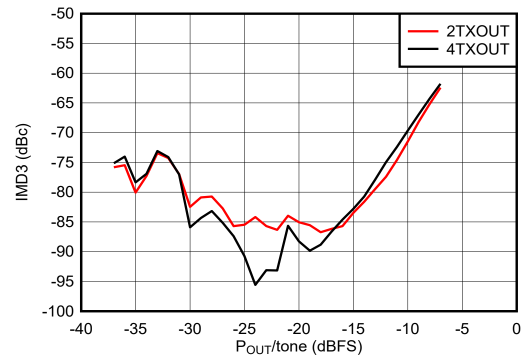


f_{DAC} = 11796.48 MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 6-324. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

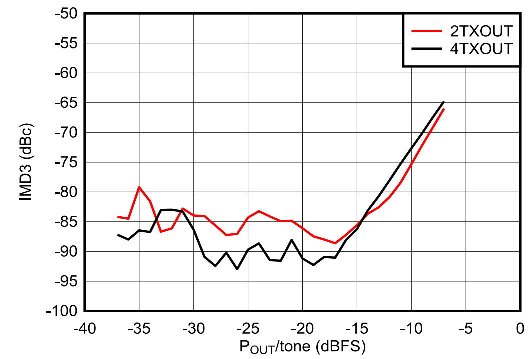
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



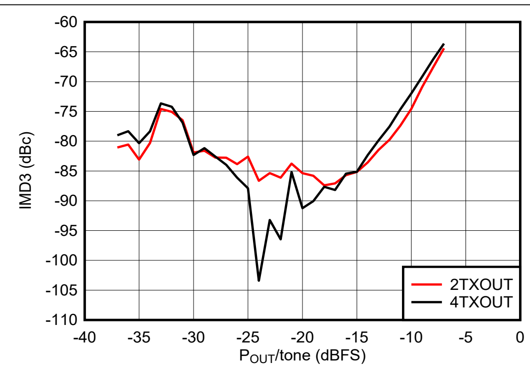
f_{DAC} = 5898.24 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 6-325. TX IMD3 vs Digital Level at 0.85 GHz



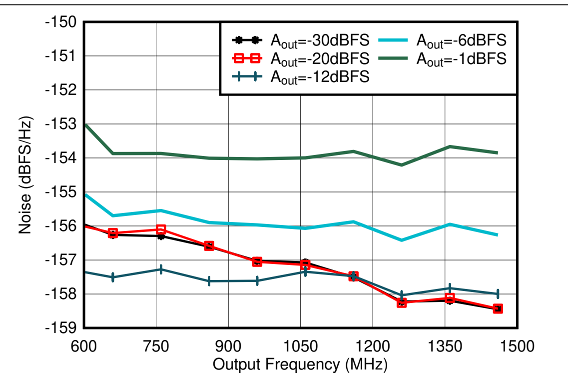
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 6-326. TX IMD3 vs Digital Level at 0.85 GHz



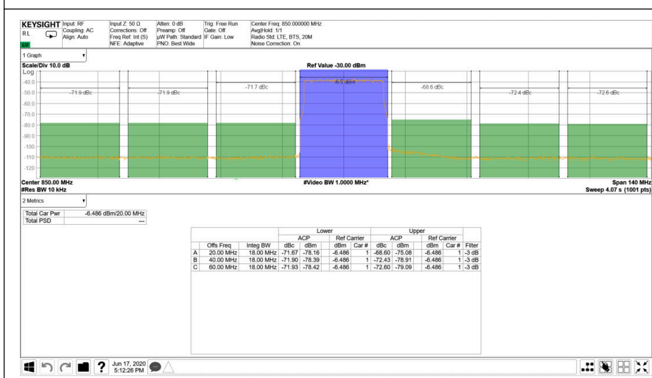
f_{DAC} = 11796.48 MSPS, interleave mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 6-327. TX IMD3 vs Digital Level at 0.85 GHz



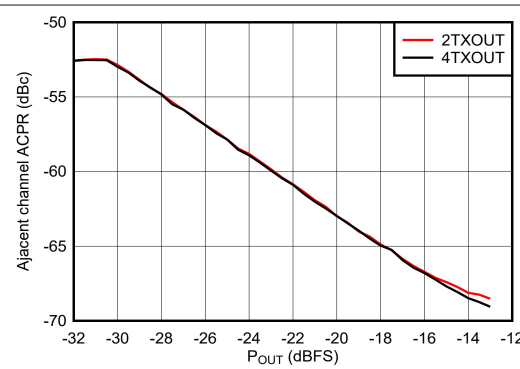
Matching at 0.8 GHz, Single tone, f_{DAC} = 11.79648 GSPS, interleave mode, 40-MHz offset, DSA = 0dB

図 6-328. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-329. TX 20-MHz LTE Output Spectrum at 0.85 GHz

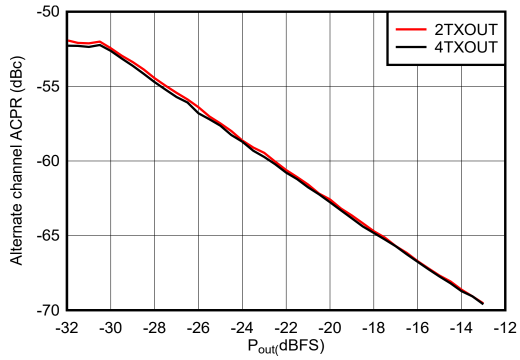


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-330. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

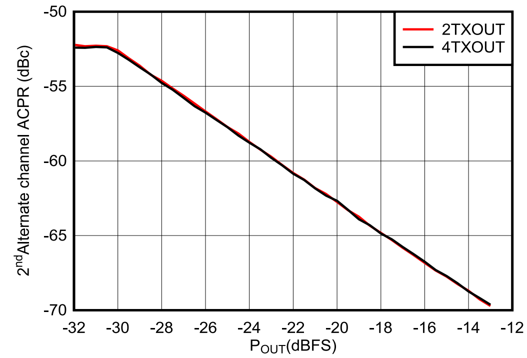
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



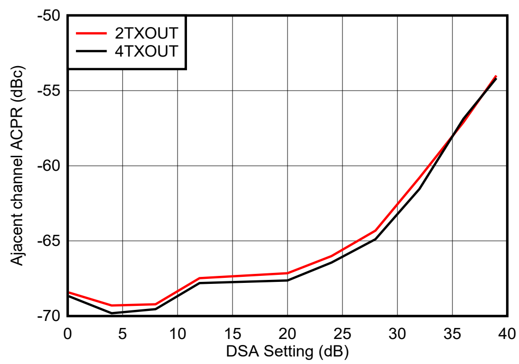
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-331. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz



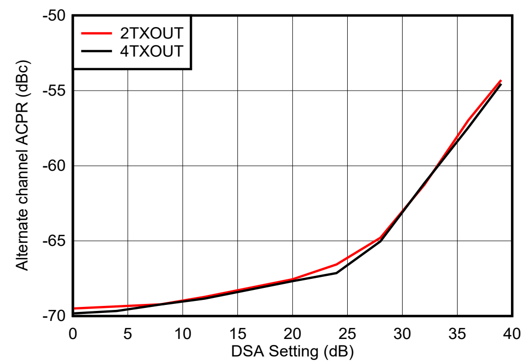
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-332. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz



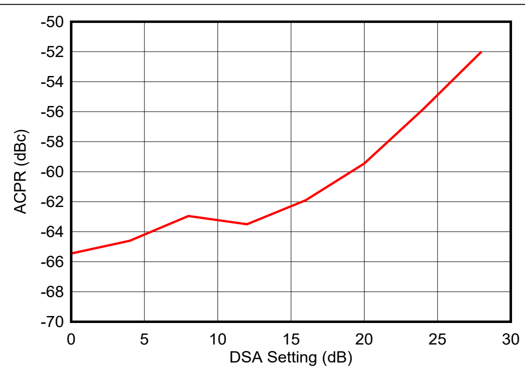
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-333. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



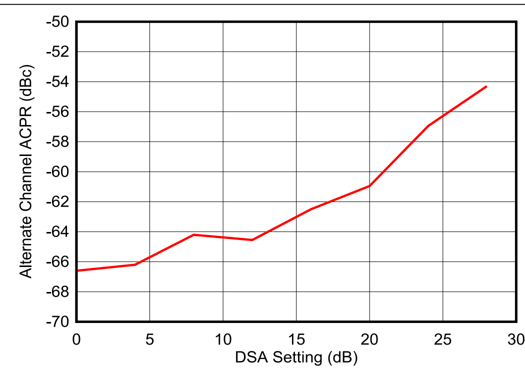
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-334. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-335. TX 100-MHz NR ACPR vs DSA at 0.85 GHz

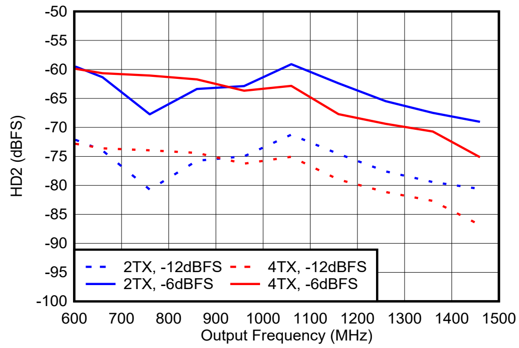


Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-336. TX 100-MHz NR alt-ACPR vs DSA at 0.85 GHz

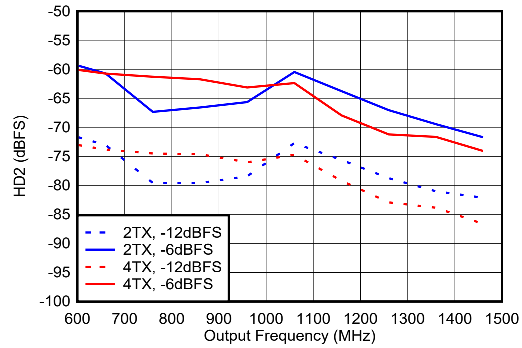
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



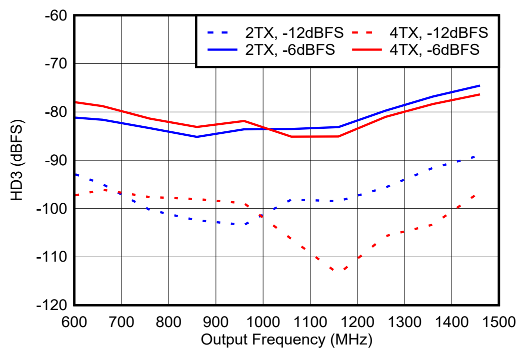
Matching at 0.8 GHz, f_{DAC} = 5898.24 GSPS, straight mode

図 6-337. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



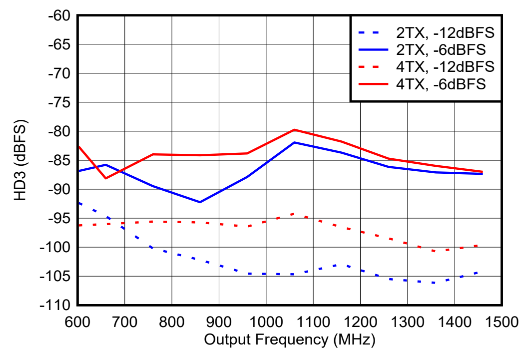
Matching at 0.8 GHz, f_{DAC} = 8847.36 GSPS, straight mode

図 6-338. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



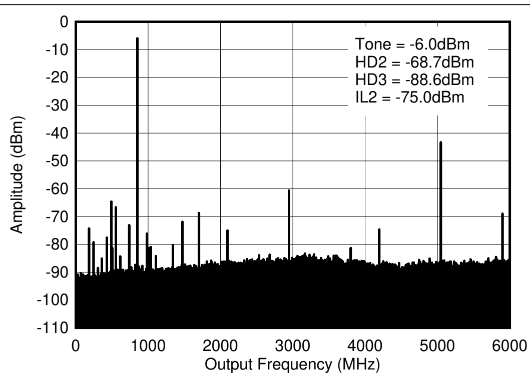
Matching at 0.8 GHz, f_{DAC} = 5898.24 MSPS, straight mode, normalized to output power at harmonic frequency

図 6-339. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



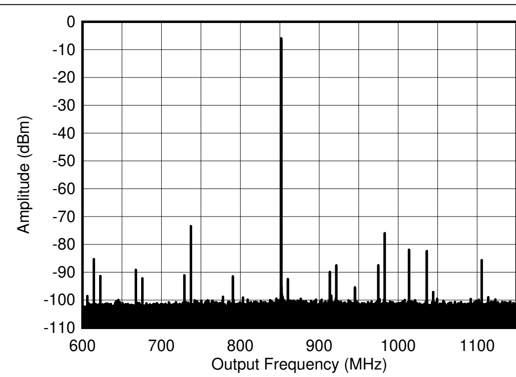
Matching at 0.8 GHz, f_{DAC} = 8847.36 MSPS, straight mode, normalized to output power at harmonic frequency

図 6-340. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-341. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

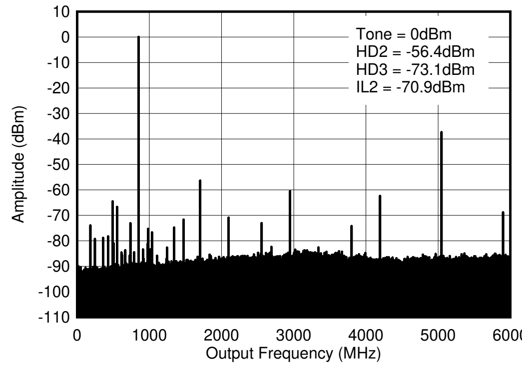


f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 6-342. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

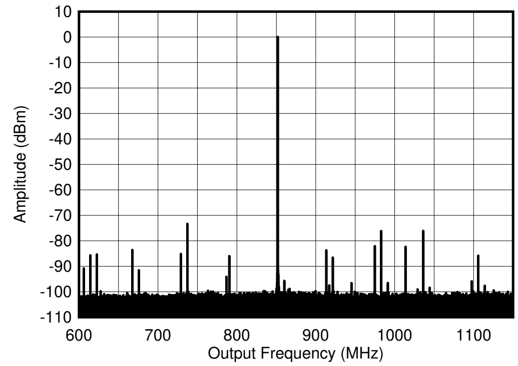
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



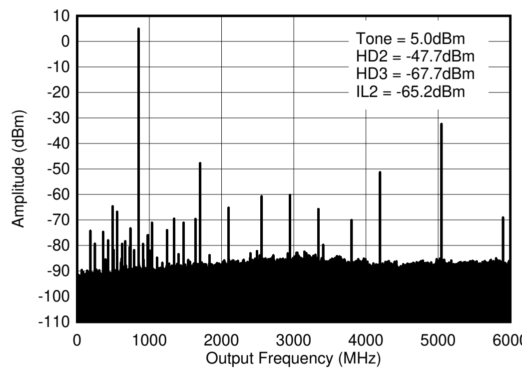
f_{DAC} = 5898.24 MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-343. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



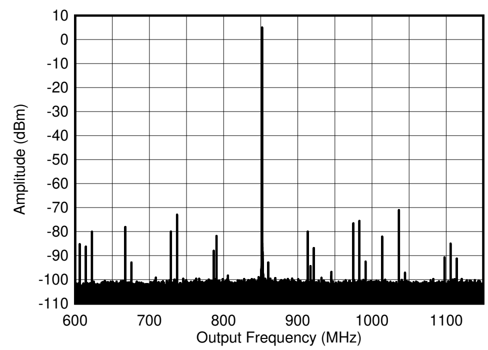
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 6-344. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



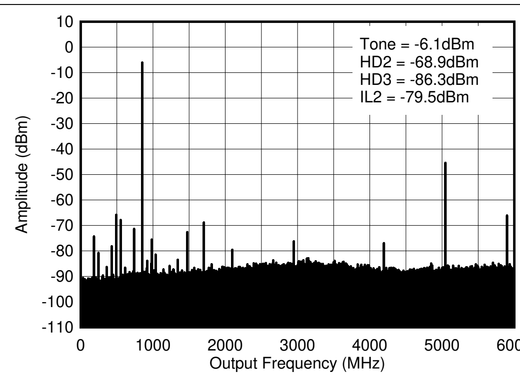
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-345. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



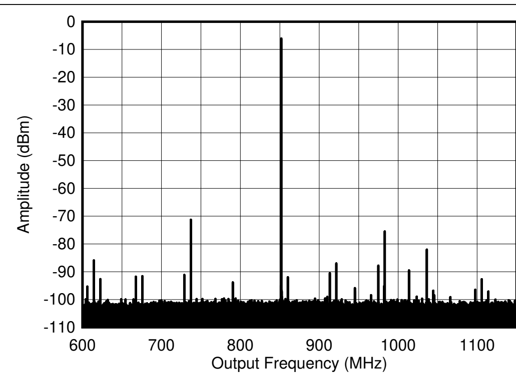
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 6-346. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-347. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

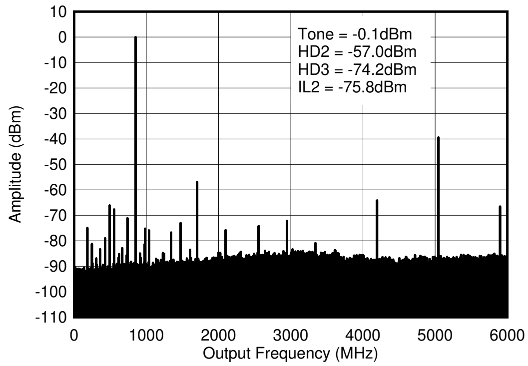


f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 6-348. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

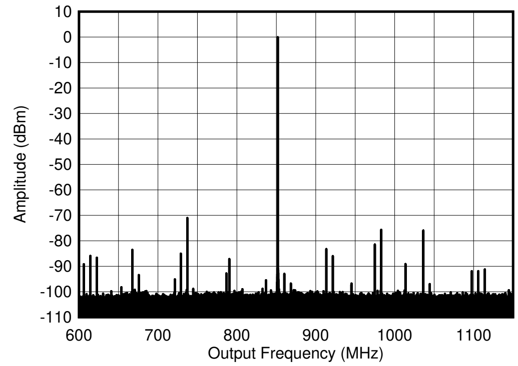
6.12.9 TX Typical Characteristics at 800 MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



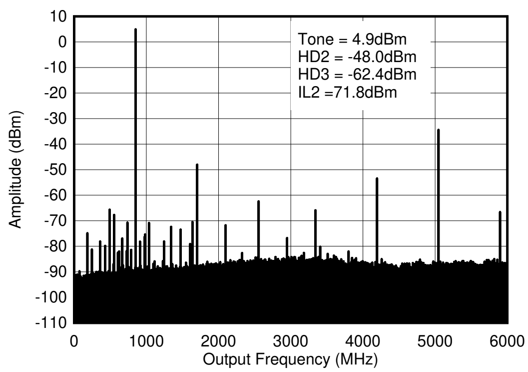
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-349. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



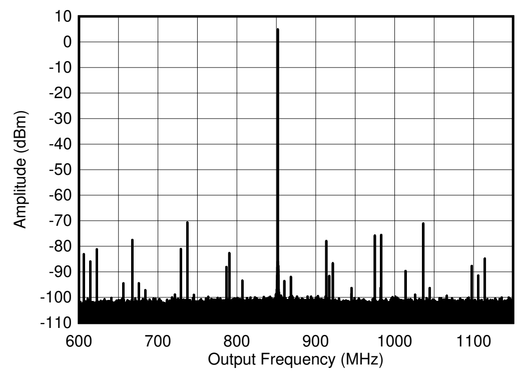
f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 6-350. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24 MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-351. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})

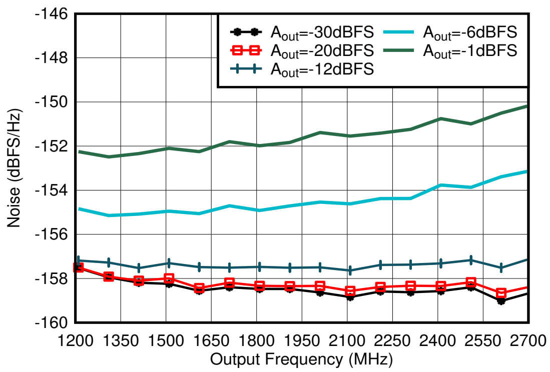


f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 6-352. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

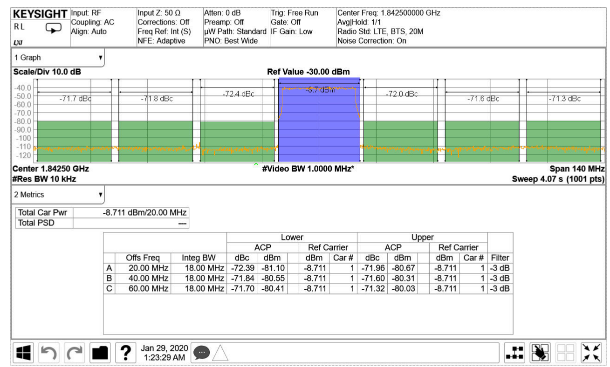
6.12.10 TX Typical Characteristics at 1.8 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



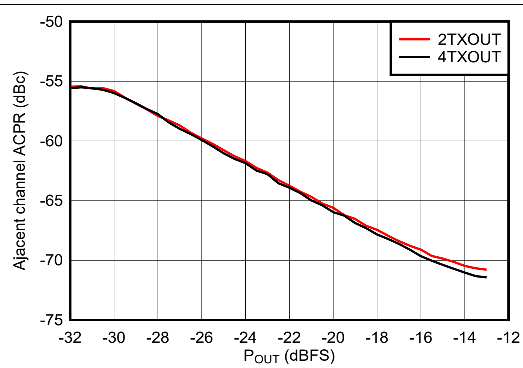
Matching at 1.8 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

図 6-353. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



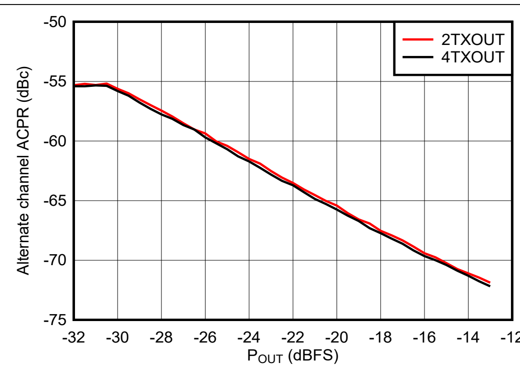
TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-354. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



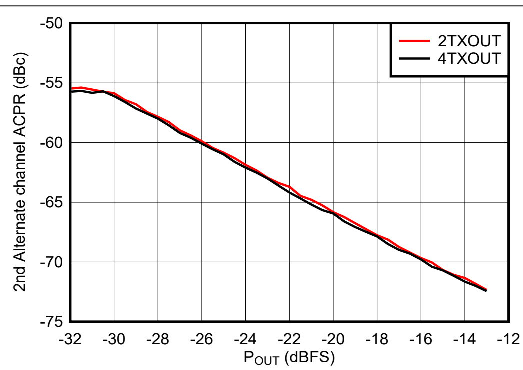
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-355. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



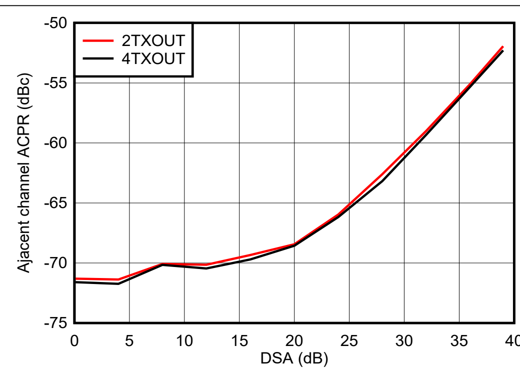
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-356. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-357. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz

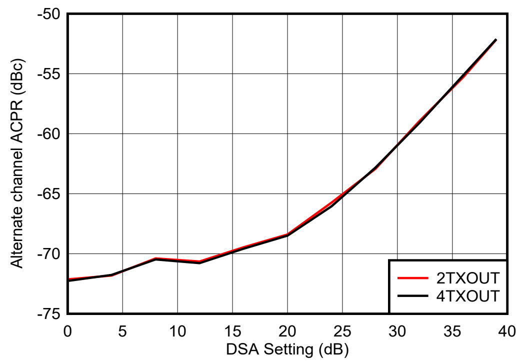


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-358. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

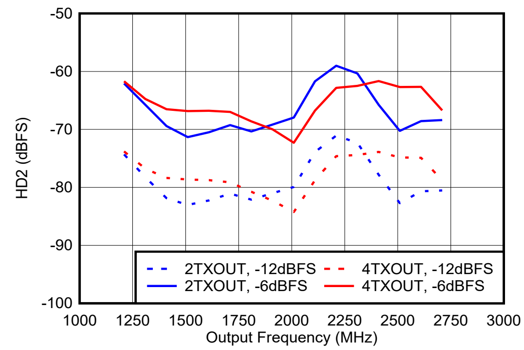
6.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



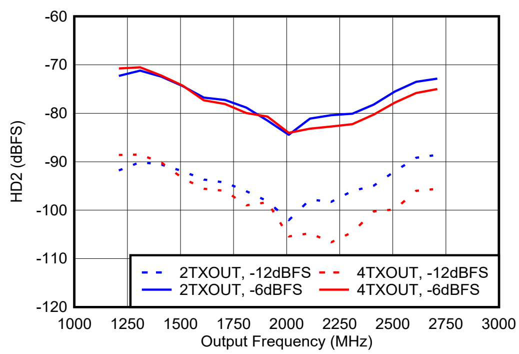
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-359. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



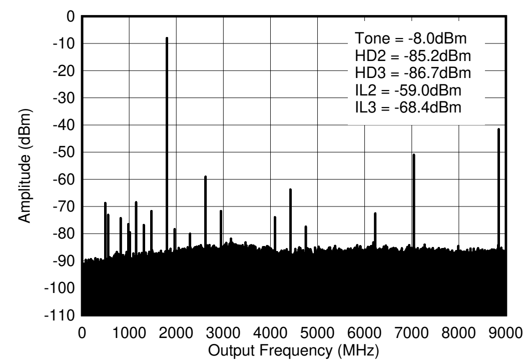
Matching at 1.8 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-360. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



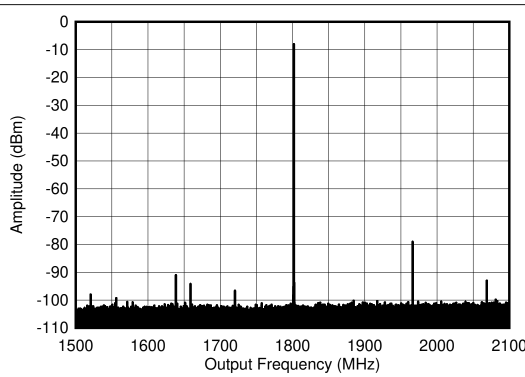
Matching at 1.8 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-361. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



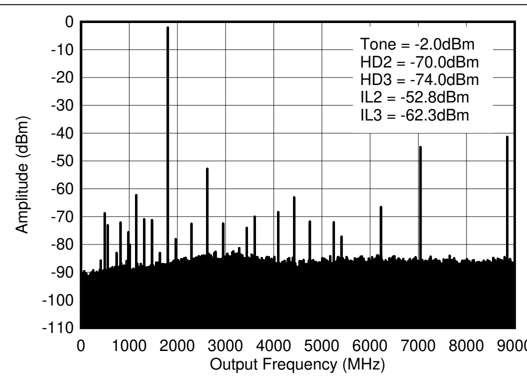
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-362. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 6-363. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

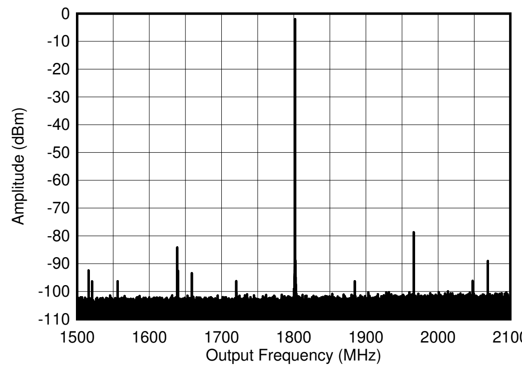


f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-364. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

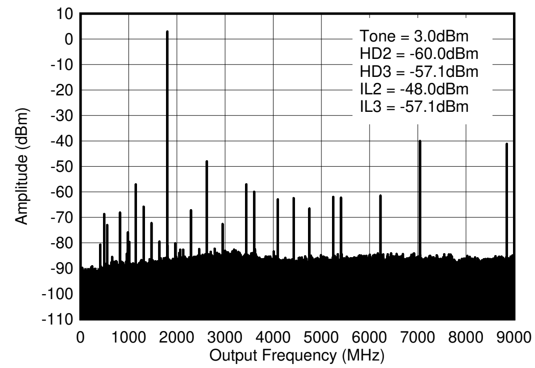
6.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



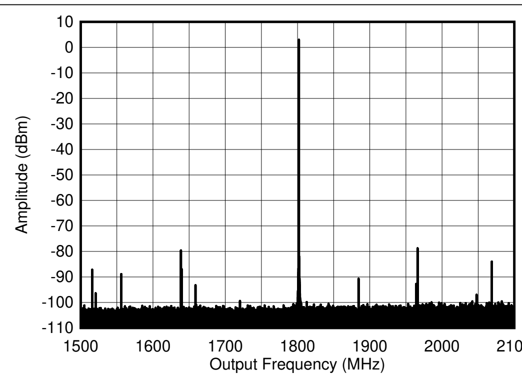
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 6-365. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



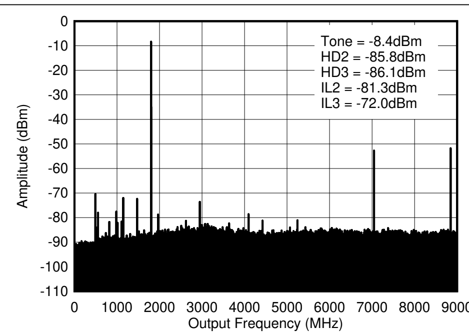
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-366. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



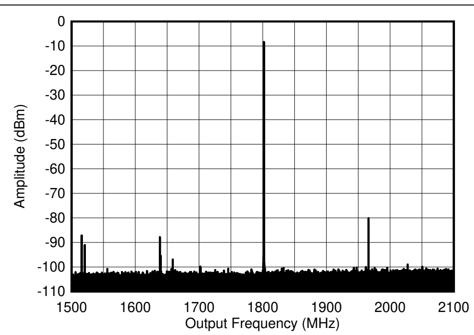
f_{DAC} = 8847.36 MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 6-367. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



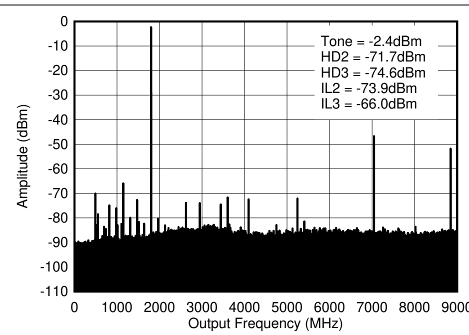
f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-368. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 6-369. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

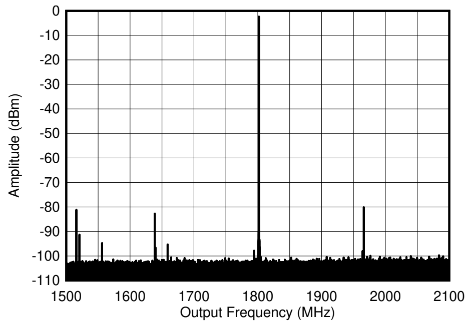


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-370. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

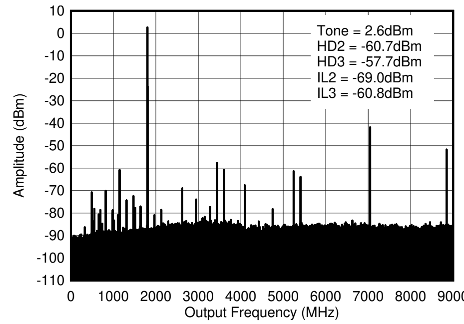
6.12.10 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



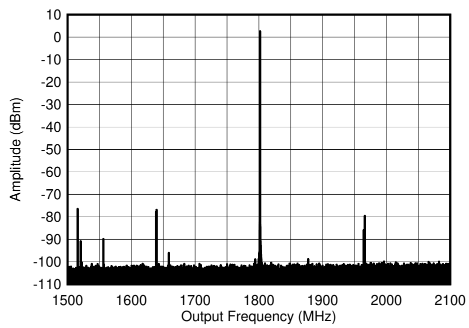
f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 6-371. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-372. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

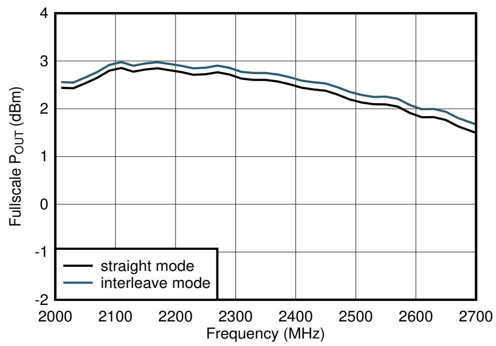


f_{DAC} = 8847.36 MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 6-373. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

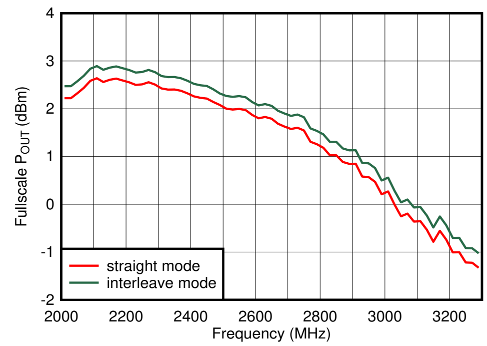
6.12.11 TX Typical Characteristics at 2.6 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



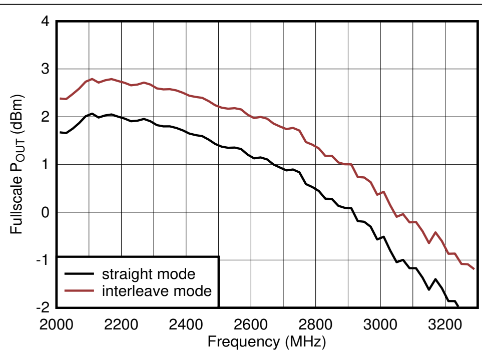
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

図 6-374. TX Full Scale vs RF Frequency at 5898.24 MSPS



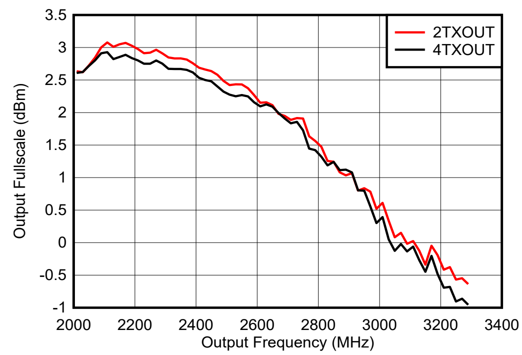
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

図 6-375. TX Full Scale vs RF Frequency at 8847.36 MSPS



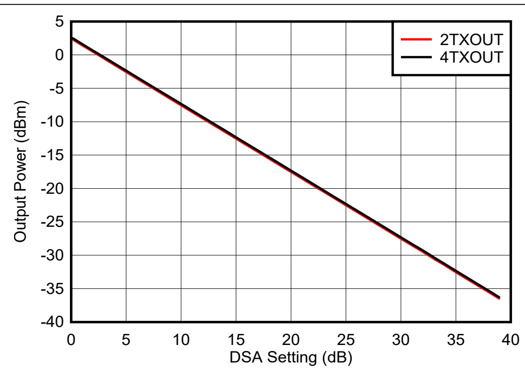
Including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

図 6-376. TX Full Scale vs RF Frequency at 11796.48 MSPS



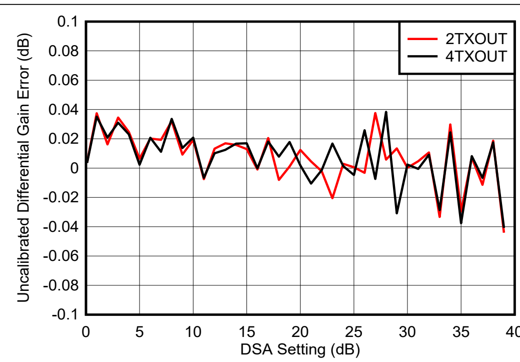
f_{DAC} = 8847.36 MSPS, interleave mode, including PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 2.6 GHz matching

図 6-377. TX Output Fullscale vs Output Frequency and Channel



f_{DAC} = 8847.36 MSPS, A_{out} = -0.5 dBFS, matching 2.6 GHz

図 6-378. TX Output Power vs DSA Setting and Channel at 2.6 GHz

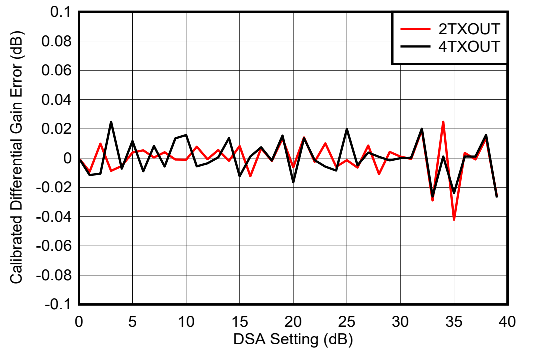


f_{DAC} =8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-379. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

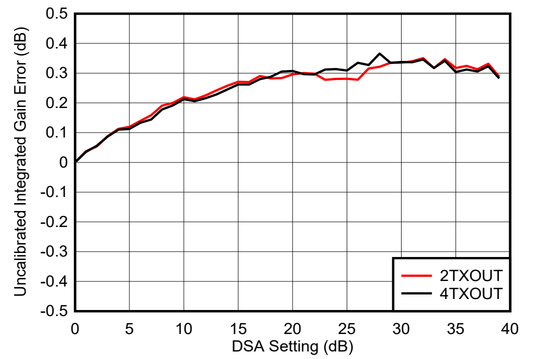
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



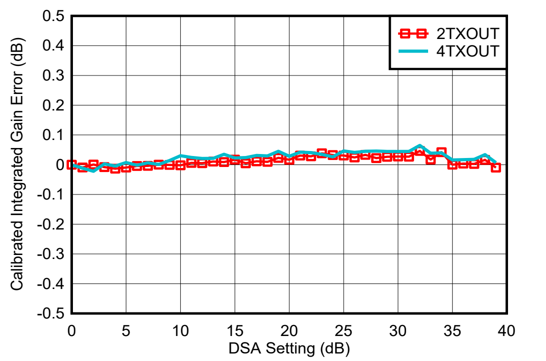
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-380. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



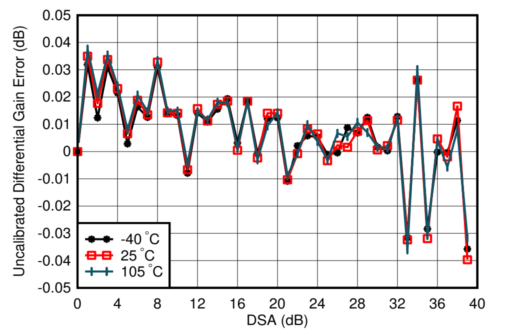
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-381. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-382. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

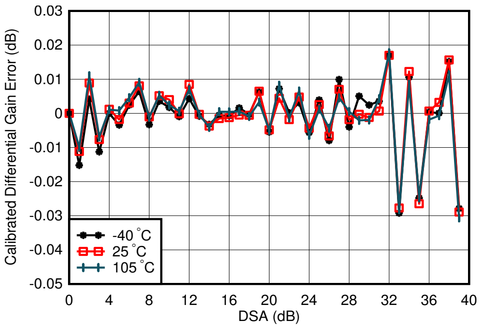


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-383. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz

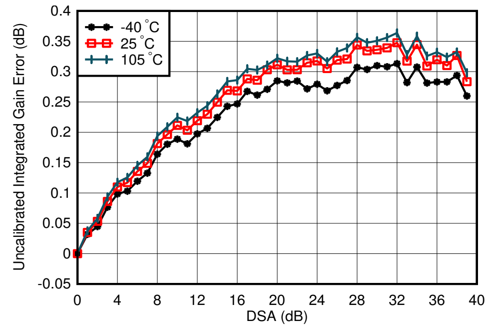
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



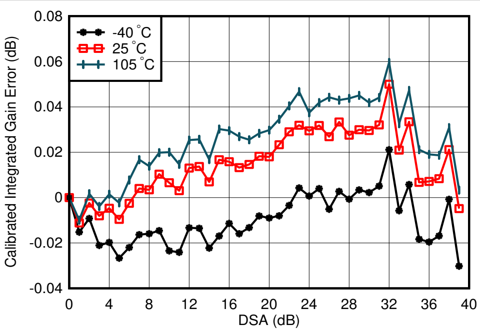
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-384. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



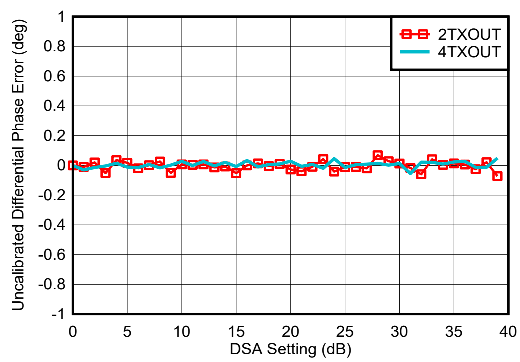
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-385. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-386. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

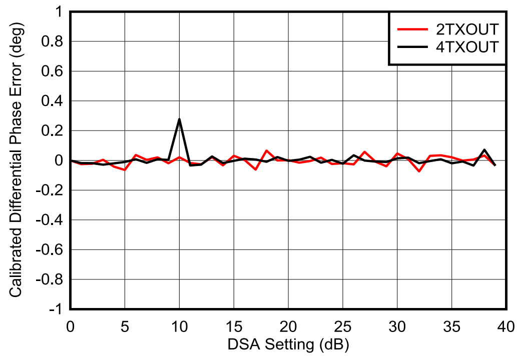


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-387. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz

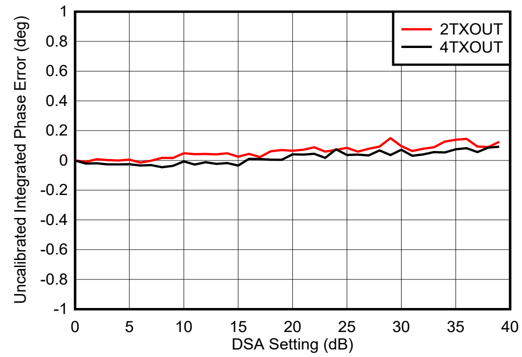
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



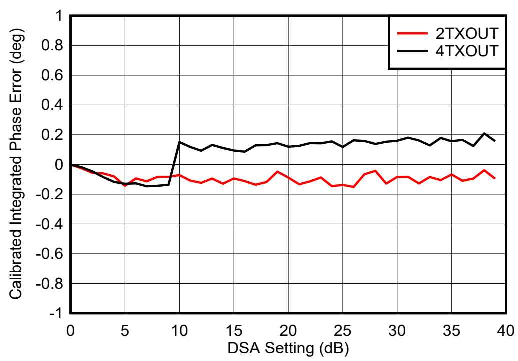
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 6-388. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



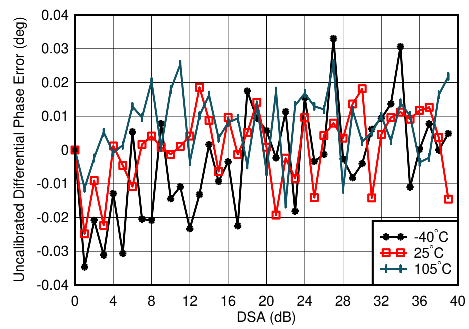
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-389. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-390. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

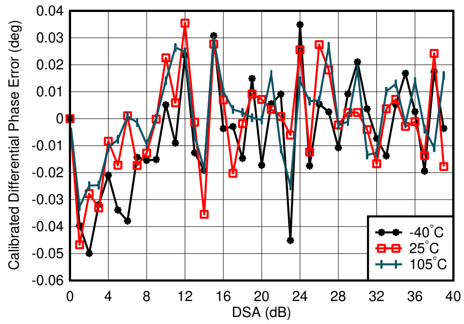


f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-391. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz

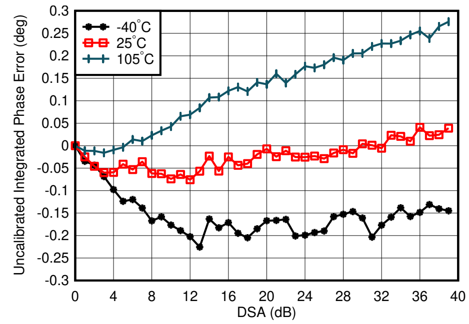
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



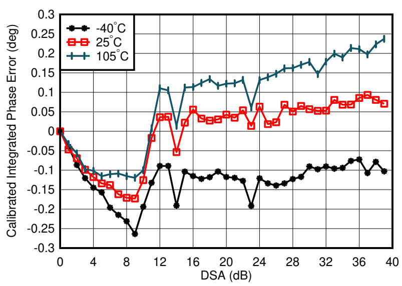
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-392. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



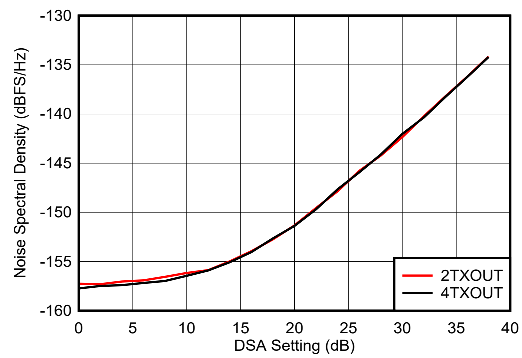
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-393. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



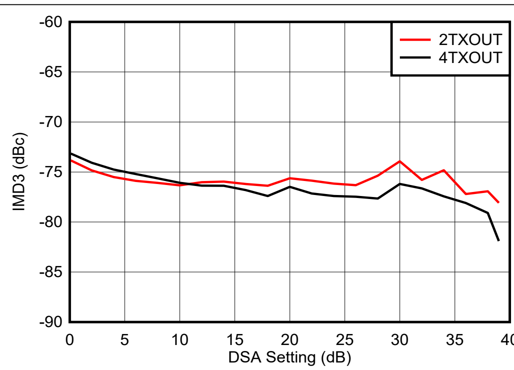
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-394. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



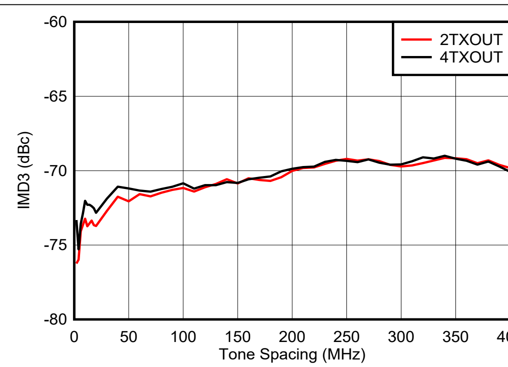
f_{DAC} = 8847.36 MSPS, straight mode, matching at 2.6 GHz, P_{OUT} = –13 dBFS

図 6-395. TX Output Noise vs Channel and Attenuation at 2.6 GHz



f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 6-396. TX IMD3 vs DSA Setting at 2.6 GHz

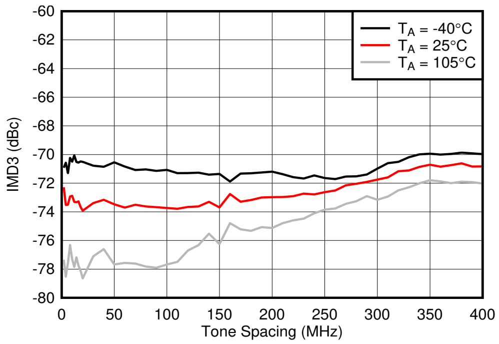


f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 6-397. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz

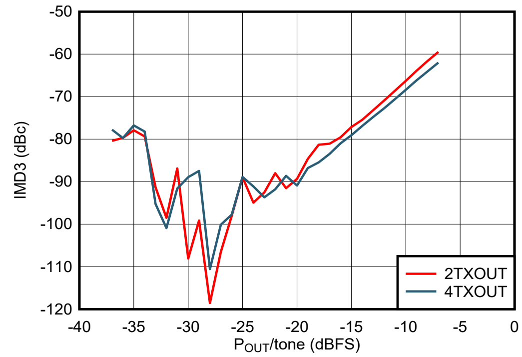
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



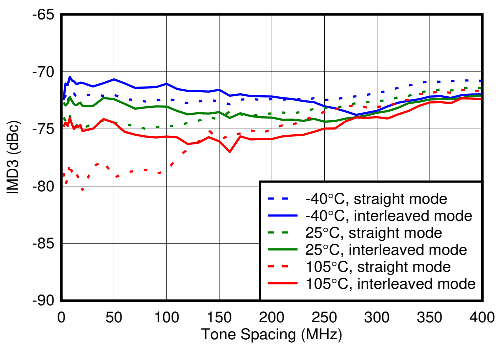
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone, worst channel, dither = 1.

図 6-398. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



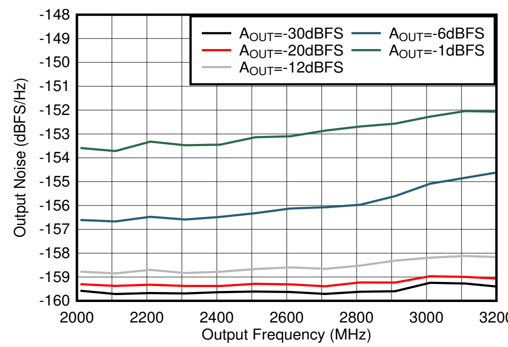
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, $f_{SPACING}$ = 20 MHz, dither = 1, matching at 2.6 GHz

図 6-399. TX IMD3 vs Digital Level at 2.6 GHz



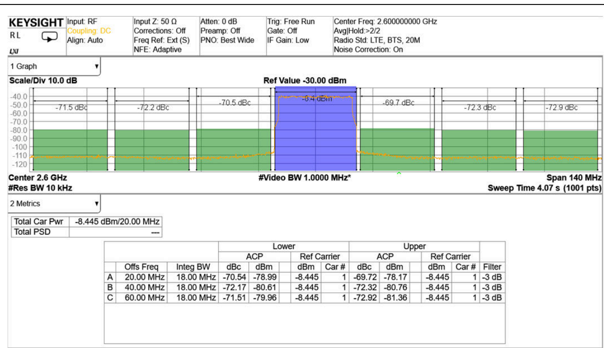
f_{DAC} = 8847.36 MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 6-400. TX IMD3 vs Tone Spacing and Temperature



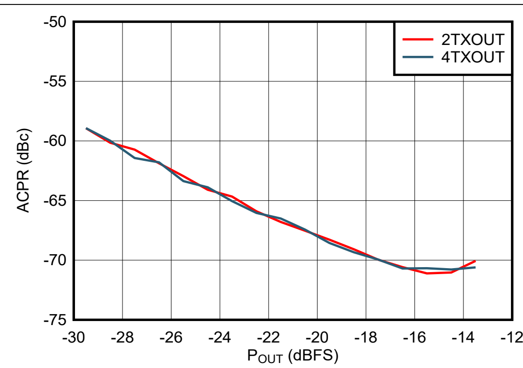
Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

図 6-401. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz



TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-402. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)

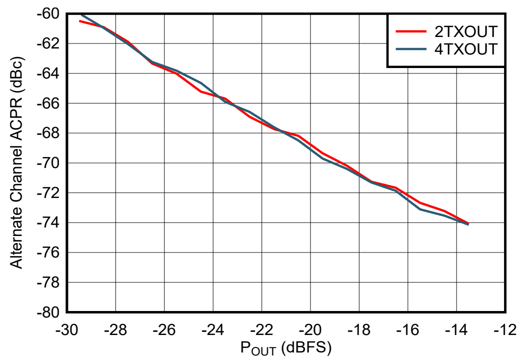


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-403. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz

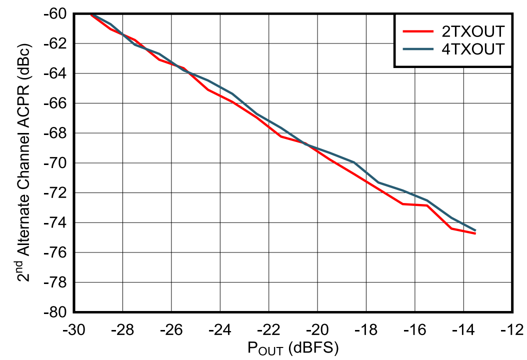
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



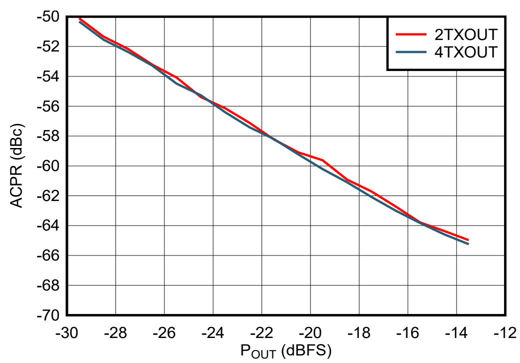
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-404. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



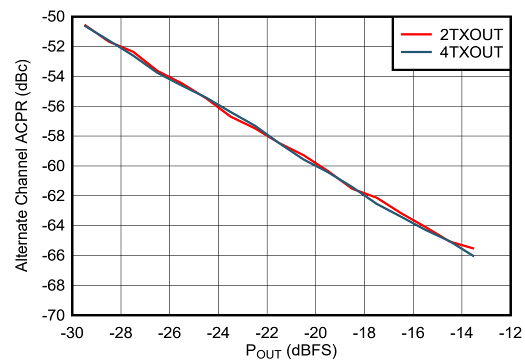
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-405. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz



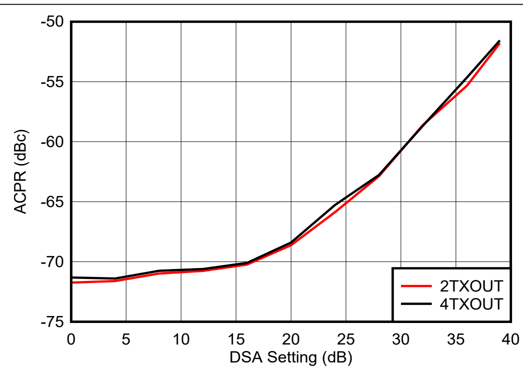
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-406. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz



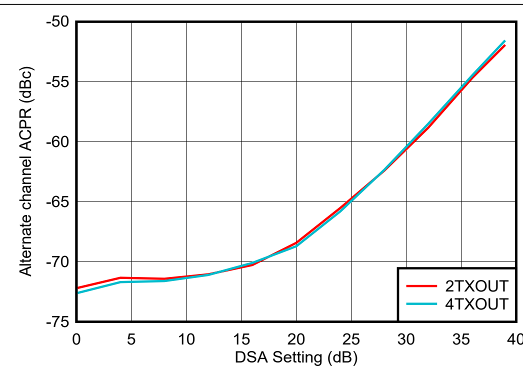
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-407. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-408. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

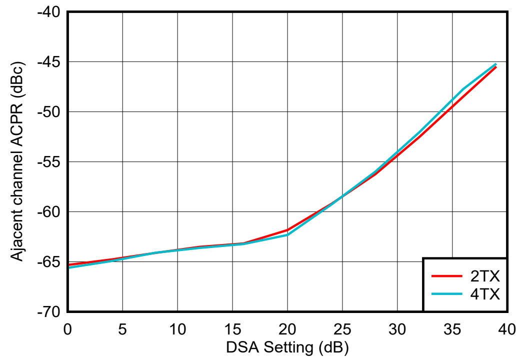


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-409. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

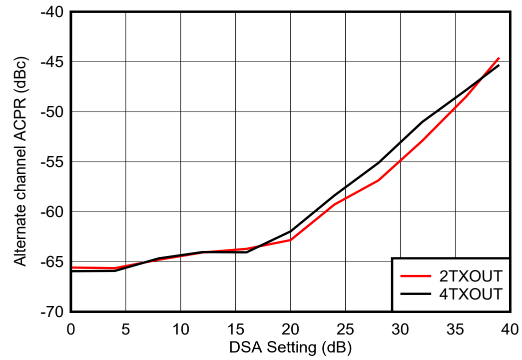
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



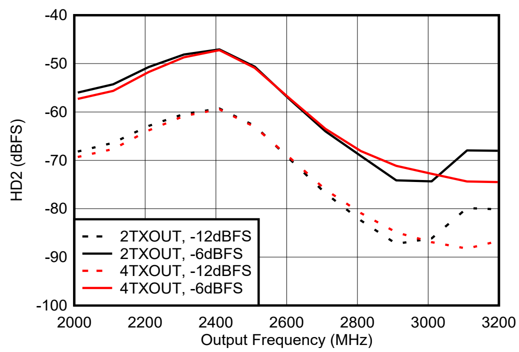
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-410. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



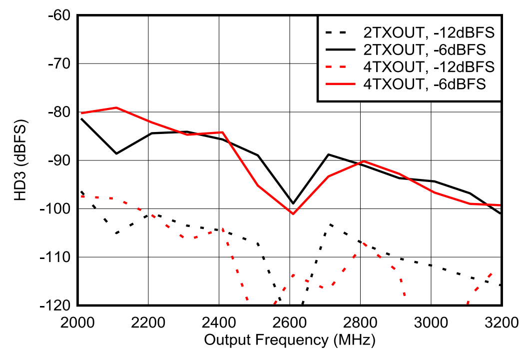
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-411. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



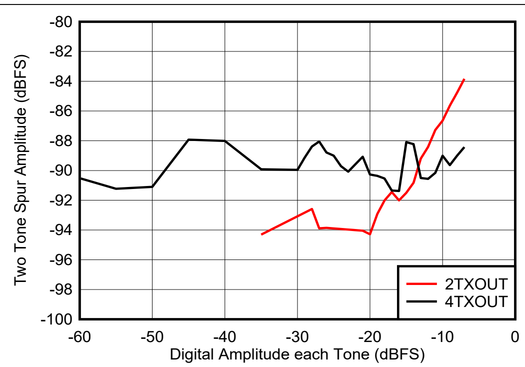
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-412. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



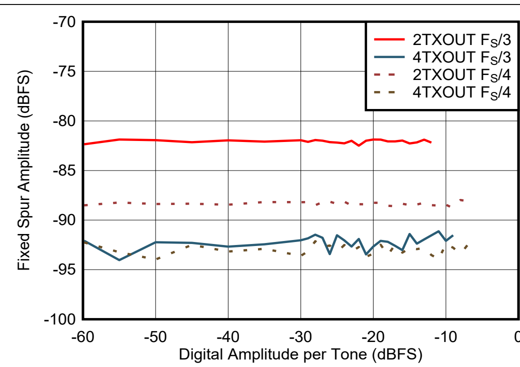
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-413. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz



Inband = 2600 MHz ± 600 MHz, f_{DAC} = 12 GSPS, not including F_S/3 and F_S/4, external clock mode, non-interleave mode

図 6-414. Two Tone Inband SFDR vs Digital Amplitude at 2.6 GHz

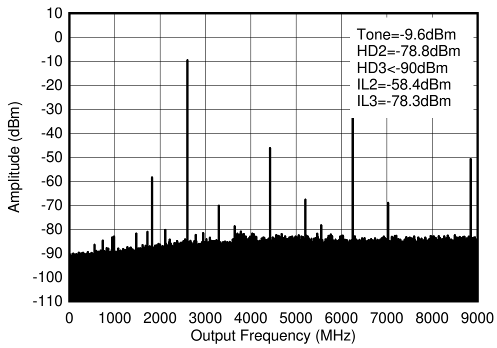


Inband = 2600 MHz ± 600 MHz, f_{DAC} = 12 GSPS, external clock mode, non-interleave mode

図 6-415. Two Tone Inband Fixed Spurs vs Digital Amplitude at 2.6 GHz

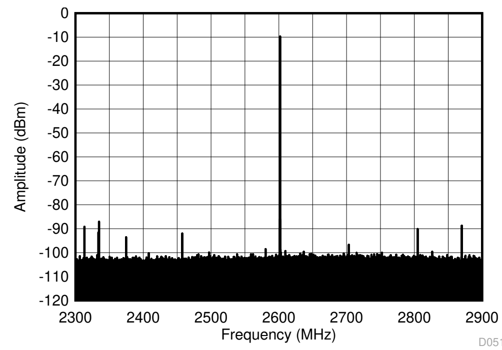
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



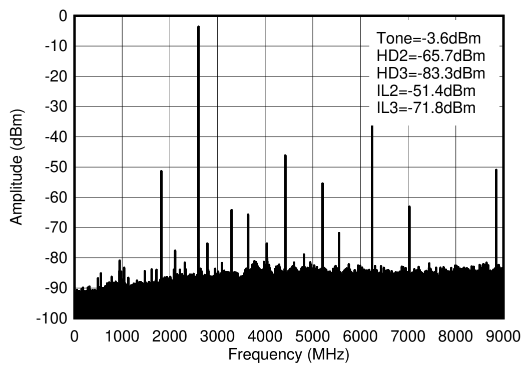
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-416. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



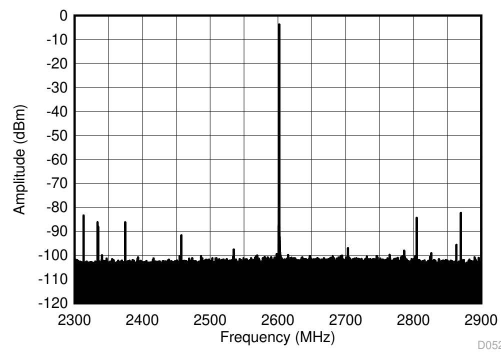
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 6-417. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



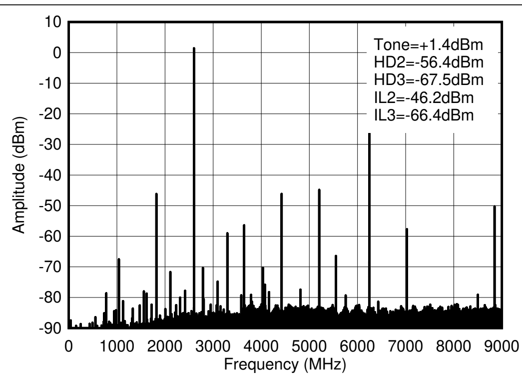
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-418. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



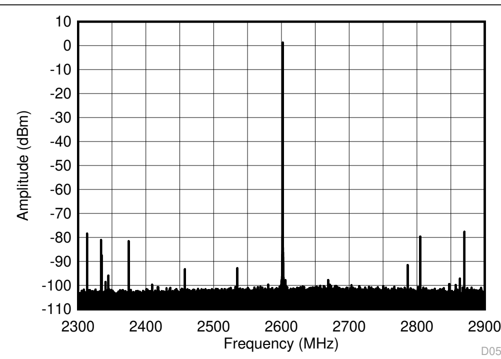
f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 6-419. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-420. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

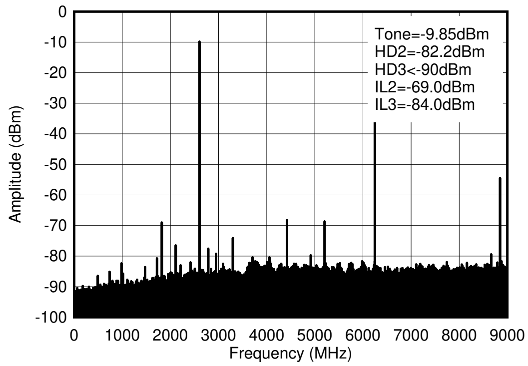


f_{DAC} = 8847.36 MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 6-421. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

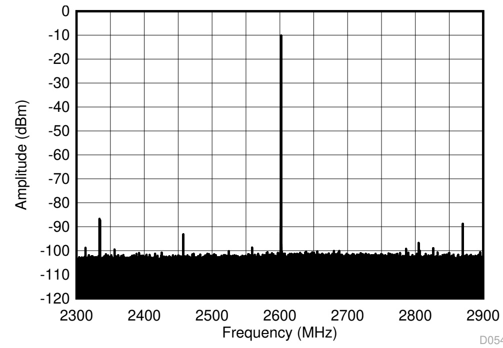
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



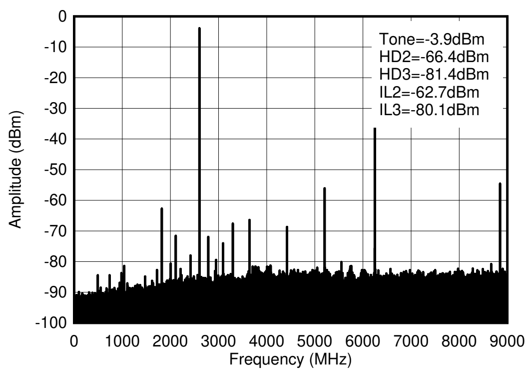
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-422. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



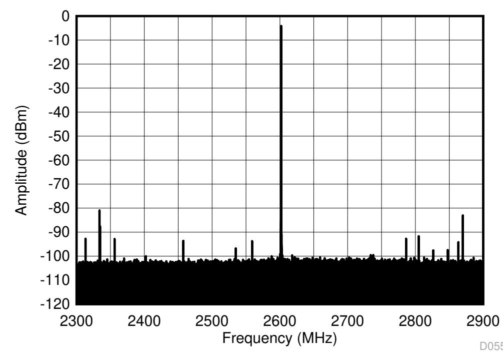
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 6-423. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-424. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})

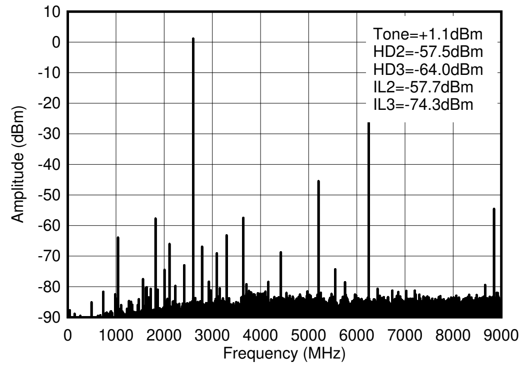


f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 6-425. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

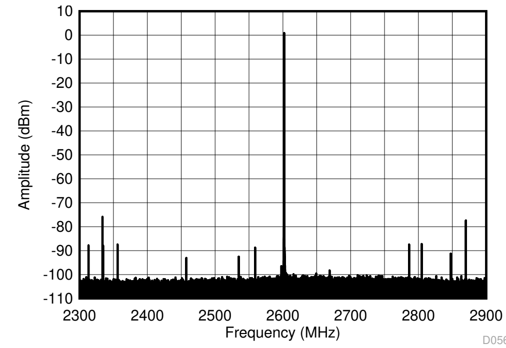
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



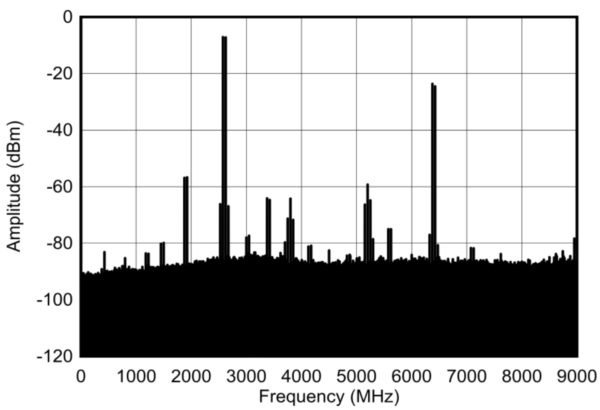
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT} and is due to mixing with digital clocks.

図 6-426. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



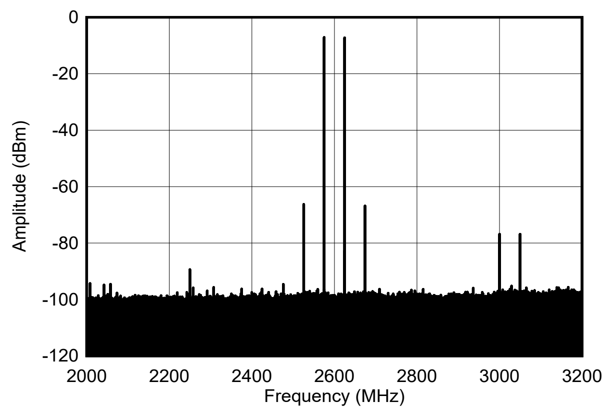
f_{DAC} = 8847.36 MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 6-427. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



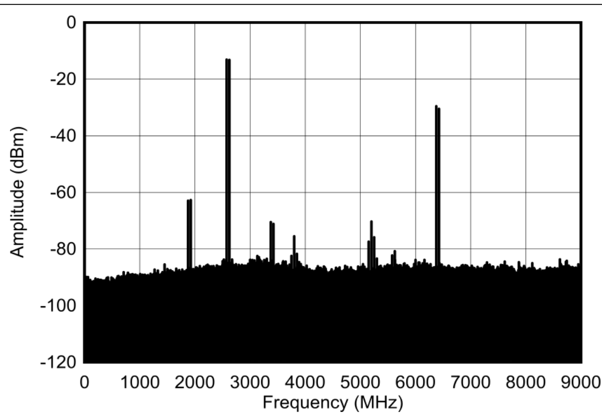
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-428. TX Dual Tone Output Spectrum at 2.6 GHz, -7 dBFS each (0 - $_{DAC}$)



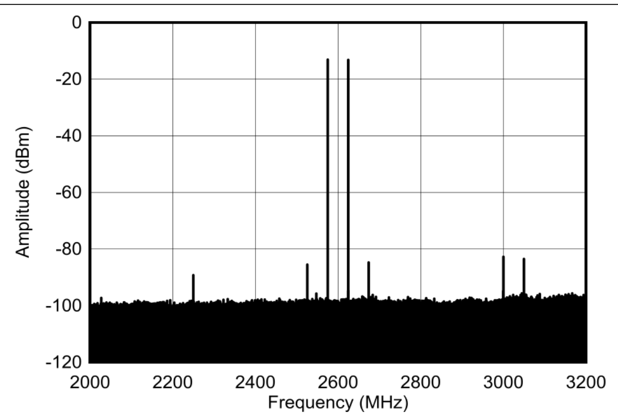
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-429. TX Dual Tone Output Spectrum at 2.6 GHz, -7 dBFS each (±600 MHz)



f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-430. TX Dual Tone Output Spectrum at 2.6 GHz, -13 dBFS each (0 - $_{DAC}$)

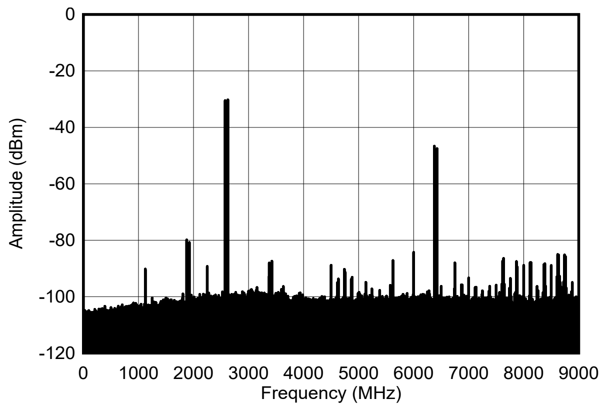


f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-431. TX Dual Tone Output Spectrum at 2.6 GHz, -13 dBFS each (±600 MHz)

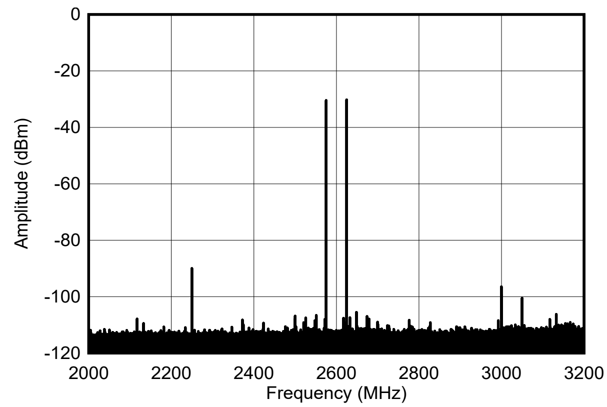
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



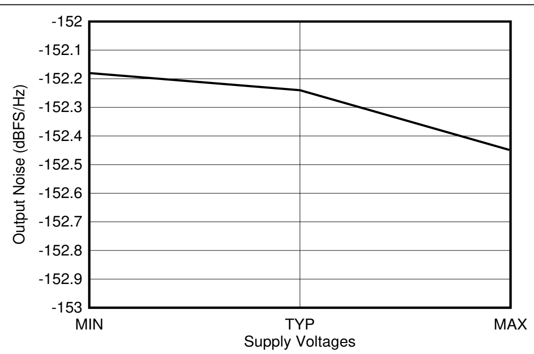
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-432. TX Dual Tone Output Spectrum at 2.6 GHz, -30 dBFS each (0 - $_{DAC}$)



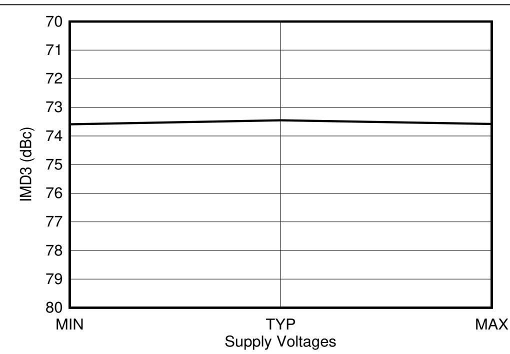
f_{DAC} = 9000 MSPS, external clock mode, non-interleave mode

図 6-433. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each (±600 MHz)



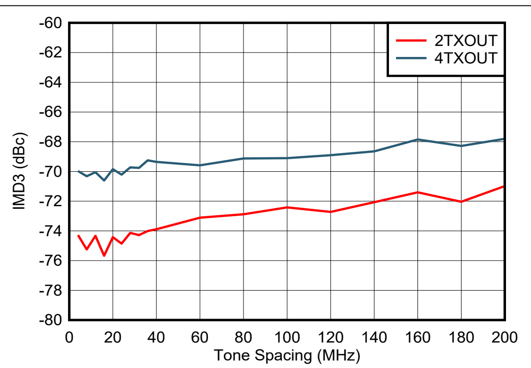
f_{DAC} = 11796.48 MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –1 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

図 6-434. TX Output Noise vs Supply Voltage at 2.6 GHz



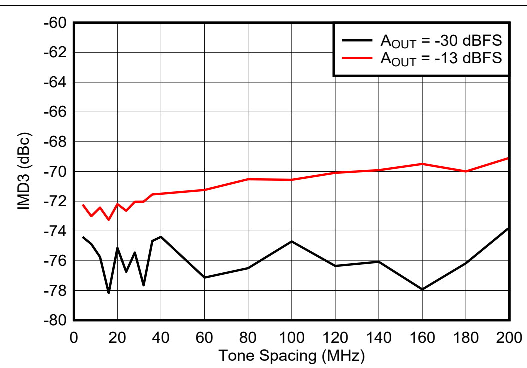
f_{DAC} = 11796.48 MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

図 6-435. TX IMD3 vs Supply Voltage at 2.6 GHz



f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

図 6-436. IMD3 vs Tone Spacing and Channel at 2.6 GHz

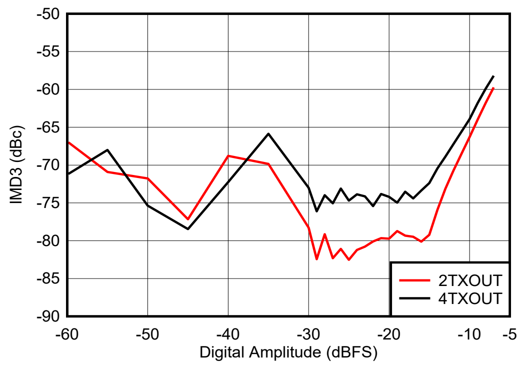


f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

図 6-437. IMD3 vs Tone Spacing and Amplitude at 2.6 GHz

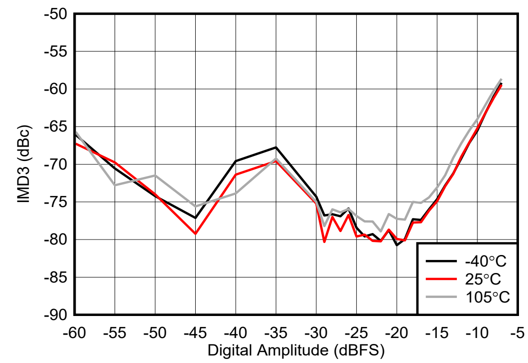
6.12.11 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



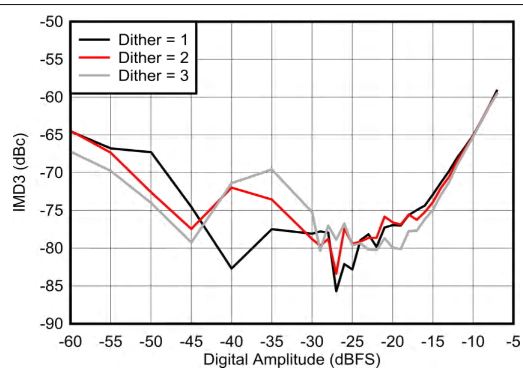
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

図 6-438. IMD3 vs Digital Amplitude and Channel at 2.6 GHz



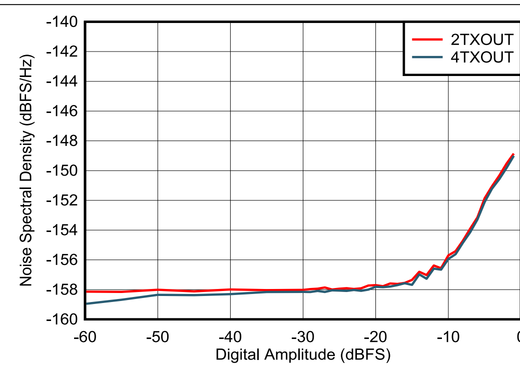
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

図 6-439. IMD3 vs Digital Amplitude and Temperature at 2.6 GHz



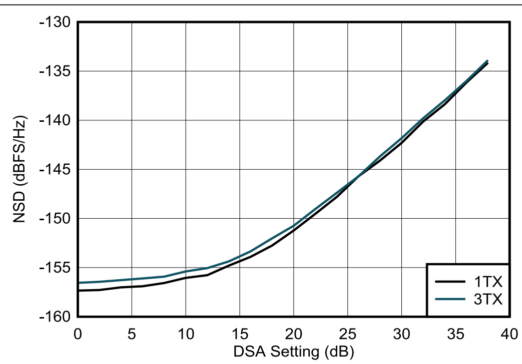
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode

図 6-440. IMD3 vs Digital Amplitude and Dither at 2.6 GHz



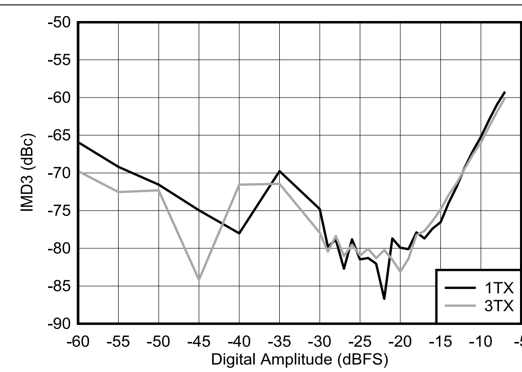
f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode, 50 MHz offset

図 6-441. NSD vs Digital Amplitude and Channel at 2.6 GHz



f_{DAC} = 9000 MSPS, non-interleave mode, external clock mode, 50 MHz offset

図 6-442. NSD vs Digital Amplitude and Temperature at 2.6 GHz

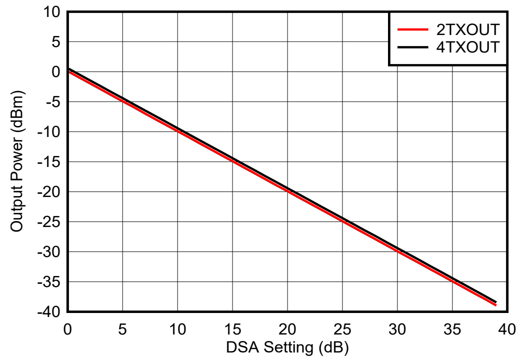


f_{DAC} = f_{CLK} = 9000 MSPS, non-interleave mode

図 6-443. External Clock Additive Phase Noise at 2.6 GHz

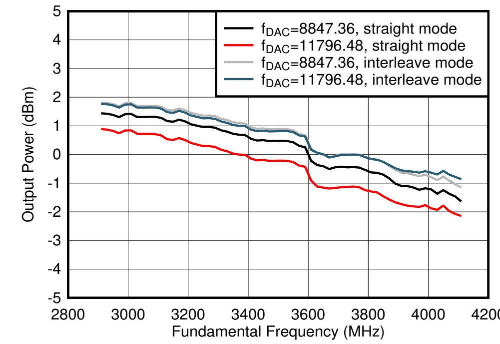
6.12.12 TX Typical Characteristics at 3.5 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



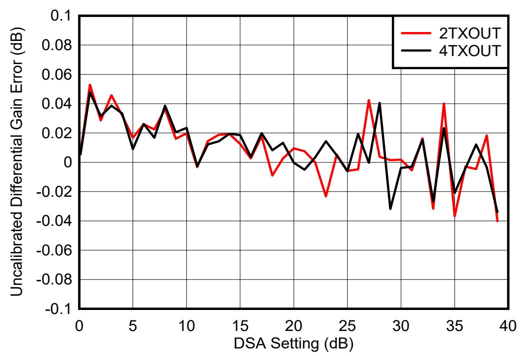
A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

図 6-444. TX Output Power vs DSA Setting at 3.5 GHz



A_{out} = -0.5 dFBS, 3.5 GHz Matching, included PCB and cable losses

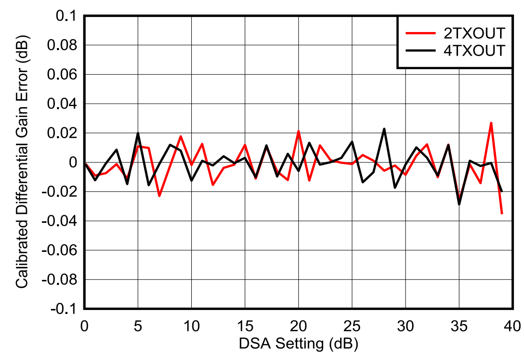
図 6-445. TX Output Power vs Frequency



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

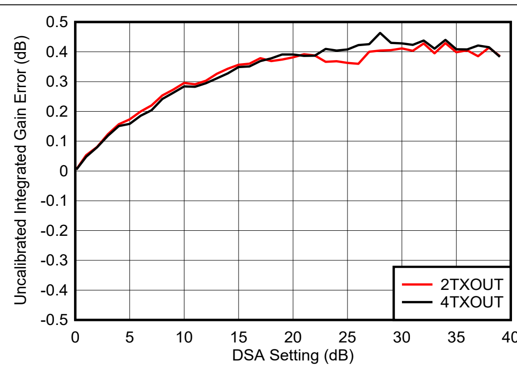
図 6-446. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

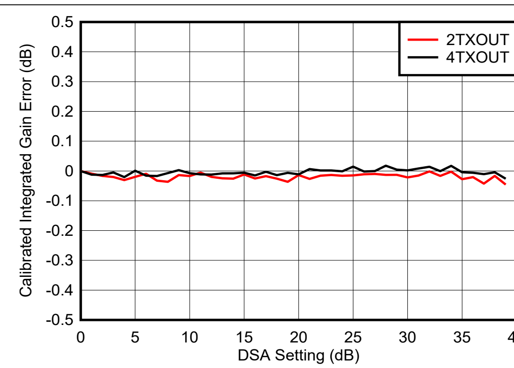
図 6-447. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-448. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



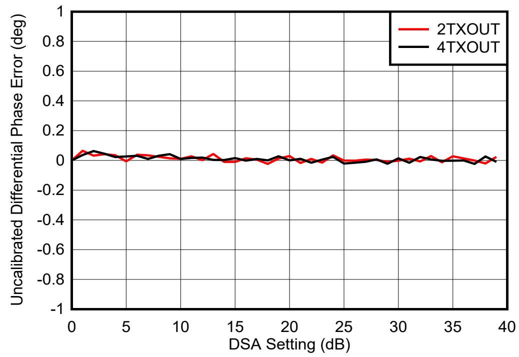
3.5 GHz Matching, included PCB and cable losses

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-449. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

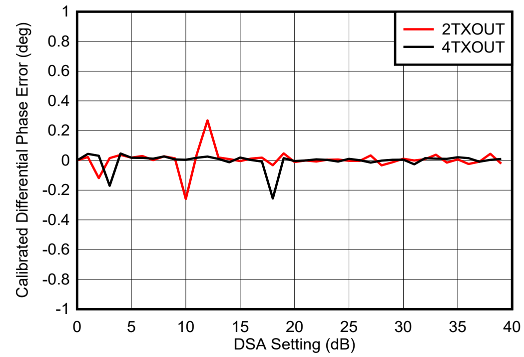
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1^{st} Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



3.5 GHz Matching, included PCB and cable losses

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

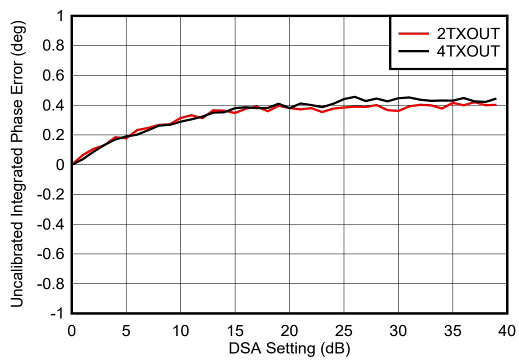
図 6-450. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting). Phase DNL spike may occur at any DSA setting.

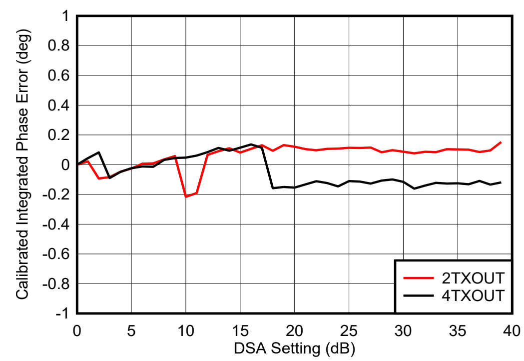
図 6-451. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-452. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



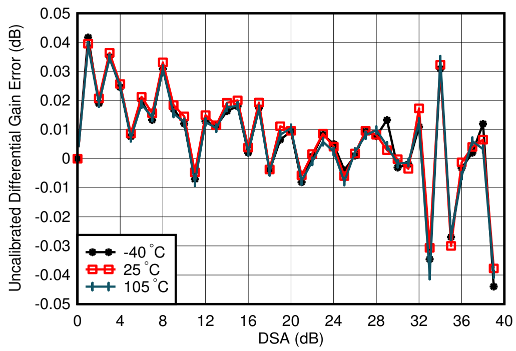
3.5 GHz Matching, included PCB and cable losses

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-453. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz

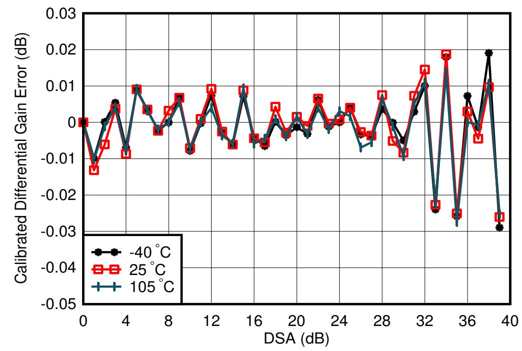
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



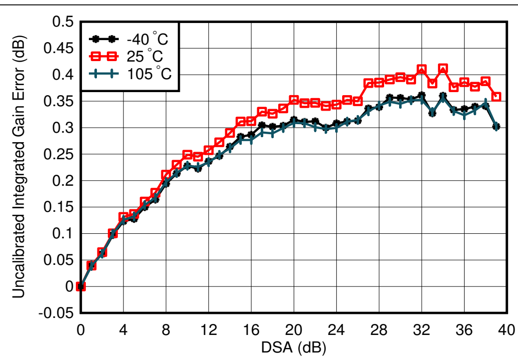
3.5 GHz Matching, 1TX
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-454. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



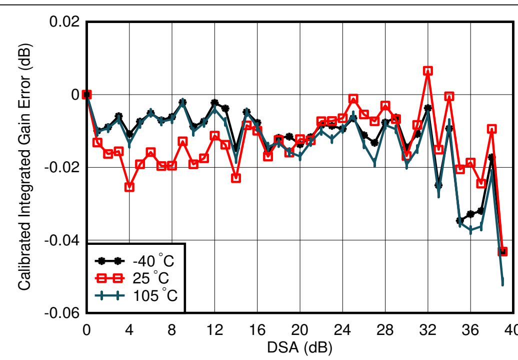
3.5 GHz Matching, 1TX, Calibrated at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-455. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-456. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz

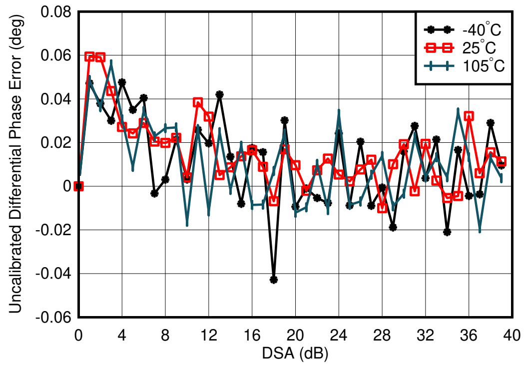


3.5 GHz Matching, 1TX, Calibrated at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-457. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz

6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

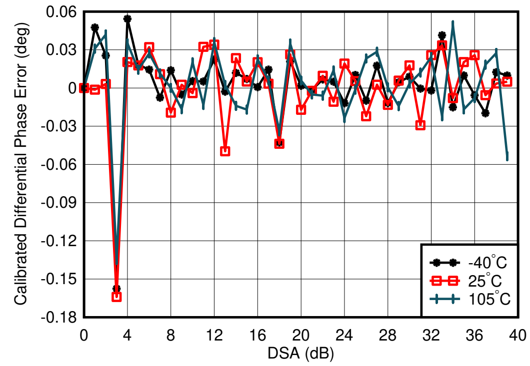
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



3.5 GHz Matching, 1TX

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

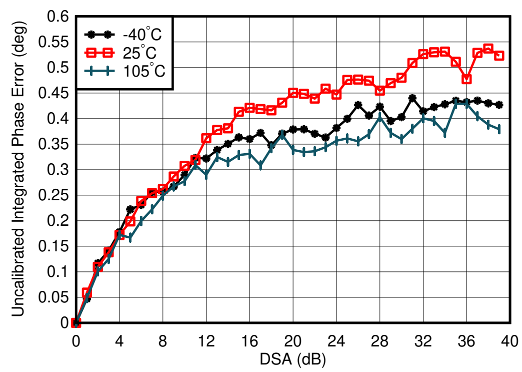
図 6-458. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

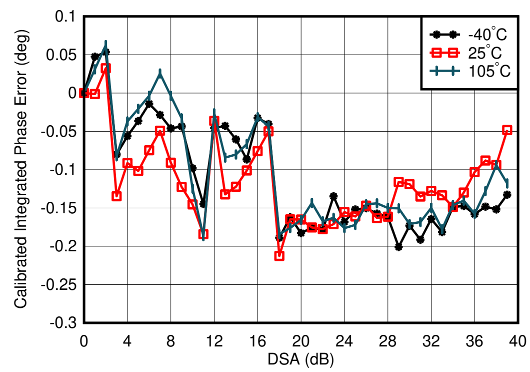
図 6-459. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

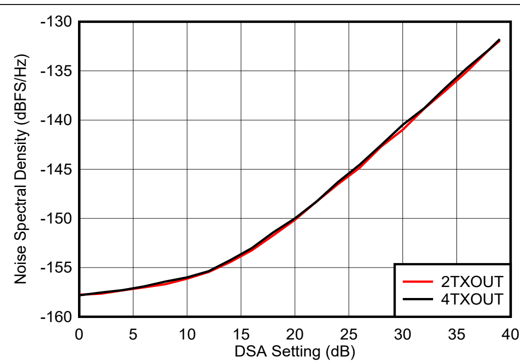
図 6-460. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

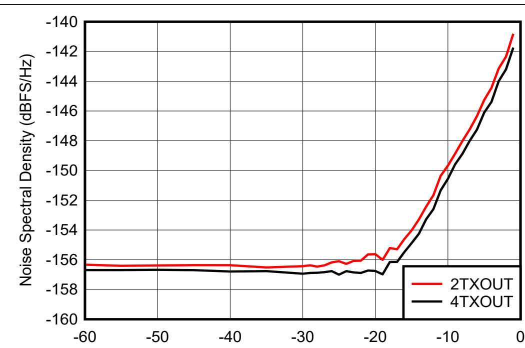
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-461. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



A. f_{DAC} = 11796.48 MSPS, interleave mode, matching at 3.5 GHz, A_{out} = –13 dBFS.

図 6-462. TX NSD vs DSA Setting at 3.5 GHz

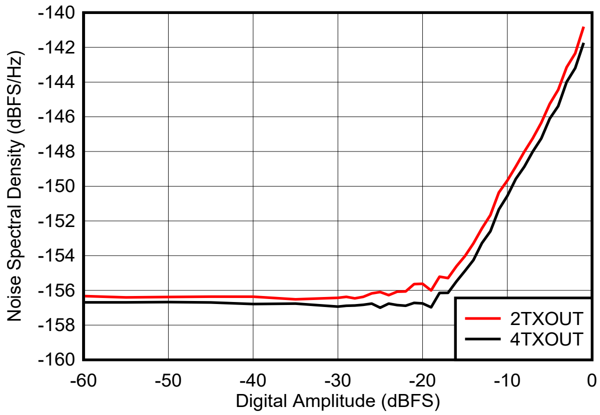


A. f_{DAC} = 12 MSPS, external clock mode, non-interleave mode

図 6-463. TX NSD vs Digital Amplitude and Temperature at 3.75 GHz

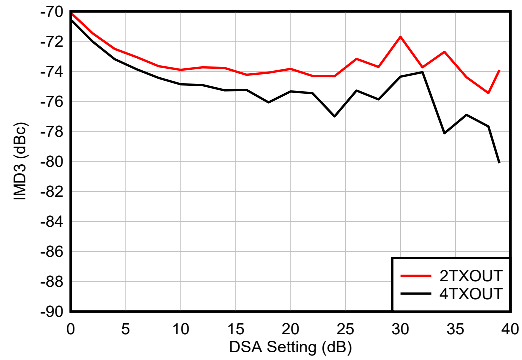
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



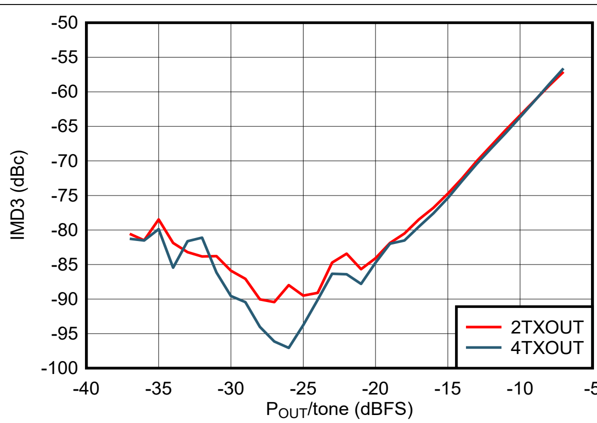
A. f_{DAC} = 12 MSPS, external clock mode, non-interleave mode

図 6-464. TX NSD vs Digital Amplitude and Channel at 3.75 GHz



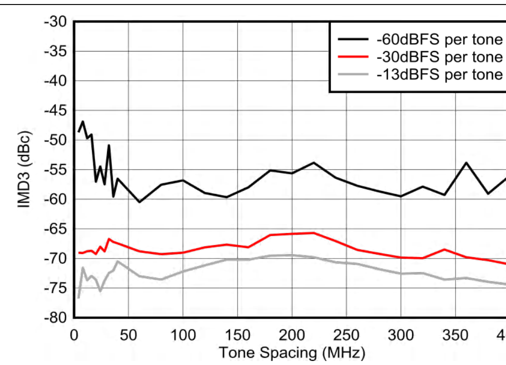
20-MHz tone spacing, 3.5 GHz Matching, –13 dBFS each tone, included PCB and cable losses

図 6-465. TX IMD3 vs DSA Setting at 3.5 GHz



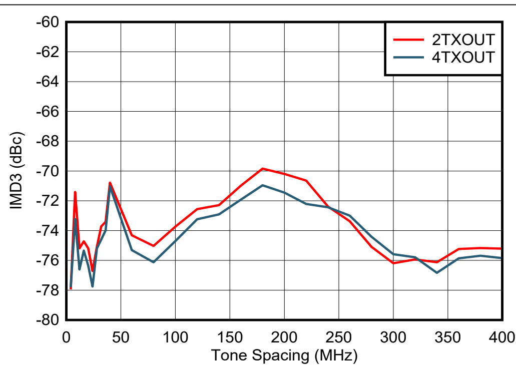
20-MHz tone spacing, 3.5 GHz Matching

図 6-466. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



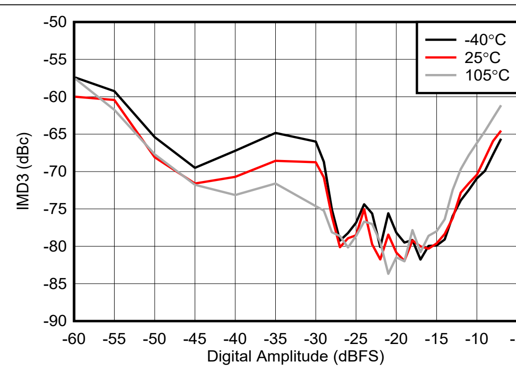
50-MHz tone spacing, external clock mode, non-interleave mode

図 6-467. TX IMD3 vs Tone Spacing and Amplitude at 3.75 GHz



50-MHz tone spacing, external clock mode, non-interleave mode

図 6-468. TX IMD3 vs Tone Spacing and Channel at 3.75 GHz

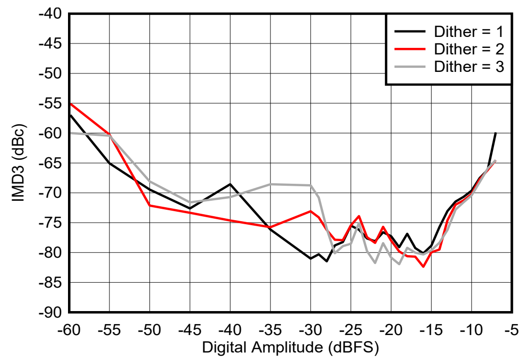


50-MHz tone spacing, external clock mode, non-interleave mode

図 6-469. TX IMD3 vs Digital Amplitude and Temperature at 3.75 GHz

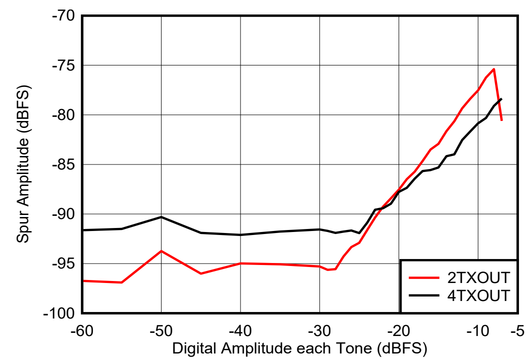
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



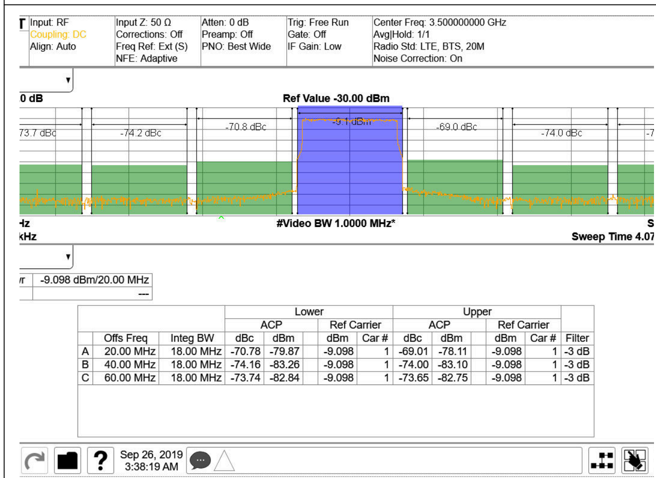
50-MHz tone spacing, external clock mode, non-interleave mode

図 6-470. TX IMD3 vs Digital Amplitude and Dither at 3.75 GHz



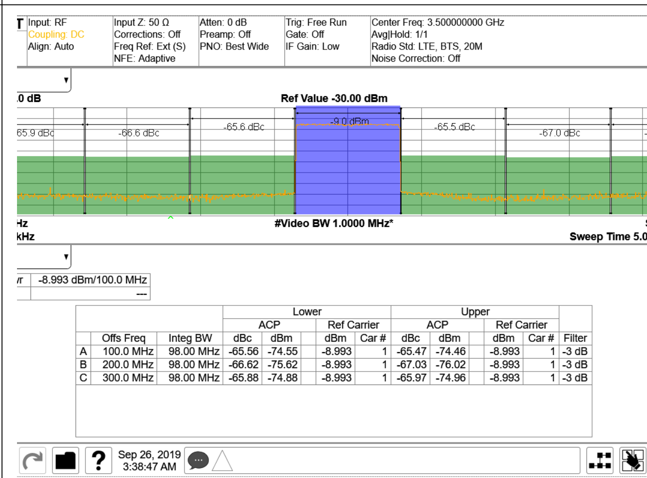
Inband = 3.75 GHz ± 600 MHz, f_{DAC} = 9 GSPS, external clock mode, non-interleave mode.

図 6-471. Two Tone Inband SFDR vs Digital Amplitude at 3.75 GHz



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 6-472. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)

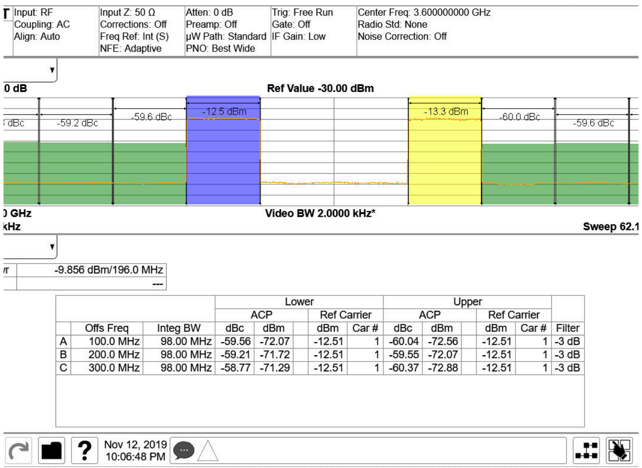


3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-473. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)

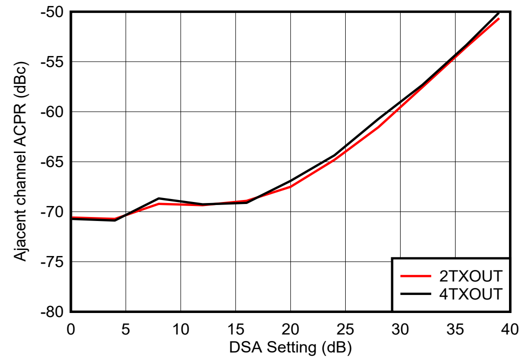
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



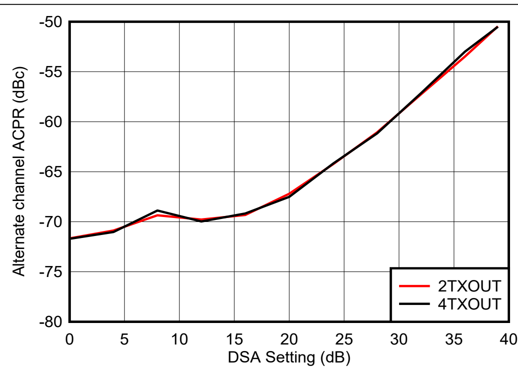
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-474. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz



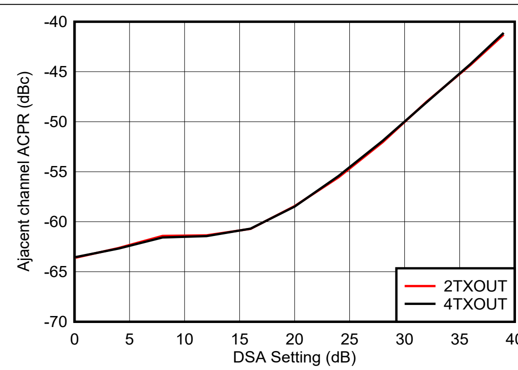
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 6-475. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz



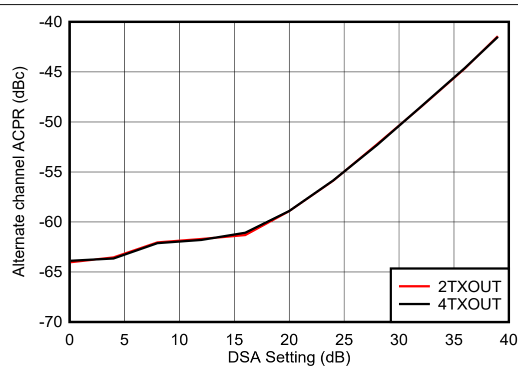
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 6-476. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



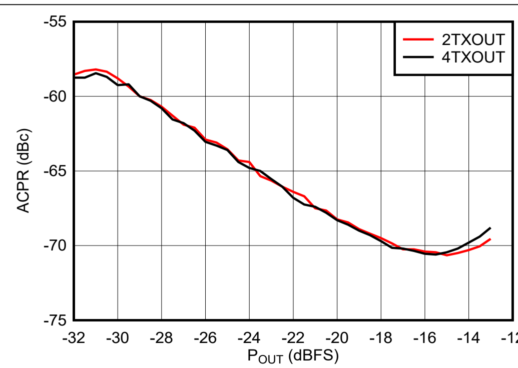
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-477. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-478. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz

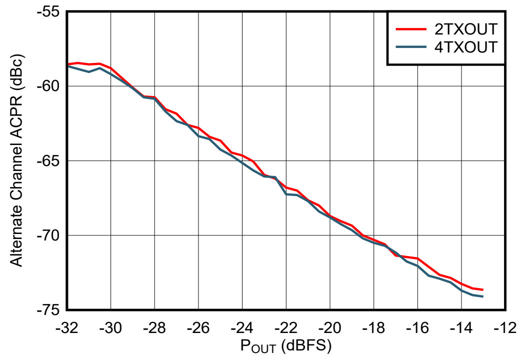


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 6-479. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz

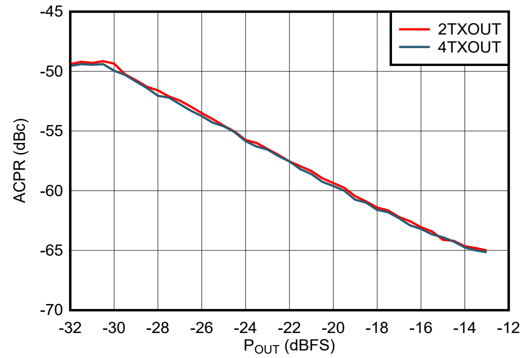
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



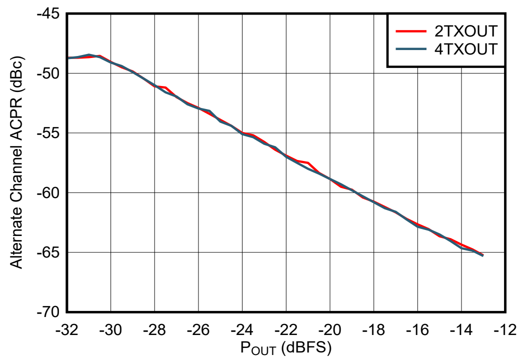
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 6-480. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



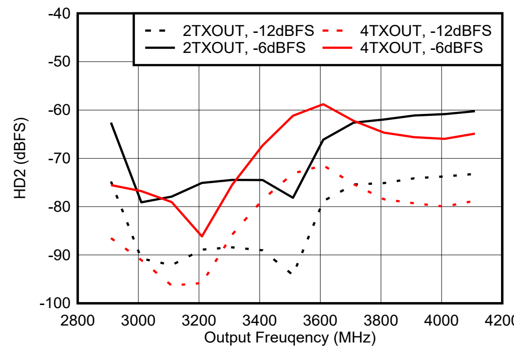
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-481. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz



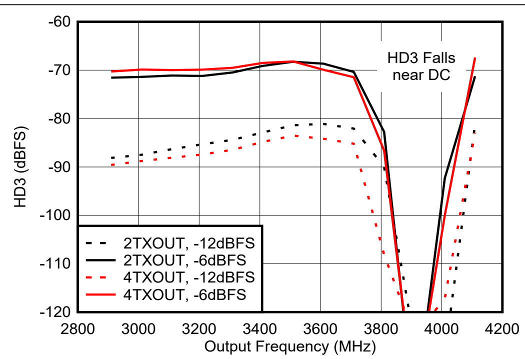
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 6-482. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz



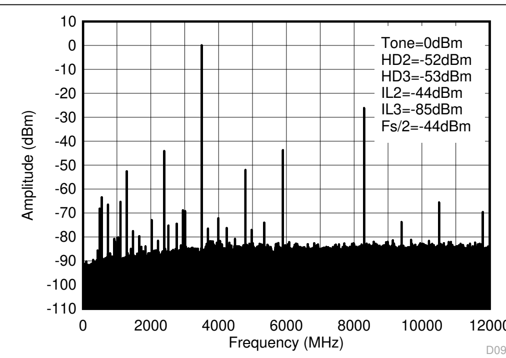
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-483. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

図 6-484. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz

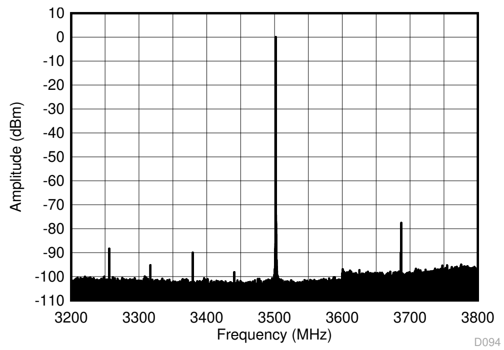


Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-485. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

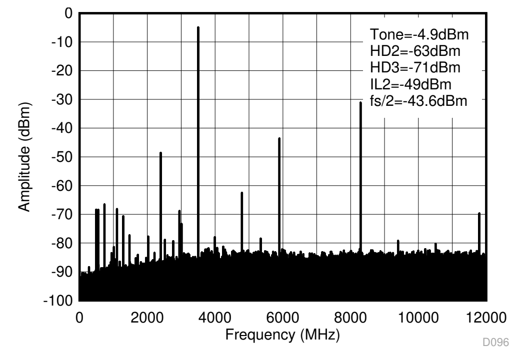
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



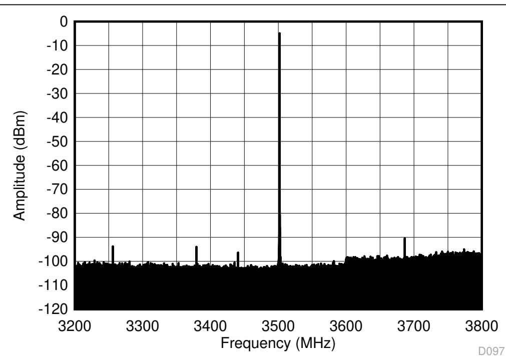
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-486. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



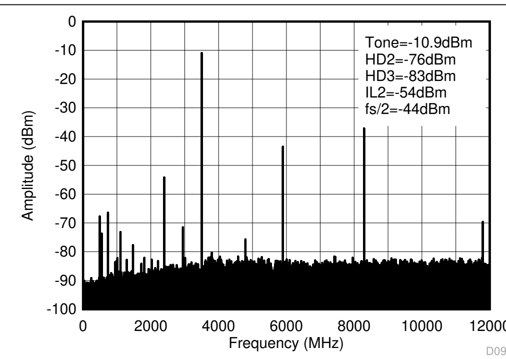
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-487. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



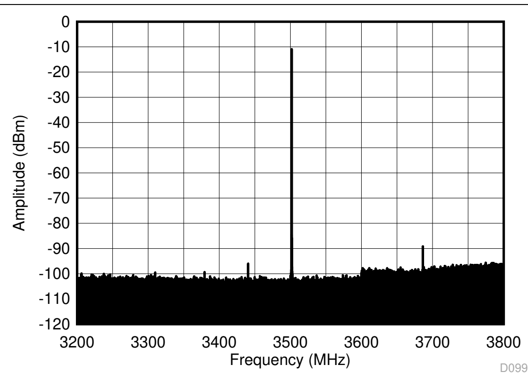
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-488. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



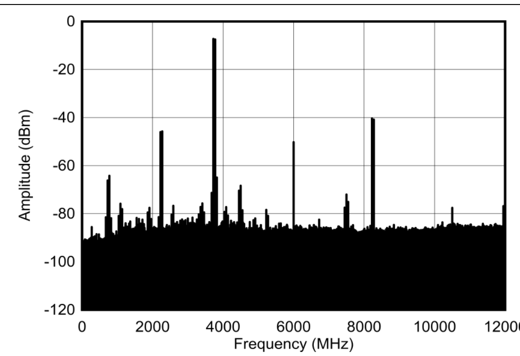
Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-489. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



Matching at 3.5 GHz, f_{DAC} = 11.79648 GSPS, interleave mode.

図 6-490. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)

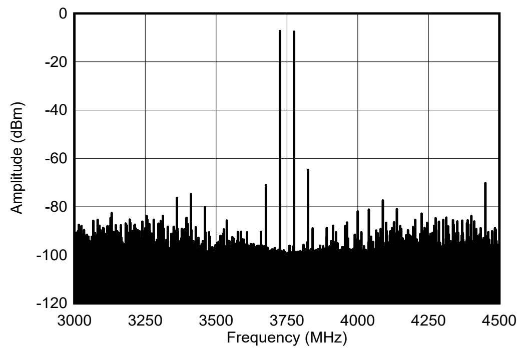


Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 6-491. TX Dual Tone Output Spectrum at 3.75 GHz, -7 dBFS each (0 - f_{DAC})

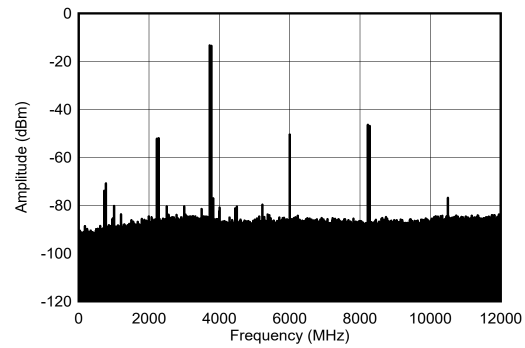
6.12.12 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



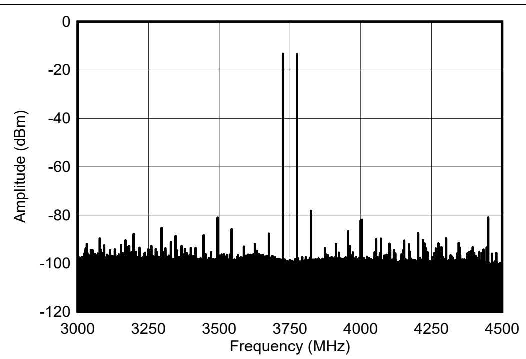
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

図 6-492. TX Dual Tone Output Spectrum at 3.75 GHz, -7 dBFS each (±600 MHz)



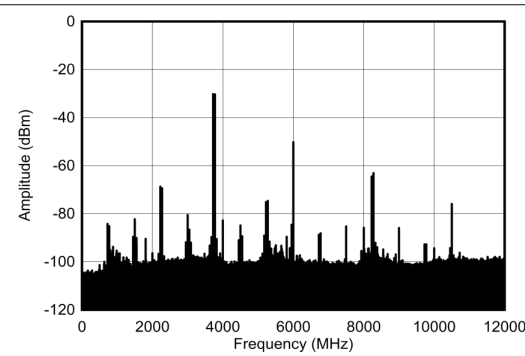
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

図 6-493. TX Dual Tone Output Spectrum at 3.75 GHz, -13 dBFS each (0 - f_{DAC})



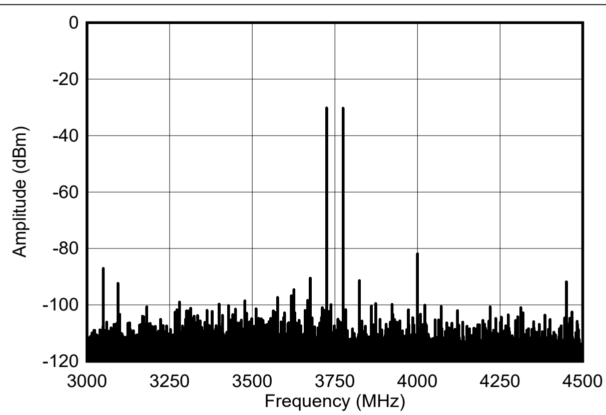
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

図 6-494. TX Dual Tone Output Spectrum at 3.75 GHz, -13 dBFS each (±600 MHz)



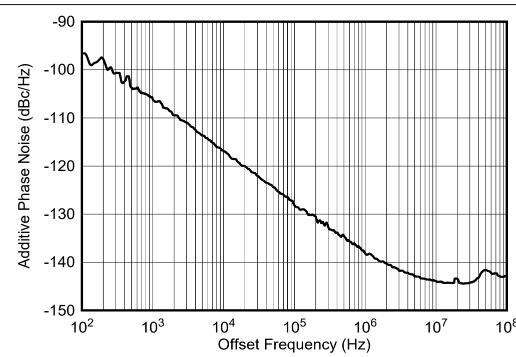
Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

図 6-495. TX Dual Tone Output Spectrum at 3.75 GHz, -30 dBFS each (0 - f_{DAC})



Matching at 3.5 GHz, 50 MHz tone spacing, f_{DAC} = 12 GSPS, non-interleave mode.

図 6-496. TX Dual Tone Output Spectrum at 3.75 GHz, -30 dBFS each (±600 MHz)

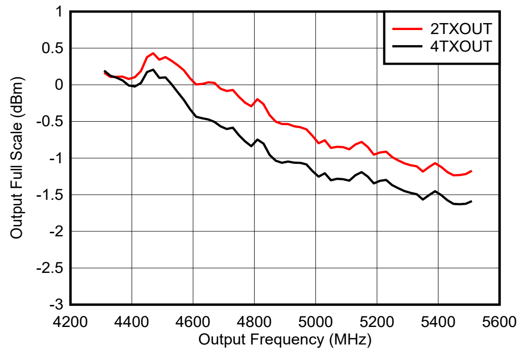


f_{DAC} = f_{CLK} = 12 GSPS, non-interleave mode.

図 6-497. External Clock Additive Phase Noise at 3.7 GHz

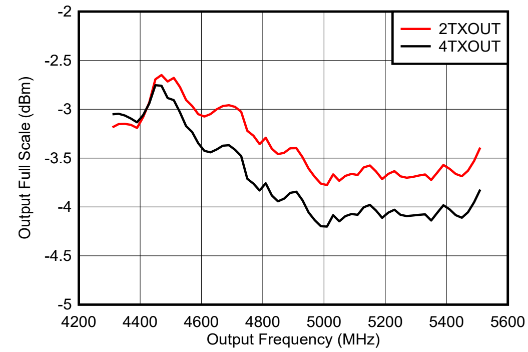
6.12.13 TX Typical Characteristics at 4.9 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



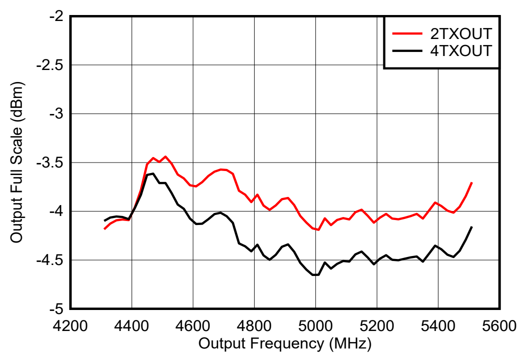
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

図 6-498. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS



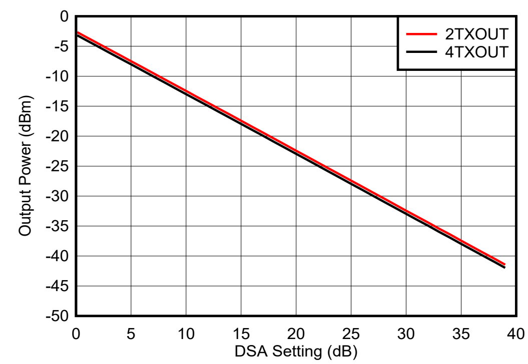
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

図 6-499. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Mixed Mode, 2nd Nyquist Zone



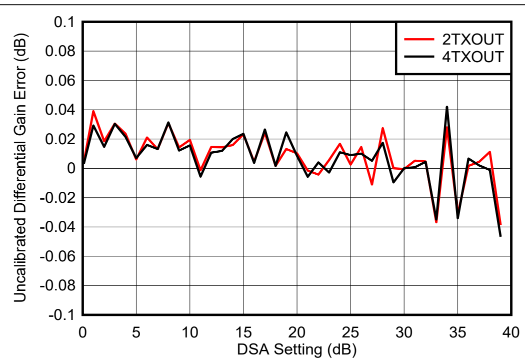
Excluding PCB and cable losses, A_{out} = -0.5 dBFS, DSA = 0, 4.9 GHz matching

図 6-500. TX Full Scale vs RF Frequency and Channel at 8847.36 MSPS, Mixed Mode, 2nd Nyquist Zone



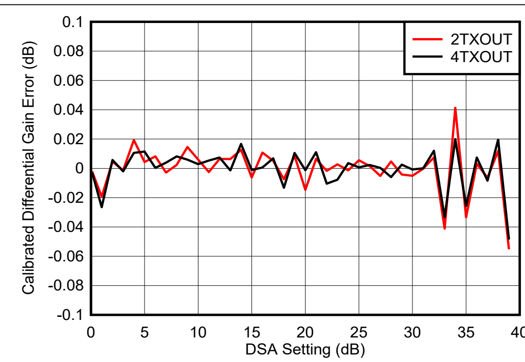
f_{DAC} = 11796.48 MSPS, A_{out} = -0.5 dBFS, matching 4.9 GHz

図 6-501. TX Output Power vs DSA Setting and Channel at 4.9 GHz



f_{DAC}=11796.48 MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-502. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

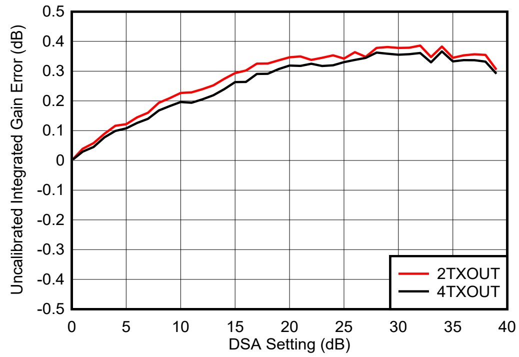


f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-503. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

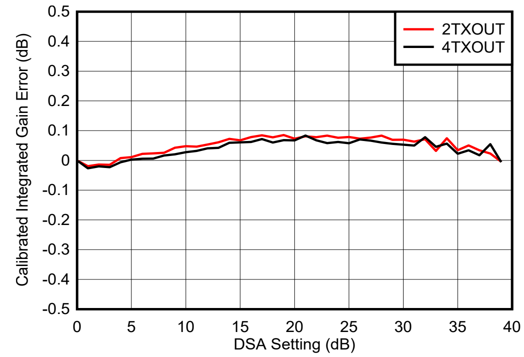
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



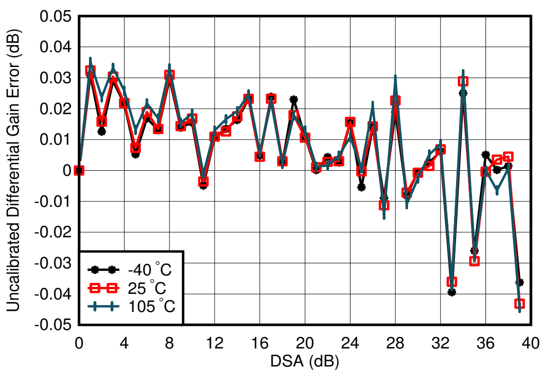
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-504. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



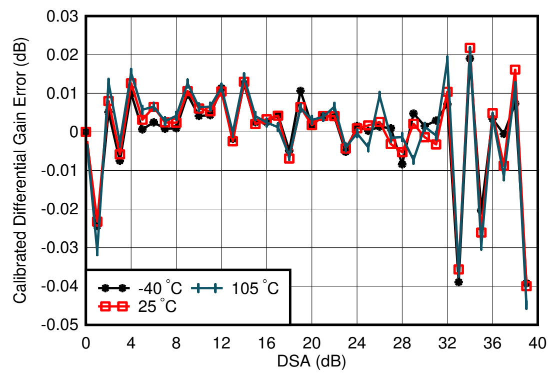
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-505. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-506. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

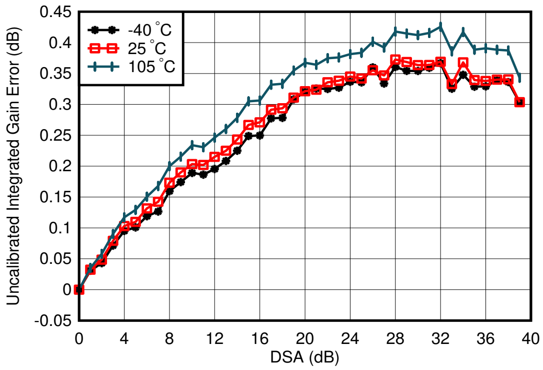


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 6-507. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

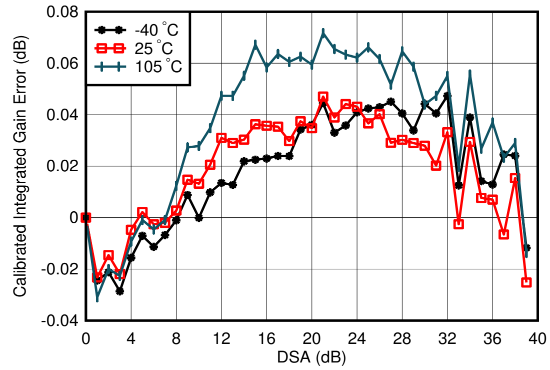
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



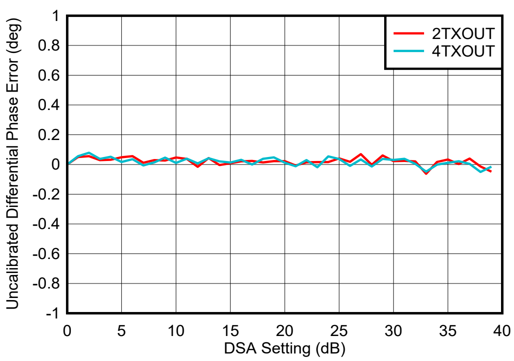
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-508. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



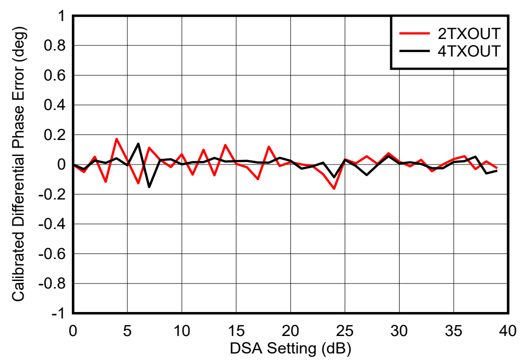
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 6-509. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-510. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

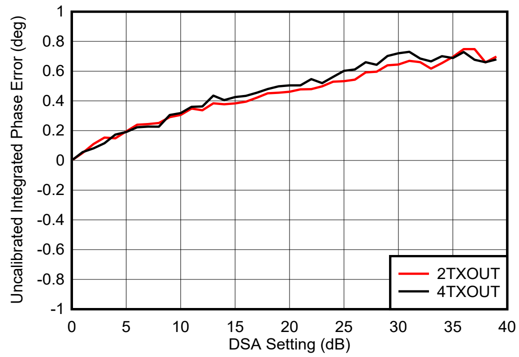


f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 6-511. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

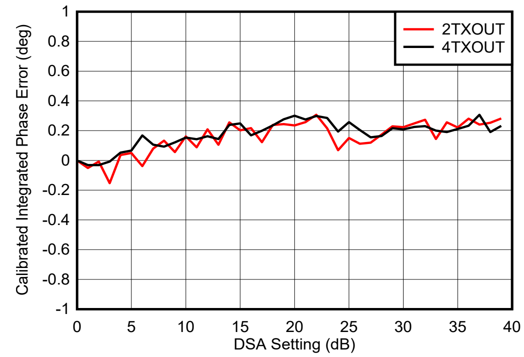
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

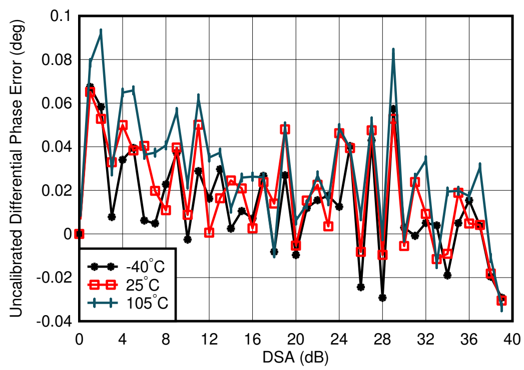
図 6-512. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

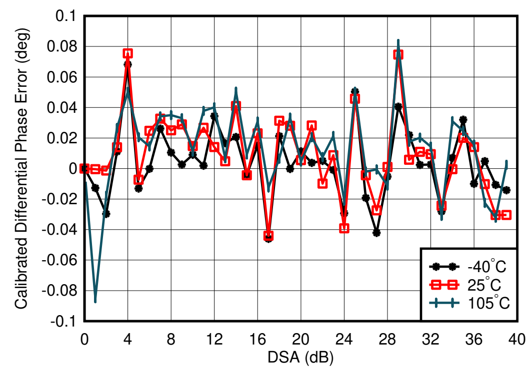
図 6-513. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-514. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



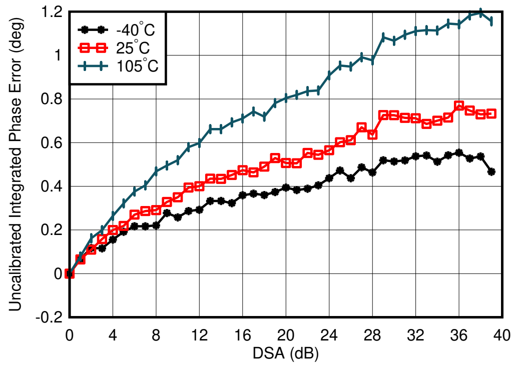
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 6-515. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

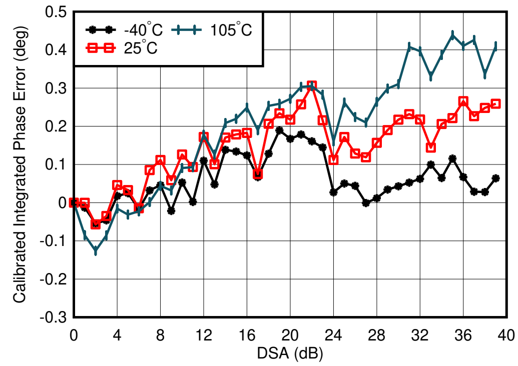
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



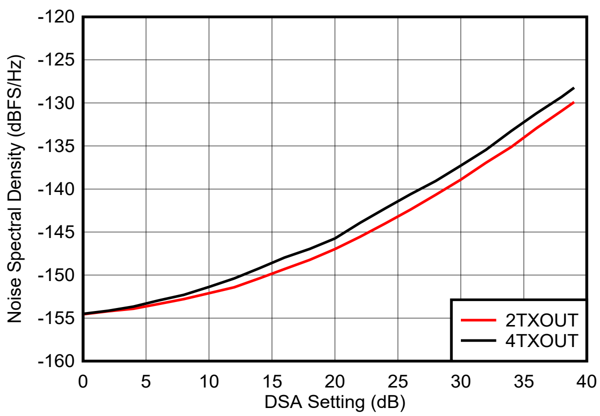
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-516. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



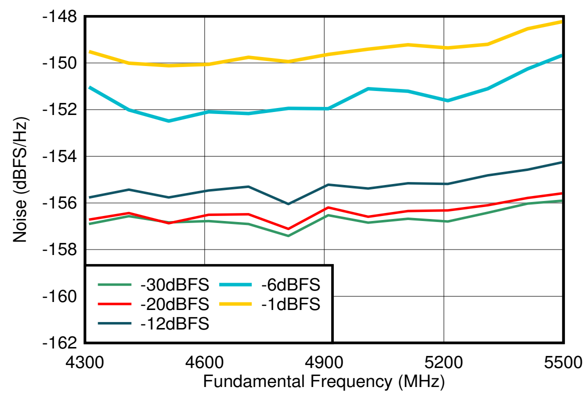
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-517. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, P_{OUT} = –13 dBFS

図 6-518. TX Output Noise vs DSA Setting and Channel at 4.9 GHz

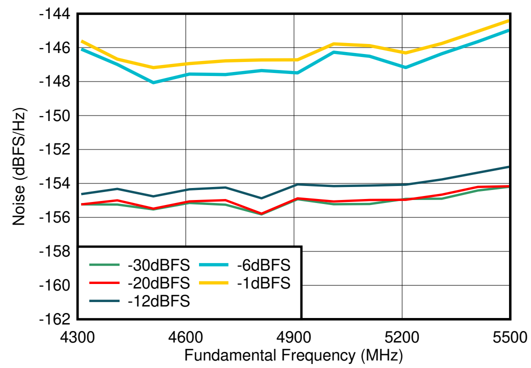


f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz, A_{out} = –13 dBFS.

図 6-519. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA = 0 dB)

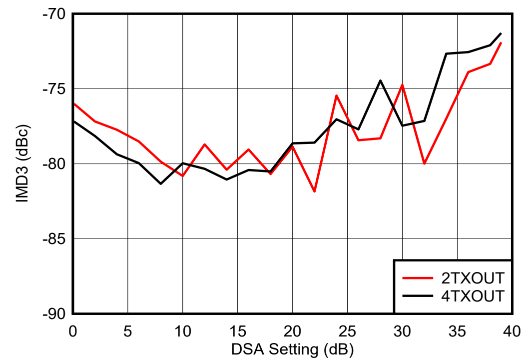
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



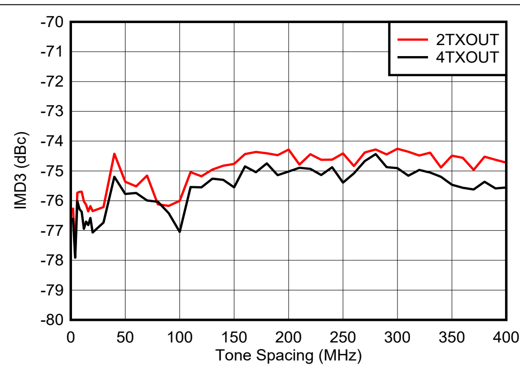
f_{DAC} = 11796.48 MSPS, interleave mode, matching at 4.9 GHz, A_{out} = –13 dBFS.

図 6-520. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA = 6 dB)



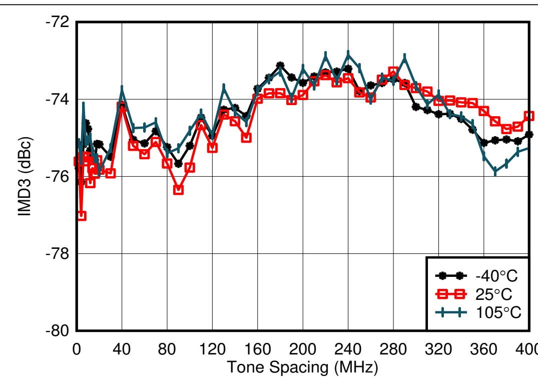
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, -13 dBFS each tone

図 6-521. TX IMD3 vs DSA Setting at 4.9 GHz



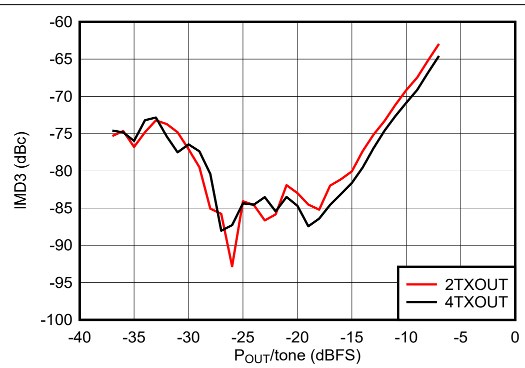
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone

図 6-522. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



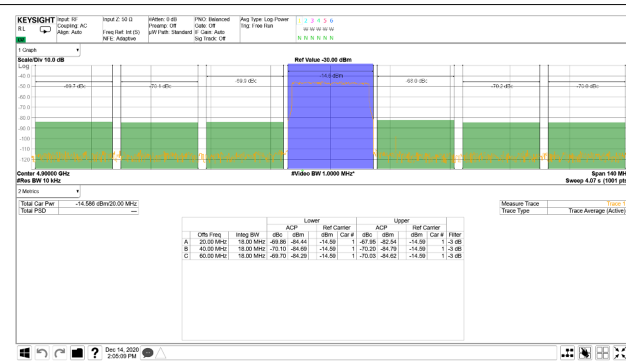
f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone, worst channel

図 6-523. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz



f_{DAC} = 11796.48 MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, $f_{SPACING}$ = 20 MHz

図 6-524. TX IMD3 vs Digital Level at 4.9 GHz

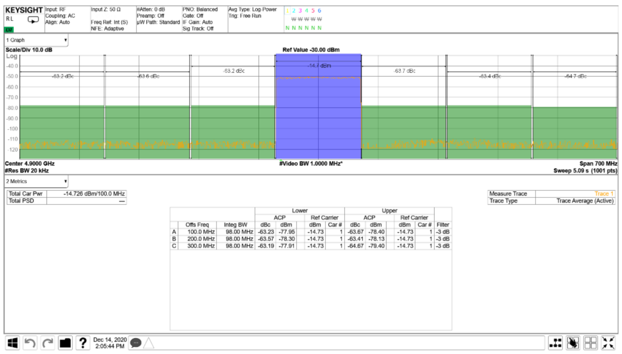


TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-525. TX 20-MHz LTE Output Spectrum at 4.9 GHz

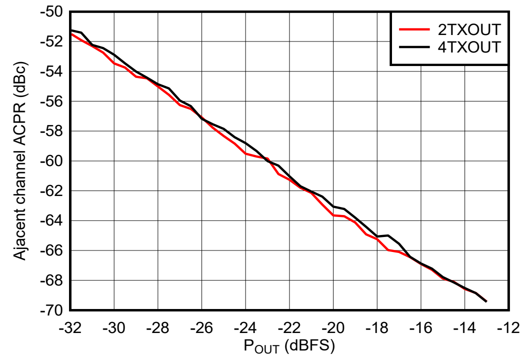
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



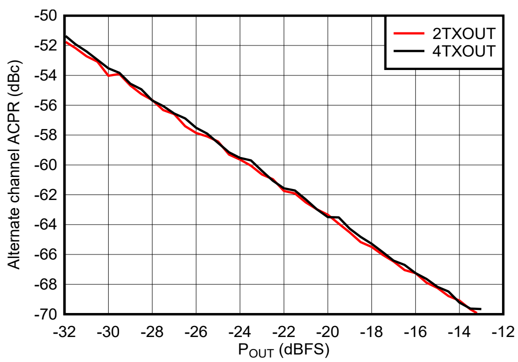
TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-526. TX 100-MHz NR Output Spectrum at 4.9 GHz



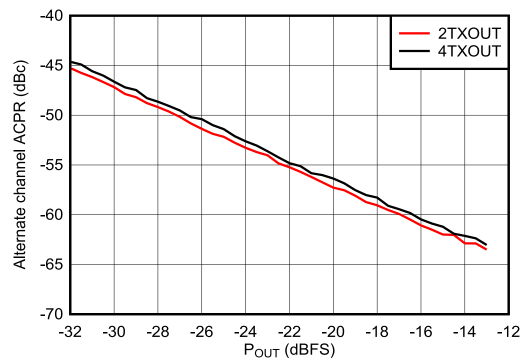
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-527. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



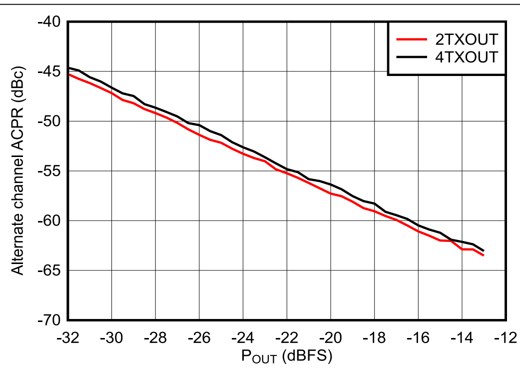
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-528. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



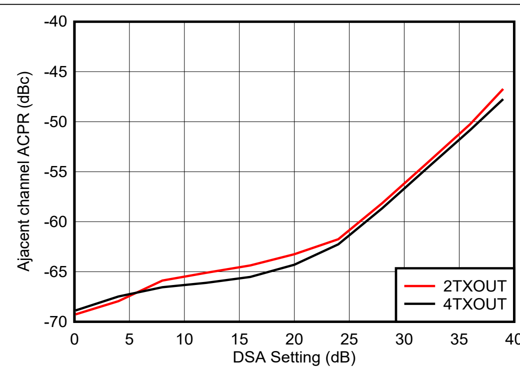
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-529. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-530. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

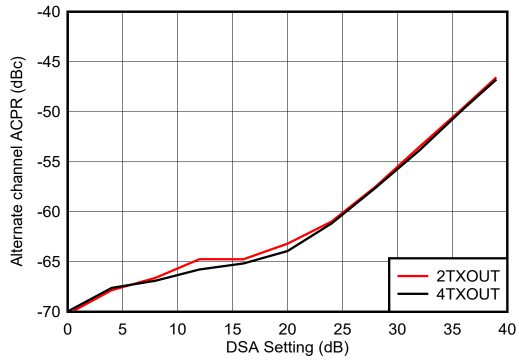


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-531. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

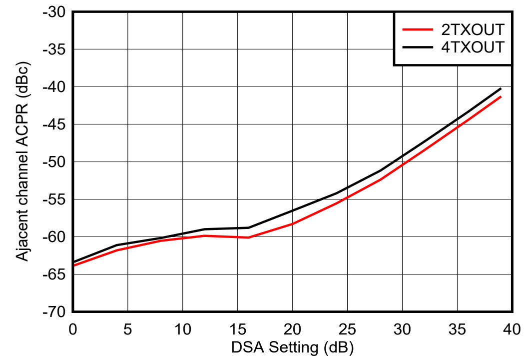
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



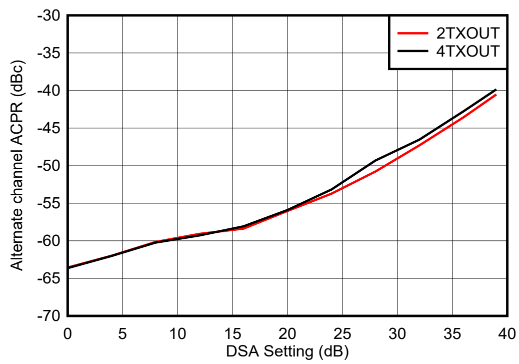
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 6-532. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz



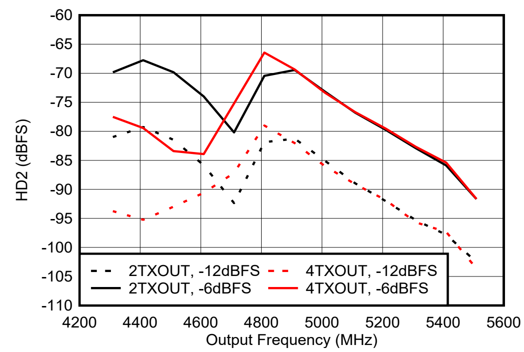
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-533. TX 100-MHz NR ACPR vs DSA at 4.9 GHz



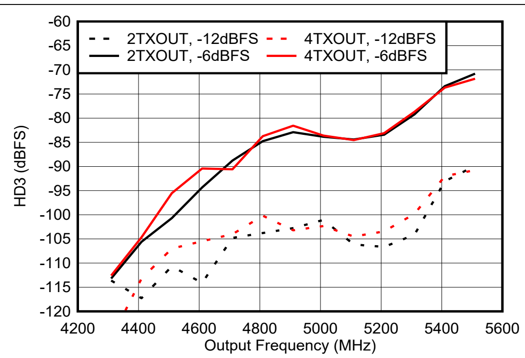
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 6-534. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz



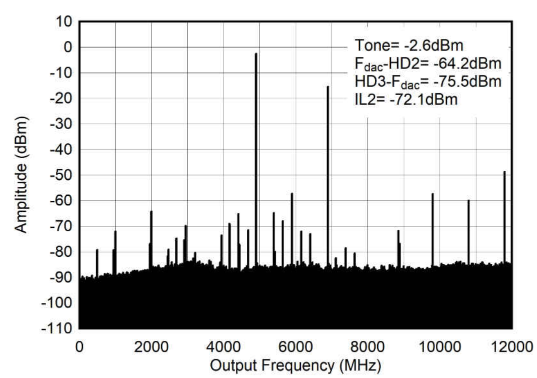
Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-535. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



Matching at 4.9 GHz, f_{DAC} = 11.79648 GSPS, interleave mode, normalized to output power at harmonic frequency

図 6-536. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

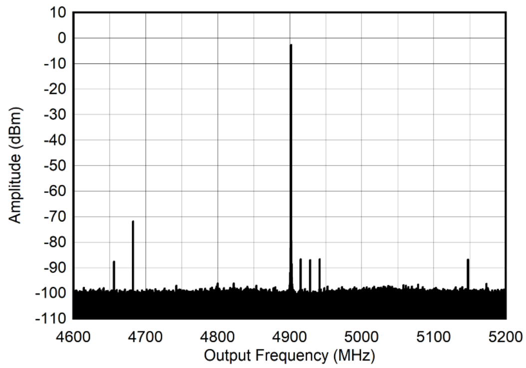


f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-537. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

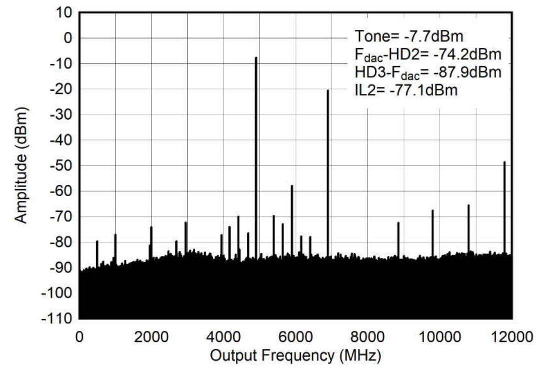
6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



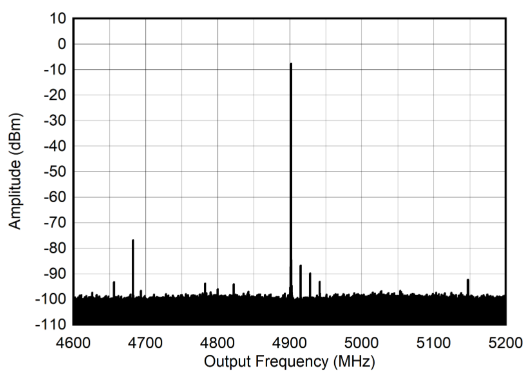
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 6-538. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



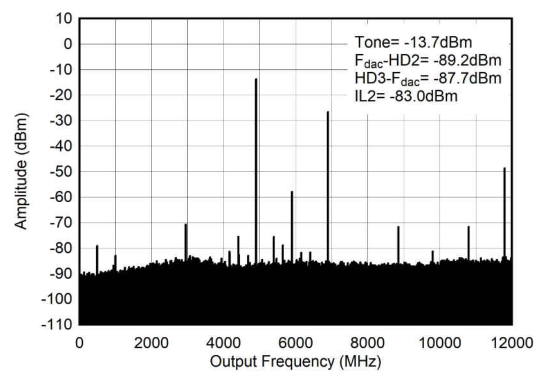
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-539. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



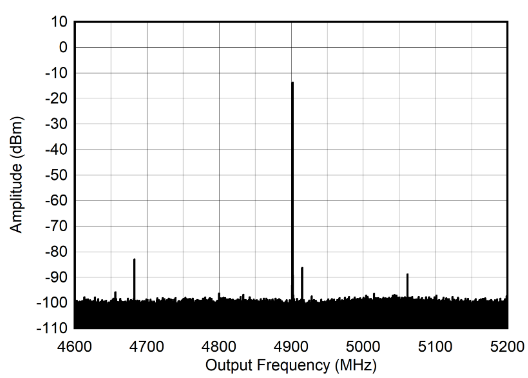
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 6-540. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = f_S/n ± f_{OUT}.

図 6-541. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})

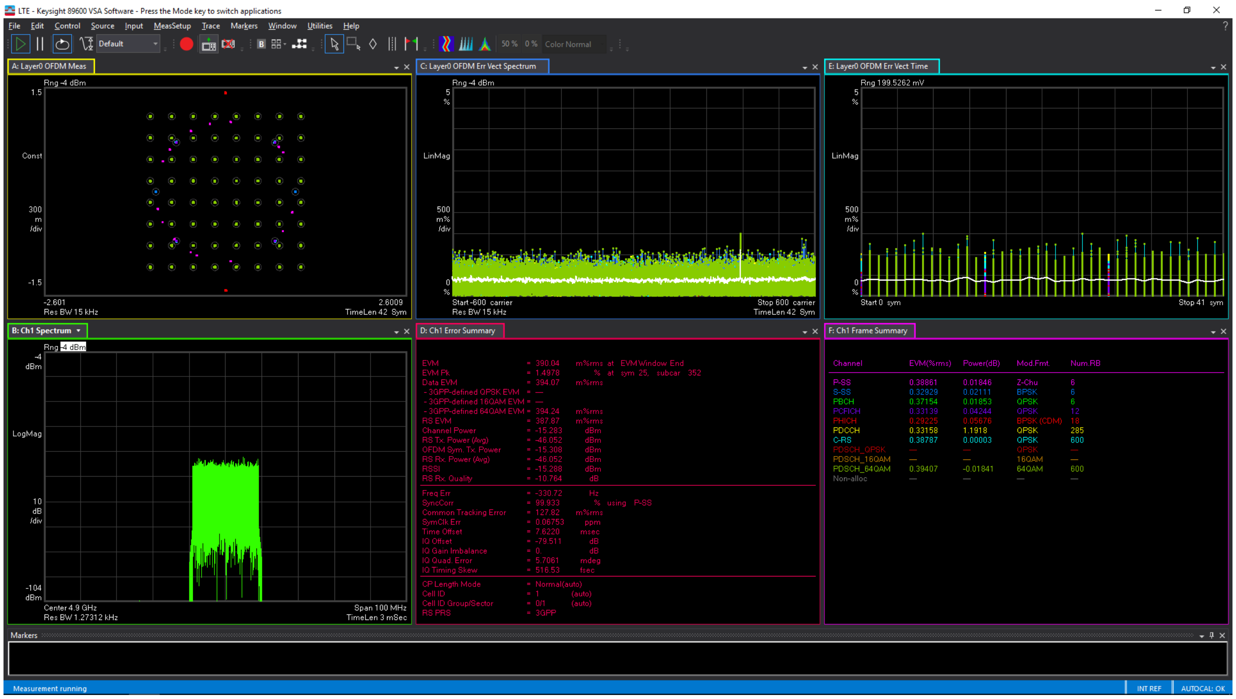


f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 6-542. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)

6.12.13 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52 MSPS, f_{DAC} = 11796.48 MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52 MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

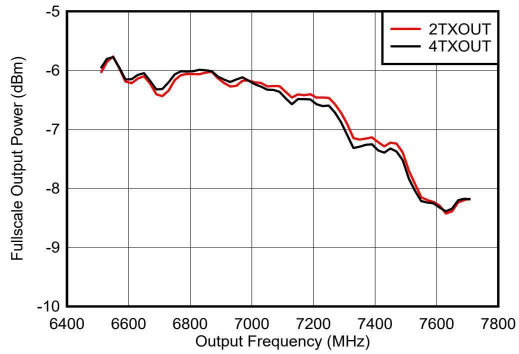


TM1.1, P_{OUT_RMS} = –13 dBFS

図 6-543. TX 20-MHz LTE Error Vector Magnitude at 4.9 GHz

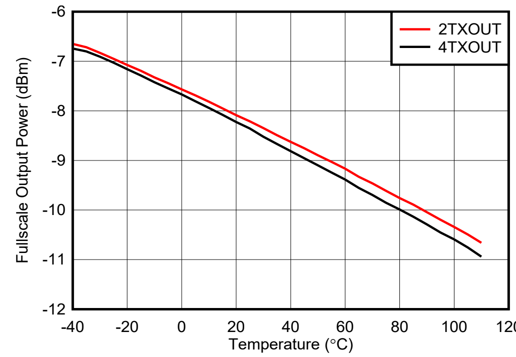
6.12.14 TX Typical Characteristics at 7.1 GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2^{nd} Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



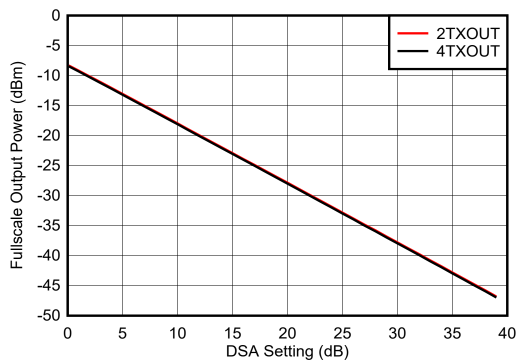
Excluding PCB and cable losses

図 6-544. TX Full Scale vs RF Frequency and Channel



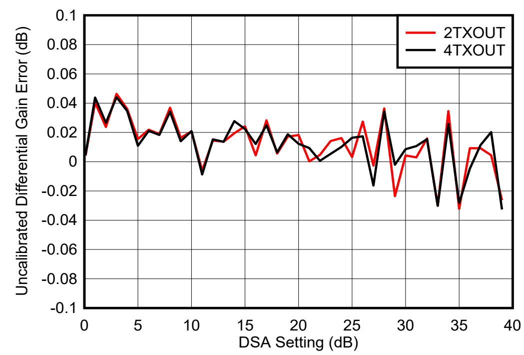
Excluding PCB and cable losses

図 6-545. TX Full Scale vs Temperature and Channel at 7.1 GHz



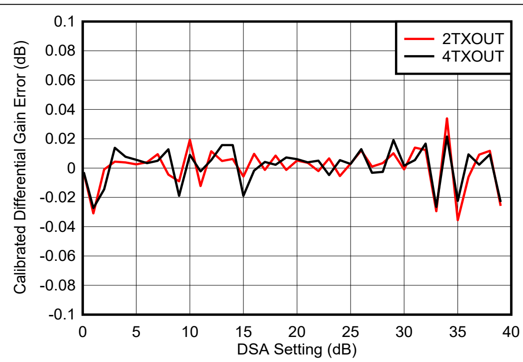
Excluding PCB and cable losses

図 6-546. TX Full Scale vs DSA Setting and Channel at 7.1 GHz



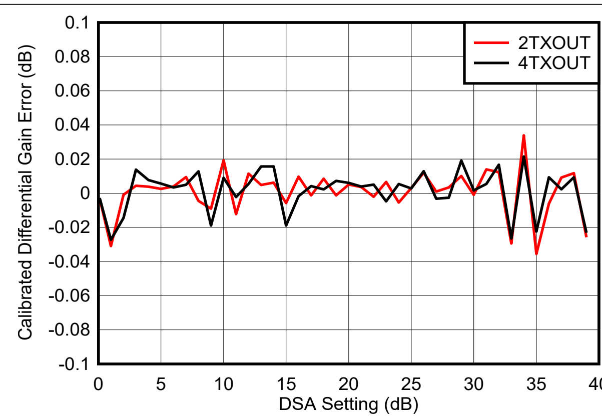
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 6-547. Uncalibrated Differential Gain Error vs Channel at 7.1 GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 6-548. Uncalibrated Differential Gain Error vs Temperature at 7.1 GHz

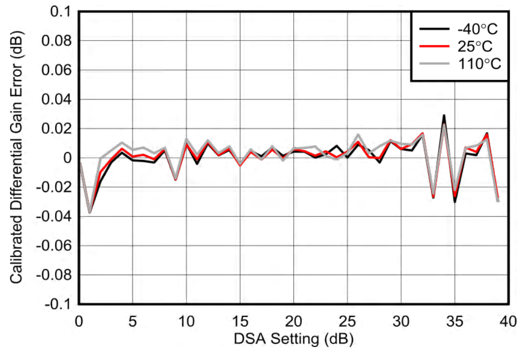


Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 6-549. Calibrated Differential Gain Error vs Channel at 7.1 GHz

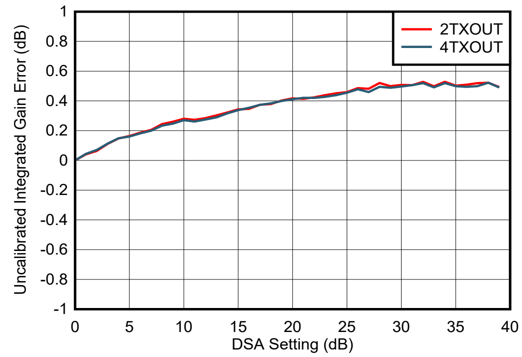
6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



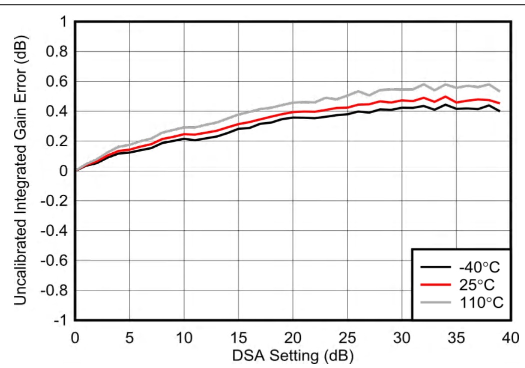
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 6-550. Calibrated Differential Gain Error vs Temperature at 7.1 GHz



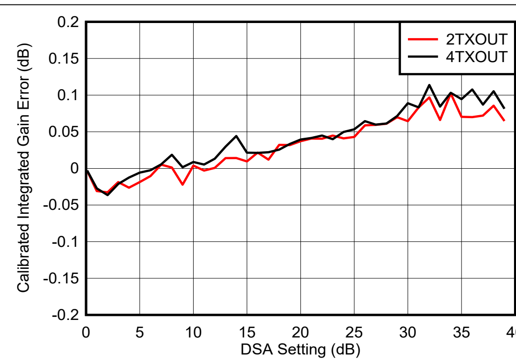
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 6-551. Uncalibrated Integrated Gain Error vs Channel at 7.1 GHz



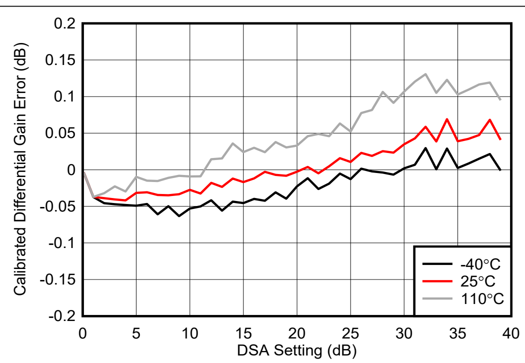
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 6-552. Uncalibrated Integrated Gain Error vs Temperature at 7.1 GHz



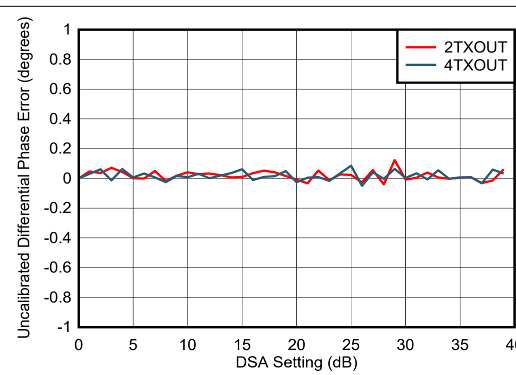
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 6-553. Calibrated Integrated Gain Error vs Channel at 7.1 GHz



Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 6-554. Calibrated Integrated Gain Error vs Temperature at 7.1 GHz

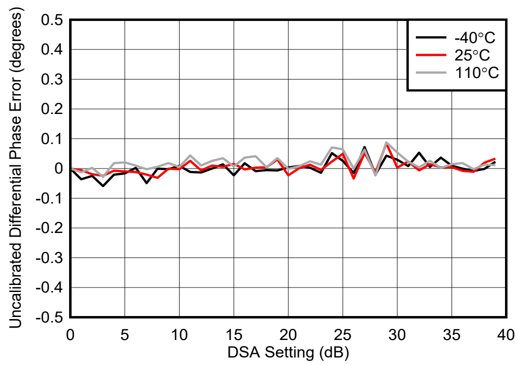


Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 6-555. Uncalibrated Differential Phase Error vs Channel at 7.1 GHz

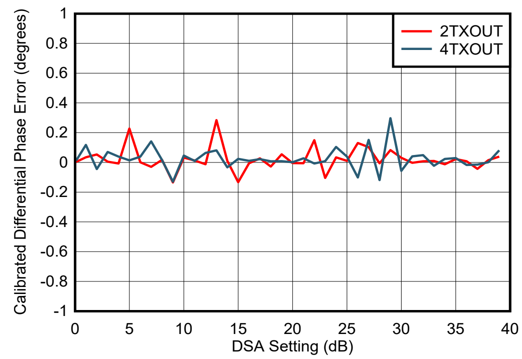
6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



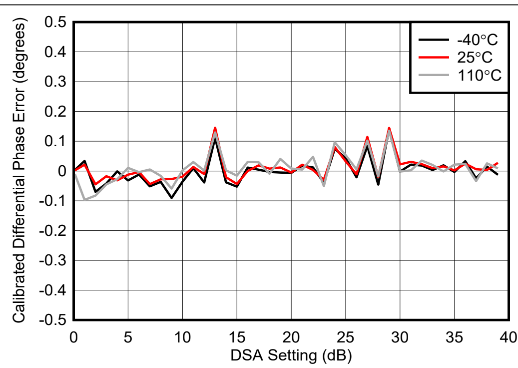
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 6-556. Uncalibrated Differential Phase Error vs Temperature at 7.1 GHz



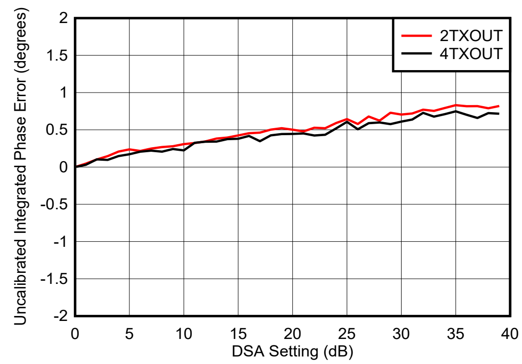
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 6-557. Calibrated Differential Phase Error vs Channel at 7.1 GHz



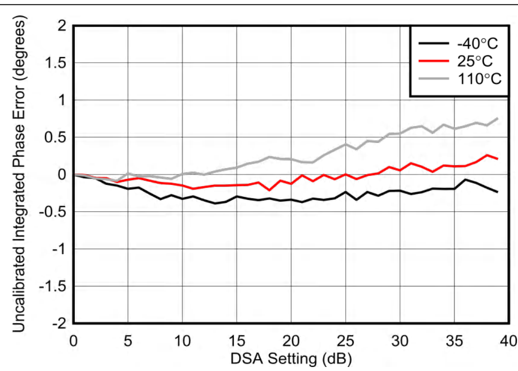
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 6-558. Calibrated Differential Phase Error vs Temperature at 7.1 GHz



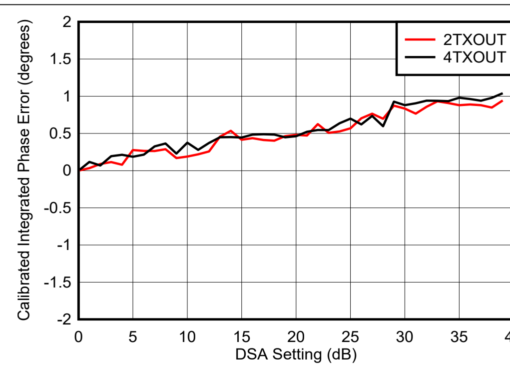
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-559. Uncalibrated Integrated Phase Error vs Channel at 7.1 GHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-560. Uncalibrated Integrated Phase Error vs Temperature at 7.1 GHz

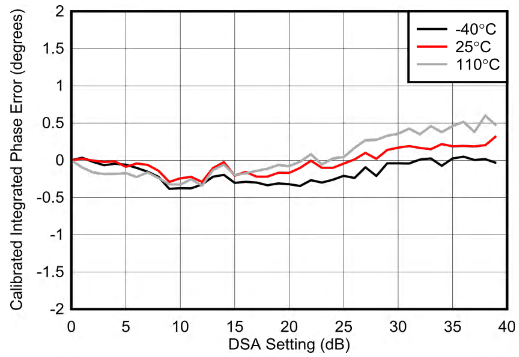


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-561. Calibrated Integrated Phase Error vs Channel at 7.1 GHz

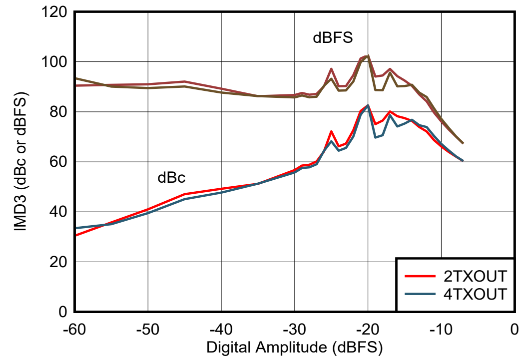
6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



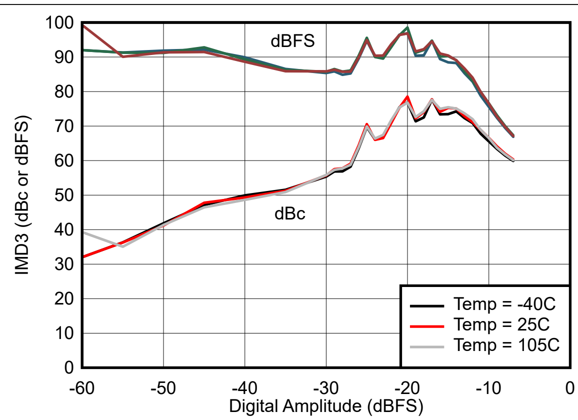
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-562. Calibrated Integrated Phase Error vs Temperature at 7.1 GHz



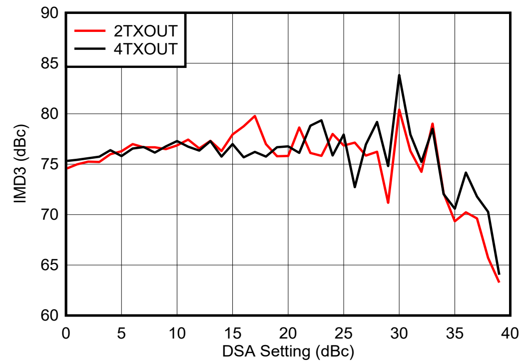
Tone spacing = 50 MHz

図 6-563. IMD3 vs Digital Amplitude and Channel at 7.1 GHz



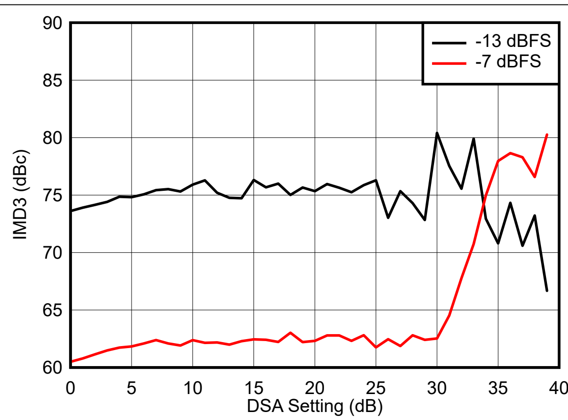
Tone spacing = 50 MHz

図 6-564. IMD3 vs Digital Amplitude and Temperature at 7.1 GHz



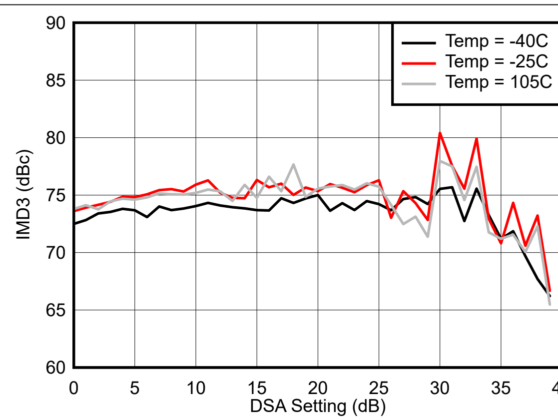
Tone spacing = 50 MHz

図 6-565. IMD3 vs DSA Setting and Channel at 7.1 GHz



Tone spacing = 50 MHz

図 6-566. IMD3 vs DSA Setting and Digital Amplitude at 7.1 GHz



Tone spacing = 50 MHz

図 6-567. IMD3 vs DSA Setting and Temperature at 7.1 GHz

6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.

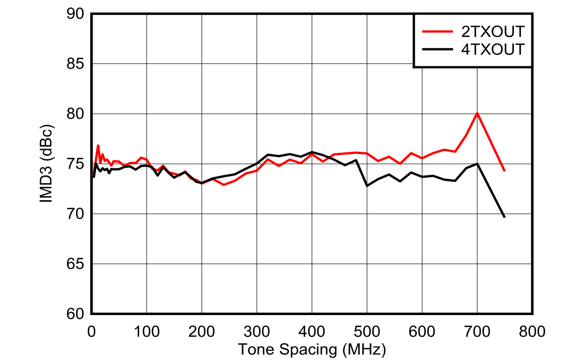


図 6-568. IMD3 vs Tone Spacing and Channel at 7.1 GHz

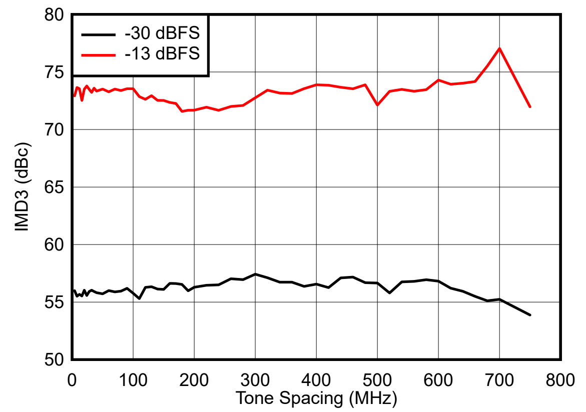


図 6-569. IMD3 vs Tone Spacing and Digital Amplitude at 7.1 GHz

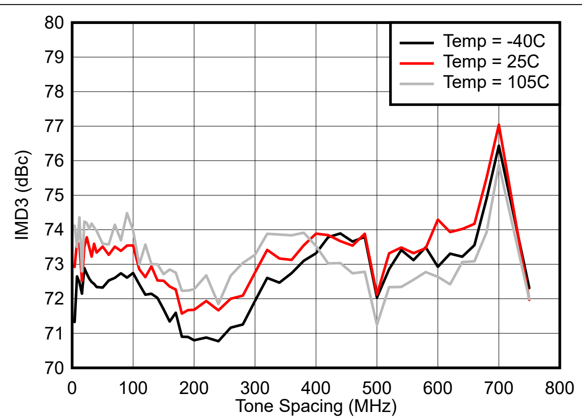
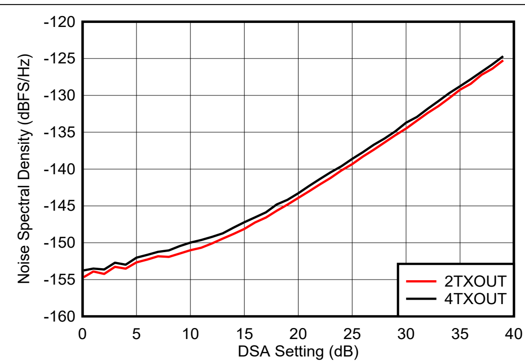
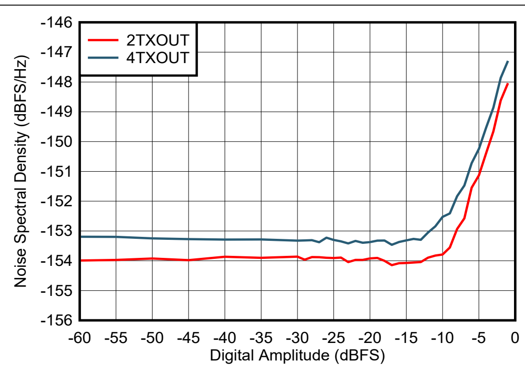


図 6-570. IMD3 vs Tone Spacing and Temperature at 7.1 GHz



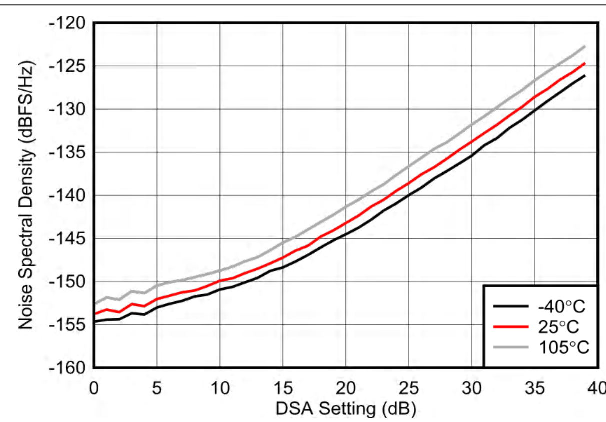
Tone at -12 dBFS, 50 MHz offset from tone

図 6-571. NSD vs DSA Setting and Channel at 7.1 GHz



50 MHz offset from tone

図 6-572. NSD vs DSA Setting and Amplitude at 7.1 GHz

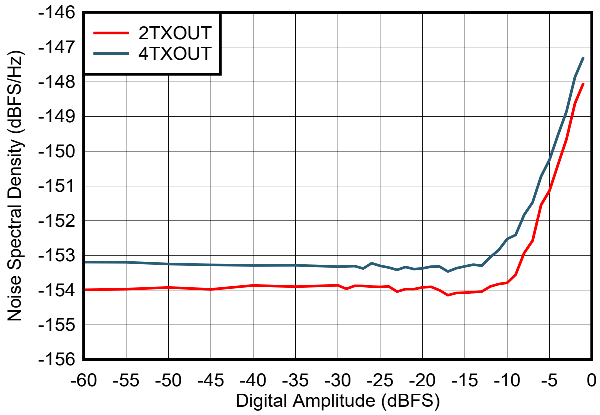


Tone at -12 dBFS, 50 MHz offset from tone

図 6-573. NSD vs DSA Setting and Temperature at 7.1 GHz

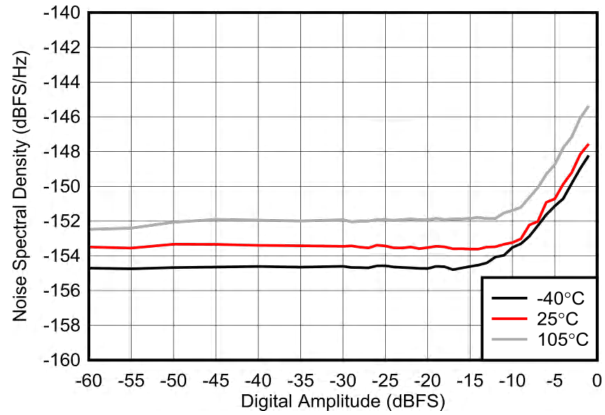
6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



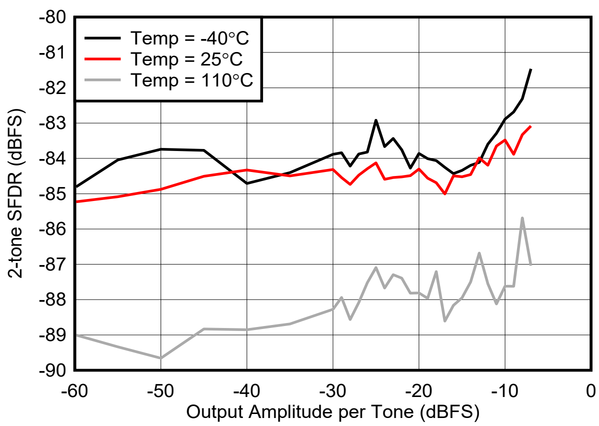
50 MHz offset from tone

図 6-574. NSD vs Digital Amplitude and Channel at 7.1 GHz



50 MHz offset from tone

図 6-575. NSD vs Digital Amplitude and Temperature at 7.1 GHz



50 MHz tone spacing, inband = 7100 MHz ± 200 MHz, excluding IMD3 components separately

図 6-576. Two Tone Inband SFDR vs Output Amplitude at 7.1 GHz

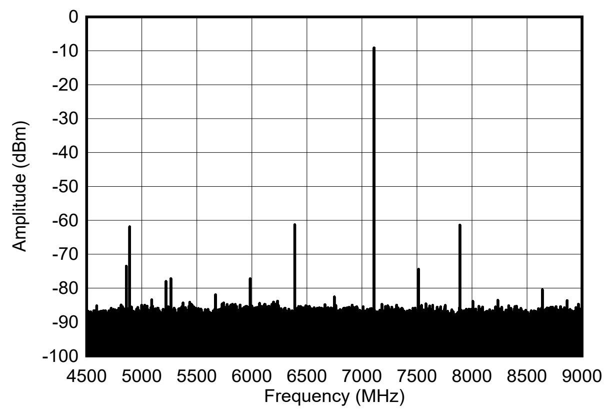


図 6-577. Single Tone Output Spectrum at 7.1 GHz, -1 dBFS (Nyquist)

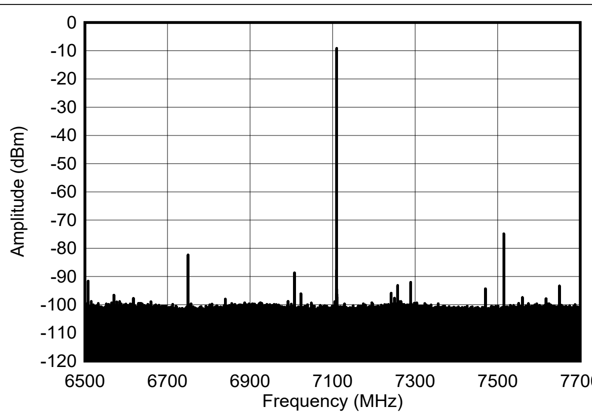


図 6-578. Single Tone Output Spectrum at 7.1 GHz, -1 dBFS (narrow span)

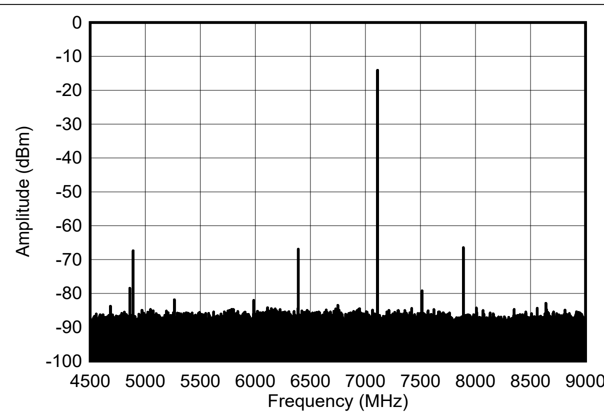


図 6-579. Single Tone Output Spectrum at 7.1 GHz, -6 dBFS (Nyquist)

6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.

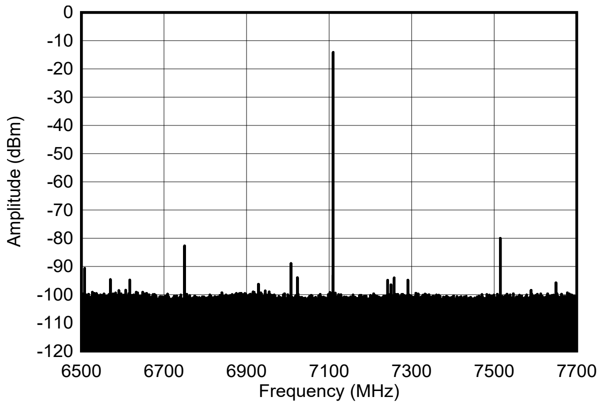


図 6-580. Single Tone Output Spectrum at 7.1 GHz, -6 dBFS (narrow span)

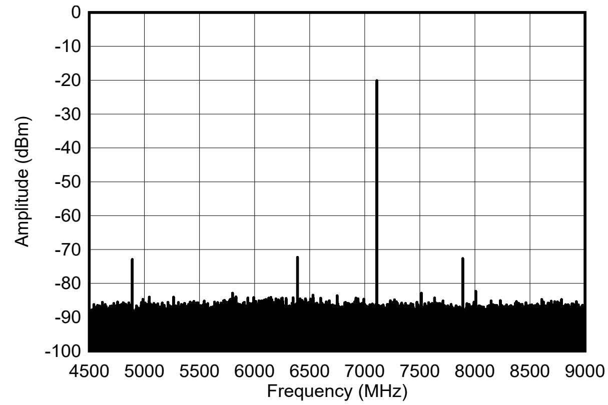


図 6-581. Single Tone Output Spectrum at 7.1 GHz, -12 dBFS (Nyquist)

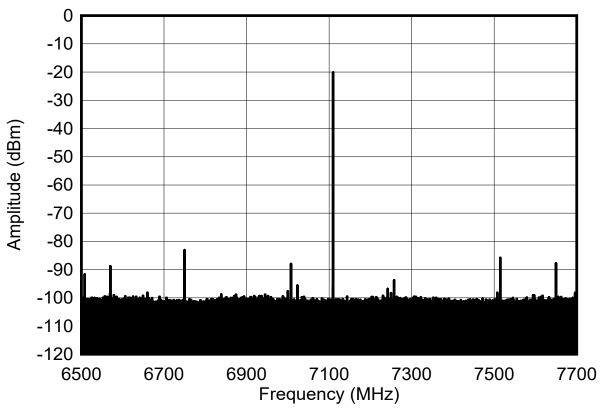
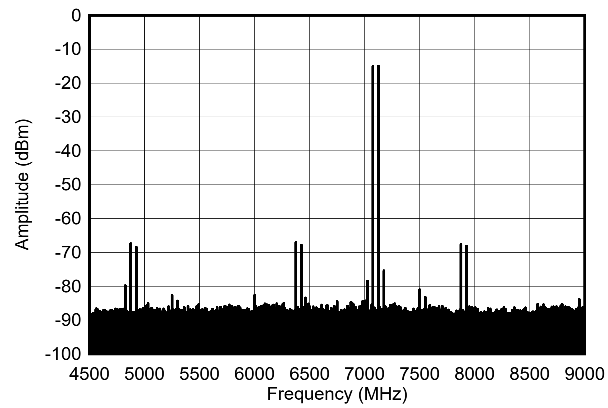
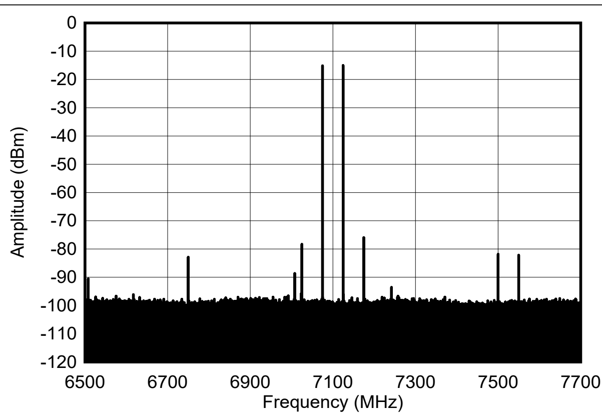


図 6-582. Single Tone Output Spectrum at 7.1 GHz, -12 dBFS (narrow span)



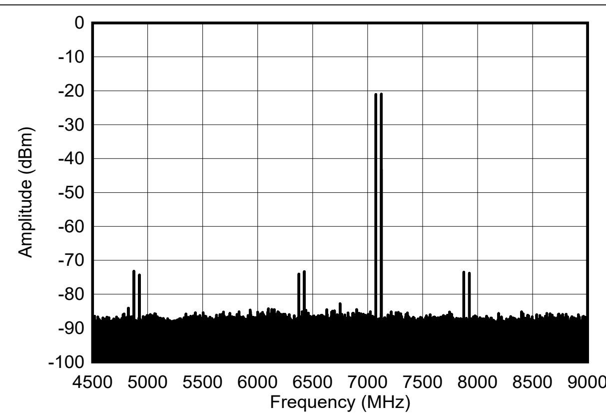
50 MHz Tone Spacing

図 6-583. Two Tone Output Spectrum at 7.1 GHz, -7 dBFS each (Nyquist)



50 MHz Tone Spacing

図 6-584. Two Tone Output Spectrum at 7.1 GHz, -7 dBFS each (narrow band)

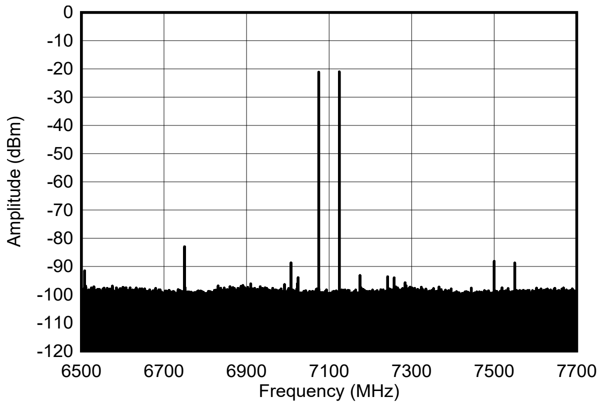


50 MHz Tone Spacing

図 6-585. Two Tone Output Spectrum at 7.1 GHz, -13 dBFS each (Nyquist)

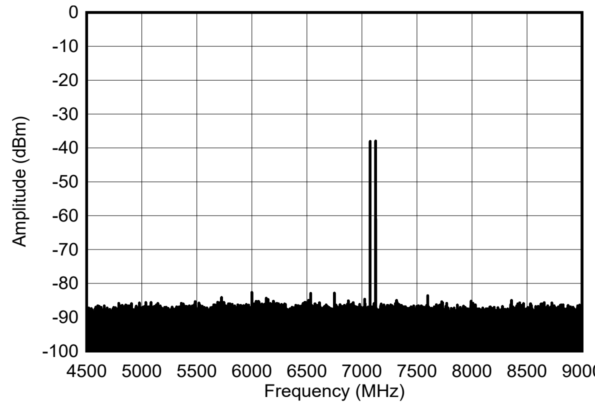
6.12.14 TX Typical Characteristics at 7.1 GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 500 MSPS, f_{DAC} = 9000 MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 18x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 7.1 GHz matching.



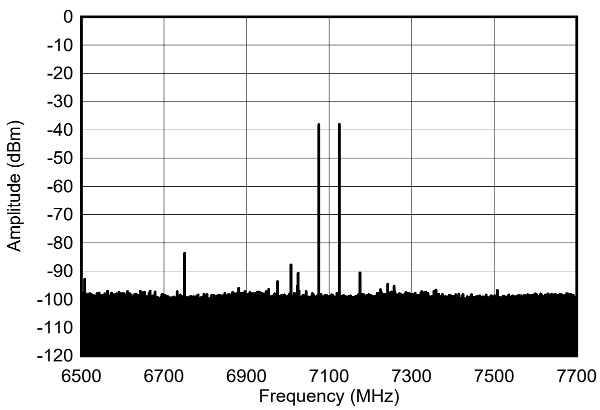
50 MHz Tone Spacing

図 6-586. Two Tone Output Spectrum at 7.1 GHz, -13 dBFS each (narrow span)



50 MHz Tone Spacing

図 6-587. Two Tone Output Spectrum at 7.1G Hz, -30 dBFS each (Nyquist)



50 MHz Tone Spacing

図 6-588. Two Tone Output Spectrum at 7.1 GHz, -30 dBFS each (narrow span)

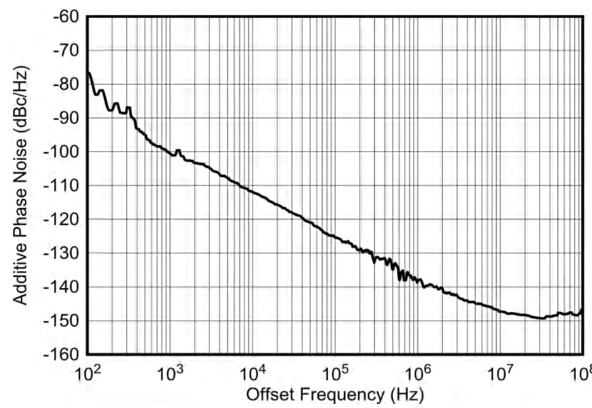
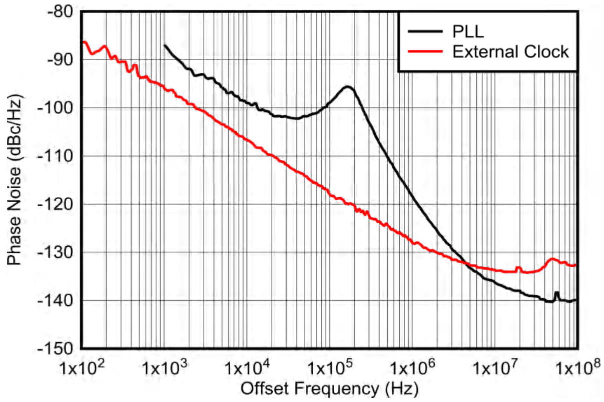


図 6-589. External Clock Additive Phase Noise at 7.1 GHz

6.12.15 PLL and Clock Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



measured at TX output, normalized to 12GHz by 20*log10(12GHz/F_{OUT})

図 6-590. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz

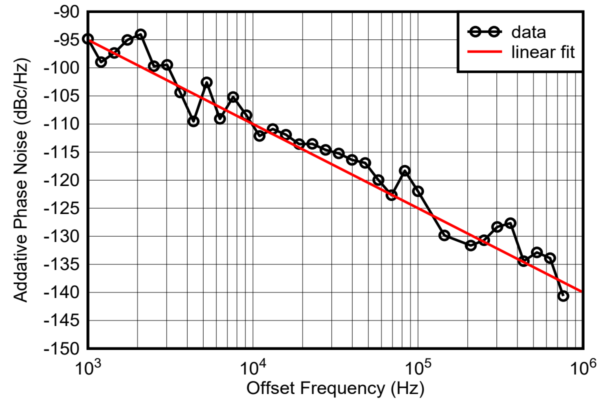
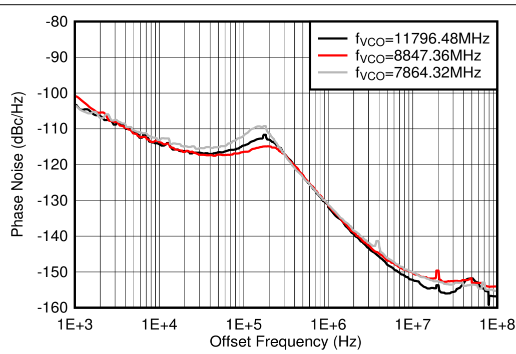
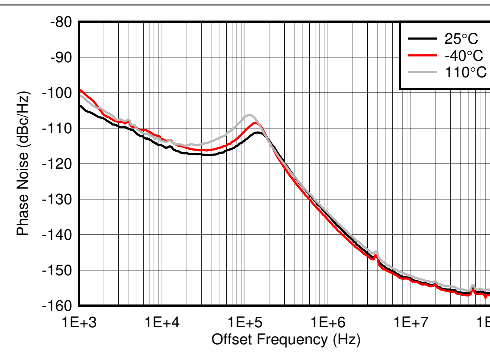


図 6-591. RX Addative Phase Noise at 9.61GHz



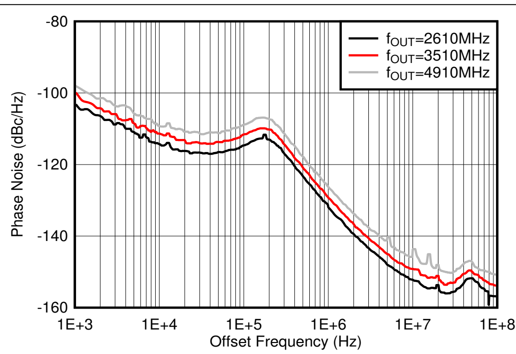
PLL enabled, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-592. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



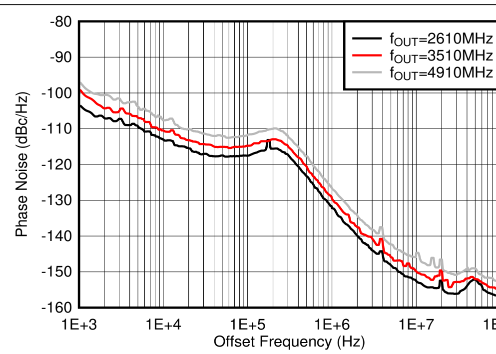
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-593. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



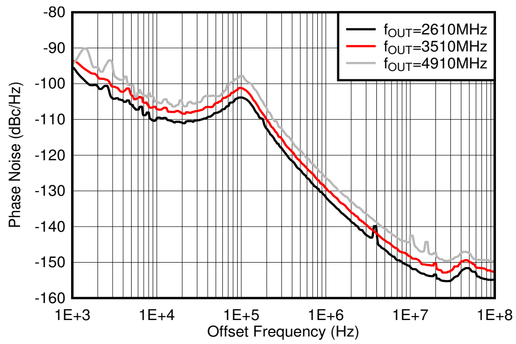
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-594. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



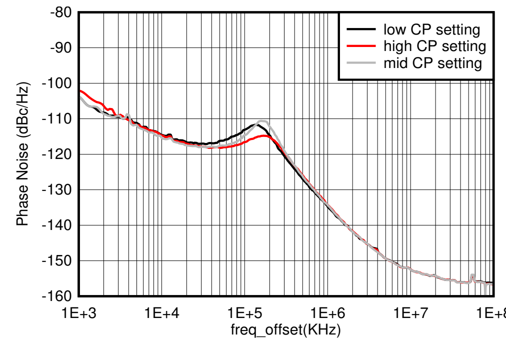
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-595. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



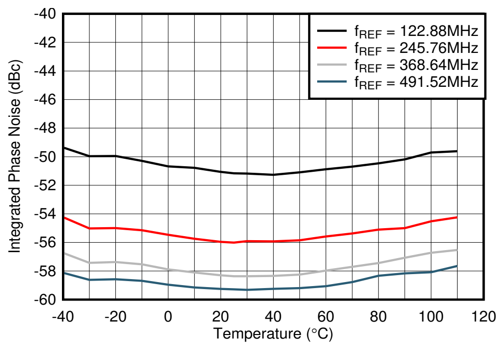
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-596. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



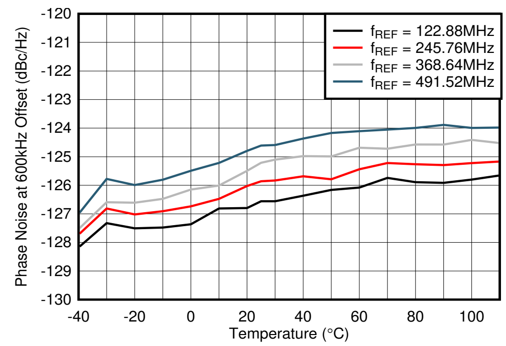
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-597. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz



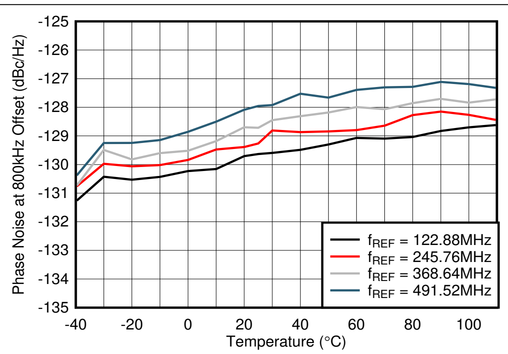
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 6-598. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



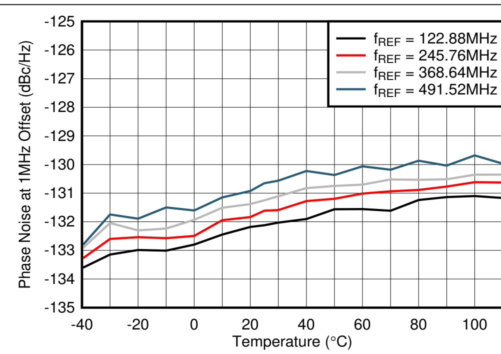
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-599. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



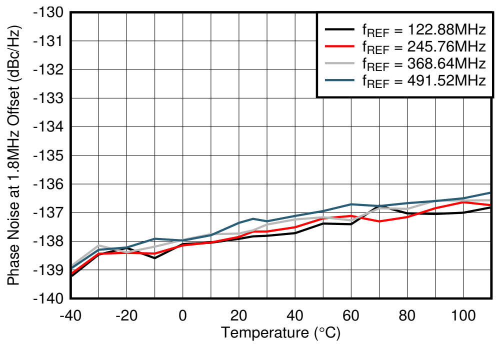
A. PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-600. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



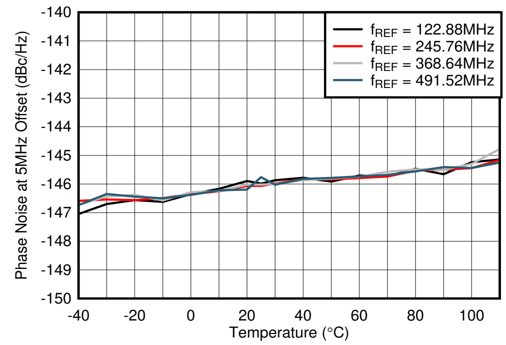
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-601. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



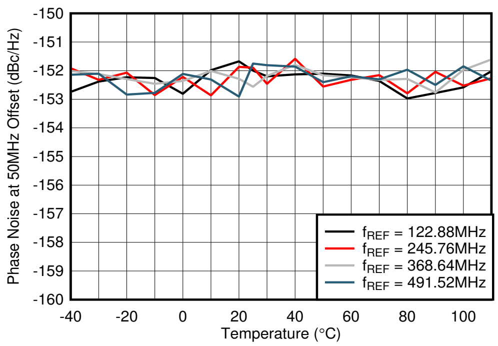
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-602. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



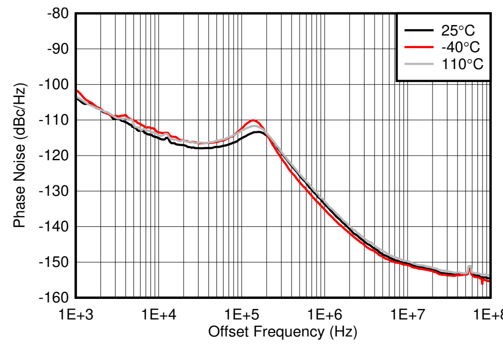
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-603. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



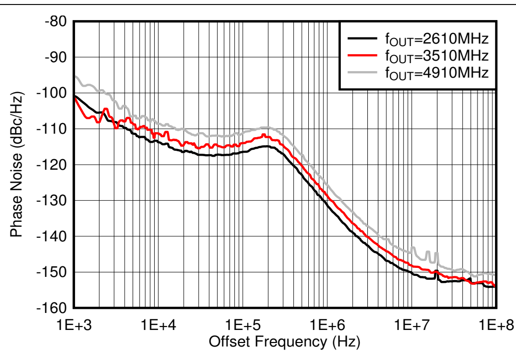
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-604. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



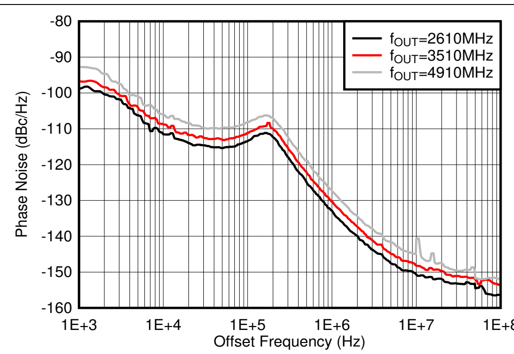
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-605. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



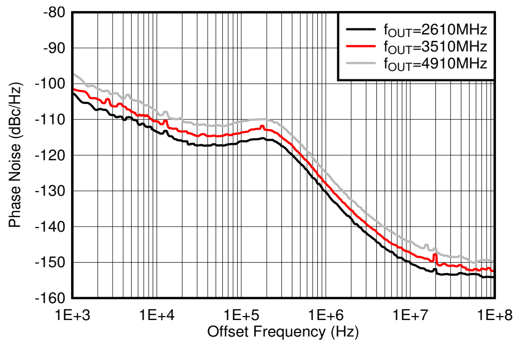
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-606. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



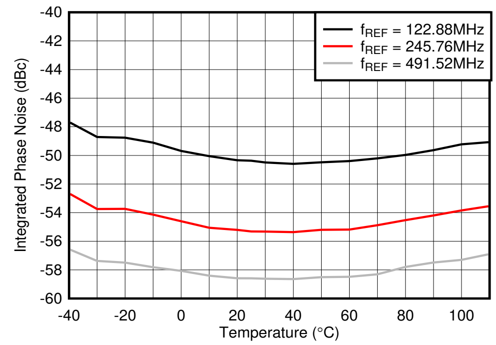
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-607. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



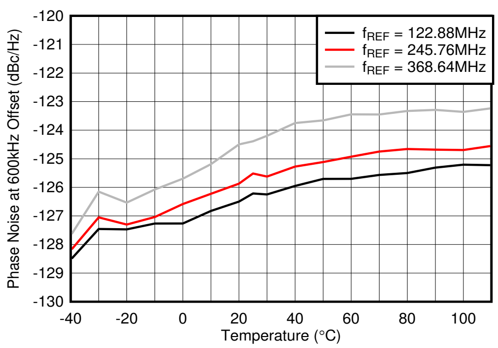
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-608. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



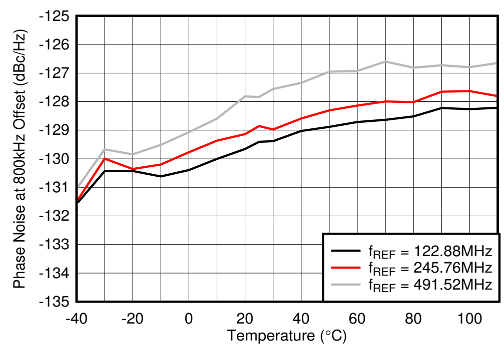
PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 6-609. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



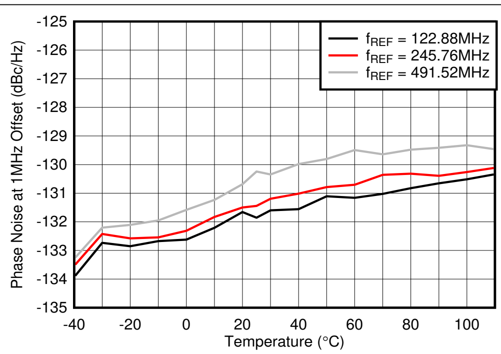
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-610. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



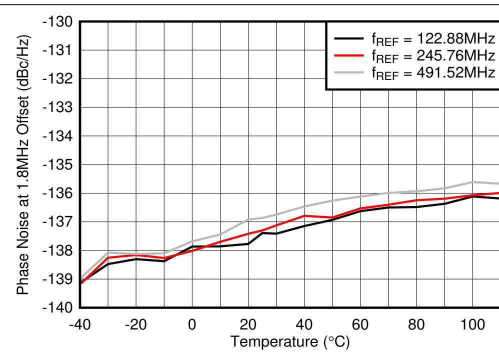
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-611. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



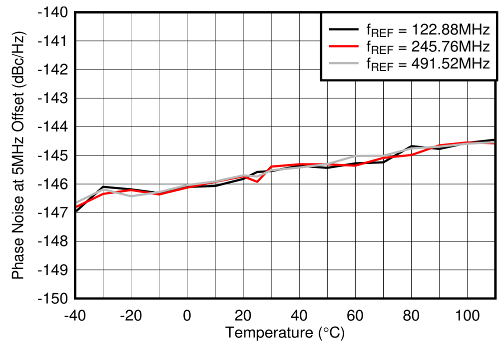
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-612. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



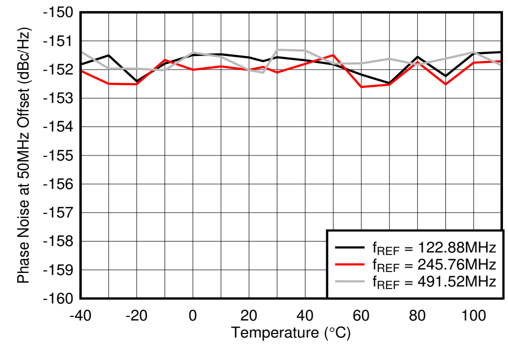
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-613. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



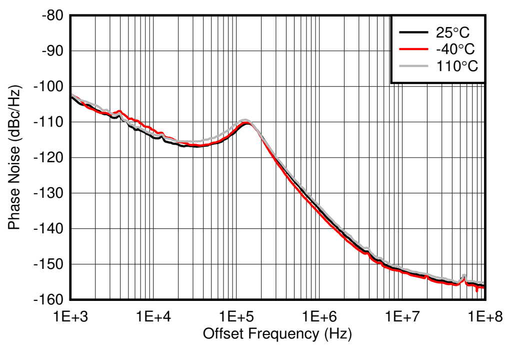
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-614. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



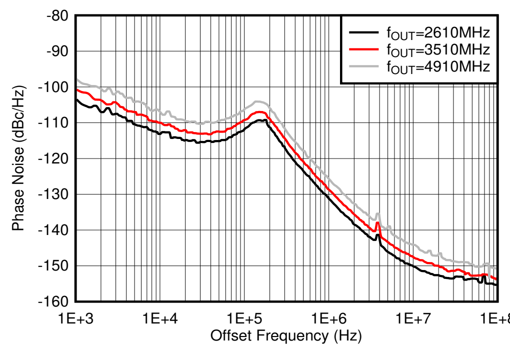
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-615. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



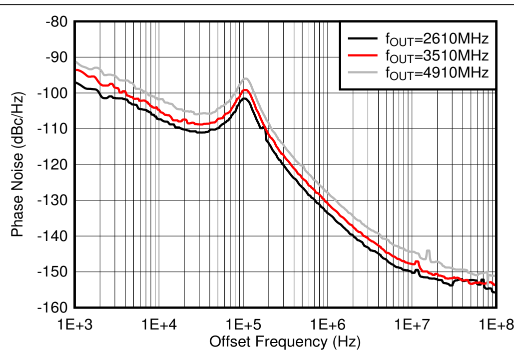
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-616. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



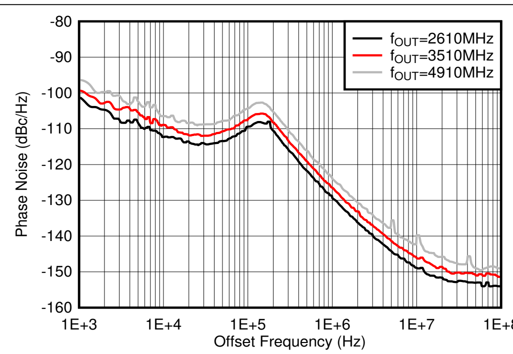
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-617. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



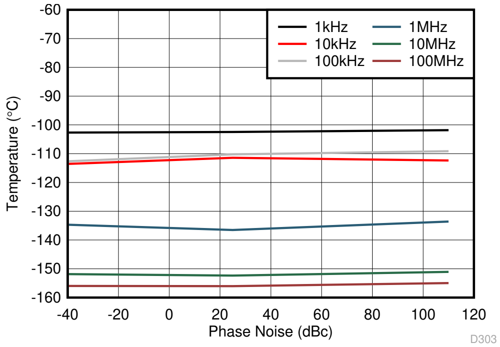
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-618. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



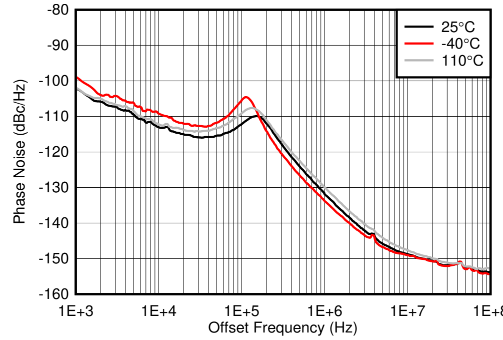
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-619. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, minimum LPF BW, measured at 2TXOUT

図 6-620. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-621. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

7 Device and Documentation Support

7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

7.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

7.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

7.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7903IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7903I	Samples
AFE7903IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7903 SNPB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

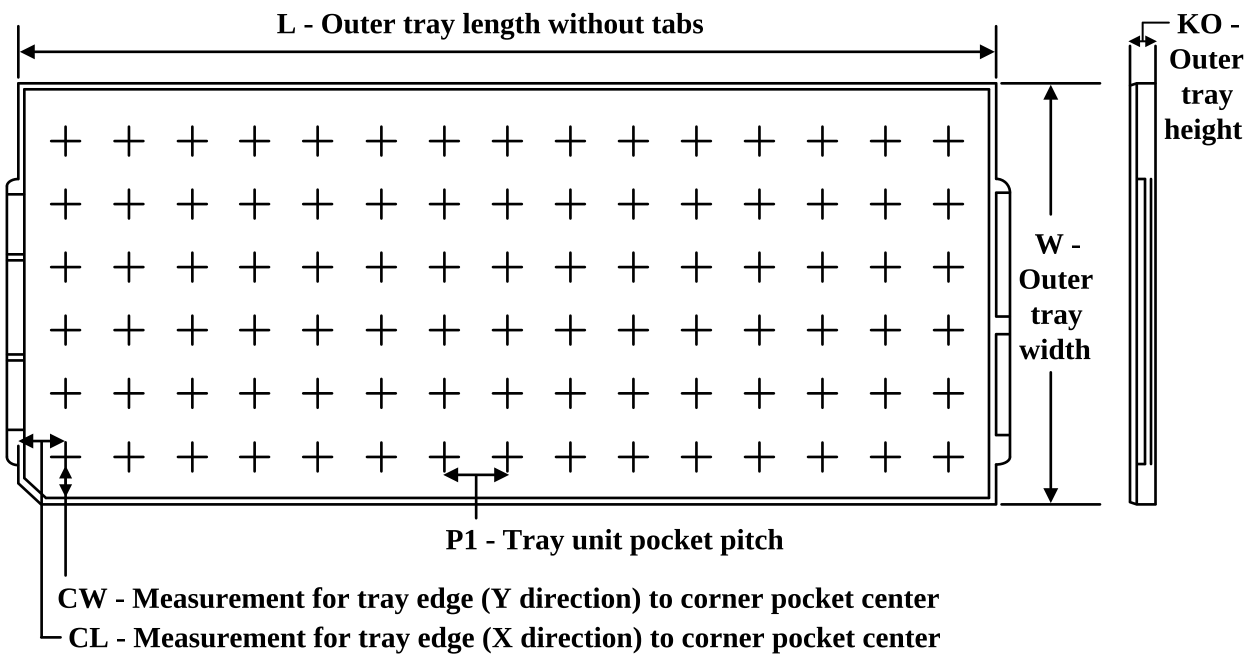
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

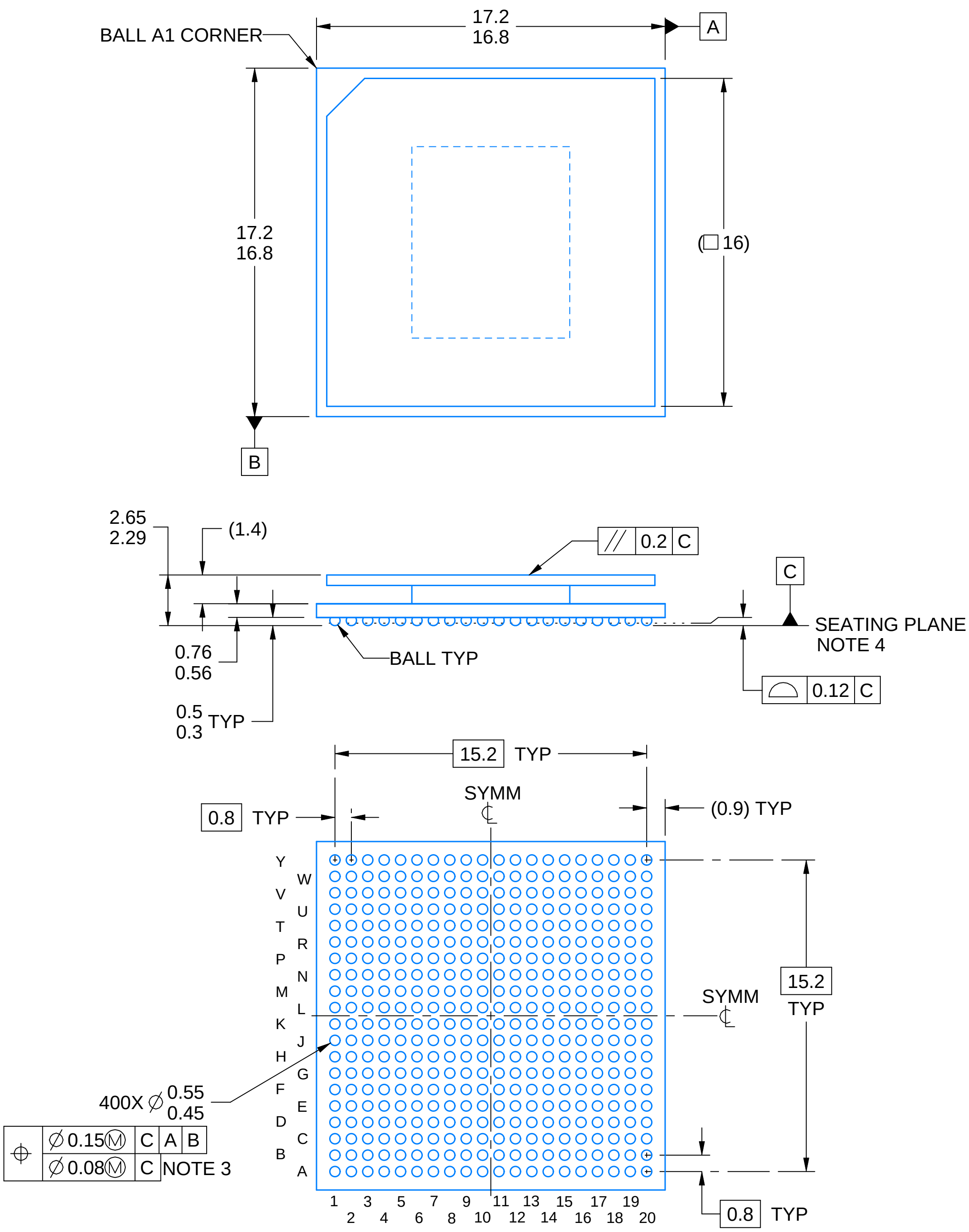
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

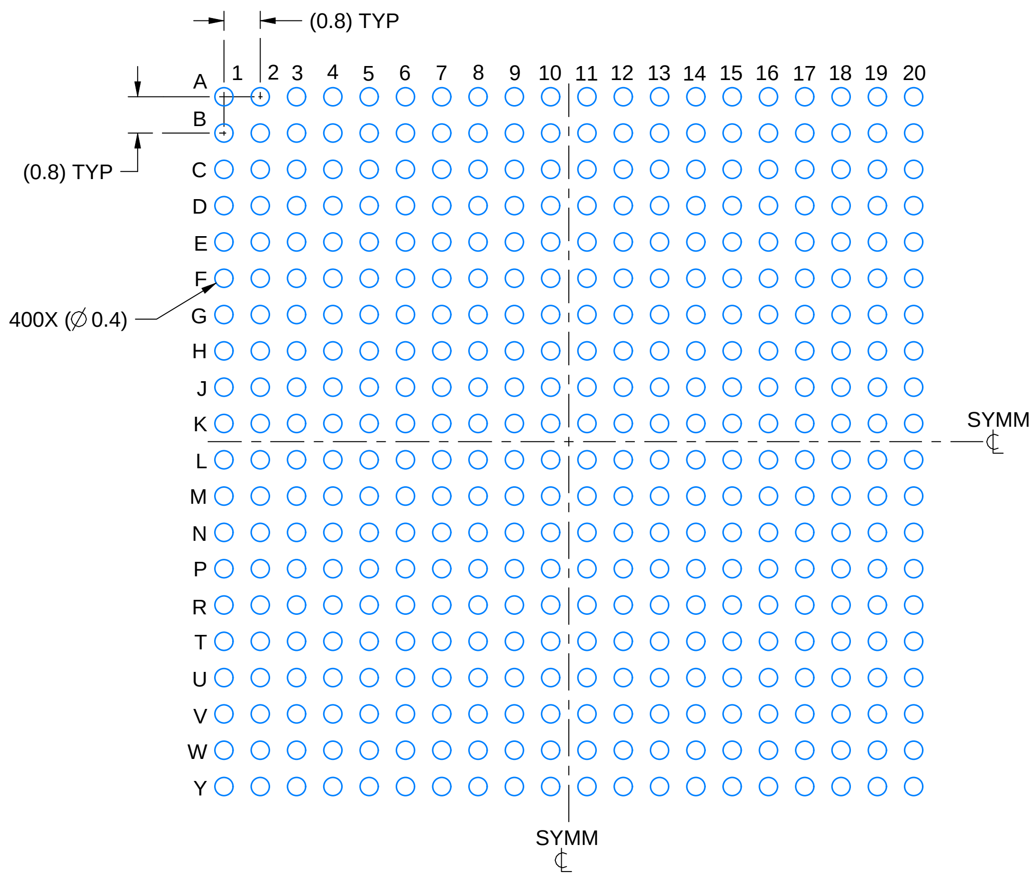
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7903IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7903IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7903IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7903IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



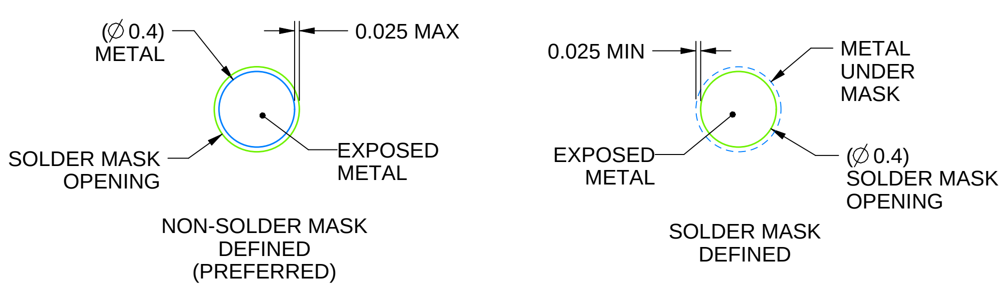
4221311/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

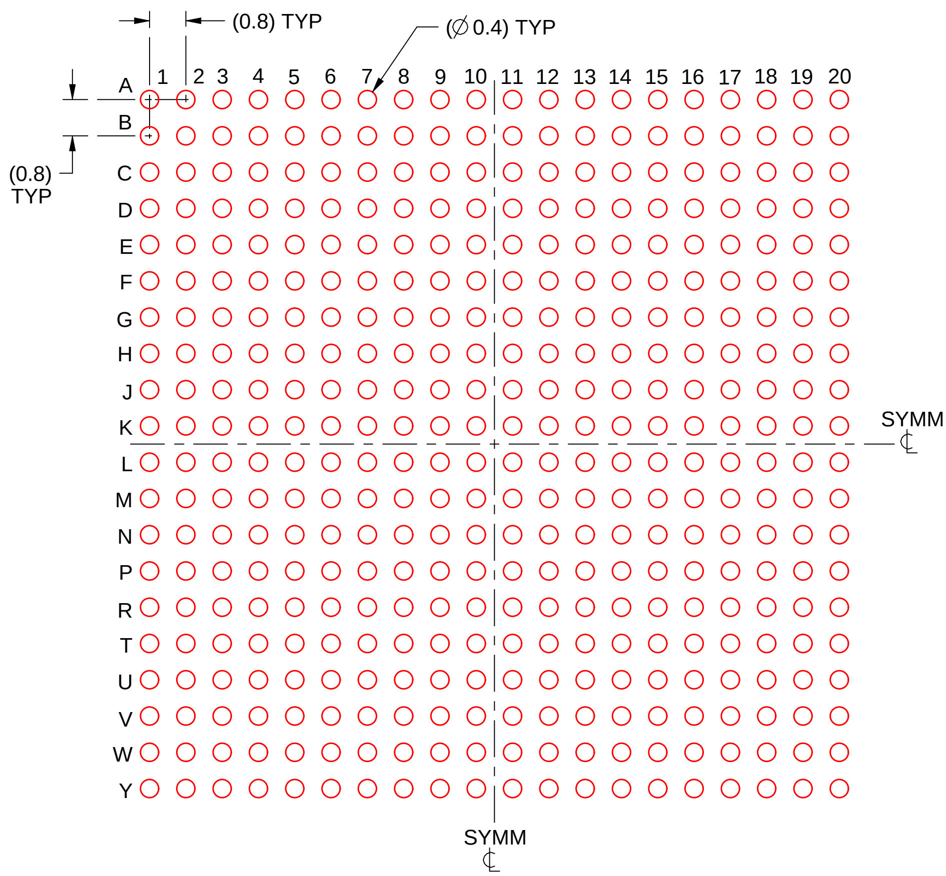


SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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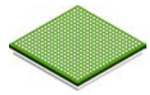
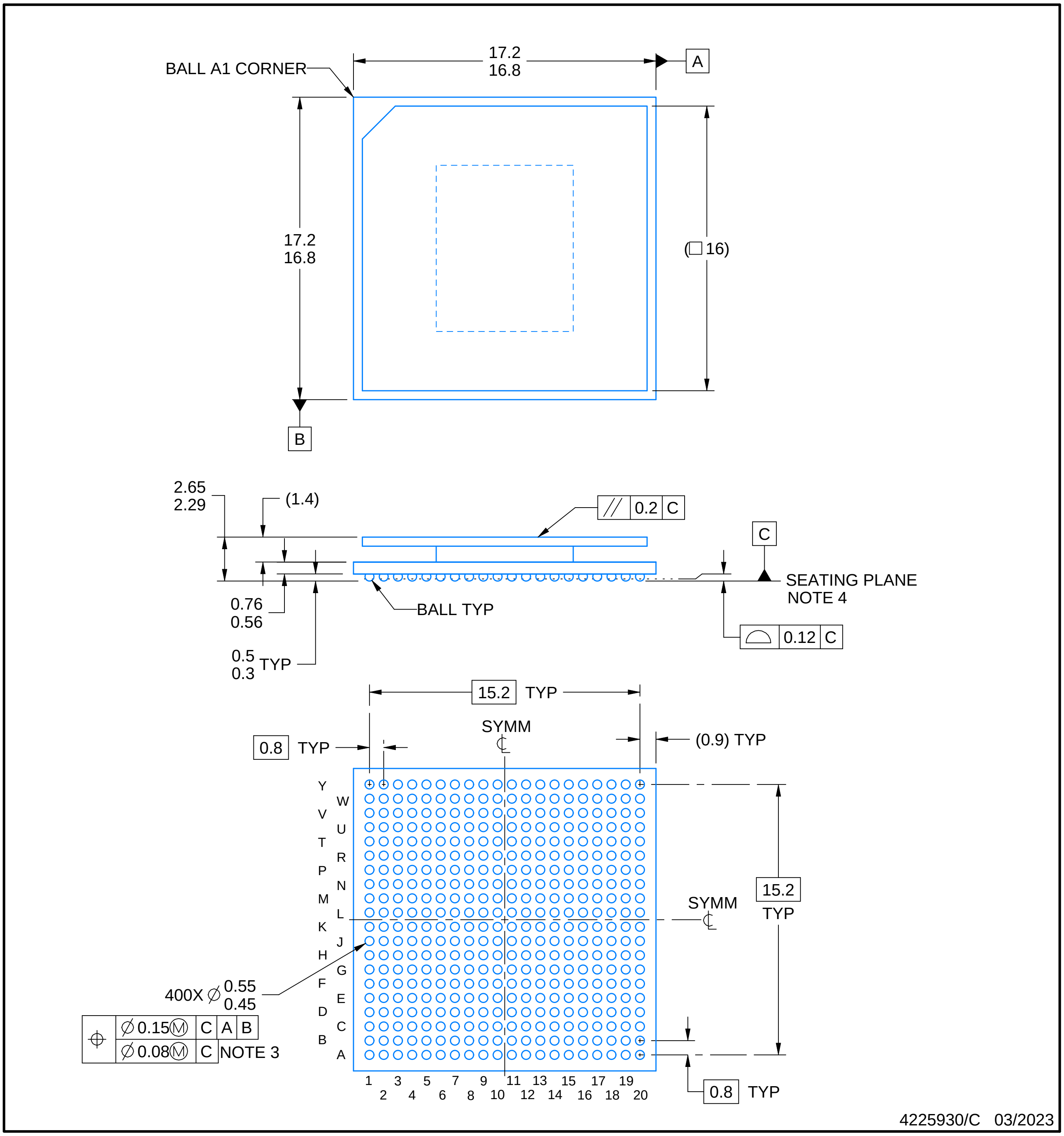


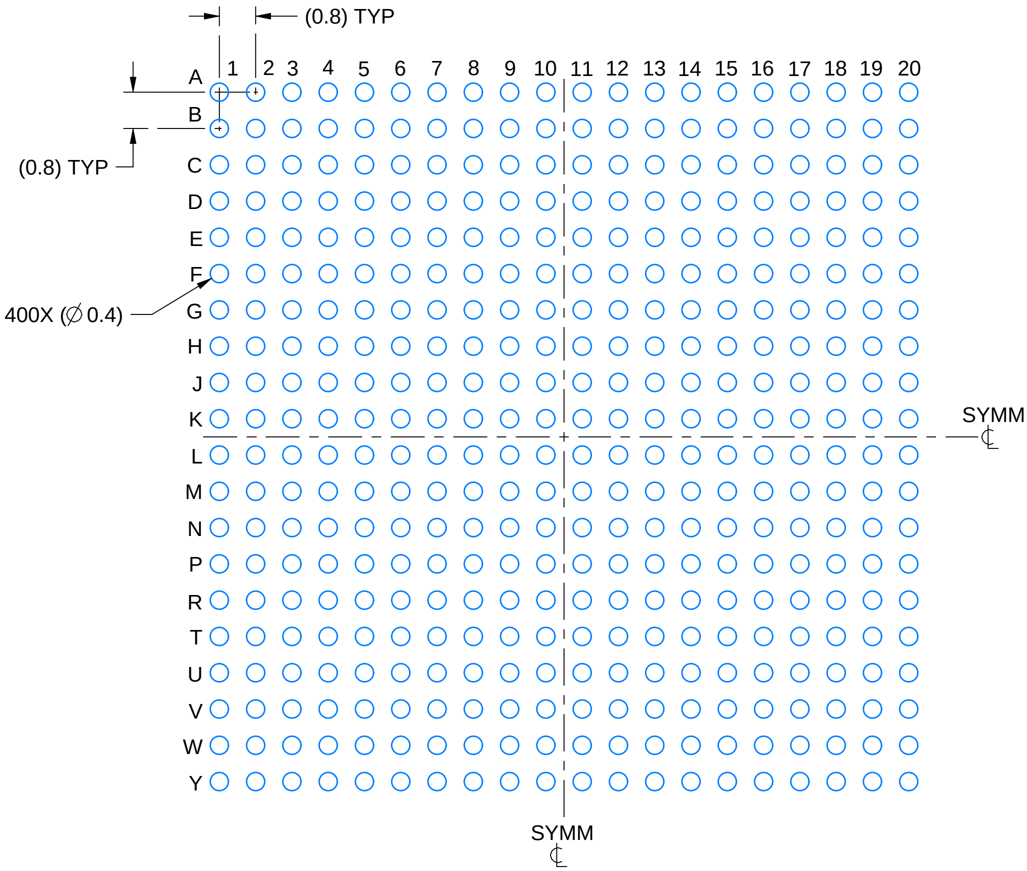
FCBGA - 2.65 mm max height

BALL GRID ARRAY

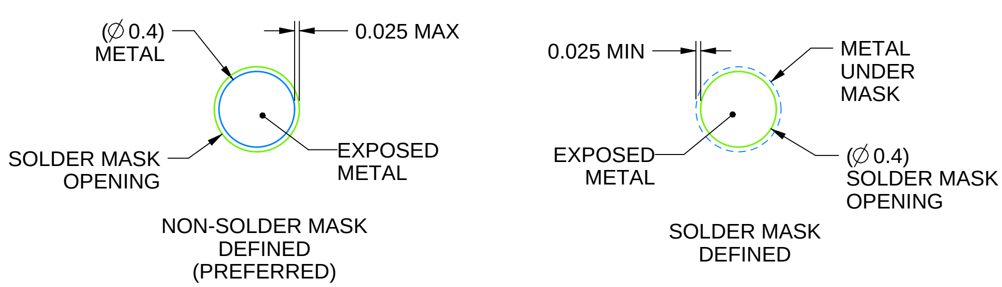


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

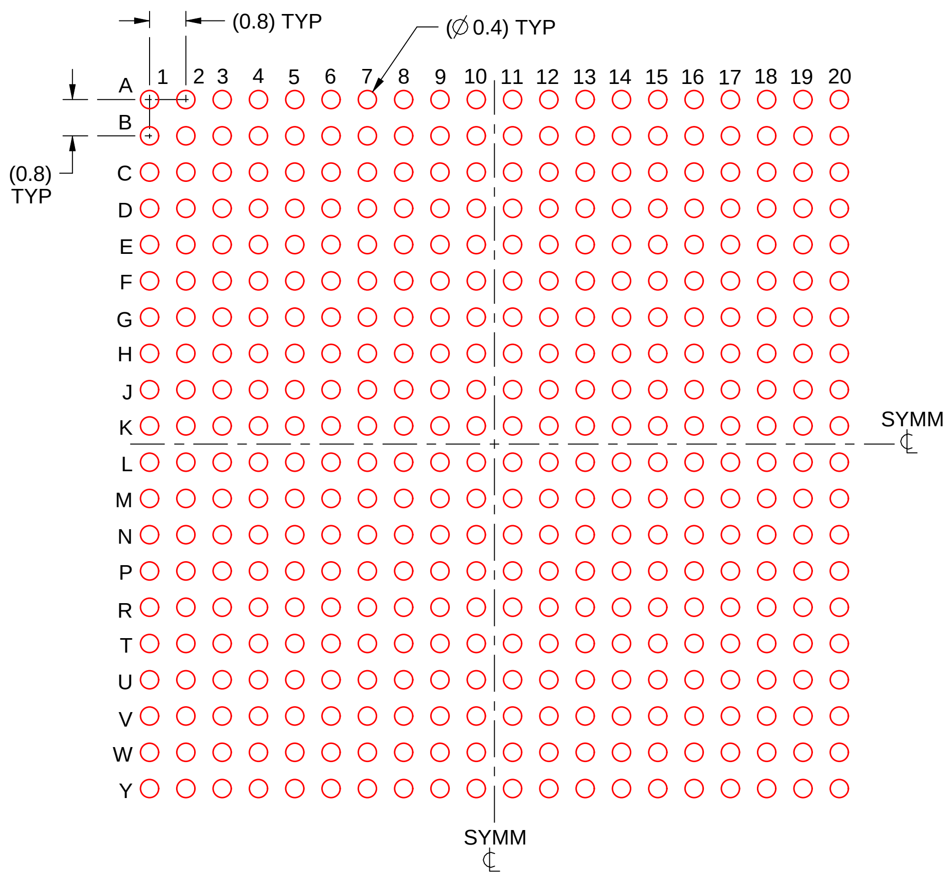


SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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