

AFE7955 12GSPS DAC と 3GSPS ADC 搭載、2T3R RF サンプリグ AFE

1 特長

- デュアル RF サンプリグ 12GSPS 送信 DAC
- トリプル RF サンプリグ 3GSPS 受信 ADC
- 最大 RF 信号帯域幅：1200MHz
- RF 周波数範囲：600MHz～12GHz
- デジタル・ステップ・アッテネータ (DSA)：
 - TX：40dB レンジ、0.125dB ステップ
 - RX：25dB レンジ、0.5dB ステップ
- シングルまたはデュアル・バンドの DUC と DDC
- TX または RX ごとに 16 個の NCO
- DAC もしくは ADC クロック用の内部 PLL もしくは VCO、または DAC もしくは ADC サンプル・レートでの外部クロックを選択可能
- SerDes データ・インターフェイス：
 - JESD204B、JESD204C 適合
 - 8 つの SerDes トランシーバ (最高 29.5Gbps)
 - サブクラス 1 のマルチデバイス同期
- パッケージ：17mm × 17mm FCBGA、0.8mm ピッチ

2 アプリケーション

- レーダー
- 追尾フロント・エンド
- 防衛無線
- 戦術通信網
- ワイヤレス通信テスト

3 概要

AFE7955 は、高性能で広帯域のマルチチャネル・トランシーバで、2 つの RF サンプリグ・トランスミッタ・チェーンと 3 つの RF サンプリグ・レシーバ・チェーンを内蔵しています。このデバイスは、最大 12GHz で動作するため、追加の周波数変換段を必要とせず、L、S、C、X バンドの周波数範囲について直接 RF サンプリグが可能です。密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

TX 信号パスは、TX チャネルあたり最大 1200MHz の信号帯域幅を実現する補間およびデジタル昇圧変換オプションをサポートしています。DUC の出力は、2 次ナイキスト動作を拡張する混在モード出力方式で 12GSPS の DAC (D/A コンバータ) を駆動します。DAC 出力は、40dB レンジ、1dB アナログ・ステップ、0.125dB デジタル・ステップの可変ゲイン・アンプ (TX DSA) を内蔵しています。

2 つのレシーバ・チェーンには、25dB レンジの DSA (デジタル・ステップ・アッテネータ) と、3GSPS の ADC (A/D コンバータ) が含まれています。2 つのレシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションにより信号帯域幅を RX チャネルごとに最高 1200MHz で最適化できます。

追加のレシーバ・チャネルには、最大 1200MHz の帯域幅をサポートする単一の広帯域 DDC があります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AFE7955	FC-BGA	17mm × 17mm

- 利用可能なすべてのパッケージについては、このデータシート末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。





Table of Contents

1 特長	1	5.8 Digital Electrical Characteristics.....	18
2 アプリケーション	1	5.9 Power Supply Electrical Characteristics.....	19
3 概要	1	5.10 Timing Requirements.....	25
4 Revision History	3	5.11 Switching Characteristics.....	26
5 Specifications	4	5.12 Typical Characteristics.....	27
5.1 Absolute Maximum Ratings.....	4	6 Device and Documentation Support	116
5.2 ESD Ratings.....	4	6.1 ドキュメントの更新通知を受け取る方法.....	116
5.3 Recommended Operating Conditions.....	5	6.2 サポート・リソース.....	116
5.4 Thermal Information AFE79xx.....	5	6.3 Trademarks.....	116
5.5 Transmitter Electrical Characteristics.....	6	6.4 静電気放電に関する注意事項.....	116
5.6 RF ADC Electrical Characteristics.....	12	6.5 用語集.....	116
5.7 PLL/VCO/Clock Electrical Characteristics.....	16	7 Mechanical, Packaging, and Orderable Information	116

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	−0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	−0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCML, VDD1P8GPIO, VDDA1P8	−0.5	2.1	V
Pin Voltage Range	{1/3}RXIN+/-	−0.5	VDDR1P8+0.3	V
	1FBIN+/-, 2FB+/-	−0.5	VDDFB1P8+0.3	V
	{1/3}TXOUT+/-	−0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	−0.3	1.4	V
	{1:8}SRX+/-	−0.3	1.4	V
	{1:8}STX+/-	−0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	−0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	−0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	−0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T _A	Ambient temperature	–40		85	°C
T _J	Operating Junction Temperature			110 ⁽¹⁾	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

5.4 Thermal Information AFE79xx

THERMAL METRIC ⁽¹⁾		17mmx17mm FC-BGA	UNIT
		400 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	16.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.42	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.85	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Transmitter Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC _{RES}	DAC resolution			14		bits
f _{RFout}	RF output frequency range	f _{DAC} = 12 GSPS, 1 st Nyquist	600		6000	MHz
		f _{DAC} = 12 GSPS, 2 nd Nyquist	6000		12000	
		f _{DAC} = 9 GSPS, 1 st Nyquist	600		4500	
		f _{DAC} = 9 GSPS, 2 nd Nyquist	4500		9000	
		f _{DAC} = 6 GSPS, 1 st Nyquist	600		3000	
		f _{DAC} = 6 GSPS, 2 nd Nyquist	3000		6000	
P _{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f _{out} = 850 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f _{out} = 1800 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f _{out} = 2600 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f _{out} = 3500 MHz, -0.5dBFS		3.9		dBm
		f _{out} = 4900 MHz, -0.5dBFS		3.1		dBm
		f _{out} = 3500 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f _{out} = 4900 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f _{out} = 4900 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f _{out} = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
		f _{out} = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm
R _{TERM}	Output termination resistor	Default setting		50		Ω
ATT _{range}	DSA Attenuation range			40		dB
ATT _{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT _{phase-err}	DSA Gain Steps Phase accuracy, any 8dB range	f _{out} = 850MHz ⁽¹⁾		±1		deg
		f _{out} = 1800MHz ⁽¹⁾		±1		deg
		f _{out} = 2600MHz ⁽¹⁾		±1		deg
		f _{out} = 3500MHz ⁽¹⁾		±1		deg
		f _{out} = 4900MHz ⁽¹⁾		±1		deg
		f _{out} = 8100MHz ⁽¹⁾		±2		deg
G _{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F _{out} < 4.9G		1.2		

5.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$, -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$, -13dBFS each tone		-74.4		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -13dBFS each tone		-71.1		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -13dBFS each tone		-67.8		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -13dBFS each tone		-64		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		50.8		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		51.9		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46.1		dBc
$f_{\text{S}}/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode		-51.9		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$, interleave mode		-46.0		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

5.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850\text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-48		dBFS

5.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3 \cdot f_s/4$	Fixed Spur	2nd Nyquist, $f_{\text{DAC}} = 5898.24\text{MSPS}$		-76		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 8847.36\text{MSPS}$		-89		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 11796.48\text{MSPS}$		-63		dBFS
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 0.85\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 1.8425\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc

5.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.4		%
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-136.9		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-134.6		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-133.0		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

5.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
PN _{TXADD}	Additive Phase Noise External Clock Mode ⁽²⁾	$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) After DSA calibration procedure
(2) Single side band, input clock phase noise subtracted.

5.6 RF ADC Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC _{RES}	ADC resolution			14		bits
F _{RFin}	RF input frequency range		600		12000	MHz
P _{FS_CW,min}	Min Full scale input power, at device pins ⁽¹⁾	$f_{\text{IN}} = 830\text{ MHz}$, DSA=0dB		-2.9		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA=0dB		-2.8		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA=0dB		-1.8		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA=0dB		-0.4		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA=0dB		0.1		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA=0dB		2.1		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA=0dB		4.3		dBm
P _{FS_CW,MAX}	MAX Full scale input power - reliability limited, at device pins	$f_{\text{IN}} = 830\text{ MHz}$, DSA = 20dB		16.7		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA = 20dB		17.0		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA = 20dB		18		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA = 20dB		18.5		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA = 20dB		19.3		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA = 20dB		21.3		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA = 20dB		23.5		dBm
S ₁₁	Input Return Loss	with matching network		-12.0		dB
ATT _{range}	DSA Attenuation range			25.0		dB
ATT _{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	$\Delta = \text{Gatt}(\text{X}) - \text{Gatt}(\text{X}-1)$, $F_{\text{in}} = 3610\text{MHz}$, after calibration		± 0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}} = 3610\text{MHz}$, after calibration		± 0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}} = 4910\text{MHz}$, after calibration		± 1.8		deg
NSD	Noise Density (small signal)	$f_{\text{IN}} = 830\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.2		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.0		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA = 3dB ⁽³⁾		-154.4		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA = 3dB ⁽³⁾		-154.1		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.1		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA = 3dB ⁽³⁾		-150		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA = 3dB ⁽³⁾		-151		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$, 3<=Atten<=22		-156.0		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, 3<=Atten<=25		-155.7		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, 3<=Atten<=25		-155.4		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$, 3<=Atten<=25		-152.5		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$, 3<=Atten<=25		-152.5		dBFS/Hz

5.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF _{min}	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 830 \text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760 \text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610 \text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610 \text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910 \text{ MHz}$		22.4		dB
		$f_{\text{IN}} = 8150 \text{ MHz}$		27.3		dB
		$f_{\text{IN}} = 9610 \text{ MHz}$		30		dB
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830 \text{ MHz}^{(4)}$		20.0		dB
		$f_{\text{IN}} = 1760 \text{ MHz}^{(4)}$		20.6		dB
		$f_{\text{IN}} = 2610 \text{ MHz}^{(4)}$		21.9		dB
		$f_{\text{IN}} = 3610 \text{ MHz}^{(4)}$		23.5		dB
		$f_{\text{IN}} = 4910 \text{ MHz}^{(4)}$		22.3		dB
		$f_{\text{IN}} = 8150 \text{ MHz}^{(4)}$		27.9		dB
		$f_{\text{IN}} = 9610 \text{ MHz}^{(4)}$		30.7		dB
NF _{max}	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830 \text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760 \text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610 \text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610 \text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910 \text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150 \text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610 \text{ MHz}$		45		dB
IMD3	3 rd order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82.4		dBc
		$f_{\text{IN}} = 1770 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84.1		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920 \text{ MHz}, 3 \leq \text{Atten} \leq 12$		-75.9		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}, 3 \leq \text{Atten} \leq 12$, 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$, 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830 \text{ MHz}$		88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		78.9		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		71		dBFS

5.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(2)}$	$f_{\text{IN}} = 830\text{ MHz}$		-85.5		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-90.5		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-84.2		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 830\text{ MHz}$		-80.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-85.3		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-75.4		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 830\text{ MHz}$		-88.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-80.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-81.7		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-78		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		89.8		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$, with board trim		-79.0		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$, with board trim		-101.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$, with board trim		-100		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$, with board trim		-101		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$, with board trim		-99.1		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$, with board trim		-107		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$, with board trim		-107		dBFS

5.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-95.4		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95.2		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-100		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-102		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-80		dBFS
TX-FB Isolation	1TXOUT to 1FBIN	$f_{\text{IN}} = 830\text{ MHz}$		-84		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-88		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-85		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-75		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-71		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-69		dBc
TX-RX Isolation	1TXOUT to 1RXIN 3TXOUT to 3RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-86		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-87		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-91		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-83		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-68		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-68		dBc

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB

5.7 PLL/VCO/Clock Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{\text{DAC}} = f_{\text{VCO}}$, $f_{\text{OUT}} = f_{\text{DAC}}/4$, normalized to f_{VCO} .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f_{VCO3}	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
$\text{DIV}_{\text{FBAD C}}$	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
$\text{DIV}_{\text{RXAD C}}$	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise $F_{\text{PLL}} = 11.79848 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 8.84736 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 9.8403 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 7.86432 \text{ GHz}$ $F_{\text{REF}} = 491.52 \text{ MHz}$	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F_{rms}	Clock PLL integrated phase error ⁽¹⁾	$f_{\text{PLL}} = 11.79848 \text{ GHz}$, [1KHz, 100MHz]		-43.4		dBc/Hz
		$f_{\text{PLL}} = 8.8536 \text{ GHz}$, [1KHz, 100MHz]		-47.6		dBc/Hz
		$f_{\text{PLL}} = 9.8304 \text{ GHz}$, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
$\text{PN}_{\text{pll_flat}}$	Normalized PLL flat Noise	$f_{\text{VCO}} = 11796.48 \text{ MHz}$		-226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz

5.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SS}	Input Clock level		0.6		1.8	Vppdiff
Coupling				AC Coupling Only		
	REFCLK input impedance ⁽²⁾	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution

(2) Refer to S11 data available from TI for impedance vs frequency

5.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V _{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V _{SRCOM}	SerDes Input Common Mode		0.4	0.5	0.6	V
Z _{SRdiff}	SerDes Internal Differential Termination ⁽¹⁾			100		Ω
F _{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance ⁽²⁾	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V _{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V _{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z _{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V _{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V _{IL}	Low-Level Input Voltage		0.4×VDD1 P8GPIO			V
I _{IH}	High-Level Input Current		-250		250	μA
I _{IL}	Low-Level Input Current		-250		250	μA
C _L	CMOS input capacitance			2		pF
V _{OH}	High-Level Output Voltage		VDD1P8G PIO-0.2			V
V _{OL}	Low-Level Output Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
Clock _{MODE}				PLL Clock Mode Only		
F _{SYSREFMAX}	SYSREF Input Frequency Maximum			40		MHz
V _{SWINGSRMAX}	SYSREF Input Swing Maximum			1.8		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} < 500MHz		0.3		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} > 500MHz		0.6		Vppdiff ⁽³⁾
V _{COMSRMAX}	SYSREF Input Common Mode Voltage Maximum			0.8		V
V _{COMSRMIN}	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z _T	Input termination	differential		100 ⁽¹⁾		Ω
C _L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V _{ICOM}	Input Common Voltage			1.2		V
V _{ID}	Differential Input Voltage swing			450		Vppdiff ⁽³⁾

5.8 Digital Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff ⁽³⁾
Z_T	Internal Termination			100		Ω

- (1) SYSREF termination is programmable between 100 Ω , 150 Ω and 300 Ω
- (2) Loss tolerance is bump to bump from STX to SRX
- (3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

5.9 Power Supply Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 2T1F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec $f_{\text{DAC}} = 5898.24$ SPS $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85$ GHz 64/66 coding, 16.22Gbps TX: 2-4-4-1, FB: 1-2-4-1		460		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			338		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71.3		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			734		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1273		mA
P_{diss}	Power Dissipation			3623		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 2T2R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% TX Dual Band 18x Int, FB 6x Dec, RX Dual Band 24x Dec. TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}}=f_{\text{IN}}= 1.9, 2.6$ GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 1-2-4-1, RX: 1-8-16-1		461		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			528		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69.1		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			780		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1671		mA
P_{diss}	Power Dissipation			4387		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 2T2R1F - FDD FB 100% on TX Dual Band 18x Int, FB 6x Dec RX Dual Band RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 1-2-4-1, RX: 1-8-16-1		801		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			606		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71.6		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1261		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2409		mA
P_{diss}	Power Dissipation			6402		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 2T2R1F - FDD FB 100% on 7.3728 GSPS DAC, 2.4576 GSPS ADC. TX dual band 15x Int, FB 5x decimation, RX dual band 20x decimation. TX/FB Rate 491.52 Msps, RX Rate 122.88 Msps $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 1-2-4-1, RX: 1-8-16-1		780		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			581		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			67		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1192		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2203		mA
P_{diss}	Power Dissipation			6037		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 2T2R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 3.5\text{ GHz}$ $f_{\text{RX}} = 3.5\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-4-2-1, FB: 2-2-4-2, RX: 2-4-4-1		459		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			548		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			877		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1754		mA
P_{diss}	Power Dissipation			4616		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6a: TDD 2T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		388		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			372		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1066		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1677		mA
P_{diss}	Power Dissipation			4323		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6b: TDD 2R (TX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		374		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			391		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			68.3		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			597		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1233		mA
P_{diss}	Power Dissipation			3356		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6c: TDD 2T2R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		385		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			376		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLCO			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			949		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1566		mA
P_{diss}	Power Dissipation			4081		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6d: FDD 2T2R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		534		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			413		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLCO			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1208		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1947		mA
P_{diss}	Power Dissipation			5078		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			244		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			16		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			51		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			249		mA
P_{diss}	Power Dissipation			795		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: 2T2R1F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 5898.24\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 0.85\text{ GHz}$ $f_{\text{RX}} = 0.8\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 2-4-4-1, FB: 1-2-4-1, RX: 1-4-8-1		798		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			432		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1041		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1637		mA
P_{diss}	Power Dissipation			5106		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 9: 2T2R1F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{\text{DAC}} = 8847.36\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 4-4-2-1, FB: 2-2-2-1, RX: 2-4-4-1		798		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			541		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1139		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2065		mA
P_{diss}	Power Dissipation			5811		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10a: TDD 2T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 4-4-2-1, FB/RX: 2-2-4-2		484		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			489		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71.3		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1256		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2038		mA
P_{diss}	Power Dissipation			5272		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10b: TDD 2R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 4-4-2-1, FB/RX: 2-2-4-2		377		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			507		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			625		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1452		mA
P_{diss}	Power Dissipation			3813		mW

5.9 Power Supply Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10c: TDD 2T2R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 4-4-2-1, FB/RX: 2-2-4-2		457		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			494		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			71		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1098		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1891		mA
P_{diss}	Power Dissipation			4907		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10d: FDD 2T2R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} =$ 11796.48 MSPS, mixed mode, $f_{\text{ADC}} =$ 2949.12 MSPS $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 4-4-2-1, FB/RX: 2-2-2-1		642		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			527		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1418		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2364		mA
P_{diss}	Power Dissipation			6120		mW

5.10 Timing Requirements

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_s(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_h(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_s(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_h(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK ⁽¹⁾			$5 + t_{\text{SCLK}}$	ns
$t_s(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_h(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{\text{(SCLK)_W}}$	Minimum SCLK period: registers write			25	ns
$t_{\text{(SCLK)_R}}$	Minimum SCLK period: registers read			50	ns
$t_{\text{d(data_out)}}$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

5.11 Switching Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

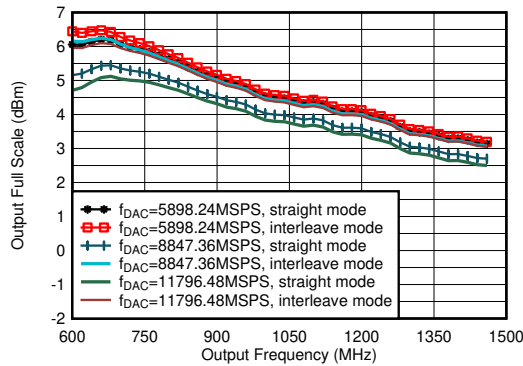
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t _{JESD TX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles ⁽¹⁾
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD RX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles ⁽¹⁾
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD FB}	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles ⁽¹⁾
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

5.12 Typical Characteristics

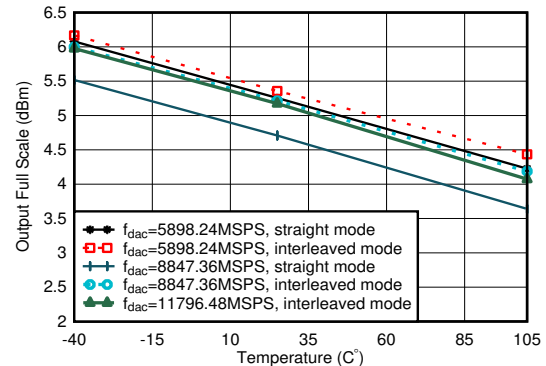
5.12.1 TX Typical Characteristics 800 MHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



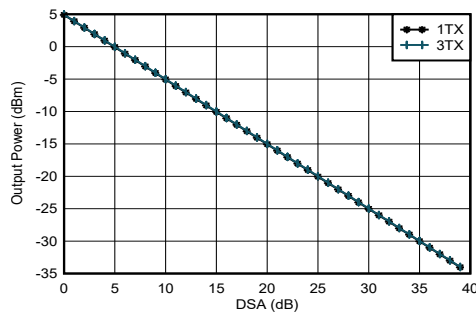
including PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 0.8 GHz matching

FIG 5-1. TX Output Fullscale vs Output Frequency



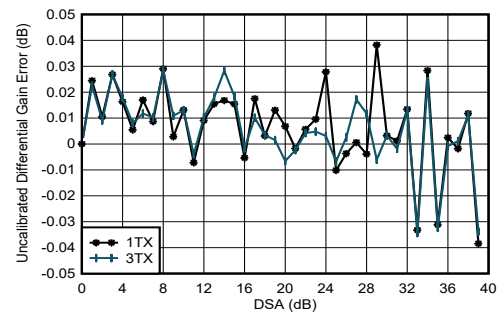
including PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 0.8 GHz matching

FIG 5-2. TX Output Fullscale vs Temperature



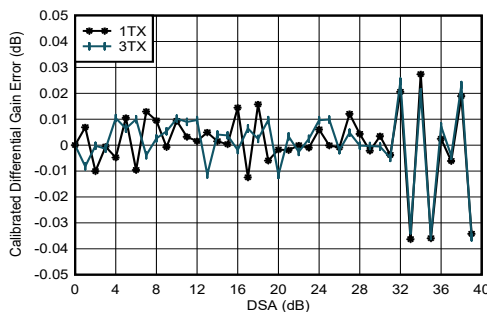
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $A_{\text{out}} = -0.5$ dBFS, matching 0.8 GHz

FIG 5-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz



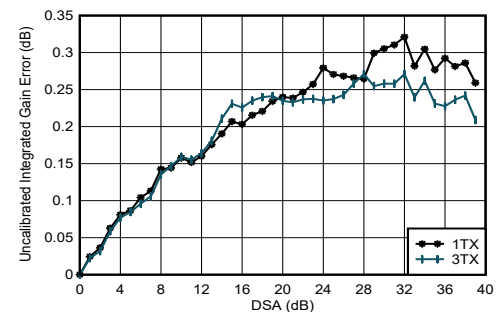
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

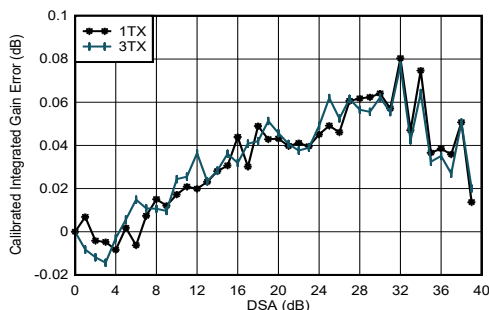


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

FIG 5-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

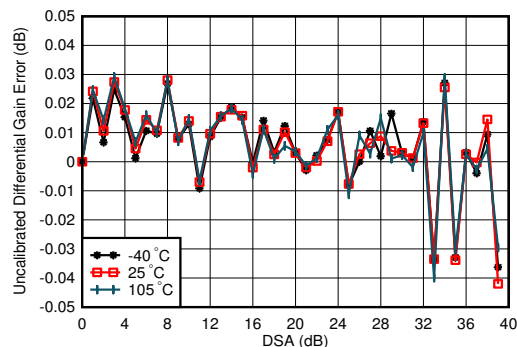
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



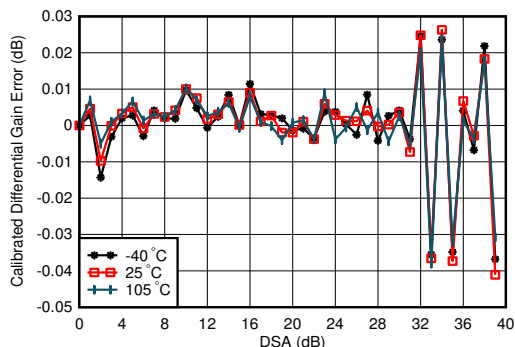
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

FIG 5-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



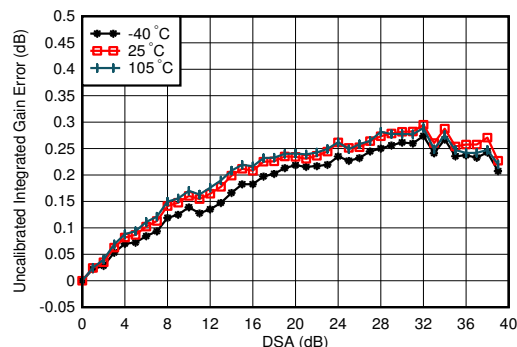
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



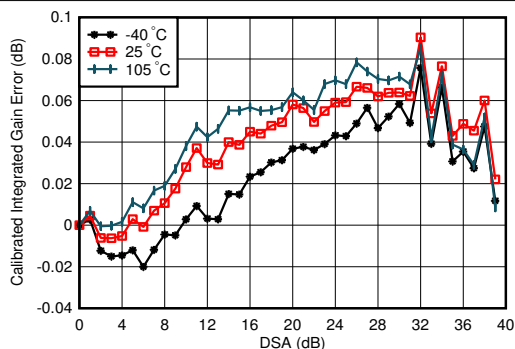
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



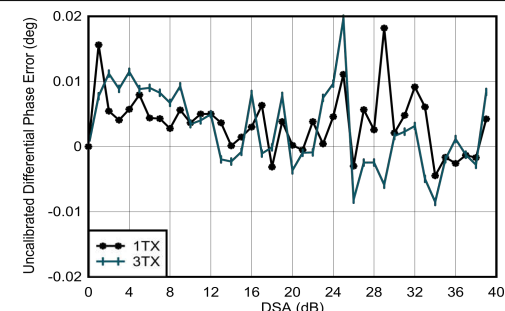
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

FIG 5-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

FIG 5-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

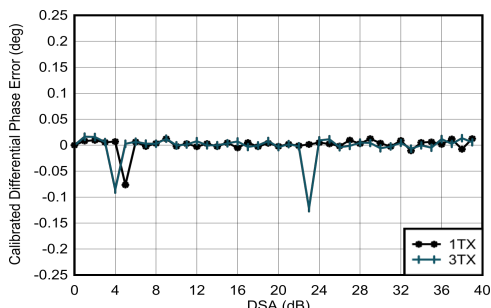


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

FIG 5-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

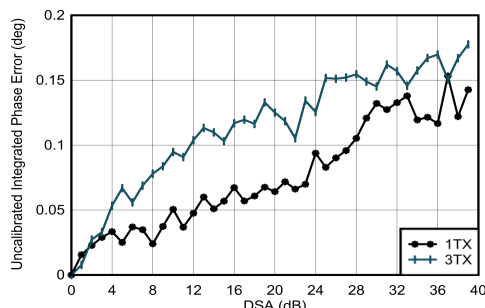
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



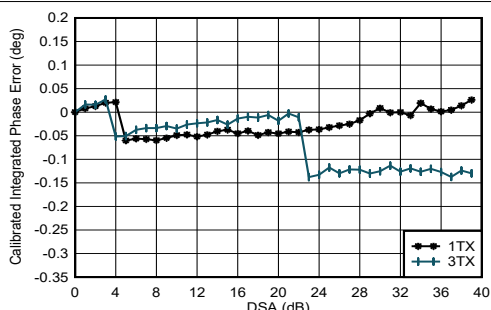
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

FIG 5-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



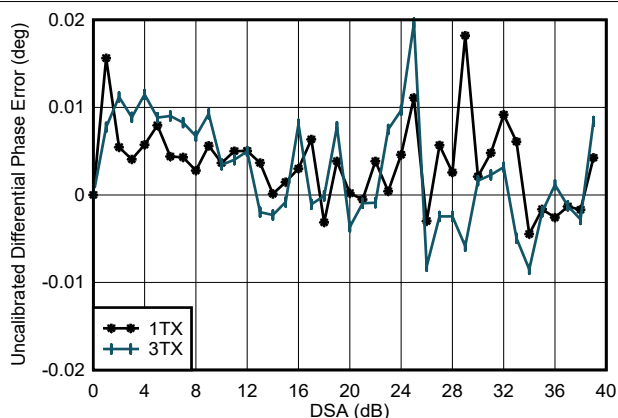
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

FIG 5-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

FIG 5-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

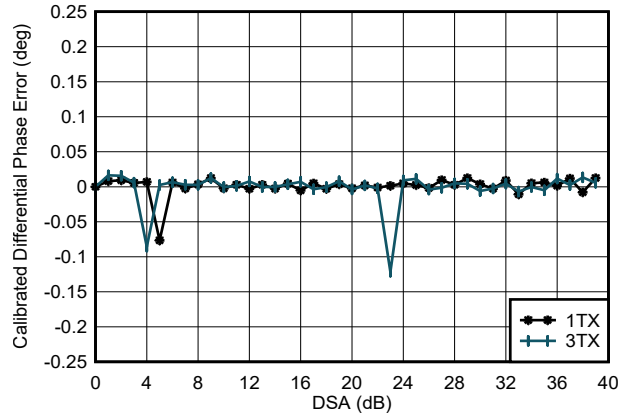


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

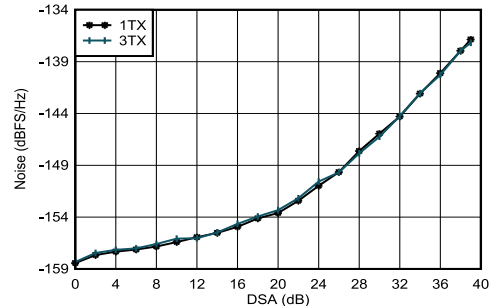
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



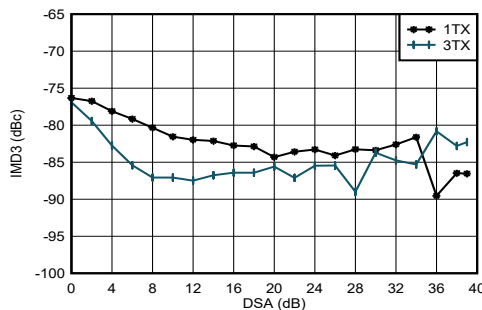
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

图 5-17. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



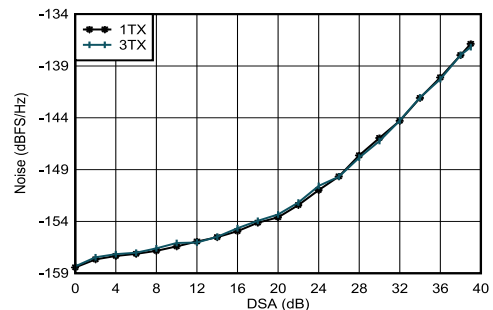
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

图 5-18. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



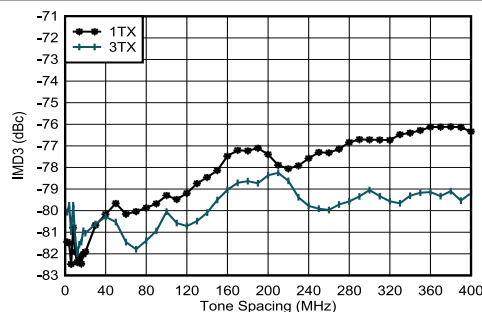
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
 Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

图 5-19. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



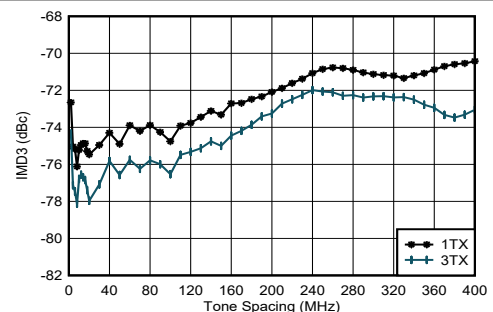
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz,
 $P_{\text{OUT}} = -13$ dBFS

图 5-20. TX Output Noise vs Channel and Attenuation at 0.85 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

图 5-21. TX IMD3 vs DSA Setting at 0.85 GHz

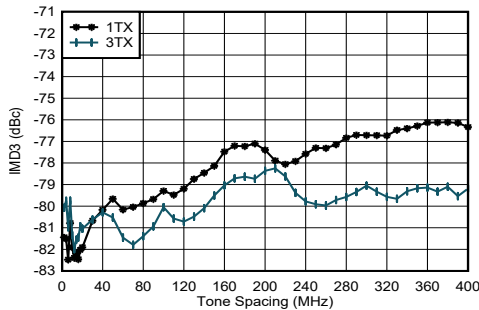


$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

图 5-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

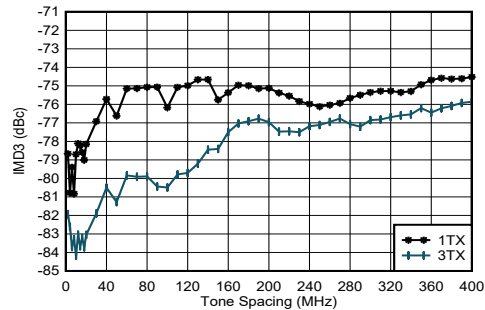
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



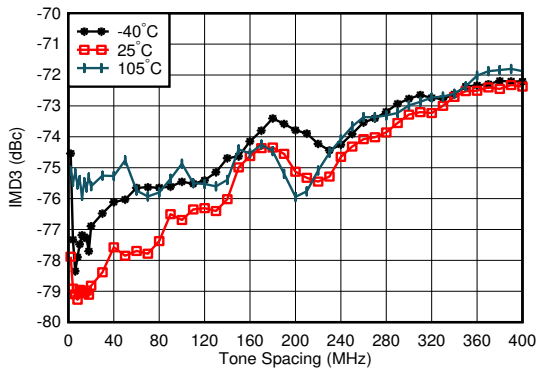
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

FIG 5-23. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



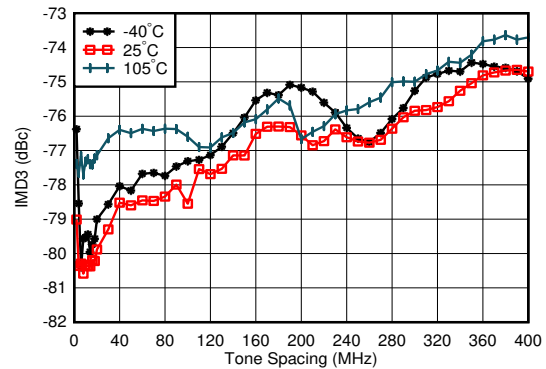
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

FIG 5-24. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



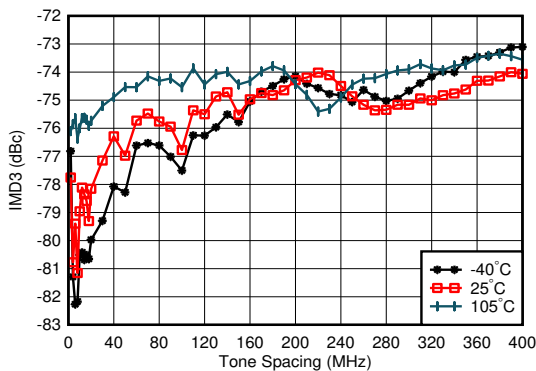
$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

FIG 5-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



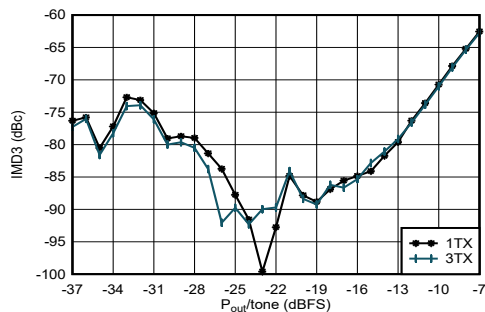
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

FIG 5-26. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

FIG 5-27. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

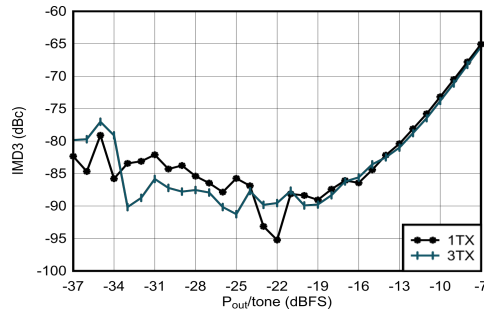


$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

FIG 5-28. TX IMD3 vs Digital Level at 0.85 GHz

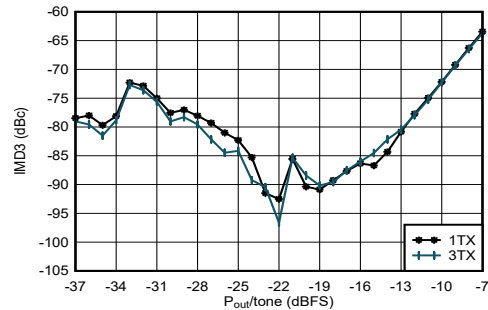
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



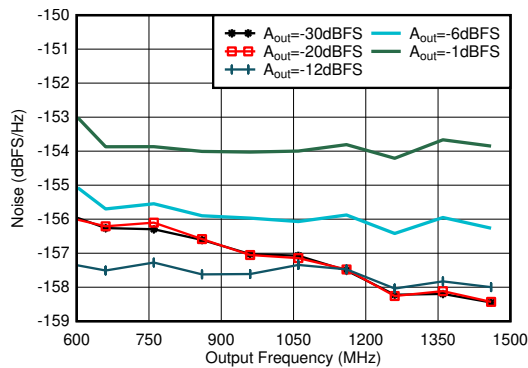
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

FIG 5-29. TX IMD3 vs Digital Level at 0.85 GHz



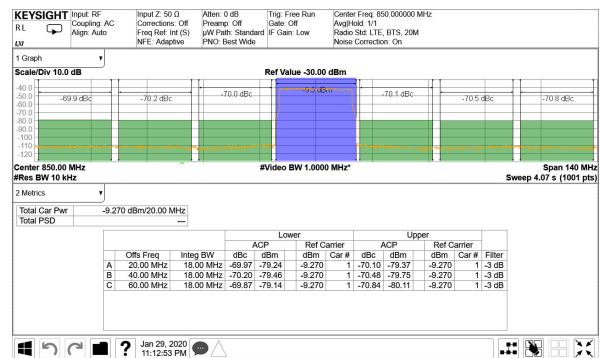
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

FIG 5-30. TX IMD3 vs Digital Level at 0.85 GHz



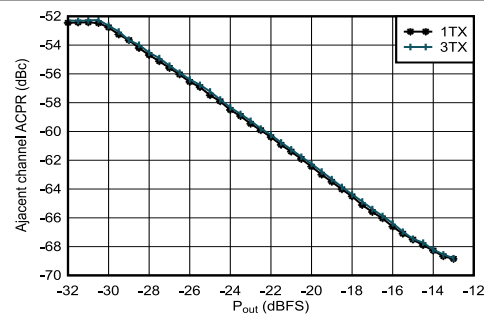
Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSPS,
interleave mode, 40-MHz offset, DSA = 0dB

FIG 5-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



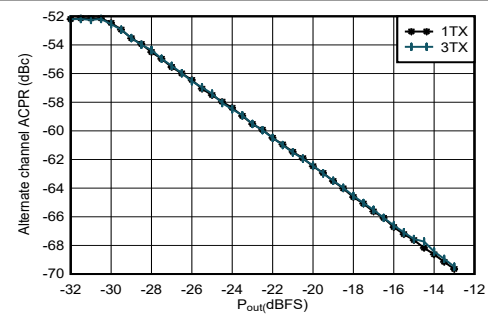
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

FIG 5-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

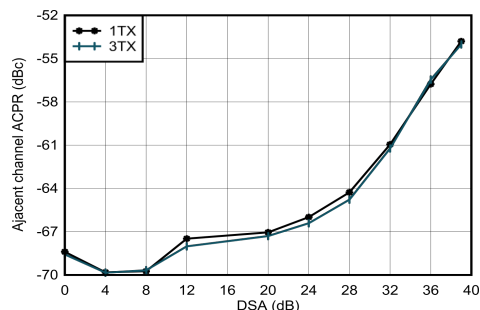


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

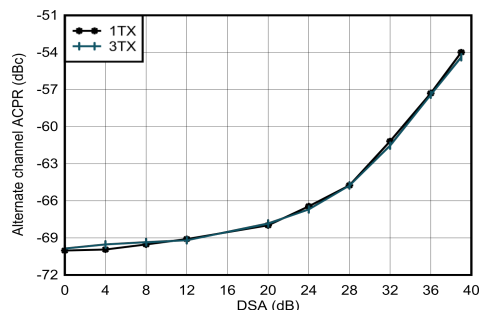
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



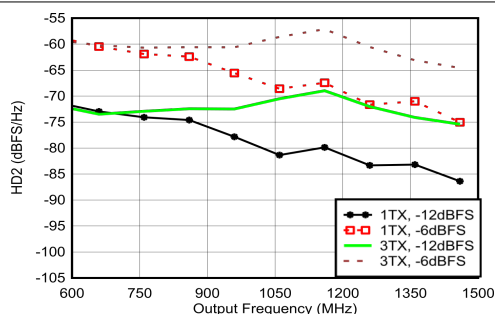
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-35. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



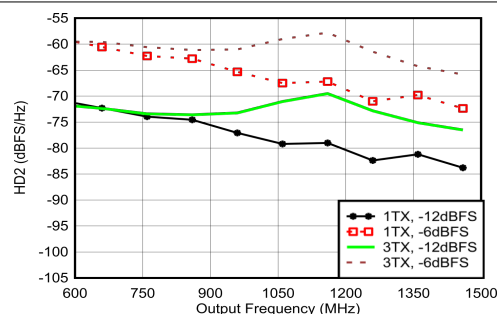
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 5-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



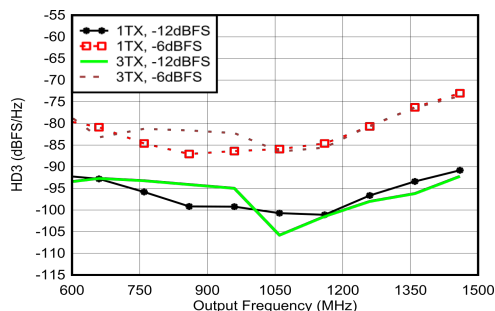
Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24$ GSPS, straight mode

Figure 5-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



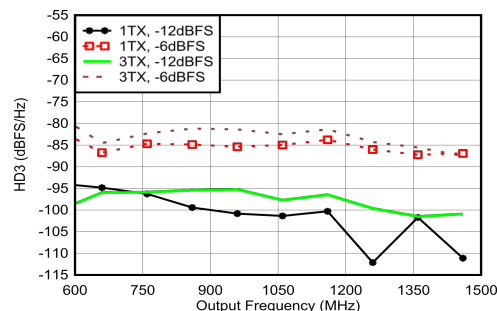
Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36$ GSPS, straight mode

Figure 5-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24$ MSPS, straight mode, normalized to output power at harmonic frequency

Figure 5-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

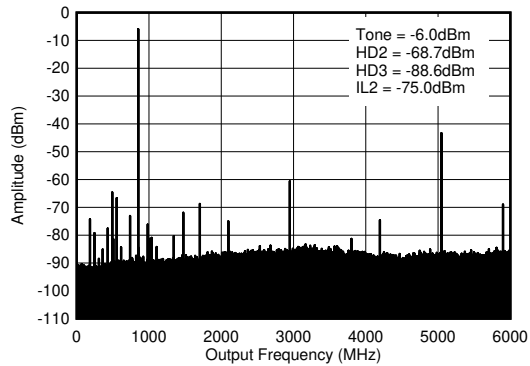


Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36$ MSPS, straight mode, normalized to output power at harmonic frequency

Figure 5-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

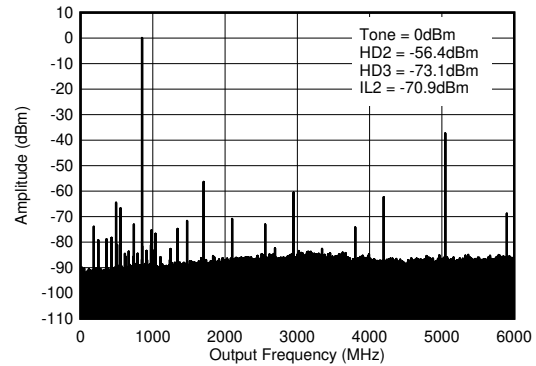
5.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



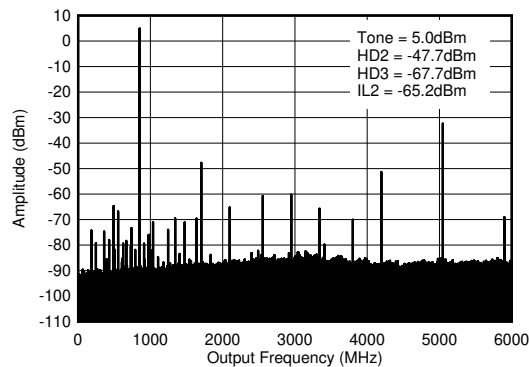
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/\text{n} \pm f_{\text{OUT}}$.

FIG 5-41. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/\text{n} \pm f_{\text{OUT}}$.

FIG 5-42. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

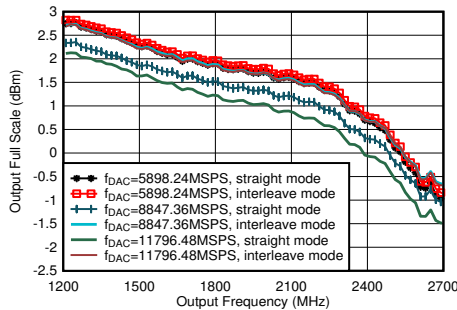


$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/\text{n} \pm f_{\text{OUT}}$.

FIG 5-43. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

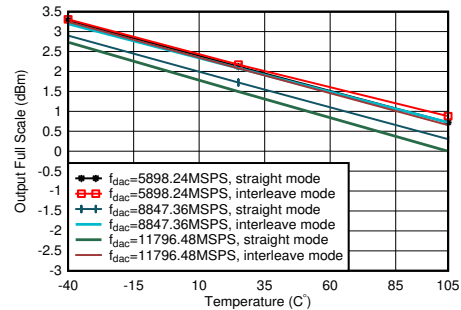
5.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



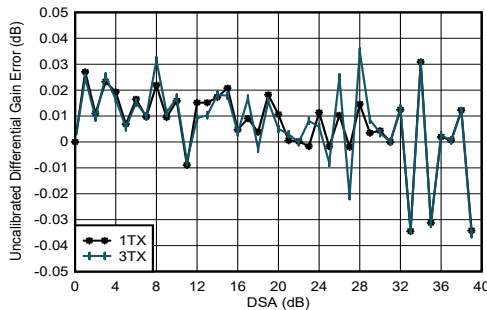
including PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 1.8 GHz matching

Figure 5-44. TX Output Fullscale vs Output Frequency



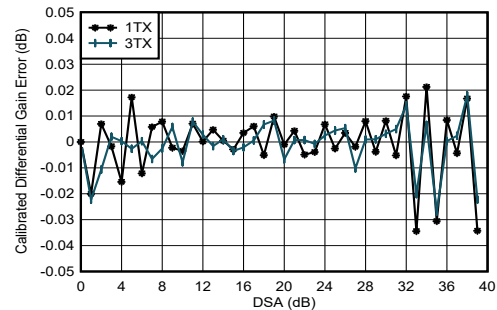
$A_{\text{out}} = -0.5$ dBFS, matching 1.8 GHz

Figure 5-45. TX Output Power vs Temperature at 1.8 GHz



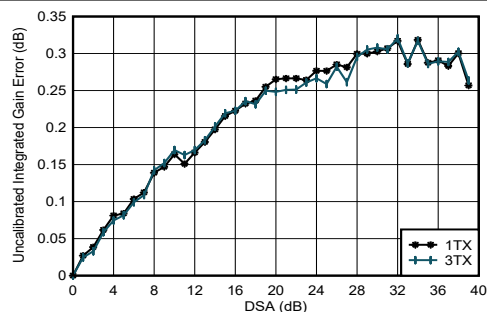
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 5-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



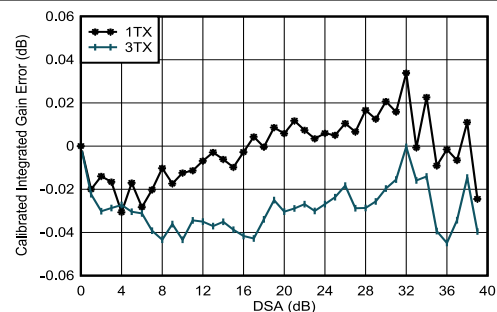
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 5-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 5-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

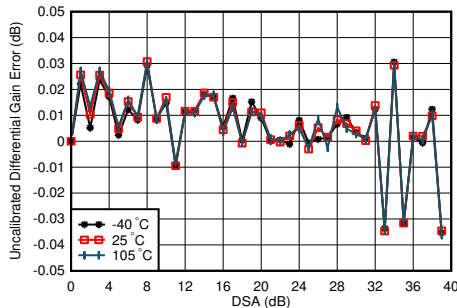


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 5-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

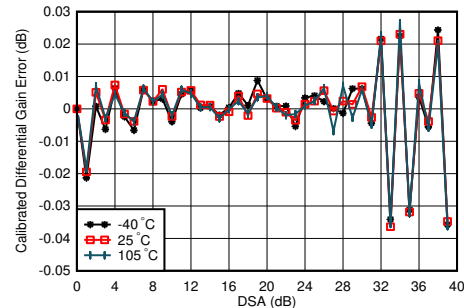
5.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



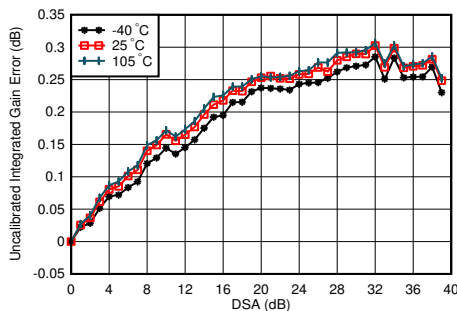
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



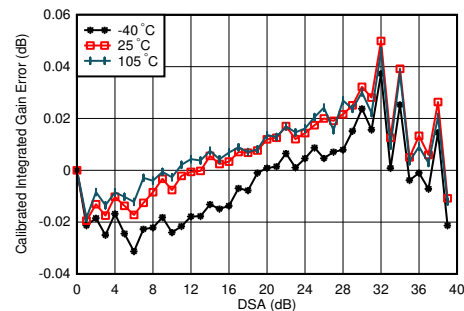
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



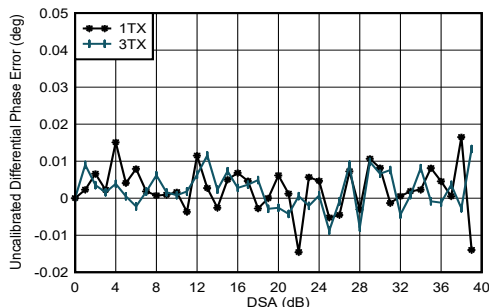
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



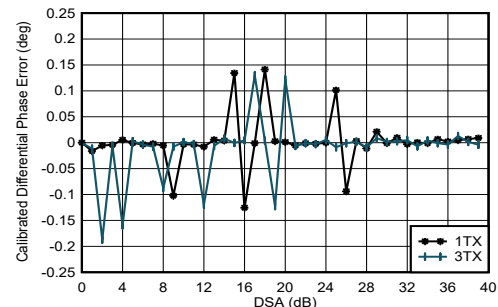
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

FIG 5-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

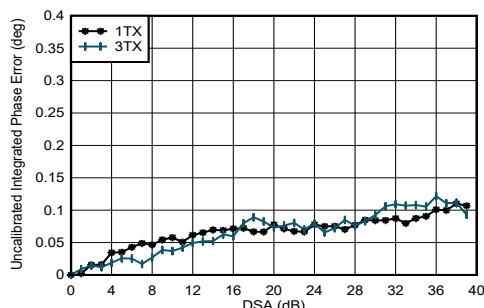


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
 Phase DNL spike may occur at any DSA setting.

FIG 5-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

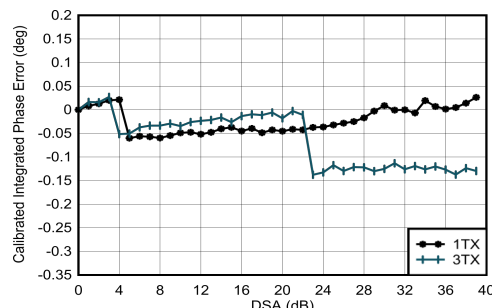
5.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



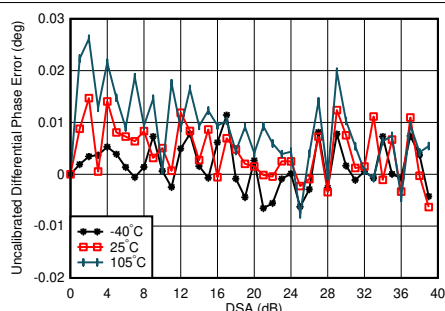
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



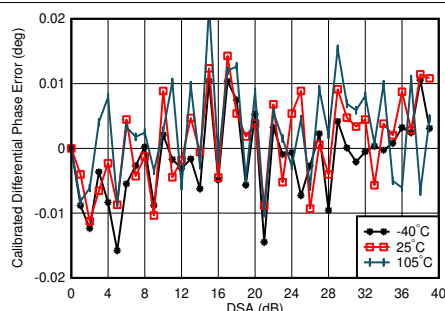
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



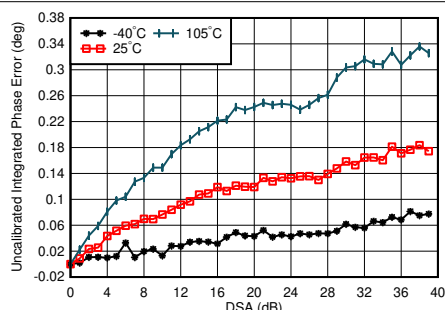
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

FIG 5-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



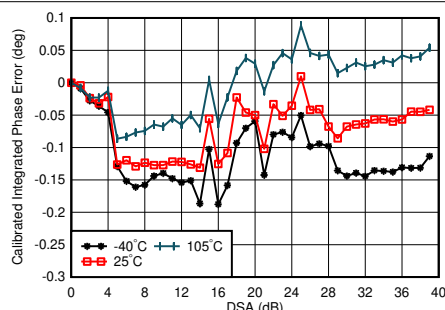
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

FIG 5-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-60. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz

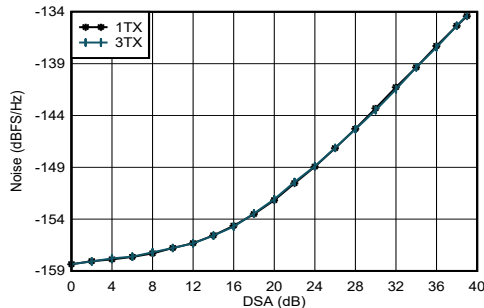


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-61. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz

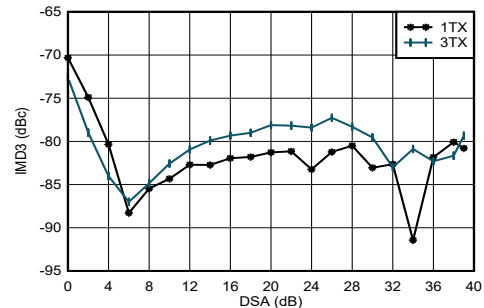
5.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



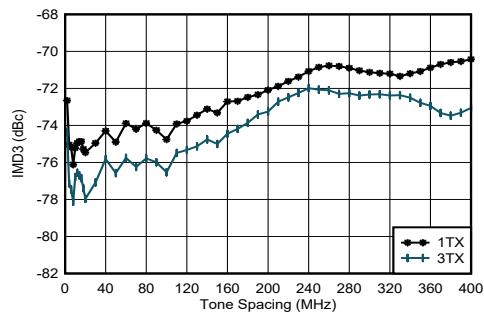
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, $P_{\text{OUT}} = -13$ dBFS

图 5-62. TX Output Noise vs Channel and Attenuation at 1.8 GHz



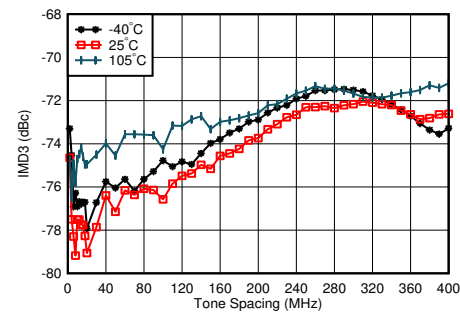
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone

图 5-63. TX IMD3 vs DSA Setting at 1.8 GHz



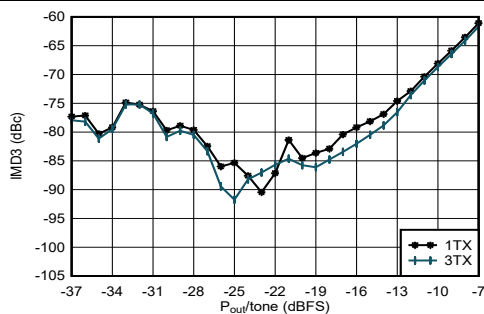
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone

图 5-64. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz



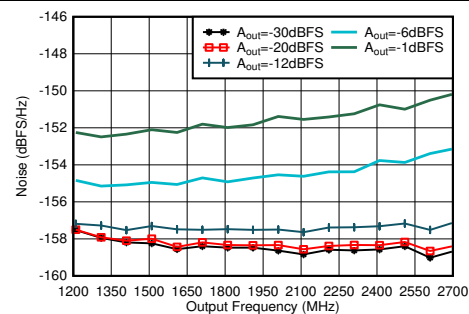
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone, worst channel

图 5-65. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, $f_{\text{SPACING}} = 20$ MHz, matching at 1.8 GHz

图 5-66. TX IMD3 vs Digital Level at 1.8 GHz

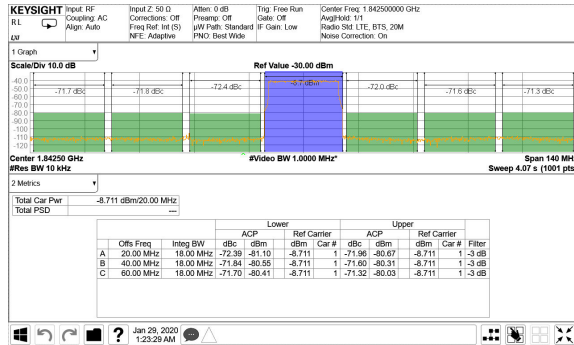


Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, 40-MHz offset

图 5-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz

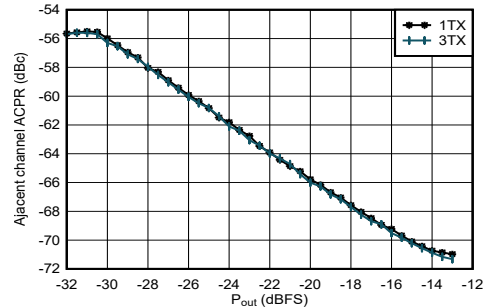
5.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



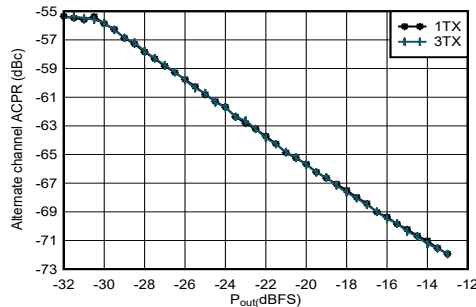
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

FIG 5-68. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



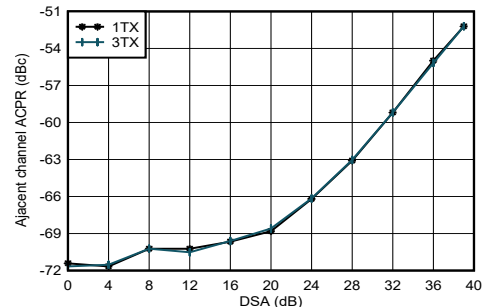
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-69. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



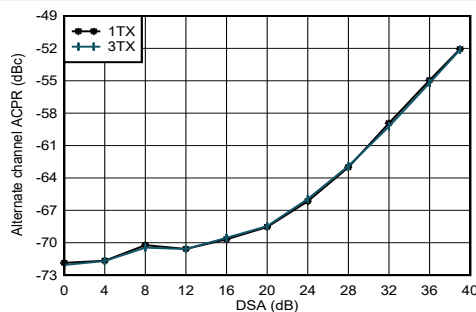
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-70. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



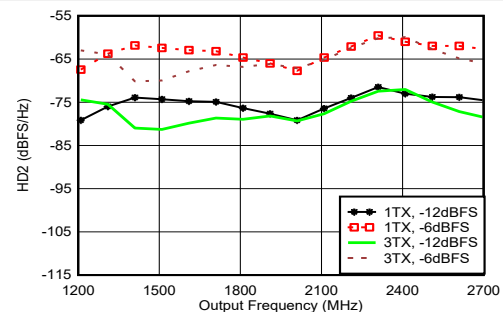
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-71. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-72. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz

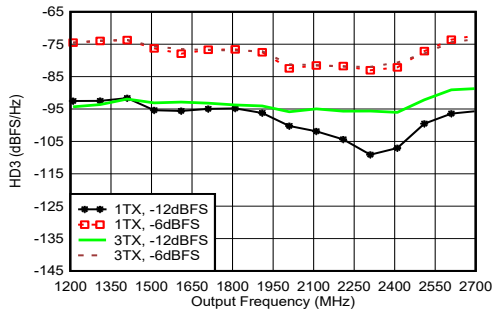


Matching at 1.8 GHz, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz

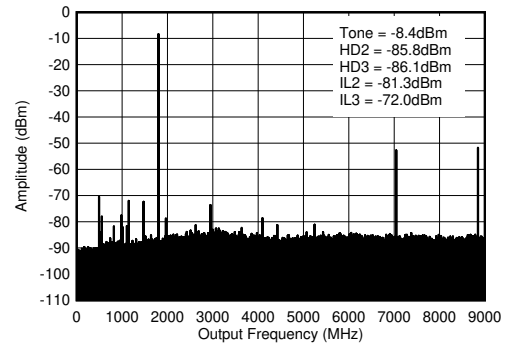
5.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



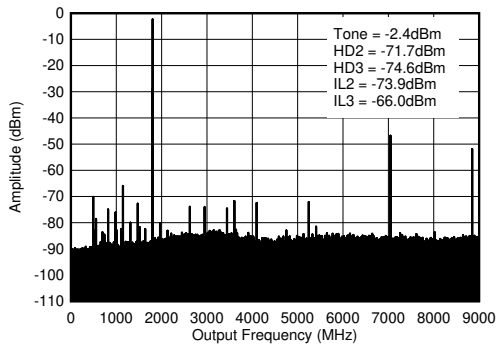
Matching at 1.8 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



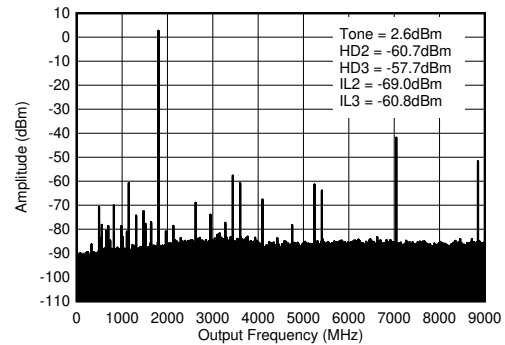
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

FIG 5-75. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

FIG 5-76. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

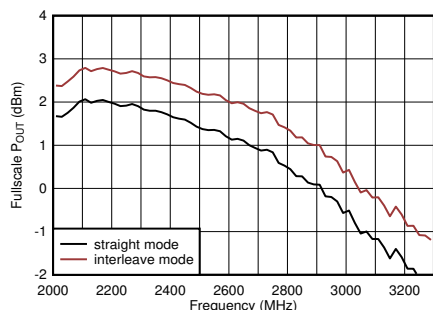


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

FIG 5-77. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

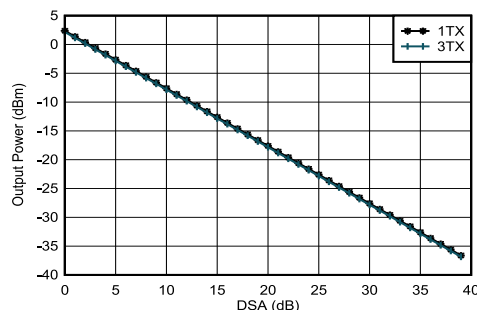
5.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



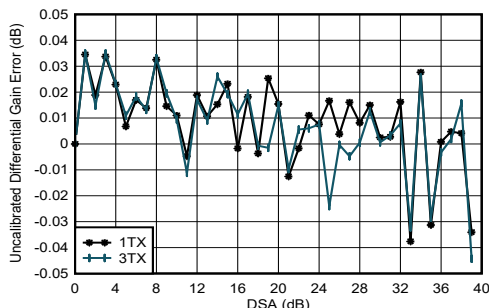
Including PCB and cable losses, $A_{\text{OUT}} = -0.5$ dBFS, DSA = 0, 2.6 GHz matching

FIG 5-78. TX Full Scale vs RF Frequency at 11796.48 MSPS



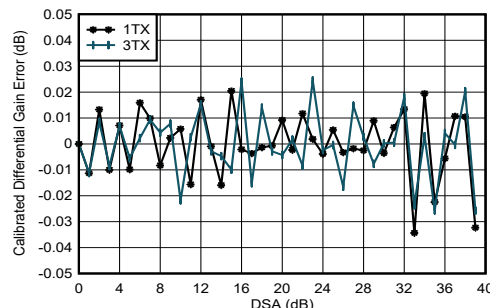
$f_{\text{DAC}} = 8847.36$ MSPS, $A_{\text{OUT}} = -0.5$ dBFS, matching 2.6 GHz

FIG 5-79. TX Output Power vs DSA Setting and Channel at 2.6 GHz



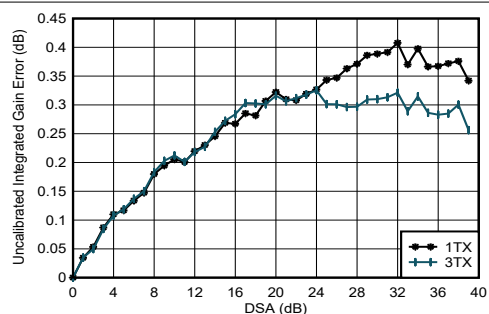
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



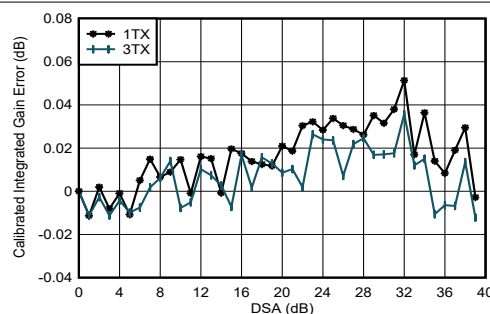
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-82. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

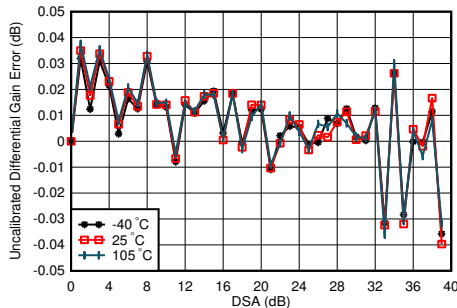


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-83. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

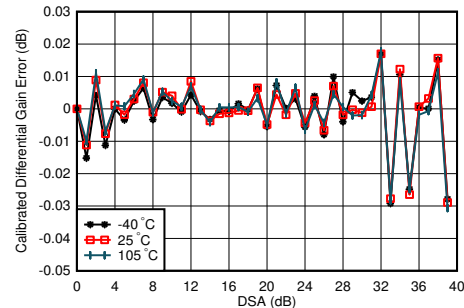
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



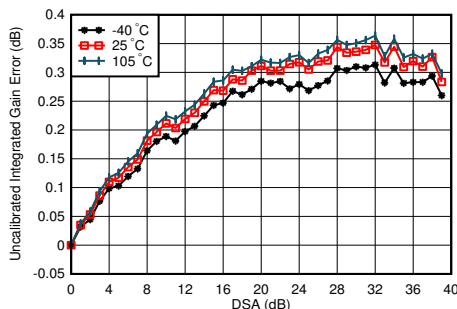
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-84. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



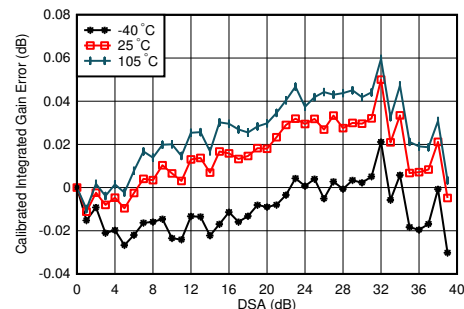
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-85. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



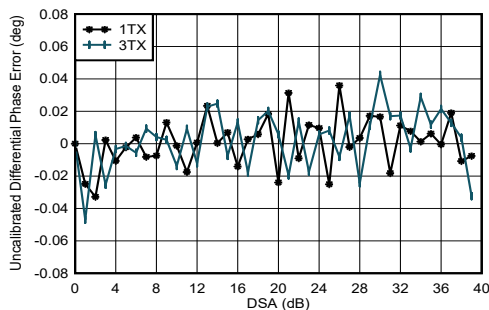
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



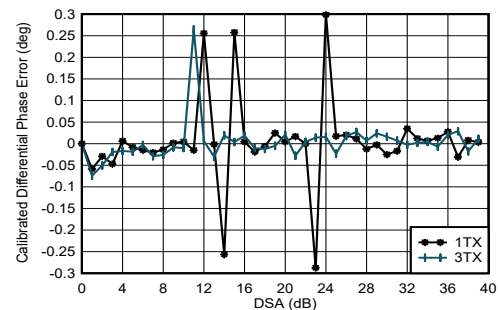
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

FIG 5-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz

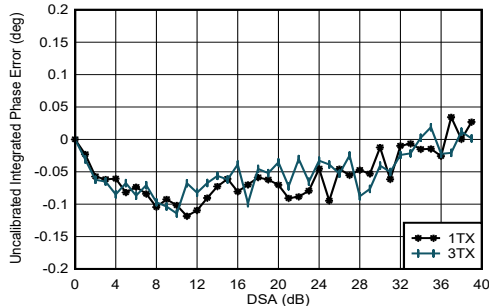


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

FIG 5-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz

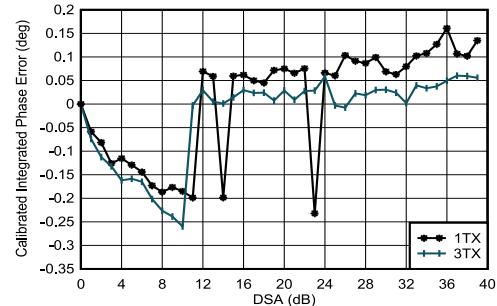
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



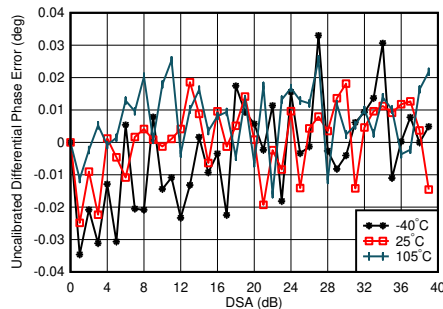
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-90. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



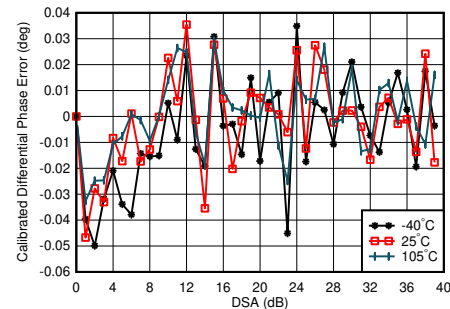
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-91. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



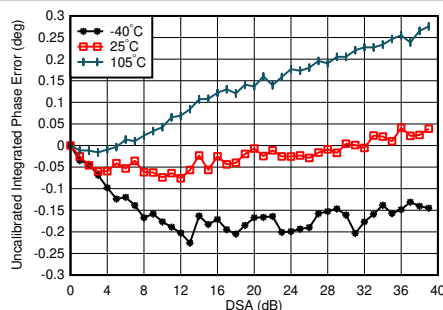
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

FIG 5-92. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



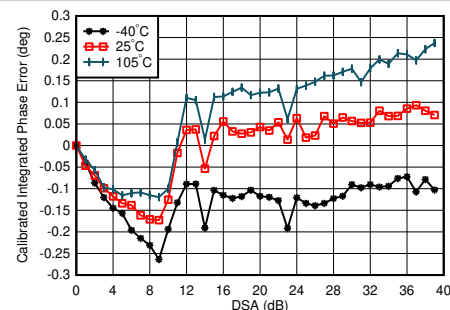
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

FIG 5-93. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz

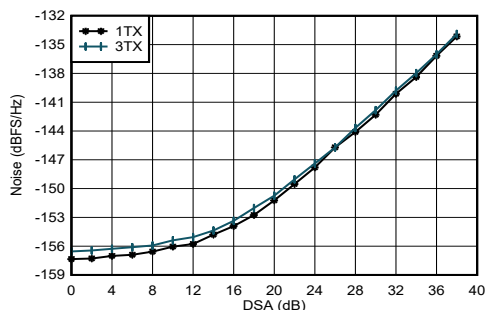


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz

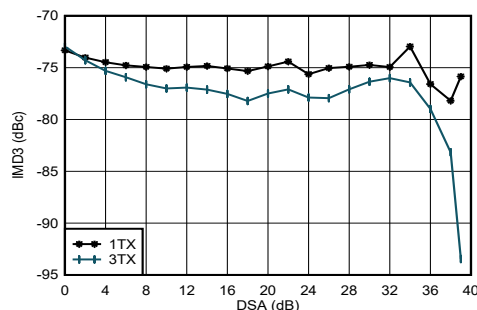
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



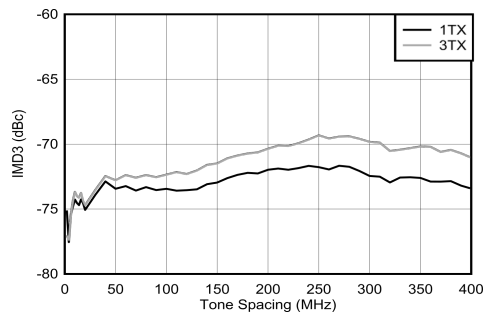
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz,
 $P_{\text{OUT}} = -13$ dBFS

FIG 5-96. TX Output Noise vs Channel and Attenuation at 2.6 GHz



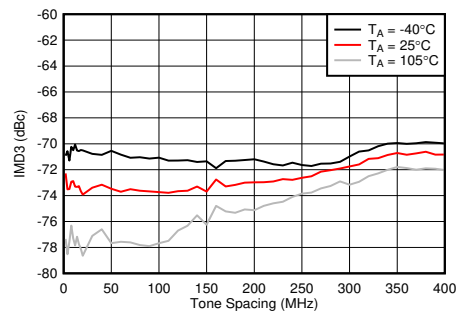
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz,
 matching at 2.6 GHz, -13 dBFS each tone

FIG 5-97. TX IMD3 vs DSA Setting at 2.6 GHz



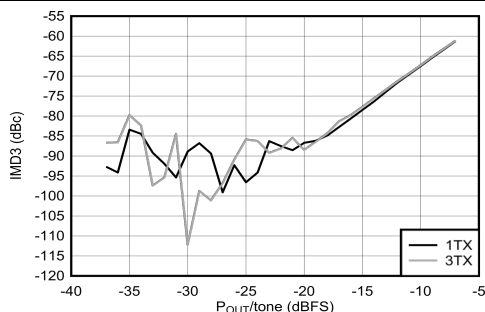
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz,
 matching at 2.6 GHz, -13 dBFS each tone

FIG 5-98. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



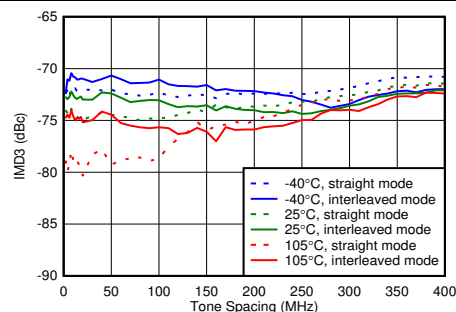
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz,
 matching at 2.6 GHz, -13 dBFS each tone, worst channel.

FIG 5-99. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 2.6 GHz

FIG 5-100. TX IMD3 vs Digital Level at 2.6 GHz

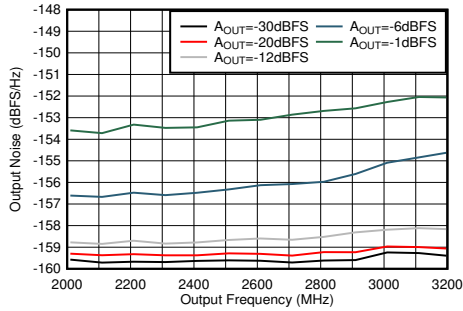


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz,
 matching at 2.6 GHz, -13 dBFS each tone

FIG 5-101. TX IMD3 vs Tone Spacing and Temperature

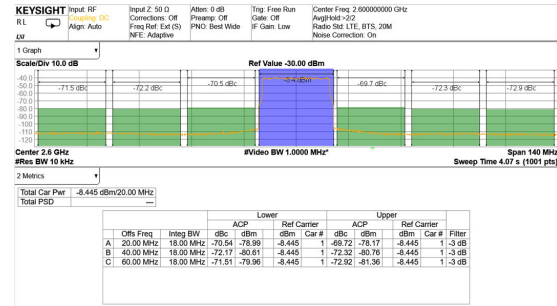
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



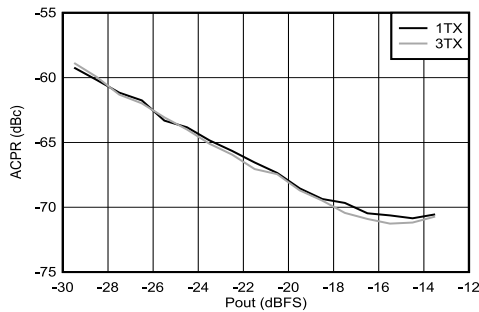
Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, 40-MHz offset

FIG 5-102. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz



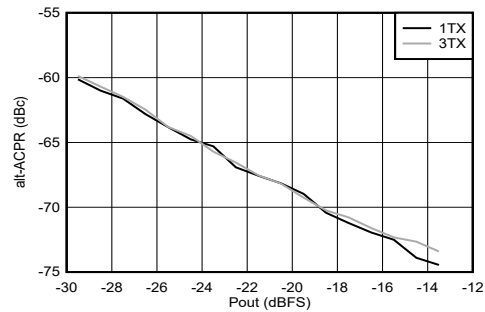
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

FIG 5-103. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)



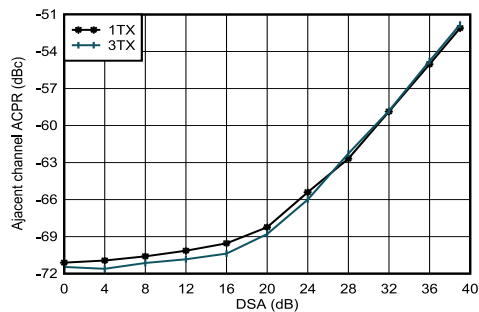
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



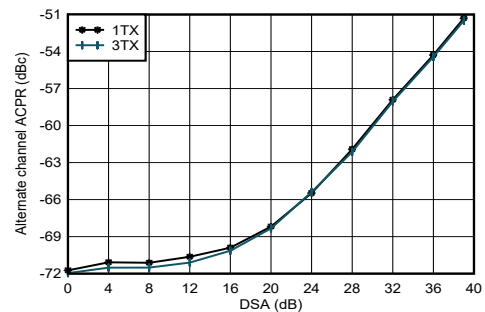
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

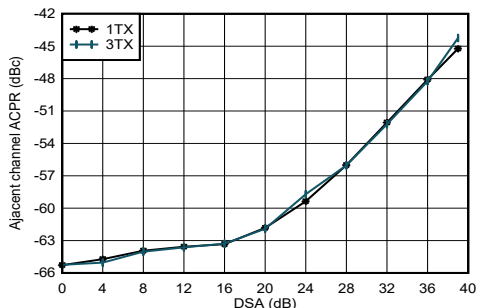


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

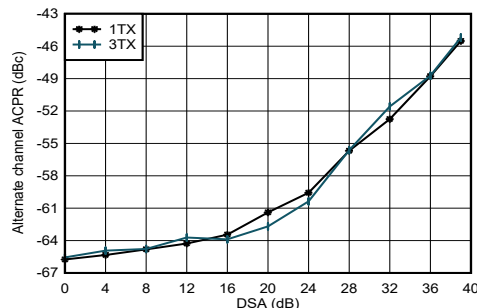
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



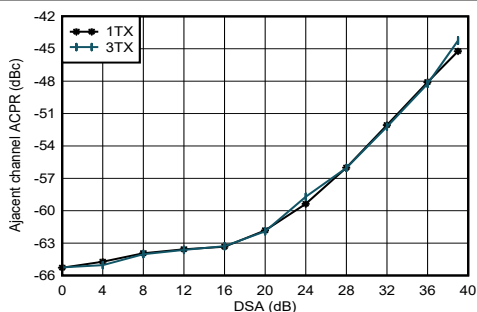
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-108. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



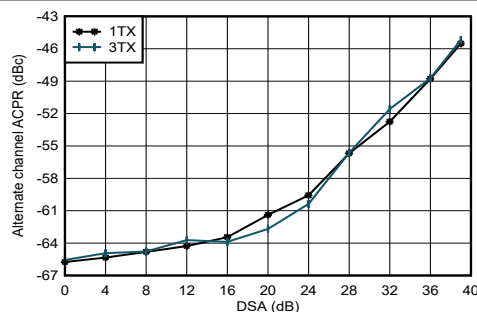
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



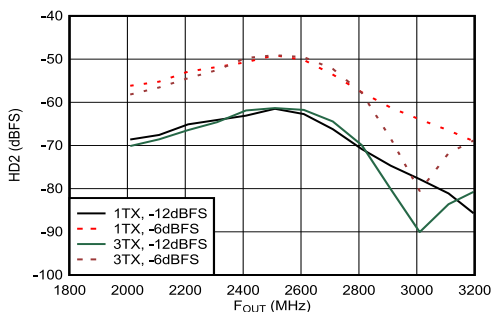
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

FIG 5-110. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



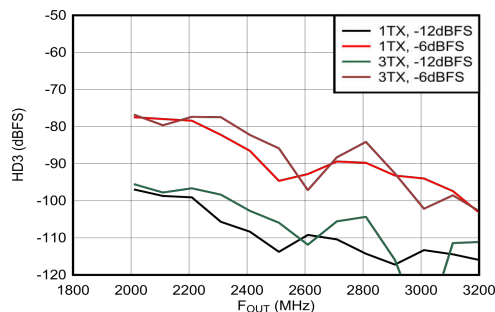
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

FIG 5-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz

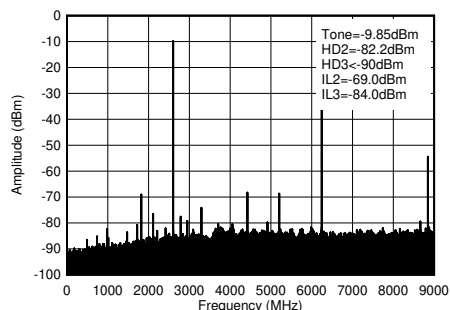


Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

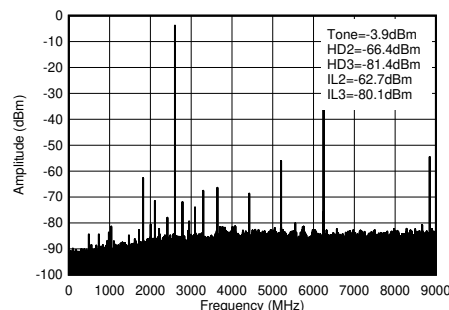
5.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



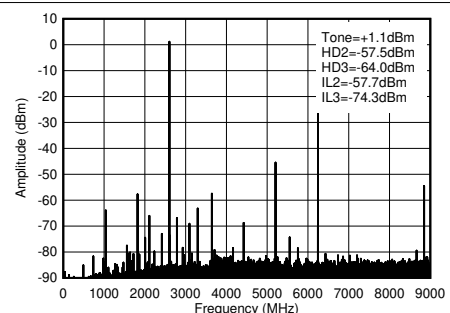
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 5-114. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



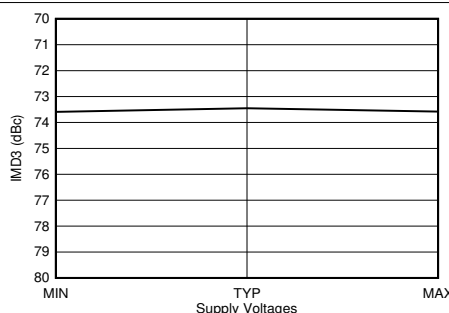
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 5-115. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 5-116. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)

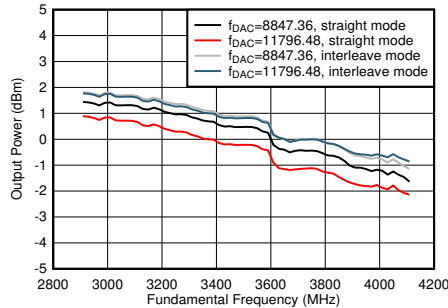


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 5-117. TX IMD3 vs Supply Voltage at 2.6 GHz

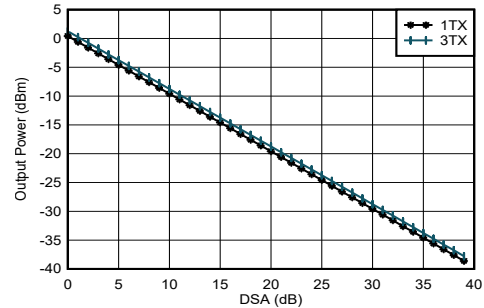
5.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



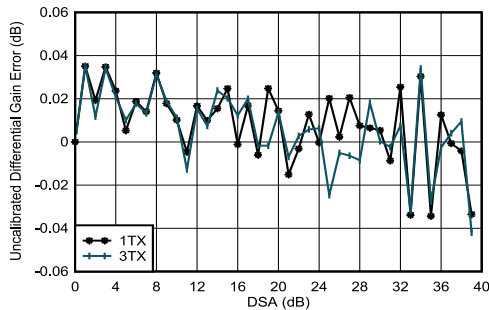
$A_{\text{out}} = -0.5\text{dBFS}$, 3.5 GHz Matching, included PCB and cable losses

FIG 5-118. TX Output Power vs Frequency



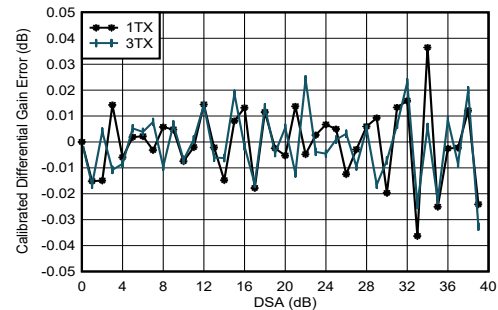
$A_{\text{out}} = -0.5$ dBFS, 3.5 GHz Matching, included PCB and cable losses

FIG 5-119. TX Output Power vs DSA Setting at 3.5 GHz



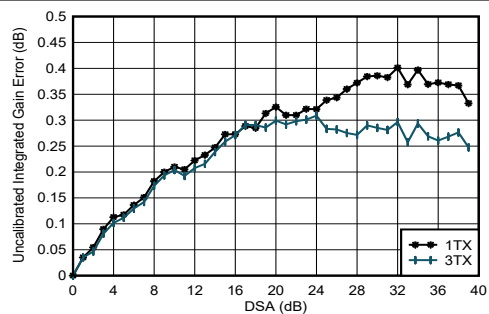
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



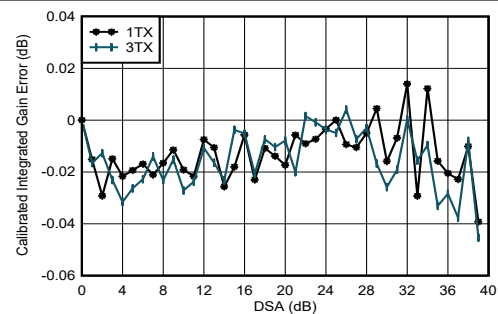
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

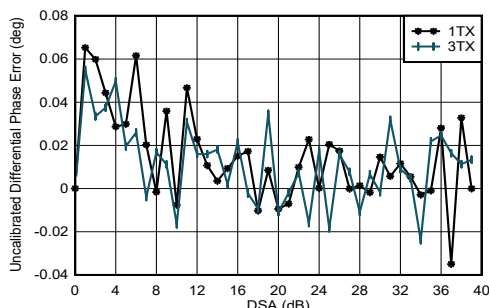


3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

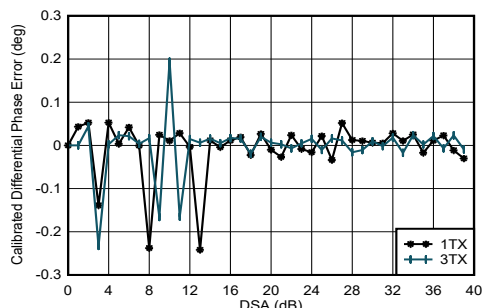
5.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



3.5 GHz Matching, included PCB and cable losses

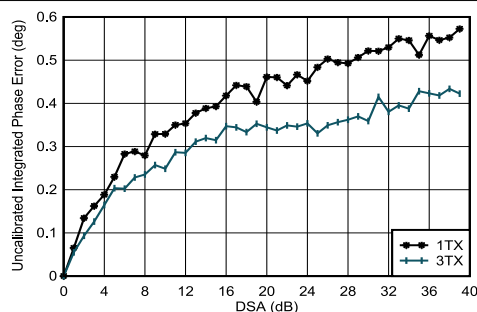
FIG 5-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses

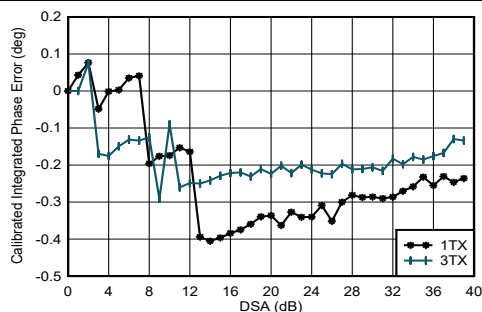
Phase DNL spike may occur at any DSA setting.

FIG 5-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



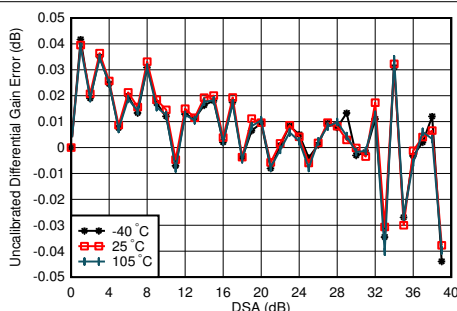
3.5 GHz Matching, included PCB and cable losses

FIG 5-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



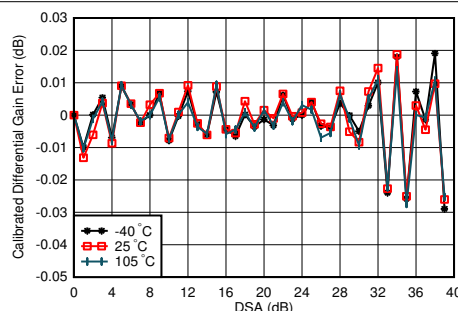
3.5 GHz Matching, included PCB and cable losses

FIG 5-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 1TX

FIG 5-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

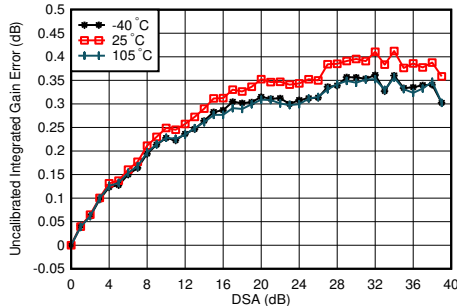


3.5 GHz Matching, 1TX, Calibrated at 25°C

FIG 5-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

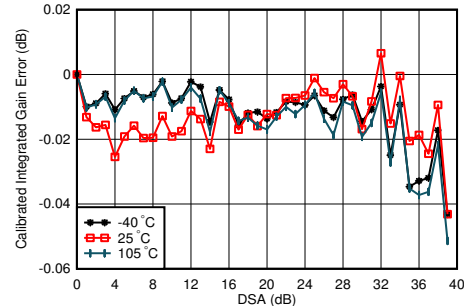
5.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



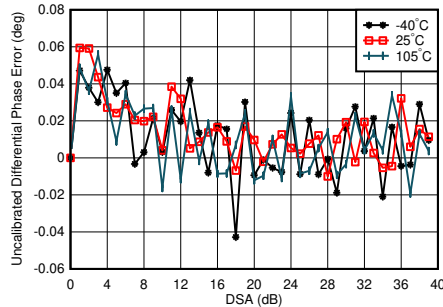
3.5 GHz Matching, 1TX

FIG 5-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

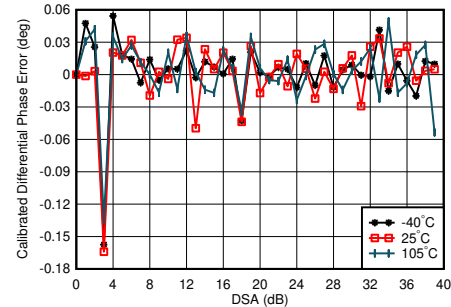
FIG 5-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

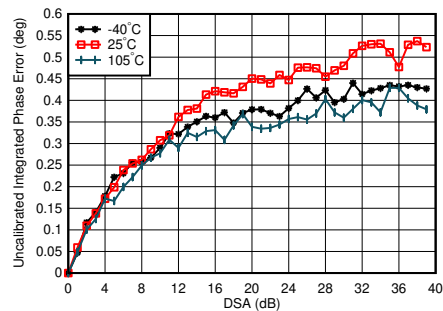
FIG 5-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

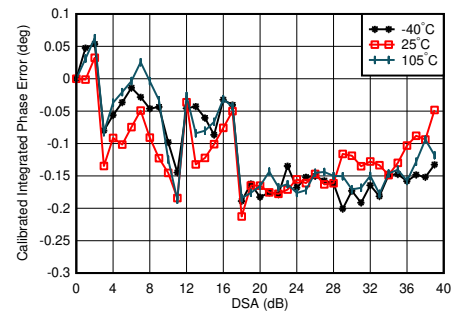
FIG 5-133. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting}=0)$

FIG 5-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



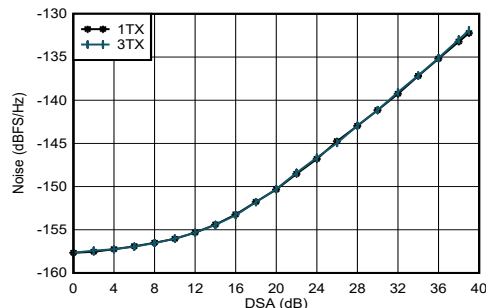
3.5 GHz Matching, 1TX, Calibrated at 25°C

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting}=0)$

FIG 5-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz

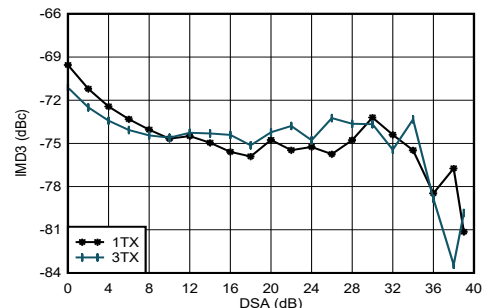
5.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



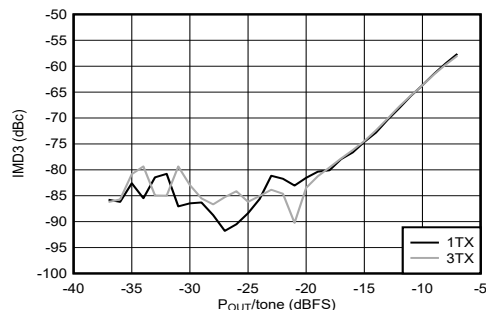
A. $f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 3.5 GHz, $A_{\text{out}} = -13$ dBFS.

FIG 5-136. TX NSD vs DSA Setting at 3.5 GHz



20-MHz tone spacing, 3.5 GHz Matching, -13 dBFS each tone, included PCB and cable losses

FIG 5-137. TX IMD3 vs DSA Setting at 3.5 GHz



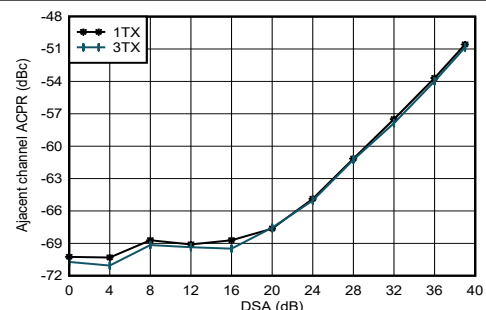
20-MHz tone spacing, 3.5 GHz Matching

FIG 5-138. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



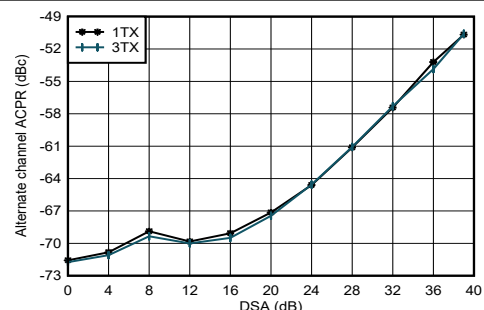
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

FIG 5-139. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

FIG 5-140. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

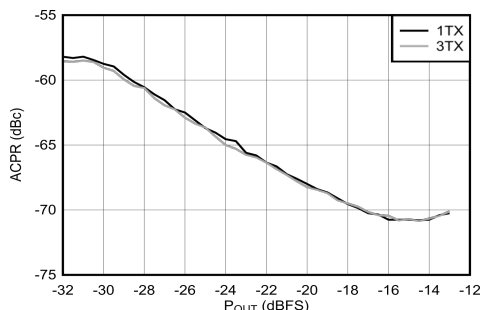


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

FIG 5-141. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz

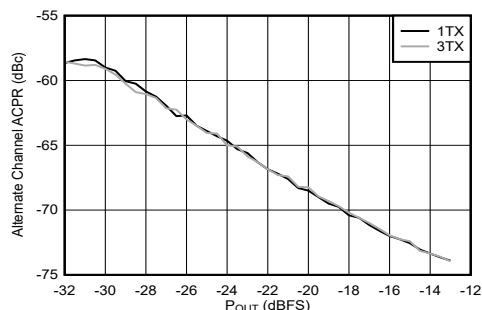
5.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated



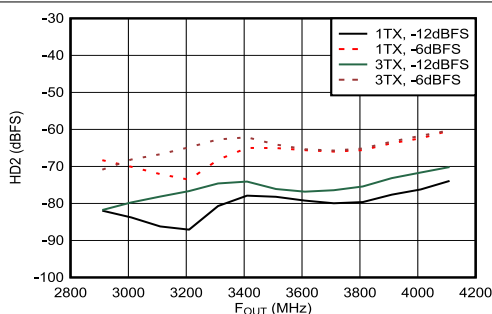
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

FIG 5-142. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



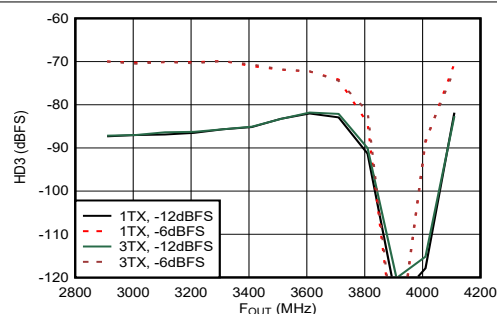
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

FIG 5-143. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



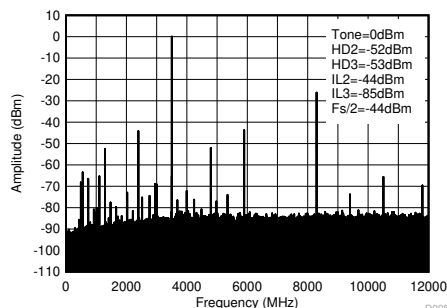
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



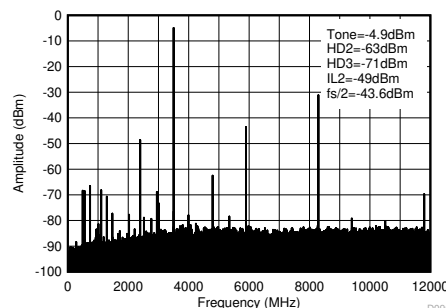
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

FIG 5-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

FIG 5-146. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

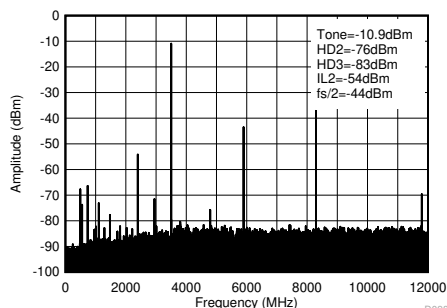


Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

FIG 5-147. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

5.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated

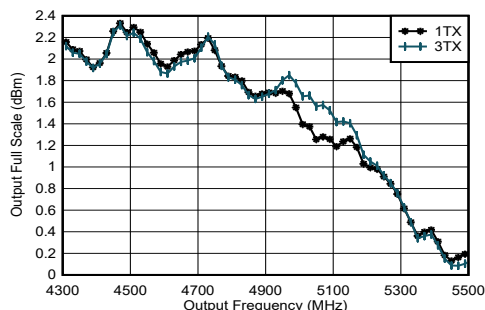


Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

✎ 5-148. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0- f_{DAC})

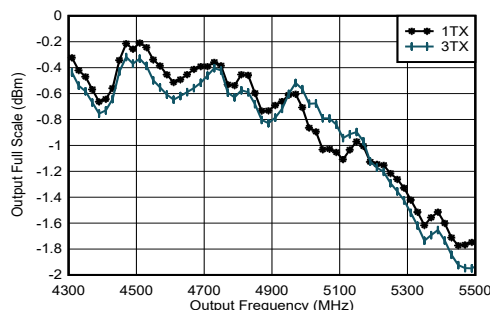
5.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



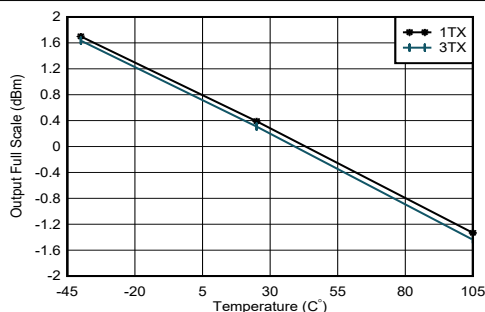
Excluding PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 4.9 GHz matching

FIG 5-149. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS



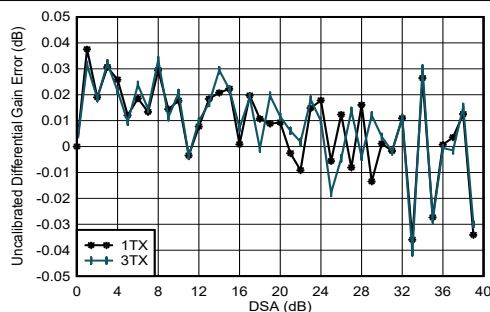
Excluding PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 4.9 GHz matching

FIG 5-150. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode, 2nd Nyquist Zone



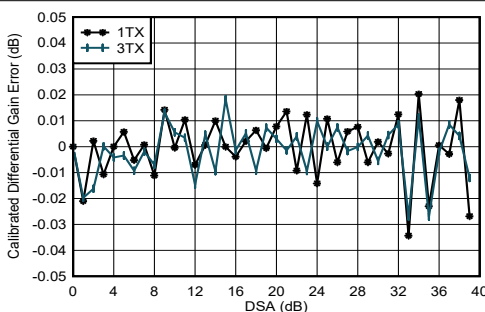
$f_{\text{DAC}} = 11796.48$ MSPS, $A_{\text{out}} = -0.5$ dBFS, matching 4.9 GHz

FIG 5-151. TX Output Power vs DSA Setting and Channel at 4.9 GHz



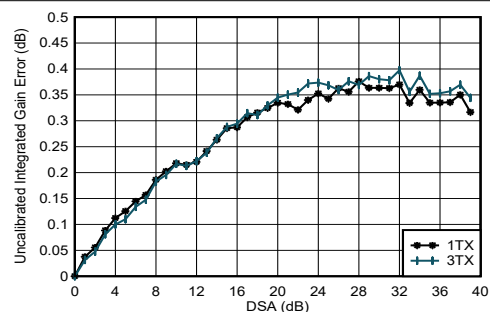
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

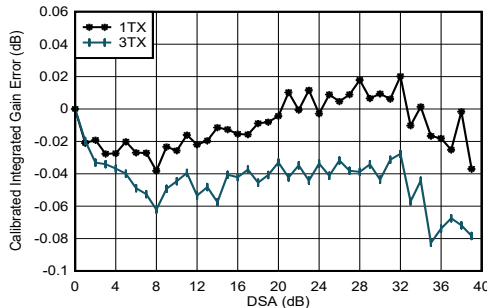


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

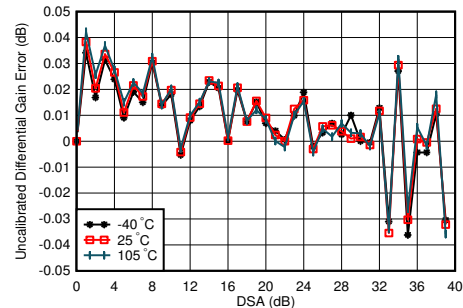
5.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



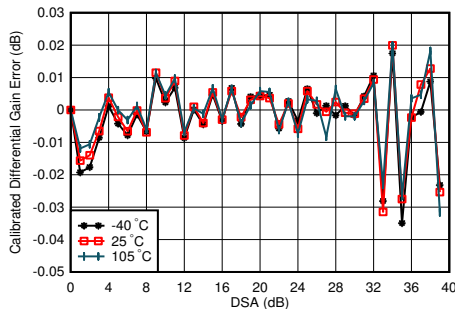
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



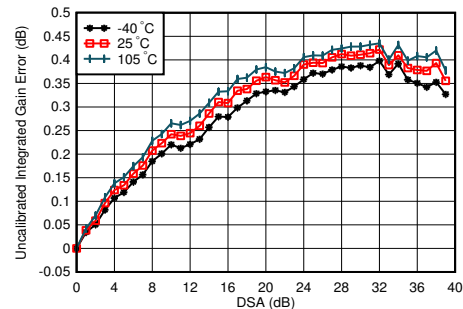
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



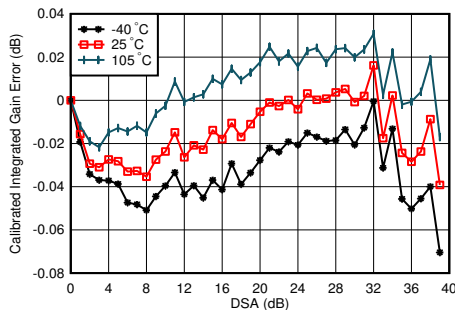
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

FIG 5-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



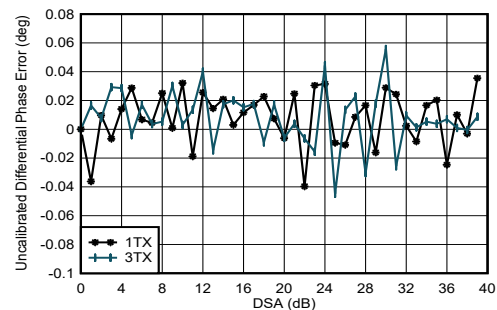
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

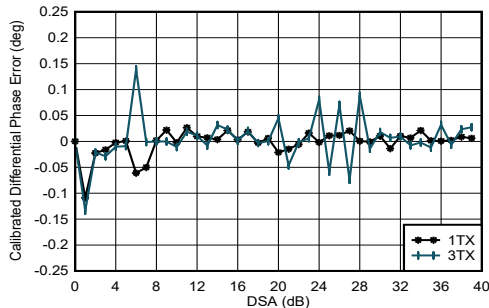


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

FIG 5-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

5.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated

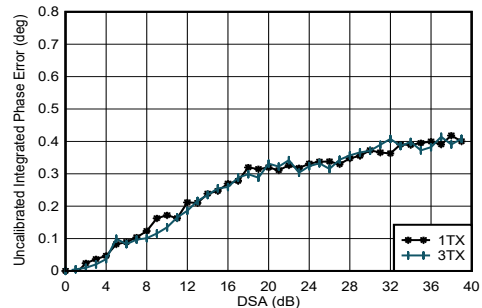


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Phase DNL spike may occur at any DSA setting.

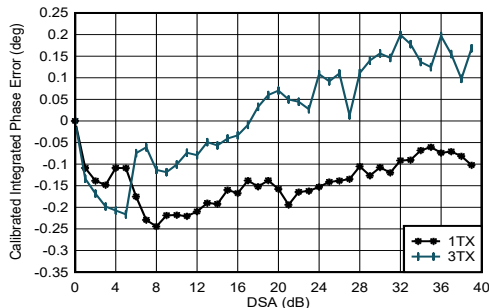
FIG 5-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

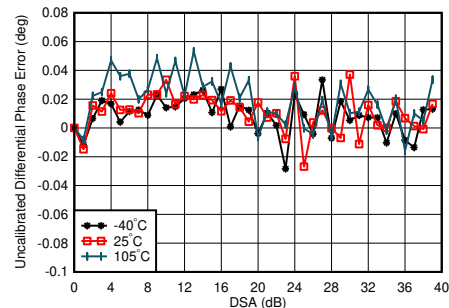
FIG 5-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

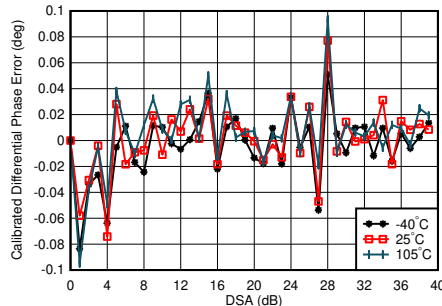
FIG 5-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

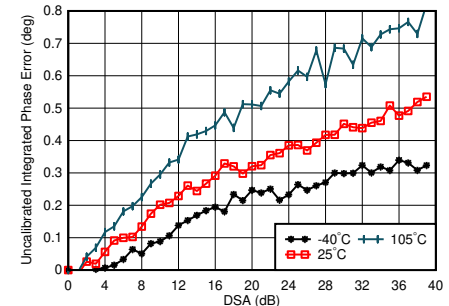
FIG 5-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

FIG 5-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



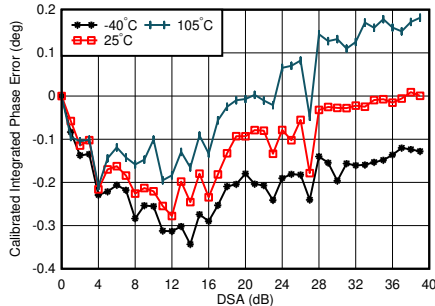
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

FIG 5-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

5.12.5 TX Typical Characteristics at 4.9 GHz (continued)

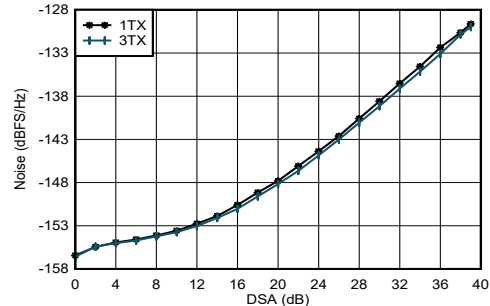
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at 25°C

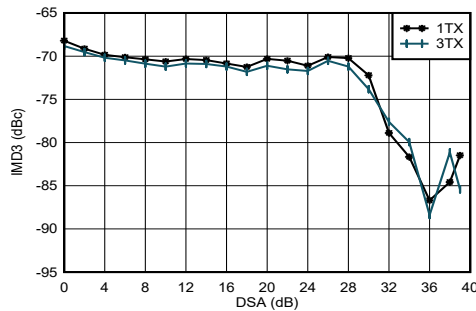
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



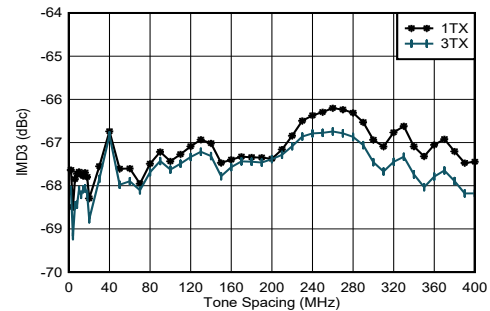
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $P_{\text{OUT}} = -13$ dBFS

FIG 5-168. TX Output Noise vs Channel and Attenuation at 2.6 GHz



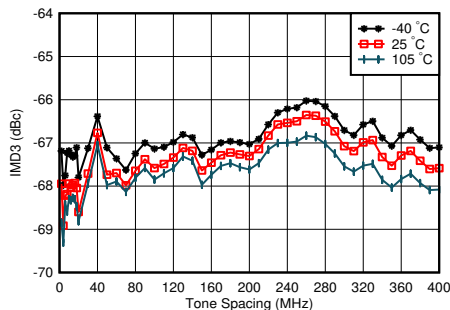
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone

FIG 5-169. TX IMD3 vs DSA Setting at 4.9 GHz



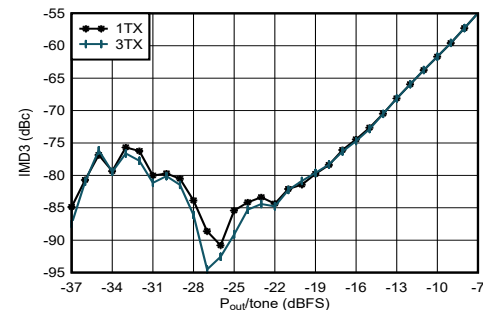
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone

FIG 5-170. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone, worst channel

FIG 5-171. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

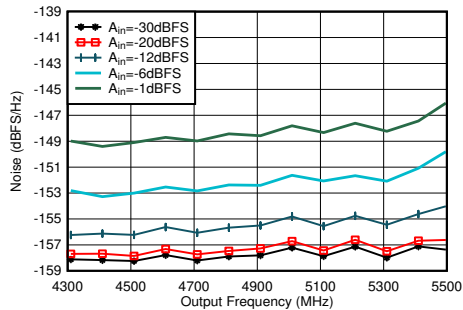


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, $f_{\text{SPACING}} = 20\text{MHz}$

FIG 5-172. TX IMD3 vs Digital Level at 4.9 GHz

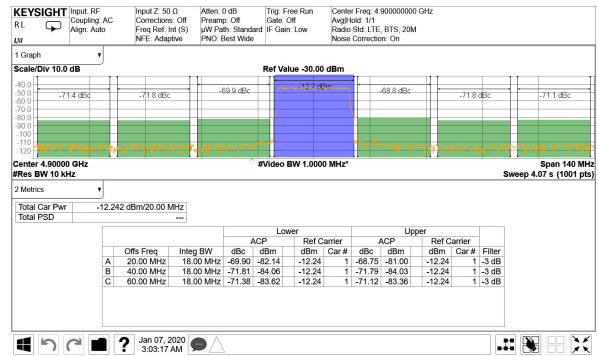
5.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



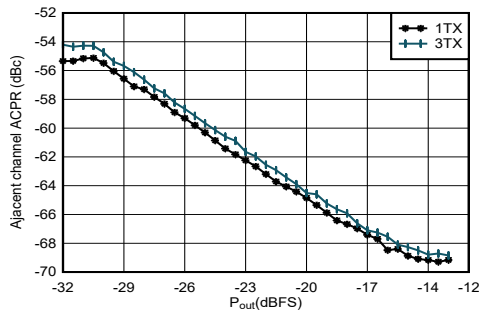
Matching at 4.9 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSps, interleave mode, 40-MHz offset, DSA=0dB

FIG 5-173. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz



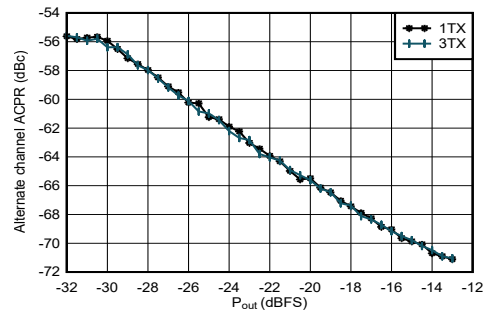
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

FIG 5-174. TX 20-MHz LTE Output Spectrum at 4.9 GHz



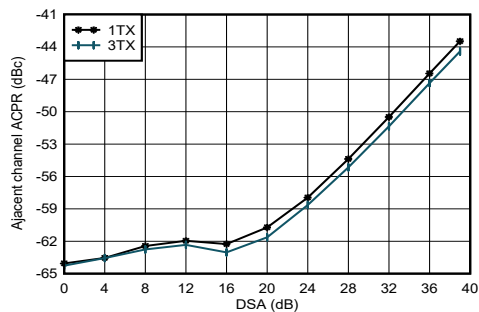
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-175. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



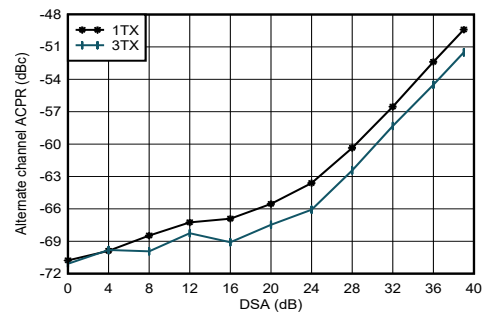
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-176. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-177. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

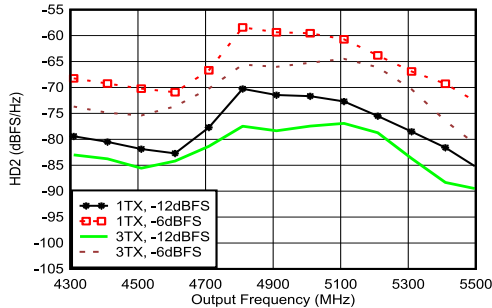


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

FIG 5-178. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz

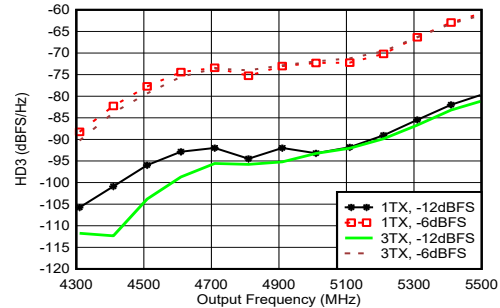
5.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated



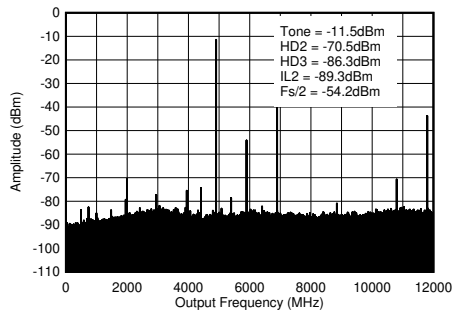
Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



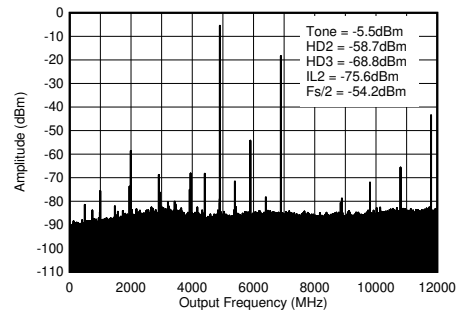
Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

FIG 5-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz



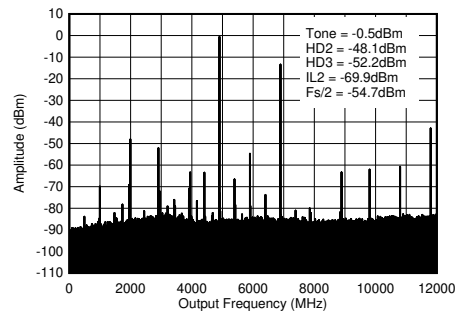
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

FIG 5-181. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

FIG 5-182. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)

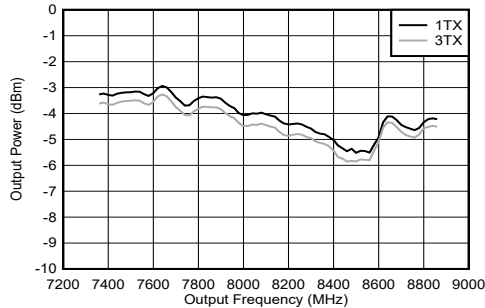


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

FIG 5-183. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)

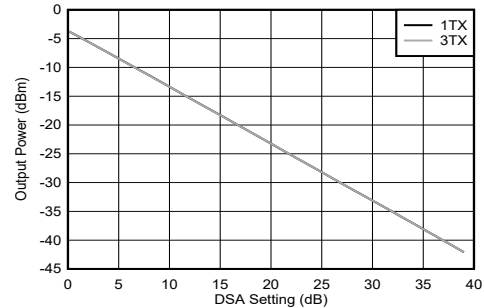
5.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



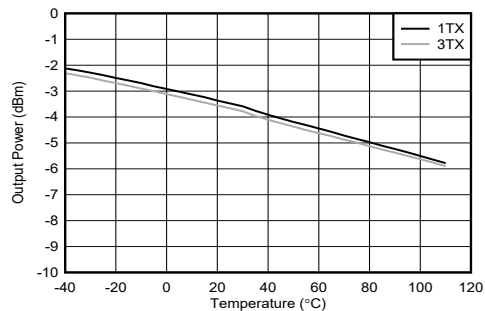
includes PCB and cable losses.

FIG 5-184. TX Output Power vs Frequency at 8.1 GHz



includes PCB and cable losses.

FIG 5-185. TX Output Power vs DSA Setting at 8.1 GHz



includes PCB and cable losses.

FIG 5-186. TX Output Power vs Temperature at 8.1 GHz

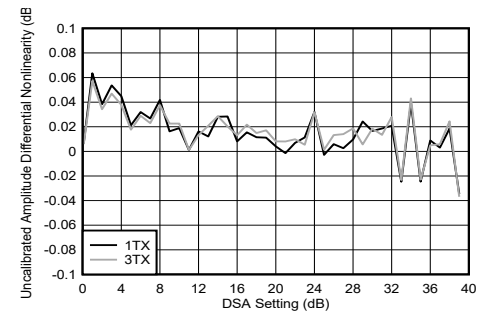


FIG 5-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.1 GHz

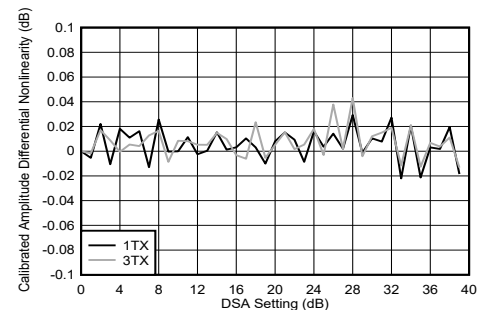


FIG 5-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.1 GHz

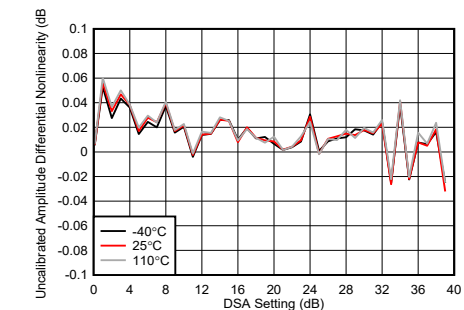


FIG 5-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.1 GHz

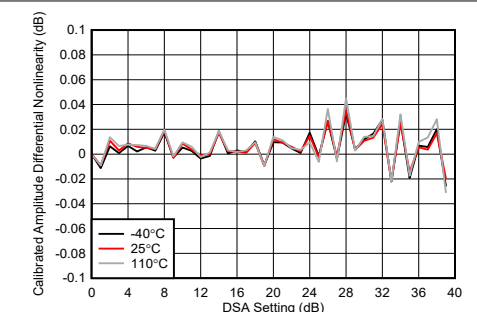


FIG 5-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.1 GHz

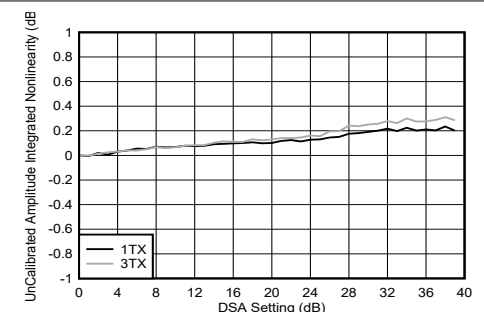


FIG 5-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.1 GHz

5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

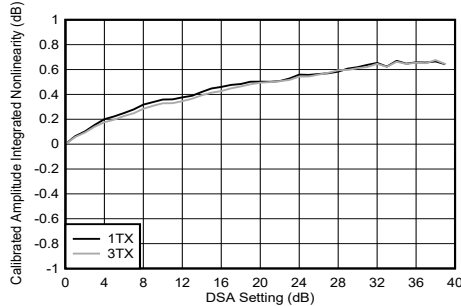


FIG 5-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

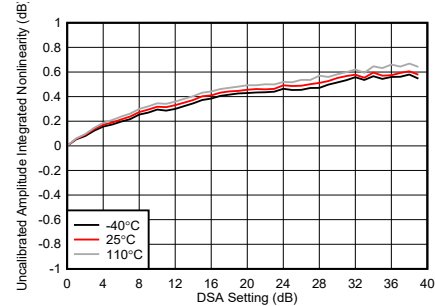


FIG 5-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

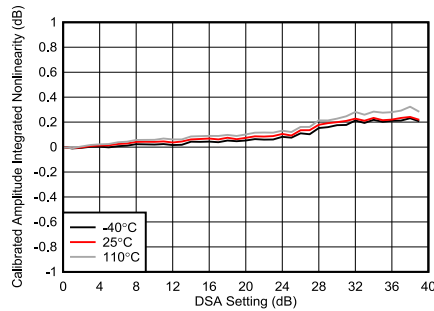


FIG 5-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

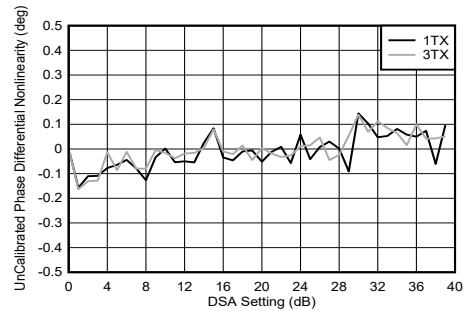


FIG 5-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

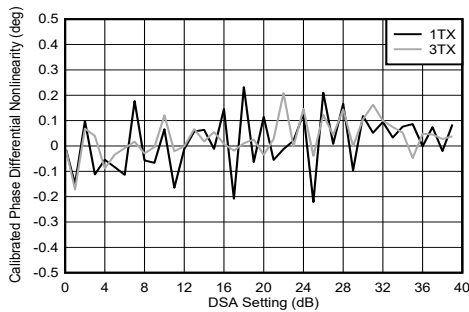


FIG 5-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

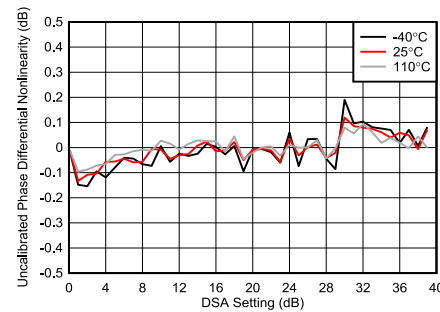


FIG 5-197. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

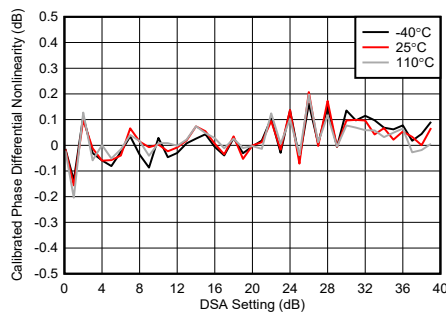


FIG 5-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

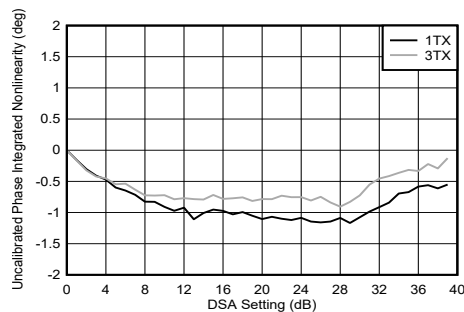


FIG 5-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

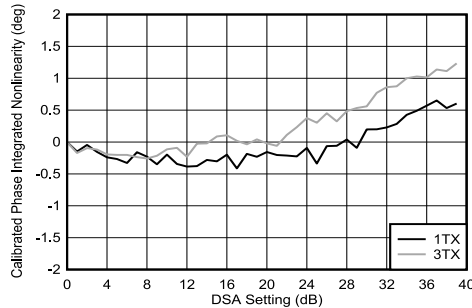


图 5-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.1 GHz

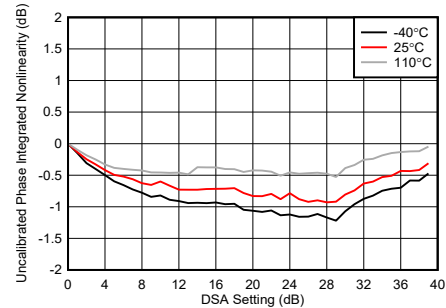


图 5-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.1 GHz

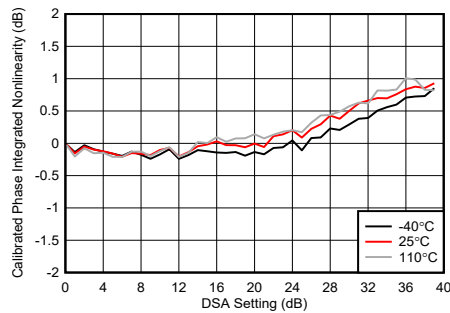
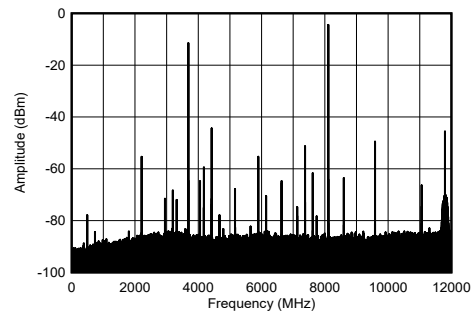
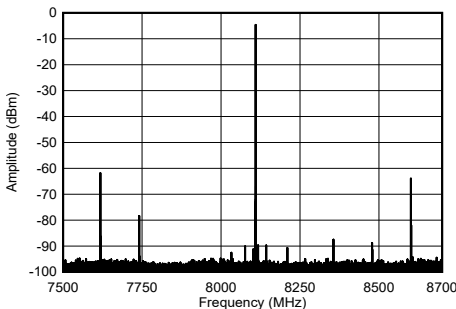


图 5-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.1 GHz



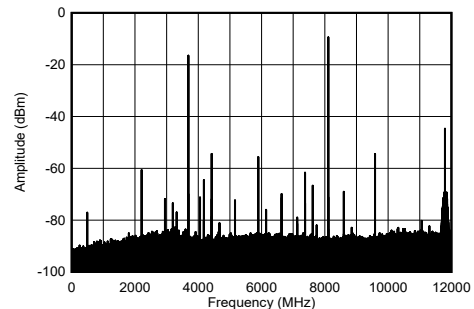
-1 dBFS

图 5-203. TX Single Tone Output Spectrum at 8.1 GHz



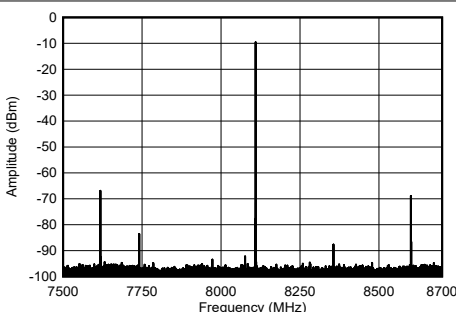
-1 dBFS

图 5-204. TX Single Tone Output Spectrum at 8.1 GHz



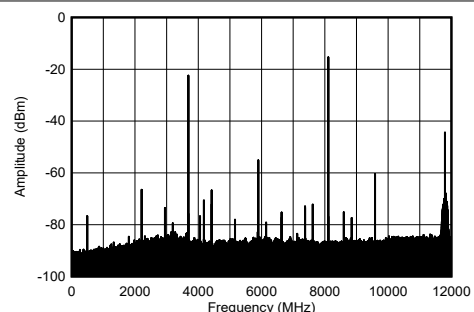
-6 dBFS

图 5-205. TX Single Tone Output Spectrum at 8.1 GHz



-6 dBFS

图 5-206. TX Single Tone Output Spectrum at 8.1 GHz

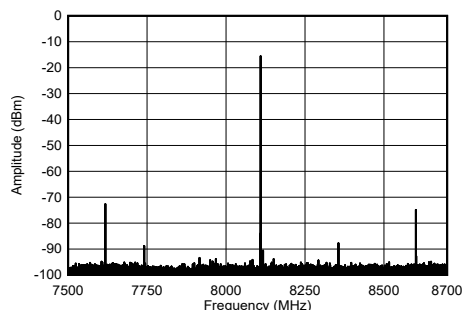


-12 dBFS

图 5-207. TX Single Tone Output Spectrum at 8.1 GHz

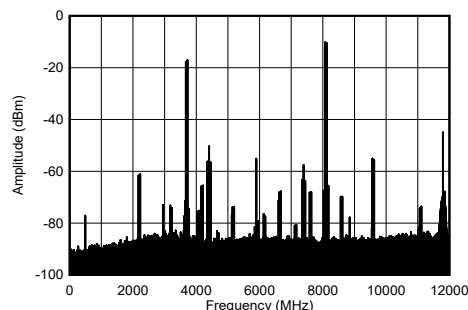
5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



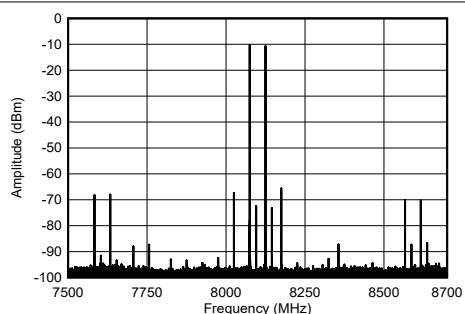
-12 dBFS

FIG 5-208. TX Single Tone Output Spectrum at 8.11 GHz



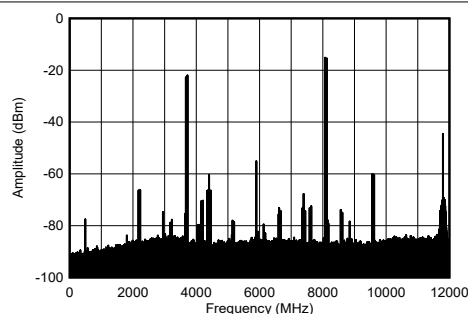
50 MHz tone spacing, -7 dBFS each tone

FIG 5-209. TX Dual Tone Output Spectrum at 8.11 GHz



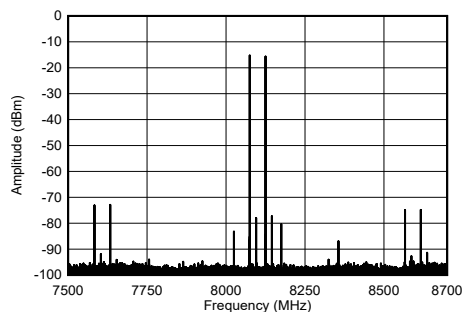
50 MHz tone spacing, -7 dBFS each tone

FIG 5-210. TX Dual Tone Output Spectrum at 8.11 GHz



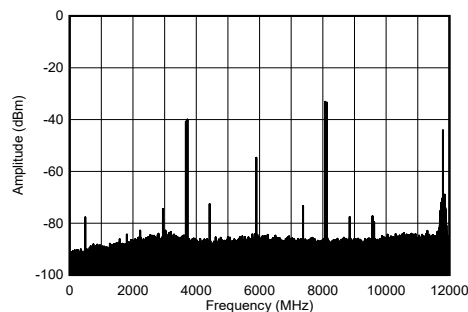
50 MHz tone spacing, -12 dBFS each tone

FIG 5-211. TX Dual Tone Output Spectrum at 8.11 GHz



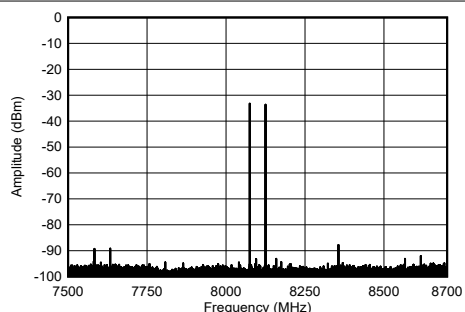
50 MHz tone spacing, -12 dBFS each tone

FIG 5-212. TX Dual Tone Output Spectrum at 8.11 GHz



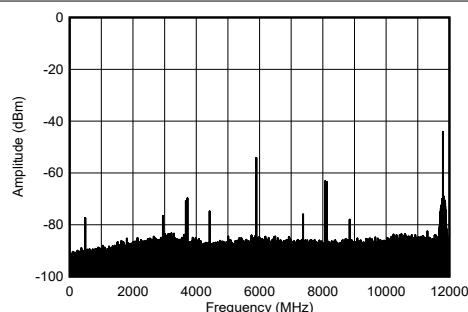
50 MHz tone spacing, -30 dBFS each tone

FIG 5-213. TX Dual Tone Output Spectrum at 8.11 GHz



50 MHz tone spacing, -30 dBFS each tone

FIG 5-214. TX Dual Tone Output Spectrum at 8.11 GHz

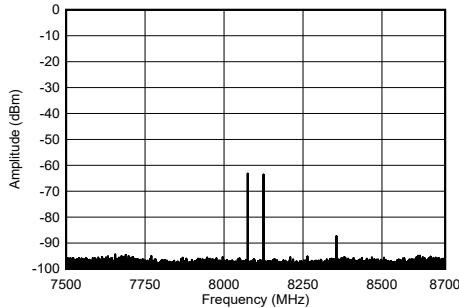


50 MHz tone spacing, -60 dBFS each tone

FIG 5-215. TX Dual Tone Output Spectrum at 8.11 GHz

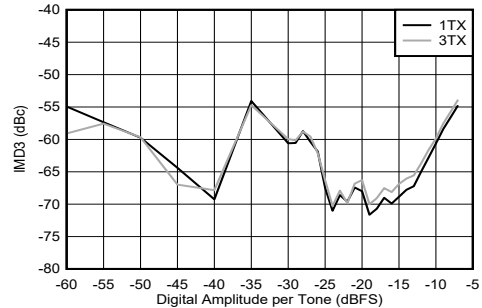
5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



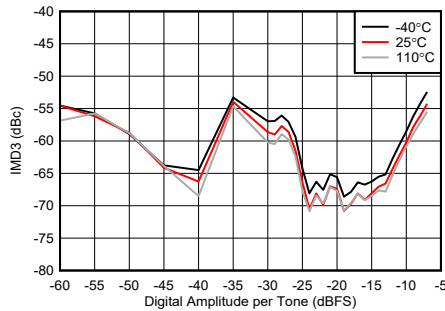
50 MHz tone spacing, -60 dBFS each tone

FIG 5-216. TX Dual Tone Output Spectrum at 8.11 GHz



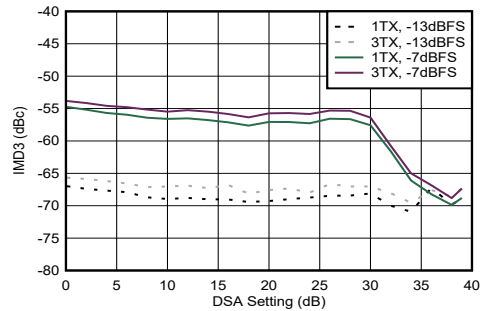
-7 dBFS each tone, 50 MHz tone spacing

FIG 5-217. TX IMD3 vs Digital Amplitude at 8.11 GHz



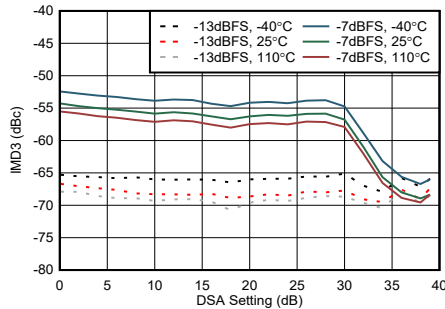
-7 dBFS each tone, 50 MHz tone spacing

FIG 5-218. TX IMD3 vs Digital Amplitude at 8.11 GHz



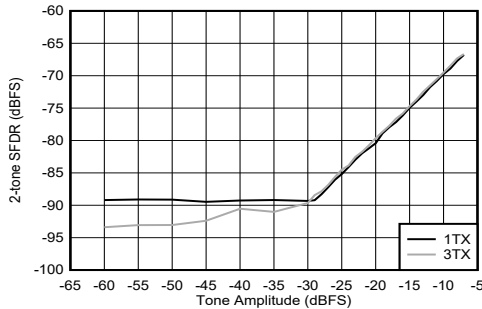
50 MHz tone spacing

FIG 5-219. TX IMD3 vs DSA Setting at 8.11 GHz



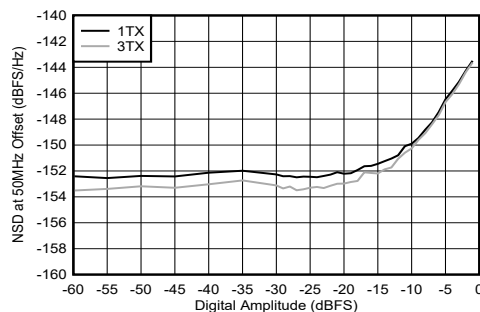
50 MHz tone spacing

FIG 5-220. TX IMD3 vs DSA Setting at 8.11 GHz



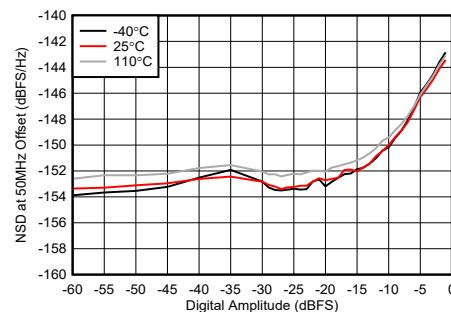
50 MHz tone spacing

FIG 5-221. TX 2-Tone SFDR vs Digital Amplitude at 8.11 GHz



50 MHz offset

FIG 5-222. TX NSD vs Digital Amplitude at 8.11 GHz

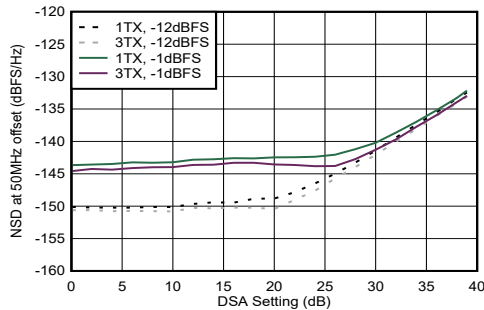


50 MHz offset

FIG 5-223. TX NSD vs Digital Amplitude at 8.11 GHz

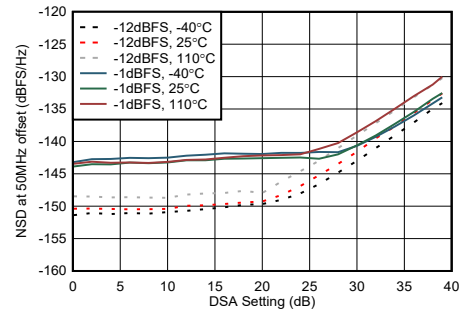
5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching



50 MHz offset

FIG 5-224. TX NSD vs DSA Setting at 8.11 GHz



50 MHz offset

FIG 5-225. TX NSD vs DSA Setting at 8.11 GHz

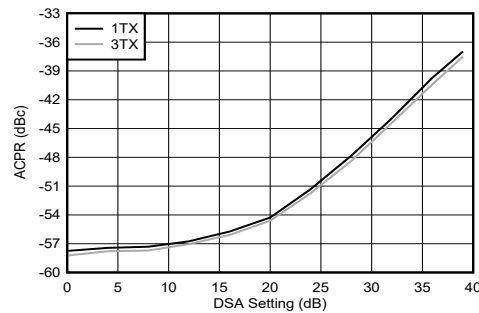


FIG 5-226. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

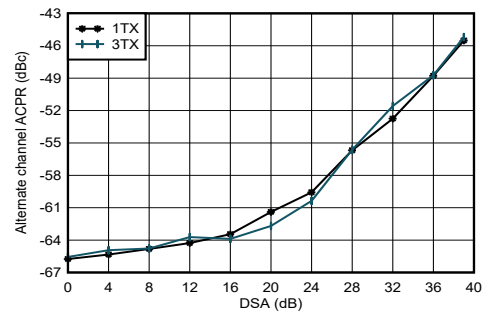


FIG 5-227. TX NR100 MHz alt-ACPR vs DSA Setting 8.11 GHz

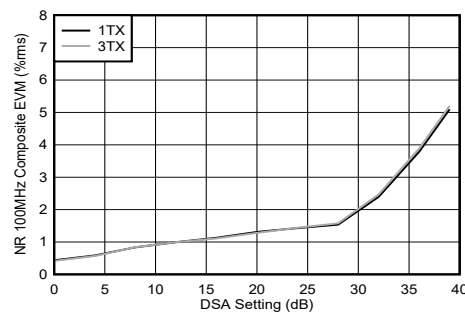


FIG 5-228. TX NR100 MHz EVM vs DSA Setting 8.11 GHz

5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

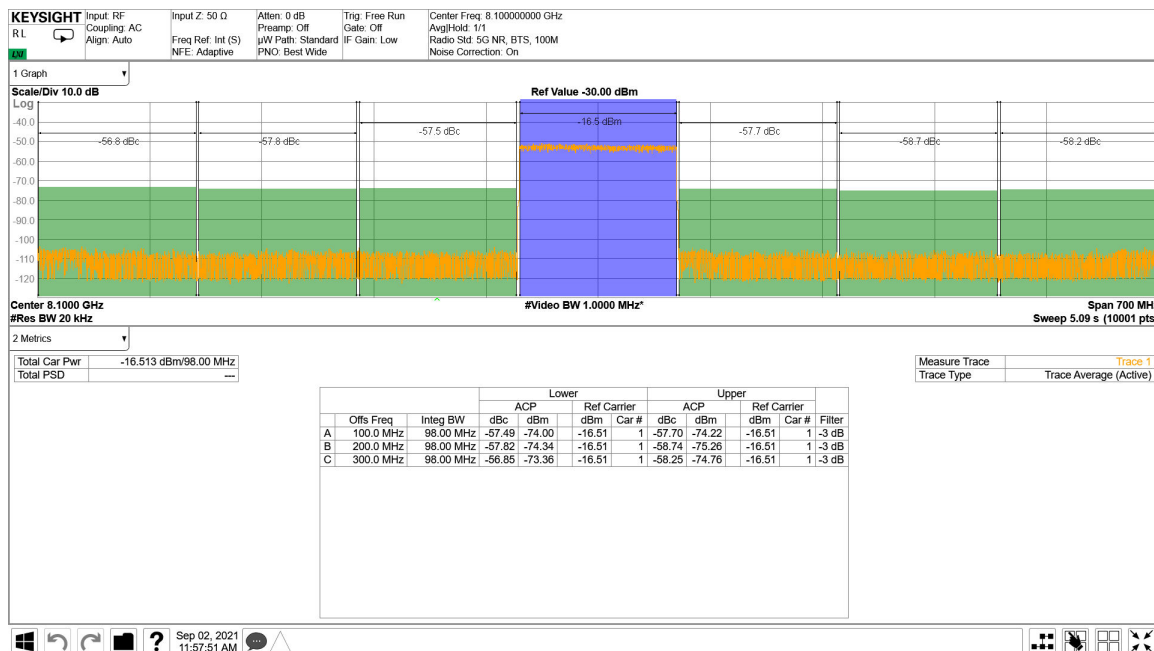


图 5-229. TX 100 MHz NR Output Spectrum at 8.11 GHz

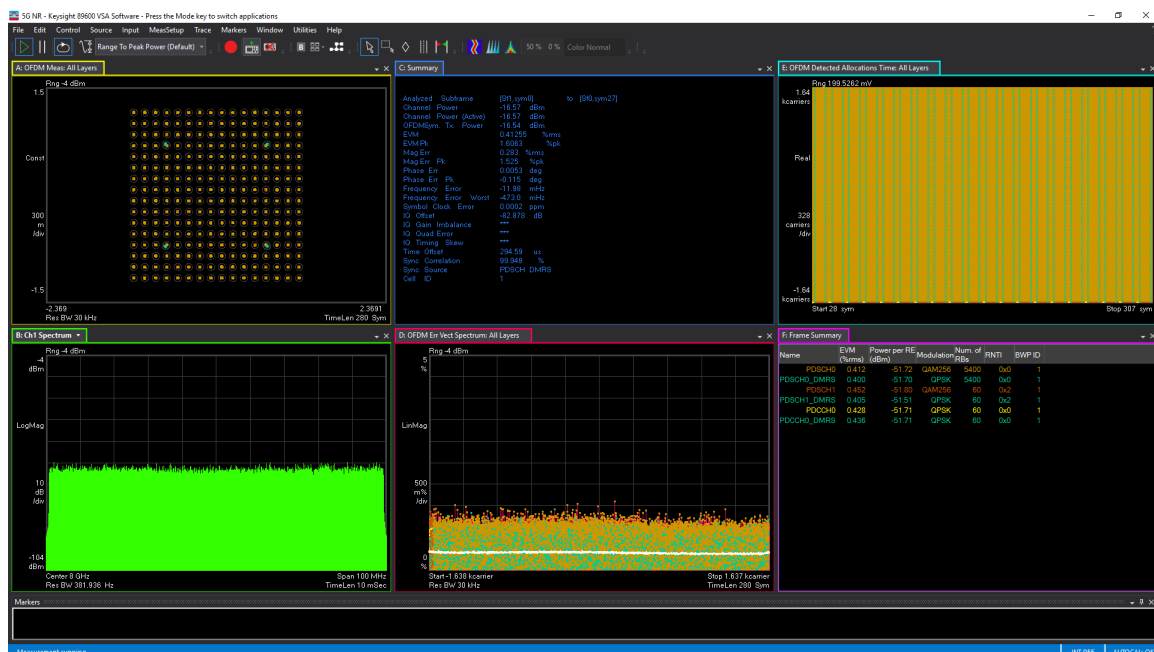


图 5-230. TX 100 MHz NR EVM at 8.11 GHz

5.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1 GHz matching

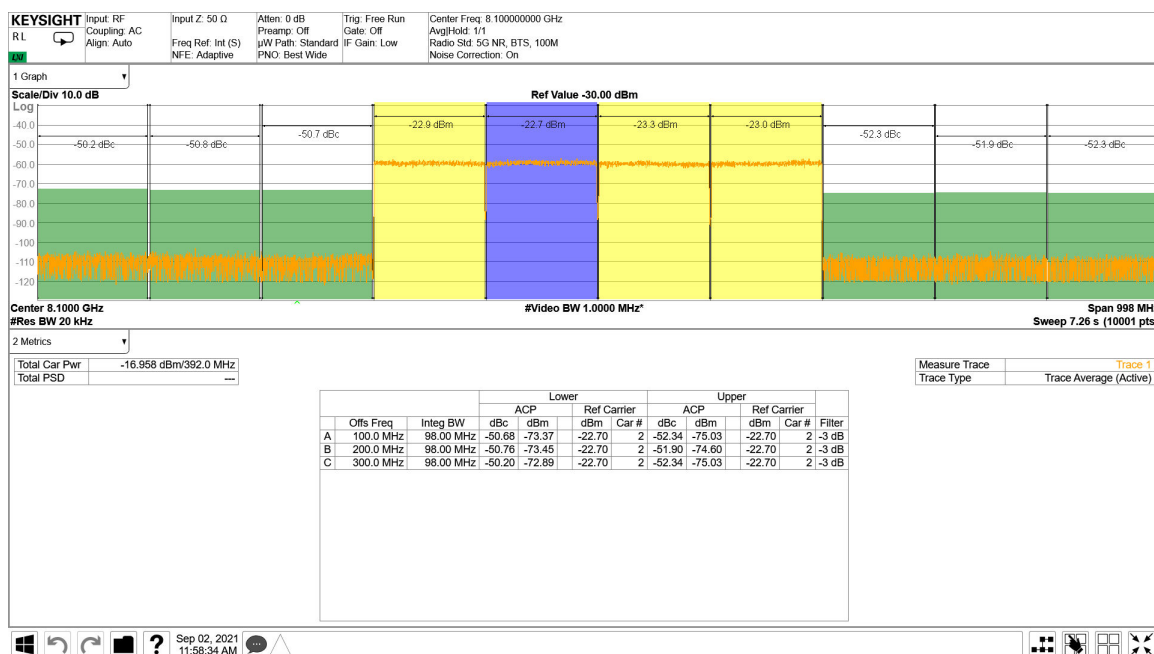


图 5-231. TX 4x100 MHz NR Output Spectrum 8.11 GHz

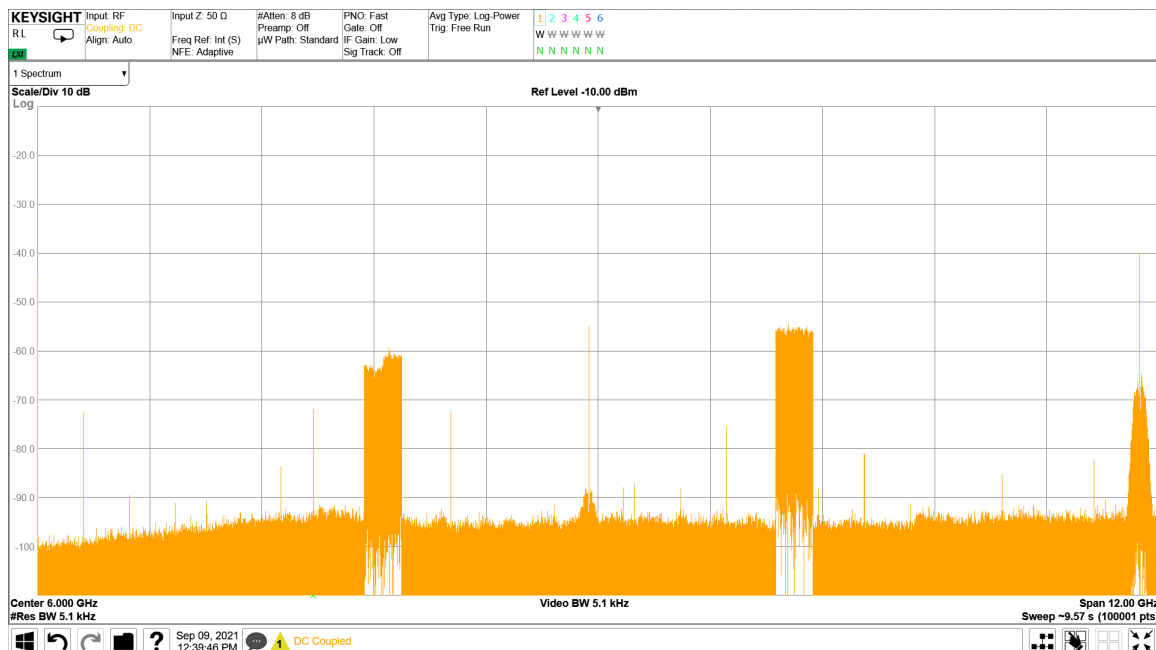
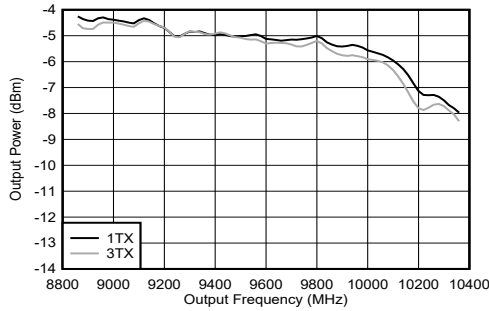


图 5-232. TX 4x100 MHz NR Output Spectrum 8.11 GHz

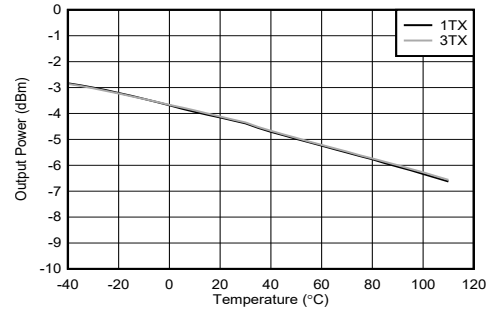
5.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



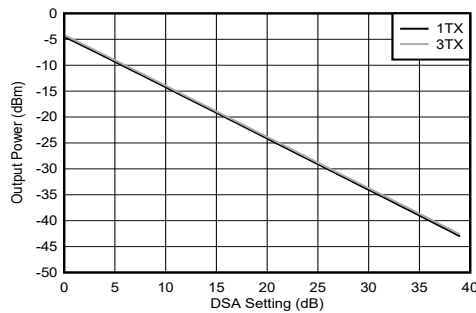
Includes PCB and cable losses.

FIG 5-233. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

FIG 5-234. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

FIG 5-235. TX Output Power vs DSA Setting at 9.61 GHz

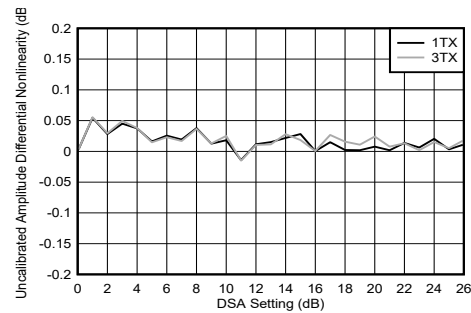


FIG 5-236. TX DSA Uncalibrated Amplitude Differential Nonlinearity

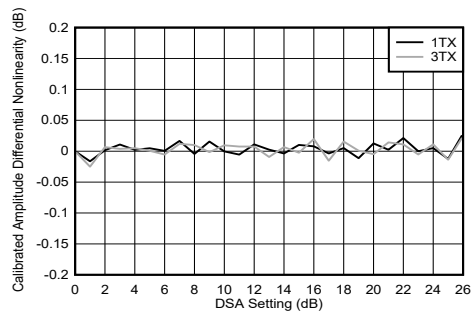


FIG 5-237. TX DSA Calibrated Amplitude Differential Nonlinearity

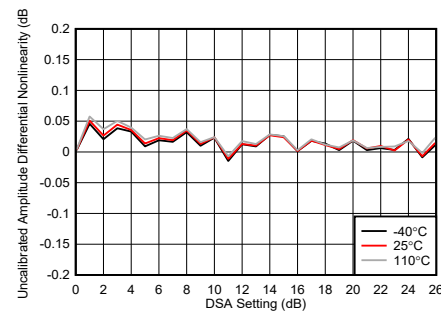


FIG 5-238. TX DSA Uncalibrated Amplitude Differential Nonlinearity

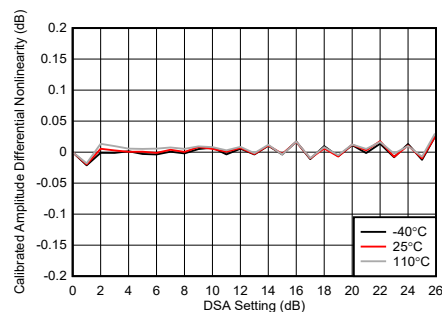


FIG 5-239. TX DSA Calibrated Amplitude Differential Nonlinearity

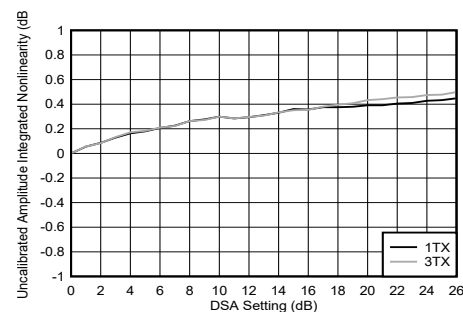


FIG 5-240. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching

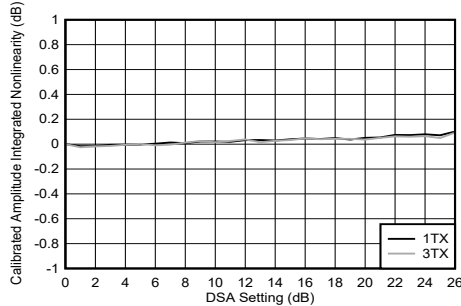


Figure 5-241. TX DSA Calibrated Amplitude Integrated Nonlinearity

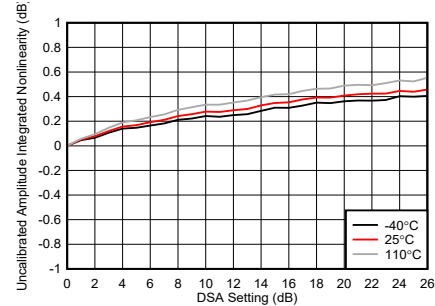


Figure 5-242. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

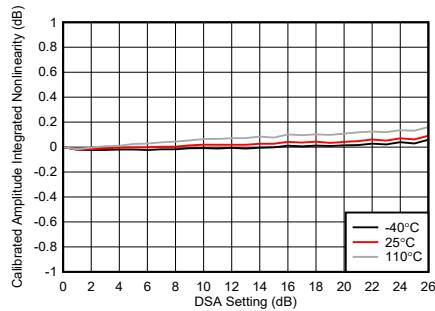


Figure 5-243. TX DSA Calibrated Amplitude Integrated Nonlinearity

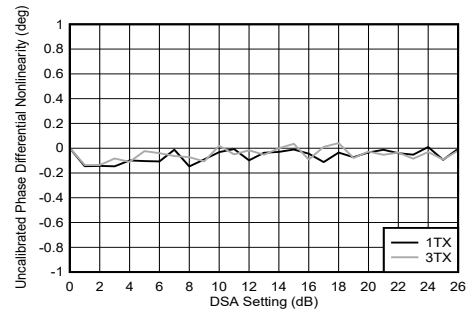


Figure 5-244. TX DSA Uncalibrated Phase Differential Nonlinearity

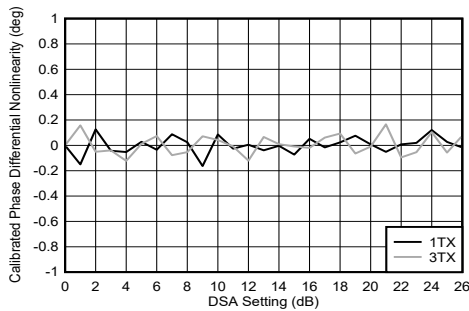


Figure 5-245. TX DSA Calibrated Phase Differential Nonlinearity

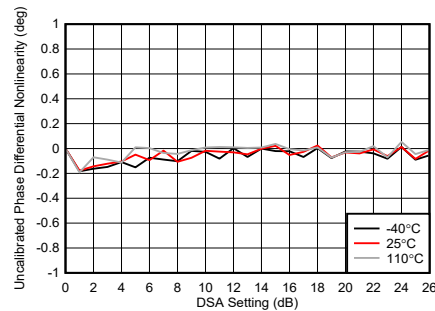


Figure 5-246. TX DSA Uncalibrated Phase Differential Nonlinearity

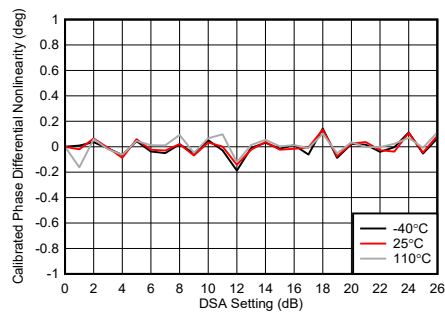


Figure 5-247. TX DSA Calibrated Phase Differential Nonlinearity

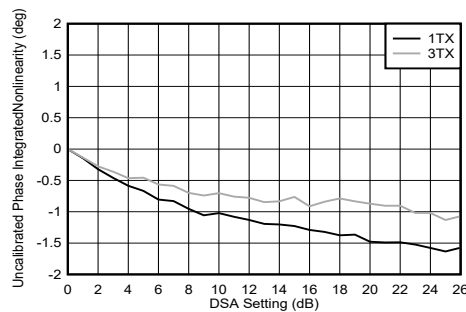


Figure 5-248. TX DSA Uncalibrated Phase Integrated Nonlinearity

5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching

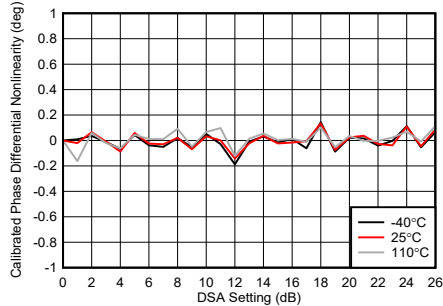


图 5-249. TX DSA Calibrated Phase Integrated Nonlinearity

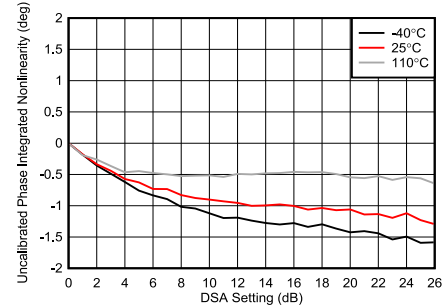


图 5-250. TX DSA Uncalibrated Phase Integrated Nonlinearity

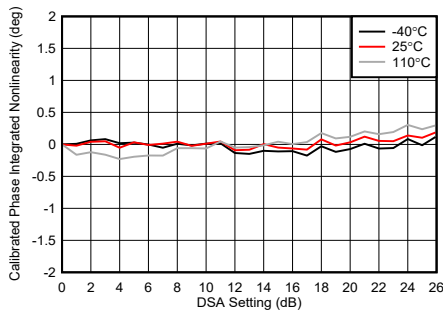
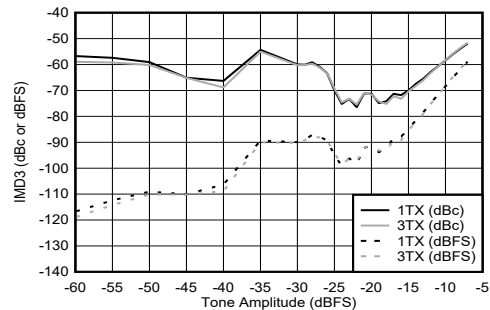
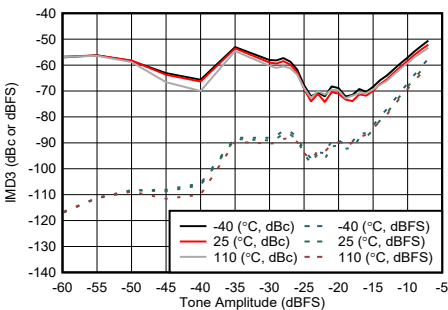


图 5-251. TX DSA Calibrated Amplitude Integrated Nonlinearity



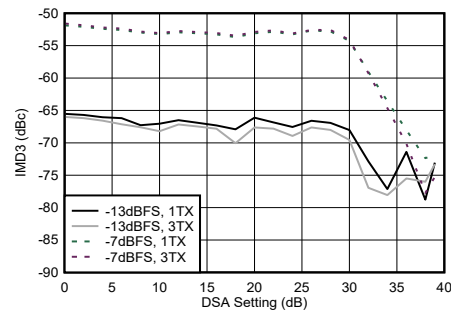
50 MHz tone spacing

图 5-252. TX IMD3 vs Digital Amplitude at 9.61 GHz



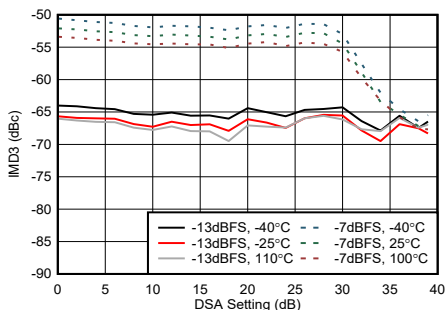
50 MHz tone spacing

图 5-253. TX IMD3 vs Digital Amplitude at 9.61 GHz



50 MHz tone spacing

图 5-254. TX IMD3 vs DSA Setting at 9.61 GHz



50 MHz tone spacing

图 5-255. TX IMD3 vs DSA Setting at 9.61 GHz

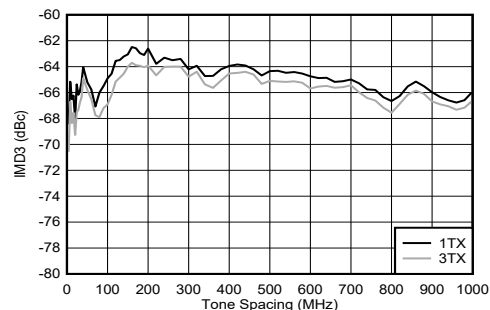


图 5-256. TX IMD3 vs Tone Spacing at 9.61 GHz

5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching

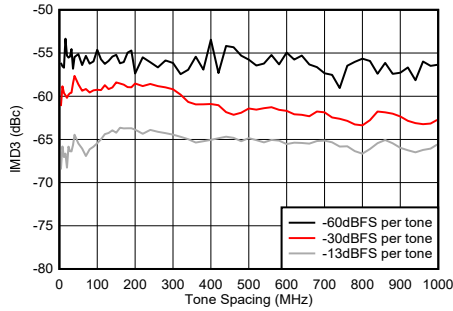


FIG 5-257. TX IMD3 vs Tone Spacing at 9.61 GHz

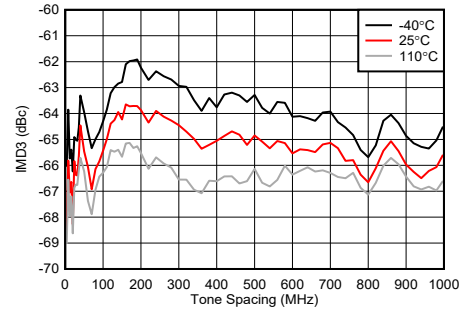


FIG 5-258. TX IMD3 vs Tone Spacing at 9.61 GHz

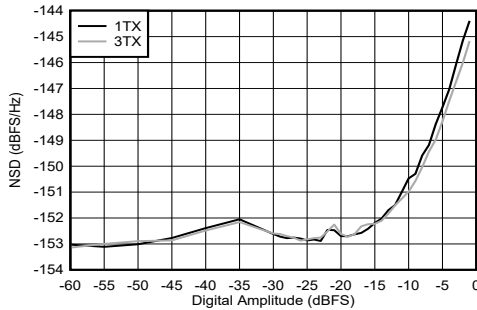


FIG 5-259. TX NSD vs Digital Amplitude at 9.61 GHz

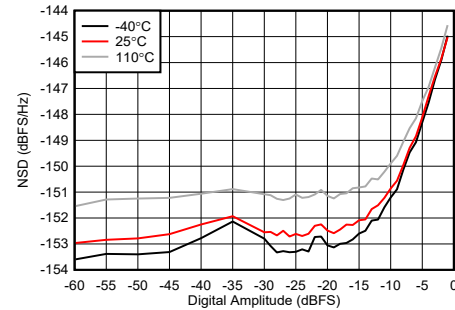


FIG 5-260. TX NSD vs Digital Amplitude at 9.61 GHz

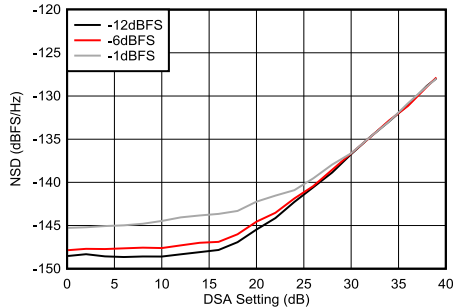


FIG 5-261. TX NSD vs DSA Setting at 9.61 GHz

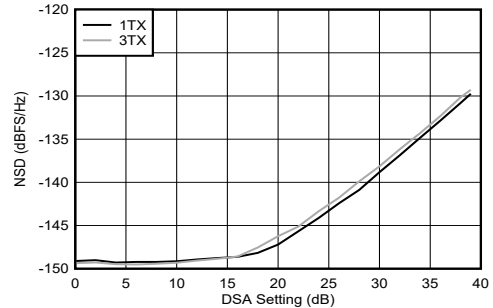


FIG 5-262. TX NSD vs DSA Setting at 9.61 GHz

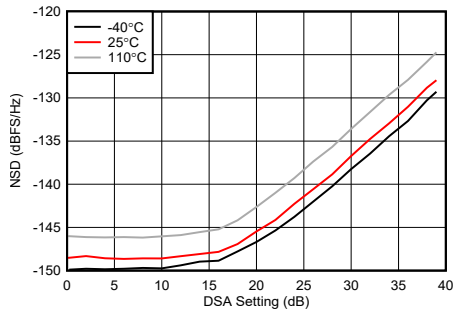
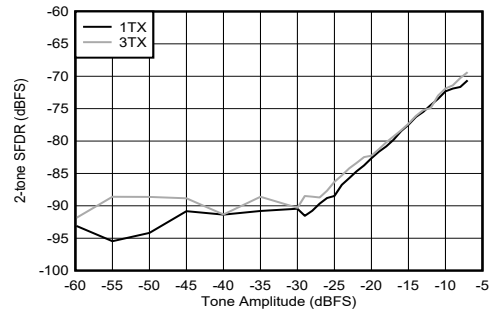


FIG 5-263. TX NSD vs DSA Setting at 9.61 GHz

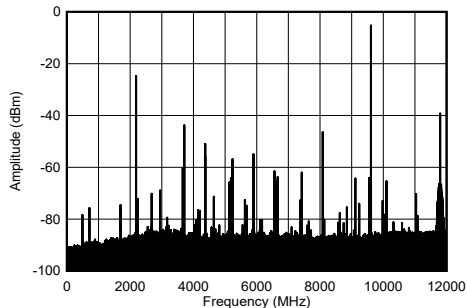


50 MHz tone spacing

FIG 5-264. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz

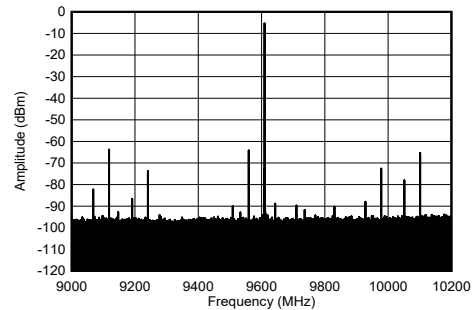
5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



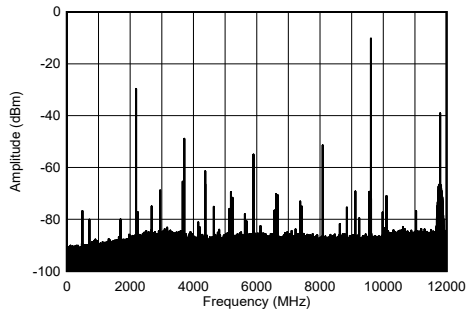
Includes PCB and cable losses.

✎ 5-265. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (wideband)



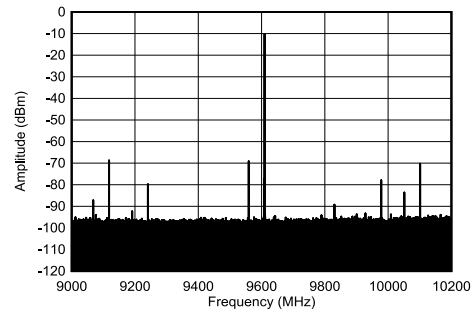
Includes PCB and cable losses.

✎ 5-266. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (1.2 GHz BW)



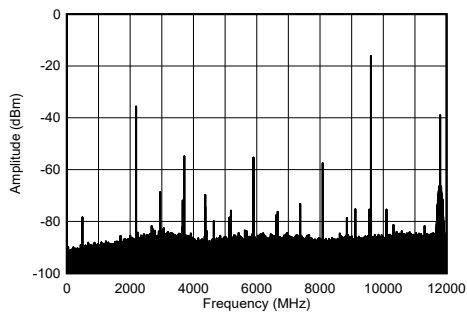
Includes PCB and cable losses.

✎ 5-267. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (wideband)



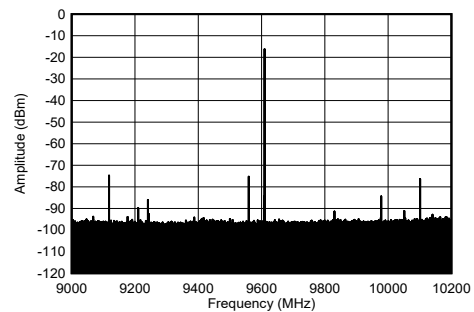
Includes PCB and cable losses.

✎ 5-268. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (1.2 GHz BW)



Includes PCB and cable losses.

✎ 5-269. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)

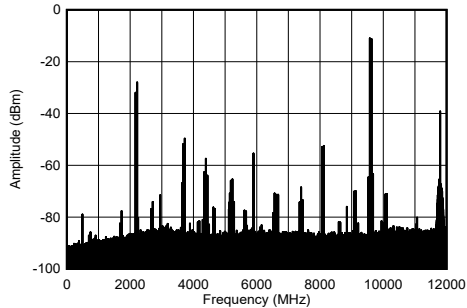


Includes PCB and cable losses.

✎ 5-270. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (1.2GHz BW)

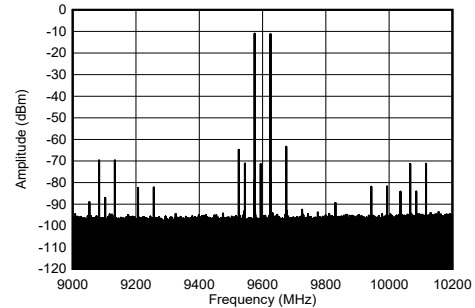
5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



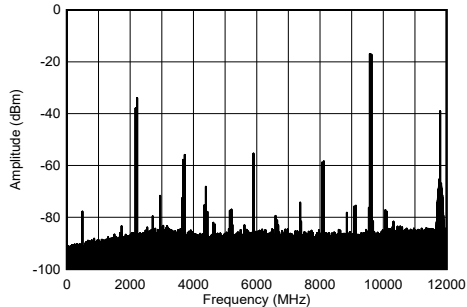
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-271. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (wideband)



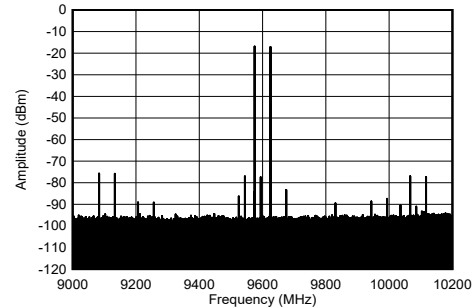
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-272. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (1.2 GHz BW)



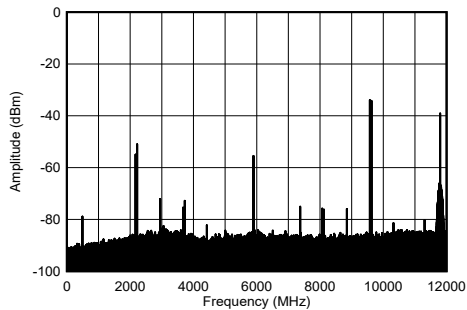
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-273. TX 2-Tone Spectrum at 9.61 GHz and -13 dBFS (wideband)



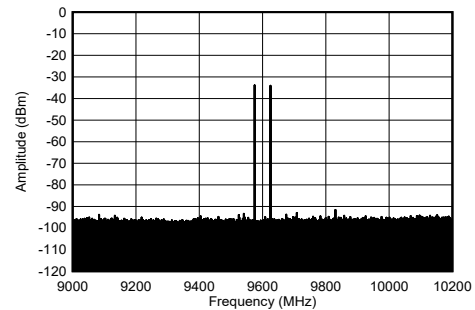
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-274. TX 2-Tone Spectrum at 9.61 GHz and -13 dBFS (1.2 GHz BW)



Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-275. TX 2-Tone Spectrum at 9.61 GHz and -30 dBFS Each (wideband)

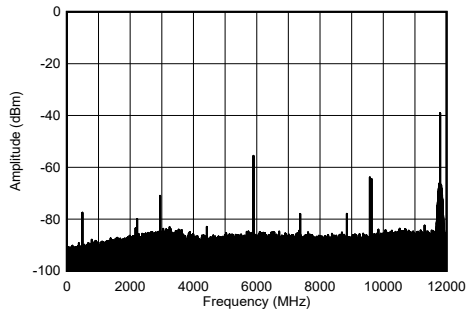


Includes PCB and cable losses, 50 MHz tone spacing.

Figure 5-276. TX 2-Tone Spectrum at 9.61 GHz and -30 dBFS Each (1.2 GHz BW)

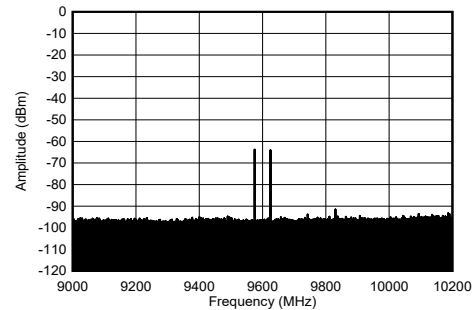
5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



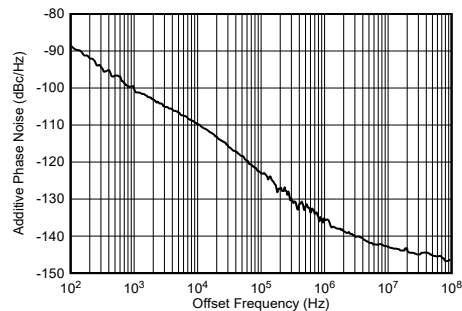
Includes PCB and cable losses, 50 MHz tone spacing.

FIG 5-277. TX 2-Tone Spectrum at 9.61 GHz and -60 dBFS Each (wideband)



Includes PCB and cable losses, 50MHz tone spacing.

FIG 5-278. TX 2-Tone Spectrum at 9.61 GHz and -60 dBFS Each (1.2 GHz BW)



Single sideband, external clock mode, input clock phase noise removed

FIG 5-279. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz

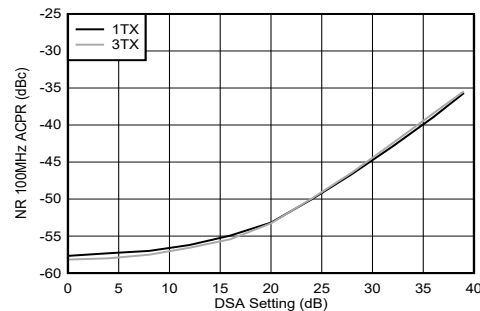


FIG 5-280. TX NR100 MHz ACPR vs DSA Setting at 9.61 GHz

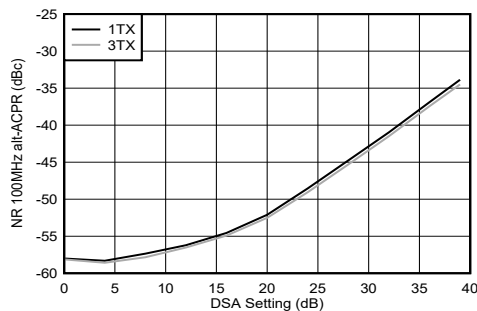


FIG 5-281. TX NR100 MHz alt-ACPR vs DSA Setting at 9.61 GHz

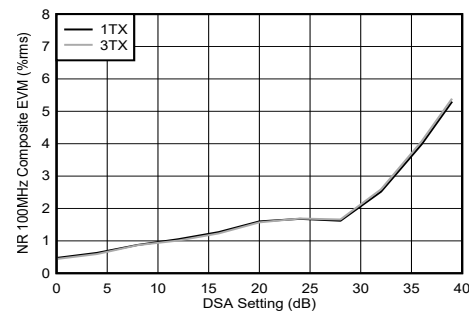
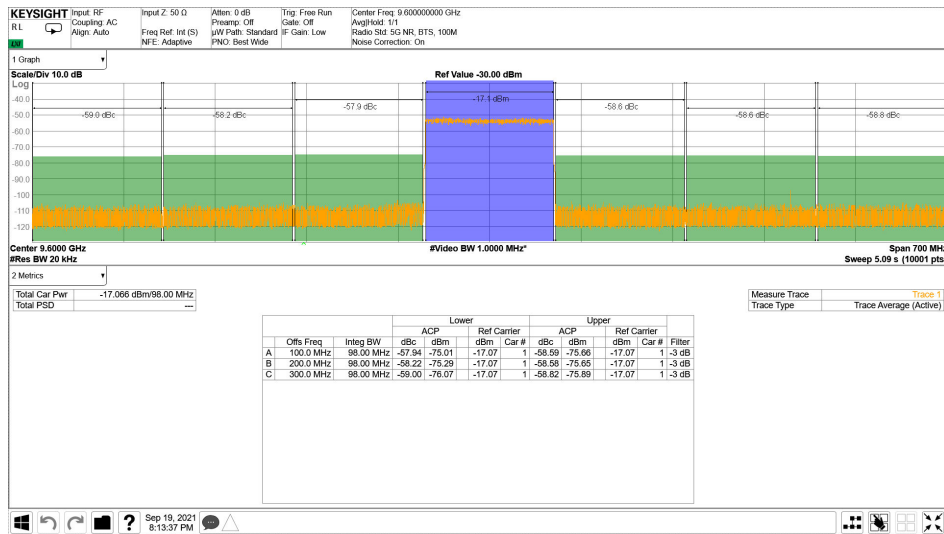


FIG 5-282. TX NR100 MHz EVM vs DSA Setting at 9.61 GHz

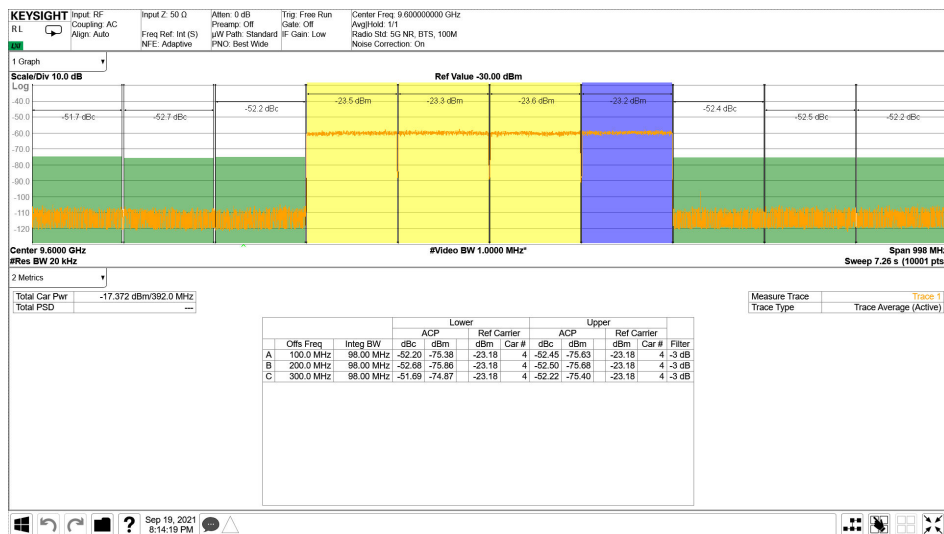
5.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



Includes PCB and cable losses.

FIG 5-283. TX NR100 MHz Output Spectrum at 9.61 GHz

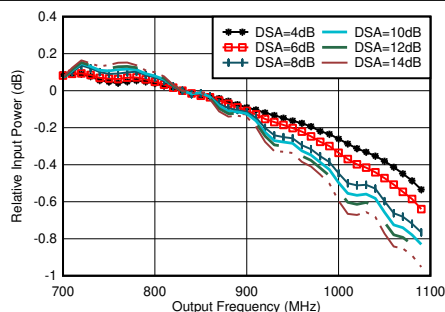


Includes PCB and cable losses.

FIG 5-284. TX 4xNR100 MHz Output Spectrum at 9.61 GHz

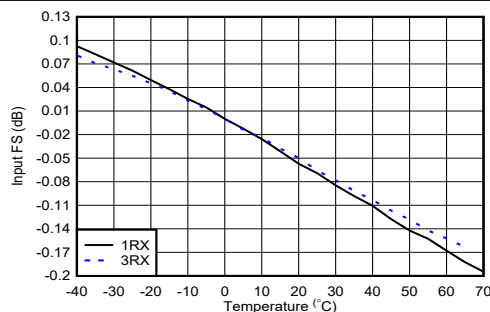
5.12.8 RX Typical Characteristics at 800 MHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



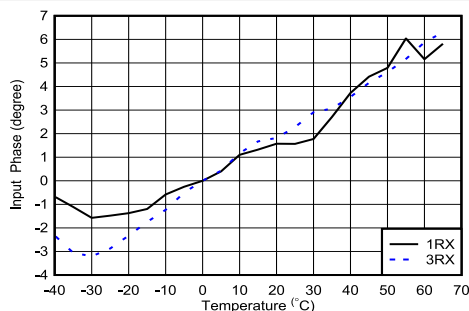
With 0.8 GHz matching, normalized to 830 MHz

FIG 5-285. RX In-Band Gain Flatness for Channel 1RX, $f_{\text{IN}} = 830\text{ MHz}$



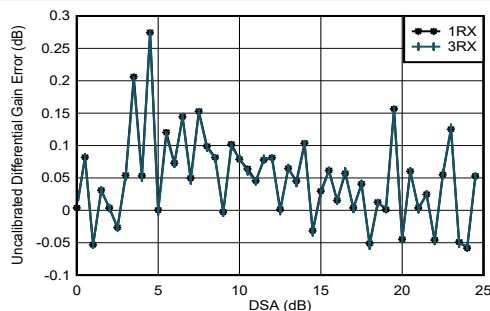
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

FIG 5-286. RX Input Fullscale vs Temperature and Channel at 800 MHz



With 0.8 GHz matching, normalized to phase at 25°C

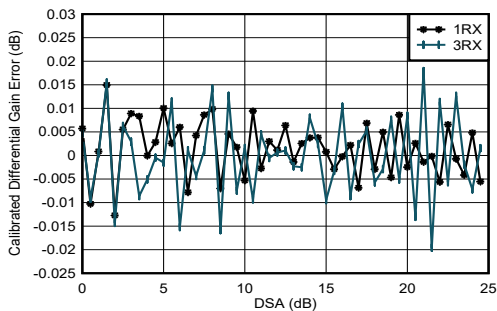
FIG 5-287. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 0.8\text{ GHz}$



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

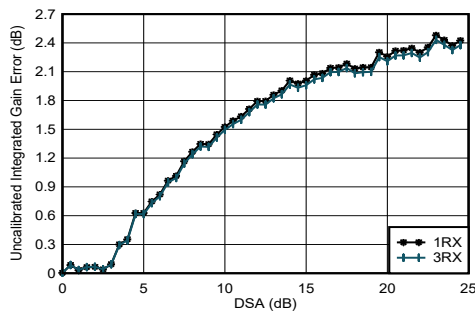
FIG 5-288. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

FIG 5-289. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



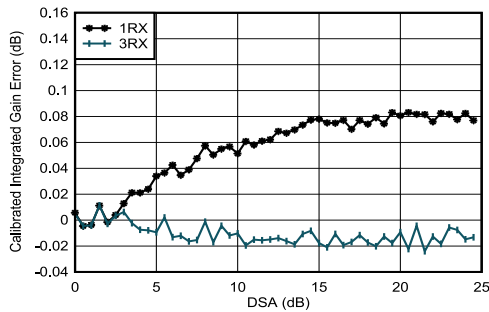
With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-290. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

5.12.8 RX Typical Characteristics at 800 MHz (continued)

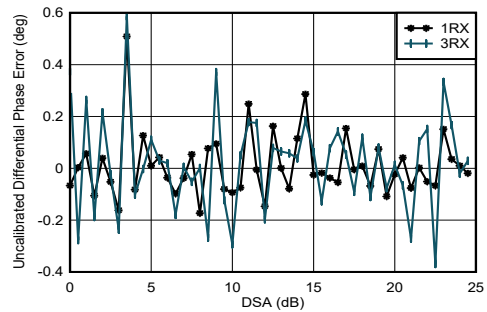
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

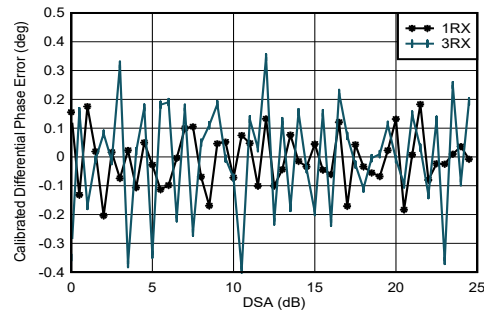
FIG 5-291. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

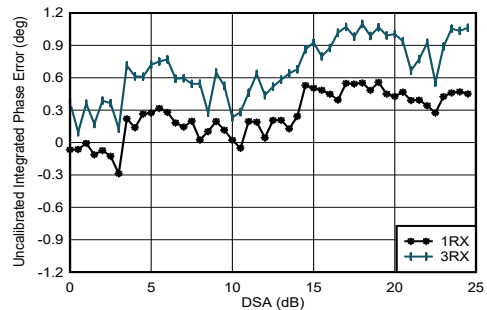
FIG 5-292. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

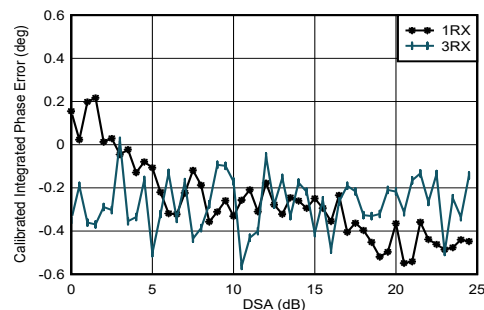
FIG 5-293. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

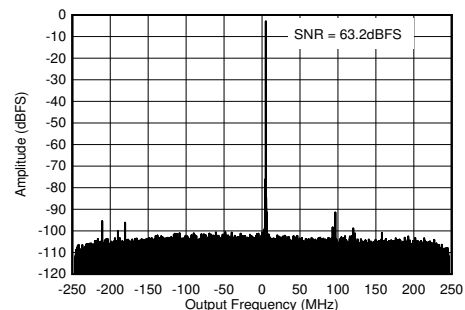
FIG 5-294. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

FIG 5-295. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

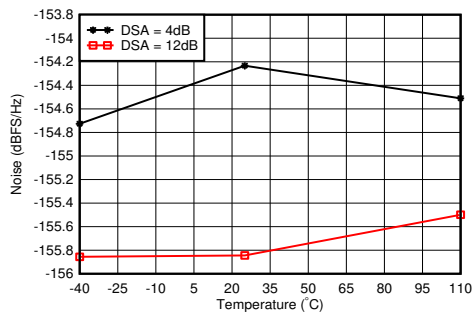


With 0.8 GHz matching, $f_{\text{IN}} = 840 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

FIG 5-296. RX Output FFT at 0.8 GHz

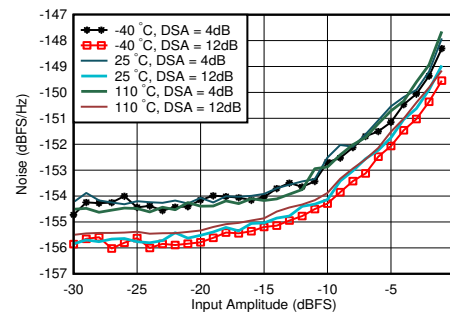
5.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



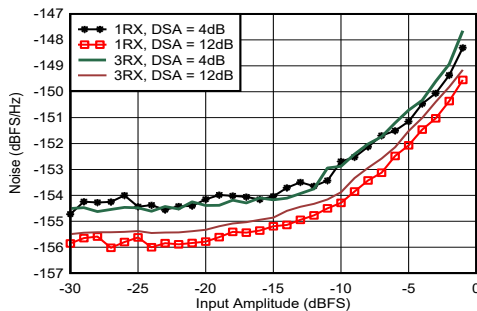
With 0.8 GHz matching, 12.5-MHz offset from tone

FIG 5-297. RX Noise Spectral Density vs Temperature at 0.8 GHz



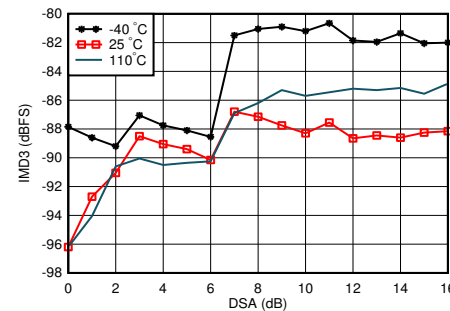
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

FIG 5-298. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



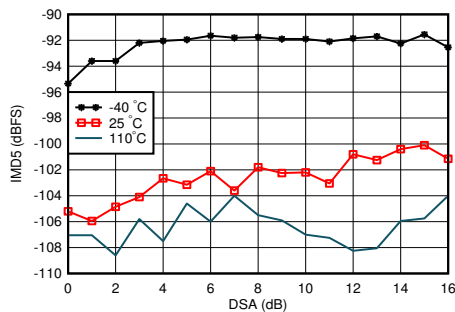
With 0.8 GHz matching, 12.5-MHz offset from tone

FIG 5-299. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



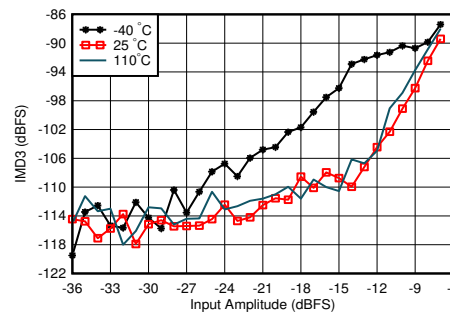
A. With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

FIG 5-300. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

FIG 5-301. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz

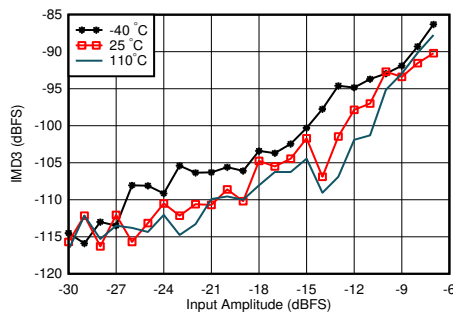


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

FIG 5-302. RX IMD3 vs Input Level and Temperature at 0.8 GHz

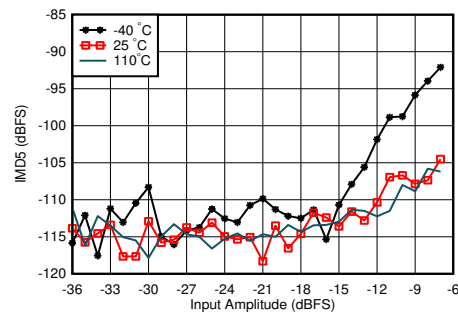
5.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



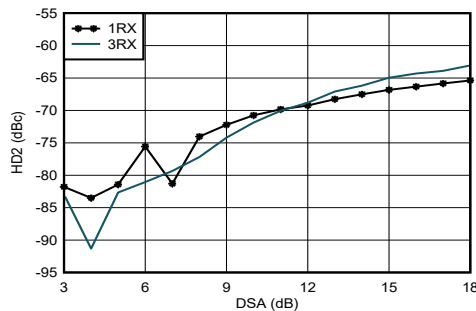
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

FIG 5-303. RX IMD3 vs Input Level and Temperature at 0.8 GHz



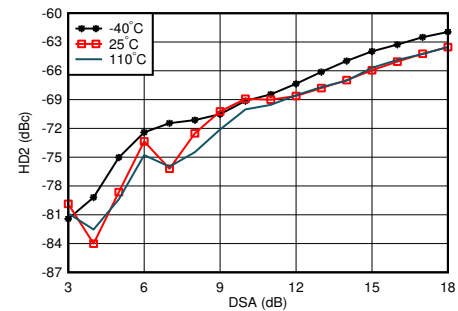
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

FIG 5-304. RX IMD5 vs Input Level and Temperature at 0.8 GHz



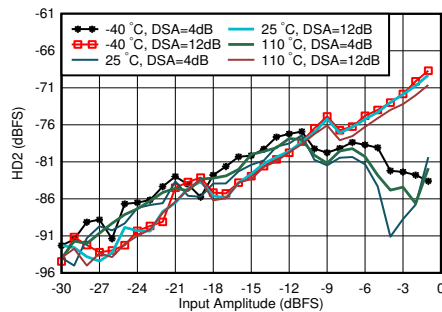
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-305. RX HD2 vs DSA Setting and Channel at 0.8 GHz



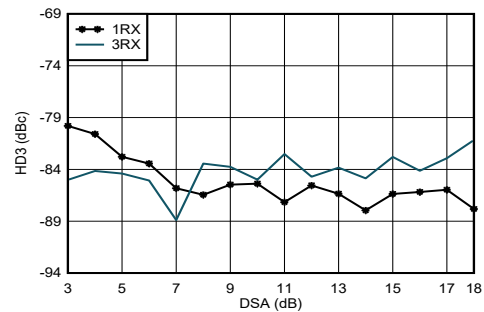
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-306. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-307. RX HD2 vs Input Level and Temperature at 0.8 GHz

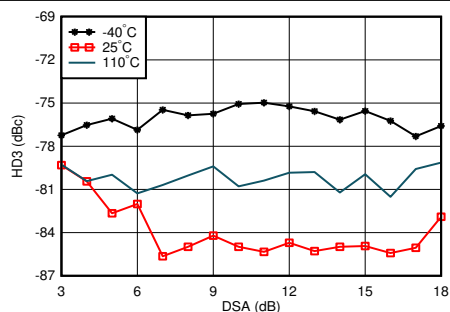


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-308. RX HD3 vs DSA Setting and Channel at 0.8 GHz

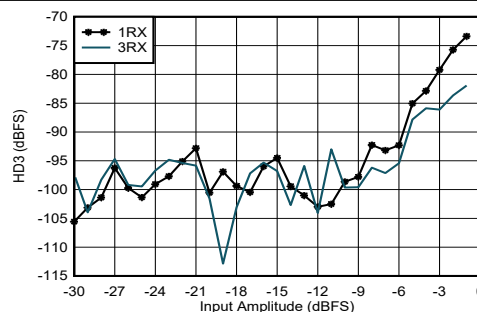
5.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



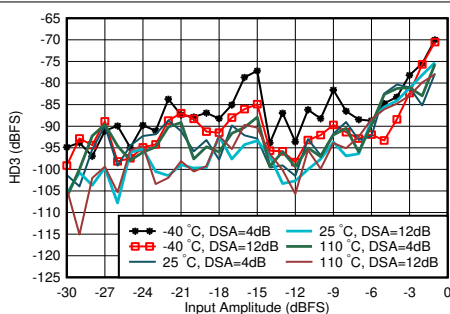
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-309. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



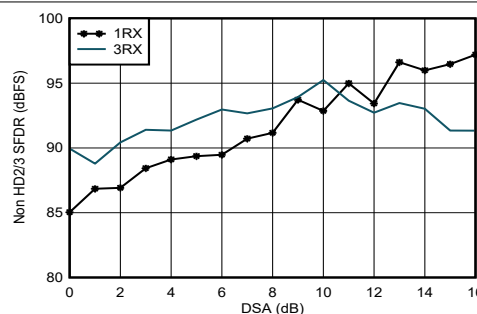
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-310. RX HD3 vs Input Level and Channel at 0.8 GHz



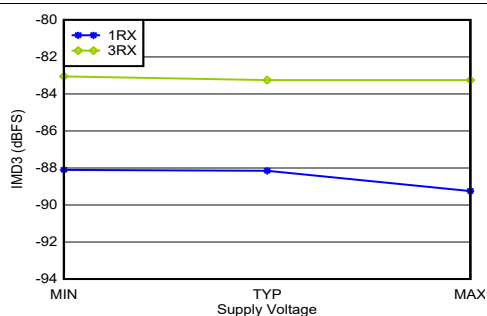
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-311. RX HD3 vs Input Level and Temperature at 0.8 GHz



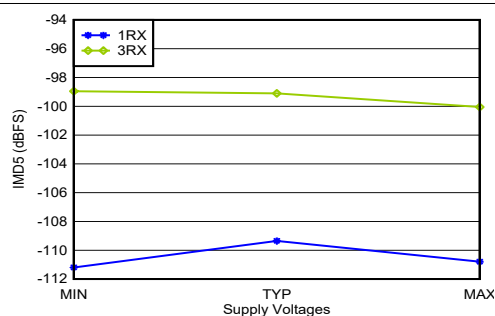
With 0.8 GHz matching

FIG 5-312. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-313. RX IMD3 vs Supply and Channel at 0.8 GHz

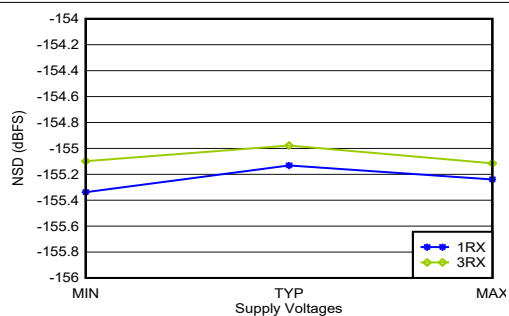


With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-314. RX IMD5 vs Supply and Channel at 0.8 GHz

5.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.

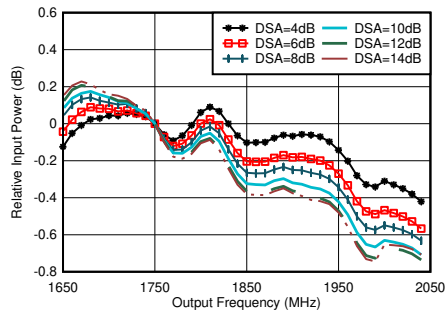


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 5-315. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

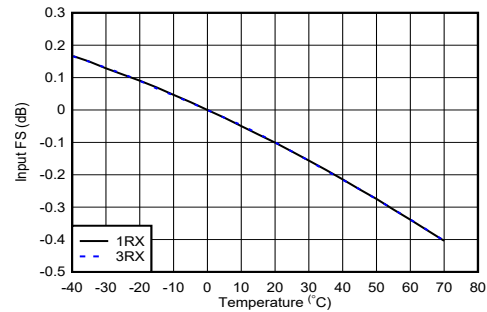
5.12.9 RX Typical Characteristics at 1.75-1.9 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



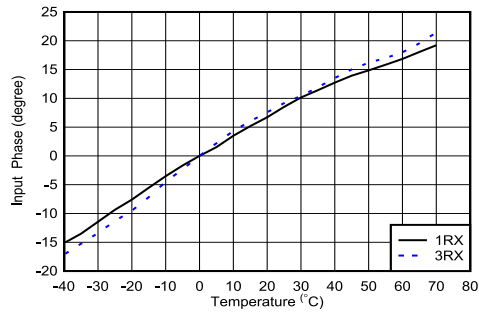
With 1.8 GHz matching, normalized to 1.75 GHz

FIG 5-316. RX In-Band Gain Flatness, $f_{\text{IN}} = 1750\text{ MHz}$



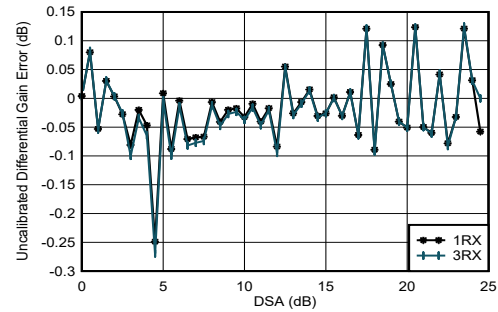
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

FIG 5-317. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

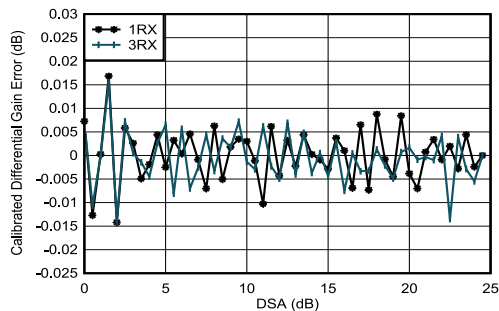
FIG 5-318. RX Input Phase vs Temperature and DSA at $f_{\text{IN}} = 1.75\text{ GHz}$



With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

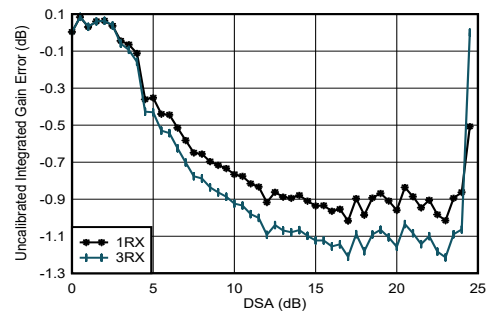
FIG 5-319. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

FIG 5-320. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



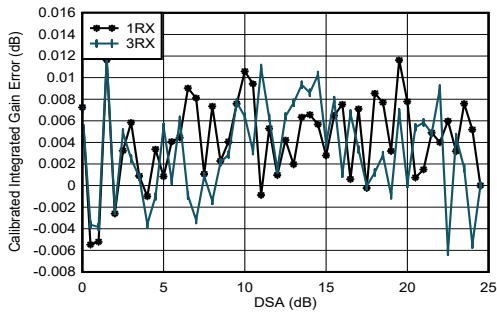
With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-321. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

5.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

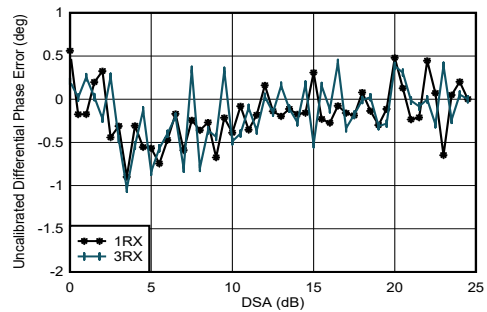
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

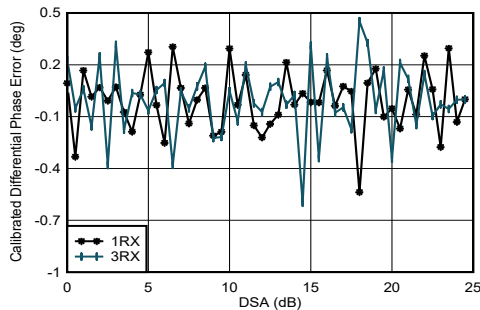
FIG 5-322. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

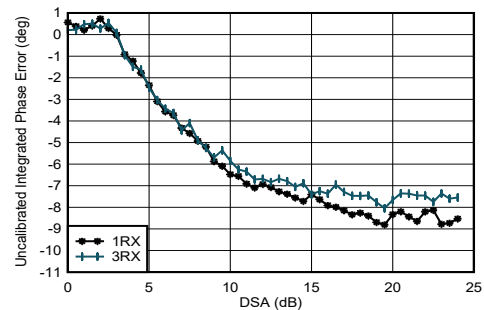
FIG 5-323. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

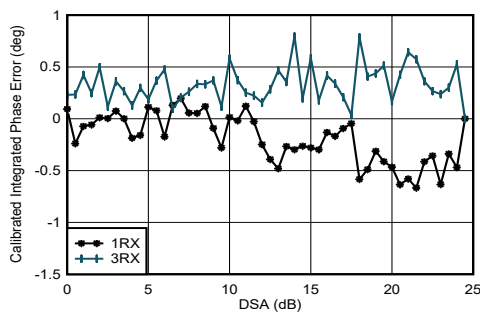
FIG 5-324. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

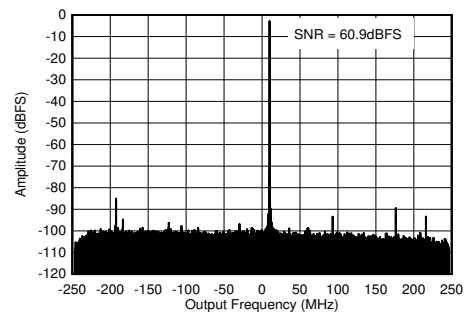
FIG 5-325. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

FIG 5-326. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

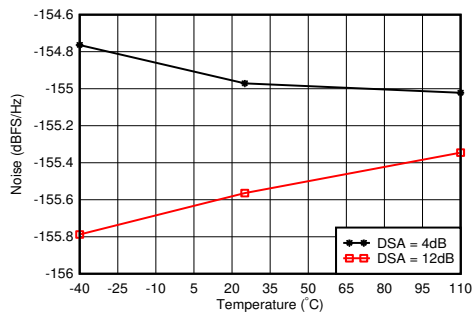


With 1.8 GHz matching, $f_{\text{IN}} = 2610 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

FIG 5-327. RX Output FFT at 1.75 GHz

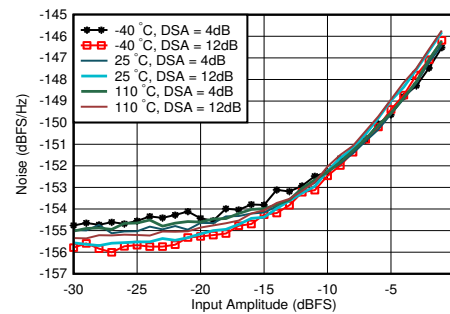
5.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



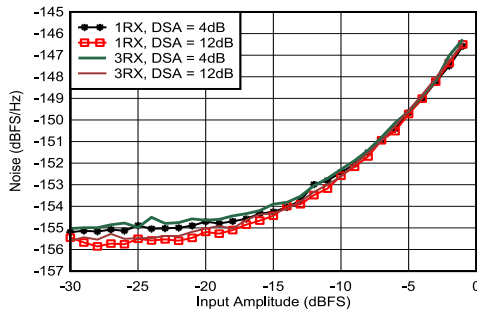
With 1.8 GHz matching, 12.5-MHz offset from tone

FIG 5-328. RX Noise Spectral Density vs Temperature at 1.75 GHz



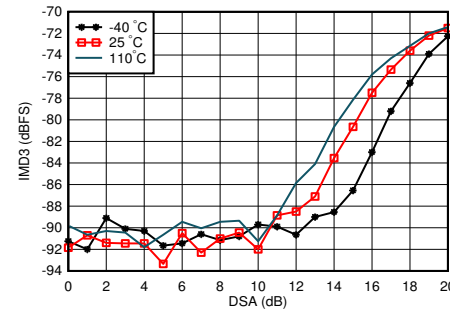
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

FIG 5-329. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



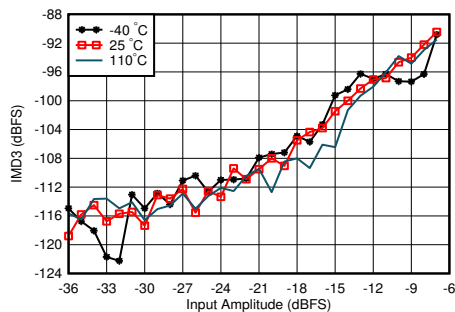
With 1.8 GHz matching, 12.5-MHz offset from tone

FIG 5-330. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



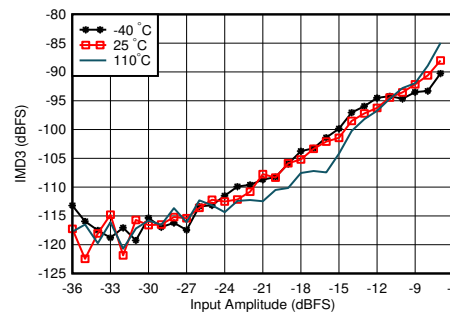
With 1.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

FIG 5-331. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

FIG 5-332. RX IMD3 vs Input Level and Temperature at 1.75 GHz

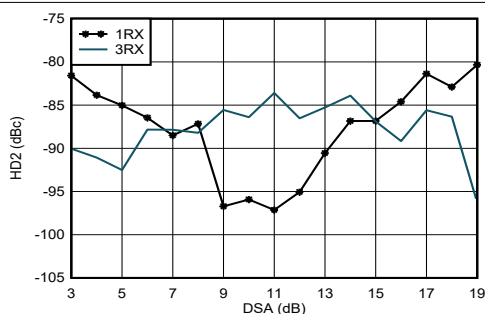


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

FIG 5-333. RX IMD3 vs Input Level and Temperature at 1.75 GHz

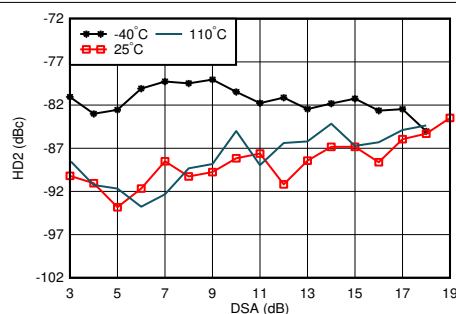
5.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



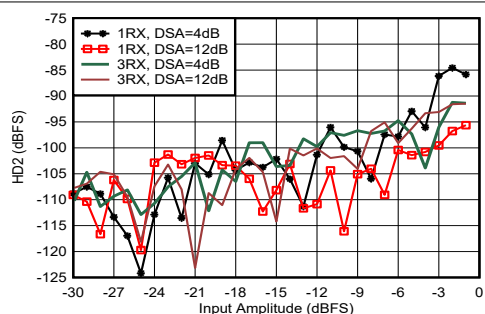
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-334. RX HD2 vs DSA Setting and Channel at 1.9 GHz



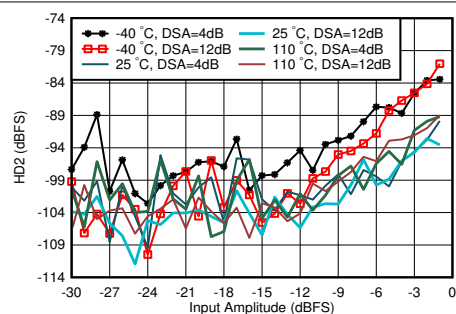
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-335. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



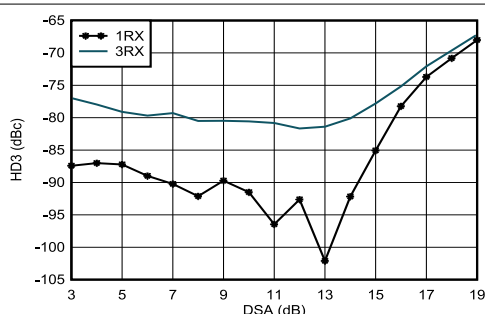
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-336. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



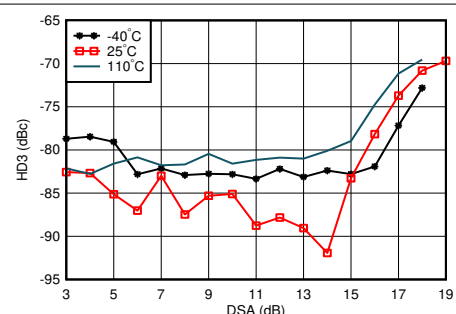
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-337. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

FIG 5-338. RX HD3 vs DSA Setting and Channel at 1.9 GHz

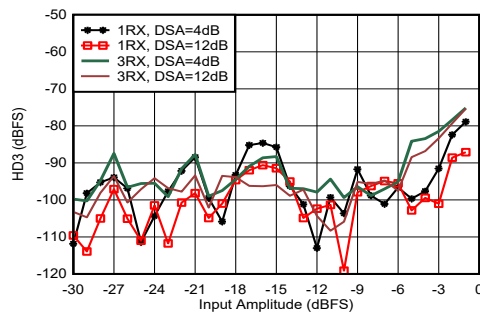


With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

FIG 5-339. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

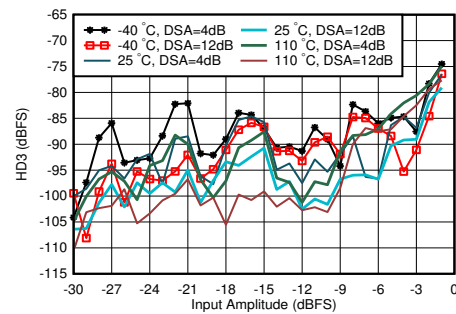
5.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



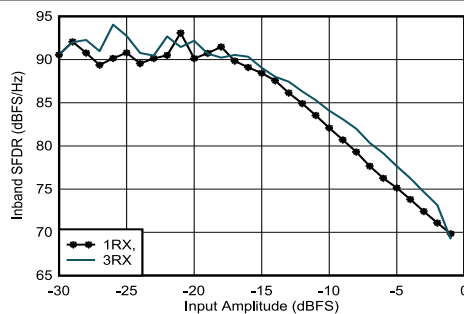
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

FIG 5-340. RX HD3 vs Input Level and Channel at 1.9 GHz



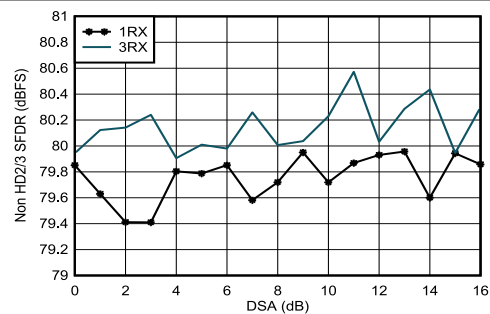
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

FIG 5-341. RX HD3 vs Input Level and Temperature at 1.9 GHz



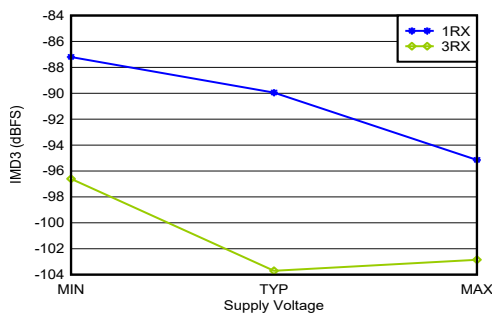
With 1.8 GHz matching, decimated by 3

FIG 5-342. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude at 1.75 GHz



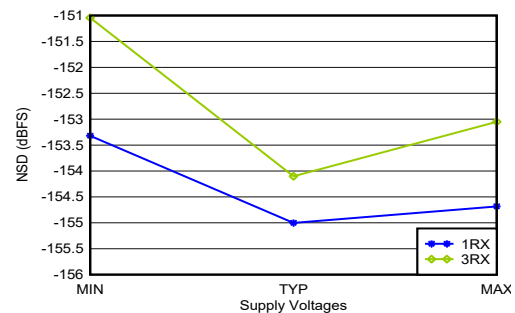
With 1.8 GHz matching

FIG 5-343. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



With 1.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-344. RX IMD3 vs Supply and Channel at 1.75 GHz

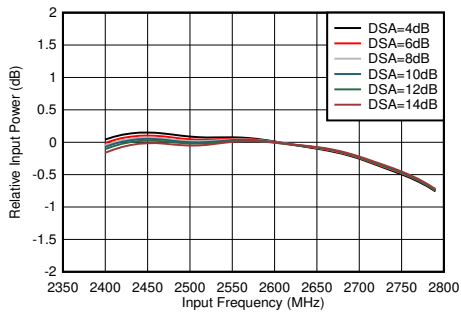


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-345. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

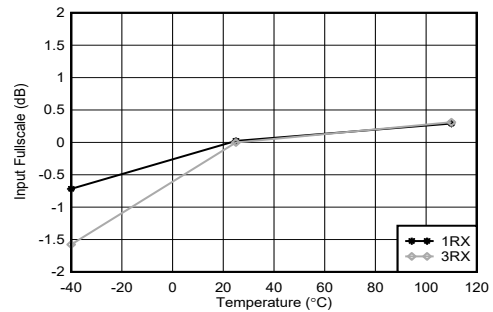
5.12.10 RX Typical Characteristics at 2.6 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



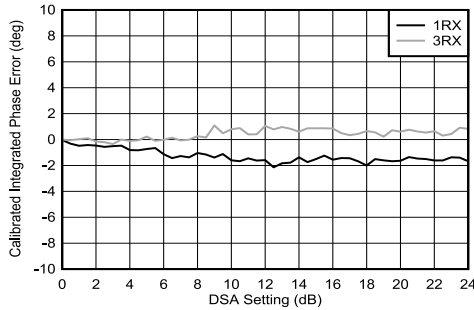
With matching, normalized to power at 2.6 GHz for each DSA setting

FIG 5-346. RX Inband Gain Flatness, $f_{\text{IN}} = 2600 \text{ MHz}$



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

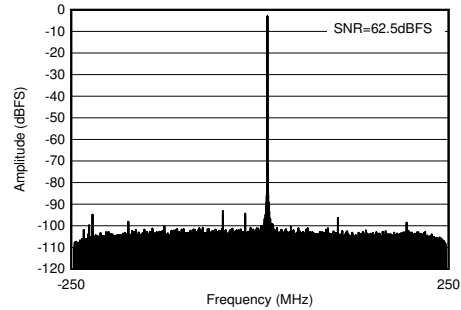
FIG 5-347. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

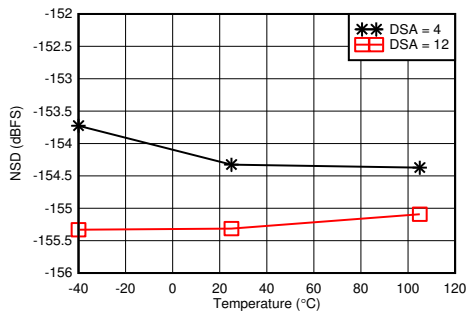
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

FIG 5-348. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



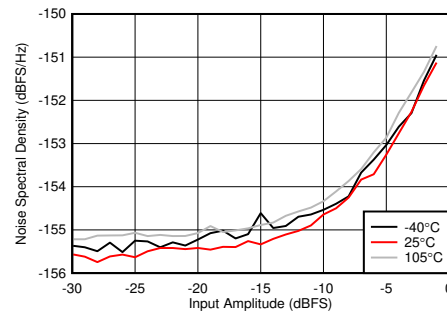
With 2.6 GHz matching, $f_{\text{IN}} = 2610 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

FIG 5-349. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

FIG 5-350. RX Noise Spectral Density vs Temperature at 2.6 GHz

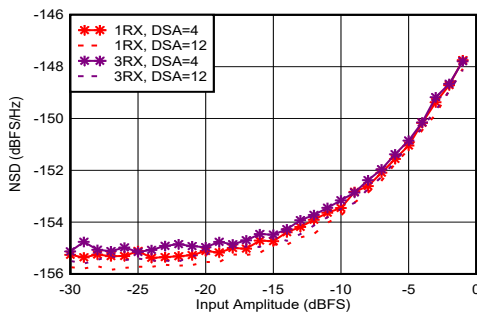


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

FIG 5-351. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

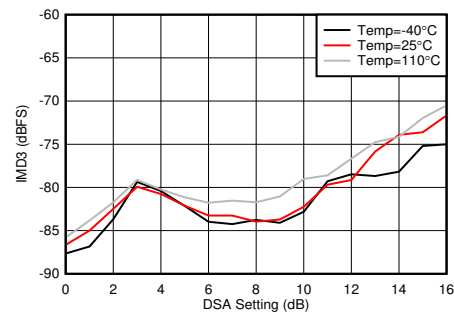
5.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



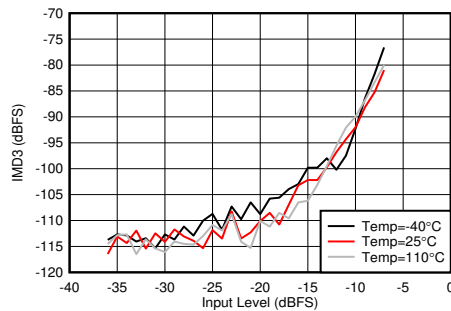
With 2.6 GHz matching, 12.5-MHz offset from tone

FIG 5-352. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



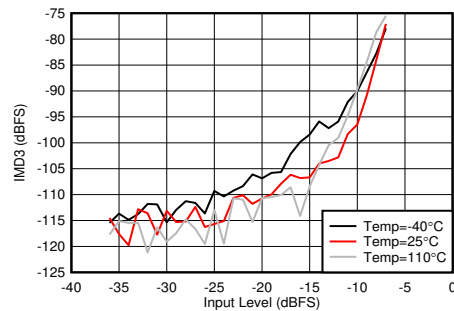
With 2.6 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

FIG 5-353. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



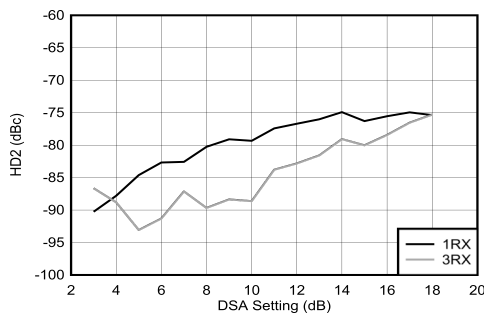
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

FIG 5-354. RX IMD3 vs Input Level and Temperature at 2.6 GHz



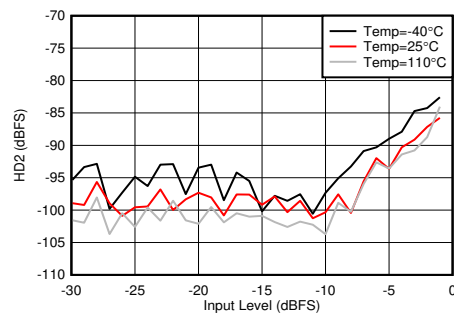
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

FIG 5-355. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-356. RX HD2 vs DSA Setting and Channel at 2.6 GHz

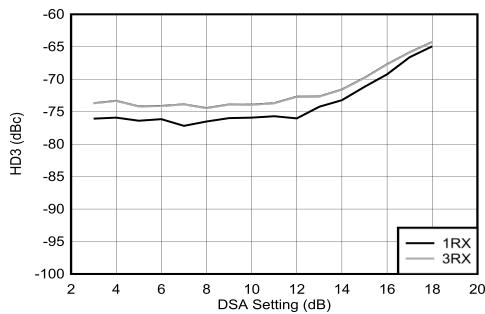


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-357. RX HD2 vs Input Level and Temperature at 2.6 GHz

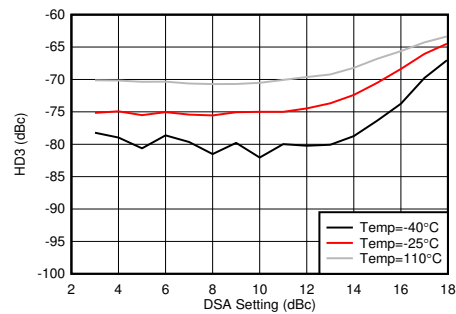
5.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



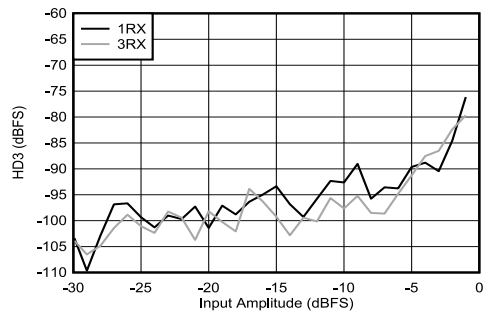
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-358. RX HD3 vs DSA Setting and Channel at 2.6 GHz



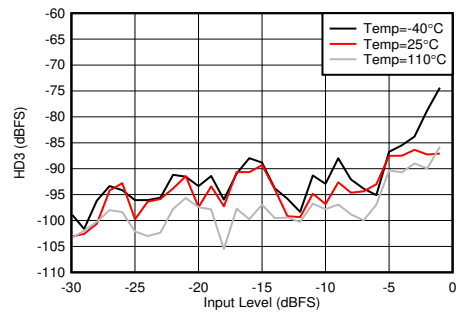
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-359. RX HD3 vs DSA Setting and Temperature at 2.6 GHz



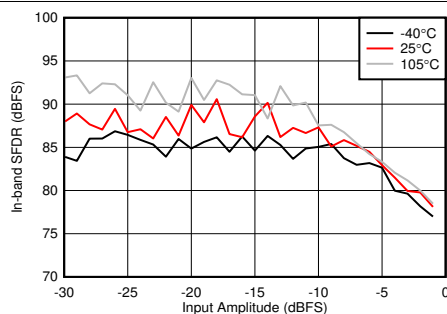
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-360. RX HD3 vs Input Level and Channel at 2.6 GHz



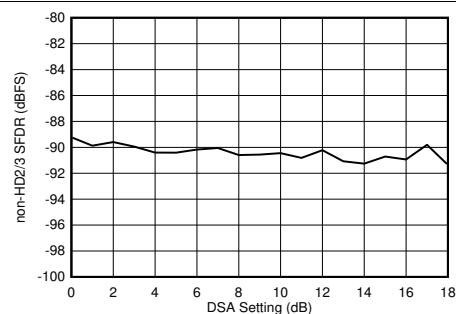
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-361. RX HD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, decimate by 4

FIG 5-362. RX In-Band SFDR ($\pm 300 \text{ MHz}$) vs Input Amplitude and Temperature at 2.6 GHz

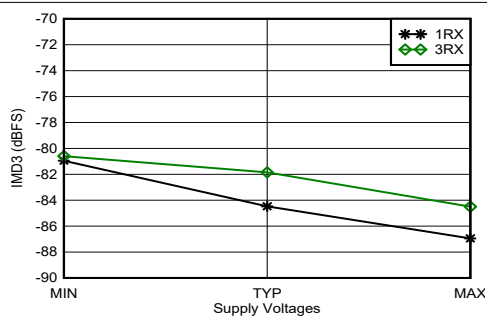


With 2.6 GHz matching

FIG 5-363. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

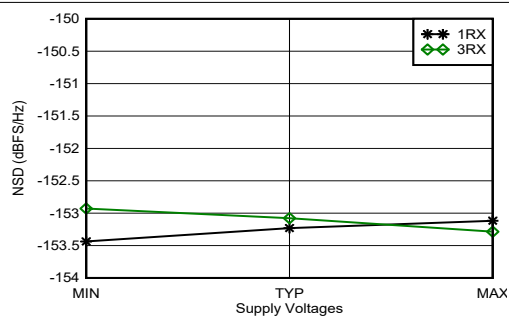
5.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-364. RX IMD3 vs Supply and Channel at 2.6 GHz

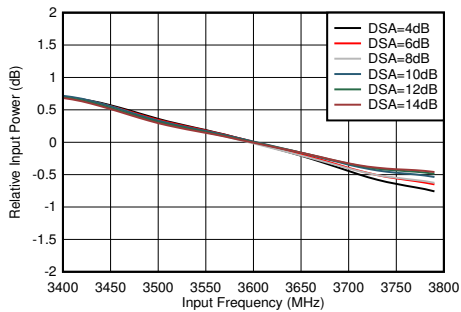


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-365. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

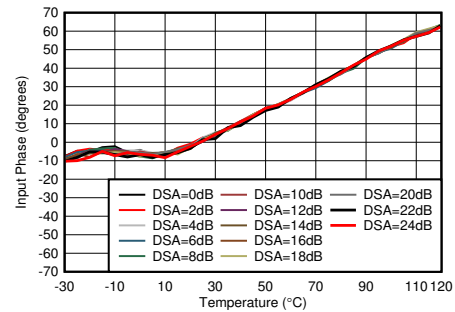
5.12.11 RX Typical Characteristics at 3.5 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



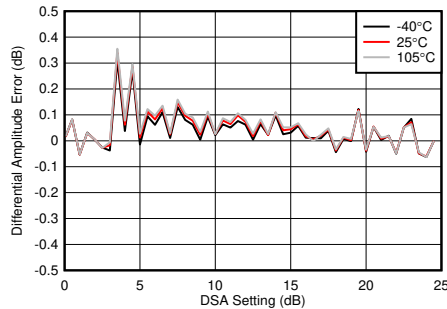
With 3.6 GHz matching, normalized to 3.6 GHz

FIG 5-366. RX In-Band Gain Flatness, $f_{\text{IN}} = 3600 \text{ MHz}$



With 3.6 GHz matching, normalized to phase at 25°C

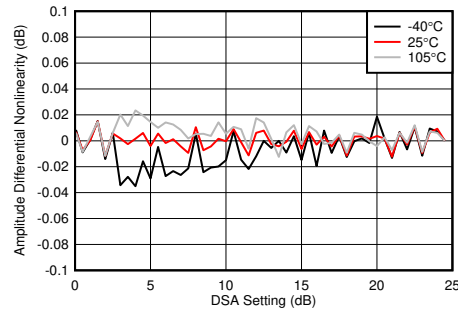
FIG 5-367. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

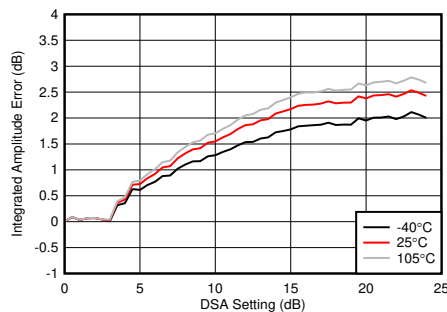
FIG 5-368. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

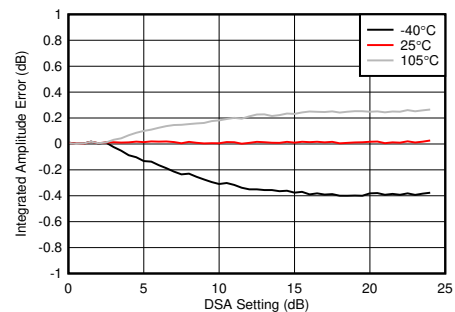
FIG 5-369. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-370. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



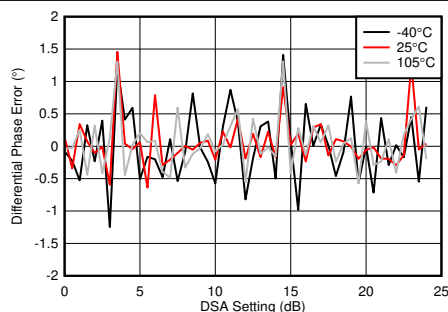
With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-371. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

5.12.11 RX Typical Characteristics at 3.5 GHz (continued)

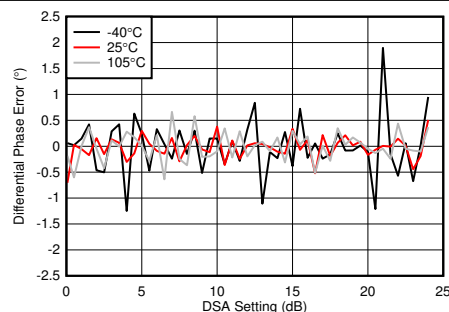
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

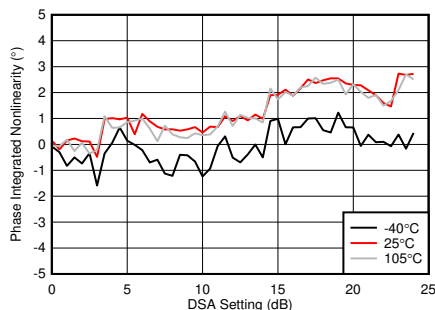
FIG 5-372. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

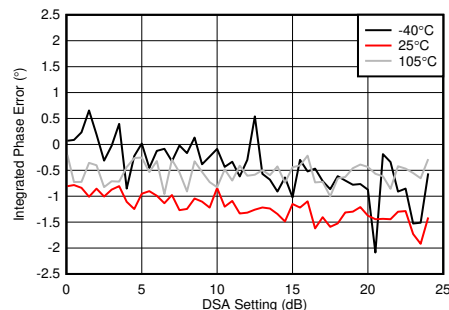
FIG 5-373. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

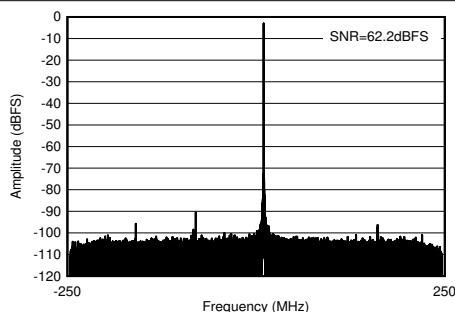
FIG 5-374. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

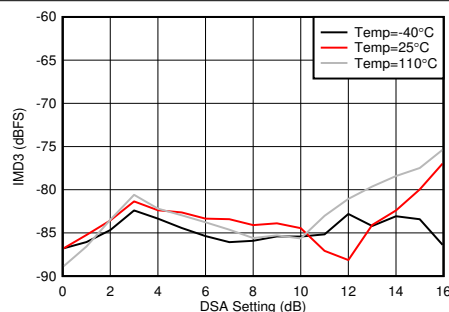
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

FIG 5-375. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching, $f_{\text{IN}} = 3610 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

FIG 5-376. RX Output FFT at 3.6 GHz

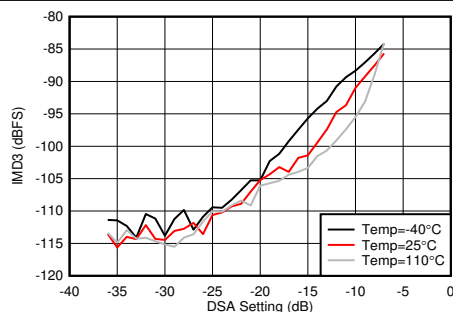


With 3.5 GHz matching, each tone at -7 dBFS , 20-MHz tone spacing

FIG 5-377. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

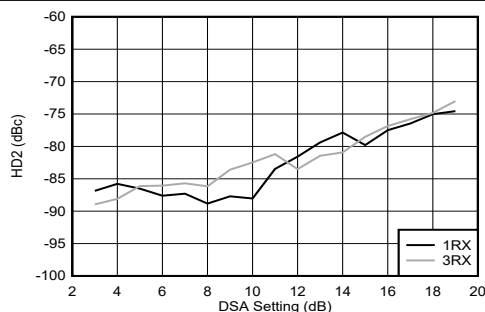
5.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



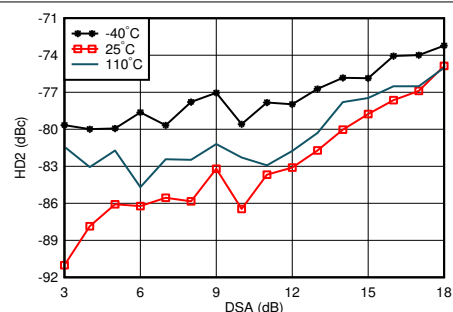
With 3.5 GHz matching, 20-MHz tone spacing

Figure 5-378. RX IMD3 vs Input Level and Temperature at 3.6 GHz



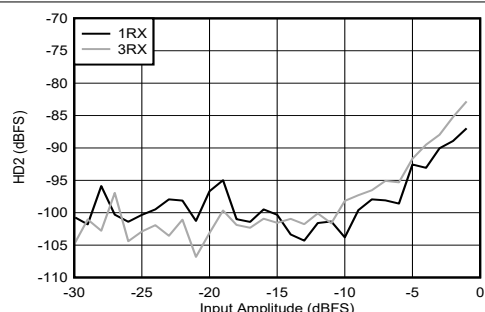
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-379. RX HD2 vs DSA Setting and Channel at 3.6 GHz



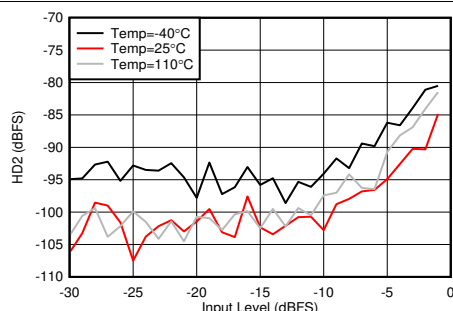
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-380. RX HD2 vs DSA Setting and Temperature at 3.6 GHz



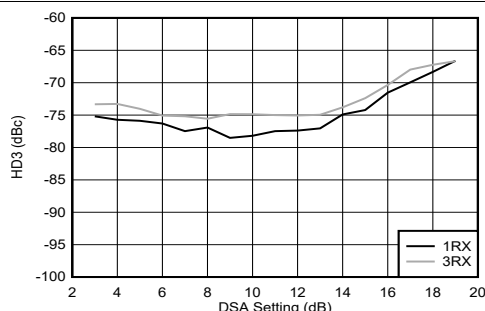
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-381. RX HD2 vs Input Level and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-382. RX HD2 vs Input Level and Temperature at 3.6 GHz

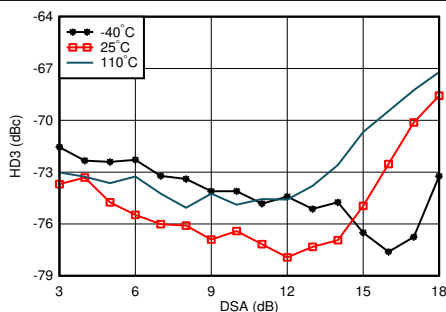


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 5-383. RX HD3 vs DSA Setting and Channel at 3.6 GHz

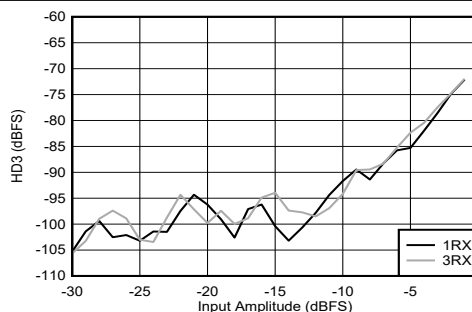
5.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



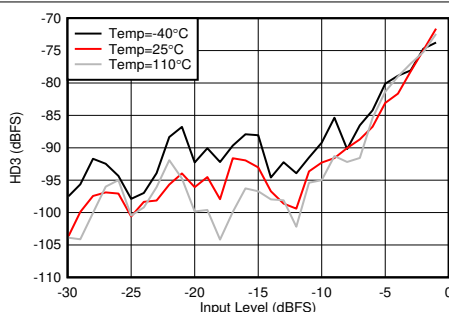
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-384. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



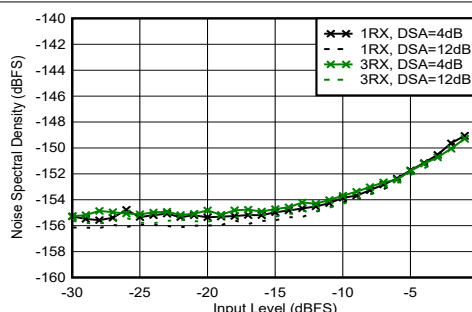
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-385. RX HD3 vs Input Level and Channel at 3.6 GHz



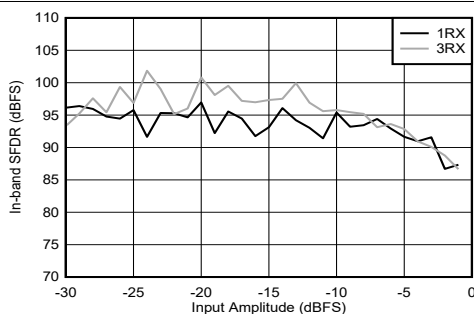
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-386. RX HD3 vs Input Level and Temperature at 3.6 GHz



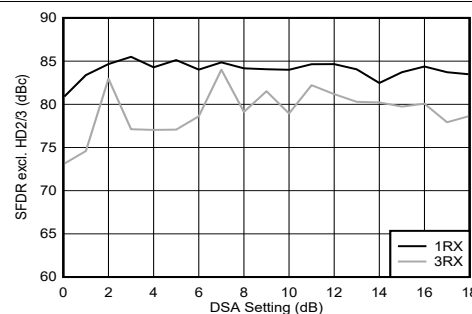
With 3.5 GHz matching, 12.5-MHz offset from tone

FIG 5-387. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

FIG 5-388. RX In-Band SFDR ($\pm 200\text{ MHz}$) vs Input Level and Channel at 3.6 GHz

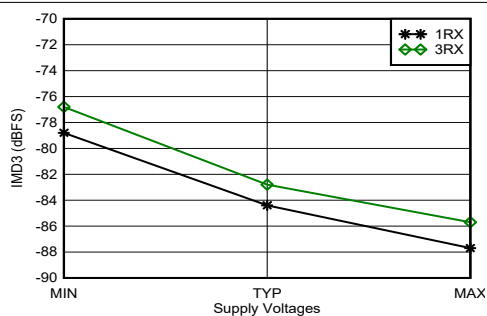


With 3.5 GHz matching

FIG 5-389. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

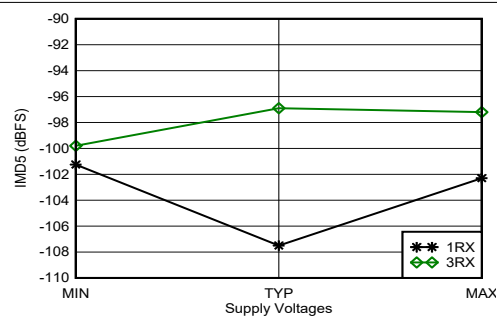
5.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



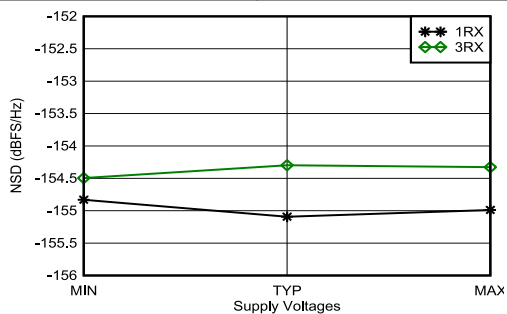
With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-390. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-391. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

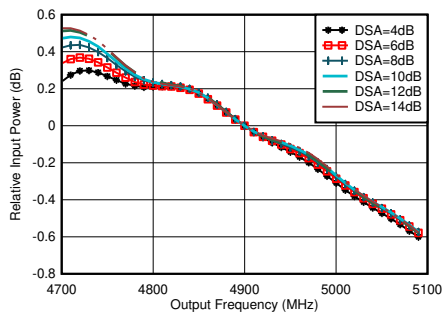


With 3.6 GHz matching, tone at -20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 5-392. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

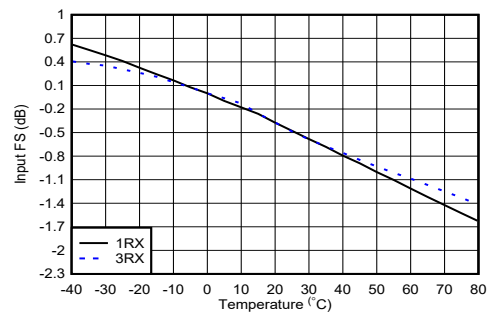
5.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



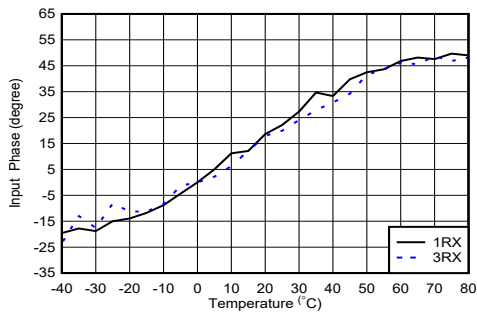
With matching, normalized to power at 4.9GHz for each DSA setting

FIG 5-393. RX Inband Gain Flatness, $f_{\text{IN}} = 4900 \text{ MHz}$



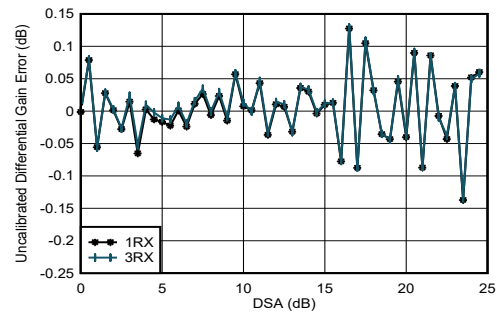
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

FIG 5-394. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

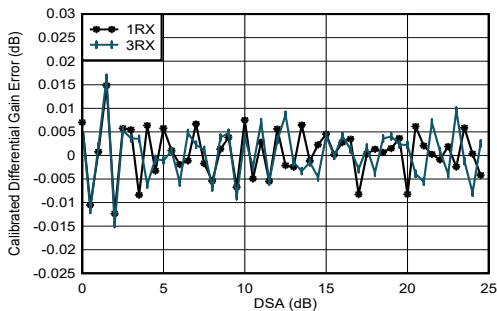
FIG 5-395. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 4.9 \text{ GHz}$



With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

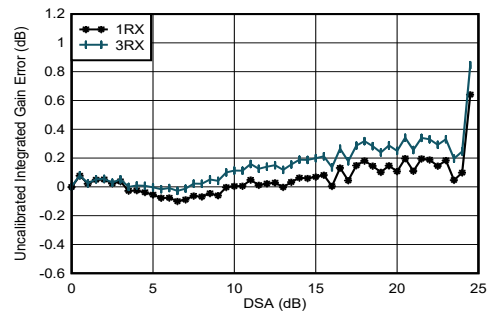
FIG 5-396. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

FIG 5-397. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



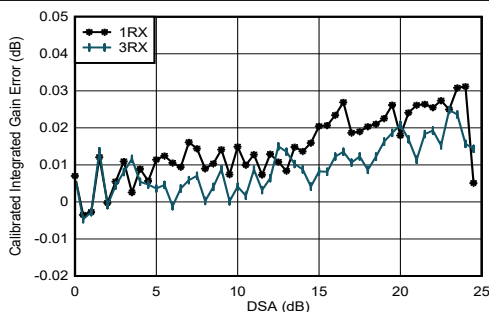
With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

FIG 5-398. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

5.12.12 RX Typical Characteristics at 4.9 GHz (continued)

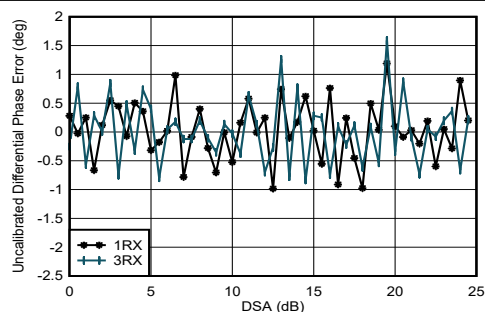
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

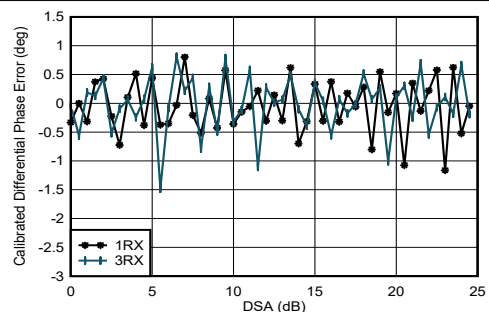
FIG 5-399. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

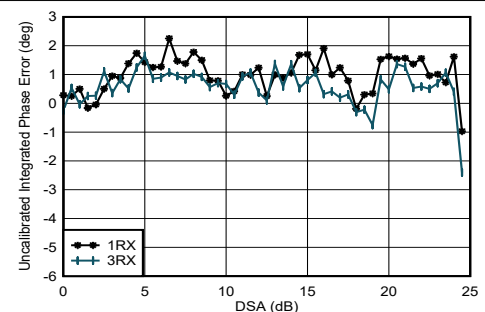
FIG 5-400. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

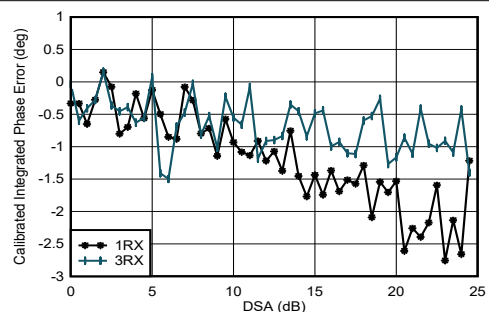
FIG 5-401. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

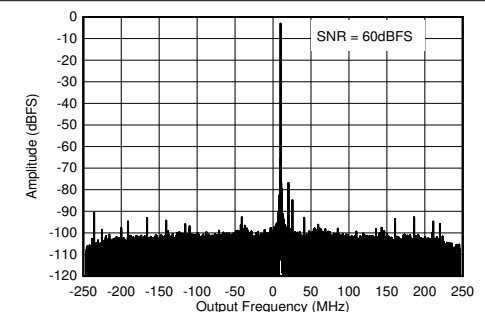
FIG 5-402. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

FIG 5-403. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

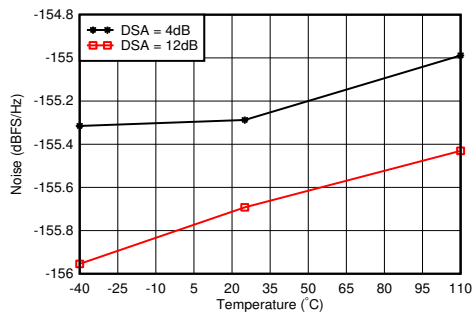


With 4.9 GHz matching, $f_{\text{IN}} = 4910 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

FIG 5-404. RX Output FFT at 4.9 GHz

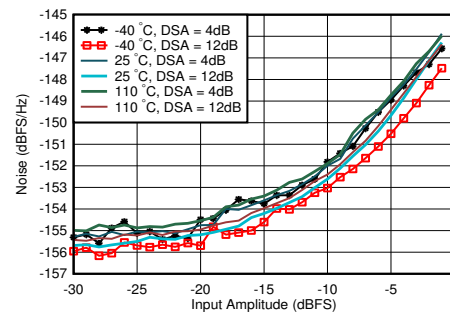
5.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



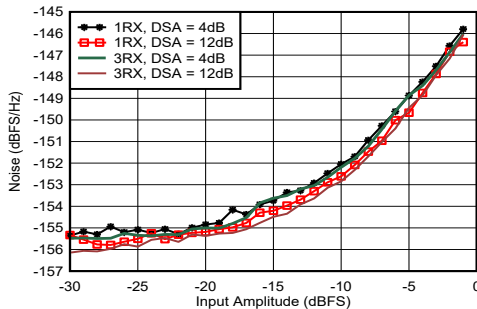
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 5-405. RX Noise Spectral Density vs Temperature at 4.9 GHz



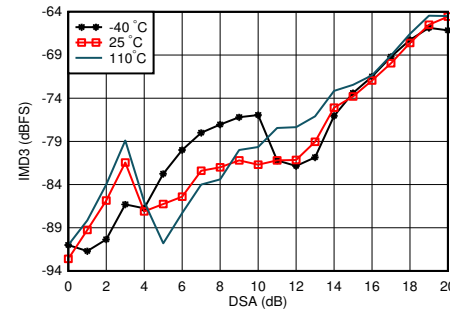
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 5-406. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



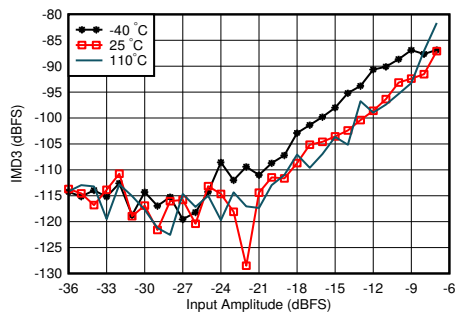
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 5-407. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



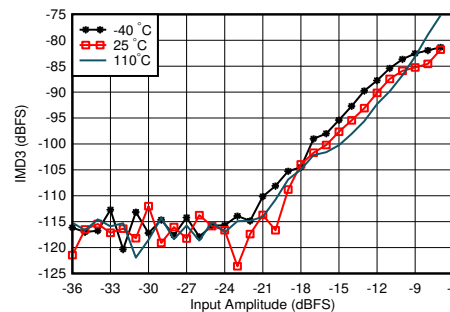
With 4.9 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 5-408. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 5-409. RX IMD3 vs Input Level and Temperature at 4.9 GHz

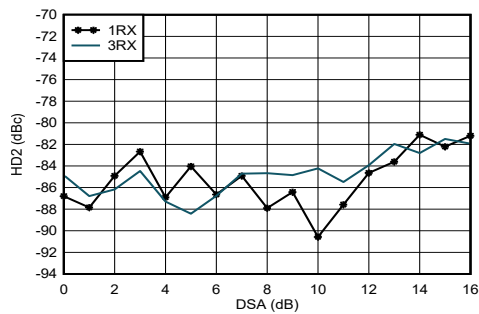


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 5-410. RX IMD3 vs Input Level and Temperature at 4.9 GHz

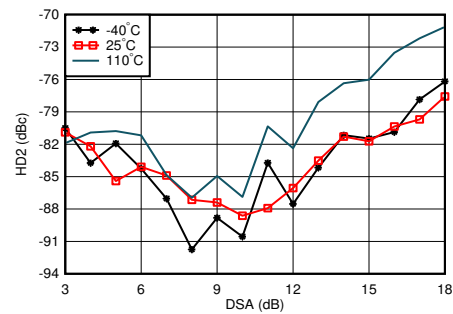
5.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



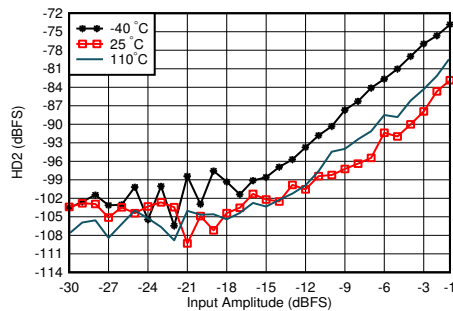
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-411. RX HD2 vs DSA Setting and Channel at 4.9 GHz



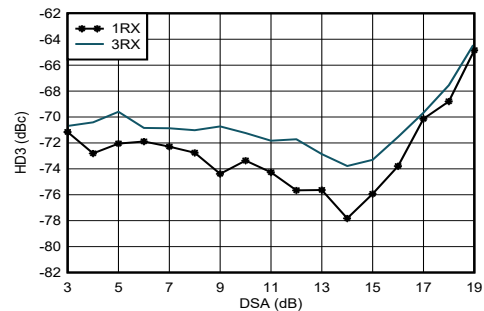
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-412. RX HD2 vs DSA and Temperature at 4.9 GHz



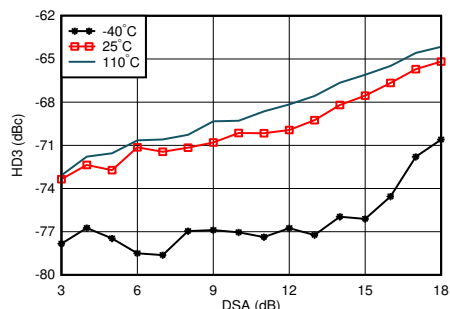
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

FIG 5-413. RX HD2 vs Input Level and Temperature at 4.9 GHz



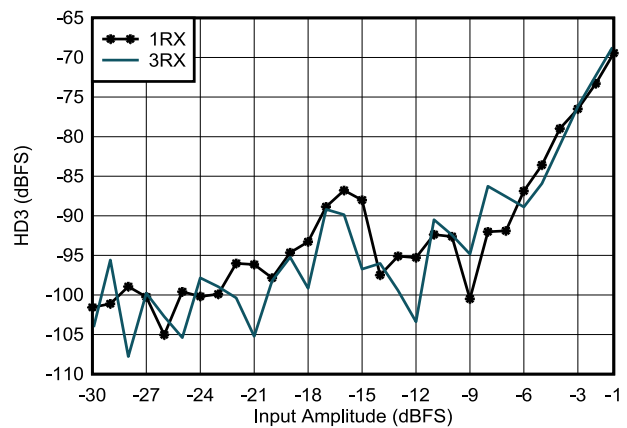
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-414. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-415. RX HD3 vs DSA Setting and Temperature at 4.9 GHz

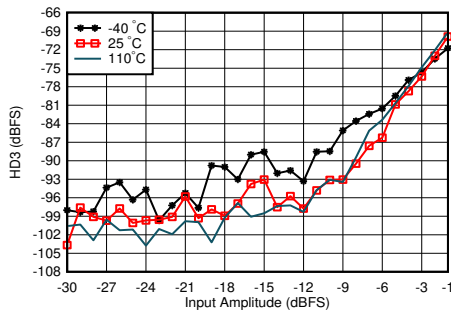


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-416. RX HD3 vs Input Level and Channel at 4.9 GHz

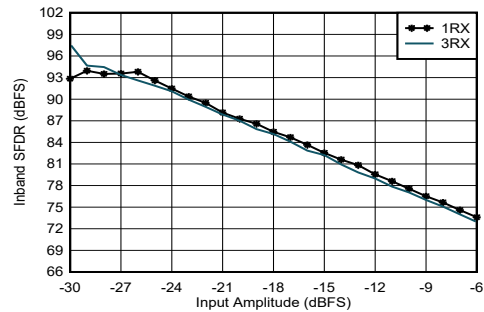
5.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



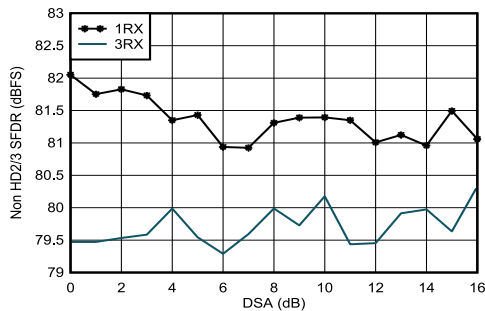
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

FIG 5-417. RX HD3 vs Input Level and Temperature at 4.9 GHz



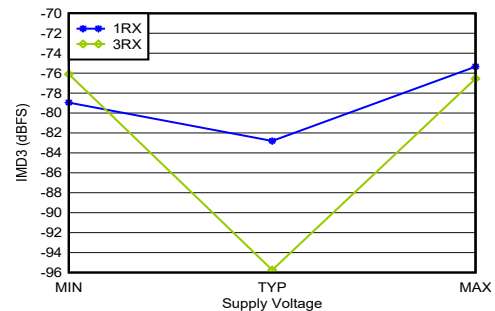
With 4.9 GHz matching, decimate by 3

FIG 5-418. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude and Channel at 4.9 GHz



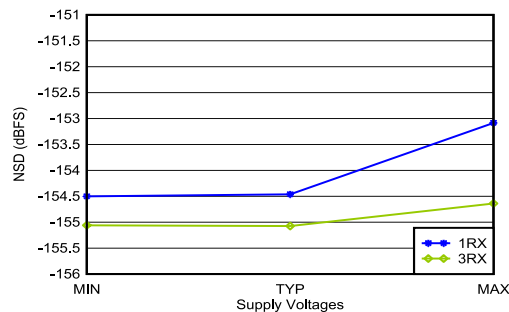
With 4.9 GHz matching

FIG 5-419. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-420. RX IMD3 vs Supply and Channel at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

FIG 5-421. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

5.12.13 RX Typical Characteristics at 8.1GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1GHz matching.

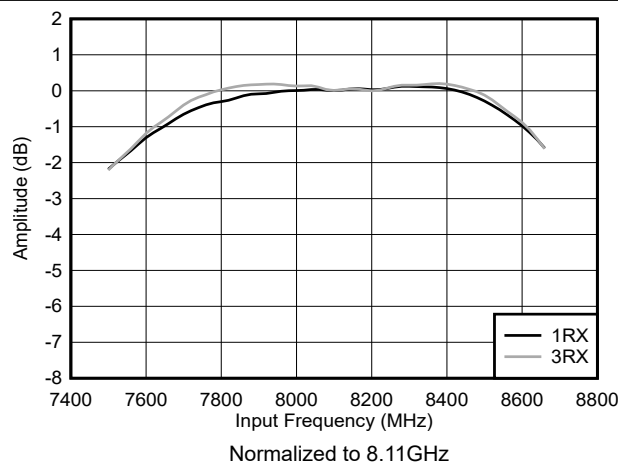


Figure 5-422. RX Amplitude vs Frequency and Channel

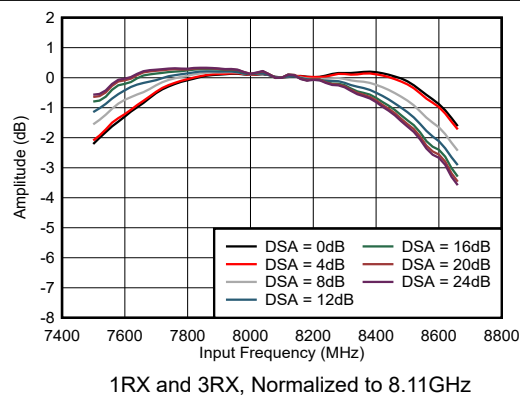


Figure 5-423. RX Amplitude vs Frequency and DSA Setting

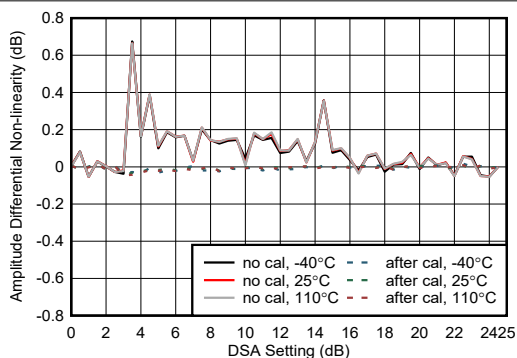


Figure 5-424. RX Amplitude Differential Nonlinearity at 8.11GHz

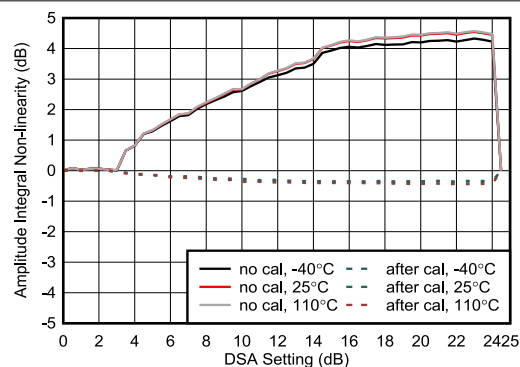


Figure 5-425. RX Amplitude Integrated Nonlinearity at 8.11GHz

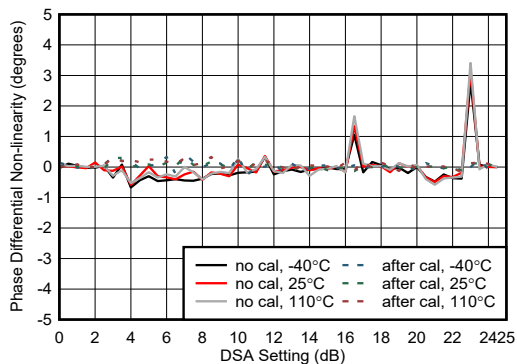


Figure 5-426. RX Phase Differential Nonlinearity at 8.11GHz

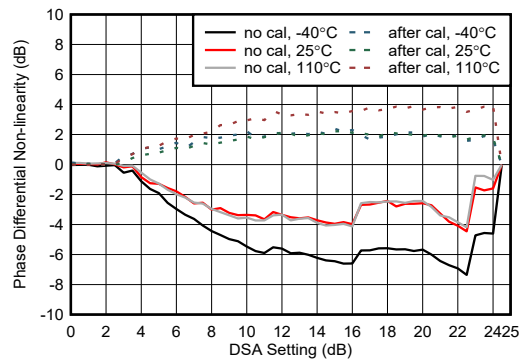


Figure 5-427. RX Phase Differential Nonlinearity at 8.11GHz

5.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1GHz matching.

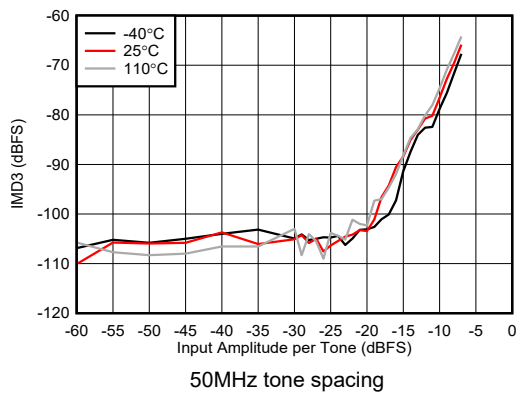


图 5-428. RX IMD3 vs Input Amplitude at 8.1GHz

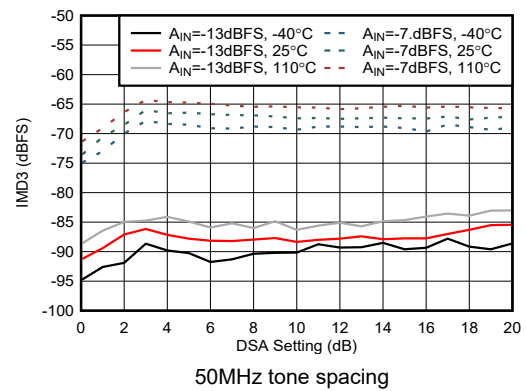


图 5-429. RX IMD3 vs DSA Setting at 8.1GHz

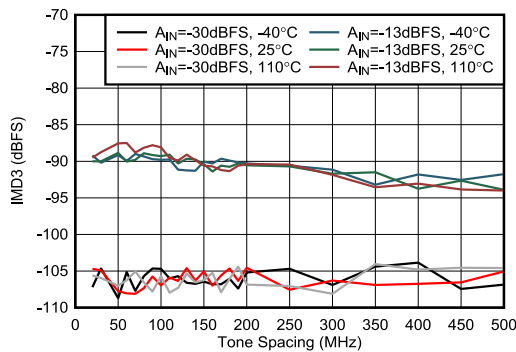


图 5-430. RX IMD3 vs Tone Spacing at 8.1GHz

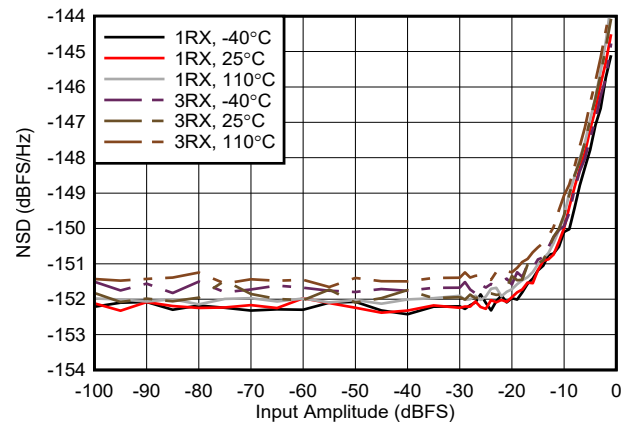


图 5-431. RX NSD vs Digital Amplitude at 8.1GHz

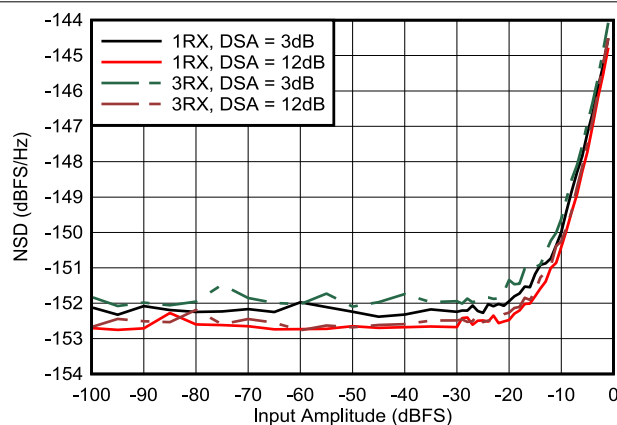


图 5-432. RX NSD vs Digital Amplitude at 8.1GHz

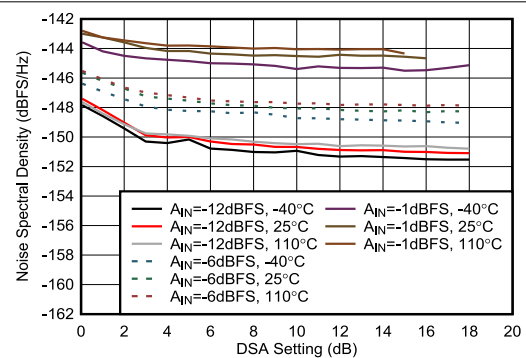


图 5-433. RX NSD vs DSA Setting at 8.1GHz

5.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1GHz matching.

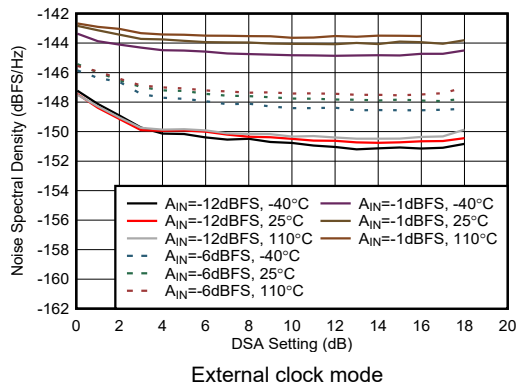


Figure 5-434. RX NSD vs DSA Setting at 8.1GHz

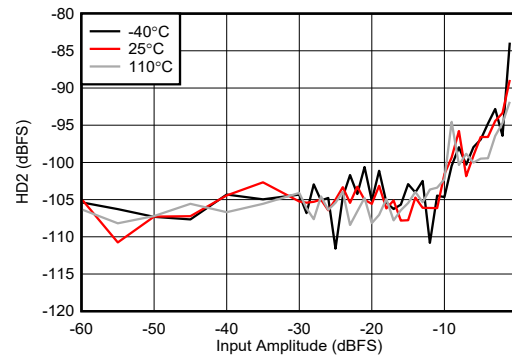


Figure 5-435. RX HD2 vs Digital Amplitude at 8.1GHz

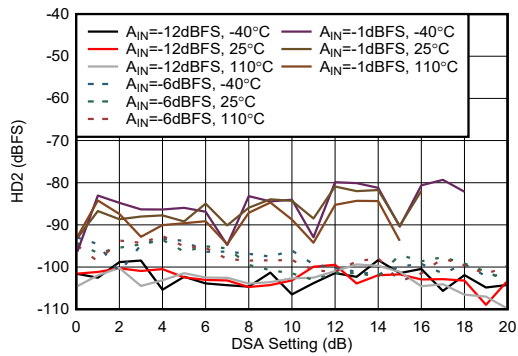


Figure 5-436. RX HD2 vs DSA Setting at 8.1GHz

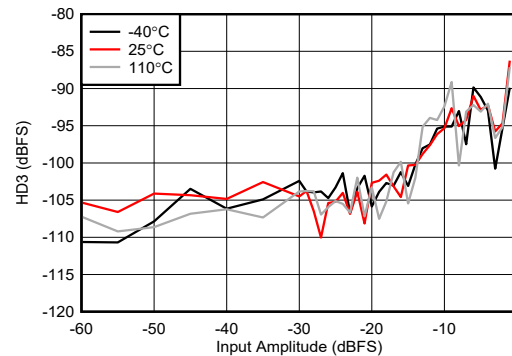


Figure 5-437. RX HD3 vs Digital Amplitude at 8.1GHz

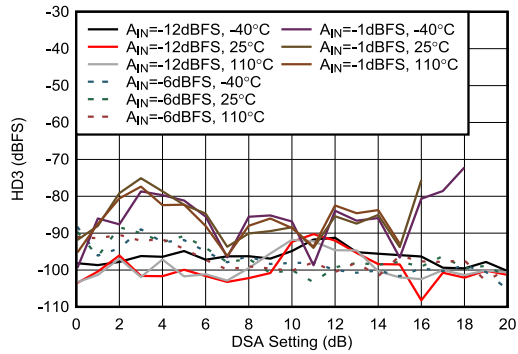


Figure 5-438. RX HD3 vs DSA Setting at 8.1GHz

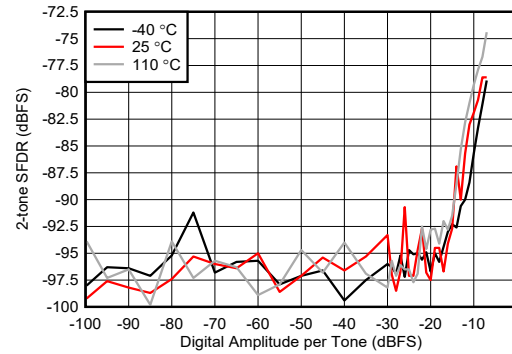


Figure 5-439. RX 2-tone SFDR vs Digital Amplitude at 8.1GHz

5.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1GHz matching.

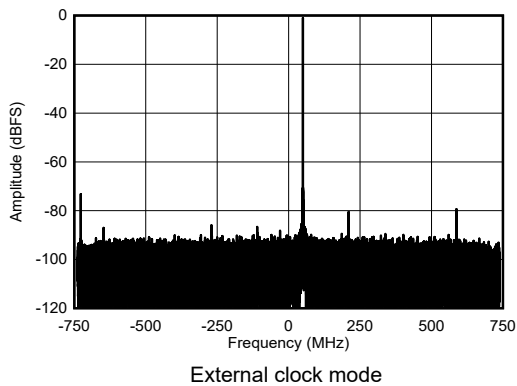


FIG 5-440. RX Single Tone Output FFT at 8.11GHz, -1dBFS

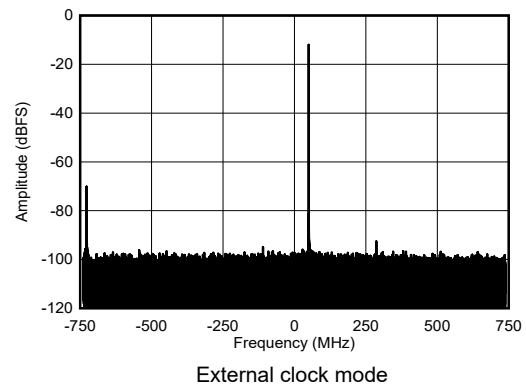


FIG 5-441. RX Single Tone Output FFT at 8.11GHz, -12dBFS

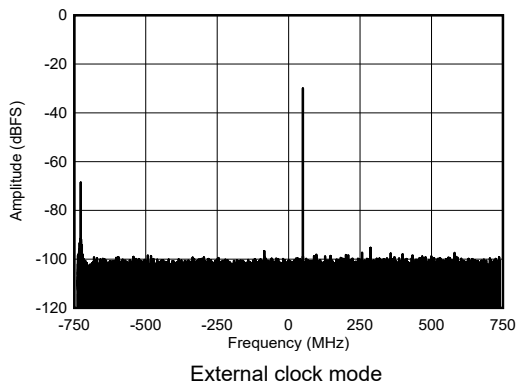


FIG 5-442. RX Single Tone Output FFT at 8.11GHz, -30dBFS

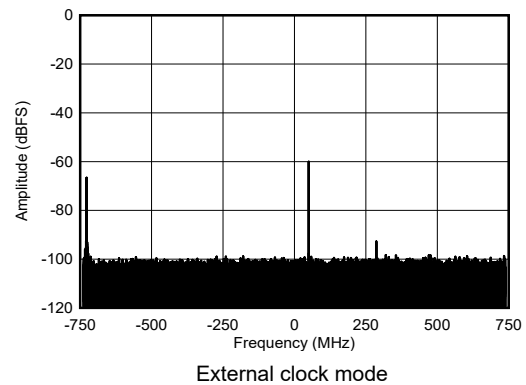


FIG 5-443. RX Single Tone Output FFT at 8.11GHz, -60dBFS

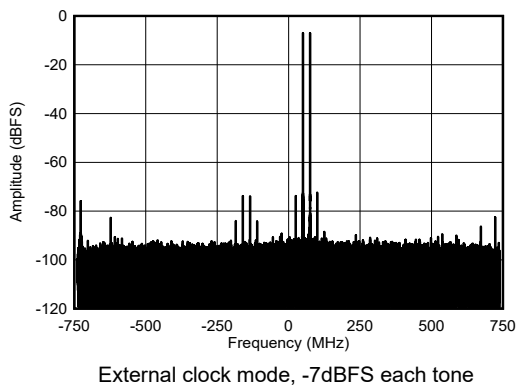


FIG 5-444. RX Dual Tone Output FFT at 8.11GHz

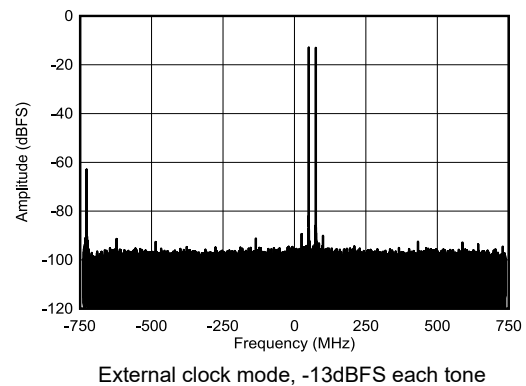
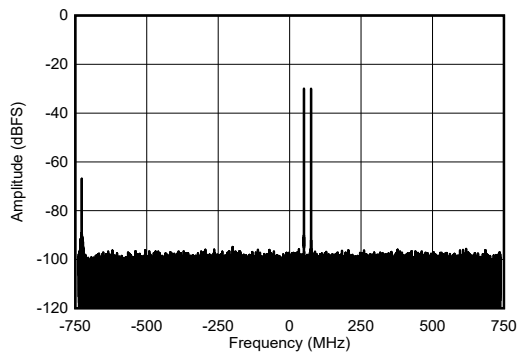


FIG 5-445. RX Dual Tone Output FFT at 8.11GHz

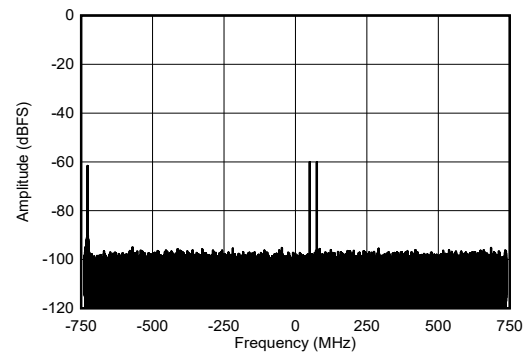
5.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1GHz matching.



External clock mode, -30dBFS each tone

FIG 5-446. RX Dual Tone Output FFT at 8.11GHz

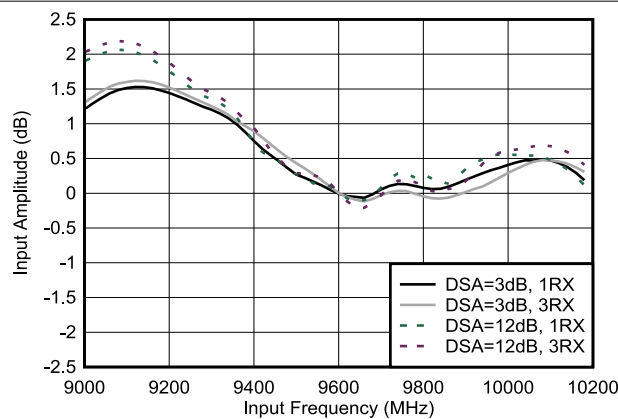


External clock mode, -60dBFS each tone

FIG 5-447. RX Dual Tone Output FFT at 8.11GHz

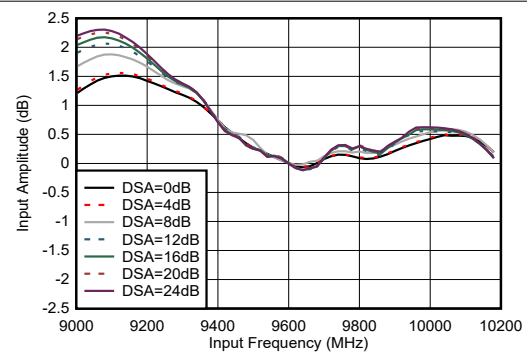
5.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.



Normalized to 9.6 GHz

FIG 5-448. RX Input Amplitude vs Frequency



Normalized to 9.6 GHz

FIG 5-449. RX Input Amplitude vs Frequency at 9.6 GHz

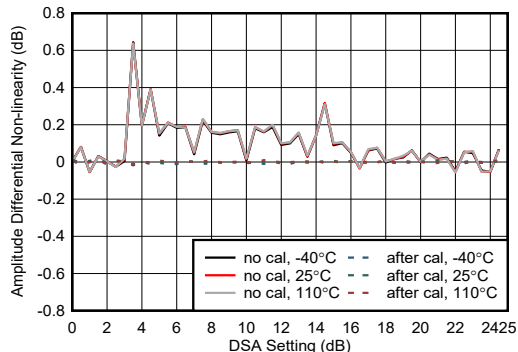


FIG 5-450. RX Amplitude Differential Non-Linearity at 9.6 GHz

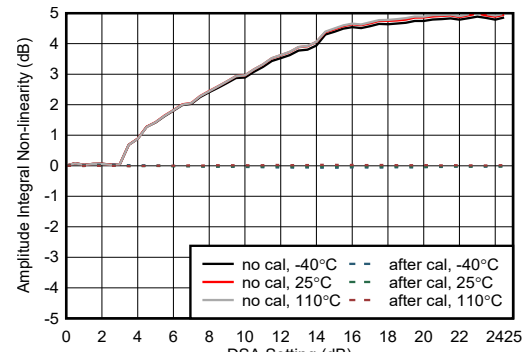


FIG 5-451. RX Amplitude Integrated Non-linearity at 9.6 GHz

5.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.

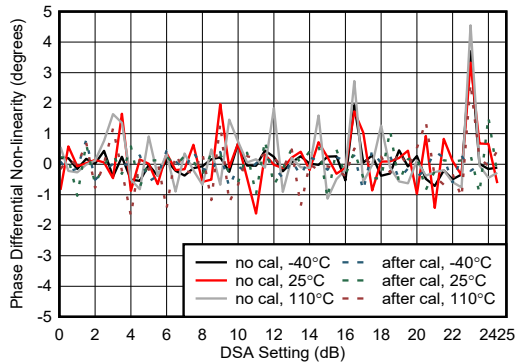


图 5-452. RX Phase Differential Non-linearity at 9.6 GHz

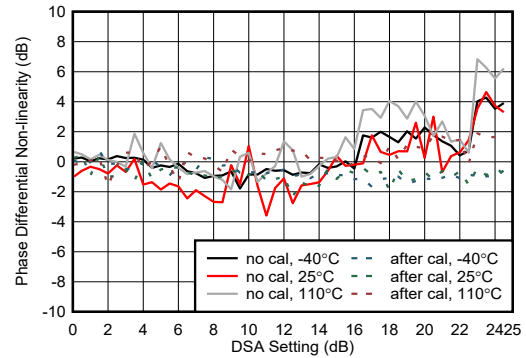


图 5-453. RX Phase Integrated Non-linearity at 9.6 GHz

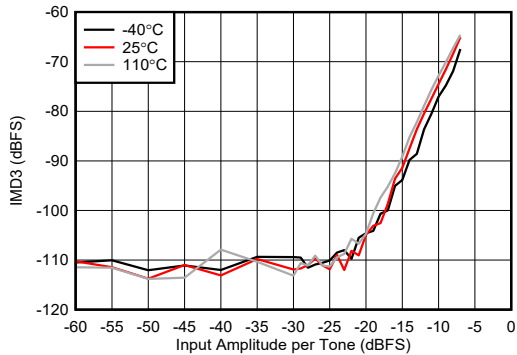


图 5-454. RX IMD3 vs Digital Amplitude at 9.6 GHz

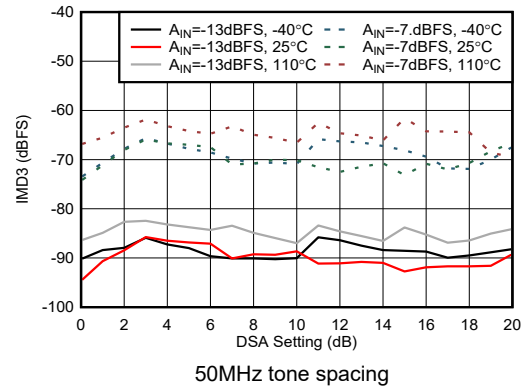


图 5-455. RX IMD3 vs DSA Setting at 9.6 GHz

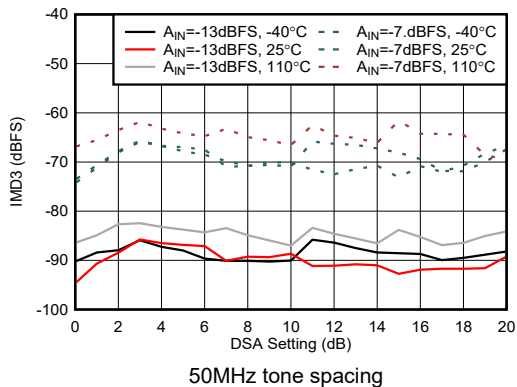


图 5-456. RX IMD3 vs DSA Setting at 9.6 GHz

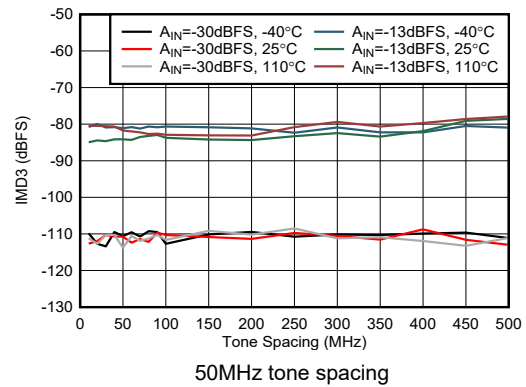


图 5-457. RX IMD3 vs Tone Spacing at 9.6 GHz

5.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.

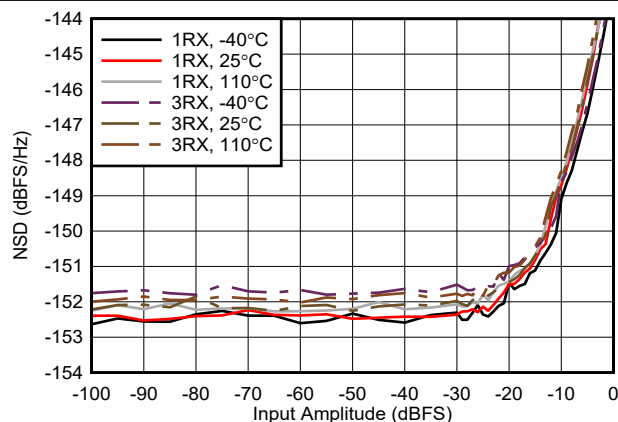


FIG 5-458. RX NSD vs Digital Amplitude at 9.6 GHz

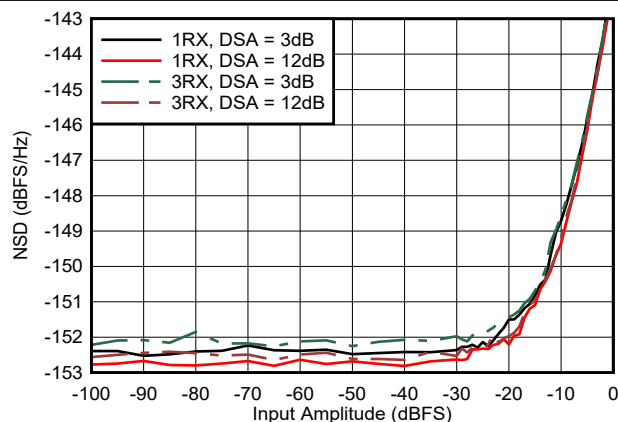


FIG 5-459. RX NSD vs Digital Amplitude at 9.6 GHz

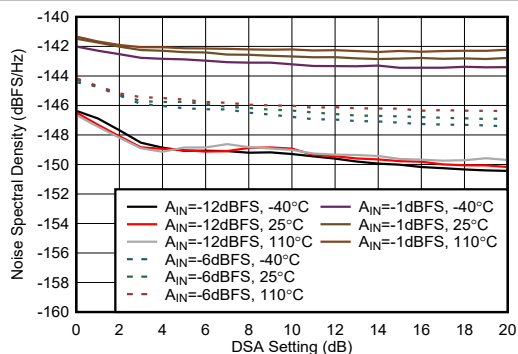


FIG 5-460. RX NSD vs DSA Setting at 9.6 GHz

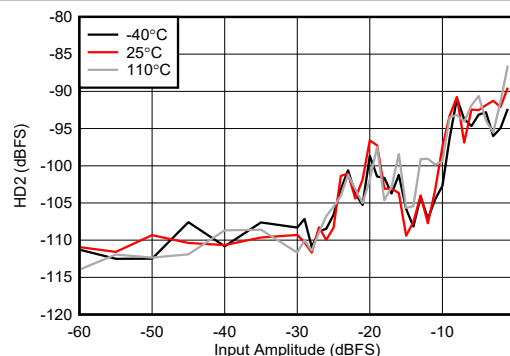


FIG 5-461. RX HD2 vs Digital Level at 9.6 GHz

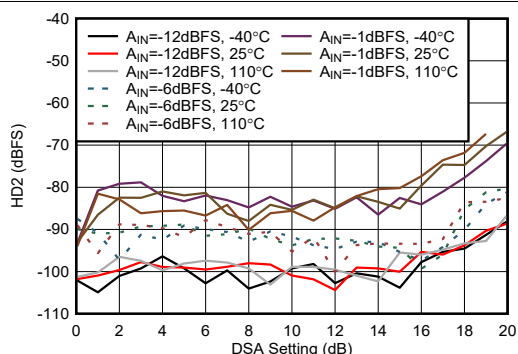


FIG 5-462. RX HD2 vs DSA Setting at 9.6 GHz

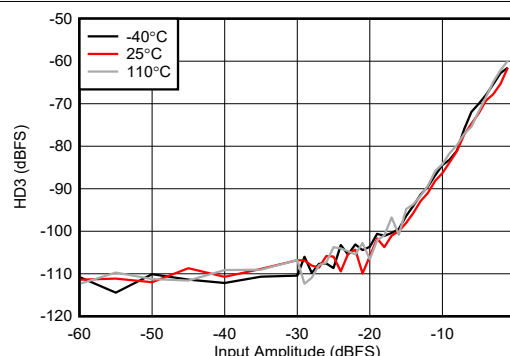


FIG 5-463. RX HD3 vs Digital Level at 9.6 GHz

5.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.

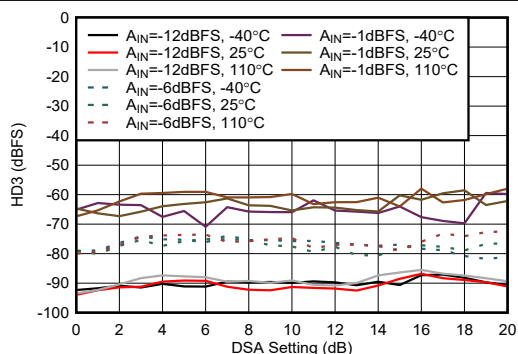
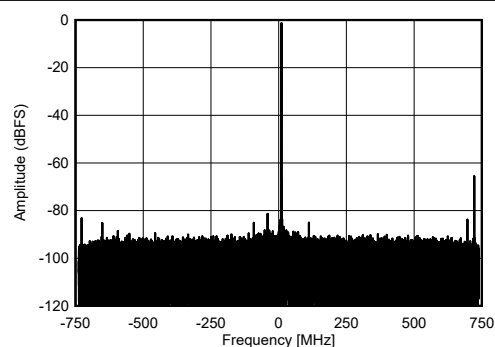
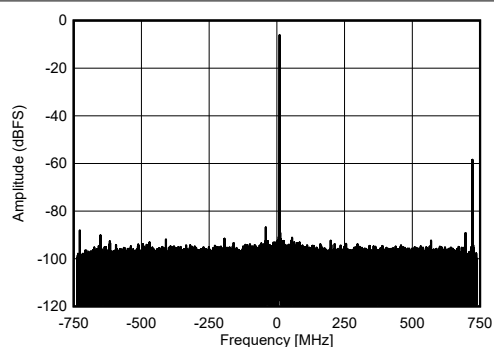


FIG 5-464. RX HD3 vs DSA Setting at 9.6 GHz



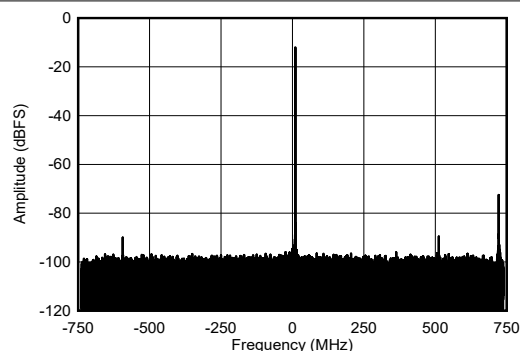
-1 dBFS

FIG 5-465. RX Single Tone Output FFT at 9.61 GHz



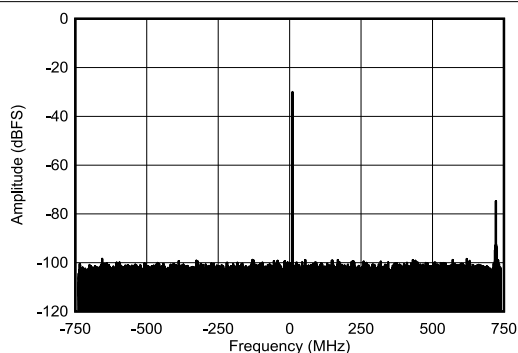
-6 dBFS

FIG 5-466. RX Single Tone Output FFT at 9.61 GHz



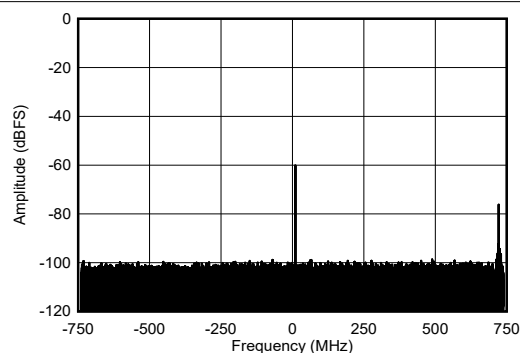
-12 dBFS.

FIG 5-467. RX Single Tone Output FFT at 9.61 GHz



-30 dBFS

FIG 5-468. RX Single Tone Output FFT at 9.61 GHz

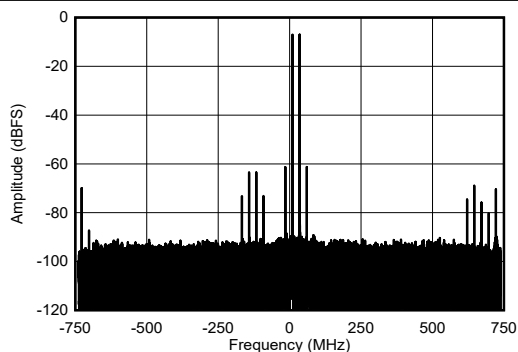


-60 dBFS

FIG 5-469. RX Single Tone Output FFT at 9.61 GHz

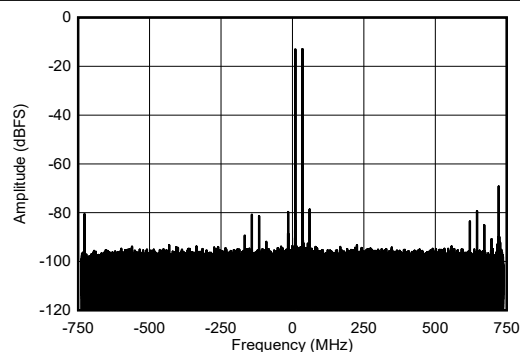
5.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.



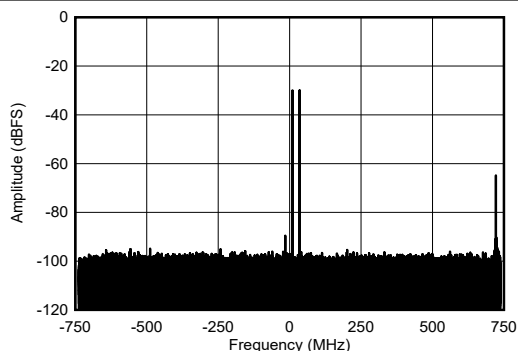
9.61 GHz and 9.635 GHz, -7 dBFS each tone

FIG 5-470. RX Two Tone Output FFT at 9.61 GHz



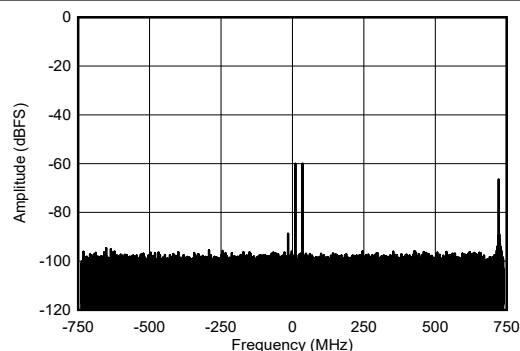
9.61 GHz and 9.635 GHz, -13 dBFS each tone

FIG 5-471. RX Two Tone Output FFT at 9.61 GHz



9.61 GHz and 9.635 GHz, -30 dBFS each tone

FIG 5-472. RX Two Tone Output FFT at 9.61 GHz

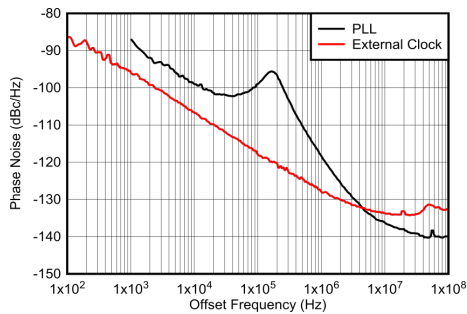


9.61 GHz and 9.635 GHz, -60 dBFS each tone

FIG 5-473. RX Two Tone Output FFT at 9.61 GHz

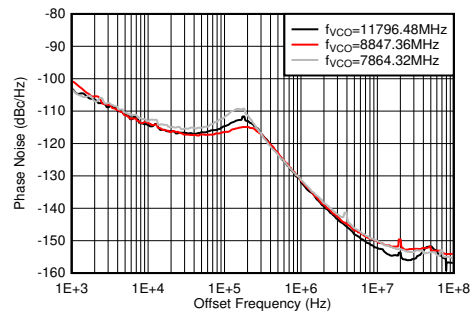
5.12.15 PLL and Clock Typical Characteristics

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, $f_{\text{REF}} = 491.52 \text{ MHz}$, Phase noise measured at TX output



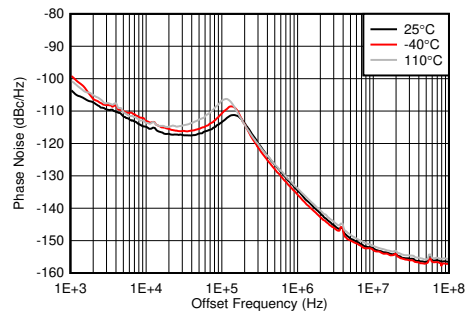
measured at TX output, normalized to 12 GHz by $20 \times \log_{10}(12\text{GHz}/f_{\text{OUT}})$

Figure 5-474. Phase Noise vs Offset Frequency for PLL and External Clock at 12 GHz



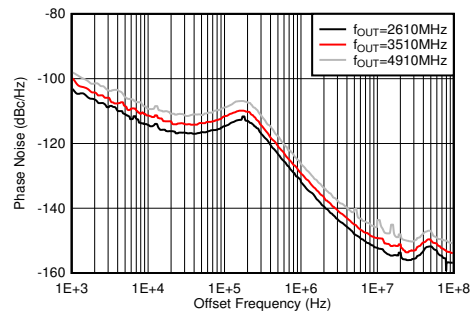
PLL enabled, $f_{\text{REF}} = 491.52 \text{ MSPS}$, measured at TX output

Figure 5-475. Phase Noise vs Offset Frequency and f_{VCO} at $f_{\text{OUT}} = 2610 \text{ MHz}$



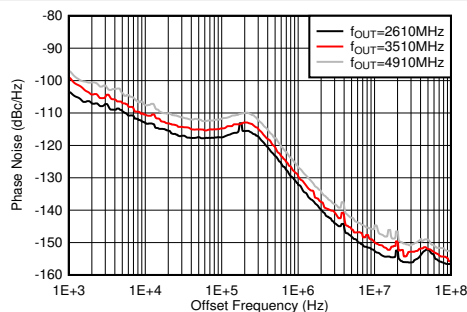
PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52 \text{ MSPS}$, measured at TX output

Figure 5-476. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at $f_{\text{OUT}} = 1910 \text{ MHz}$



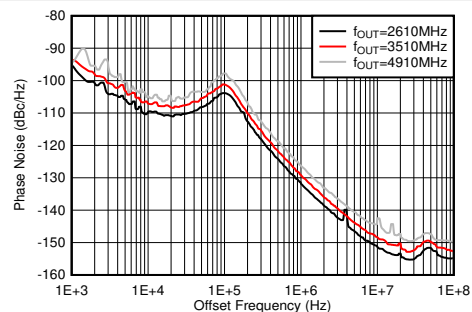
PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52 \text{ MSPS}$, measured at TX output

Figure 5-477. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



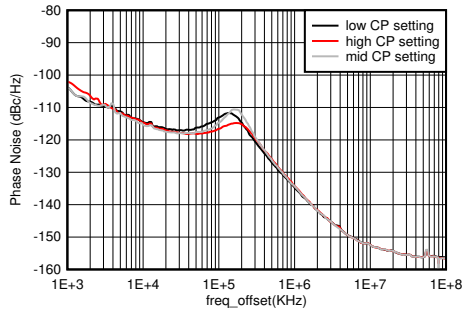
PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52 \text{ MSPS}$, measured at TX output

Figure 5-478. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



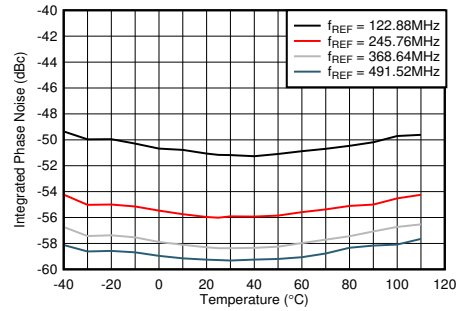
PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52 \text{ MSPS}$, measured at TX output

Figure 5-479. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



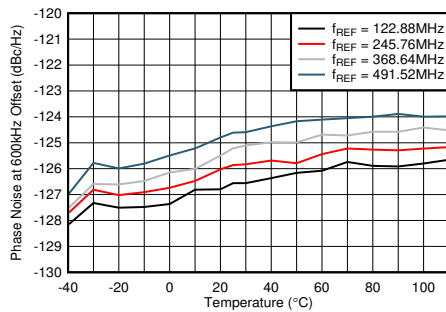
PLL enabled, $f_{VCO} = 11796.48$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-480. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at $f_{OUT} = 2.6$ GHz



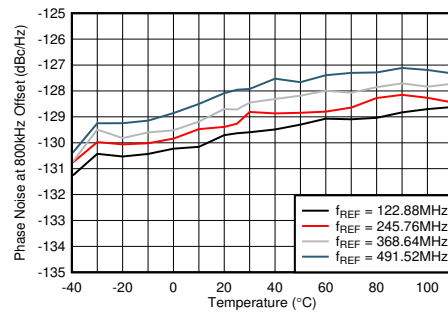
PLL enabled, $f_{VCO} = 11796.48$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

Figure 5-481. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



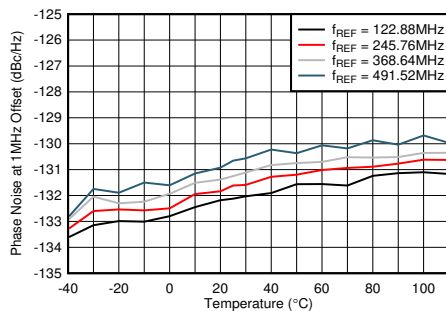
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-482. Phase Noise for 12-GHz VCO at 600 kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



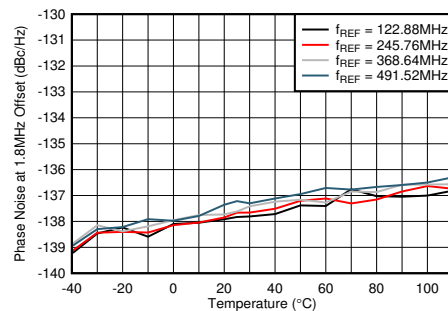
A. PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-483. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



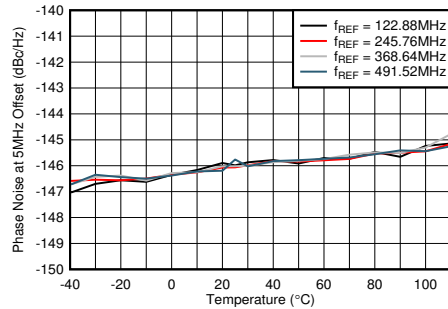
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-484. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



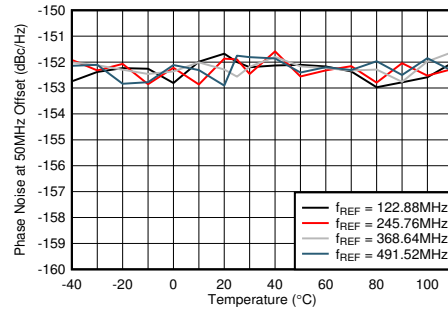
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-485. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



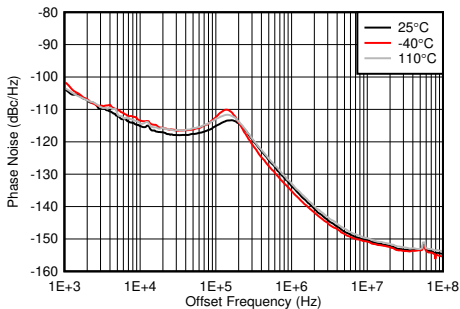
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-486. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



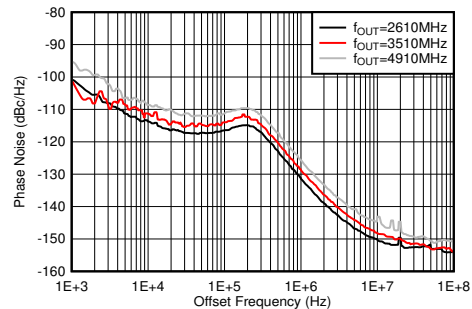
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 5-487. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



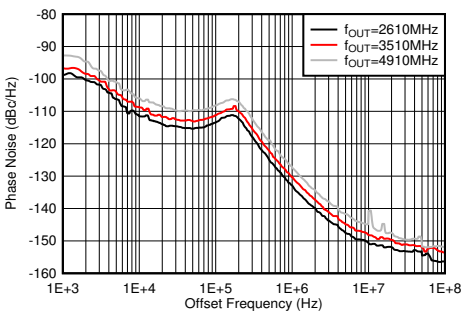
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-488. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



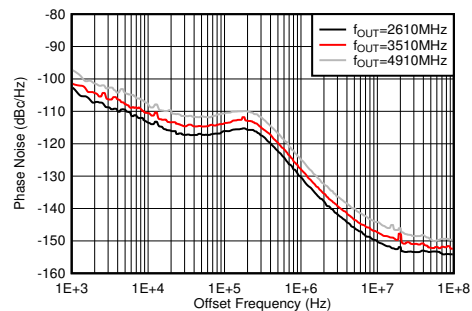
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-489. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



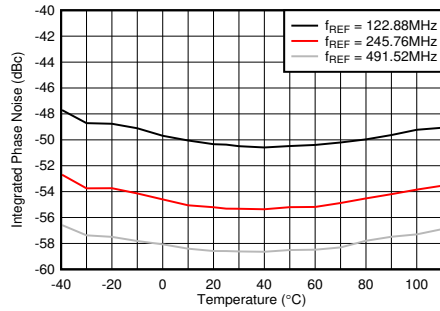
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-490. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



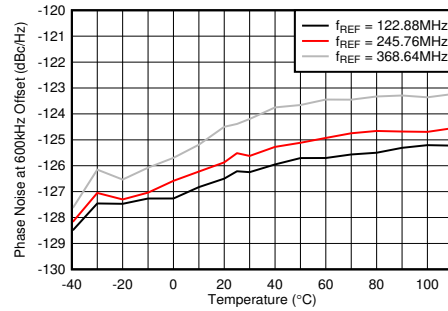
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-491. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



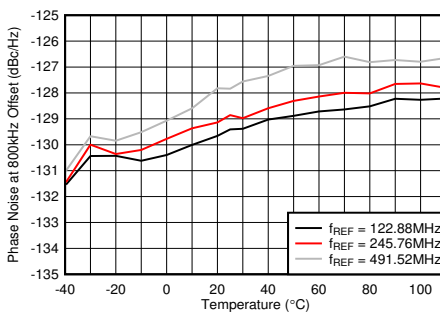
PLL enabled, $f_{VCO} = 9830.4$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

Figure 5-492. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



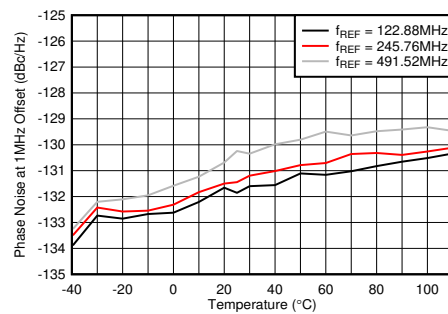
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-493. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



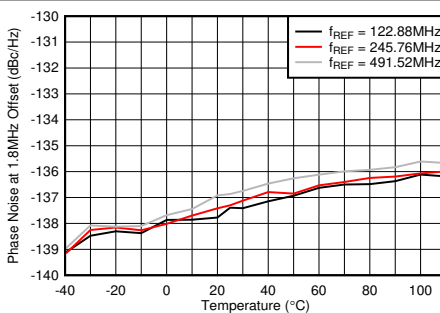
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-494. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



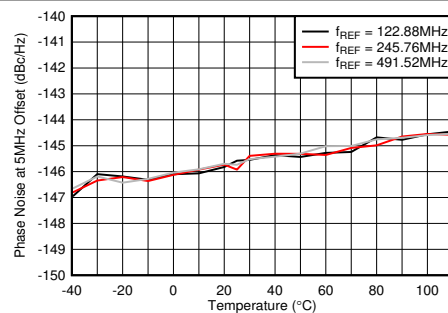
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-495. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



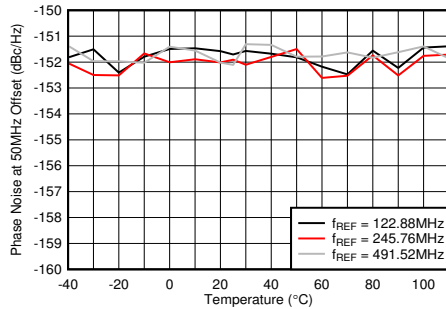
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-496. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



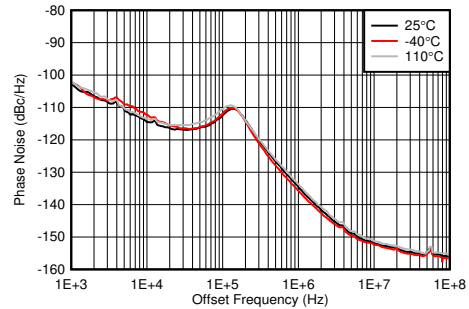
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-497. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



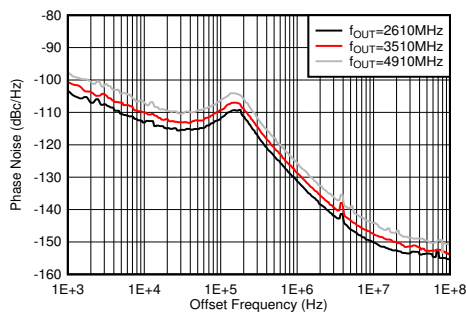
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 5-498. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



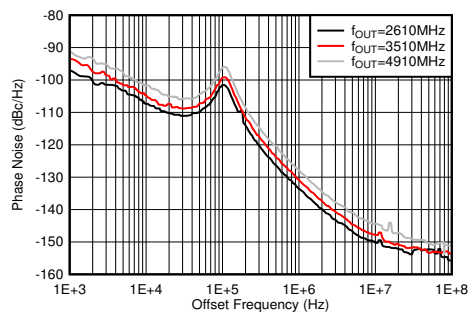
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-499. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



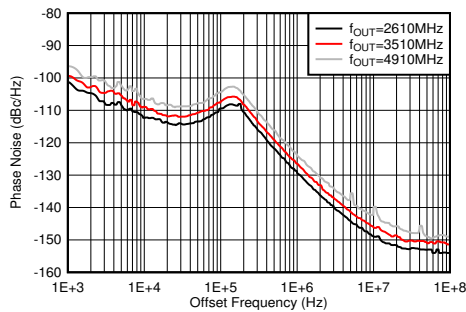
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-500. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



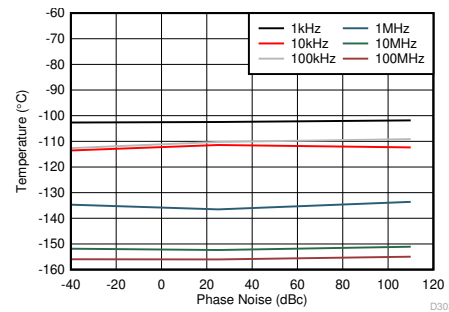
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-501. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



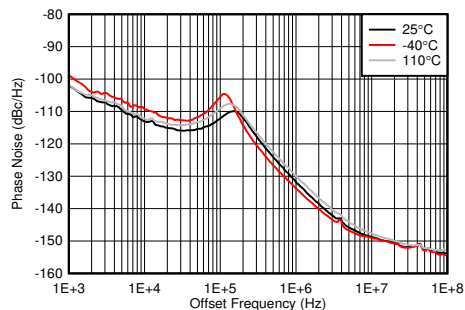
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-502. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, minimum LPF BW, measured at TX output

Figure 5-503. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at $f_{OUT} = 2.6$ GHz



PLL enabled, $f_{VCO} = 7864.32$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 5-504. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz

6 Device and Documentation Support

6.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

6.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

6.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

6.5 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7955IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7955I	Samples
AFE7955IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7955 SNPB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

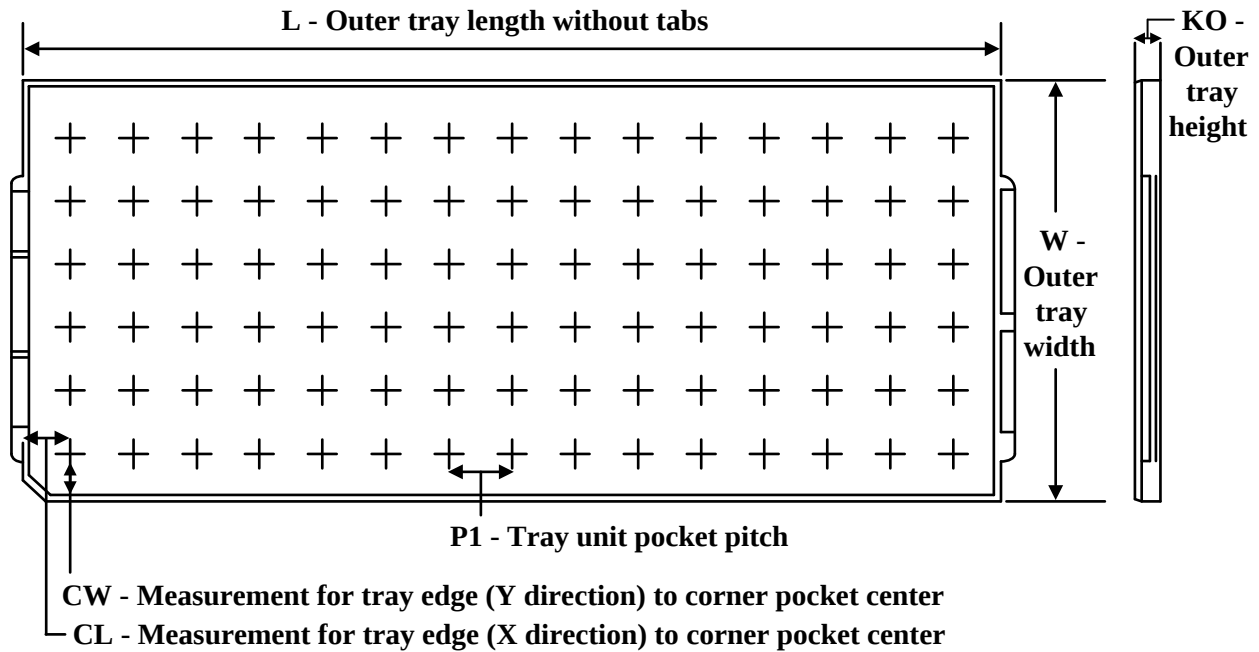
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

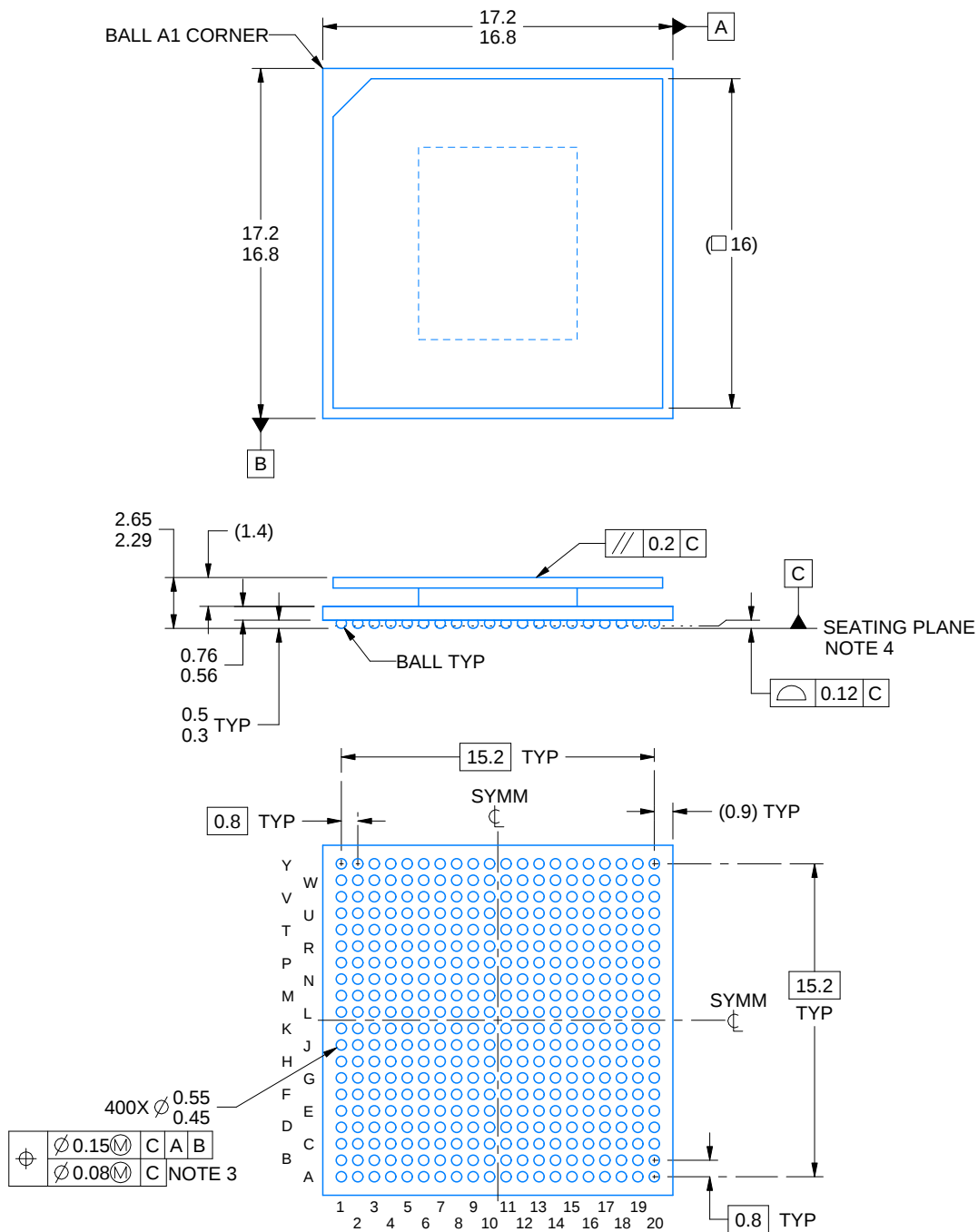
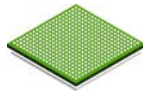
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AFE7955IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7955IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7955IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7955IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



4221311/D 03/2023

NOTES:

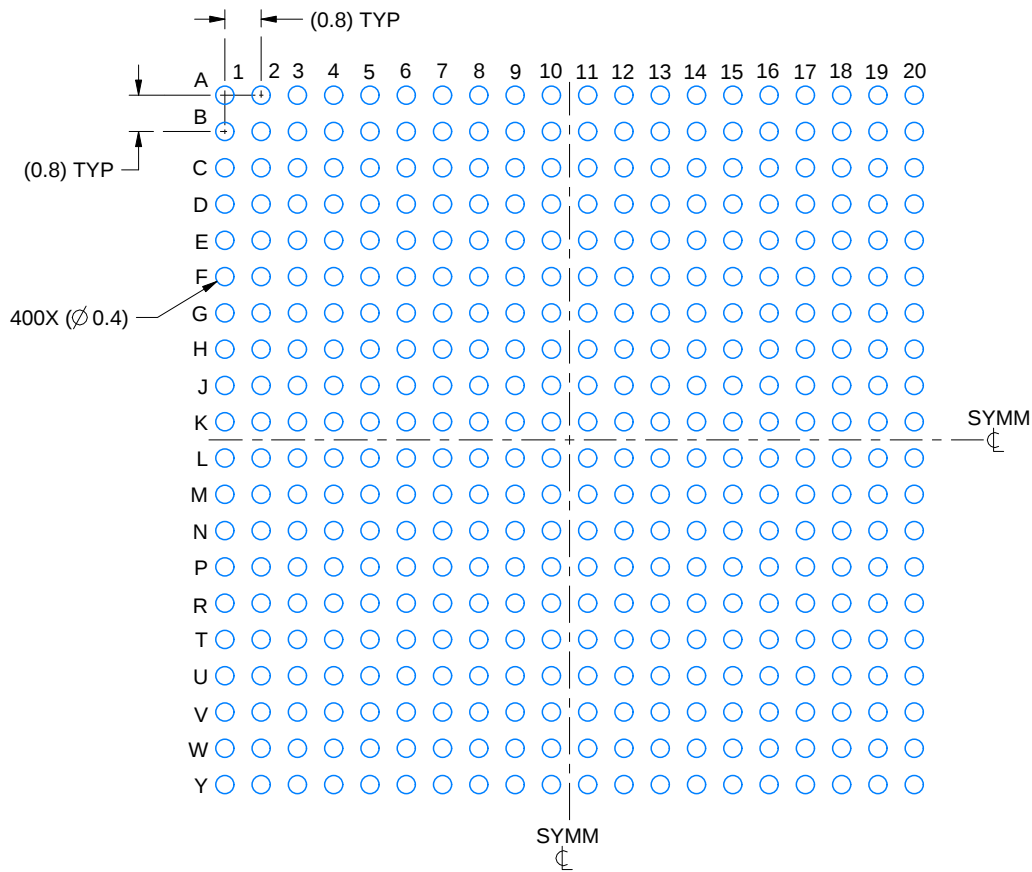
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

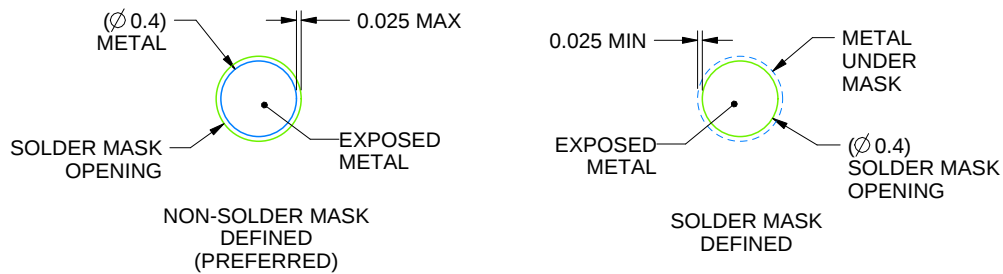
ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

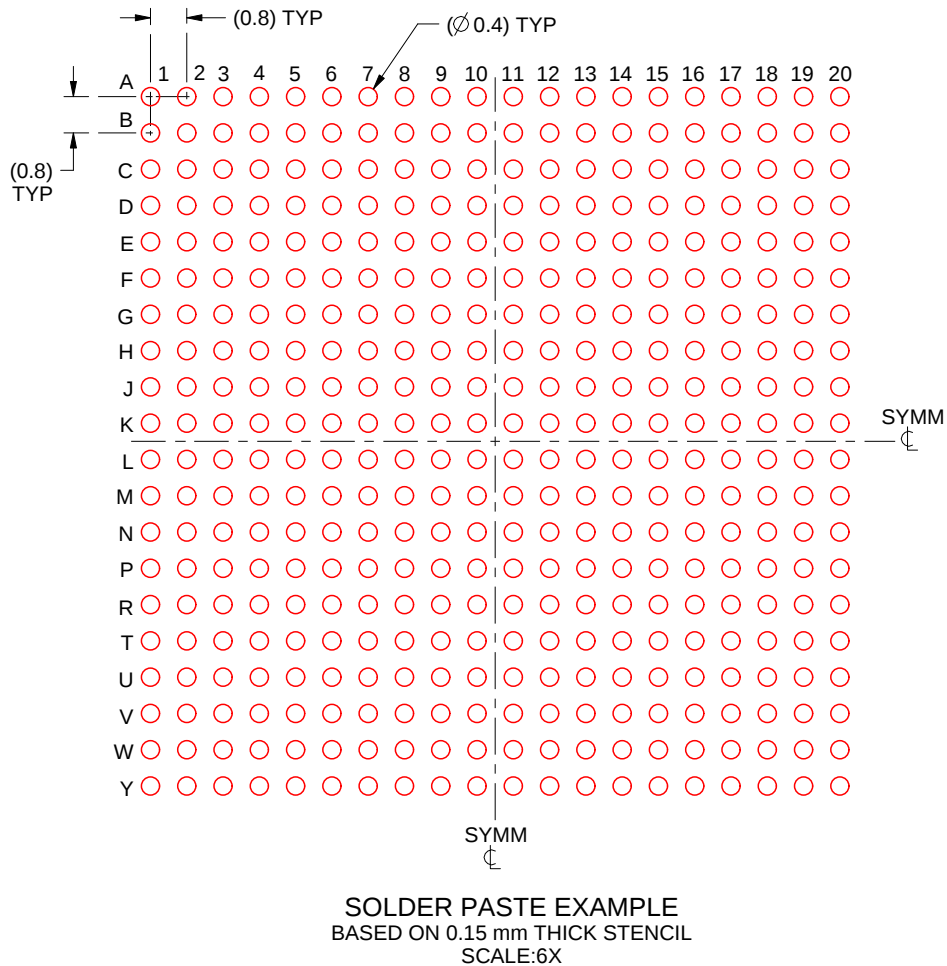
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

FCBGA - 2.65 mm max height

Technical drawing of a 400X ball grid array (BGA) component. The drawing includes three views: a top view showing the overall dimensions (17.2 x 17.2 mm) and a 16x16 grid of balls; a side view showing the component's profile with dimensions for the balls (0.56 mm diameter, 0.3 mm height) and the component body (2.29 mm height); and a bottom view showing the ball pitch (0.5 mm) and the component's footprint. The drawing also includes a table of dimensions and a note about the component's material and finish.

Top View Dimensions:

- Overall width: 17.2 mm
- Overall height: 17.2 mm
- Ball pitch: 0.5 mm
- Grid size: 16x16 balls

Side View Dimensions:

- Component height: 2.29 mm
- Ball diameter: 0.56 mm
- Ball height: 0.3 mm
- Seating plane: NOTE 4

Bottom View Dimensions:

- Ball pitch: 0.5 mm
- Component footprint: 15.2 mm x 15.2 mm
- Ball diameter: 0.5 mm

Table of Dimensions:

Symbol	Value	Unit	Material	Finish
50	0.5	mm	C	A
18	0.5	mm	C	B

Note 3: 400X 0.55 0.45

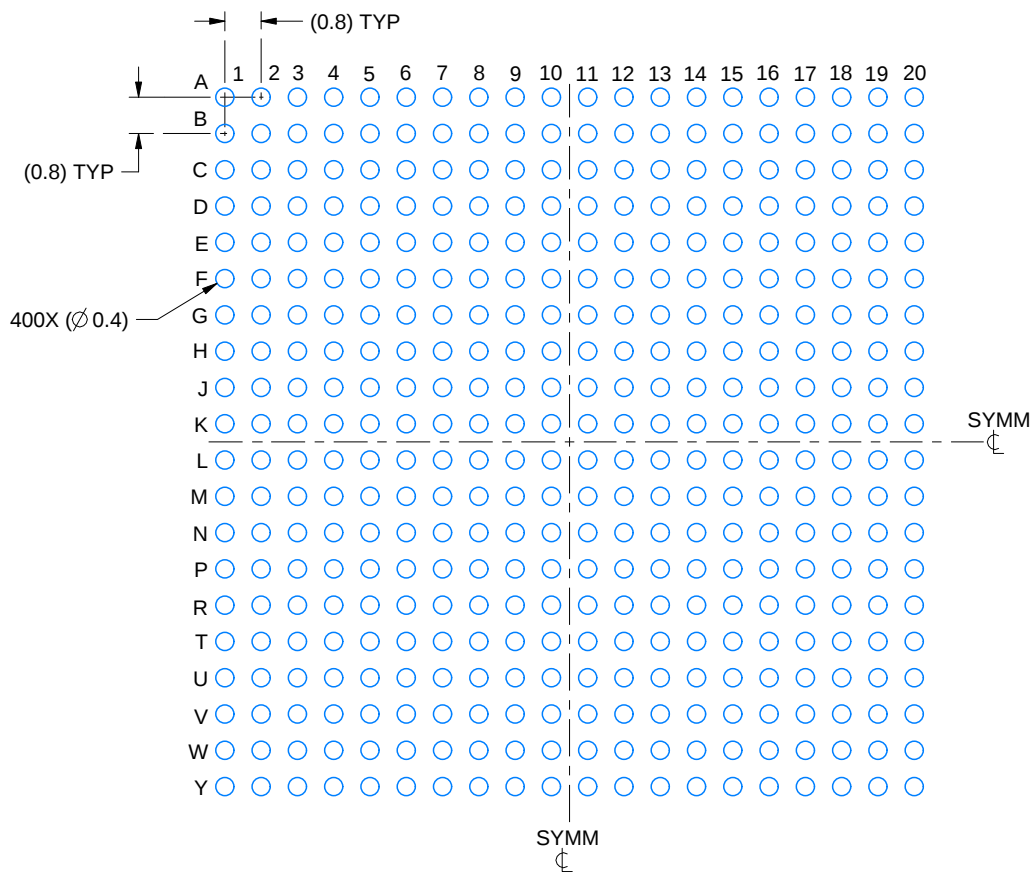
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

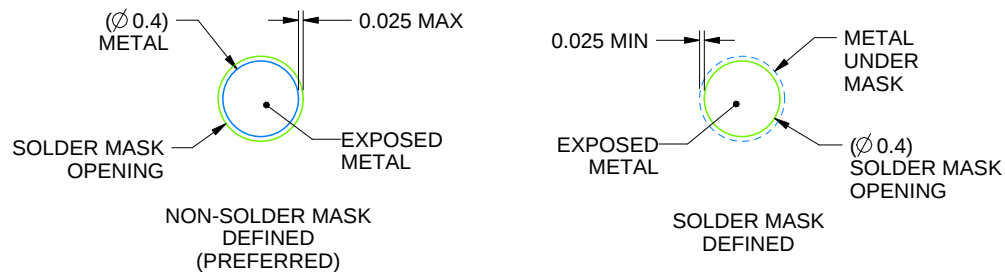
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

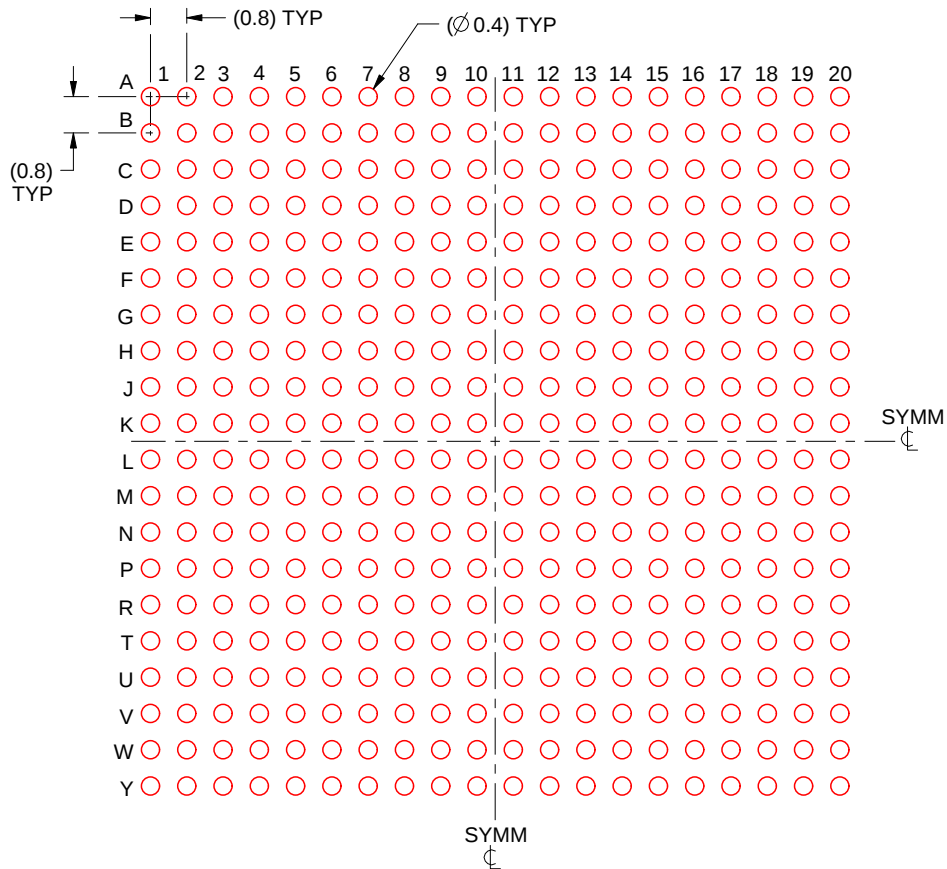
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated