AWRL1432
JAJSQU7A – JULY 2023 – REVISED FEBRUARY 2024

AWRL1432 シングル・チップ 76～81GHz 車載用レーダー・センサ

1 特長

- FMCW トランシーバ
  - PLL、トランスミッタ、レシーバ、ベースバンド、ADC を内蔵
  - 76GHz～81GHz の範囲に対応、5GHz の連続帯域幅
  - 3 つの受信チャネルと 2 つの送信チャネル
  - 短距離
  - Tx あたり 11dBm の出力電力 (標準値)
  - 14.5dB のノイズ指数 (標準値)
  - 1MHz で -89dBc/Hz の位相ノイズ (標準値)
  - FMCW の動作
  - 5MHz IF 帯域幅、実数のみの Rx チャネル
  - フラクショナル N PLL を使用した超高精度のチャープ エンジン
  - トランスミッタごとのバイナリ位相シフタ
- 処理部品
  - 単精度 FPU (160MHz) を搭載した Arm® M4F® コア
  - テキサス･インスツルメンツのレーダー ハードウェア アクセラレータ (HWA 1.2)、FFT、対数振幅、CFAR 動作 (80MHz) 用
- 複数の低消費電力モードをサポート
  - アイドル モードとディープ スリープ モード
- パワー マネージメント
  - 1.8V および 3.3V IO のサポート
  - 内蔵 LDO ネットワークにより PSRR の向上を実現
  - BOM 最適化モードと電力最適化モード
  - 1.8V IO モード用の 1 つまたは 2 つの電源レール、3.3V IO モード用の 2 つまたは 3 つの電源レール
- FCCSP デバイスのパッケージ サイズ：6.45mm × 6.45mm
- 較正および自己テストを内蔵
  - 内蔵ファームウェア (ROM)
  - 自己完結型のオンチップ較正システム
- ホスト インターフェイス
  - UART
  - CAN-FD
  - SPI
  - LIN
- RDIF (レーダー データ インターフェイス)、未加工 ADC サンプル キャプチャ用
- ユーザー アプリケーションで利用可能なその他のインターフェイス
  - QSPI
  - I2C
  - JTAG
  - GPIO
  - PWM インターフェイス
- 内部メモリ
  - 1MB のオンチップ RAM
  - レーダー キューブ用の構成可能な L3 共有メモリ
  - データおよびコード RAM (512/640/768KB)
- 機能安全準拠予定
  - 機能安全アプリケーション向けに開発
  - ASIL B までを対象とするハードウェア インテグリティ
- 12 x 12、102 BGA ボールの FCCSP パッケージ
- AEC Q-100 認定済み
- クロック ソース
  - プライマリ クロック用の 40.0MHz 水晶振動子
  - 40.0MHz の外部駆動クロック (方形波 / 正弦波) をサポート
  - 低消費電力動作用 32kHz 内部発振器
- 動作時の温度範囲対応
  - 動作時の接合部温度範囲：-40℃～125℃

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2 アプリケーション

- キック・ツー・オープン (ブート)
- 自動パーキング機能
- カー・ドア・オープナー
- クロス・トラフィック・アシスト (フロント)
- 死角検出
- 車線変更支援

3 概要

AWRL1432 ミリ波センサ デバイスは、FMCW レーダー テクノロジーをベースとする統合型シングル チップ ミリ波センサです。このデバイスは 76GHz～81GHz の帯域で動作でき、主に 4 つの電源ドメインに区分されています。

- **RF / アナログ サブシステム**:このブロックには、RF 信号の送受信に必要なすべての RF およびアナログ コンポーネントが含まれています。
- **フロント エンド コントローラ サブシステム (FECSS)**:FECSS には、レーダー フロント エンドの構成、制御、較正を担当するプロセッサが含まれています。
- **アプリケーション サブシステム (APPSS)**:APPSS には、ユーザーによるプログラムが可能な ARM Cortex M4 が実装されており、カスタム制御や車載用インターフェイス アプリケーションに使用できます。トップ サブシステム (TOPSS) は、APPSS 電源ドメインの一部であり、クロッキングおよびパワー マネージメント サブブロックを含んでいます。
- **ハードウェア アクセラレータ (HWA)**:HWA ブロックは、FFT、CFAR (Constant False Alarm Rate、一定誤警報率)、スケーリング、圧縮などの一般的なレーダー処理を負荷分担して、APPSS を補完します。

AWRL1432 は、使用事例の要件に基づいて状態 (電源オンまたはオフ) を制御するために、上記の各電源ドメインに対して個別のノブを備えています。このデバイスにはスリープやディープ スリープなどのさまざまな低消費電力状態を実行する機能もあり、クロック ゲーティングによって、また、デバイスの内部 IP ブロックをオフにすることによって、低消費電力のスリープ モードを実現しています。このデバイスでは、そのようなシナリオで保持されるアプリケーション イメージや RF プロファイルなど、デバイスの一部の内容を保持することもできます。

さらに、このデバイスは、テキサス・インスツルメンツの低消費電力 45nm RF CMOS プロセスで製造され、超小型の外形で、かつてないレベルの統合を実現しています。AWRL1432 は、死角検出、キック ツー オープン、駐車支援、ドア障害物検出などのアプリケーションのために、車載分野での低消費電力、自己監視機能付き、超高精度レーダー システム向けに設計されています。

パッケージ情報

部品番号(1)	パッケージ	本体サイズ(2)	トレイ / テープ アンド リール	説明
XA1432ADQGAMF	AMF (FCCSP、102)	6.45mm × 6.45mm		量産試作 ES1.1 。低消費電力ディープ スリープ有効
XA1432BDBAAMF	AMF (FCCSP、102)	6.45mm × 6.45mm		量産試作 ES2.0 。ASIL-B 対応予定低消費電力ディープ スリープ有効認証済みブート
AWRL1432BDBGAMFRQ1	AMF (FCCSP、102)	6.45mm × 6.45mm	テープ アンド リール	車載用製品バリアント。ASIL-B 対応予定ディープスリープ有効。大量。
AWRL1432BDBGAMFQ1	AMF (FCCSP、102)	6.45mm × 6.45mm	トレイ	車載用製品バリアント。ASIL-B 対応予定ディープスリープ有効。少量。
AWRL1432BDBAAMFRQ1	AMF (FCCSP、102)	6.45mm × 6.45mm	テープ アンド リール	車載用製品バリアント。ASIL-B 対応予定ディープスリープ有効。認証済みブート大量。

パッケージ情報 (続き)

部品番号(1)	パッケージ	本体サイズ(2)	トレイ / テープ アンド リール	説明
AWRL1432BDBAAMFQ1	AMF (FCCSP、102)	6.45mm × 6.45mm	トレイ	車載用製品バリアント。ASIL-B 対応予定ディープスリープ有効。認証済みブート大量。

(1) 詳細については、を参照してください。セクション 12
(2) 詳細については、を参照してください。セクション 10.1

ADVANCE INFORMATION

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4 機能ブロック図

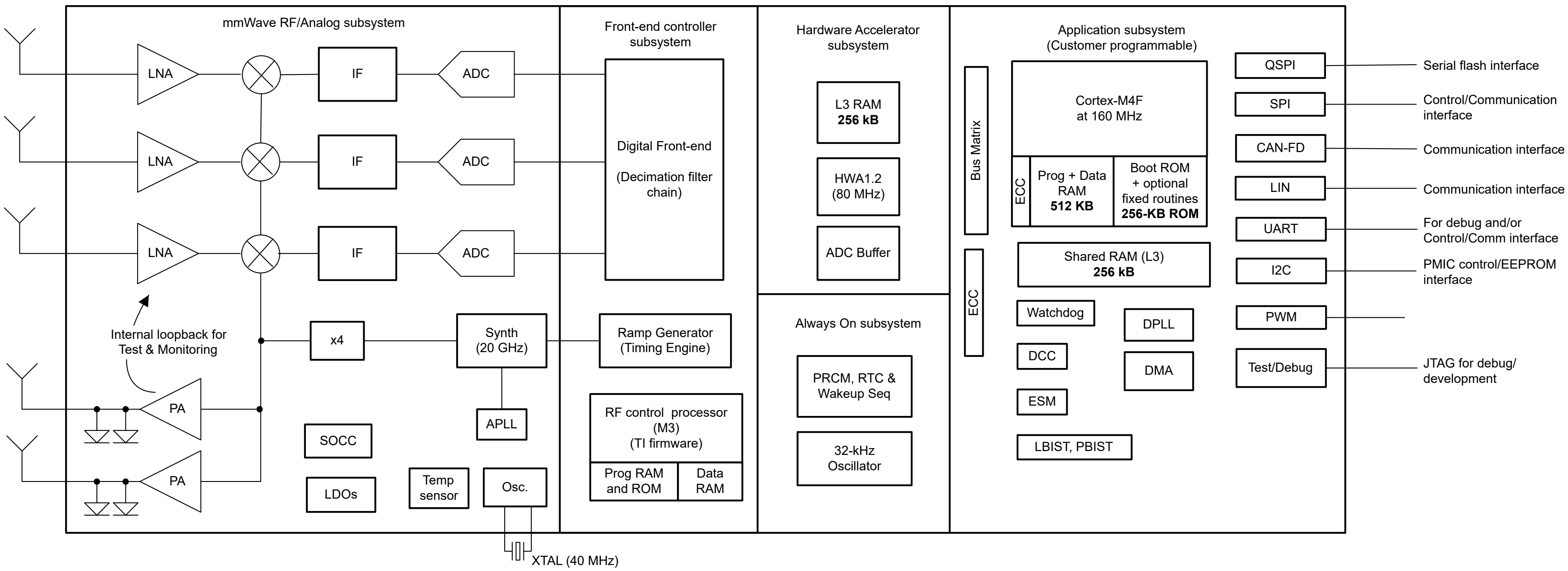


図 4-1. 機能ブロック図

Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Device Comparison

The following table compares the features of radar devices.

表 5-1. Device Features Comparison

FUNCTION	AWRL1432	AWRL6432	AWR1843AOP (1)	AWR1843 (1)	AWR1642
Antenna on Package (AOP)	-	-	Yes	-	-
Number of receivers	3	3	4	4	4
Number of transmitters	2	2	3(2)	3(2)	2
RF frequency range	76 to 81 GHz	57 to 64 GHz	76 to 81 GHz	76 to 81 GHz	76 to 81 GHz
On-chip memory	1 MB	1 MB	2MB	2MB	1.5MB
Max I/F (Intermediate Frequency) (MHz)	5	5	10	10	5
Max real sampling rate (Msps)	12.5	12.5	25	25	12.5
Max complex sampling rate (Msps)	-	-	12.5	12.5	6.25
Safety and Security					
Functional Safety -Compliance	ASIL-B Targeted	ASIL-B Targeted	ASIL-B	ASIL-B	-
Device Security(3)	-	-	Yes	Yes	Yes
Processors					
MCU	M4F	M4F	R4F	R4F	R4F
DSP	-	-	C674x	C674x	C674x
HWA	Yes	Yes	Yes	Yes	-
Peripherals					
Serial Peripheral Interface (SPI) ports	2	2	2	2	2
Quad Serial Peripheral Interface (QSPI)	Yes	Yes	Yes	Yes	Yes
Inter-Integrated Circuit (I2C) interface	1	1	1	1	1
Controller Area Network (Classical CAN) interface	-	-	1	1	1
Controller Area Network (CAN-FD) interface	1	1	1	1	-
DSP Trace	-	-	Yes	Yes	Yes
PWM	Yes	Yes	Yes	Yes	Yes
DMM Interface	-	-	Yes	Yes	Yes
Hardware In Loop (HIL/DMM)	-	-	Yes	Yes	Yes
GPADC	Yes	Yes	Yes	Yes	Yes
ADC Raw Data Capture	RDIF	RDIF	LVDS	LVDS	LVDS
LIN	Yes	Yes	-	-	-
UART	2	2	2	2	2
1-V bypass mode	N/A	N/A	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
Per Chirp configurable TX phase shifter	BPM Only	BPM Only	Yes(4)	Yes(4)	BPM only

表 5-1. Device Features Comparison (続き)

FUNCTION		AWRL1432	AWRL6432	AWR1843AOP [(1)]	AWR1843 [(1)]	AWR1642
Product status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	AI	AI	PD[(5)]	PD[(5)]	PD[(5)]

(1) Developed for Functional Safety applications, the device supports hardware integrity up to ASIL-B. Refer to the related documentation for more details. Non-Functional Safety Variants are also available for AWRL1432 device.
(2) 3 Tx Simultaneous operation is supported only with 1-V LDO bypass and PA LDO disable mode. In this mode, the 1-V supply needs to be fed on the VOUT PA pin.
(3) Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.
(4) 6 bits linear Phase Shifter.
(5) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

ADVANCE INFORMATION

ADVANCE INFORMATION

5.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors	TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.
Automotive mmWave Sensors	TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.
Companion Products for AWRL1432	Review products that are similar to this product.
Reference designs for AWRL1432	TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.
Obstacle detection reference design	This reference design demonstrates the use of the AWRL1432/AWR1642 single-chip mmWave sensor with integrated DSP as an obstacle-detection sensor for the car door and trunk, enabling applications like automatic car door openers and intelligent car doors that can accurately detect obstacles/objects in a wide field of view (FoV).

6 Terminal Configurations and Functions

6.1 Pin Diagrams

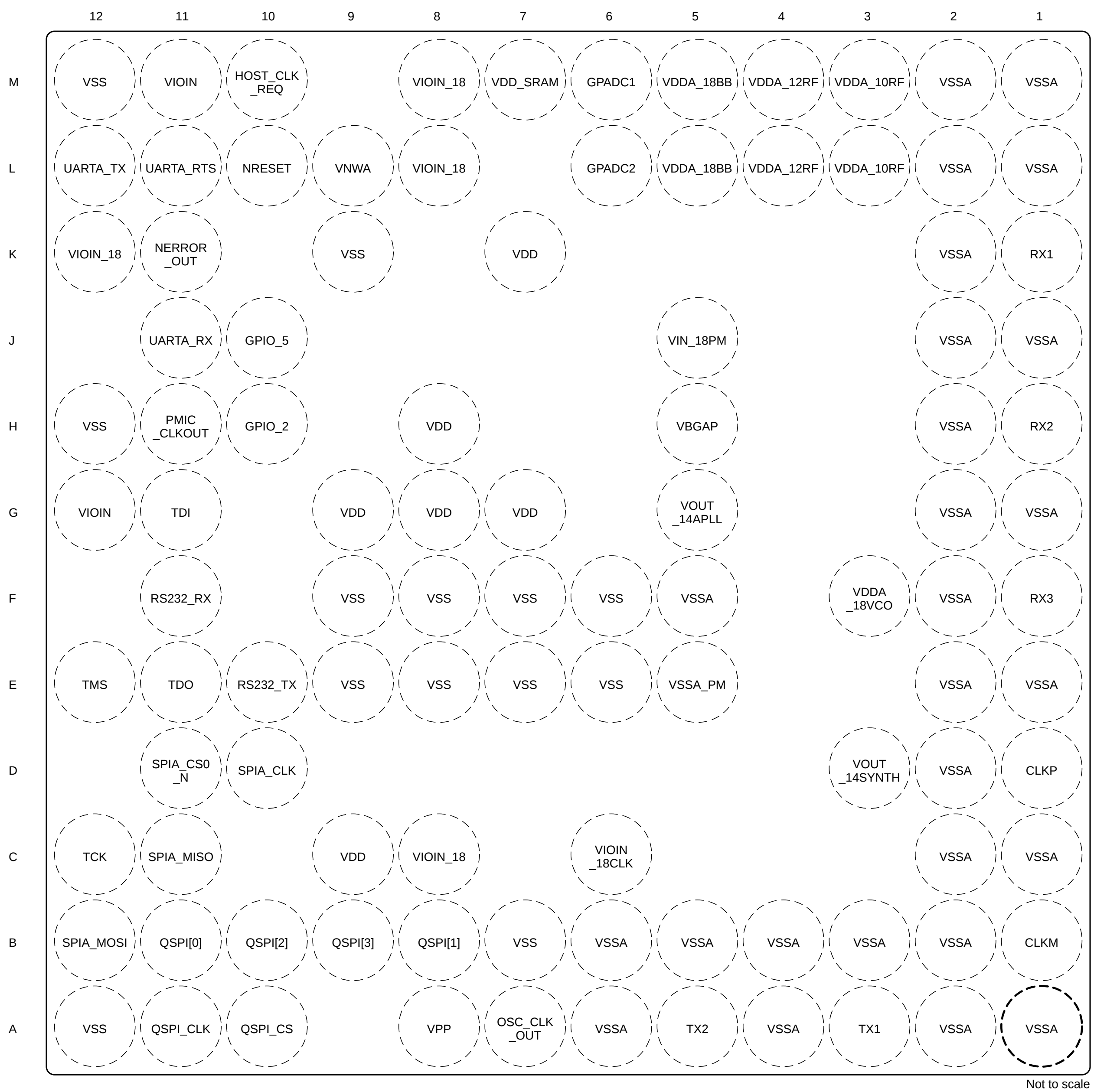


図 6-1. BGA Pin Diagram (Top View)

ADVANCE INFORMATION

ADVANCE INFORMATION

6.2 Signal Descriptions

注

All digital IO pins of the device (except NRESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

表 6-1. Analog Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
CLKM	XTAL CLKM pin	A	B10
CLKP	XTAL CLKP pin	A	D10
GPADC1	GPADC input 1	A	M10
NRESET	NRESET input	A	M3, M4
OSC_CLK_OUT	Oscillator Clock output	A	A8, B8
VBGAP	BandGap reference pin	A	H10

表 6-2. CAN Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
CAN_FD_RX	CAN Receive Data	I	J3
CAN_FD_TX	CAN Transmit Data	O	K3

表 6-3. Clock Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
MCU_CLKOUT	MCU clock output	O	J4, L3
PMIC_CLKOUT	PMIC clock output	O	H3
RTC_CLK_IN	RTC clock input	I	C3, G3, H2, J4, L4

表 6-4. EPWM Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
EPWMA	EPWM Output A	O	E4, F2, F4, L4
EPWMB	EPWM Output B	O	E3, F1, F3, J2
EPWM_SYNC_IN	EPWM Sync Input	I	G3, H4, J2
EPWM_SYNC_OUT	EPWM Sync output	O	G3

表 6-5. GPIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
GPIO_0	General Purpose Input/Output	IO	E3
GPIO_1	General Purpose Input/Output	IO	E4
GPIO_2	General Purpose Input/Output	IO	H2
GPIO_3	General Purpose Input/Output	IO	J3
GPIO_4	General Purpose Input/Output	IO	J4
GPIO_5	General Purpose Input/Output	IO	J2
GPIO_6	General Purpose Input/Output	IO	L4
GPIO_7	General Purpose Input/Output	IO	L3

表 6-6. I2C Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
I2C_SCL	I2C Clock	IO	C4, F1, H4, K3, L3

表 6-6. I2C Signal Descriptions (続き)

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
I2C_SDA	I2C Data	IO	B4, F4, G2, H2, J3

表 6-7. JTAG Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
TCK	JTAG Test Clock Input	I	F3
TDI	JTAG Test Data Input	I	F2
TDO	JTAG Test Data Output	O	E2
TMS	JTAG Test Mode Select Input	I	G3

表 6-8. LIN Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
LIN_RX	LIN Receive Data	I	G2, H2, J2, J3
LIN_TX	LIN Transmit Data	O	H3, H4, K3, L3, L4

表 6-9. MDO Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
MDO_CLK	MDO Clock	O	D2, F1, L4
MDO_D0	MDO data 0	O	C2, F3, H2
MDO_D1	MDO data 1	O	C4, E3, H4, J3
MDO_D2	MDO data 2	O	B4, E4, G2, K3
MDO_D3	MDO data 3	O	C3, F4, J2, J4, L3
MDO_FRM_CLK	MDO Frame Clock	O	D3, E2, H3, L3

表 6-10. Power Supply Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	BGA PIN
VDD	1.2V Core supply	PWR	C9, G7, G8, G9, H8, K7
VDDA_12RF	1.2V RF Supply	PWR	L4, M4
VDDA_18BB	1.8V analog supply	PWR	L5, M5
VDDA_18VCO	1.8V analog supply	PWR	F3
VDD_SRAM	1.2V SRAM supply	PWR	M7
VIN_18PM	1.8V core supply	PWR	J5
VIOIN	1.8V analog supply	PWR	G12, M11
VIOIN_18	1.8V analog supply	PWR	C8, K12, L8, M8
VIOIN_18CLK	1.8V analog supply	PWR	C6
VNWA	1.2V VNWA supply. Always connected to SRAM supply	PWR	L9
VPP	Voltage supply for fuse chain	PWR	A8
VSS	Ground	GND	A12, B7, E6, E7, E8, E9, F6, F7, F8, F9, H12, K9, M12
VSSA	Ground	GND	A1, A2, A4, A6, B2, B3, B4, B5, B6, C1, C2, D2, E1, E2, F2, F5, G1, G2, H2, J1, J2, K2, L1, L2, M1, M2

ADVANCE INFORMATION

表 6-10. Power Supply Signal Descriptions (続き)

SIGNAL NAME	DESCRIPTION	PIN TYPE	BGA PIN
VSSA_PM	Ground	GND	E5

表 6-11. QSPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	BGA PIN
QSPI_D0	QSPI Data bit 0	IO	B11
QSPI_D1	QSPI Data bit 1	I	B8
QSPI_D2	QSPI Data bit 2	I	B10
QSPI_D3	QSPI Data bit 3	I	B9
QSPI_SCLK	QSPI clock	IO	A11
QSPI_CS	QSPI Chip select	O	A10

表 6-12. RS232 Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
RS232_RX	RS232 Receive Data	I	G2
RS232_TX	RS232 Transmit Data	O	H4

表 6-13. SPIA Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
SPIA_CLK	SPIA Clock	IO	F1
SPIA_CS0_N	SPIA Chip Select 0	IO	F4
SPIA_CS1_N	SPIA Chip Select 1	IO	G3, H2, H3
SPIA_MISO	SPIA MISO	IO	E4
SPIA_MOSI	SPIA MOSI	IO	E3

表 6-14. SPIB Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
SPIB_CLK	SPIB Clock	IO	D2, F1, G3, L4
SPIB_CS0_N	SPIB Chip Select 0	IO	D3, F2, F4, J4
SPIB_CS1_N	SPIB Chip Select 1	IO	F3, H4
SPIB_MISO	SPIB MISO	IO	C3, E4, G2, G3, L3
SPIB_MOSI	SPIB MOSI	IO	C2, E3, F3, K3

表 6-15. System Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
HOST_CLK_REQ	Host clock request output	O	L3
NERROR_OUT	NERROR output signal	O	J4
SYNC_IN	Sync input	I	B4, G3, J2, J3, J4
WARM_RESET_OUT	Warm reset output	O	G3, H2
WU_REQIN	Wakeup Request input	I	C4, H2, J4, K3, L3, L4

表 6-16. UARTA Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
UARTA_RTS	UARTA RTS output	O	L4

表 6-16. UARTA Signal Descriptions (続き)

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
UARTA_RX	UARTA Receive Data	I	J3
UARTA_TX	UARTA Transmit Data	O	K3

表 6-17. UARTB Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	AMY PIN
UARTB_RX	UARTB Receive Data	I	G2, J3
UARTB_TX	UARTB Transmit Data	O	H4, K3

ADVANCE INFORMATION

表 6-18. Pin Muxing Table

BGA BALL NUMBER (1)	BALL NAME (2)	SIGNAL NAME (3)	PINCNTL REGISTER (4)	PIN CNTL REGISTER ADDRESS (5) (11)	MODE (6)	TYPE (7)	PULL UP/ DOWN TYPE (8)	BALL STATE DURING RST (9)	BALL STATE AFTER RST (10)
H10	GPIO_2	GPIO_2	PADAL_CFG_REG	0x5A00 002C	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_RX			1	I			
		WARM_RESET_OUT			2	O			
		I2C_SDA			3	IO			
		SPIA_CS1_N			4	IO			
		WU_REQIN			5	I			
		RTC_CLK_IN			6	I			
		MDO_D0			7	O			
J10	GPIO_5	GPIO_5	PADAV_CFG_REG	0x5A00 0054	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SYNC_IN			1	I			
		LIN_RX			2	I			
		EPWMB			3	O			
		EPWM_SYNC_IN			4	I			
		MDO_D3			5	O			
M10	HOST_CLK_REQ	HOST_CLK_REQ	PADAX_CFG_REG	0x5A00 005C	0	O	PU/PD	OFF/OFF/OFF	OFF/SS/OFF
		GPIO_7			1	IO			
		MCU_CLKOUT			2	O			
		LIN_TX			3	O			
		WU_REQIN			4	I			
		SPIB_MISO			5	IO			
		I2C_SCL			6	IO			
		MDO_D3			8	O			
		MDO_FRM_CLK			9	O			
K11	NERROR_OUT	NERROR_OUT	PADAU_CFG_REG	0x5A00 0050	0	O	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_4			1	IO			
		SYNC_IN			2	I			
		SPIB_CS0_N			3	IO			
		WU_REQIN			4	I			
		RTC_CLK_IN			5	I			
		MCU_CLKOUT			6	O			
		MDO_D3			7	O			
H11	PMIC_CLKOUT	PMIC_CLKOUT	PADAK_CFG_REG	0x5A00 0028	0	O	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_TX			1	O			
		SPIA_CS1_N			2	IO			
		MDO_FRM_CLK			3	O			
B11	QSPI[0]	QSPI[0]	PADAC_CFG_REG	0x5A00 0008	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_MOSI			1	IO			
		MDO_D0			2	O			
B8	QSPI[1]	QSPI[1]	PADAD_CFG_REG	0x5A00 000C	0	I	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_MISO			1	IO			
		RTC_CLK_IN			2	I			
		MDO_D3			3	O			
B10	QSPI[2]	QSPI[2]	PADAE_CFG_REG	0x5A00 0010	0	I	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		I2C_SCL			1	IO			
		WU_REQIN			2	I			
		MDO_D1			3	O			

表 6-18. Pin Muxing Table (続き)

BGA BALL NUMBER (1)	BALL NAME(2)	SIGNAL NAME(3)	PINCNTL REGISTER(4)	PIN CNTL REGISTER ADDRESS(5) (11)	MODE (6)	TYPE (7)	PULL UP/ DOWN TYPE(8)	BALL STATE DURING RST(9)	BALL STATE AFTER RST (10)
B9	QSPI[3]	QSPI[3]	PADAF_CFG_REG	0x5A00 0014	0	I	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		I2C_SDA			1	IO			
		SYNC_IN			2	I			
		MDO_D2			3	O			
A11	QSPI_CLK	QSPI_CLK	PADAA_CFG_REG	0x5A00 0000	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_CLK			1	IO			
		MDO_CLK			2	O			
A10	QSPI_CS	QSPI_CS	PADAB_CFG_REG	0x5A00 0004	0	O	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_CS0_N			1	IO			
		MDO_FRM_CLK			2	O			
F11	RS232_RX	RS232_RX	PADAP_CFG_REG	0x5A00 003C	0	I	PU/PD	OFF/OFF/UP	ON/OFF/UP
		I2C_SDA			1	IO			
		UARTB_RX			2	I			
		LIN_RX			3	I			
		MDO_D2			4	O			
		SPIB_MISO			5	IO			
E10	RS232_TX	RS232_TX	PADAO_CFG_REG	0x5A00 0038	0	O	PU/PD	OFF/OFF/OFF	OFF/SS/OFF
		I2C_SCL			1	IO			
		UARTB_TX			2	O			
		LIN_TX			3	O			
		EPWM_SYNC_IN			4	I			
		MDO_D1			5	O			
		SPIB_CS1_N			6	IO			
D10	SPIA_CLK	SPIA_CLK	PADAG_CFG_REG	0x5A00 0018	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		EPWMB			1	O			
		I2C_SCL			2	IO			
		SPIB_CLK			3	IO			
		MDO_CLK			4	O			
D11	SPIA_CS0_N	SPIA_CS0_N	PADAH_CFG_REG	0x5A00 001C	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		EPWMA			1	O			
		I2C_SDA			2	IO			
		SPIB_CS0_N			3	IO			
		MDO_D3			4	O			
C11	SPIA_MISO	SPIA_MISO	PADAJ_CFG_REG	0x5A00 0024	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_1			1	IO			
		EPWMA			2	O			
		SPIB_MISO			3	IO			
		MDO_D2			4	O			
B12	SPIA_MOSI	SPIA_MOSI	PADAI_CFG_REG	0x5A00 0020	0	IO	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_0			1	IO			
		EPWMB			2	O			
		SPIB_MOSI			3	IO			
		MDO_D1			4	O			

ADVANCE INFORMATION

ADVANCE INFORMATION

表 6-18. Pin Muxing Table (続き)

BGA BALL NUMBER (1)	BALL NAME(2)	SIGNAL NAME(3)	PINCNTL REGISTER(4)	PIN CNTL REGISTER ADDRESS(5) (11)	MODE (6)	TYPE (7)	PULL UP/ DOWN TYPE(8)	BALL STATE DURING RST(9)	BALL STATE AFTER RST (10)
C12	TCK	TCK	PADAT_CFG_REG	0x5A00 004C	0	I	PU/PD	OFF/OFF/DOWN	ON/OFF/DOWN
		EPWMB			1	O			
		SPIB_CS1_N			2	IO			
		SPIB_MOSI			3	IO			
		MDO_D0			4	O			
G11	TDI	TDI	PADAR_CFG_REG	0x5A00 0044	0	I	PU/PD	OFF/OFF/DOWN	ON/OFF/DOWN
		EPWMA			1	O			
		SPIB_CS0_N			2	IO			
E11	TDO	TDO	PADAS_CFG_REG	0x5A00 0048	0	O	PU/PD	OFF/OFF/OFF	OFF/SS/OFF
		MDO_FRM_CLK			1	O			
E12	TMS	TMS	PADAQ_CFG_REG	0x5A00 0040	0	I	PU/PD	OFF/OFF/UP	ON/OFF/UP
		WARM_RESET_OUT			1	O			
		SPIA_CS1_N			2	IO			
		SYNC_IN			3	I			
		SPIB_MISO			4	IO			
		SPIB_CLK			5	IO			
		RTC_CLK_IN			6	I			
		EPWM_SYNC_IN			7	I			
		EPWM_SYNC_OUT			8	O			
L11	UARTA_RTS	UART_RTS	PADAW_CFG_REG	0x5A00 0058	0	O	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_6			1	IO			
		LIN_TX			2	O			
		SPIB_CLK			3	IO			
		WU_REQIN			4	I			
		EPWMA			5	O			
		RTC_CLK_IN			6	I			
		MDO_CLK			7	O			
J11	UARTA_RX	UARTA_RX	PADAM_CFG_REG	0x5A00 0030	0	I	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_3			1	IO			
		LIN_RX			2	I			
		CAN_FD_RX			3	I			
		SYNC_IN			4	I			
		UARTB_RX			5	I			
		I2C_SDA			6	IO			
		MDO_D1			7	O			
L12	UARTA_TX	UARTA_TX	PADAN_CFG_REG	0x5A00 0034	0	O	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_TX			1	O			
		CAN_FD_TX			2	O			
		SPIB_MOSI			3	IO			
		WU_REQIN			4	I			
		UARTB_TX			5	O			
		I2C_SCL			6	IO			
		MDO_D2			7	O			

(1) **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
(2) **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
(3) **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
(4) **PINCNTL_REGISTER:** APPSS Register name for PinMux Control
(5) **PINCNTL ADDRESS:** APPSS Address for PinMux Control

(6) **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.

(7) **TYPE:** Signal type and direction:
- I = Input
- O = Output
- IO = Input or Output

(8) **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- Pull Up: Internal pullup
- Pull Down: Internal pulldown
- An empty box means No pull.

(9) **BALL STATE DURING RST**: State of Ball during reset in the format of RX/TX/Pull Status
- RX (Input buffer)
  - Off: The input buffer is **disabled**.
  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- Pull Status (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

(10) **BALL STATE AFTER RST**: State of Ball after reset in the format of RX/TX/Pull Status
- RX (Input buffer)
  - Off: The input buffer is **disabled**.
  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - SS: The subsystem selected with MUXMODE determines the output buffer state.
- Pull status (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up resistor** is turned on.
  - Down: Internal **pull-down resistor** is turned on.
  - NA: No internal pull resistor.
- An empty box, NA, or "-" means Not Applicable.

(11) Pin Mux Control Value maps to lower 4 bits of register.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

PARAMETERS[(1)] [(2)]		MIN	MAX	UNIT
VDD	1.2 V digital power supply	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os operate on the same VIOIN voltage level	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIOIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VDDA_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VDDA_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
RX1-3	Externally applied power on RF inputs		10	dBm
TX1-2	Externally applied power on RF outputs[(3)]		10	dBm
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	125	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AECQ100-002 [(1)]	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j) [(1)]	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
–40°C	100% duty cycle	1.2	600 (6%)
75°C			2000 (20%)
95°C			6500 (65%)
125°C			900 (9%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	1.2 V digital power supply	1.14	1.2	1.26	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.89	V
VIOIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.89	V
VDDA_18BB	1.8-V Analog baseband power supply	1.71	1.8	1.89	V
VDDA_18VCO	1.8V RF VCO supply	1.71	1.8	1.89	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[1:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

ADVANCE INFORMATION

ADVANCE INFORMATION

7.5 Power Supply Specifications

7.5.1 Power Optimized 3.3V I/O Topology

表 7-1 describes the power rails from an external power supply block to the device via a 3.3V I/O topology.

表 7-1. Power Supply Rails Characteristics: Power Optimized 3.3V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
3.3 V	Digital I/Os	Input: VIOIN
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.2 V	Core Digital and SRAMs, RF	Input: VDD, VNWA, VDD_SRAM, VDDA_12RF LDO Output: VDDA_10RF

7.5.2 BOM Optimized 3.3V I/O Topology

表 7-2 describes the power rails from an external power supply block to the device via a BOM Optimized 3.3V I/O Topology.

表 7-2. Power Supply Rails Characteristics: BOM Optimized 3.3V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
3.3V	Digital I/Os	Input: VIOIN
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VDDA_10RF, VDD_SRAM, VOUT_14APLL, VDDA_12RF, VDD

7.5.3 Power Optimized 1.8V I/O Topology

表 7-3 describes the power rails from an external power supply block to the device via a power optimized 1.8V I/O topology.

表 7-3. Power Supply Rails Characteristics: Power Optimized 1.8V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VIOIN, VIN_18PM, VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.2 V	Core Digital and SRAMs, RF, VNWA	Input: VDD, VDD_SRAM, VNWA,VDDA_12RF LDO Output: VDDA_10RF

7.5.4 BOM Optimized 1.8V I/O Topology

表 7-4 describes the power rails from an external power supply block to the device via a BOM optimized 1.8V I/O topology.

表 7-4. Power Supply Rails Characteristics: BOM Optimized 1.8V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, Digital I/Os	Input: VIOIN, VDDA_18VCO, VIOIN_18CLK, VIOIN_18, VDDA_18BB, VIN_18PM, VDDA_18VCO LDO Output: VDD, VDD_SRAM, VDDA_10RF, VDDA_12RF, VOUT_14APLL, VOUT_14SYNTH

7.5.5 System Topologies

The following the system topologies are supported.

- Topology 1: Peripheral Mode, under the control of external MCU
- Topology 2: Autonomous mode, with connection to a remote host via LIN/CAN

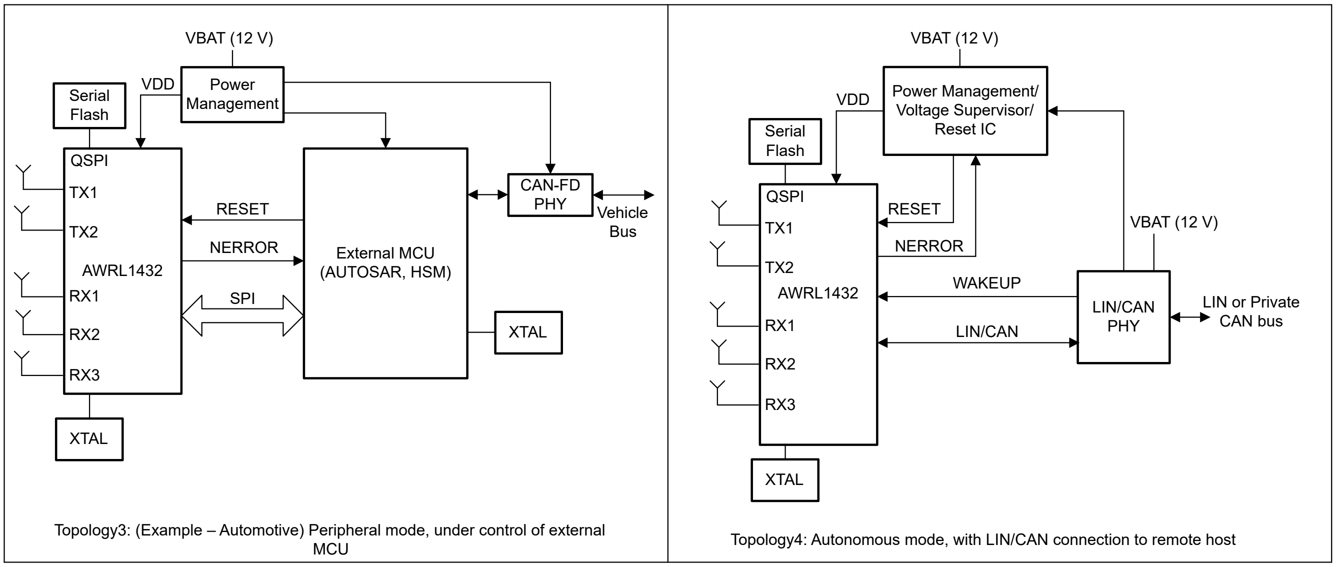


図 7-1. System Topologies

7.5.5.1 Power Topologies

The device supports two unique power topologies for BOM optimized and Power Optimized modes. Above tables summarizes these options.

7.5.5.1.1 BOM Optimized Mode

In this mode the device can be powered using one 1.8V regulator OR using a 3.3V and a 1.8V regulator mode. The choice of one rail vs two rails is dependent on the IO voltages needed.

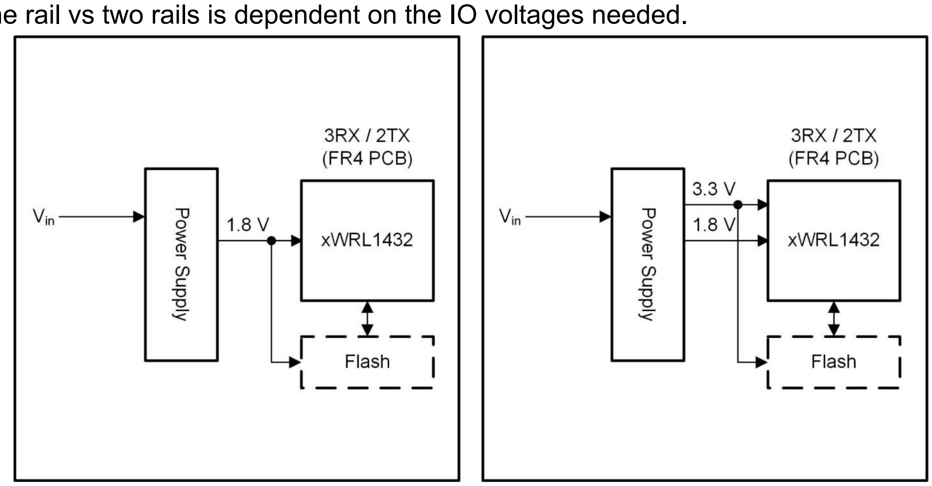


図 7-2. BOM Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.5.5.1.2 Power Optimized Mode

This mode is for applications needing ultra-low power applications. The device can either be powered using two rails (1.8 V and 1.2 V) or with three rails (3.3 V, 1.8 V and 1.2 V).

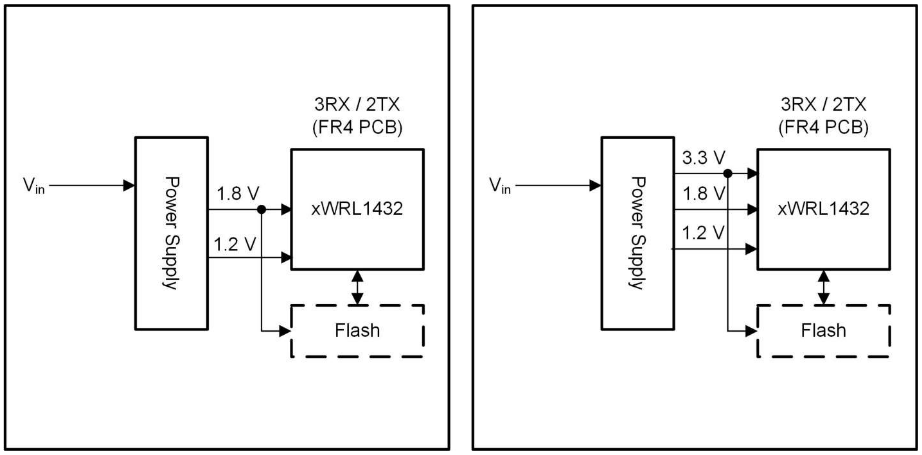


図 7-3. Power Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.5.6 Noise and Ripple Specifications

The 1.8-V power supply ripple specifications mentioned in 表 7-5 are defined to meet a target spur level of –105 dBc (RF Pin = –15 dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1-dB increase in supply ripple leads to a ~1 dB increase in spur level. Values quoted are peak-peak levels for a sinusoidal input applied at the specified frequency. These values are being optimized and are subject to change.

表 7-5. Noise and Ripple Specifications

FREQ (kHZ)	NOISE SPECIFICATION		RIPPLE SPECIFICATION	
	1.8 V (µV/√Hz)	1.2V (µV/√Hz)1	1.8 V (mVpp)	1.2V (mVpp)1
10	6.057	44.987	0.035	1.996
100	2.677	26.801	0.760	2.233
200	2.388	28.393	0.955	3.116
500	0.757	9.559	0.504	1.152
1000	0.419	1.182	0.379	0.532
2000	0.179	1.256	0.153	0.561
5000	0.0798	0.667	0.079	0.297
10000	0.0178	0.104	0.017	0.046

1. 1.2V noise/ripple specification is only for power optimized supply configurations.

7.6 Power Save Modes

表 7-6 lists the supported power states.

表 7-6. Device Power States

Power State	Details
Active	Active Power State is when RF/chirping activity is ongoing
Processing	Processing Power State is when data is being processed RF turned off(1)
Idle	Idle Power State is during inter-frame/inter-burst/inter-chirp idle time
Deep Sleep	Lowest possible power state of the device where the contents of the device can be retained (Application Image, Chirp Profile etc) and device need not boot from scratch again. Device can enter this state after the frame processing is complete in order to save power significantly. Deep sleep exit can be through a number of external wakeup sources and internal timing maintenance.

(1) The power consumed here also includes the Hardware Accelerator Power Consumption.

7.6.1 Typical Power Consumption Numbers

表 7-7 lists the typical power consumption for each power save modes in different power topologies and antenna configurations.

Below quoted power numbers in 表 7-7, 表 7-8 and 表 7-9 are based on initial silicon measurements and might be subjected to change/improvement pertaining to further characterization

表 7-7. Estimated Power Consumed in 3.3-V IO Mode

Power Mode		Power Consumption (mW)(1)	
		Power Optimized Mode	BOM Optimized Mode
Active (2TX, 3RX)	Sampling: 12.5 MSps, Continuous Streaming Mode (CW) mode Freq =77 GHz TX Power = 10dBm RX gain = 30 dB	1358	1867
Active (2TX, 2RX)		1267	1747
Active (1TX, 2RX)		1013	1368
Active (1TX, 1RX)		945	1271
Processing		159	233
Idle (Frame Idle)	APPSS CM4 = 20MHz, FECSS, HWA powered off, SPI Interface active	13.80	23.13
Deep sleep	Memory Retained = 114KB	1.38	1.34

(1) The Power consumption numbers are for a typical usecase i.e. for a Nominal device at 25C ambient temperature and nominal voltage conditions.

表 7-8. Estimated Power Consumed in 1.8-V IO Mode

Power Mode	Power Consumption (mW)	
	Power Optimized Mode	BOM Optimized Mode
Deep Sleep	0.640	0.780

表 7-9. Use-Case Power Consumed in 3.3-V Power Optimized Topology

Parameter		Condition	Typical (mW)
Average Power Consumption (Presence Detection -Minor Motion)	**RF Front End Configuration :** 2TX, 3RX 5MHz Sampling Rate Num of ADC samples = 64 Ramp End time = 19us Chirp Idle Time = 6us Chirp Slope = 32MHz/us Number of chirps per burst = 8 Burst Periodicity = 315us Number of bursts per frame = 1 Device configured to go to deep sleep state after active operation. Memory Retained in deep sleep = 900KB	1Hz Update Rate	2.6

7.7 Peak Current Requirement per Voltage Rail

表 7-10 provides the max split rail current numbers.

ADVANCE INFORMATION

表 7-10. Maximum Peak Current per Voltage Rail

Mode(1)	IO Voltage(3)	Maximum Current (mA) (2)		
		1.2V: total current drawn by all nodes driven by 1.2V rail	1.8V: total current drawn by all nodes driven by 1.8V rail	3.3V: total current drawn by all nodes driven by 3.3V rail
BOM Optimized	3.3 V	NA	1360	90
BOM Optimized	1.8V	NA	1450	NA
Power Optimized	3.3 V	1100	270	90
Power Optimized	1.8 V	1100	360	NA

(1) Exercise full functionality of device, including 2TX, 3RX simultaneous operation, HWA, M4F and various host comm/interface peripherals active (CAN, LIN, I2C, GPADC), test across full temperature range
(2) The specified current values are at typical supply voltage level.
(3) The exact VIOIN current depends on the peripherals used and their frequency of operation.

7.8 RF Specification

Over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver(1)	Noise figure	76 to 81 GHz		14.5		dB
	1-dB compression point (Out Of Band)(2)			–9		dBm
	Maximum gain			40		dB
	Gain range			10		dB
	Gain step size			2		dB
	IF bandwidth(3)				5	MHz
	ADC sampling rate (real)				12.5	Msps
	ADC resolution			12		Bits
Transmitter(1)	Output Power			11		dBm
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				400	MHz/μs
	Phase noise at 1-MHz offset	76 to 81 GHz		–89		dBc/Hz

(1) The polarity of LO signal for TX2 is inverted with respect to TX1, hence the phase of the signal is expected to have 180^0 offset. Enabling BPM on a transmitter chain will create additional 180^0 phase offset on that chain. The polarity of LO signal for RX2 is inverted with respect to RX1 and RX3, hence the phase of the signal is expected to have 180^0 offset. This can be taken care during post-processing, in HWA or external processing.
(2) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone well below the HPF cut-off frequency.
(3) The analog IF stages include high-pass filtering, with configurable first-order high-pass corner frequency. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)
175, 350, 700, 1400

The filtering performed by the digital baseband chain is targeted to provide less than ±0.5 dB pass-band ripple/droop.

図 7-4 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

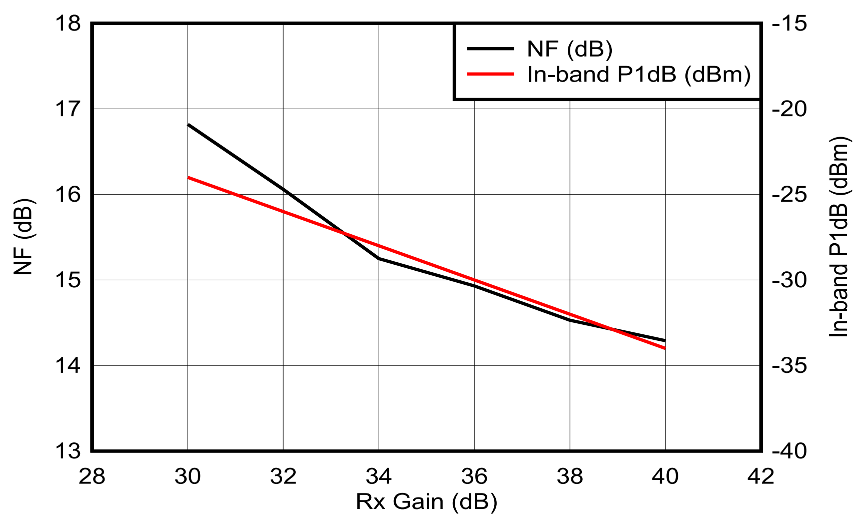


図 7-4. Noise Figure, In-band P1dB vs Receiver Gain

ADVANCE INFORMATION

7.9 Supported DFE Features

- TX output back-off
  - Binary Phase Modulation supported on each TX
- RX gain
  - Real RX channels
  - Total RX gain range of 30 dB to 40 dB, in 2 dB steps
- VCO
  - Single VCO covering entire RF sweep bandwidth up to 5 GHz.
- High-pass filter
  - Supports corner frequency options 175 KHz, 350 KHz, 700 KHz, 1400 KHz
  - First-order high pass filter only
- Low-pass filter
  - Max IF bandwidth supported is 5 MHz
  - 40 dB stopband rejection, two filtering options supported
  - 80% visibility – IF bandwidth is 80% of Nyquist and is 30% faster due to quicker settling time, compared with 90% visibility
  - 90% visibility – IF bandwidth is 90% of Nyquist (has longer setting time due to larger filter length)
- Timing Engine
  - Support for chirps, bursts and frames
    - Larger idle times can give more power saving
    - Chirp accumulation (averaging) possible across closely spaced chirps to reduce memory requirement
  - Provision for per-chirp dithering of parameters

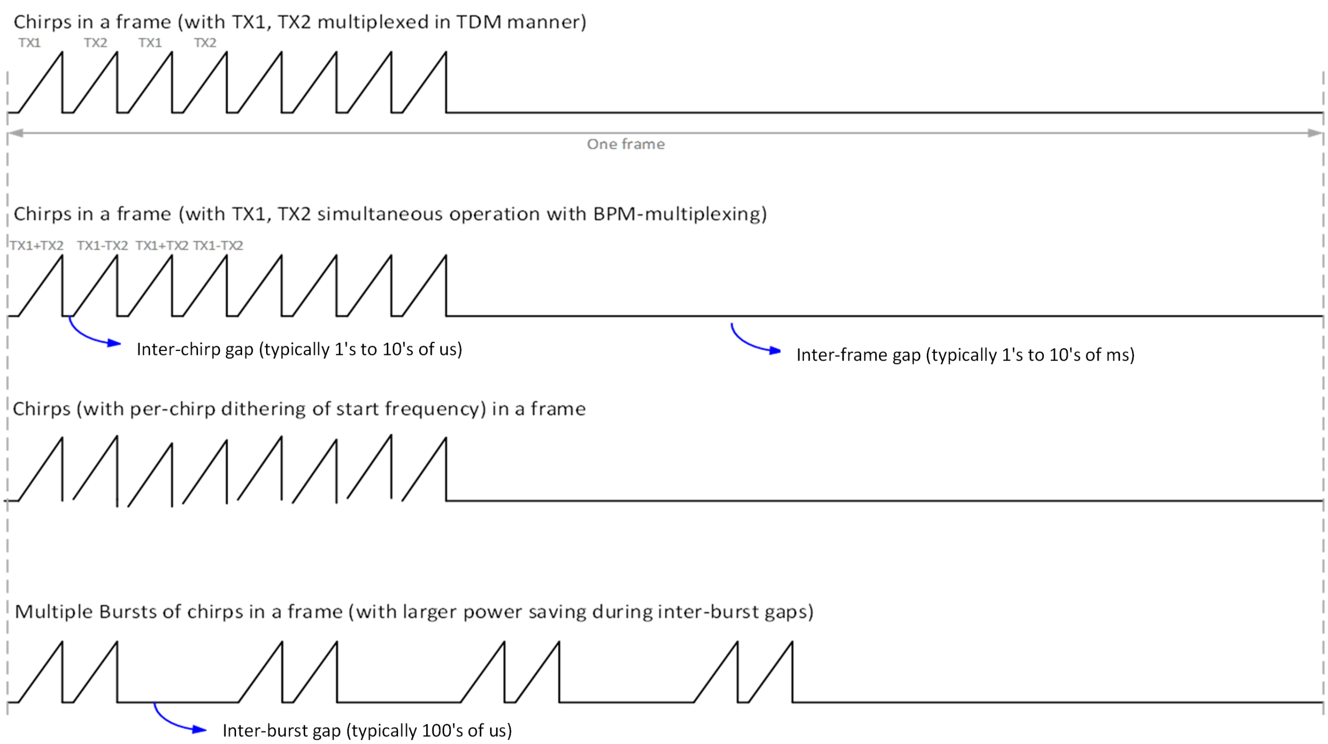


図 7-5. Chip Profile Supported by Timing Engine

7.10 CPU Specifications

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TYP	UNIT
Application Subsystem (M4F Family)	Clock Speed	160	MHz
	Tightly Coupled Memory - A (Program + Data)	512	KB
Shared Memory	Shared L3 Memory(1)	256	KB
	L3 Memory dedicated for HWA	256	KB

(1) L3 memory is configurable

7.11 Thermal Resistance Characteristics

表 7-11. Thermal Resistance Characteristics for FCCSP Package [AMF0102A]

THERMAL METRICS(1) (4)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	8.5
$R\Theta_{JB}$	Junction-to-board	6.2
$R\Theta_{JA}$	Junction-to-free air	24.7
Psi_{JC}	Junction-to-package top	0.36
Psi_{JB}	Junction-to-board	6.2

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/ JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

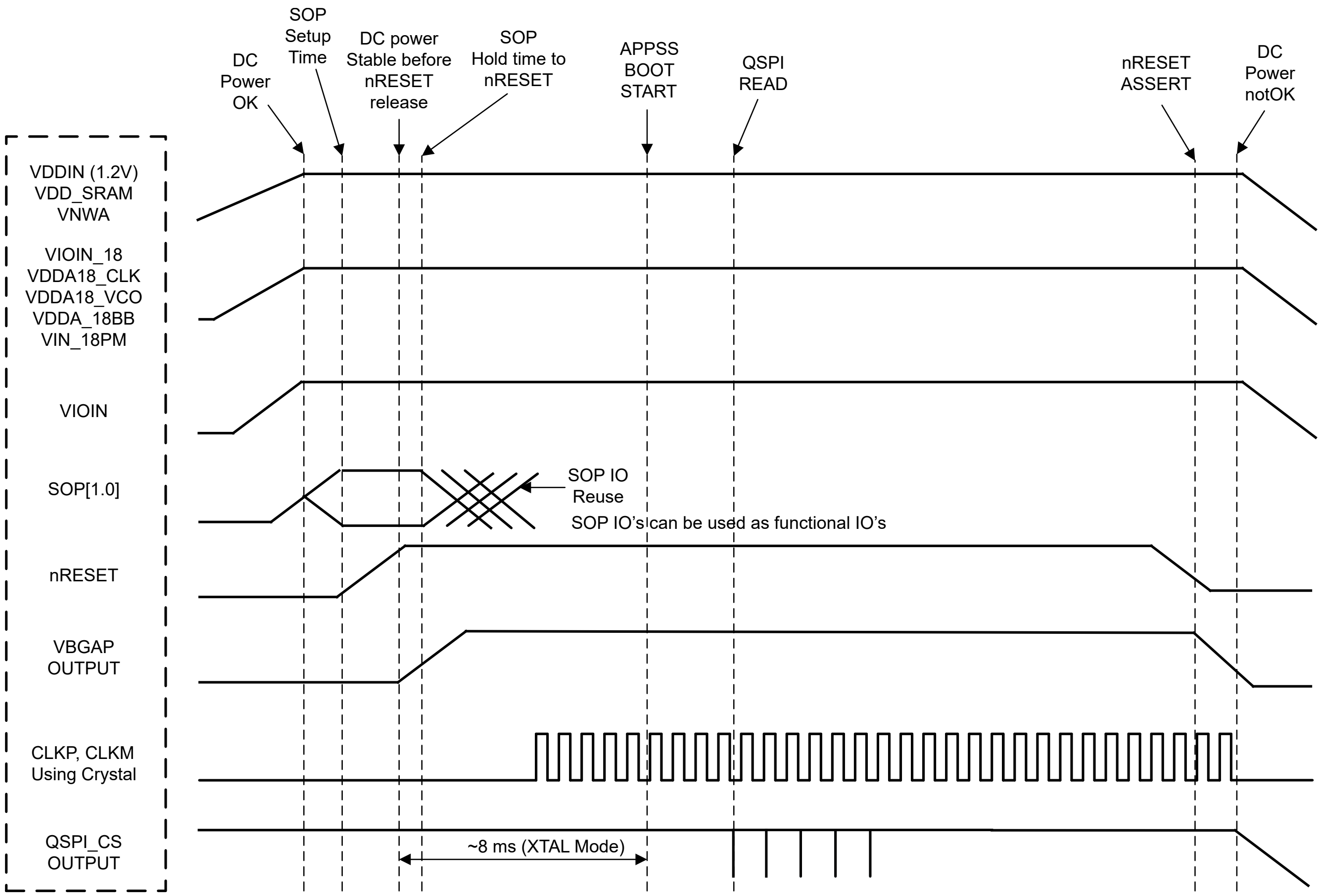
(4) Test Condition: Power=1.305W at 25°C

7.12 Timing and Switching Characteristics

7.12.1 Power Supply Sequencing and Reset Timing

The AWRL1432 device expects all external voltage rails to be stable before reset is deasserted. 図 7-6 describes the device wake-up sequence.

ADVANCE INFORMATION



A. MCU_CLK_OUT in autonomous mode, where AWRL1432 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

図 7-6. Device Wake-up Sequence

7.12.2 Synchronized Frame Triggering

The AWRL1432 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC_IN pulse should be always greater than the active frame duration in all instances.

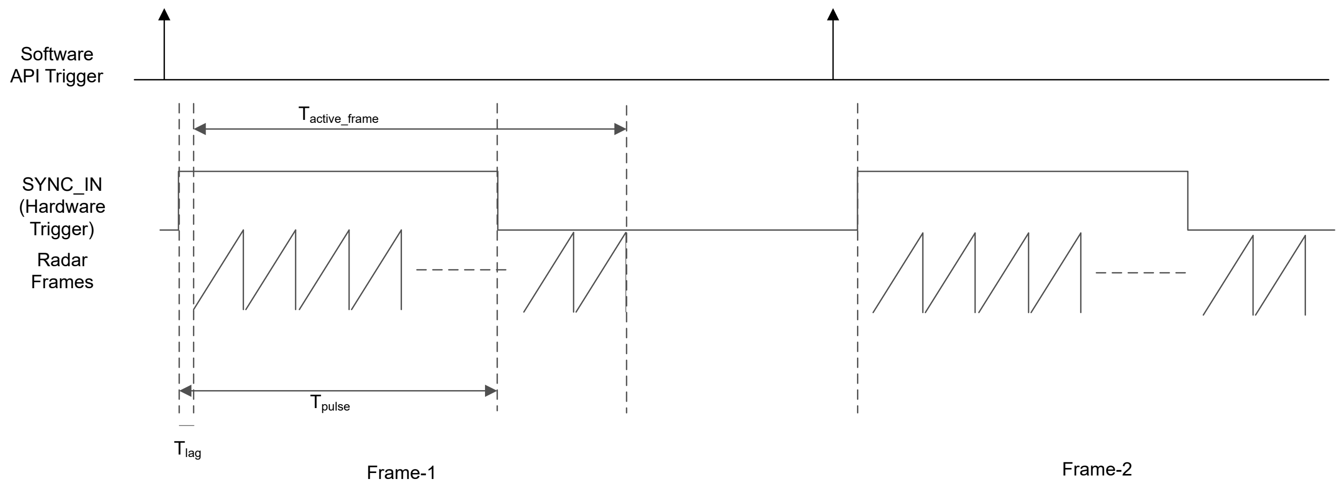


図 7-7. Sync In Hardware Trigger

表 7-12. Frame Trigger Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{active_frame}	Active frame duration	User defined		ns
T_{pulse}		25	< T_{active_frame}	

7.12.3 Input Clocks and Oscillators

7.12.3.1 Clock Specifications

The AWRL1432 requires external clock source (that is, a 40-MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal connected to the device pins 図 7-8 shows the crystal implementation.

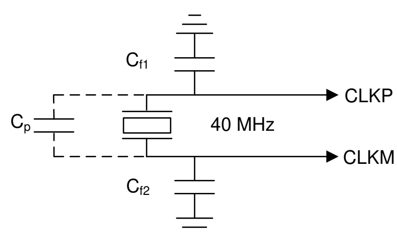


図 7-8. Crystal Implementation

注

The load capacitors, C_{f1} and C_{f2} in 図 7-8, should be chosen such that 式 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

表 7-13 lists the electrical characteristics of the clock crystal.

ADVANCE INFORMATION

表 7-13. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		125	°C
Frequency tolerance	Crystal frequency tolerance(1) (2) (3)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects radar sensor accuracy.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. 表 7-14 lists the electrical characteristics of the external clock signal.

ADVANCE INFORMATION

表 7-14. External Clock Mode Specifications

PARAMETER		SPECIFICATION MIN	SPECIFICATION TYP	SPECIFICATION MAX	UNIT
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-V_{il}	0.00		0.20	ns
	DC-V_{ih}	1.6		1.95	ns
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Frequency Tolerance	-100		100	ppm

ADVANCE INFORMATION

7.12.4 MultiChannel buffered / Standard Serial Peripheral Interface (McSPI)

The McSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus

7.12.4.1 McSPI Features

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receive mode
- Controller multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - Per channel configuration for clock definition, polarity enabling, and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for McSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

7.12.4.2 SPI Timing Conditions

表 7-15 presents timing conditions for McSPI

表 7-15. McSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.12.4.3 SPI—Controller Mode

7.12.4.3.1 Timing and Switching Requirements for SPI - Controller Mode

表 7-16 and 表 7-16 present timing requirements for SPI - Controller Mode.

表 7-16. SPI Timing Requirements - Controller Mode

NO.(1) (8)			MODE	MIN	MAX	UNIT
SM4	$t_{su(MISO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge (1)		5		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge (1)		3		ns

表 7-17. SPI Switching Characteristics - Controller Mode

NO.(1) (8)			MODE	MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK (1) (2)		24.6(3)		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low (1)		-1 + 0.5P(3) (4)		ns

表 7-17. SPI Switching Characteristics - Controller Mode (続き)

NO.[1] [8]			MODE	MIN	MAX	UNIT
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high [1]		-1 + 0.5P[4]		ns
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition [1]		-2	5	ns
SM7	$t_{sk(CS-SIMO)}$	Delay time, SPI_CS[x] active to SPI_D[x] transition		5		ns
SM8	$t_{d(SPICLK-CS)}$	Delay time, SPI_CS[x] active to SPI_CLK first edge	Controller_PHA0_POL 0; Controller_PHA0_POL 1;[5]	-4 + B[6]		ns
			Controller_PHA1_POL 0; Controller_PHA1_POL 1;[5]	-4 + A[7]		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPI_CLK last edge to SPI_CS[x] inactive	Controller_PHA0_POL 0; Controller_PHA0_POL 1;[5]	-4 + A[7]		ns
			Controller_PHA1_POL 0; Controller_PHA1_POL 1; [5]	-4 + B[6]		ns
SM11	Cb	Capacitive load for each bus line		3	15	pF

(1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data
(2) Related to the SPI_CLK maximum frequency
(3) 20 ns cycle time = 50 MHz
(4) P = SPICLK period
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register
(6) B = (TCS + .5) × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even >= 2.
(7) When P = 20.8 ns, A = (TCS + 1) × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
When P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data

注

Supported frequency of Radar SPI Peripheral mode is 40MHz in full cycle and 20MHz in Half cycle mode.

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7.12.4.3.2 Timing and Switching Characteristics for SPI Output Timings—Controller Mode

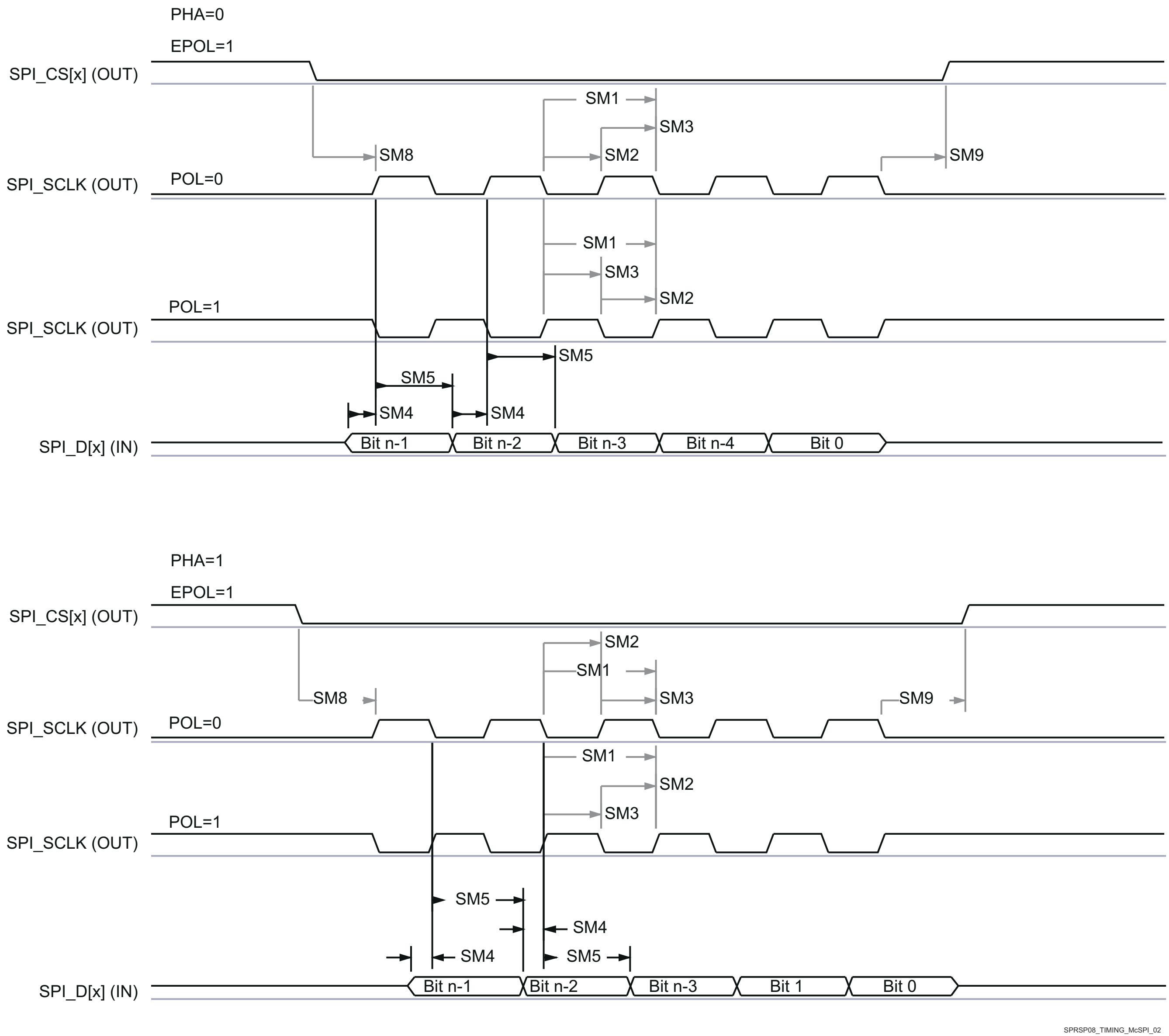

図 7-9. SPI Timing -Controller Mode Receive

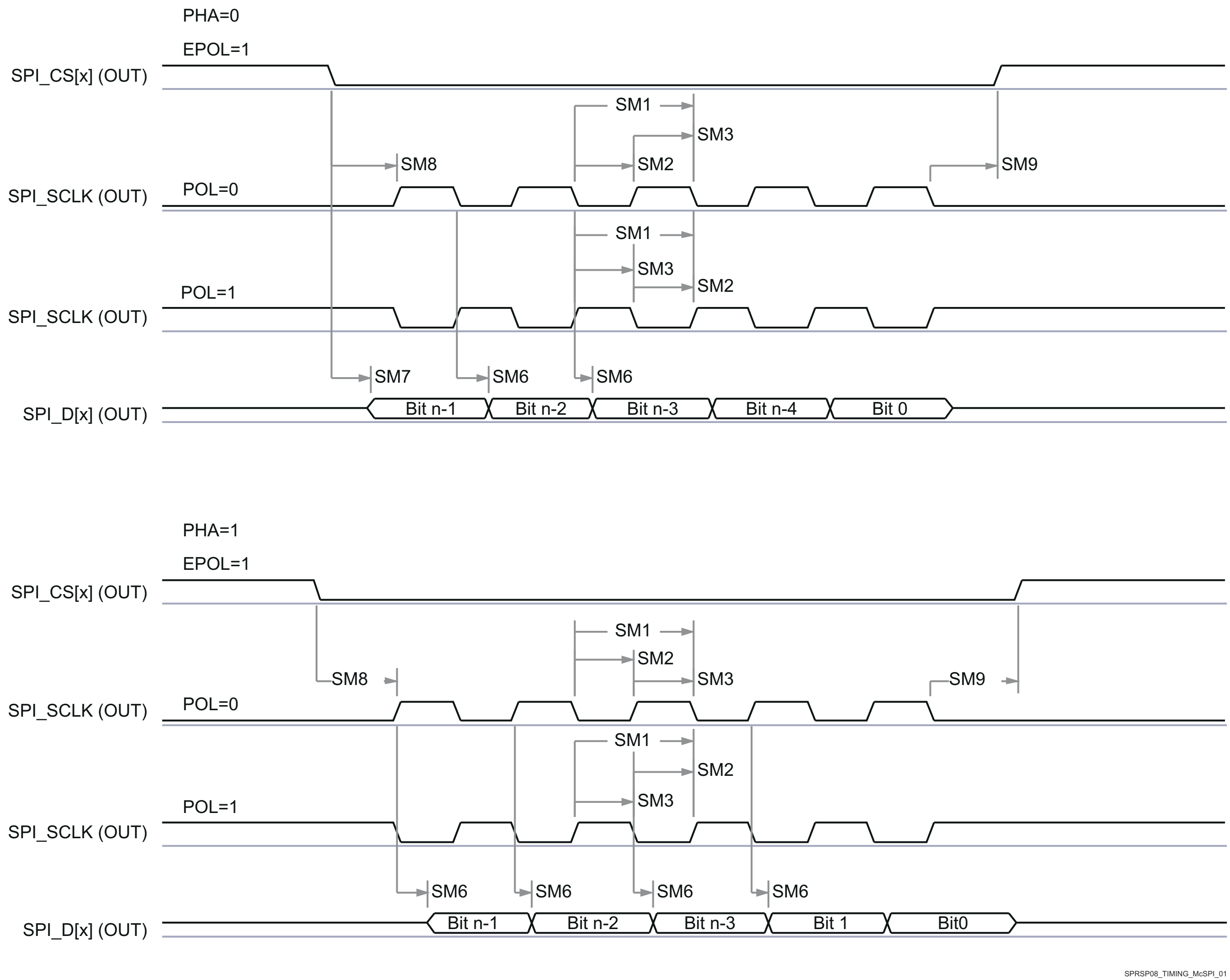

図 7-10. SPI Timing- Controller Mode Transmit

7.12.4.4 SPI—Peripheral Mode

7.12.4.4.1 Timing and Switching Requirements for SPI - Peripheral Mode

表 7-18 and 表 7-19 present timing requirements for SPI -Peripheral Mode.

表 7-18. SPI Timing Requirements - Peripheral Mode

NO.[(1)] [(3)]	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK	24.6		ns
SS2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low	0.45*P[(2)]		ns
SS3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high	0.45*P[(2)]		ns
SS4	$t_{su(SIMO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge	3		ns
SS5	$t_{h(SPICLK-SIMO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge	1		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPI_CS[x] valid before SPI_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPI_CS[x] valid after SPI_CLK last edge	5		ns
SS10	sr	Input Slew Rate for all pins	1	3	ns
SS11	Cb	Capacitive load on D0 and D1	2	15	pF

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表 7-19. SPI Switching Characteristics Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-SOMI)}$	Delay time, SPI_CLK active edge to McSPI_somi transition	0	5.77	ns
SS7	$t_{sk(CS-SOMI)}$	Delay time, SPI_CS[x] active edge to McSPI_somi transition	5.77		ns

(1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) P = SPICLK period.
(3) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

7.12.4.4.2 Timing and Switching Characteristics for SPI Output Timings—Secondary Mode

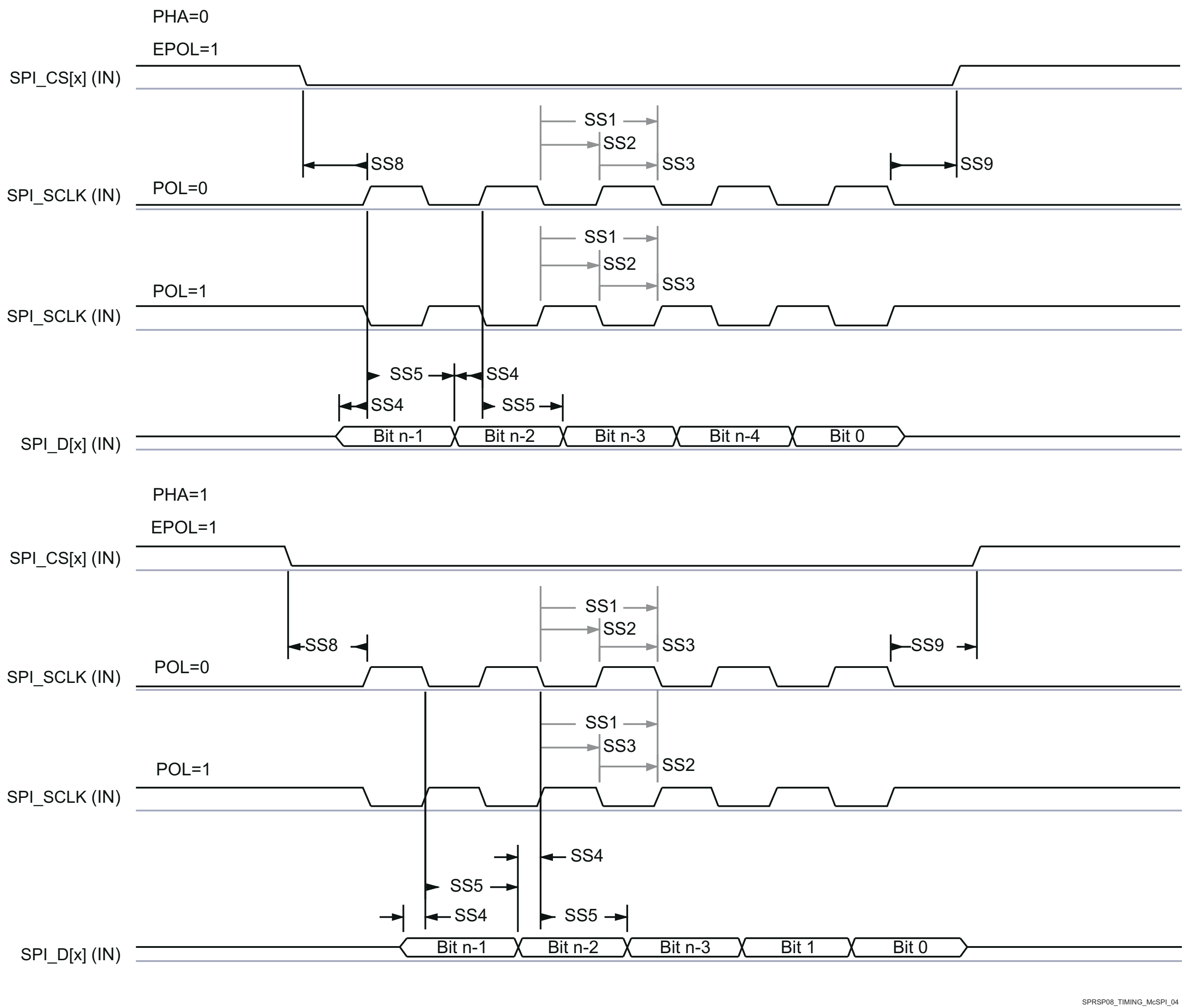

図 7-11. SPI Timing - Peripheral mode Receive

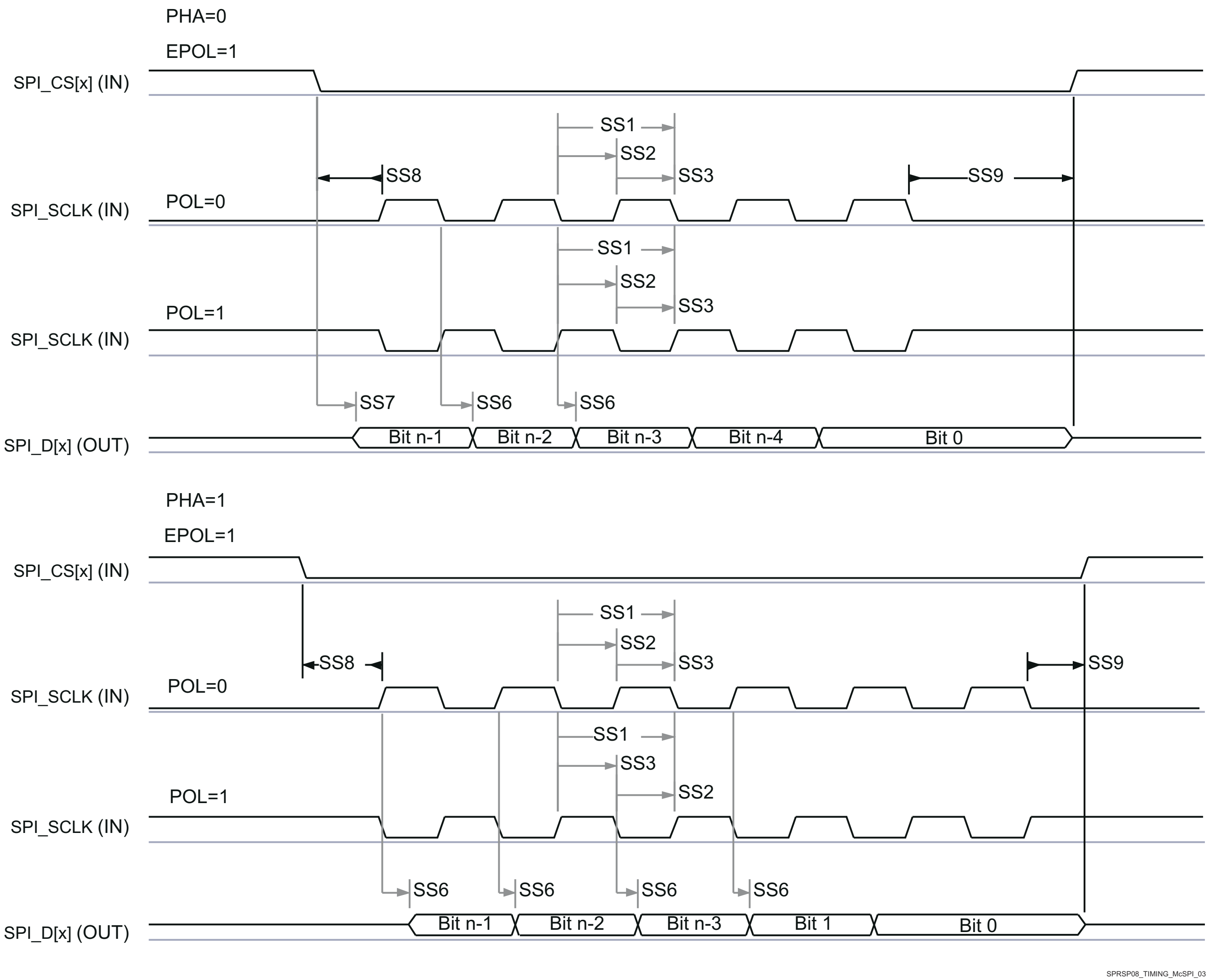

図 7-12. SPI Timing - Peripheral mode Transmit

ADVANCE INFORMATION

7.12.5 RDIF Interface Configuration

The supported Radar Data InterFace (RDIF) is developed as a debug interface (for example: to capture raw ADC data) and not as a production interface. The RDIF has four data lanes, one Bit Clock lane, and one Frame Clock lane. From this interface, high-speed data is sent out for debug purposes. The RDIF interface supports the following data rates[1]:

- 400 Mbps
- 320 Mbps
- 200 Mbps
- 160 Mbps
- 100 Mbps

7.12.5.1 RDIF Interface Timings

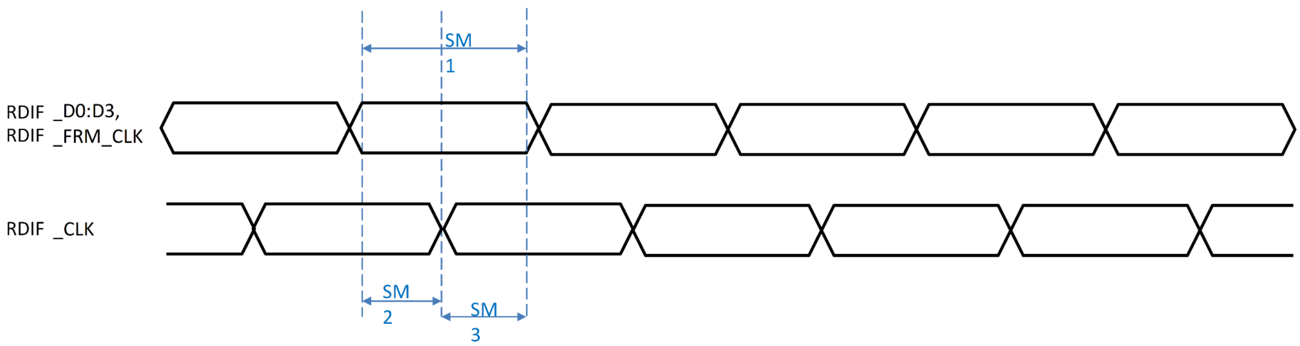

図 7-13. RDIF Timing Requirements

表 7-20. Timing Requirements for RDIF Interface

No.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	Tb (RDIF_D[x])	Bit Interval, RDIF_d[x]	Internal Clock	9.6		ns
SM2	Tvb (RDIF_D[x] - RDIF_CLK)	Data valid time, RDIF_d[x] and RDIF_frm_clk valid before RDIF_clk active edge	Internal Clock	4.8		ns
SM3	Tva (RDIF_CLK - RDIF_D[x])	Data valid time, RDIF_d[x] valid after RDIF_clk active edge	Internal Clock	4.8		ns
SM4	C_b	Capacitive load for each bus line		3	15	pF

1 Aggregated data rate over four data lanes.

7.12.5.2 RDIF Data Format

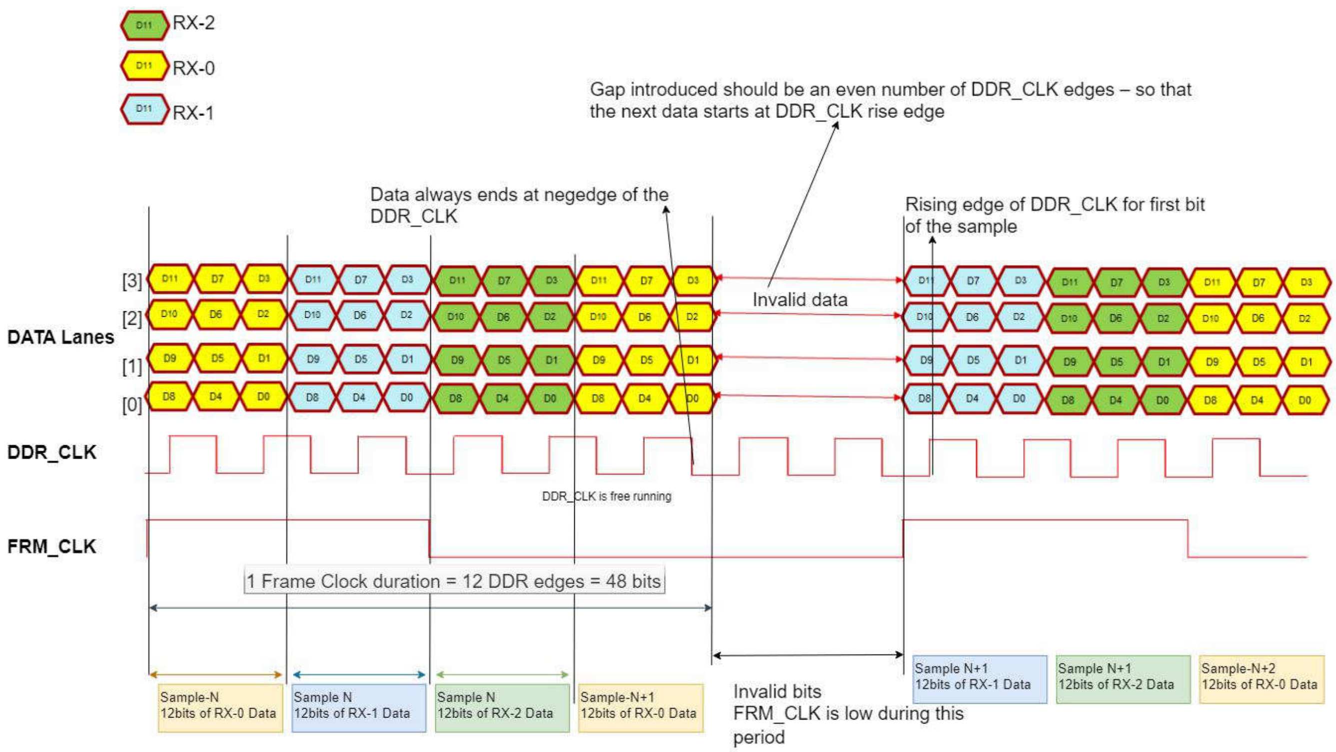

図 7-14. RDIF Data Format

- The samples are sent one channel by one channel as shown in the diagram above. All the 12-bits of one channel are sent on 4 data lanes in 3 DDR_CLK edges, followed by next RX channel.
- The frame clock (FRM_CLK) spans 12 DDR_CLK edges and 48 bits are sent in 1 FRM_CLK
- The FRM_CLK can have gaps in between. This is required as the interface rate is greater than the incoming rate
- DDR_CLK is continuous.
- DDR_CLK is generated from 400MHz ADC CLK (one of the ADC CLKs) - selected for the DFE. It is the same 400MHz clock selected for DFE.
- New sample always starts at the rise edge of the DDR_CLK
- The FRM_CLK is valid for the entire data bit and is meets the Tsu/Th wrt DDR_CLK.

7.12.6 LIN

The LIN module can be programmed to work either as an SCI or as a LIN. The SCI hardware features are augmented to achieve LIN compatibility. The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-/ multiple- with a message identification for multicast transmission between any network nodes.

The LIN has following features:

- Compatibility with LIN 1.3 , 2.0, and 2.1 protocols
- Configurable Baud Rate up to 20 kpbs
- Two external pins: LINRX and LINTX.
- Multi-buffered receive and transmit units
- Identification masks for message filtering
- Automatic Controller header generation
  - Programmable synchronization break field
  - Synchronization field

  - Identifier field
- Peripheral automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- 231 programmable transmission rates with 7 fractional bits
- Wake up on LINRX dominant level from transceiver
- Automatic wake up support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- Capability to use Direct Memory Access (DMA) for transmit and receive data.
- 2 Interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

表 7-21. LIN Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate	1		20	kHz

7.12.7 General-Purpose Input/Output

7.12.7.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

表 7-22 lists the switching characteristics of output timing relative to load capacitance.

表 7-22. Switching Characteristics for Output Timing versus Load Capacitance (C_L)

PARAMETER[(1) (2)]		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	

表 7-22. Switching Characteristics for Output Timing versus Load Capacitance (C_L) (続き)

PARAMETER(1) (2)		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

ADVANCE INFORMATION

7.12.8 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

7.12.8.1 Dynamic Characteristics for the CANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_FD\_tx)}$	Delay time, transmit shift register to CAN_FD_tx pin(1)			15	ns
$t_{d(CAN\_FD\_rx)}$	Delay time, CAN_FD_rx pin to receive shift register(1)			15	ns

(1) These values do not include rise/fall times of the output buffer.

7.12.9 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions in compatibility mode
- Supports two individually enabled interrupt lines: level 0 and level 1
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from one to eight bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or one parity bit, odd or even parity
  - Stop programmable for one or two stop bits
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Two multiprocessor communication formats allow communication between more than two devices
- Sleep mode is available to free CPU resources during multiprocessor communication and then wake up to receive an incoming message
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Five error flags and Seven status flags provide detailed information regarding SCI events
- Two external pins: RS232_RX and RS232_TX
- Multi-buffered receive and transmit units

7.12.9.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		115200		Hz

7.12.10 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multi-controller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^2C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - START byte
  - Multi-controller transmitter/ target receiver mode
  - Multi-controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

注

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

ADVANCE INFORMATION

7.12.10.1 I2C Timing Requirements

		STANDARD MODE (1)		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45 (1)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

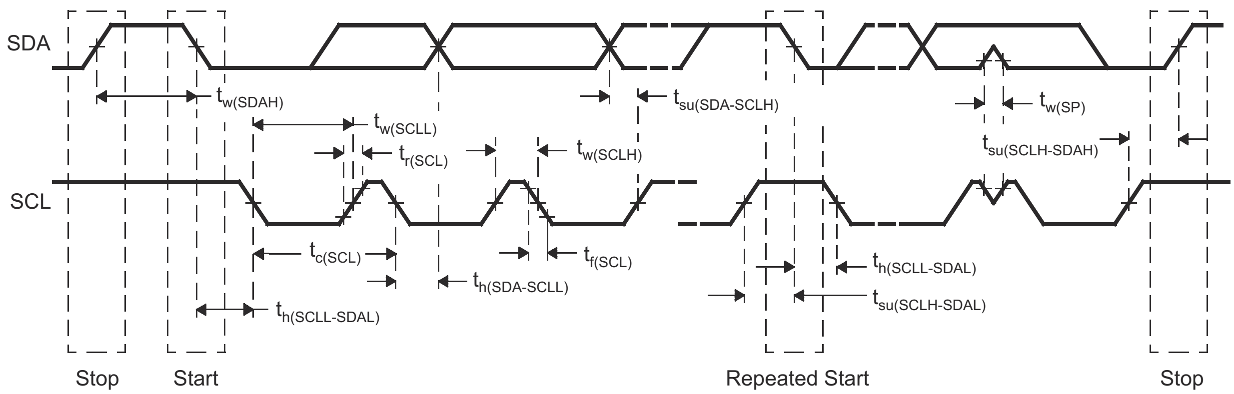

図 7-15. I2C Timing Diagram

注

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

7.12.11 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

セクション 7.12.11.2 and セクション 7.12.11.3 assume the operating conditions stated in セクション 7.12.11.1.

7.12.11.1 QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.12.11.2 Timing Requirements for QSPI Input (Read) Timings

		MIN[(1)] [(2)]	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	5			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	5 – P[(3)]			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1 + P[(3)]			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

ADVANCE INFORMATION

7.12.11.3 QSPI Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	12.5			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	Y*P – 3[1] [2]			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	Y*P – 3[1] [2]			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1[2] [3]		–M*P + 2.5[2] [3]	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1[2] [3]		N*P + 2.5[2] [3]	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[1] transition	–2		4	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[1] driven (lo-z)	–P – 4[2]		–P +1[2]	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[1] tri-stated (hi-z)	–P – 4[2]		–P +1[2]	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–2 – P[2]		4– P[2]	ns
Q12	$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	5			ns
Q13	$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1			ns
Q14	$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	5 — P[2]			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1 + P[2]			ns

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

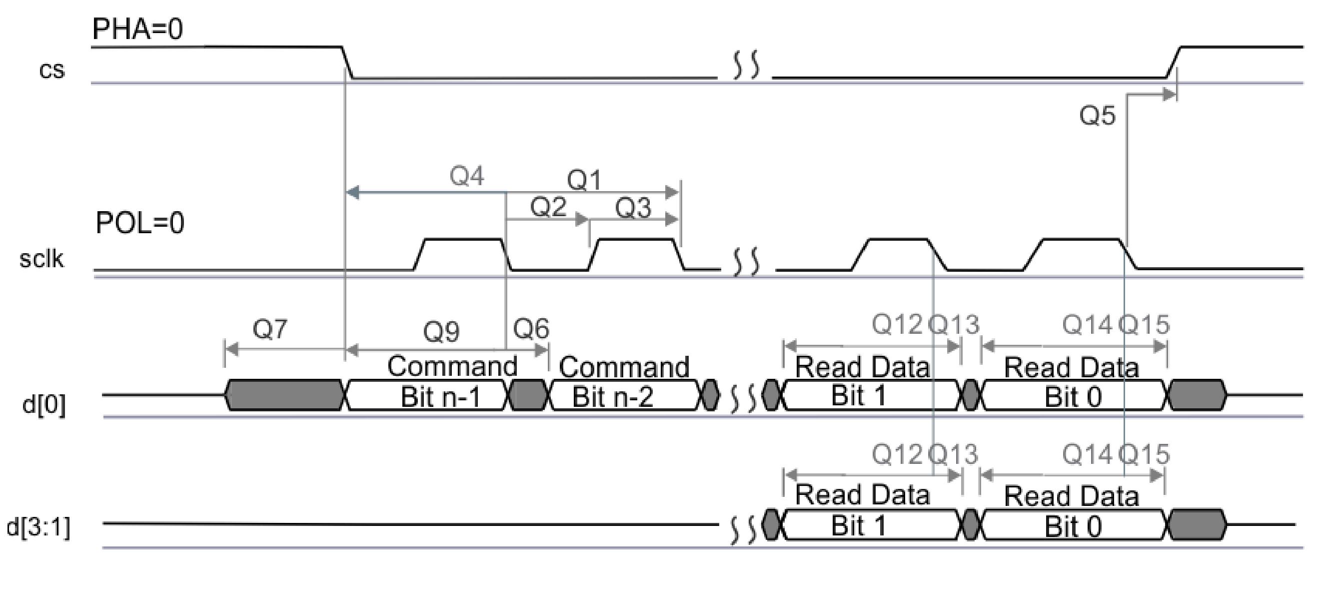

図 7-16. QSPI Read (Clock Mode 0)

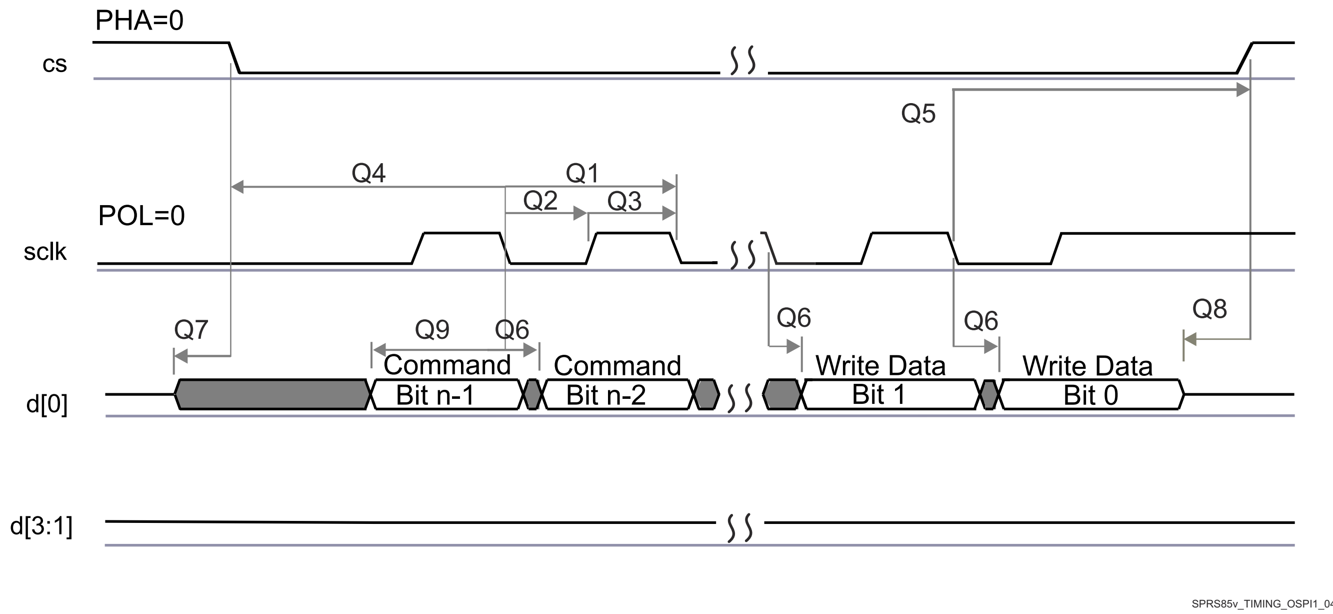

図 7-17. QSPI Write (Clock Mode 0)

ADVANCE INFORMATION

ADVANCE INFORMATION

7.12.12 JTAG Interface

セクション 7.12.12.2 and セクション 7.12.12.3 assume the operating conditions stated in セクション 7.12.12.1.

7.12.12.1 JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.12.12.2 Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	20			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	20			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

7.12.12.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		15	ns

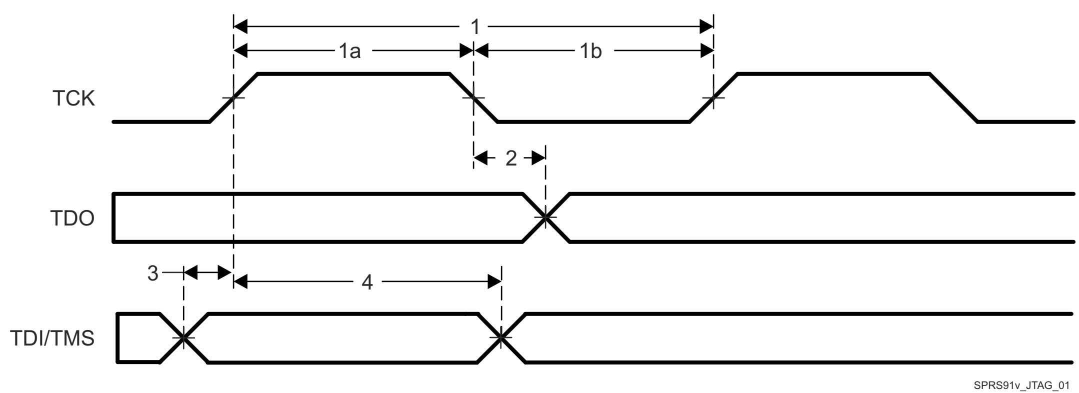

図 7-18. JTAG Timing

8 Detailed Description

8.1 Overview

The AWRL1432 device is a complete SOC which include mmWave front end, customer programmable MCU and analog baseband signal chain for two transmitters and three receivers. This device is applicable as a radar-on-a-chip in use-cases with quality provision for memory, processing capacity, and application code size. These could be cost-effective automotive applications that are evolving from 24-GHz narrowband implementation and some emerging radar applications. Typical application examples for this device include gesture detection and kick sensor. In terms of scalability, the AWRL1432 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. The AWRL1432 device also provides high speed data interfaces like RDIF and is suitable for ADC capture.

ADVANCE INFORMATION

8.2 機能ブロック図

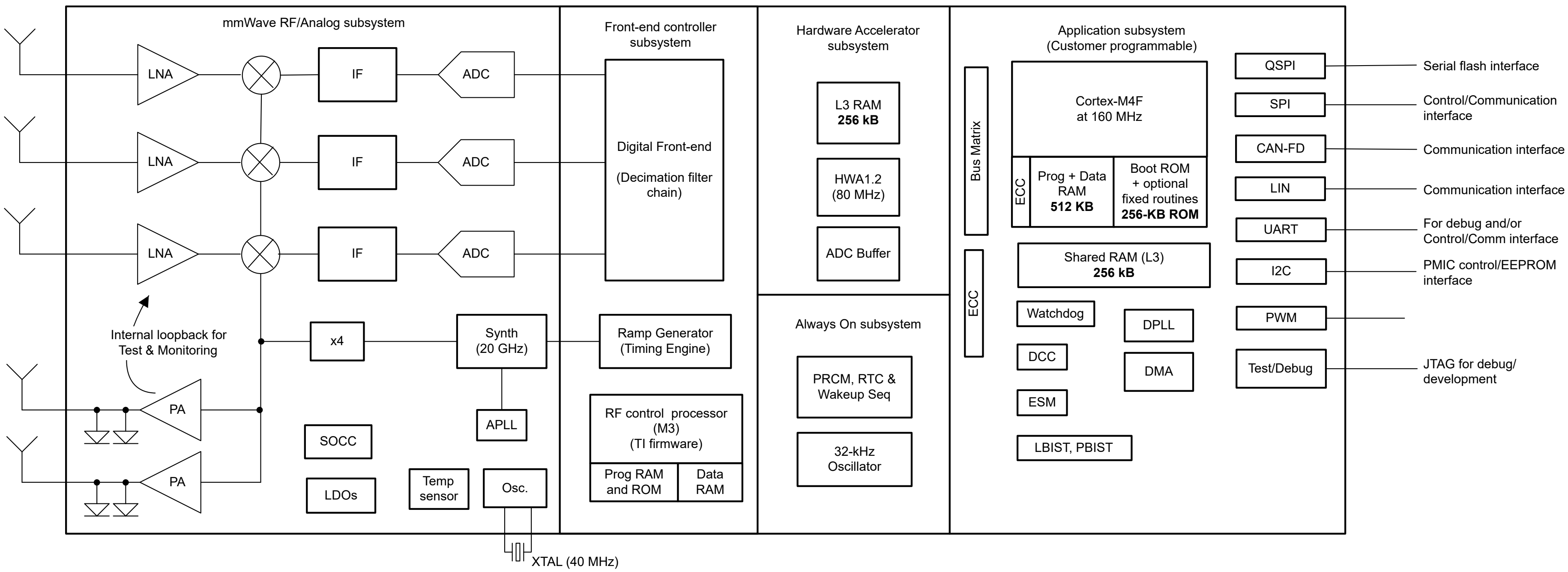

図 8-1. 機能ブロック図

8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The two TX can be operated simultaneously for beam forming in BPM mode or individually in TDM mode. Similarly, the device allows configuring the number of receive channels based on application and power requirements. For system power saving, RF and analog subsystems can be put into low power mode configuration.

8.3.2 Clock Subsystem

The AWRL1432 clock subsystem generates 76 to 81 GHz from an input reference from a crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

図 8-2 describes the clock subsystem.

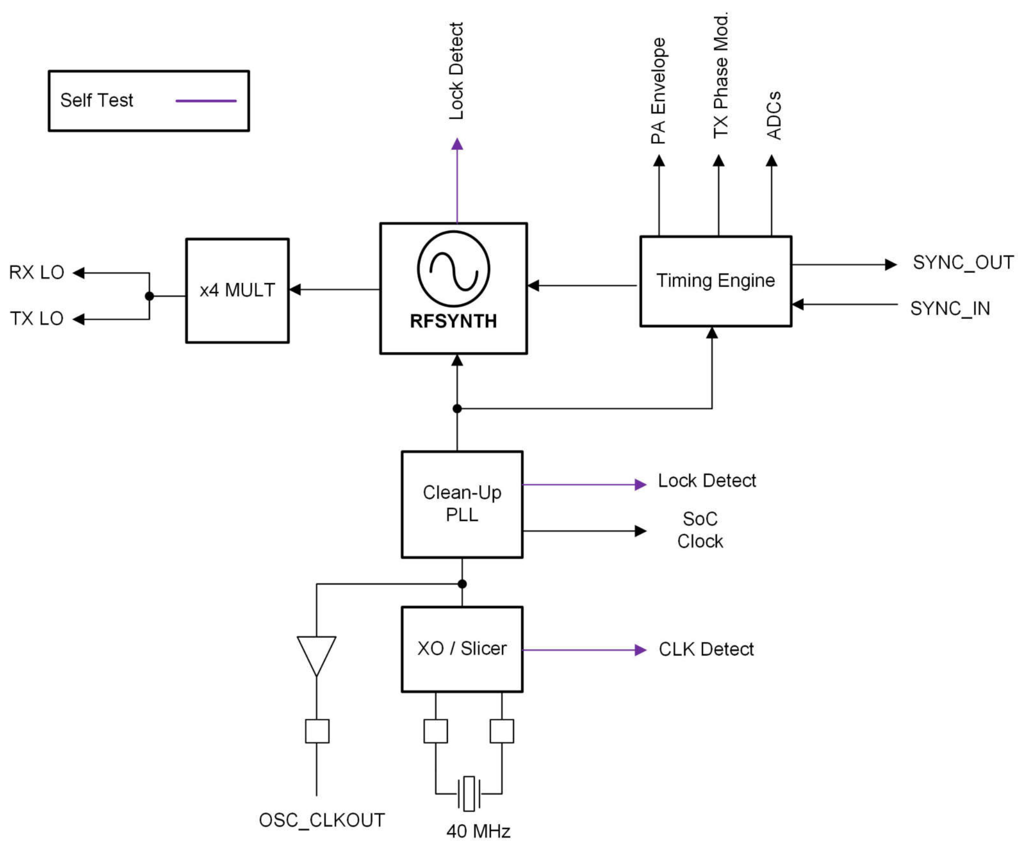

図 8-2. Clock Subsystem

ADVANCE INFORMATION

8.3.3 Transmit Subsystem

The AWRL1432 transmit subsystem consists of two parallel transmit chains, each with independent phase and amplitude control. The device supports binary phase modulation for MIMO radar.

The transmit chains also support programmable backoff for system optimization.

図 8-3 describes the transmit subsystem.

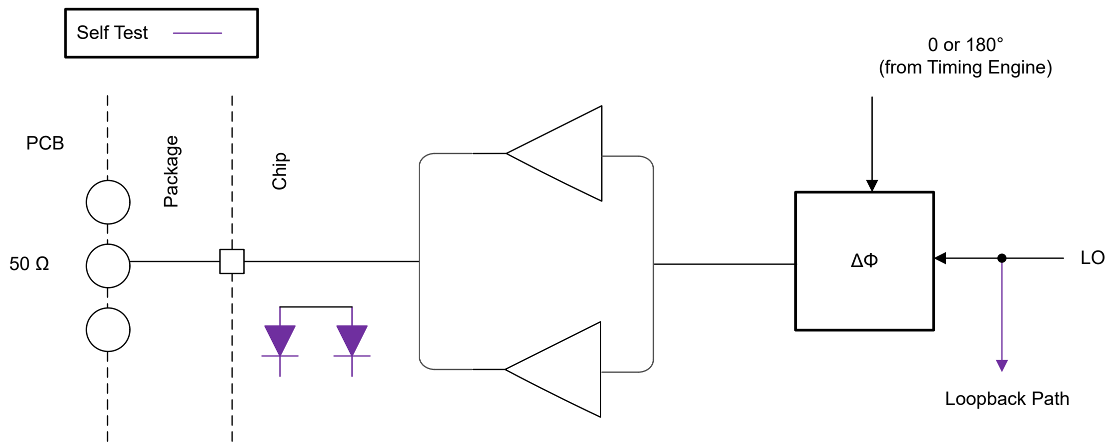

図 8-3. Transmit Subsystem (Per Channel)

8.3.4 Receive Subsystem

The AWRL1432 receive subsystem consists of three parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All three receive channels can either operate simultaneously OR can be powered down individually based on system power needs and application design.

The AWRL1432 device supports a real baseband architecture, which uses real mixer, single IF and ADC chains to provide output for each receiver channel. The device is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 5 MHz.

図 8-4 describes the receive subsystem.

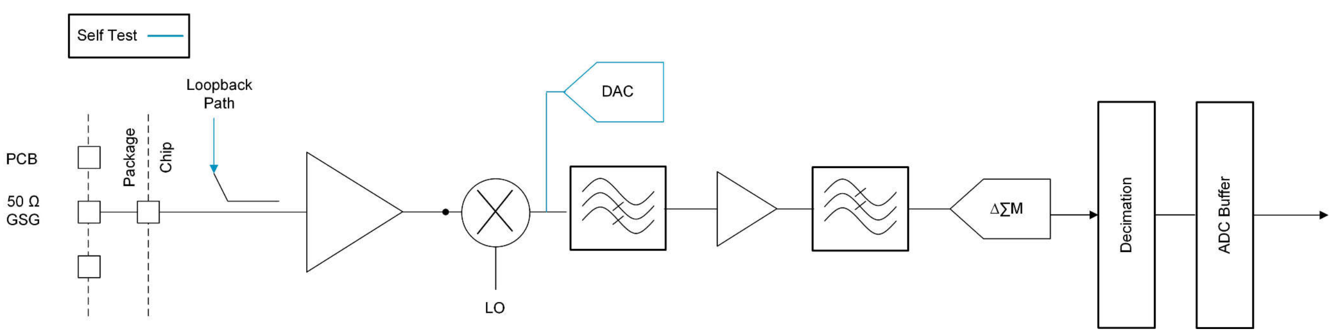

図 8-4. Receive Subsystem (Per Channel)

8.3.5 Processor Subsystem

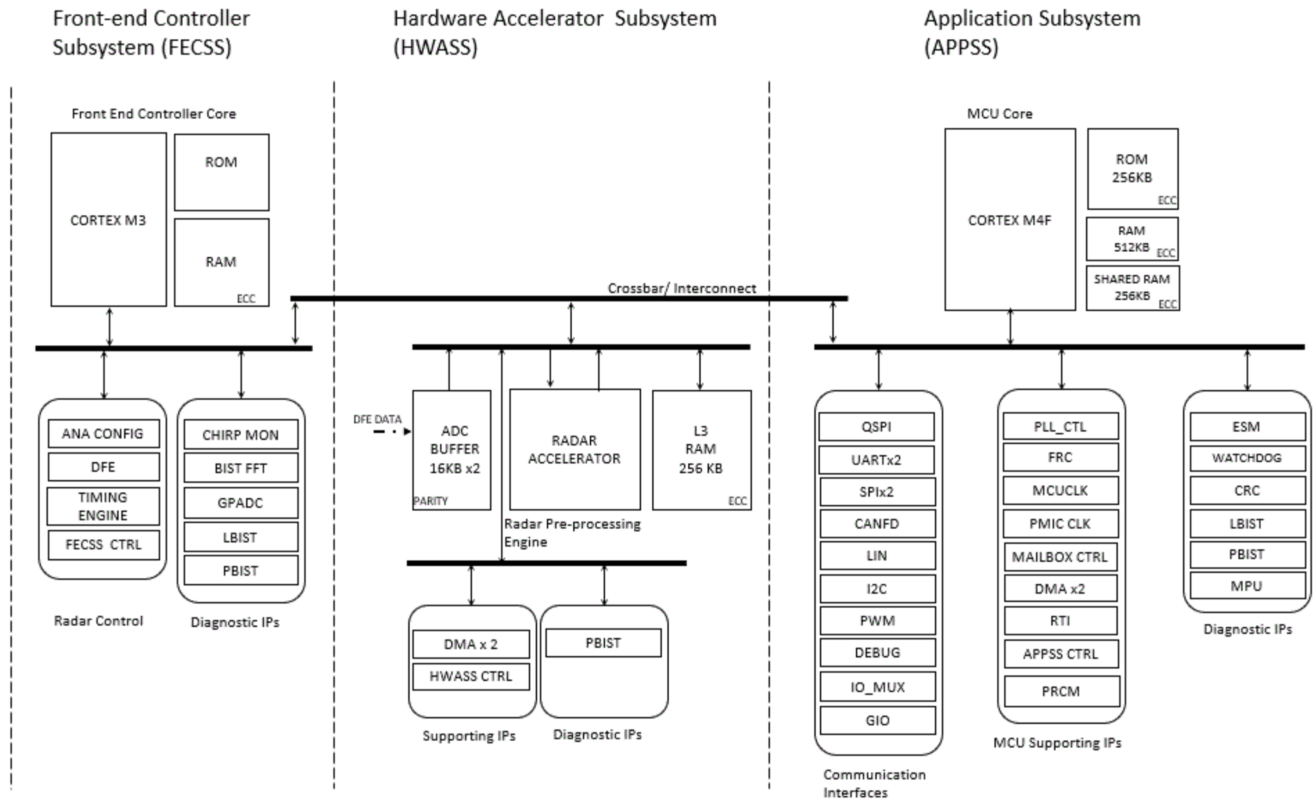

図 8-5. Processor Subsystem

図 8-5 shows the block diagram for customer programmable processor subsystems in the AWRL1432 device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. The left hand side shows the HWA, a high-bandwidth interconnect for high performance (64-bit, 80MHz), and associated peripherals data transfer. RDIF interface for Measurement data output, L3 Radar data cube memory, the ADC buffers, the CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Main Subsystem. The Main Subsystem is the brain of the device and controls all the device peripherals and house-keeping activities of the device. The Main Subsystem contains Cortex-M4F processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I^2C, UART, SPIs, CAN, PMIC clocking module, PWM, LIN,and others) connected to Main Interconnect through Peripheral Central Resource (PCR interconnect).

8.3.6 Automotive Interface

The AWRL1432 communicates with the automotive network over the following main interfaces:

- CAN-FD
- LIN

ADVANCE INFORMATION

8.3.7 Host Interface

The host interface can be provided through a SPI, LIN, UART, or CAN-FD interface.

The AWRL1432 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral) for host control . All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host.
- Host Interrupt - an indication that the mmWave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

8.3.8 Main Subsystem Cortex-M4F

The main system includes an ARM Cortex M4F processor clocked with a maximum operating frequency of 160 MHz. User applications executing on this processor control the overall operation of the device, including radar control through well-defined API messages, radar signal processing (assisted by the radar hardware accelerator), and peripherals for external interfaces.

See the Technical Reference Manual for a complete description and memory map.

8.3.9 Hardware Accelerator (HWA1.2) Features

- Fast FFT computation, with programmable 2^N sizes, up to 1024-point complex FFT
- Internal FFT bit-width of 24 bits for good Signal-to-Quantization-Noise Ratio (SQNR) performance
- Fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for pre-FFT processing – Ex: DC estimation and subtraction
- DC estimation & subtraction, Interference estimation & zero-out, Real window, Complex pre-multiplication
- Magnitude (absolute value) and Log-magnitude computation
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
- Chaining and looping mechanism to sequence a set of operations one after another with minimal intervention from the main processor
- Peak detection – CFAR (CFAR-CA, CFAR-OS) detector
- Basic statistics, including Sum and 1D Max
- Compression engine for radar cube memory optimization

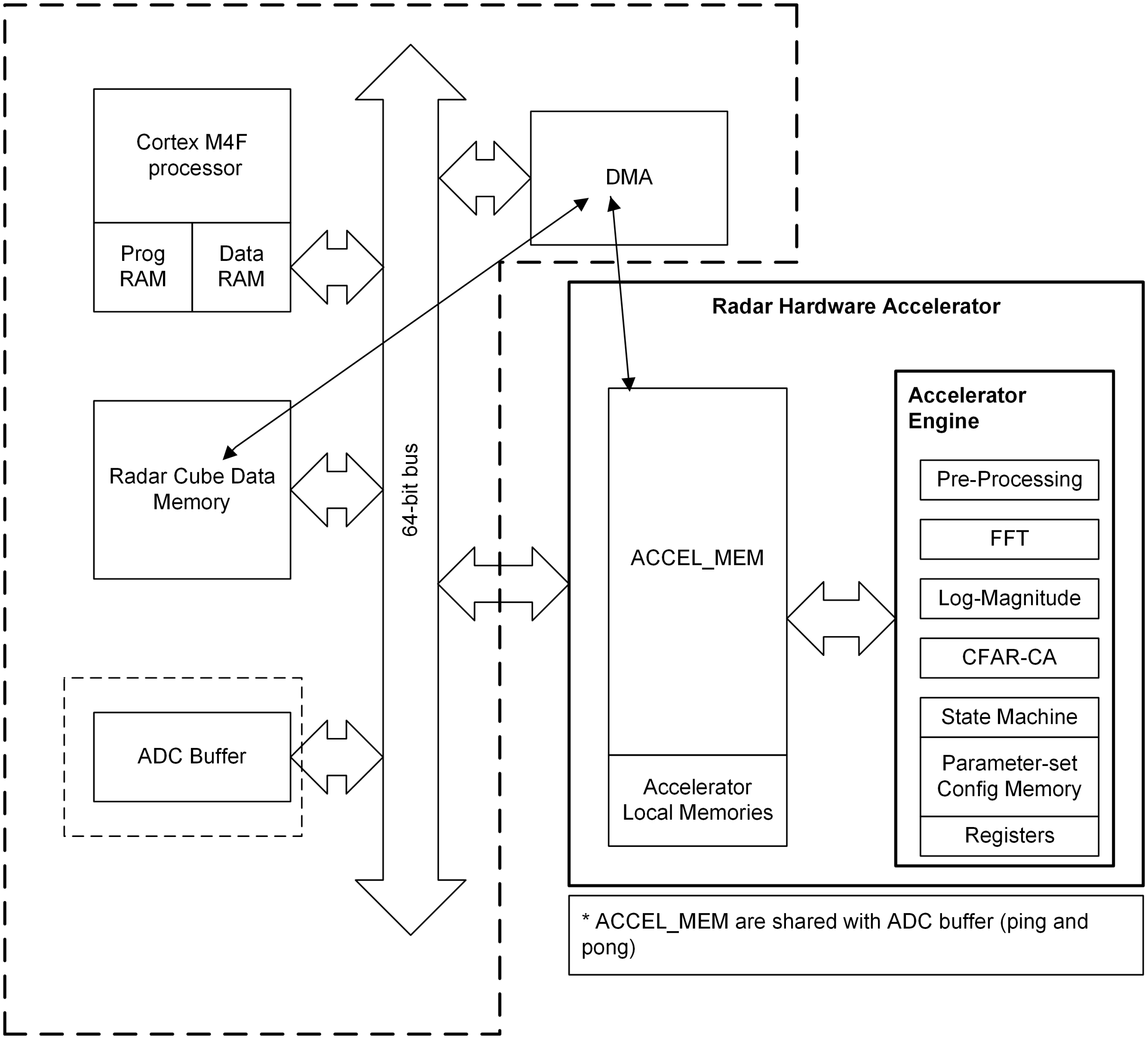

図 8-6. HWA 1.2 Functional Block Diagram

8.3.9.1 Hardware Accelerator Feature Differences Between HWA1.1 and HWA1.2

Feature		**HWA1.0, HWA1.1 (xWR1843, xWR6843)**	**HWA1.2 (xWRL6432, xWRL1432)**
FFT features	FFT sizes	1024, 512, 256, ...	1024, 512, 256, ...
	Internal bit-width	24-bit I, 24-bit Q	24-bit I, 24-bit Q
		Configurable butterfly scaling at each stage	Configurable butterfly scaling at each stage
	FFT stitching	up to 4096 point	up to 4096 point
FFT benchmark for **four** 256-pt FFTs		1312 clock cycles (6.56 µs at 200 MHz)	1320 clock cycles (16.5 µs at 80 MHz)
No. of parameter-sets		16	32
Local memory		64KB	64KB

Feature	HWA1.0, HWA1.1 (xWR1843, xWR6843)	HWA1.2 (xWRL6432, xWRL1432)
Input and Output formatter	• A and B-dim addressing of local memory • Programmable scaling	• A and B-dim addressing of local memory • Programmable scaling
Pre-FFT processing	• Interference zero out with fixed threshold, based on magnitude • Complex multiplication (7 modes) • Real window coefficients	• DC estimation and subtraction • Interference zero out with adaptive statistics, based on mag, mag-diff. Interference count indication. • Complex multiplication (7 modes) • Real window coefficients
Post-FFT processing	Log-magnitude (0.3 dB accuracy)	Log-magnitude (0.06 dB accuracy)
Compression and De-compression support	Not available in HWA1.0 (xWR1843), Available in HWA1.1 (xWR6843)	Available
Detection	CFAR-CA (linear and log modes)	• CFAR-CA (linear and log modes) • CFAR-OS (window size up to 32 on each side)
Statistics	1D Sum, 1D Max	1D Sum, 1D Max

8.4 Other Subsystems

8.4.1 GPADC Channels (Service) for User Application

The AWRL1432 device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to two external voltages. The GPADC1, and GPADC2 pins are used for this purpose.

- GPADC itself is controlled by TI firmware running inside the FEC subsystem and access to it for customer's external voltage monitoring purpose is via 'APPSS' calls routed to the FEC subsystem. This API could be linked with the user application running on MSS M4F.
- Device Firmware package (DFP) provides APIs to configure and measure these signals. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

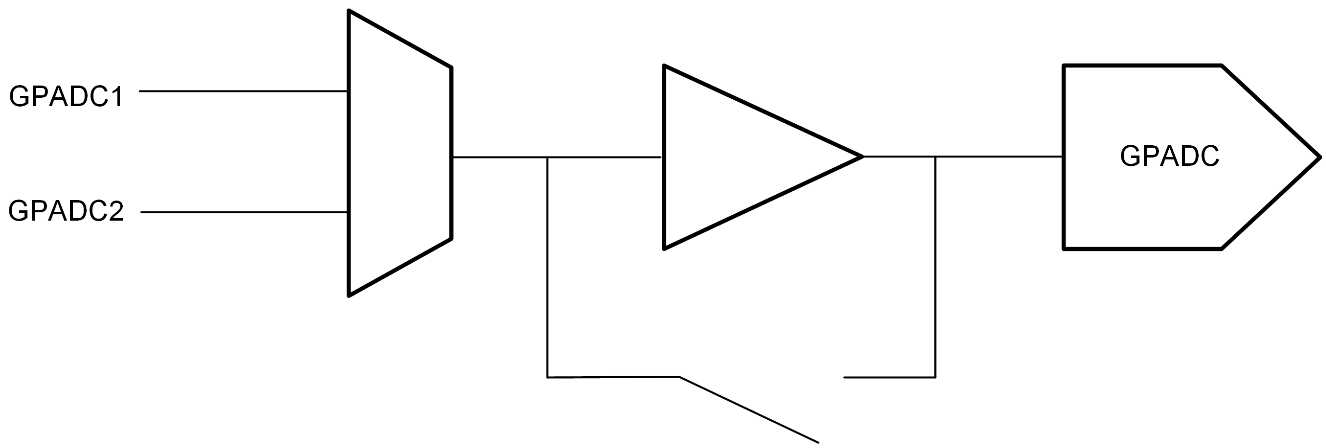

図 8-7. GPADC Path

GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7°C.

8.4.2 GPADC Parameters

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	8	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate(2)	831	Ksps
ADC sampling time(2)	300	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.
(2) GPADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

8.5 Memory Partitioning Options

AWRL1432 devices will have a total memory of 1MB. The L3 memory has two memory banks and can be associated with radar cube memory or with the Cortex-M4F RAM.

表 8-1. Memory Partition Options

		Config 1	Config 2	Config 3
Radar data memory* (L3)	Includes data cube, detection matrix, heatmap	256KB	384kB	512KB
Application (M4F program + data)	Includes drivers, mmWavelink, BIOS (and AUTOSAR)	768KB	640KB	512KB
Total memory		1024KB	1024KB	1024KB

ADVANCE INFORMATION

The entire RAM is retainable. Additionally, each memory cluster can be independently turned off (if needed). The clusters are defined as below

表 8-2. Memory Retention Options

<table>
<tr><th colspan="3">RAM_1</th><th colspan="2">RAM_2</th><th>RAM_3</th><th>Shared</th><th>HWA</th></tr>
<tr><td colspan="3">256KB</td><td colspan="2">128KB</td><td>128KB</td><td>256KB</td><td>256KB</td></tr>
<tr><td colspan="3">BANK #1(1)</td><td colspan="2">BANK #2</td><td>BANK #3</td><td></td><td></td></tr>
<tr><td>Cluster #1</td><td>Cluster #3</td><td>Cluster #4</td><td>Cluster #2</td><td colspan="2">Cluster #5</td><td>Cluster #6</td><td></td></tr>
<tr><td>64kB</td><td>64KB</td><td>128KB</td><td>16KB</td><td>112KB</td><td>128KB</td><td>256KB</td><td>256KB</td></tr>
</table>

(1) Retention memories have power switches. These Banks represent memory configurations.

8.6 Boot Modes

As soon as device reset is de-asserted, the processor of the APPSS starts executing its bootloader from an on-chip ROM memory.

The bootloader operates in three basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

表 8-3 enumerates the relevant SOP combinations and how these map to bootloader operation.

表 8-3. SOP Combinations

SOP1	SOP0	BOOTLOADER MODE AND OPERATION
0	0	**Flashing Mode** Device Bootloader spins in loop to allow flashing of user application (or device firmware patch - Supplied by TI) to the serial flash.
0	1	**Functional Mode** Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it.
1	1	**Debug Mode** Bootloader is bypassed and M4F processor is halted. This allows user to connect emulator at a known point.

9 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Application information can be found on AWR Application web page.

9.2 Reference Schematic

Please check the device product page for latest Hardware design information under Design Kits - typically, at Design and Development

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB

- Altium AWRL1432 EVM Design Files
- AWRL1432 EVM Schematic Drawing, Assembly Drawing, and Bill of Materials

ADVANCE INFORMATION

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWRL1432*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). 図 10-1 provides a legend for reading the complete device name for any *AWRL1432*device.

For orderable part numbers of *AWRL1432* devices in the ABL0161 package types, see the Package Option Addendum of this document (when available), the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the AWRL1432 Device Errata ..

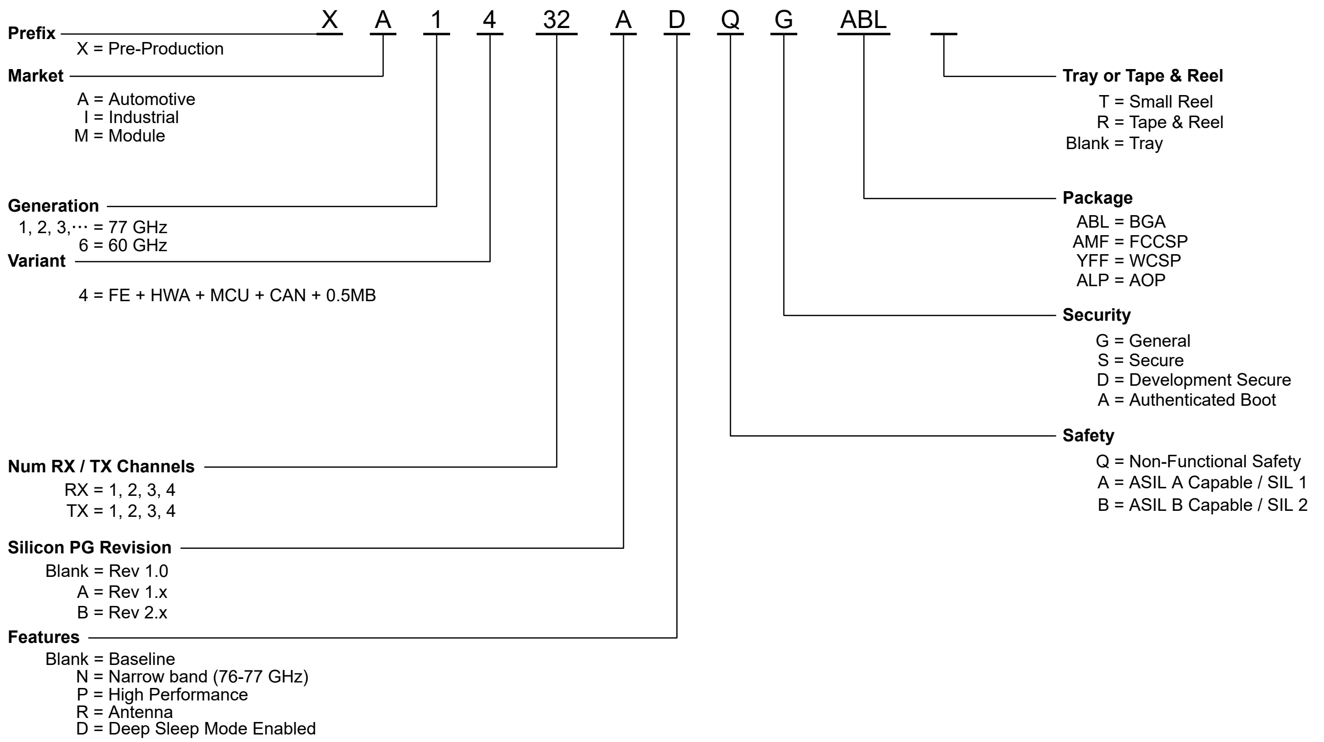

図 10-1. Device Nomenclature

10.2 Tools and Software

Models

AWRL1432 BSDL model — Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

AWRL1432 IBIS model — IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the peripherals, and other technical collateral follows.

Errata

AWRL1432 Device Errata . Describes known advisories, limitations, and cautions on silicon and provides workarounds.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help—straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

E2E™ is a trademark of Texas Instruments.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from July 1, 2023 to February 28, 2024 (from Revision * (July 2023) to Revision A (February 2024)) **Page**

- 「概要」セクションのアプリケーションを更新 2

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

ADVANCE INFORMATION

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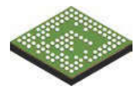
PACKAGING INFORMATION

OPNs	BL	TRAY / TAPE AND REEL	Purpose
XA1432ADQGAMF	BODY		Pre-production ES1.1. Low Power, Deep Sleep Enabled
XA1432BDBAAMF	BODY		Pre-production ES2.0. ASIL-B targeted. Low Power, Deep Sleep Enabled. Authenticated Boot.
AWRL1432BDBGAMFRQ1	BODY	Tape and Reel	Automotive production variant ES2.0. ASIL-B targeted. Low Power, Deep Sleep enabled. High quantity.
AWRL1432BDBGAMFQ1	BODY	Tray	Automotive production variant ES2.0. ASIL-B targeted. Low Power, Deep Sleep enabled. Low quantity.
AWRL1432BDBAAMFRQ1	BODY	Tape and Reel	Automotive production variant ES2.0. ASIL-B targeted. Low Power, Deep Sleep enabled. Authenticated Boot. High quantity.
AWRL1432BDBAAMFQ1	BODY	Tray	Automotive production variant ES2.0. ASIL-B targeted. Low Power, Deep Sleep enabled. Authenticated Boot. High quantity.

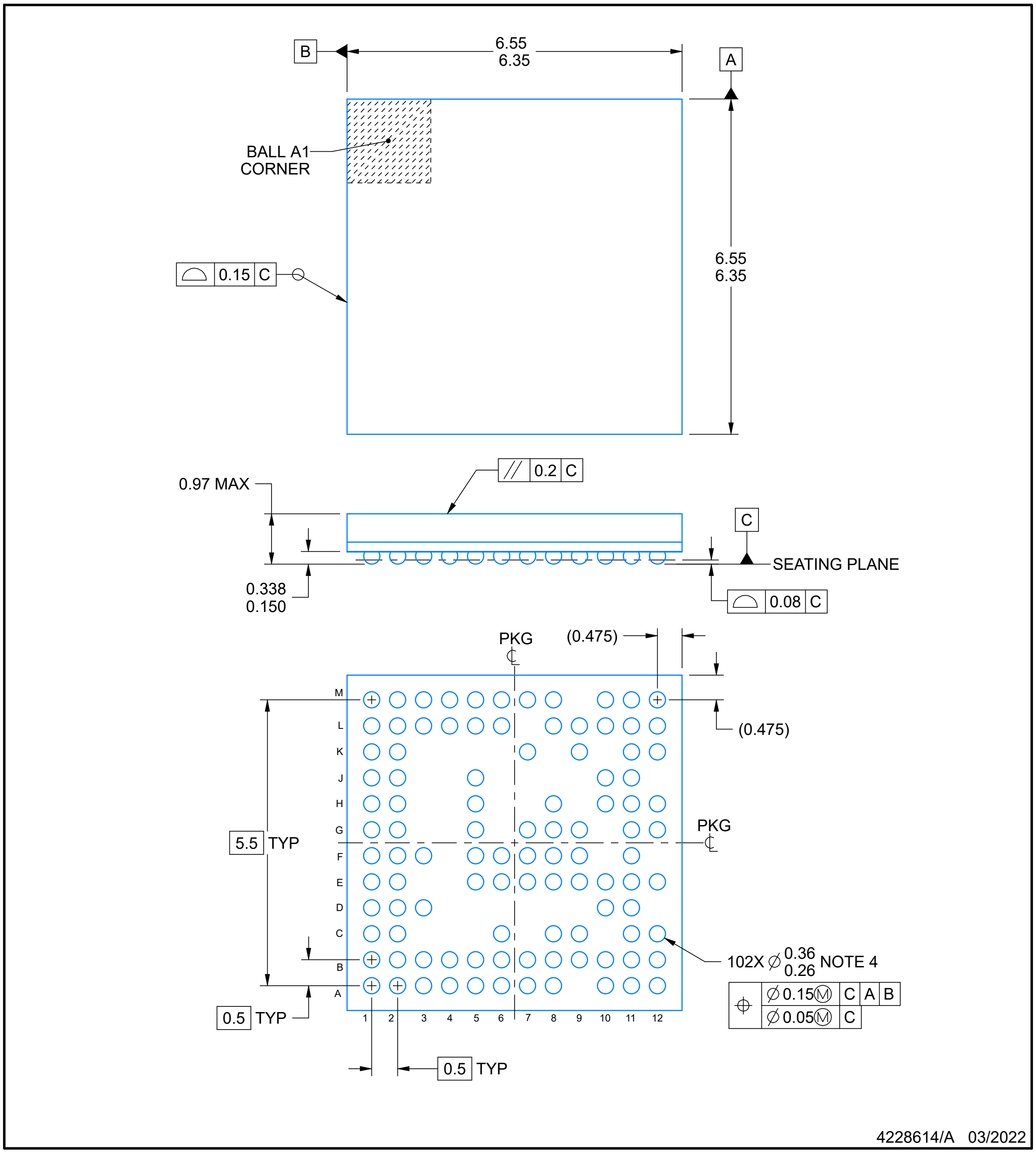
PACKAGE OUTLINE



AMF0102A

FCCSP - 0.97 mm max height

FLIP CHIP CHIP SCALE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C.

ADVANCE INFORMATION

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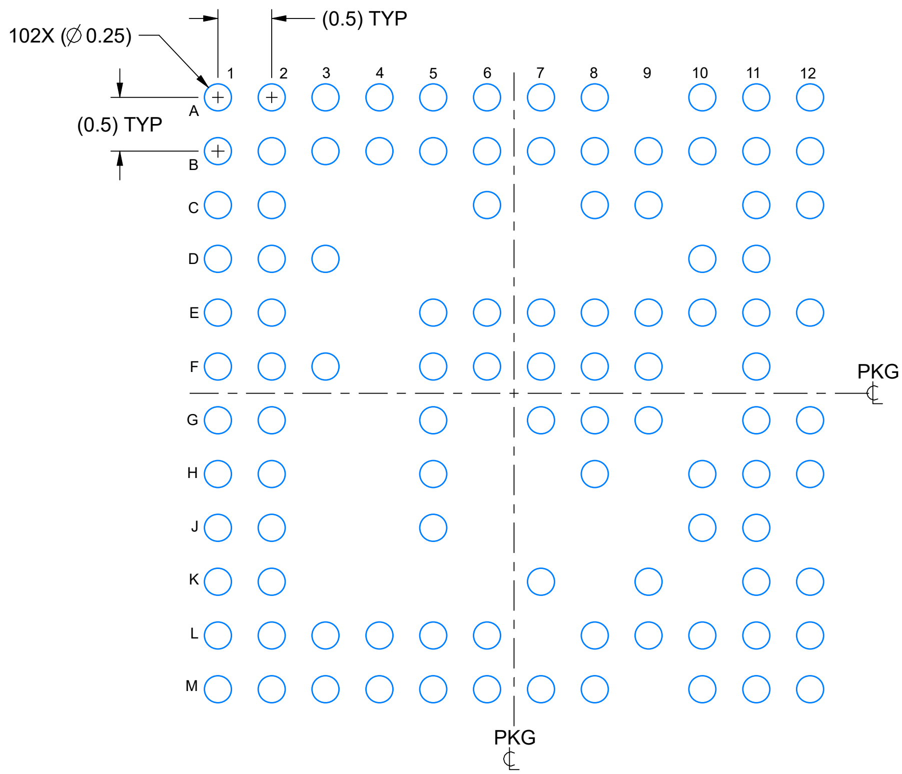
EXAMPLE BOARD LAYOUT

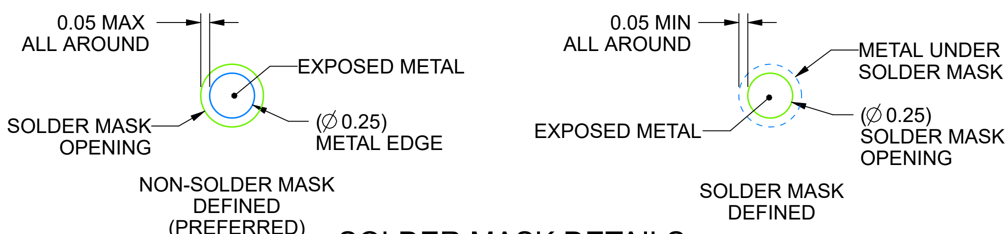
AMF0102A

FCCSP - 0.97 mm max height

FLIP CHIP CHIP SCALE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

4228614/A 03/2022

NOTES: (continued)

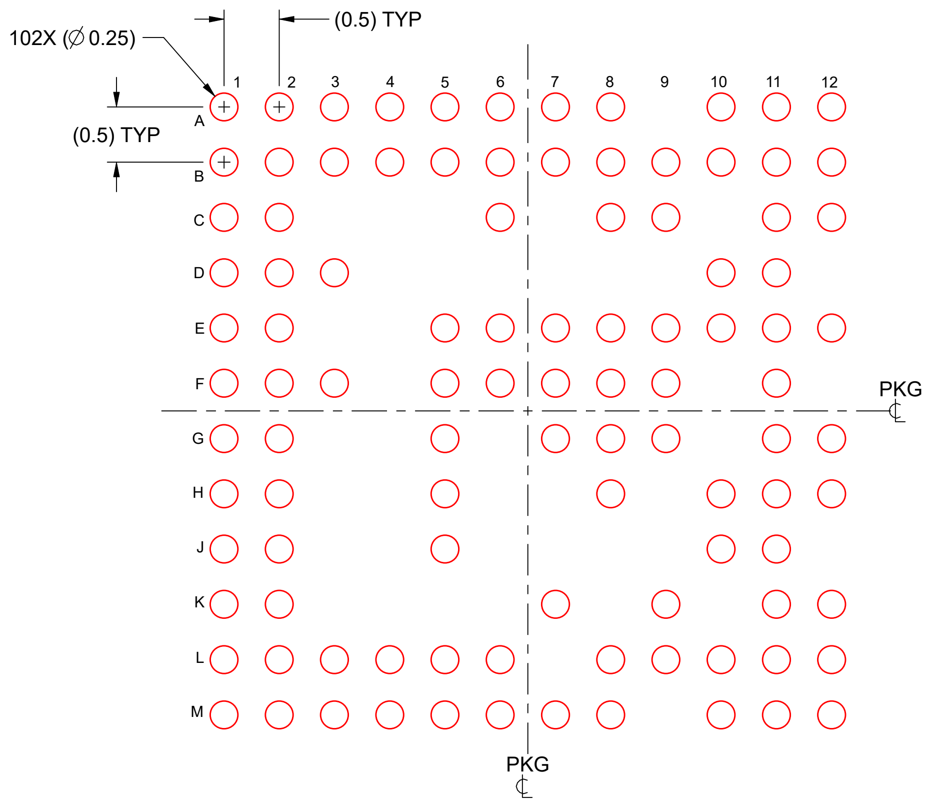
5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

AMF0102A

FCCSP - 0.97 mm max height

FLIP CHIP CHIP SCALE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

4228614/A 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XA1432ADQGAMF	ACTIVE	FCCSP	AMF	102	1	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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