

BQ25895 I²C 制御のシングル・セル 5A 高速充電器、MaxCharge™ による高入力電圧と可変電圧の 3.1A 昇圧動作

1 特長

- 高効率の 5A、1.5MHz スイッチ・モード降圧充電
 - 充電電流 2A で 93%、3A で 91% の充電効率
 - 高入力電圧 (9V~12V) に対して最適化
 - 軽負荷動作のための低消費電力 PFM モード
- 4.5V~5.5V の可変出力電圧による昇圧モード動作
 - 出力電流最大 3.1A で、500KHz~1.5MHz を選択可能な昇圧コンバータ
 - 5V 時に 1A 出力で 93% の昇圧効率
- 充電モードと昇圧モードを切り換えるための制御回路を内蔵
- 単一入力力で、USB 入力と調整可能な複数の高電圧アダプタをサポート
 - 3.9V~14V の入力電圧範囲に対応
 - USB 2.0、USB 3.0 規格、高電圧アダプタをサポートする入力電流制限 (100mA~3.25A、50mA 分解能)
 - 最高 14V の入力電圧制限による最大電力トラッキングで広範なアダプタに対応
 - USB SDP、CDP、DCP、非標準アダプタの自動検出
- 入力電流オプティマイザ (ICO) により、アダプタの過負荷を引き起こさずに入力電力を最大化
- 充電器の出力からセル端子までの抵抗補償 (IRCOMP)
- 最大 9A まで 11mΩ のバッテリー放電 MOSFET により最高のバッテリー放電効率を実現
- システム・モニタ用の ADC を内蔵 (電圧、温度、充電電流)
- ナロー VDC (NVDC) パワー・パス管理
 - バッテリー未接続または深放電状態でも即時オン
 - バッテリー補助モードで理想ダイオード動作
- BATFET 制御により出荷モード、ウェイクアップ、完全システム・リセットをサポート
- 柔軟性の高い、自律モードおよび I²C モードにより最適なシステム性能を実現
- すべての MOSFET、電流センシング、ループ補償を含む高度な統合
- 12μA の小さいバッテリー・リーク電流で出荷モードをサポート
- 高精度
 - ±0.5% の充電電圧レギュレーション
 - ±5% の充電電流レギュレーション
 - ±7.5% の入力電流レギュレーション
- 安全
 - 充電および昇圧モードでのバッテリー温度検出

— サーマル・レギュレーションおよびサーマル・シャットダウン

2 アプリケーション

- パワー・バンク、モバイル Wi-Fi ホットスポット
- ワイヤレス Bluetooth スピーカー
- 携帯用インターネット・デバイス

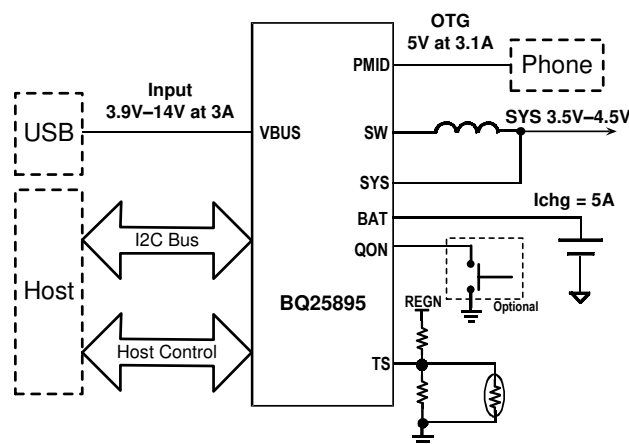
3 概要

BQ25895 は、シングル・セルのリチウムイオンおよびリチウムポリマー・バッテリー用の、高度に統合された 5A スイッチモード・バッテリー充電管理およびシステム・パワー・パス管理デバイスです。これらのデバイスは、高い入力電圧での高速な充電に対応しています。パワー・パスのインピーダンスが低いため、スイッチ・モードの動作効率が最適化され、バッテリー充電時間の短縮と、放電フェーズにおけるバッテリー駆動時間の延長を実現できます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
BQ25895	WQFN (24)	4.00mm x 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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4 Revision History

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• データシート全体にわたって WEBENCH を削除.....	1
• データシート全体にわたって包括的な用語を更新.....	1
• Changed PMID description	4
• Changed REG01 default setting from 06 to 05.....	33
Changes from Revision A (May 216) to Revision B (May 2018)	Page
• Added "SW (peak for 10 ns duration)" To the Absolute Maximum Rating	6
• Updated the セクション 7.4 values.....	6
• Changed V _{SYS} TYP value From: V _{BAT} + 50 mV To: I _(SYS) + 150 mV.....	7
• Changed the title of 図 7-4 From: Charge Current Accuracy To: I ² C Setting	12
• Changed axis title of 図 7-8 From: BAT Voltage (V) To: Input Current Limit (mA).....	12
• Changed V _{VREF} to V _{REGN} in 図 8-7	22
• Changed V _{VREF} to V _{REGN} in 式 2	22
• Changed V _{REF} to V _{REGN} in 図 8-8	23
• Added sentence to the Battery Monitor section "In battery only mode, .."	24
• Changed bit 5 From: 0 To: 1 in 図 8-21	35
• Changed the Description values of 表 8-26 From: mV To: mA.....	47
• Changed the Type values of Bits 6 to Bit 0 in 表 8-28 From: R/W To: R.....	48
• Added V _{REF} system pullup voltage to 表 9-1	49
• Changed 図 9-3	51
Changes from Revision * (March 2015) to Revision A (May 2016)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1

5 概要 (続き)

充電およびシステムの設定に I²C シリアル・インターフェイスを使用できるため、真に柔軟なソリューションとなります。

このデバイスは、標準の USB ホスト・ポート、USB 充電ポート、USB 準拠の可変高電圧アダプタなど、幅広い入力ソースをサポートしています。可変高電圧アダプタを使用した高速充電をサポートするため、BQ25895 は D+/D- ピンおよび USB スイッチ制御用の DSEL ピンによる MaxCharge™ をサポートしています。また、このデバイスには入力電流パルス・プロトコルを使用する可変高電圧アダプタをサポートするためのインターフェイスが搭載されています。デフォルトの入力電流制限を設定するには、デバイスに内蔵の USB インターフェイスを使用します。このデバイスは、入力電流および電圧のレギュレーションにより、USB 2.0 および USB 3.0 の電力仕様に準拠しています。さらに、入力電流オプティマイザ (ICO) は、入力ソースの過負荷なしで最大電力点を検出できます。このデバイスは、PMID ピンに可変の 4.5V~5.5V で最大 3.1A を供給することで、バッテリー昇圧動作をサポートし、充電 / 昇圧のモード検出機能も備えています。

6 Pin Configuration and Functions

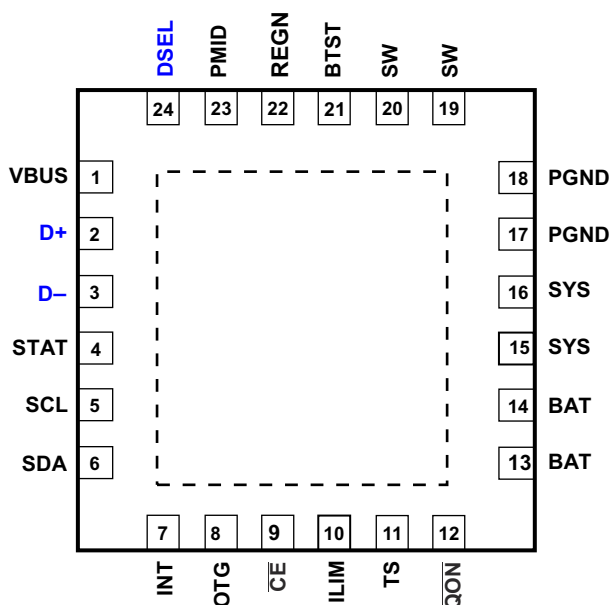


图 6-1. BQ25895 RTW (WQFN) Top View

表 6-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VBUS	1	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter (MaxCharge).
D-	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter (MaxCharge).
STAT	4	DO	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL	5	DI	I ² C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA		DIO	I ² C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	7	DO	Open-drain Interrupt Output. Connect the INT to a logic rail via 10-kΩ resistor. The INT pin sends active low, 256-μs pulse to host to report charger device status and fault.
OTG	8	DI	Boost mode enable pin. The boost mode is activated when OTG_CONFIG = 1, OTG pin is high, and no input source is detected at VBUS
CE	9	DI	Active low Charge Enable pin. Battery charging is enabled when CHG_CONFIG = 1 and CE pin = Low. CE pin must be pulled High or Low.
ILIM	10	AI	Input current limit Input. ILIM pin sets the maximum input current and can be used to monitor input current ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 0.8 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IILNLM register bits. Input current limit of less than 500 mA is not support on ILIM pin. ILIM pin can also be used to monitor input current when the voltage is below 0.8V. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN} = (K_{ILIM} \times V_{ILIM}) / (R_{ILIM} \times 0.8)$ The ILIM pin function can be disabled when EN_ILIM bit is 0.

表 6-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
TS	11	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
QON	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ duration turns on BATFET to exit shipping mode. When VBUS is not plugged-in, a logic low of t_{QON_RST} duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20uF closely to the SYS pin.
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047uF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047uF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7uF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	DO	Battery boost mode output. Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. If OTG is not used, the minimum capacitance required on PMID to PGND is 8.2 uF. If OTG is used, the minimum capacitance required on PMID to PGND is 40 uF for up-to 2.4A output and 60 uF for up-to 3.1A output.
DSEL	24	DO	Open-drain D+/D- multiplexer selection control. Connect the DSEL to a logic rail via 10-KΩ resistor. The pin is normally float and pull-up by external resistor. During セクション 8.2.3.3, the pin drives low to indicate the device D+/D- detection is in progress and needs to take control of D+, D- signals. When detection is completed, the pin keeps low when MaxCharge is detected. The pin returns to float and pulls high by external resistor when other input source type is detected.
PowerPAD™		P	Exposed pad beneath the IC for heat dissipation. Always solder PowerPAD Pad to the board, and have vias on the PowerPAD plane star-connecting to PGND and ground plane for high-current power converter.

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	VALUE
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	22	V
	PMID (converter not switching)	–0.3	22	V
	STAT	–0.3	20	V
	DSEL	–0.3	20	V
	BTST	–0.3	20	V
	SW	–2	16	V
	SW (peak for 10 ns duration)	–3	16	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, REGN, TS, \overline{CE} , \overline{QON}	–0.3	7	V
	D+, D–	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
	ILIM	–0.3	5	V
Output sink current	INT, STAT		6	mA
	DSEL		6	mA
Junction temperature		–40	150	°C
Storage temperature range, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

		VALUE	UNIT
V _{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	3.9		14 ⁽¹⁾	V
I _{IN}	Input current (VBUS)			3.25	A
I _{SYS}	Output current (SW)			5	A
V _{BAT}	Battery voltage			4.608	V
I _{BAT}	Fast charging current			5	A
	Discharging current with internal MOSFET			Up to 6 (continuous)	A
				9 (peak) (Up to 1 sec duration)	A
T _A	Operating free-air temperature range	–40		85	°C

- (1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		BQ25895	UNIT
		RTW (WQFN)	
		24-PINS	
R _{θJA}	Junction-to-ambient thermal resistance	31.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	27.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	8.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	8.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
QUIESCENT CURRENTS							
I _{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V _{BAT} = 4.2 V, V _(VBUS) < V _(UVLO) , leakage between BAT and VBUS			5	μA	
		High-Z mode, no VBUS, BATFET disabled (REG09[5]=1), battery monitor disabled, T _J < 85°C		12	23	μA	
		High-Z mode, no VBUS, BATFET enabled (REG09[5]=0), battery monitor disabled, T _J < 85°C		32	60	μA	
I _(VBUS_HIZ)	Input supply current (VBUS) in buck mode when High-Z mode is enabled	V _(VBUS) = 5 V, High-Z mode, no battery, battery monitor disabled		15	35	μA	
		V _(VBUS) = 12 V, High-Z mode, no battery, battery monitor disabled		25	50	μA	
I _(VBUS)	Input supply current (V _{BUS}) in buck mode	V _{BUS} > V _(UVLO) , V _{BUS} > V _{BAT} , converter not switching		1.5	3	mA	
		V _{BUS} > V _(UVLO) , V _{BUS} > V _{BAT} , converter switching, V _{BAT} = 3.2 V, I _{SY} S = 0A		3		mA	
		V _{BUS} > V _(UVLO) , V _{BUS} > V _{BAT} , converter switching, V _{BAT} = 3.8 V, I _{SY} S = 0 A		3		mA	
I _(BOOST)	Battery discharge current in boost mode	V _{BAT} = 4.2 V, boost mode, I _(VBUS) = 0 A, converter switching		5		mA	
VBUS/BAT POWER UP							
V _(VBUS_OP)	VBUS operating range			3.9	14	V	
V _(VBUS_UVLOZ)	VBUS for active I ² C, no battery			3.6		V	
V _(SLEEP)	Sleep mode falling threshold			25	65	120	mV
V _(SLEEPZ)	Sleep mode rising threshold			130	250	370	mV
V _(ACOV)	VBUS over-voltage rising threshold			14		14.6	V
	VBUS over-voltage falling threshold			13.5		14	V
V _{BAT(UVLOZ)}	Battery for active I2C, no VBUS			2.3			V
V _{BAT(DPL)}	Battery depletion falling threshold			2.15		2.5	V
V _{BAT(DPLZ)}	Battery depletion rising threshold			2.35		2.7	V
V _(VBUSMIN)	Bad adapter detection threshold			3.8			V
I _(BADSRC)	Bad adapter detection current source			30			mA
POWER-PATH MANAGEMENT							
V _{SY} S	Typical system regulation voltage	I _{(SY} S) = 0 A, V _{BAT} > V _{SY} S(MIN), BATFET Disabled (REG09[5]=1)		V _{BAT} + 50 mV			V
		I _{(SY} S) = 0 A, V _{BAT} < V _{SY} S(MIN), BATFET Disabled (REG09[5]=1)		V _{SY} S(MIN) + 150 mV			V
V _{SY} S(MIN)	Minimum DC system voltage output	V _{BAT} < V _{SY} S(MIN), SY_MIN = 3.5 V (REG03[3:1]=101), I _{SY} S= 0 A	3.50	3.65			V
V _{SY} S(MAX)	Maximum DC system voltage output	V _{BAT} = 4.35 V, SY_MIN = 3.5V (REG03[3:1]=101), I _{SY} S= 0 A		4.40	4.42		V

7.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{ON} (RBFET)	Top reverse blocking MOSFET (RBFET) on-resistance between VBUS and PMID	T _J = −40°C to +85°C		27	38	mΩ
		T _J = −40°C to +125°C		27	44	mΩ
R _{ON} (HSFET)	Top switching MOSFET (HSFET) on-resistance between PMID and SW	T _J = −40°C to +85°C		27	39	mΩ
		T _J = −40°C to +125°C		27	47	mΩ
R _{ON} (LSFET)	Bottom switching MOSFET (LSFET) on-resistance between SW and GND	T _J = −40°C to +85°C		16	24	mΩ
		T _J = −40°C to +125°C		16	28	mΩ
V _(FWD)	BATFET forward voltage in supplement mode	BAT discharge current 10 mA		30		mV
V _{BAT} (GD)	Battery good comparator rising threshold	V _{BAT} rising	3.4	3.55	3.7	V
V _{BAT} (GD_HYST)	Battery good comparator falling threshold	V _{BAT} falling		100		mV
BATTERY CHARGER						
V _{BAT} (REG_RANGE)	Typical charge voltage range		3.840		4.608	V
V _{BAT} (REG_STEP)	Typical charge voltage step			16		mV
V _{BAT} (REG)	Charge voltage resolution accuracy	V _{BAT} = 4.208 V (REG06[7:2]=010111) or V _{BAT} = 4.352 V (REG06[7:2]=100000) T _J = −40°C to +85°C	-0.5%		0.5%	
I _(CHG_REG_RANGE)	Typical fast charge current regulation range		0		5056	mA
I _(CHG_REG_STEP)	Typical fast charge current regulation step			64		mA
I _(CHG_REG_ACC)	Fast charge current regulation accuracy	V _{BAT} = 3.1 V or 3.8 V, I _{CHG} = 128 mA T _J = −40°C to +85°C	-20%		20%	
		V _{BAT} = 3.1 V or 3.8 V, I _{CHG} = 256 mA T _J = −40°C to +85°C	-10%		10%	
		V _{BAT} = 3.1 V or 3.8 V, I _{CHG} = 1792 mA T _J = −40°C to +85°C	-5%		5%	
V _{BAT} (LOWV)	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 1	2.6	2.8	2.9	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1])=1 (Typical 200-mV hysteresis)	2.8	3	3.1	V
I _(PRECHG_RANGE)	Precharge current range		64		1024	mA
I _(PRECHG_STEP)	Typical precharge current step			64		mA
I _(PRECHG_ACC)	Precharge current accuracy	V _{BAT} = 2.6 V, I _{PRECHG} = 256 mA	−10%		+10%	
I _(TERM_RANGE)	Termination current range		64		1024	mA
I _(TERM_STEP)	Typical termination current step			64		mA
I _(TERM_ACC)	Termination current accuracy	I _{TERM} = 256 mA, I _{CHG} ≤ 1344 mA T _J = −20°C to +85°C	−12%		12%	
		I _{TERM} = 256 mA, I _{CHG} > 1344 mA T _J = −20°C to +85°C	−20%		20%	
V _(SHORT)	Battery short voltage	VBAT falling		2		V
V _(SHORT_HYST)	Battery short voltage hysteresis	VBAT rising		200		mV
I _(SHORT)	Battery short current	VBAT < 2.2 V		100		mA
V _(RECHG)	Recharge threshold below V _{BATREG}	V _{BAT} falling, V _{RECHG} (REG06[0]=0) = 0		100		mV
		V _{BAT} falling, V _{RECHG} (REG06[0]=0) = 1		200		mV
I _{BAT} (LOAD)	Battery discharge load current	V _{BAT} = 4.2 V	15			mA
I _{SYS} (LOAD)	System discharge load current	V _{SYS} = 4.2 V	30			mA
R _{ON} (BATFET)	SYS-BAT MOSFET (BATFET) on-resistance	T _J = 25°C		11	13	mΩ
		T _J = −40°C to +125°C		11	19	mΩ
INPUT VOLTAGE / CURRENT REGULATION						
V _{IN} (DPM_RANGE)	Typical Input voltage regulation range		3.9		15.3	V
V _{IN} (DPM_STEP)	Typical Input voltage regulation step			100		mV
V _{IN} (DPM_ACC)	Input voltage regulation accuracy	V _{INDPM} = 4.4 V, 9 V	3%		3%	
I _{IN} (DPM_RANGE)	Typical Input current regulation range		100		3250	mA
I _{IN} (DPM_STEP)	Typical Input current regulation step			50		mA
I _{IN} (DPM100_ACC)	Input current 100-mA regulation accuracy V _{BAT} = 5 V, current pulled from SW	I _{INLIM} (REG00[5:0]) = 100 mA	85	90	100	mA

7.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IN(DPM_ACC)}$ Input current regulation accuracy $V_{BAT} = 5\text{ V}$, current pulled from SW	USB150, IINLIM (REG00[5:0]) = 150 mA	125	135	150	mA
	USB500, IINLIM (REG00[5:0]) = 500 mA	440	470	500	mA
	USB900, IINLIM (REG00[5:0]) = 900 mA	750	825	900	mA
	Adapter 1.5 A, IINLIM (REG00[5:0]) = 1500 mA	1300	1400	1500	mA
$I_{IN(START)}$ Input current regulation during system start up	$V_{SYS} = 2.2\text{ V}$, IINLIM (REG00[5:0]) > 200 mA			200	mA
K_{ILIM} $I_{INMAX} = K_{ILIM}/R_{ILIM}$	Input current regulation by ILIM pin = 1.5 A	320	355	390	A x Ω
D+/D- DETECTION					
$V_{(OP6_VSR)}$ D+/D- voltage source (0.6 V)		0.5	0.6	0.7	V
$V_{(3p45_VSR)}$ D+/D- voltage source (3.45 V)		3.3	3.45	3.6	V
$I_{(10UA_ISRC)}$ D+ connection check current source		7	10	14	μA
$I_{(100UA_ISINK)}$ D+/D- current sink (100 μA)		50	100	150	μA
$I_{(DPDM_LKG)}$ D+/D- Leakage current	D-, switch open	-1		1	μA
	D+, switch open	-1		1	μA
$I_{(1P6MA_ISINK)}$ D+/D- current sink (1.6 mA)		1.45	1.60	1.75	μA
$V_{(OP4_VTH)}$ D+/D- low comparator threshold		250		400	mV
$V_{(OP8_VTH)}$ D+ low comparator threshold				0.8	V
$V_{(2P7_VTH)}$ D+/D- comparator threshold for non-standard adapter detection (divider 1, 3, or 4)		2.55		2.85	V
$V_{(2P0_VTH)}$ D+/D- comparator threshold for non-standard adapter detection (divider 1, 3)		1.85		2.15	V
$V_{(1P2_VTH)}$ D+/D- comparator threshold for non-standard adapter detection (divider 2)		1.05		1.35	V
$R_{(D_DWN)}$ D- pulldown for connection check		14.25		24.8	k Ω
BAT OVERVOLTAGE/CURRENT PROTECTION					
$V_{BAT(OVP)}$ Battery over-voltage threshold	V_{BAT} rising, as percentage of $V_{BAT(REG)}$		104%		
$V_{BAT(OVP_HYST)}$ Battery over-voltage hysteresis	V_{BAT} falling, as percentage of $V_{BAT(REG)}$		2%		
$I_{BAT(FET_OCP)}$ System over-current threshold		9			A
THERMAL REGULATION AND THERMAL SHUTDOWN					
T_{REG} Junction temperature regulation accuracy	REG08[1:0] = 11		120		$^{\circ}\text{C}$
T_{SHUT} Thermal shutdown rising temperature	Temperature rising		160		$^{\circ}\text{C}$
$T_{SHUT(HYS)}$ Thermal shutdown hysteresis	Temperature falling		30		$^{\circ}\text{C}$
$V_{(LTF)}$ Cold temperature threshold, TS pin voltage rising threshold	As percentage to $V_{(REGN)}$	72.75%	73.25%	73.75%	
$V_{(LTF_HYS)}$ Cold temperature hysteresis, TS pin voltage falling	As percentage to $V_{(REGN)}$		0.4%		
$V_{(HTF)}$ Hot temperature TS pin voltage rising threshold	As percentage to $V_{(REGN)}$	47.75%	48.25%	48.75%	
$V_{(TCO)}$ Cut-off temperature TS pin voltage falling threshold	As percentage to $V_{(REGN)}$	44.25%	44.75%	45.25%	
COLD/HOT THERMISTOR COMPARATOR (BOOST MODE)					
$V_{(BCOLD1)}$ Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to $V_{(REGN)}$ REG01[5] = 1 (Approximately -20°C w/ 103AT)	79.5%	80%	80.5%	
$V_{(BCOLD1_HYS)}$ Cold temperature threshold 1, TS pin voltage falling threshold	As percentage to $V_{(REGN)}$ REG01[5] = 1		1%		
$V_{(BHOT2)}$ Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to $V_{(REGN)}$ REG01[7:6] = 10 (Approx. 65°C w/ 103AT)	30.75%	31.25%	31.75%	
$V_{(BHOT2_HYS)}$ Hot temperature threshold 2, TS pin voltage rising threshold	As percentage to $V_{(REGN)}$ REG01[7:6] = 10		3%		
PWM					
F_{SW} PWM switching frequency, and digital clock	Oscillator frequency	1.32		1.68	MHz
D_{MAX} Maximum PWM duty cycle			97%		
BOOST MODE OPERATION					
$V_{(OTG_REG_RANGE)}$ Typical boost mode regulation voltage range		4.55		5.55	V
$V_{(OTG_REG_STEP)}$ Typical boost mode regulation voltage step			64		mV
$V_{(OTG_REG_ACC)}$ Boost mode regulation voltage accuracy	$I_{(PMID)} = 0\text{ A}$, BOOSTV=5.126V (REG0A[7:4] = 1001)	-3%		3%	
$V_{(OTG_BAT)}$ Battery voltage exiting boost mode	BAT falling	2.6		2.9	V
$I_{(OTG)}$ Boost mode output current range		3.1			A
$V_{(OTG_OVP)}$ Boost mode over-voltage threshold	Rising threshold	5.8	6		V
REGN LDO					

7.5 Electrical Characteristics (continued)

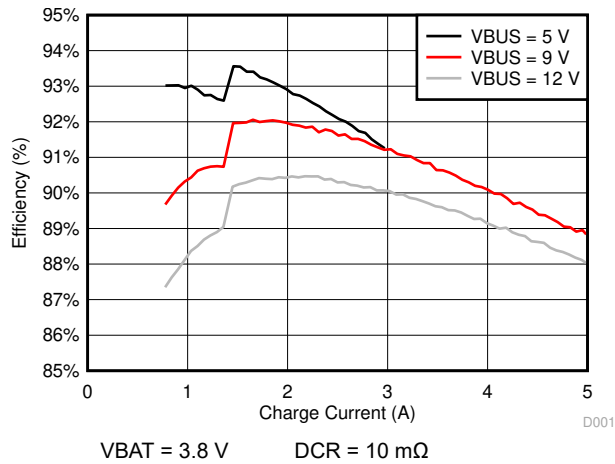
$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REGN)}$	REGN LDO output voltage	$V_{(VBUS)} = 9\text{ V}$, $I_{(REGN)} = 40\text{ mA}$	5.6	6	6.4	V
		$V_{(VBUS)} = 5\text{ V}$, $I_{(REGN)} = 20\text{ mA}$	4.7	4.8		V
$I_{(REGN)}$	REGN LDO current limit	$V_{(VBUS)} = 9\text{ V}$, $V_{(REGN)} = 3.8\text{ V}$	50			mA
ANALOG-TO-DIGITAL CONVERTER (ADC)						
RES	Resolution	Rising threshold		7		bits
$V_{BAT(RANGE)}$	Typical battery voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	V_{SYS_MIN}		4.848	V
V_{BAT_RES}	Typical battery voltage resolution			20		mV
$V_{(SYS_RANGE)}$	Typical system voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.304		4.848	V
		$V_{(VBUS)} < V_{BAT} + V_{(SLEEP)}$ and OTG mode is disabled	V_{SYS_MIN}		4.848	V
$V_{(SYS_RES)}$	Typical system voltage resolution			20		mV
$V_{(VBUS_RANGE)}$	Typical V_{VBUS} voltage range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ or OTG mode is enabled	2.6		15.3	V
$V_{(VBUS_RES)}$	Typical V_{VBUS} voltage resolution			100		mV
$I_{BAT(RANGE)}$	Typical battery charge current range	$V_{(VBUS)} > V_{BAT} + V_{(SLEEP)}$ and $V_{BAT} > V_{BAT(SHORT)}$	0		6.4	A
$I_{BAT(RES)}$	Typical battery charge current resolution			50		mA
$V_{(TS_RANGE)}$	Typical TS voltage range		21%		80%	
$V_{(TS_RES)}$	Typical TS voltage resolution			0.47%		
LOGIC I/O PIN (OTG, CE, PSEL, QON)						
V_{IH}	Input high threshold level		1.3			
V_{IL}	Input low threshold level				0.4	V
$I_{IN(BIAS)}$	High Level Leakage Current	Pull-up rail 1.8 V			1	μA
$V_{(QON)}$	Internal /QON pull-up	Battery only mode		BAT		V
		$V_{(VBUS)} = 9\text{ V}$		5.8		V
		$V_{(VBUS)} = 5\text{ V}$		4.3		V
$R_{(QON)}$	Internal /QON pull-up resistance			200		k Ω
LOGIC I/O PIN (INT, STAT, PG, DSEL)						
V_{OL}	Output low threshold level	Sink current = 5 mA, sink current			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	μA
I²C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8 V	1.3			
V_{IL}	Input low threshold level	Pull-up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA, sink current			0.4	V
I_{BIAS}	High level leakage current	Pull-up rail 1.8 V			1	μA

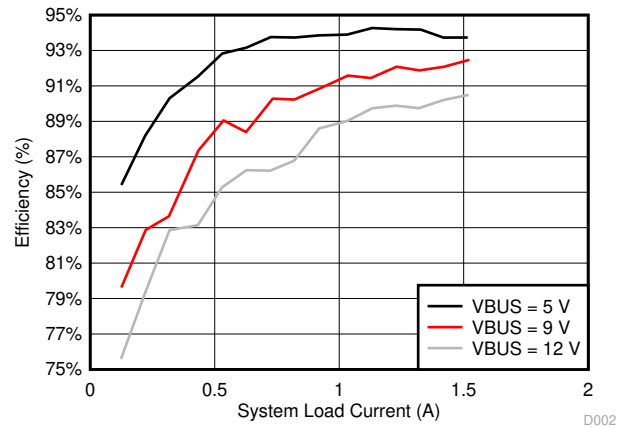
7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t _{BADSRC}	Bad Adapter detection duration			30		msec
D+/D- DETECTION						
t _{SDP_DEFAULT}	Charging timer with USB100 in default mode			2		mins
BAT OVER-VOLTAGE PROTECTION						
t _{BATOV}	Battery over-voltage deglitch time to disable charge			1		μs
BATTERY CHARGER						
t _{RECHG}	Recharge deglitch time			20		ms
CURRENT PULSE CONTROL						
t _{PUMPX_STOP}	Current pulse control stop pulse		430		570	ms
t _{PUMPX_ON1}	Current pulse control long on pulse		240		360	ms
t _{PUMPX_ON2}	Current pulse control short on pulse		70		130	ms
t _{PUMPX_OFF}	Current pulse control off pulse		70		130	ms
t _{PUMPX_DLY}	Current pulse control stop start delay		80		225	ms
BATTERY MONITOR						
t _{CONV}	Conversion time	CONV_RATE(REG02[6]) = 0		8	1000	ms
QON AND SHIPMODE TIMING						
t _{SHIPMODE}	QON low time to turn on BATFET and exit ship mode	T _J = -10°C to +60°C	1.25		2.25	s
t _{QON_RST}	QON low time to enable full system reset	T _J = -10°C to +60°C	12		18	s
t _{BATFET_RST}	BATFET off time during full system reset	T _J = -10°C to +60°C	350		550	ms
t _{SM_DLY}	Enter ship mode delay	T _J = -10°C to +60°C	10		15	s
I2C INTERFACE						
f _{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK and WATCHDOG TIMER						
f _{LPDIG}	Digital low power clock	REGN LDO disabled	18	30	45	kHz
f _{DIG}	Digital clock	REGN LDO enabled	1320	1500	1680	kHz
t _{WDT}	Watchdog reset time	WATCHDOG (REG07[5:4])=11, REGN LDO disabled	100	160		s
		WATCHDOG (REG07[5:4])=11, REGN LDO enabled	136	160		s

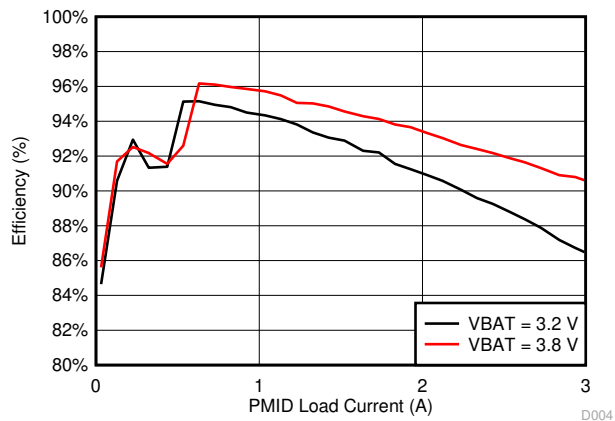
7.7 Typical Characteristics



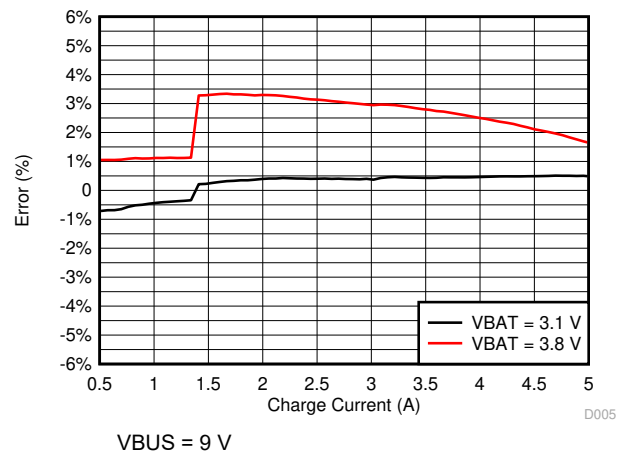
7-1. Charge Efficiency vs Charge Current



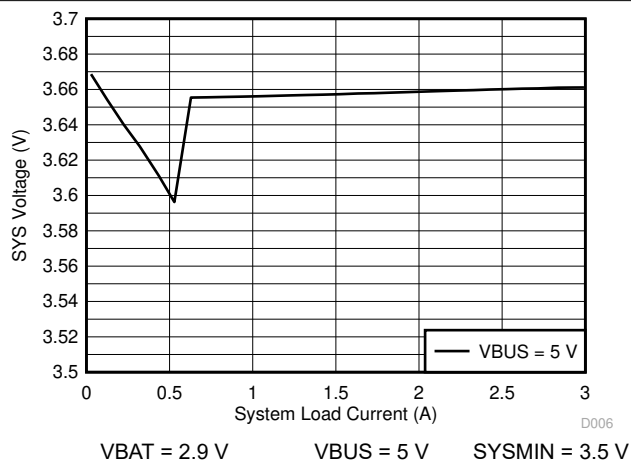
7-2. System Light Load Efficiency vs System Light Load Current



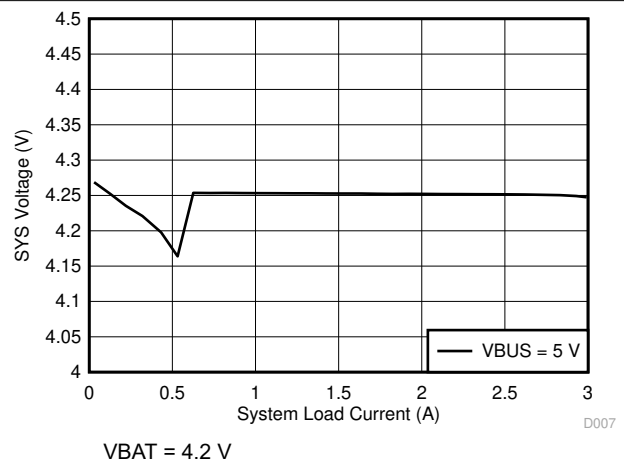
7-3. Boost Mode Efficiency vs PMID Load Current



7-4. Charge Current Accuracy vs Charge Current I²C Setting

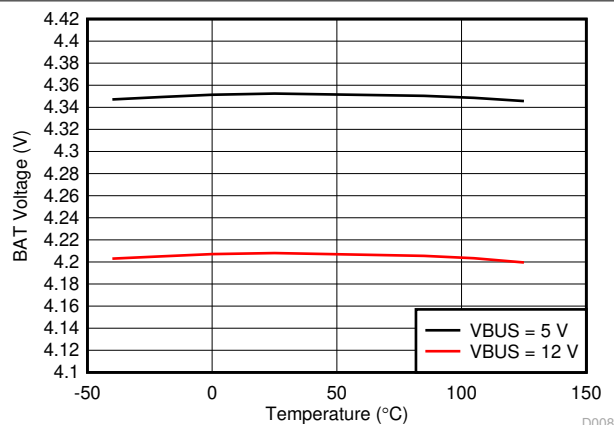


7-5. SYS Voltage Regulation vs System Load Current

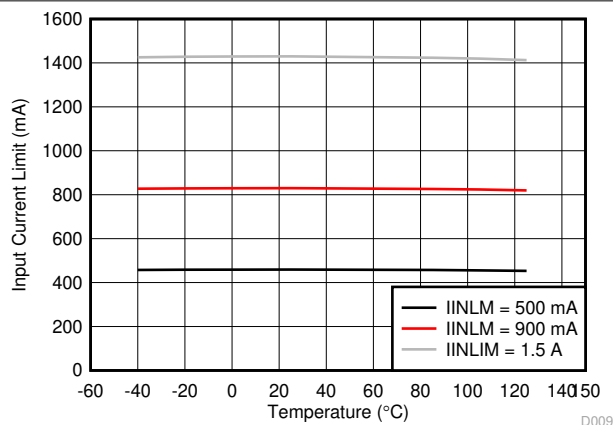


7-6. SYS Voltage Regulation vs System Load Current

7.7 Typical Characteristics (continued)



7-7. BAT Voltage vs Temperature

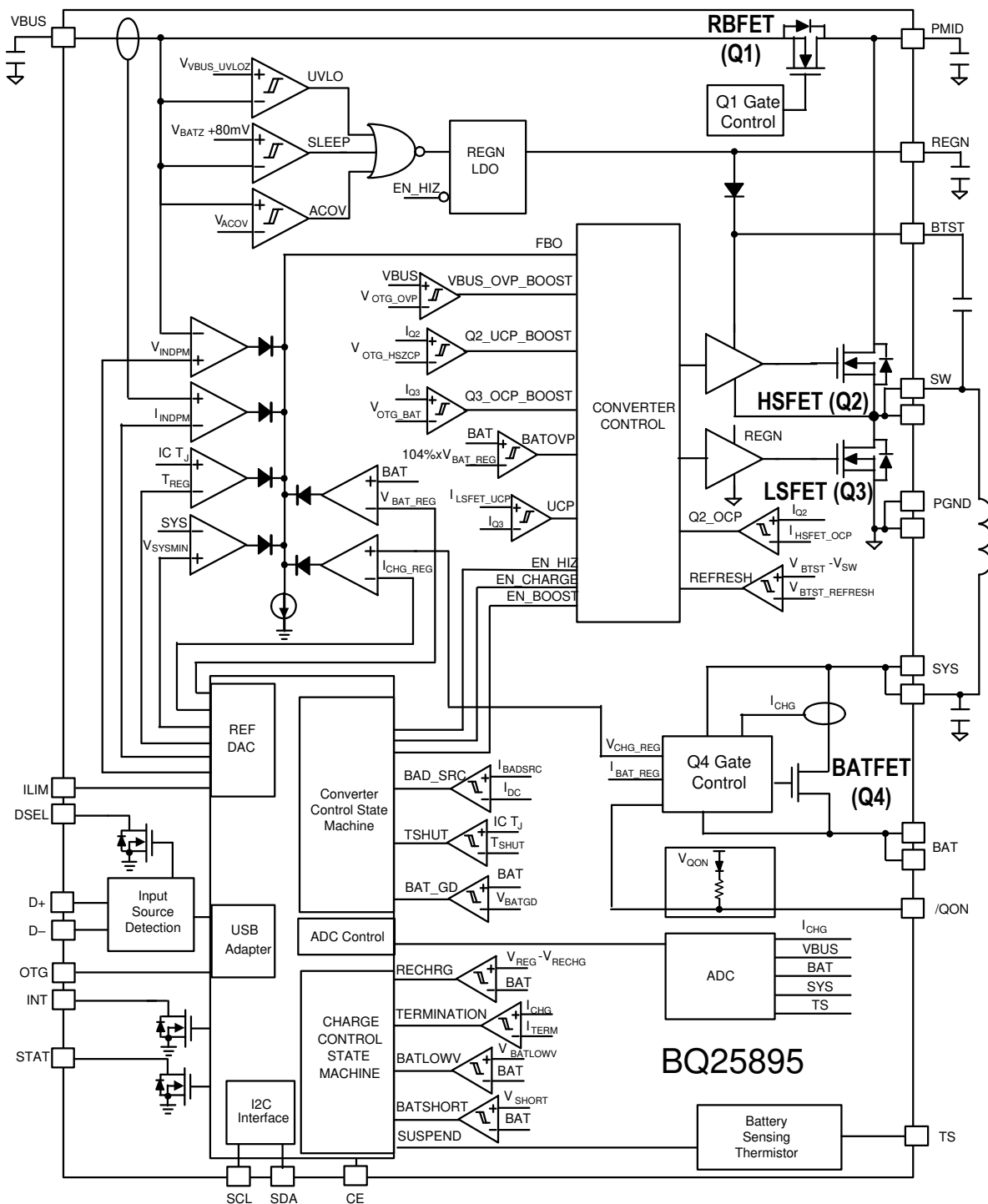


7-8. Input Current Limit vs Temperature

8 Detailed Description

The device is a highly integrated 5-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It is highly integrated with the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4). The device also integrates the bootstrap diode for the high-side gate drive.

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I²C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.2.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET ([セクション 8.2.6.3](#)). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET_OCP}$), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods describe in [セクション 8.2.10.2](#) is applied to re-enable BATFET.

8.2.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started when AUTO_DPDM_EN bit is set. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. [セクション 8.2.3.3](#) based on D+/D- to set default Input Current Limit (IINLIM) register and input source type
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

8.2.3.1 Power Up REGN Regulation (LDO)

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above V_{VBUS_UVLOZ}
2. VBUS above $V_{BAT} + V_{SLEEPZ}$ in buck mode or VBUS below $V_{BAT} + V_{SLEEP}$ in boost mode
3. After 220 ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.2.3.2 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the buck converter.

1. VBUS voltage below V_{ACOV}
2. VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

8.2.3.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the charger device runs [セクション 8.2.3.3](#) when AUTO_DPDM_EN bit is set.

The BQ25895 follows the USB Battery Charging Specification 1.2 (BC1.2) and to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. In addition, when USB DCP is detected, it initiates adjustable high voltage adapter handshake on D+/D-. The device supports MaxCharge™ handshake when MAXC_EN or HVDCP_EN is set.

After input source type detection, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINLIM) register is changed to set current limit
2. PG_STAT bit is set
3. SDP_STAT bit is updated to indicate USB100 or other input source

The host can over-write IINLIM register to change the input current limit if needed. The charger input current is always limited by the lower of IINLIM register or ILIM pin at all-time regardless of Input Current Optimizer (ICO) is enable or disabled.

When AUTO_DPDM_EN is disabled, the [セクション 8.2.3.3](#) is bypassed. The Input Current Limit (IINLIM) register, VBUS_STAT, and SPD_STAT bits are unchanged from previous values.

8.2.3.3.1 D+/D- Detection Sets Input Current Limit

The BQ25890 contains a D+/D- based input source detection to set the input current limit automatically. The D+/D- detection includes standard USB BC1.2, non-standard adapter, and adjustable high voltage adapter detections. When input source is plugged-in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

When DCP is detected, the device initiates adjustable high voltage adapter handshake including MaxCharge™, etc. The handshake connects combinations of voltage source(s) and/or current sink on D+/D- to signal input source to raise output voltage from 5 V to 9 V / 12 V. The adjustable high voltage adapter handshake can be disabled by clearing MAXC_EN and/or HVDCP_EN bits.

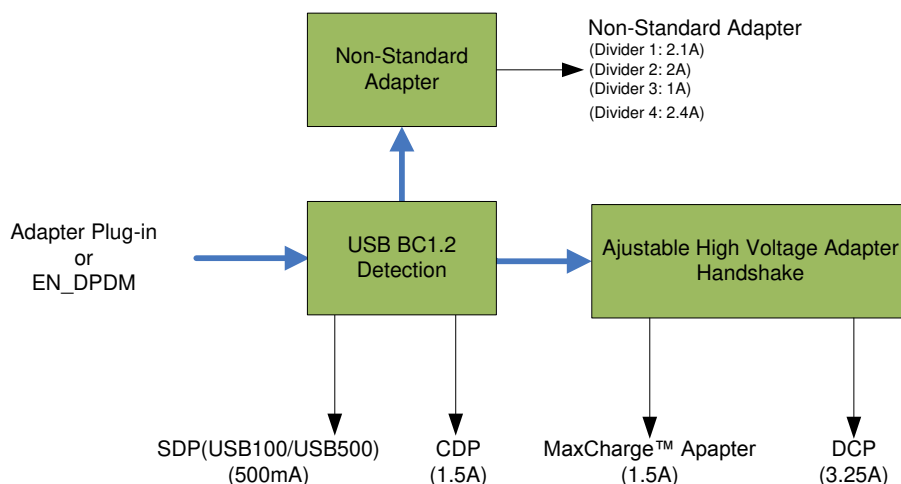


图 8-1. USB D+/D- Detection

表 8-1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1A
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1A
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4A

表 8-2. Adjustable High Voltage Adapter D+/D- Output Configurations

ADJUSTABLE HIGH VOLTAGE HANDSHAKE	D+	D-	OUTPUT
MaxCharge (12V)	I_{1P6MA_ISINK}	V_{3p45_VSRC}	12 V
MaxCharge (9V)	V_{3p45_VSRC}	I_{1P6MA_ISINK}	9 V

After the [セクション 8.2.3.3](#) is done, an INT pulse is asserted to the host. In addition, the following registers including Input Current Limit register (IINLIM), VBUS_STAT, and SDP_STAT are updated as below:

表 8-3. BQ25895 Result

D+/D- DETECTION	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	500 mA	1	001
USB CDP	1.5 A	1	010
USB DCP	3.25 A	1	011
Divider 3	1 A	1	110
Divider 1	2.1 A	1	110
Divider 4	2.4 A	1	110
Divider 2	2 A	1	110
MaxCharge	1.5 A	1	100
Unknown Adapter	500 mA	1	101

8.2.3.3.2 Force Input Current Limit Detection

In host mode, the host can force the device to run by setting FORCE_DPDM bit. After the detection is completed, FORCE_DPDM bit returns to 0 by itself and Input Result is updated.

8.2.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 14 V) for high voltage charging and provides two methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM=1)

By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.

2. Relative VINDPM based on VINDPM_OS registers (FORCE_VINDPM=0) (Default)

When FORCE_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm. The algorithm allows a wide range of adapter (V_{VBUS_OP}) to be used with flexible VINDPM threshold.

After Input Voltage Limit Threshold is set, an INT pulse is generated to signal to the host.

8.2.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is forced to the lower of 200 mA or IINLIM register setting. After the system rises above 2.2 V, the device limits input current to the lower value of ILIM pin and IILIM register (ICO_EN = 0) or IDPM_LIM register (ICO_EN = 1).

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.2.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overload the input source. The algorithm automatically identify maximum input current limit of power source without entering VINDPM to avoid input source overload.

This feature is enabled by default (ICO_EN=1) and can be disabled by setting ICO_EN bit to 0. After DCP or MaxCharge type input source is detected based on the procedures previously described ([セクション 8.2.3.3](#)). The algorithm runs automatically when ICO_EN bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected.

The actual input current limit used by the [セクション 8.2.6.2](#) is reported in IDPM_LIM register while Input Current Optimizer is enabled (ICO_EN = 1) or set by IINLIM register when the algorithm is disabled (ICO_EN = 0). In addition, the current limit is clamped by ILIM pin unless EN_ILIM bit is 0 to disable ILIM pin function.

8.2.5 Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through PMID pin. The boost mode output current rating supports maximum output current up to 3.1 A to charge smartphone and tablet at fast charging rate. The boost operation can be enabled if the conditions are valid:

1. BAT above BAT_{LOWV}
2. VBUS less than $BAT + V_{SLEEP}$ (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and OTG_CONFIG bit =1)
4. Voltage at TS (thermistor) pin is within range configured by Boost Mode Temperature Monitor as configured by BHOT and BCOLD bits
5. After 30 ms delay from boost mode enable

In boost mode, the device employs a 500 KHz or 1.5 MHz (selectable using BOOST_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is ignored when OTG_CONFIG is set.

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5V by default (selectable via BOOSTV register bits). The boost output is maintained when BAT is above V_{OTG_BAT} threshold

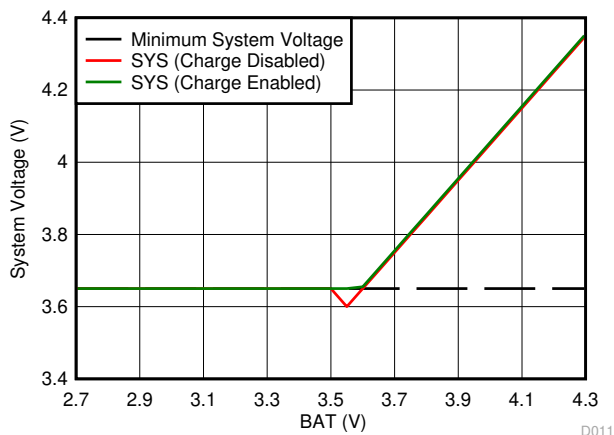
8.2.6 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.2.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.



8-2. V(SYS) vs V(BAT)

8.2.6.2 Dynamic Power Management

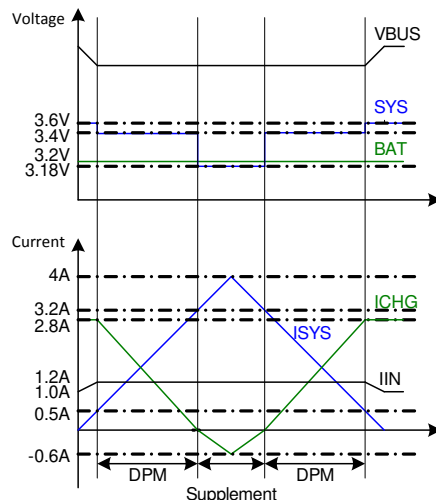
To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINLIM or IDPM_LIM) or the voltage falls below

the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the [セクション 8.2.6.3](#) where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) and/or IDPM_STAT (IINDPM) is/are set high.

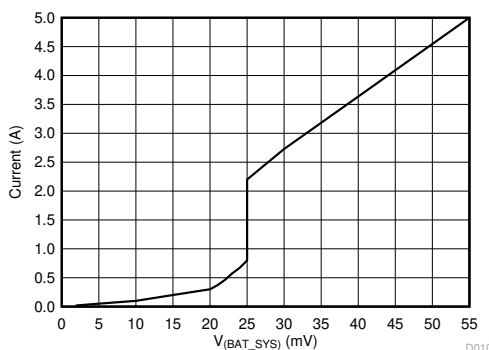
☒ 8-3 shows the DPM response with 9V/1.2A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.



☒ 8-3. DPM Response

8.2.6.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the [セクション 8.2.6.3](#). As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce $R_{DS(ON)}$ until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. ☒ 8-4 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit [セクション 8.2.6.3](#) when the battery is below battery depletion threshold.



☒ 8-4. BATFET V-I Curve

8.2.7 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 5-A charge current for high capacity battery. The 11-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.2.7.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and \overline{CE} pin is low), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in 表 8-4 always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I²C.

表 8-4. Charging Parameter Default Setting

DEFAULT MODE	BQ25895
Charging Voltage	4.208 V
Charging Current	2.048 A
Pre-charge Current	128 mA
Termination Current	256 mA
Temperature Profile	Cold/Hot
Safety Timer	12 hour

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by setting CHG_CONFIG bit, /CE pin is low and ICHG register is not 0 mA
- No thermistor fault on TS pin
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, either toggle \overline{CE} pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. In addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

8.2.7.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage.

表 8-5. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	I _{BATSHORT}	–	01
2 V – 3 V	I _{PRECHG}	128 mA	01
> 3 V	I _{CHG}	2048 mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

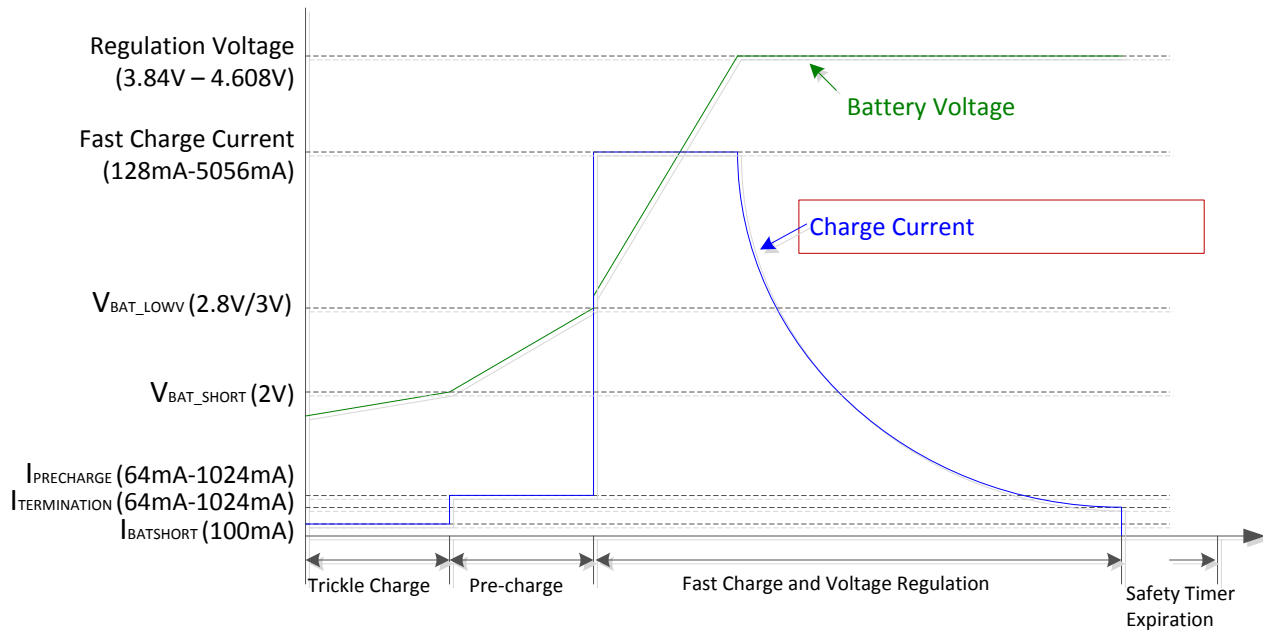


图 8-5. Battery Charging Profile

8.2.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage [セクション 8.2.6.3](#).

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

8.2.7.4 Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

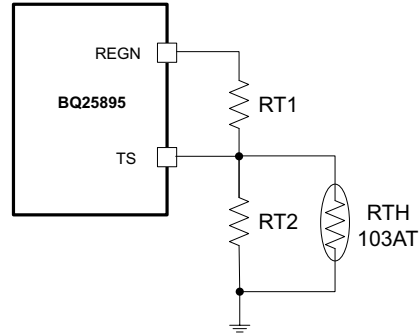
The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (V_{CLAMP}) and the minimum resistance compensation (BATCOMP).

$$V_{REG_ACTUAL} = V_{REG} + \min(I_{CHRG_ACTUAL} \times BATCOMP, V_{CLAMP}) \quad (1)$$

8.2.7.5 Thermistor Qualification

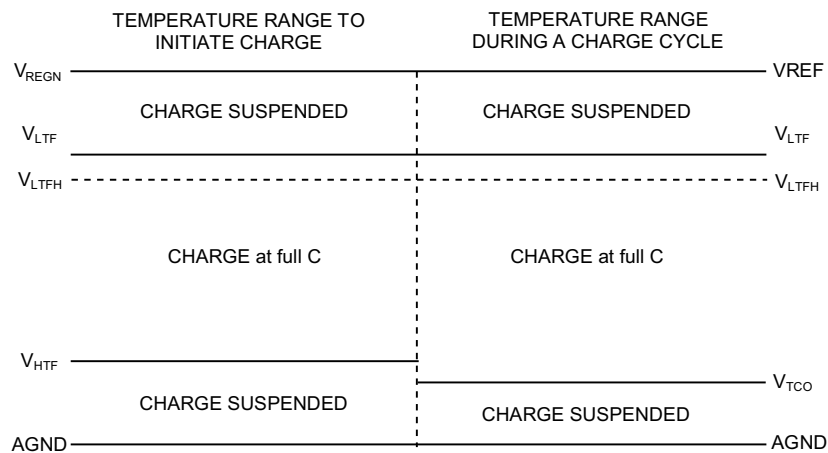
8.2.7.5.1 Cold/Hot Temperature Window in Charge Mode

The device continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.



8-6. TS Resistor Network

When the TS fault occurs, the fault register REG0C[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.



8-7. TS Pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in 8-6, the value RT1 and RT2 can be determined by using 2:

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

(2)

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

$RTH_{COLD} = 27.28 \text{ k}\Omega$

$RTH_{HOT} = 4.91 \text{ k}\Omega$

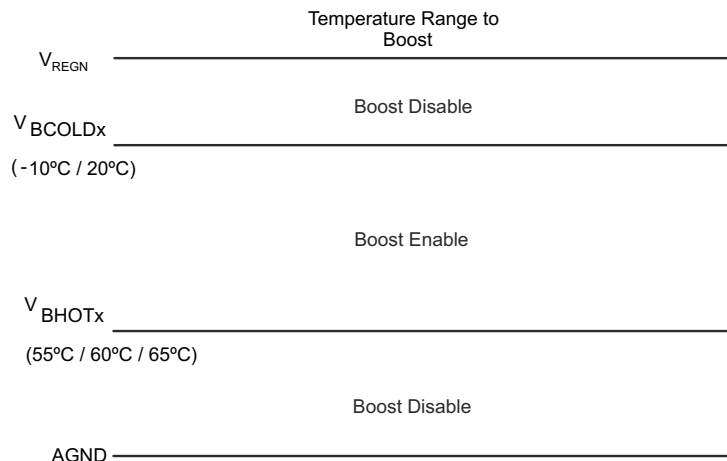
$RT1 = 5.21 \text{ k}\Omega$

$RT2 = 29.87 \text{ k}\Omega$

8.2.7.5.2 Cold/Hot Temperature Window in Boost Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLDx} to V_{BHOTx} thresholds unless boost mode temperature is disabled by setting BHOT bits to 11. When temperature

is outside of the temperature thresholds, the boost mode and BATFET are disabled and BATFET_DIS bit is set to reduce leakage current on PMID. Once temperature returns within thresholds, the host can clear BATFET_DIS bit or provide logic low to high transition on QON pin to enable BATFET and boost mode.



8-8. TS Pin Thermistor Sense Thresholds in Boost Mode

8.2.7.6 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below $V_{BATLOWV}$ threshold. The user can program fast charge safety timer through I²C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C by setting EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

8.2.8 Battery Monitor

The device includes a battery monitor to provide measurements of VBUS voltage, battery voltage, system voltage, thermistor ratio, and charging current, and charging current based on the device modes of operation. The measurements are reported in Battery Monitor Registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE = 0), the CONV_START bit can be set to start the conversion. During the conversion, the CONV_START is set and it is cleared by the device when conversion is completed. The conversion result is ready after t_{CONV} (maximum 1 second).

For continuous conversion (CONV_RATE = 1), the CONV_RATE bit can be set to initiate the conversion. During active conversion, the CONV_START is set to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_RATE is cleared.

When battery monitor is active, the REGN power is enabled and can increase device quiescent current. In battery only mode, the battery monitor is only active when $V_{(BAT)} > SYS_MIN$ setting in REG03.

表 8-6. Battery Monitor Modes of Operation

PARAMETER	REGISTER	MODES OF OPERATION			
		CHARGE MODE	BOOST MODE	DISABLE CHARGE MODE	BATTERY ONLY MODE
Battery Voltage (V_{BAT})	REG0E	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0F	Yes	Yes	Yes	Yes
Temperature (TS) Voltage (V_{TS})	REG10	Yes	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG11	Yes	Yes	Yes	NA
Charge Current (I_{BAT})	REG12	Yes	NA	NA	NA

8.2.9 Status Outputs (STAT, and INT)

8.2.9.1 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as shown in [Figure 9-1](#). The STAT pin function can be disabled by setting STAT_DIS bit.

表 8-7. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, TS fault, timer fault, input or system overvoltage). Boost Mode suspend (due to TS Fault)	blinking at 1 Hz

8.2.9.2 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256-μs INT pulse.

- USB/adaptor source identified (through PSEL or DPDM detection, with OTG pin)
- Good input source detected
 - VBUS above battery (not in sleep)
 - VBUS below V_{ACOV} threshold
 - VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG0C

When a fault occurs, the charger device sends out INT and keeps the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG0C two times consecutively. The 1st read reports the pre-existing fault register status and the 2nd read reports the current fault register status.

8.2.10 BATET (Q4) Control

8.2.10.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host sets BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

8.2.10.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit

3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)
4. A logic high to low transition on QON pin with t_{SHIPMODE} deglitch time to enable BATFET to exit shipping mode

8.2.10.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from off to on, system connects to SYS can be effectively have a power-on-reset. The QON pin supports push-button interface to reset system power without host by change the state of BATFET.

When the QON pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS=0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

8.2.11 Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adapter in order to signal adapter to increase or decrease output voltage. To enable the interface, the EN_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting one of the PUMPX_UP or PUMPX_DN bit (but not both) to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate pulse sequence is in progress and the device pulses the input current limit between current limit set forth by IINLIM or IDPM_LIM register and the 100mA current limit (I_{INDPM100_ACC}). When the pulse sequence is completed, the input current limit is returned to value set by IINLIM or IDPM_LIM register and the PUMPX_UP or PUMPX_DN bit is cleared. In addition, the EN_PUMPX can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as set forth by the IINLIM or IDPM_LIM register immediately. When EN_PUMPX bit is low, write to PUMPX_UP and PUMPX_DN bit would be ignored and have no effect on VBUS current limit.

8.2.12 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM setting and register setting (IINLIM). For example, if the register setting is 111111 for 3.25 A, and ILIM has a 260-Ω resistor (K_{ILIM} = 390 max.) to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (refer to [セクション 8.2.6.2](#) section).

The ILIM pin can also be used to monitor input current when EN_ILIM is enabled. The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following 式 4:

$$I_N = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8 \text{ V}} \quad (4)$$

For example, if ILIM pin is set with 260-Ω resistor, and the ILIM voltage is 0.4 V, the actual input current 0.615 A - 0.75 A (based on K_{ILIM} specified). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V. If ILIM pin is short, the input current limit is set by the register.

The ILIM pin function can be disabled by setting EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

8.2.13 Thermal Regulation and Thermal Shutdown

8.2.13.1 Thermal Protection in Buck Mode

The device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit

(TREG bits), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT} . The fault register CHRG_FAULT is set to 10 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is below T_{SHUT_HYS} .

8.2.13.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC surface temperature exceeds T_{SHUT} , BATFET is turned off to disable battery discharge. When IC surface temperature is below T_{SHUT_HYS} , the host can use one of the method describes in section [セクション 8.2.10.2](#) to recover.

8.2.14 Voltage and Current Monitoring in Buck and Boost Mode

8.2.14.1 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck and boost mode operations.

8.2.14.1.1 Input Overvoltage (ACOV)

The input voltage for buck mode operation is V_{VBUS_OP} . If VBUS voltage exceeds V_{ACOV} , the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT bits sets to 01. An INT is asserted to the host..

8.2.14.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

8.2.14.2 Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as LSFET current to ensure safe boost mode operation.

8.2.14.2.1 Boost Mode Overvoltage Protection

When PMID voltage rises above regulation target and exceeds V_{OTG_OVP} , the device enters overvoltage protection which stops switching and pauses boost mode (OTG_CONFIG bit remains set) until OVP fault is removed. During the overvoltage, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

8.2.15 Battery Protection

8.2.15.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

8.2.15.2 Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL} , the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. The battery is charged with $I_{BATSHORT}$ (typically 100 mA) current when $V_{BAT} < V_{SHORT}$ or precharge current as set in the IPRECHG register when the battery voltage is between V_{SHORT} and $V_{BATLOWV}$.

8.2.15.3 System Overcurrent Protection

When the system is shorted or significantly overloaded ($I_{BAT} > I_{BATOP}$) so that its current exceeds the overcurrent limit, the device latches off BATFET. Section [セクション 8.2.10.2](#) can reset the latch-off condition and turn on BATFET.

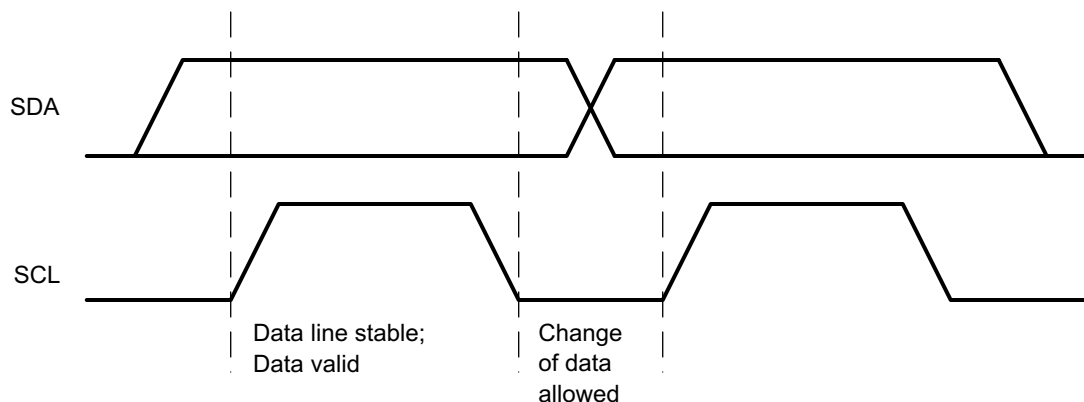
8.2.16 Serial Interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as hosts or targets when performing data transfers. A host is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with address 6AH, receiving control inputs from the host device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I²C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

8.2.16.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

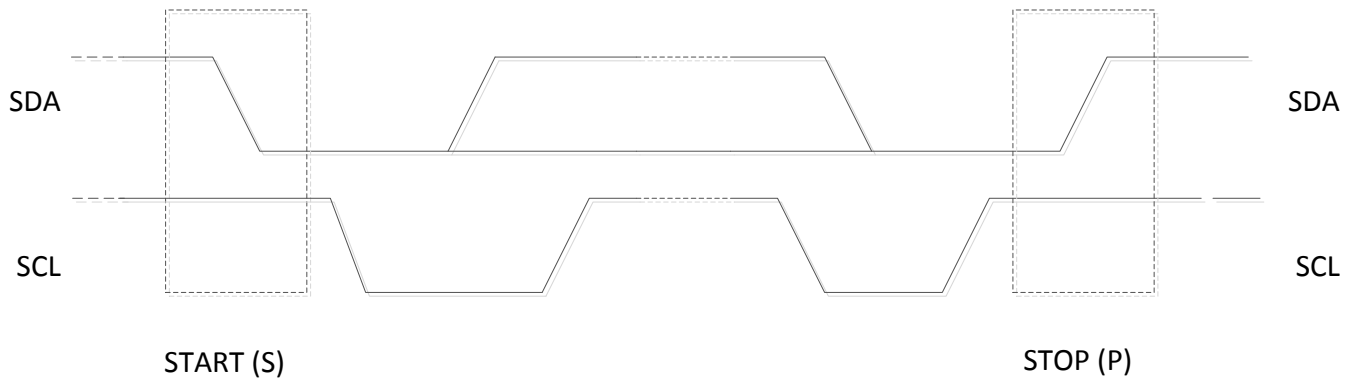


✎ 8-9. Bit Transfer on the I²C Bus

8.2.16.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

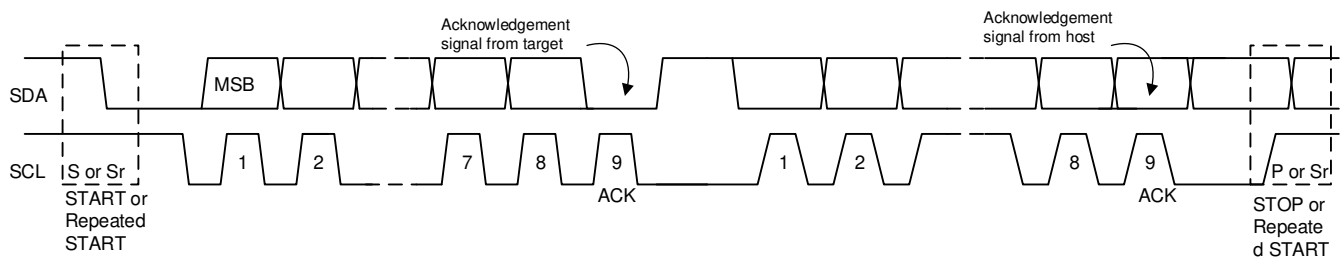
START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.



8-10. START and STOP conditions

8.2.16.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.



8-11. Data Transfer on the I²C Bus

8.2.16.4 Acknowledge (ACK) and Not Acknowledge (NACK)

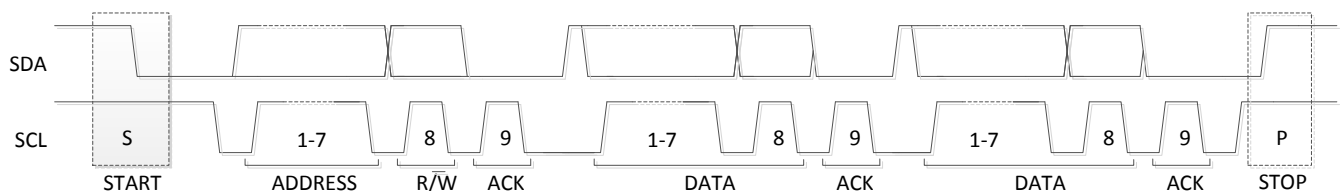
The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

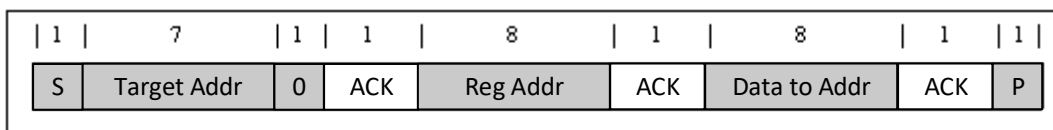
8.2.16.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

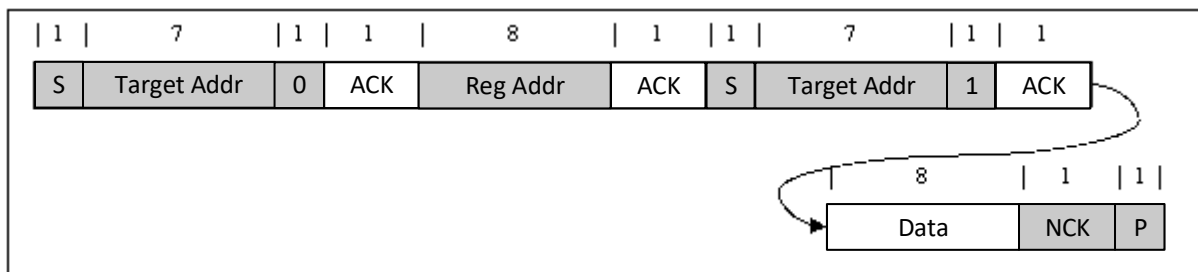


8-12. Complete Data Transfer

8.2.16.6 Single Read and Write



8-13. Single Write

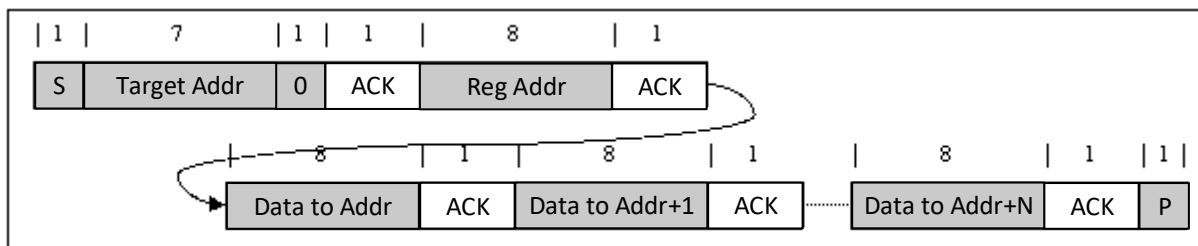


8-14. Single Read

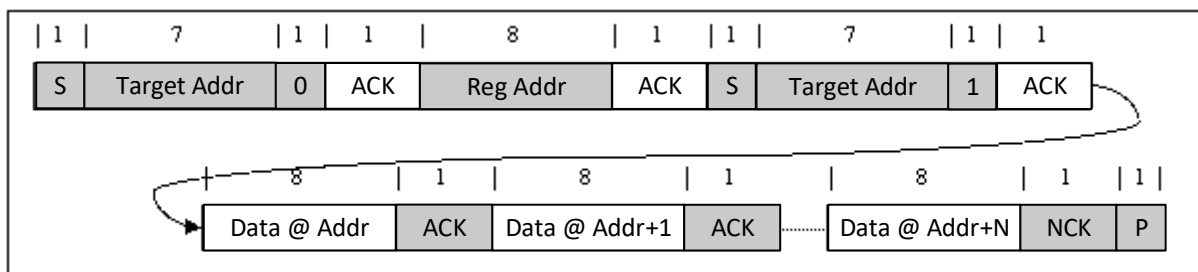
If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.2.16.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.



8-15. Multi-Write



8-16. Multi-Read

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

8.3 Device Functional Modes

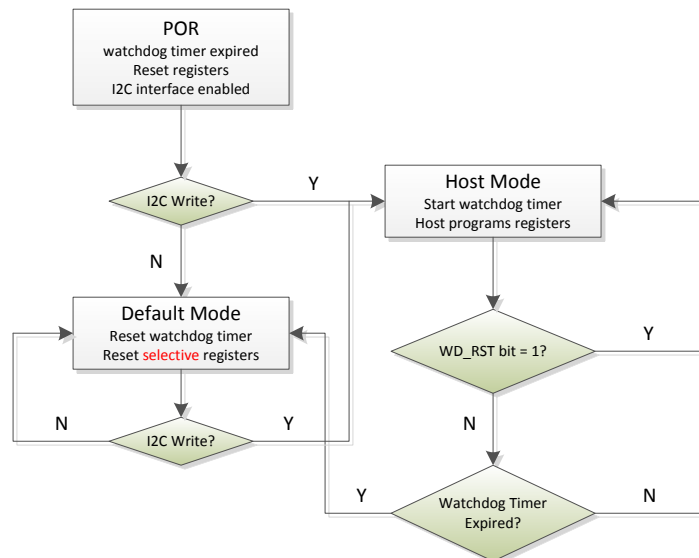
8.3.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of the 12-hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to device transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except IINLIM, VINDPM, VINDPM_OS, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.



8-17. Watchdog Timer Flow Chart

8.4 Register Maps

I2C Target Address: 6AH (1101010B + R/ \overline{W})

8.4.1 REG00

图 8-18. REG00

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-8. REG00

Bit	Field	Type	Reset	Description
7	EN_HIZ	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	EN_ILIM	R/W	by REG_RST by Watchdog	Enable ILIM Pin 0 – Disable 1 – Enable (default: Enable ILIM pin (1))
5	IINLIM[5]	R/W	by REG_RST	1600mA
4	IINLIM[4]	R/W	by REG_RST	800mA
3	IINLIM[3]	R/W	by REG_RST	400mA
2	IINLIM[2]	R/W	by REG_RST	200mA
1	IINLIM[1]	R/W	by REG_RST	100mA
0	IINLIM[0]	R/W	by REG_RST	50mA

Input Current Limit
Offset: 100mA
Range: 100mA (000000) – 3.25A (111111)
Default: 0001000 (500mA)
(Actual input current limit is the lower of I2C or ILIM pin)
IINLIM bits are changed automatically after input source
type detection is completed
USB Host SDP w/ OTG=Hi (USB500) = 500mA
USB Host SDP w/ OTG=Lo (USB100) = 500mA
USB CDP = 1.5A
USB DCP = 3.25A
Adjustable High Voltage (MaxCharge) DCP = 1.5A
Unknown Adapter = 500mA
Non-Standard Adapter = 1A/2A/2.1A/2.4A

8.4.2 REG01

图 8-19. REG01

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-9. REG01

Bit	Field	Type	Reset	Description
7	BHOT[1]	R/W	by REG_RST by Watchdog	Boost Mode Hot Temperature Monitor Threshold 00 – V_{BHOT1} Threshold (34.75%) (default) 01 – V_{BHOT0} Threshold (Typ. 37.75%) 10 – V_{BHOT2} Threshold (Typ. 31.25%) 11 – Disable boost mode thermal protection
6	BHOT[0]	R/W	by REG_RST by Watchdog	
5	BCOLD	R/W	by REG_RST by Watchdog	Boost Mode Cold Temperature Monitor Threshold 0 – V_{BCOLD0} Threshold (Typ. 77%) (default) 1 – V_{BCOLD1} Threshold (Typ. 80%)
4	VINDPM_OS[4]	R/W	by REG_RST	1600mV
3	VINDPM_OS[3]	R/W	by REG_RST	800mV
2	VINDPM_OS[2]	R/W	by REG_RST	400mV
1	VINDPM_OS[1]	R/W	by REG_RST	200mV
0	VINDPM_OS[0]	R/W	by REG_RST	100mV

8.4.3 REG02

图 8-20. REG02

7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-10. REG02

Bit	Field	Type	Reset	Description
7	CONV_START	R/W	by REG_RST by Watchdog	ADC Conversion Start Control 0 – ADC conversion not active (default). 1 – Start ADC Conversion This bit is read-only when CONV_RATE = 1. The bit stays high during ADC conversion and during input source detection.
6	CONV_RATE	R/W	by REG_RST by Watchdog	ADC Conversion Rate Selection 0 – One shot ADC conversion (default) 1 – Start 1s Continuous Conversion
5	BOOST_FREQ	R/W	by REG_RST by Watchdog	Boost Mode Frequency Selection 0 – 1.5MHz 1 – 500KHz (default) Note: Write to this bit is ignored when OTG_CONFIG is enabled.
4	ICO_EN	R/W	by REG_RST	Input Current Optimizer (ICO) Enable 0 – Disable ICO Algorithm 1 – Enable ICO Algorithm (default)
3	HVDCP_EN	R/W	by REG_RST	High Voltage DCP Enable 0 – Disable HVDCP handshake 1 – Enable HVDCP handshake (default)
2	MAXC_EN	R/W	by REG_RST	MaxCharge Adapter Enable 0 – Disable MaxCharge handshake 1 – Enable MaxCharge handshake (default)
1	FORCE_DPDM	R/W	by REG_RST by Watchdog	Force D+/D- Detection 0 – Not in D+/D- or PSEL detection (default) 1 – Force D+/D- detection
0	AUTO_DPDM_EN	R/W	by REG_RST	Automatic D+/D- Detection Enable 0 –Disable D+/D- or PSEL detection when VBUS is plugged-in 1 –Enable D+/D- or PEL detection when VBUS is plugged-in (default)

8.4.4 REG03

图 8-21. REG03

7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-11. REG03

Bit	Field	Type	Reset	Description
7	BAT_LOADEN	R/W	by REG_RST by Watchdog	Battery Load (I _{BATLOAD}) Enable 0 – Disabled (default) 1 – Enabled
6	WD_RST	R/W	by REG_RST by Watchdog	I2C Watchdog Timer Reset 0 – Normal (default) 1 – Reset (Back to 0 after timer reset)
5	OTG_CONFIG	R/W	by REG_RST by Watchdog	Boost (OTG) Mode Configuration 0 – OTG Disable 1 – OTG Enable (default)
4	CHG_CONFIG	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 - Charge Disable 1- Charge Enable (default)
3	SYS_MIN[2]	R/W	by REG_RST	0.4V Minimum System Voltage Limit Offset: 3.0V Range 3.0V-3.7V Default: 3.5V (101)
2	SYS_MIN[1]	R/W	by REG_RST	
1	SYS_MIN[0]	R/W	by REG_RST	
0	Reserved	R/W	by REG_RST by Watchdog	Reserved (default = 0)

8.4.5 REG04

图 8-22. REG04

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-12. REG04

Bit	Field	Type	Reset	Description
7	EN_PUMPX	R/W	by Software by Watchdog	Current pulse control Enable 0 - Disable Current pulse control (default) 1- Enable Current pulse control (PUMPX_UP and PUMPX_DN)
6	ICHG[6]	R/W	by Software by Watchdog	4096mA
5	ICHG[5]	R/W	by Software by Watchdog	2048mA
4	ICHG[4]	R/W	by Software by Watchdog	1024mA
3	ICHG[3]	R/W	by Software by Watchdog	512mA
2	ICHG[2]	R/W	by Software by Watchdog	256mA
1	ICHG[1]	R/W	by Software by Watchdog	128mA
0	ICHG[0]	R/W	by Software by Watchdog	64mA

8.4.6 REG05

图 8-23. REG05

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-13. REG05

Bit	Field	Type	Reset	Description
7	IPRECHG[3]	R/W	by Software by Watchdog	512mA
6	IPRECHG[2]	R/W	by Software by Watchdog	256mA
5	IPRECHG[1]	R/W	by Software by Watchdog	128mA
4	IPRECHG[0]	R/W	by Software by Watchdog	64mA
Precharge Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 128mA (0001)				
3	ITERM[3]	R/W	by Software by Watchdog	512mA
2	ITERM[2]	R/W	by Software by Watchdog	256mA
1	ITERM[1]	R/W	by Software by Watchdog	128mA
0	ITERM[0]	R/W	by Software by Watchdog	64mA
Termination Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 256mA (0011)				

8.4.7 REG06

图 8-24. REG06

7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-14. REG06

Bit	Field	Type	Reset	Description
7	VREG[5]	R/W	by Software by Watchdog	512mV
6	VREG[4]	R/W	by Software by Watchdog	256mV
5	VREG[3]	R/W	by Software by Watchdog	128mV
4	VREG[2]	R/W	by Software by Watchdog	64mV
3	VREG[1]	R/W	by Software by Watchdog	32mV
2	VREG[0]	R/W	by Software by Watchdog	16mV
1	BATLOWV	R/W	by Software by Watchdog	Battery Precharge to Fast Charge Threshold 0 – 2.8V 1 – 3.0V (default)
0	VRECHG	R/W	by Software by Watchdog	Battery Recharge Threshold Offset (below Charge Voltage Limit) 0 – 100mV (V_{RECHG}) below VREG (REG06[7:2]) (default) 1 – 200mV (V_{RECHG}) below VREG (REG06[7:2])

8.4.8 REG07

図 8-25. REG07

7	6	5	4	3	2	1	0
1	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-15. REG07

Bit	Field	Type	Reset	Description
7	EN_TERM	R/W	by Software by Watchdog	Charging Termination Enable 0 – Disable 1 – Enable (default)
6	STAT_DIS	R/W	by Software by Watchdog	STAT Pin Disable 0 – Enable STAT pin function (default) 1 – Disable STAT pin function
5	WATCHDOG[1]	R/W	by Software by Watchdog	I2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default)
4	WATCHDOG[0]	R/W	by Software by Watchdog	10 – 80s 11 – 160s
3	EN_TIMER	R/W	by Software by Watchdog	Charging Safety Timer Enable 0 – Disable 1 – Enable (default)
2	CHG_TIMER[1]	R/W	by Software by Watchdog	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs
1	CHG_TIMER[0]	R/W	by Software by Watchdog	10 – 12 hrs (default) 11 – 20 hrs
0	Reserved	R/W		Reserved (Default = 1)

8.4.9 REG08

图 8-26. REG08

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-16. REG08

Bit	Field	Type	Reset	Description
7	BAT_COMP[2]	R/W	by Software by Watchdog	80mΩ
6	BAT_COMP[1]	R/W	by Software by Watchdog	40mΩ
5	BAT_COMP[0]	R/W	by Software by Watchdog	20mΩ
4	VCLAMP[2]	R/W	by Software by Watchdog	128mV
3	VCLAMP[1]	R/W	by Software by Watchdog	64mV
2	VCLAMP[0]	R/W	by Software by Watchdog	32mV
1	TREG[1]	R/W	by Software by Watchdog	Thermal Regulation Threshold 00 – 60°C
0	TREG[0]	R/W	by Software by Watchdog	01 – 80°C 10 – 100°C 11 – 120°C (default)

8.4.10 REG09

图 8-27. REG09

7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-17. REG09

Bit	Field	Type	Reset	Description
7	FORCE_ICO	R/W	by Software by Watchdog	Force Start Input Current Optimizer (ICO) 0 – Do not force ICO (default) 1 – Force ICO Note: This bit is can only be set only and always returns to 0 after ICO starts
6	TMR2X_EN	R/W	by Software by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation (default)
5	BATFET_DIS	R/W	by Software	Force BATFET off to enable ship mode 0 – Allow BATFET turn on (default) 1 – Force BATFET off
4	Reserved	R/W		Reserved (Default = 0)
3	BATFET_DLY	R/W	by Software	BATFET turn off delay control 0 – BATFET turn off immediately when BATFET_DIS bit is set (default) 1 – BATFET turn off delay by t_{SM_DLY} when BATFET_DIS bit is set
2	BATFET_RST_EN	R/W	by Software	BATFET full system reset enable 0 – Disable BATFET full system reset 1 – Enable BATFET full system reset (default)
1	PUMPX_UP	R/W	by Software by Watchdog	Current pulse control voltage up enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed
0	PUMPX_DN	R/W	by Software by Watchdog	Current pulse control voltage down enable 0 – Disable (default) 1 – Enable Note: This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed

8.4.11 REG0A

図 8-28. REG0A

7	6	5	4	3	2	1	0
1	0	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-18. REG0A

Bit	Field	Type	Reset	Description
7	BOOSTV[3]	R/W	by Software by Watchdog	512mV
6	BOOSTV[2]	R/W	by Software by Watchdog	256mV
5	BOOSTV[1]	R/W	by Software	128mV
4	BOOSTV[0]	R/W	by Software by Watchdog	64mV
3	Reserved	R/W	by Software by Watchdog	Reserved (default = 0)
2	Reserved	R/W	by Software by Watchdog	Reserved (default = 0)
1	Reserved	R/W	by Software by Watchdog	Reserved (default = 1)
0	Reserved	R/W	by Software by Watchdog	Reserved (default = 1)

8.4.12 REG0B

図 8-29. REG0B

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-19. REG0B

Bit	Field	Type	Reset	Description
7	VBUS_STAT[2]	R	N/A	VBUS Status register BQ25895 000: No Input 001: USB Host SDP 010: USB CDP (1.5A) 011: USB DCP (3.25A) 100: Adjustable High Voltage DCP (MaxCharge) (1.5A) 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Note: Software current limit is reported in IINLIM register
6	VBUS_STAT[1]	R	N/A	
5	VBUS_STAT[0]	R	N/A	
4	CHRG_STAT[1]	R	N/A	Charging Status 00 – Not Charging 01 – Pre-charge ($< V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination Done
3	CHRG_STAT[0]	R	N/A	
2	PG_STAT	R	N/A	Power Good Status 0 – Not Power Good 1 – Power Good
1	SDP_STAT	R	N/A	USB Input Status 0 – USB100 input is detected 1 – USB500 input is detected Note: This bit always read 1 when VBUS_STAT is not 001
0	VSYS_STAT	R	N/A	VSYS Regulation Status 0 – Not in VSYSMIN regulation (BAT > VSYSMIN) 1 – In VSYSMIN regulation (BAT < VSYSMIN)

8.4.13 REG0C

图 8-30. REG0C

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-20. REG0C

Bit	Field	Type	Reset	Description
7	WATCHDOG_FAULT	R	N/A	Watchdog Fault Status Status 0 – Normal 1- Watchdog timer expiration
6	BOOST_FAULT	R	N/A	Boost Mode Fault Status 0 – Normal 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low in boost mode
5	CHRG_FAULT[1]	R	N/A	Charge Fault Status 00 – Normal
4	CHRG_FAULT[0]	R	N/A	01 – Input fault ($VBUS > V_{ACOV}$ or $VBAT < VBUS < V_{VBUSMIN}$ (typical 3.8V)) 10 - Thermal shutdown 11 – Charge Safety Timer Expiration
3	BAT_FAULT	R	N/A	Battery Fault Status 0 – Normal 1 – BATOV ($VBAT > V_{BATOV}$)
2	NTC_FAULT[2]	R	N/A	NTC Fault Status
1	NTC_FAULT[1]	R	N/A	Buck Mode: 000 – Normal 001 – TS Cold 010 – TS Hot
0	NTC_FAULT[0]	R	N/A	Boost Mode: 000 – Normal 101 – TS Cold 110 – TS Hot

8.4.14 REG0D

图 8-31. REG0D

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-21. REG0D

Bit	Field	Type	Reset	Description
7	FORCE_VINDPM	R/W	by Software	VINDPM Threshold Setting Method 0 – Run Relative VINDPM Threshold (default) 1 – Run Absolute VINDPM Threshold
6	VINDPM[6]	R/W	by Software	6400mV
5	VINDPM[5]	R/W	by Software	3200mV
4	VINDPM[4]	R/W	by Software	1600mV
3	VINDPM[3]	R/W	by Software	800mV
2	VINDPM[2]	R/W	by Software	400mV
1	VINDPM[1]	R/W	by Software	200mV
0	VINDPM[0]	R/W	by Software	100mV

8.4.15 REG0E

图 8-32. REG0E

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-22. REG0E

Bit	Field	Type	Reset	Description
7	THERM_STAT	R	N/A	Thermal Regulation Status 0 – Normal 1 – In Thermal Regulation
6	BATV[6]	R	N/A	1280mV
5	BATV[5]	R	N/A	640mV
4	BATV[4]	R	N/A	320mV
3	BATV[3]	R	N/A	160mV
2	BATV[2]	R	N/A	80mV
1	BATV[1]	R	N/A	40mV
0	BATV[0]	R	N/A	20mV

8.4.16 REG0F

图 8-33. REG0F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-23. REG0F

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved: Always reads 0
6	SYSV[6]	R	N/A	1280mV
5	SYSV[5]	R	N/A	640mV
4	SYSV[4]	R	N/A	320mV
3	SYSV[3]	R	N/A	160mV
2	SYSV[2]	R	N/A	80mV
1	SYSV[1]	R	N/A	40mV
0	SYSV[0]	R	N/A	20mV

ADDC conversion of System Voltage (V_{SYS})
Offset: 2.304V
Range: 2.304V (0000000) – 4.848V (1111111)
Default: 2.304V (0000000)

8.4.17 REG10

图 8-34. REG10

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-24. REG10

Bit	Field	Type	Reset	Description
7	Reserved	R	N/A	Reserved: Always reads 0
6	TSPCT[6]	R	N/A	29.76%
5	TSPCT[5]	R	N/A	14.88%
4	TSPCT[4]	R	N/A	7.44%
3	TSPCT[3]	R	N/A	3.72%
2	TSPCT[2]	R	N/A	1.86%
1	TSPCT[1]	R	N/A	0.93%
0	TSPCT[0]	R	N/A	0.465%

ADC conversion of TS Voltage (TS) as percentage of REGN
Offset: 21%
Range 21% (0000000) – 80% (1111111)
Default: 21% (0000000)

8.4.18 REG11

图 8-35. REG11

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-25. REG11

Bit	Field	Type	Reset	Description
7	VBUS_GD	R	N/A	VBUS Good Status 0 – Not VBUS attached 1 – VBUS Attached
6	VBUSV[6]	R	N/A	6400mV
5	VBUSV[5]	R	N/A	3200mV
4	VBUSV[4]	R	N/A	1600mV
3	VBUSV[3]	R	N/A	800mV
2	VBUSV[2]	R	N/A	400mV
1	VBUSV[1]	R	N/A	200mV
0	VBUSV[0]	R	N/A	100mV

ADC conversion of VBUS voltage (V_{BUS})
Offset: 2.6V
Range 2.6V (0000000) – 15.3V (1111111)
Default: 2.6V (0000000)

8.4.19 REG12

图 8-36. REG12

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-26. REG12

Bit	Field	Type	Reset	Description
7	Unused	R	N/A	Always reads 0
6	ICHGR[6]	R	N/A	3200mA
5	ICHGR[5]	R	N/A	1600mA
4	ICHGR[4]	R	N/A	800mA
3	ICHGR[3]	R	N/A	400mA
2	ICHGR[2]	R	N/A	200mA
1	ICHGR[1]	R	N/A	100mA
0	ICHGR[0]	R	N/A	50mA

ADC conversion of Charge Current (I_{BAT}) when $V_{BAT} > V_{BATSHORT}$
Offset: 0mA
Range 0mA (0000000) – 6350mA (1111111)
Default: 0mA (0000000)
Note:
This register returns 0000000 for $V_{BAT} < V_{BATSHORT}$

8.4.20 REG13

图 8-37. REG13

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-27. REG13

Bit	Field	Type	Reset	Description
7	VDPM_STAT	R	N/A	VINDPM Status 0 – Not in VINDPM 1 – VINDPM
6	IDPM_STAT	R	N/A	IINDPM Status 0 – Not in IINDPM 1 – IINDPM
5	IDPM_LIM[5]	R	N/A	Input Current Limit in effect while Input Current Optimizer (ICO) is enabled Offset: 100mA (default) Range 100mA (0000000) – 3.25mA (1111111)
4	IDPM_LIM[4]	R	N/A	
3	IDPM_LIM[3]	R	N/A	
2	IDPM_LIM[2]	R	N/A	
1	IDPM_LIM[1]	R	N/A	
0	IDPM_LIM[0]	R	N/A	

8.4.21 REG14

图 8-38. REG14

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-28. REG14

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	N/A	Register Reset 0 – Keep current register setting (default) 1 – Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed
6	ICO_OPTIMIZED	R	N/A	Input Current Optimizer (ICO) Status 0 – Optimization is in progress 1 – Maximum Input Current Detected
5	PN[2]	R	N/A	Device Configuration 111: BQ25895
4	PN[1]	R	N/A	
3	PN[0]	R	N/A	
2	TS_PROFILE	R	N/A	Temperature Profile 0 – Cold/Hot (default)
1	DEV_REV[1]	R	N/A	Device Revision: 01
0	DEV_REV[0]	R	N/A	

9 Application and Implementation

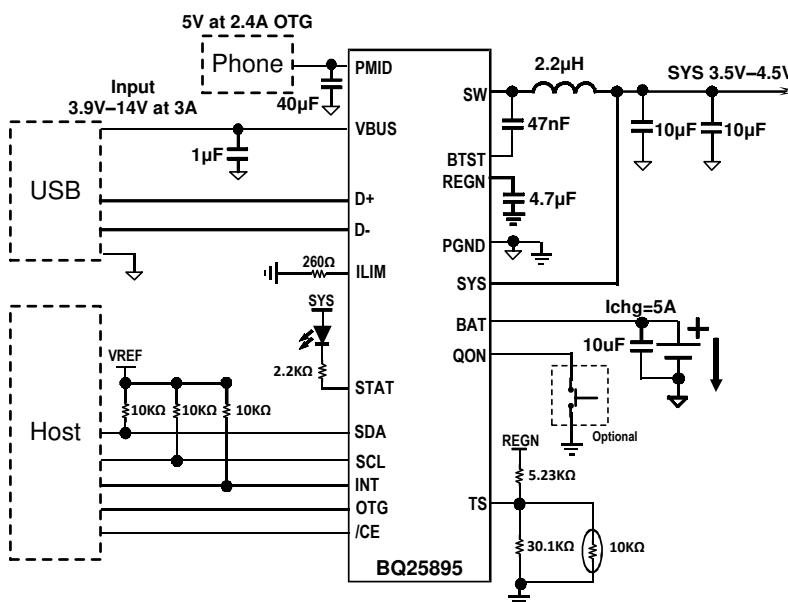
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application



9-1. BQ25895 with D+/D- Interface and 2.4-A Boost Mode Output

9.2.1 Design Requirements

For this design example, use the parameters shown in 表 9-1.

表 9-1. Design Parameter

PARAMETERS	VALUES
Input voltage range	3.9 V to 14 V
Input current limit	1.5 A
Fast charge current	5000 mA
Output voltage	4.352 V
V _{REF} system pullup voltage	1.8 V - 3.3 V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{BAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle ($D = V_{BAT}/V_{BUS}$), switching frequency (f_s) and inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{f_s \times L} \quad (6)$$

The maximum inductor ripple current happens with $D = 0.5$ or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Buck Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{PMID} occurs where the duty cycle is closest to 50% and can be estimated by [式 7](#):

$$I_{PMID} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for up to 14-V input voltage. 8.2- μ F capacitance is suggested for typical of 3 A – 5 A charging current.

9.2.2.3 System Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COU} is given:

$$I_{CSYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{SYS}}{8 LC_{SYS} f_s^2} \left(1 - \frac{V_{SYS}}{V_{BUS}} \right) \quad (9)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The charger device has internal loop compensator. To get good loop stability, 1- μ H and minimum of 20- μ F output capacitor is recommended. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

9.2.3 Application Curves

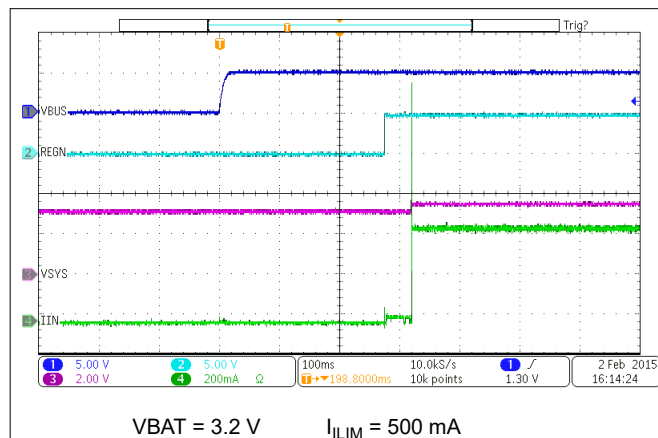


Figure 9-2. Power Up from USB100

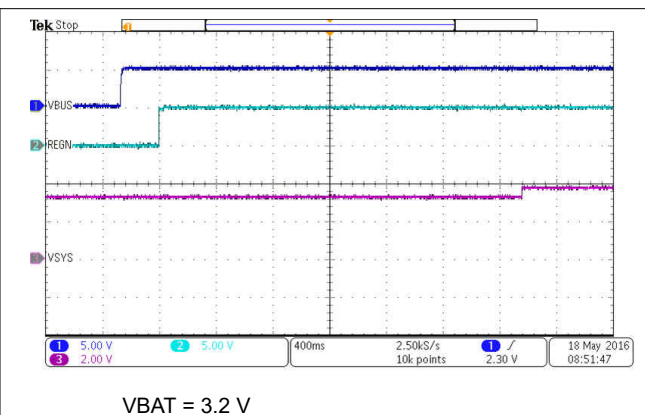


Figure 9-3. Power Up with Charge Disabled

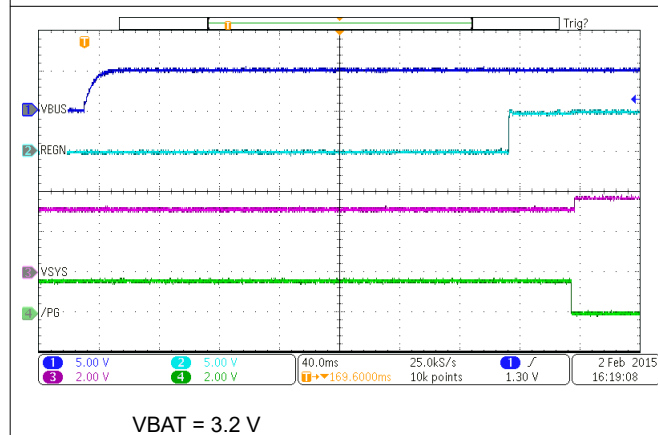


Figure 9-4. Power Up with Charge Disabled

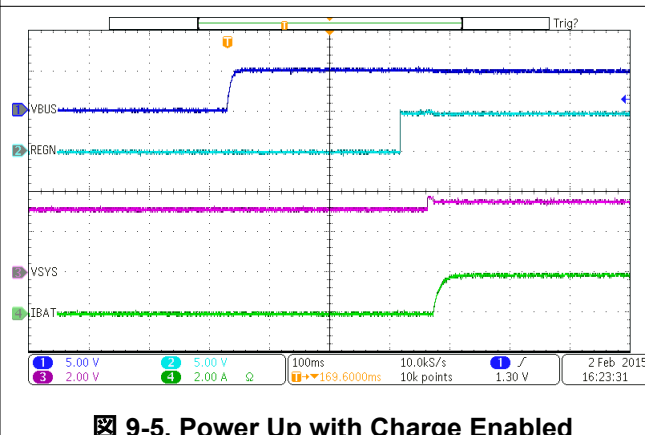


Figure 9-5. Power Up with Charge Enabled

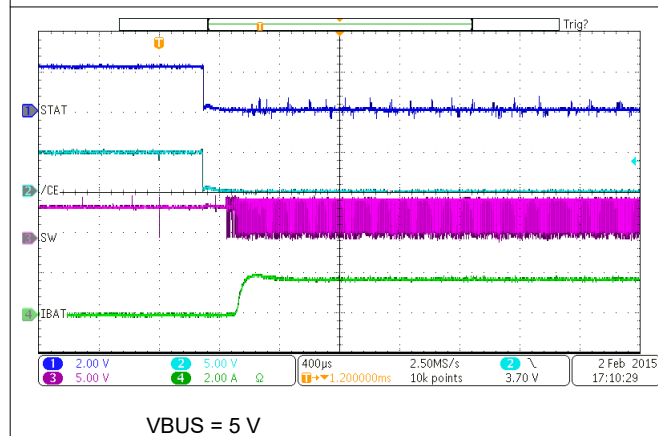


Figure 9-6. Charge Enable

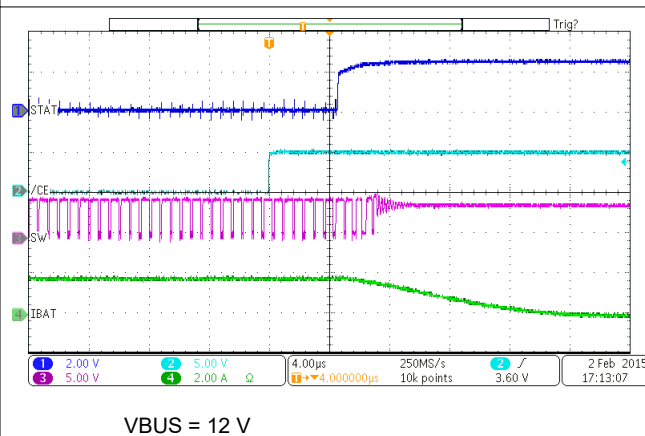
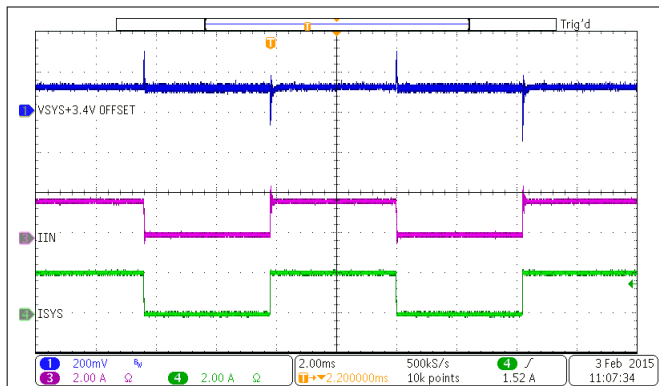


Figure 9-7. Charge Disable

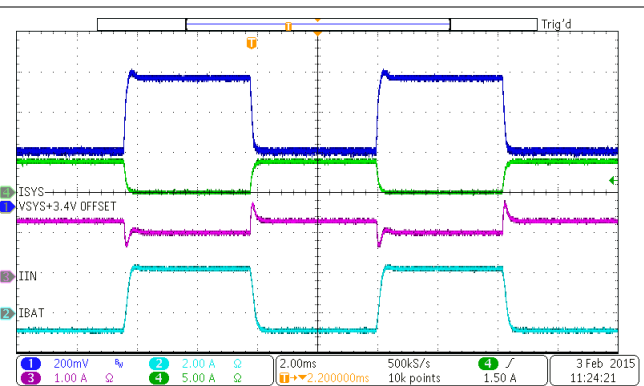


VBUS = 5 V

 $I_{IN} = 3 \text{ A}$

Charge Disable

FIG 9-8. Input Current DPM Response without Battery



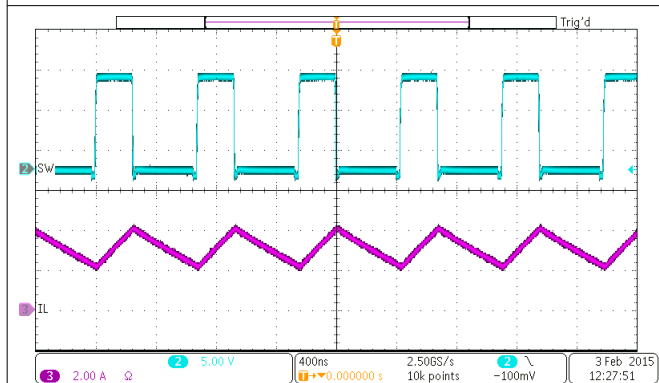
VBUS = 9 V

 $I_{IN} = 1.5 \text{ A}$

VBAT = 3.8 V

 $I_{CHG} = 2 \text{ A}$ $I_{SYS} = 0 \text{ A} - 4 \text{ A}$

FIG 9-9. Load Transient During Supplement Mode

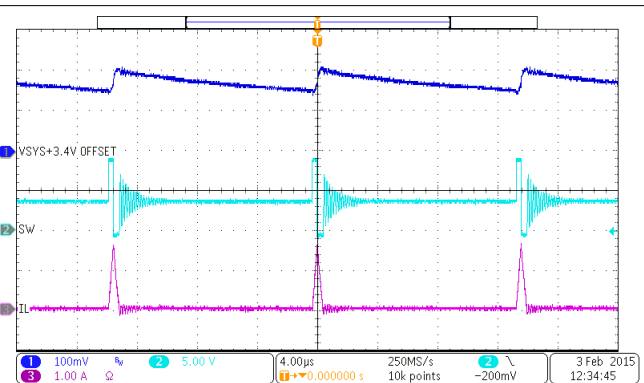


VBUS = 12 V

VBAT = 3.8 V

 $I_{CHG} = 3 \text{ A}$

FIG 9-10. PWM Switching Waveform

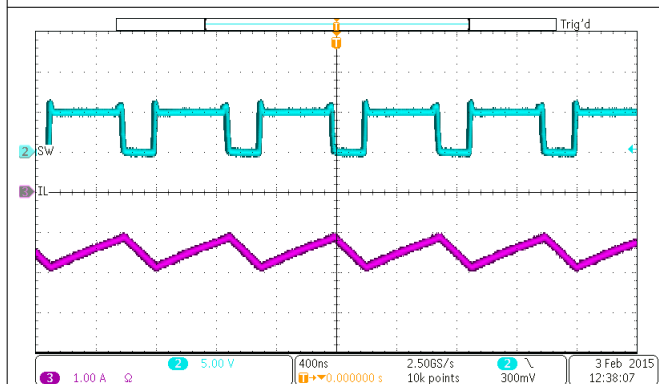


VBUS = 9V

 $I_{SYS} = 10 \text{ mA}$,

Charge Disable

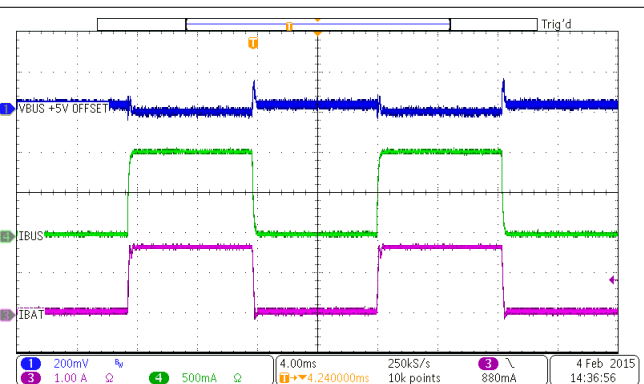
FIG 9-11. PFM Switching Waveform



VBAT = 3.8 V

 $I_{LOAD} = 1 \text{ A}$

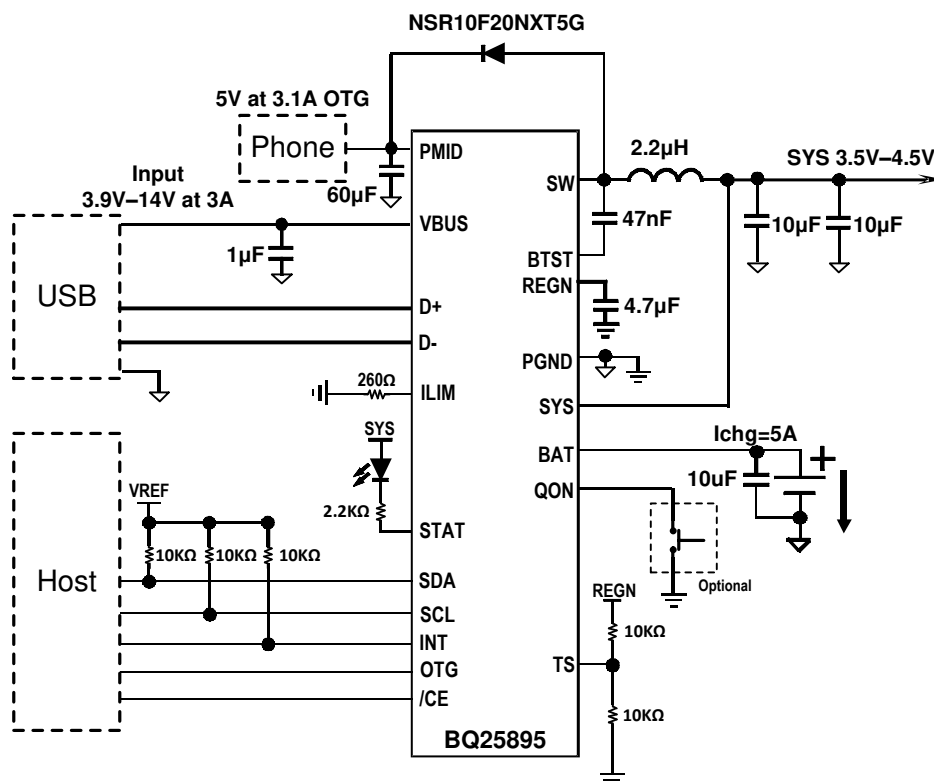
FIG 9-12. Boost Mode Switching Waveform



VBAT = 3.8 V

 $I_{LOAD} = 0 \text{ A} - 1 \text{ A}$

FIG 9-13. Boost Mode Load Transient



9-14. BQ25895 with D+/D- Interface, 3.1-A Boost Mode Output, and No Thermistor Connections

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 14 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage $> V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see [Figure 11-1](#)) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the VQFN information, refer to [Quad Flatpack No-Lead Logic Packages Application Report](#) and [QFN and SON PCB Attachment Application Report](#).

11.2 Layout Example

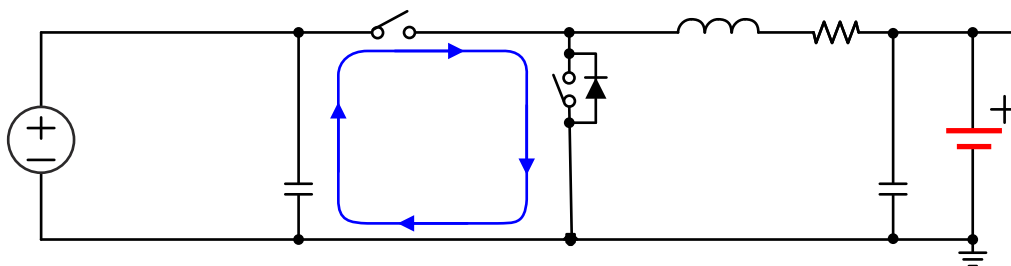


Figure 11-1. High Frequency Current Path

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25895RTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25895	Samples
BQ25895RTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ25895	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25895RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25895RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25895RTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25895RTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25895RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
BQ25895RTWR	WQFN	RTW	24	3000	346.0	346.0	33.0
BQ25895RTWT	WQFN	RTW	24	250	210.0	185.0	35.0
BQ25895RTWT	WQFN	RTW	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

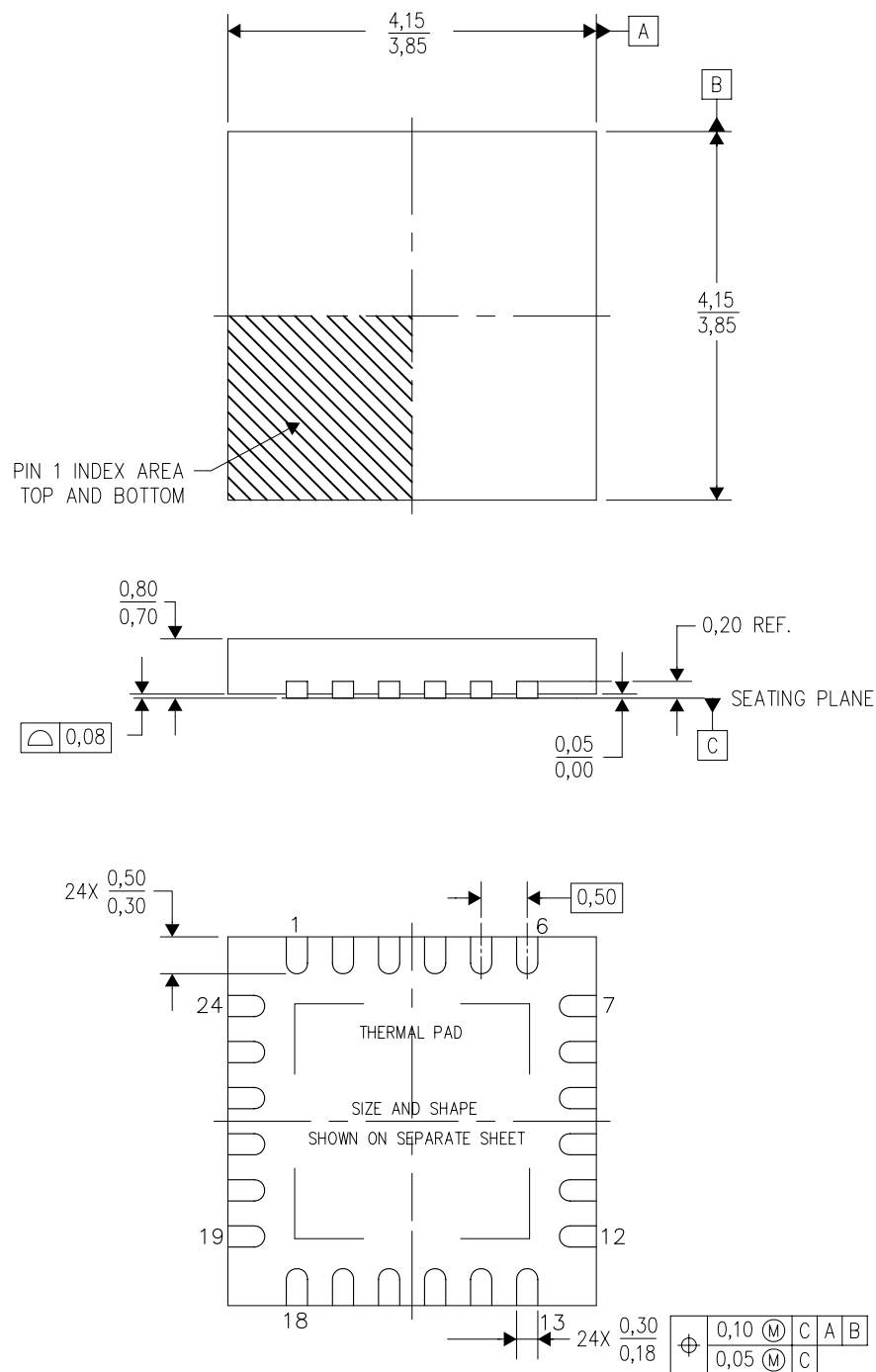
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224801/A

RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

RTW (S-PWQFN-N24)

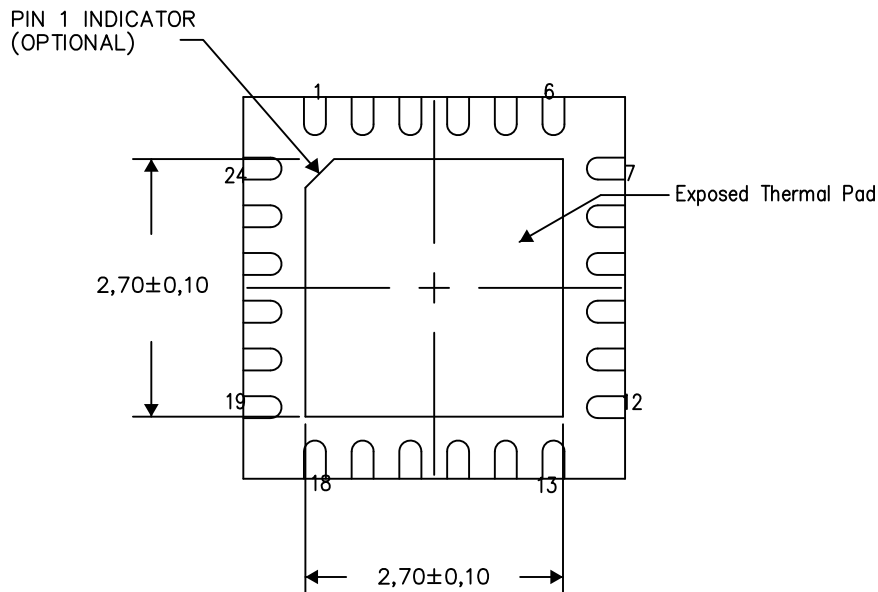
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

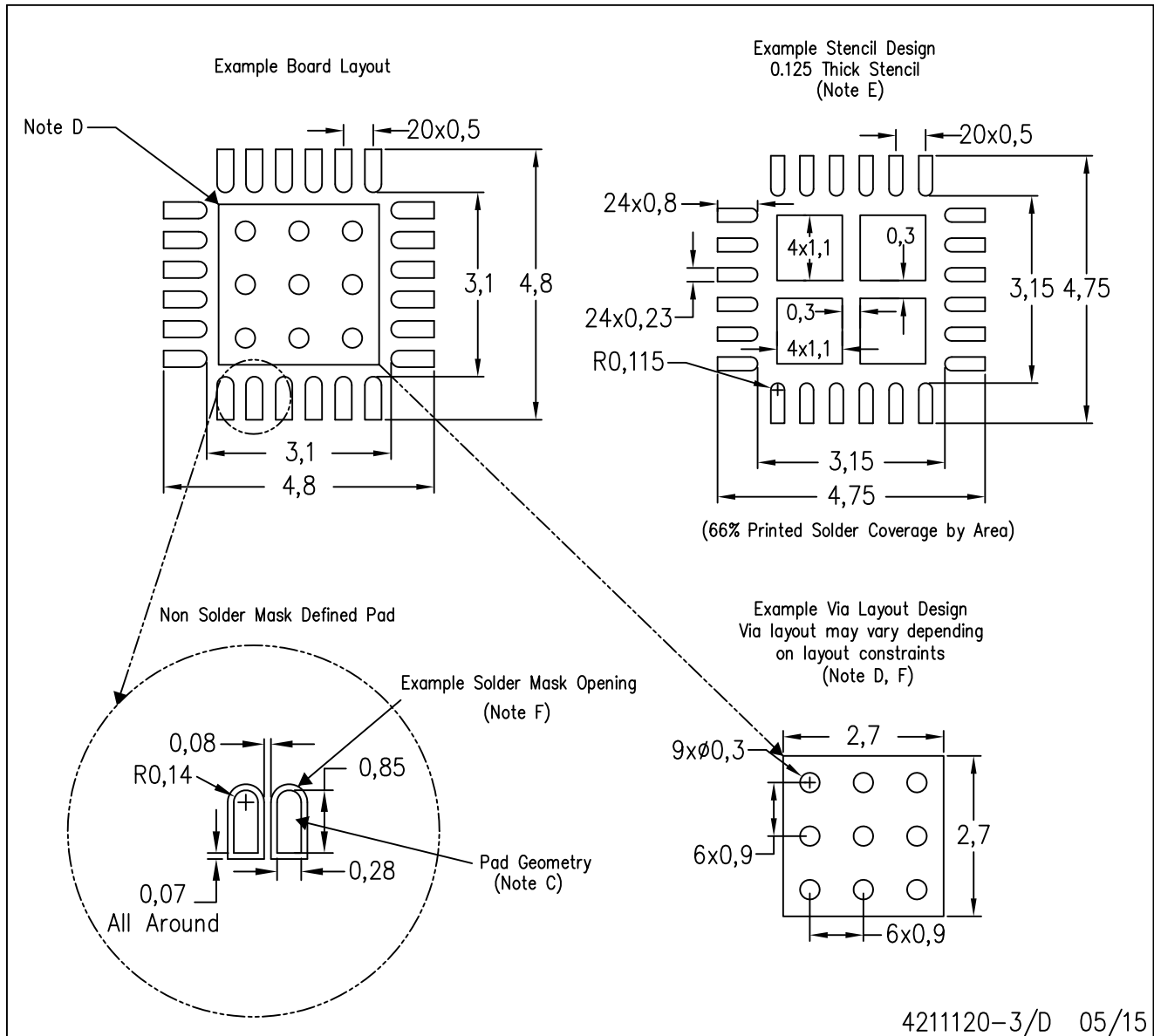
Exposed Thermal Pad Dimensions

4206249-5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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