TEXAS INSTRUMENTS
CD4051B, CD4052B, CD4053B
JAJSOR2L – AUGUST 1998 – REVISED SEPTEMBER 2023

CD405xB 8 チャネルを 1 セット備えた、CMOS アナログ・マルチプレクサ / デマルチプレクサ、ロジック・レベル変換付き

1 特長

- 幅広いデジタルおよびアナログ信号レベル:
  - デジタル:3V～20V
  - アナログ:20V_{P-P} 以下
- 低いオン抵抗、15V_{P-P} 信号入力範囲で、V_{DD} - V_{EE} = 18V において 125Ω (代表値)
- 高いオフ抵抗、V_{DD} - V_{EE} = 18V でチャネル・リーク ±100pA (代表値)
- 3V～20V のデジタル・アドレッシング信号 (V_{DD} - V_{SS} = 3V～20V) のロジック・レベル変換により、20V_{P-P} (V_{DD} - V_{EE} = 20V) に一致するスイッチ特性にアナログ信号をスイッチング、r_{ON} 5Ω (代表値、V_{DD} - V_{EE} = 15V の場合) ですべてのデジタル制御入力および電源条件において非常に低い静止電力、V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V において 0.2μW (代表値)
- オンチップでバイナリ・アドレスをデコード
- 5V、10V、15V のパラメータ定格
- 20V で静止電流を 100% テスト済み
- パッケージの温度範囲全体にわたって 18V 時に最大入力電流 1μA、25℃では 18V 時に 100nA
- Break-Before-Make スイッチングにより、チャネルのオーバーラップを排除

2 アプリケーション

- アナログおよびデジタルの多重化 / 多重分離
- アナログ・デジタルおよびデジタル・アナログ変換
- 信号ゲーティング
- ファクトリ・オートメーション
- テレビ
- 電化製品
- 民生用オーディオ
- プログラム可能な論理回路
- センサ

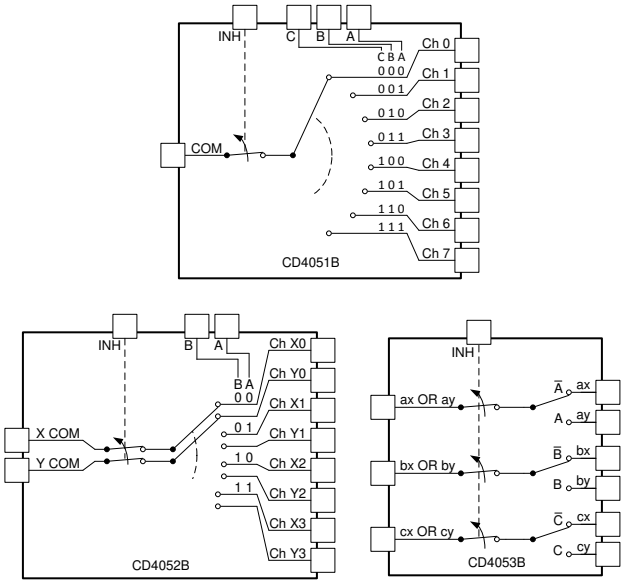
3 概要

CD405xB アナログ・マルチプレクサ / デマルチプレクサは、オン状態のインピーダンスが低くオフ状態のリーク電流が非常に小さいデジタル制御のアナログ・スイッチです。これらのマルチプレクサ回路は、制御信号の論理状態にかかわらず、V_{DD} - V_{SS} および V_{DD} - V_{EE} の電源電圧範囲全体にわたって非常に小さな静止電力しか消費しません。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (2)
CD405xB	J (CDIP、16)	19.50mm × 6.92mm
	N (PDIP、16)	19.3mm × 9.4mm
	D (SOIC、16)	9.9mm × 6mm
	NS (SOP、16)	10.2mm × 7.8mm
	PW (TSSOP、16)	5mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



CD405xB の機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision K (March 2023) to Revision L (September 2023) — **Page**

- 「パッケージ情報」表のフォーマットを更新し、パッケージ・リードのサイズを追加 ... 1
- Changed the format of the *ESD Ratings*, *Electrical Characteristics*, and *AC Performance* to consolidate package specifications ... 5

Changes from Revision J (February 2023) to Revision K (March 2023) — **Page**

- データシート全体にわたって PW パッケージ情報を追加 ... 1

Changes from Revision I (September 2017) to Revision J (February 2023) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated the *Quiescent Device Current, IDD Max* typical and maximum values ... 5
- Updated the *OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)* typical values ... 5
- Updated the *ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (Common OUT/IN) (Max)* maximum values ... 5
- Updated the *Input Low Voltage, VIL, Max* values ... 5
- Updated the *Input Current, IIN (Max)* typical values ... 5
- Updated the *Inhibit-to-Signal OUT (Channel Turning OFF)* typical values ... 5
- Updated the values in the *ESD Ratings* section ... 5
- Updated the *Typical Characteristics* section ... 10

Changes from Revision H (April 2015) to Revision I (September 2017) — **Page**

- Added the *On Channel Leakage Current – Any Channel On* figure ... 10

Changes from Revision G (October 2003) to Revision H (April 2015) — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- 「製品情報」表を追加 ... 1

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5 Pin Configuration and Functions

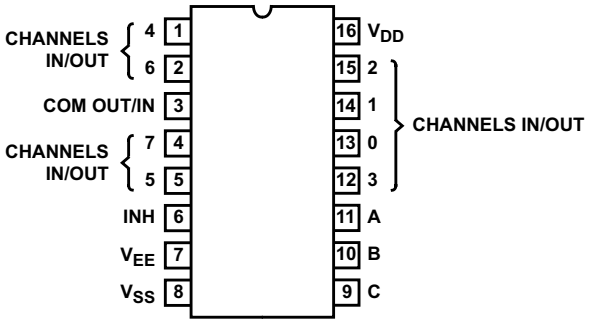

図 5-1. CD4051B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

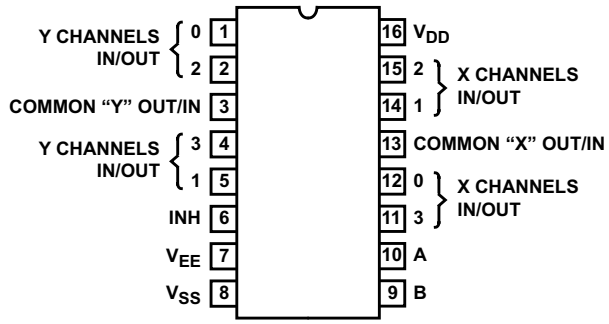

図 5-2. CD4052B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

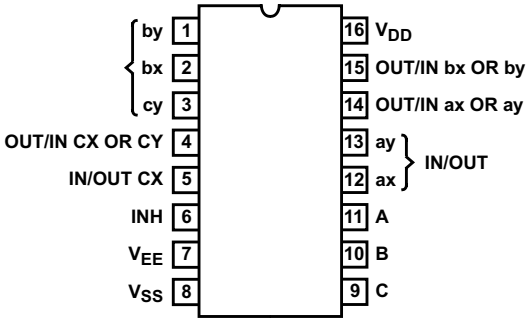

図 5-3. CD4053B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

表 5-1. Pin Functions CD4051B

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See 表 8-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See 表 8-1.
10	B	I	Channel select B. See 表 8-1.
11	A	I	Channel select A. See 表 8-1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V_{DD}	—	Positive power input

(1) I = input, O = output

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表 5-2. Pin Functions CD4052B

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See 表 8-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	B	I	Channel select B. See 表 8-1.
10	A	I	Channel select A. See 表 8-1.
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V_{DD}	—	Positive power input

(1) I = input, O = output

表 5-3. Pin Functions CD4053B

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See 表 8-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See 表 8-1.
10	B	I	Channel select B. See 表 8-1.
11	A	I	Channel select A. See 表 8-1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V_{DD}	—	Positive power input

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V_{SS} Terminal	–0.5	20	V
	DC Input Voltage		–0.5	V_{DD}+0.5	V
	DC Input Current	Any One Input	–10	10	mA
T_{JMAX1}	Maximum junction temperature, ceramic package			175	°C
T_{JMAX2}	Maximum junction temperature, plastic package			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
CD405xB all packages				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		CD405x				UNIT
		E (PDIP)	M (SOIC)	NS (SOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	73	64	116.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
	V_{IS} (V)	**V_{EE} (V)**	**V_{SS} (V)**	**V_{DD} (V)**	**TEMP**				
Quiescent Device Current, I_{DD} Max		0 V	0 V	5 V	–55°C			60	µA
					–40°C			60	
					25°C		17	60	
					85°C			150	
					125°C			150	
		0 V	0 V	10 V	–55°C			60	
					–40°C			60	
					25°C		18	60	
					85°C			300	
					125°C			300	
		0 V	0 V	15 V	–55°C			60	
					–40°C			60	
					25°C		18	60	
					85°C			600	
					125°C			600	
		0 V	0 V	20 V	–55°C			100	
					–40°C			100	
					25°C		18	100	
					85°C			3000	
					125°C			3000	
Drain to Source ON Resistance r_{ON} Max $0 \le V_{IS} \le V_{DD}$		0 V	0 V	5 V	–55°C			800	Ω
					–40°C			850	
					25°C		470	1050	
					85°C			1200	
					125°C			1300	
		0 V	0 V	10 V	–55°C			310	
					–40°C			300	
					25°C		180	400	
					85°C			520	
					125°C			550	
		0 V	0	15 V	–55°C			200	
					–40°C			210	
					25°C		125	240	
					85°C			300	
					125°C			300	
Change in ON Resistance (Between Any Two Channels), ΔR_{ON}		0 V	0 V	5 V	25°C		15		Ω
		0 V	0 V	10 V			10		
		0 V	0 V	15 V			5		

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS					MIN	TYP	MAX	UNIT
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)				0 V	0 V	18 V	–55°C			± 100	nA
							–40°C				
							25°C		± 0.3	± 100(2)	
							85°C			± 1000 (2)	
							125°C				
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)			5 or 0	–5 V	0 V	10.5 V	85°C			± 800	nA
			5	0 V	0 V	18 V	85°C			± 800	
Capacitance	Input, C_{IS}			0 V	0 V	10 V	25°C		5		pF
	Output, C_{OS}	CD4051							30		
	Output, C_{OS}	CD4052							18		
	Output, C_{OS}	CD4053							9		
	Feed through, C_{IOS}								0.2		
Prop Delay			V_{DD}	R_L = 200 kΩ		5 V	25°C		30	60	ns
				C_L = 50 pF		10 V			15	30	
				t_r, t_f = 20 ns		15 V			10	20	

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
CONTROL (ADDRESS OR INHIBIT), V_C										
Input Low Voltage, V_{IL}, Max					5 V	–55°C			0.8	V
						–40°C			0.8	
						25°C			0.8	
						85°C			0.8	
						125°C			0.8	
					10 V	–55°C			0.8	
						–40°C			0.8	
						25°C			0.8	
						85°C			0.8	
						125°C			0.8	
					15 V	–55°C			0.8	
						–40°C			0.8	
						25°C			0.8	
						85°C			0.8	
						125°C			0.8	
Input High Voltage, V_{IH}, Min					5 V	–55°C			3.5	V
						–40°C			3.5	
						25°C	3.5			
						85°C			3.5	
						125°C			3.5	
					10 V	–55°C			7	
						–40°C			7	
						25°C	7			
						85°C			7	
						125°C			7	
					15 V	–55°C			11	
						–40°C			11	
						25°C	11			
						85°C			11	
						125°C			11	
Input current, I_{IN} (Max)		V_{IN} = 0, 18			18 V	–55°C			±1	μA
						–40°C			±1	
						25°C		±0.6	±1	
						85°C			±1	
						125°C			±1	
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 7-2, Figure 7-3, and Figure 7-8)	t_r , t_f = 20ns, C_L = 50 pF, R_L = 10 kΩ	0 V	0 V	5 V			450	720	ns
			0 V	0 V	10 V			160	320	
			0 V	0 V	15 V			120	240	
			–5 V	0 V	5 V			225	450	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 7-3)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	0 V	0 V	5 V			400	720	ns
			0 V	0 V	10 V			160	320	
			0 V	0 V	15 V			120	240	
			–10 V	0 V	5 V			200	400	

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 7-10)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ	0 V	0 V	5 V			200	450	ns
			0 V	0 V	10 V			90	210	
			0 V	0 V	15 V			70	160	
			–10 V	0 V	5 V			130	300	
Input Capacitance, C_{IN} (Any Address or Inhibit Input)			–5 V	0 V	5 V	25°C		5	7.5	pF

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.
(2) Determined by minimum feasible leakage measurement for automatic testing.

6.6 AC Performance Characteristics

V_{DD} = +15 V, V_{SS} = V_{EE} = 0 V,
T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS					TYP	UNIT
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)				
Cutoff (–3dB) Frequency Channel ON (Sine Wave Input)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
		10	1		CD4052	25	
		10	1		CD4051	20	
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3 dB			V_{OS} at Any Channel		60	
Total Harmonic Distortion, THD	2(1)	5	10			0.3%	%
	3(1)	10	10			0.2%	
	5(1)	15	10			0.12%	
	V_{EE} = V_{SS}, f_{IS} = 1 kHz Sine Wave						
–40dB Feedthrough Frequency (All Channels OFF)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –40 dB				CD4052	10	
					CD4051	12	
				V_{OS} at Any Channel		8	
–40dB Signal Crosstalk Frequency	5(1)	10	1			3	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3 dB			Between Sections, CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to-Signal Crosstalk		10	10(2)			65	mV_{PEAK}
	V_{EE} = 0, V_{SS} = 0, t_r , t_f = 20 ns, mVPEAK V_{CC} = V_{DD} – V_{SS} (Square Wave)					65	mV_{PEAK}

(1) Peak-to-Peak voltage symmetrical about (V_{DD} - V_{EE}) / 2.
(2) Both ends of channel.

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6.7 Typical Characteristics

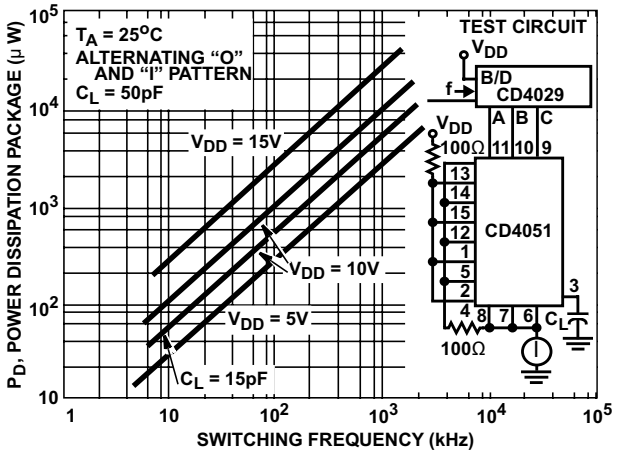

図 6-1. Dynamic Power Dissipation vs Switching Frequency (CD4051B)

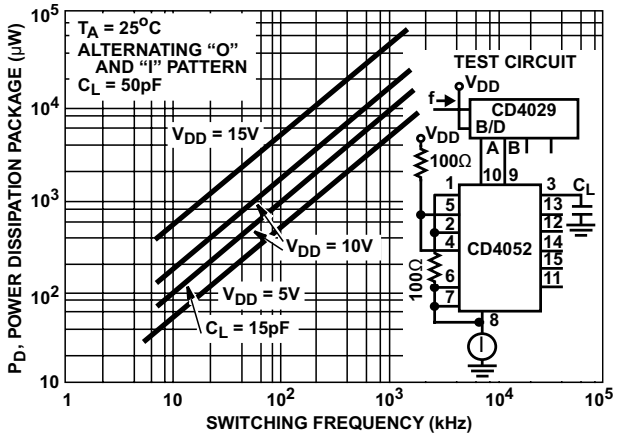

図 6-2. Dynamic Power Dissipation vs Switching Frequency (CD4052B)

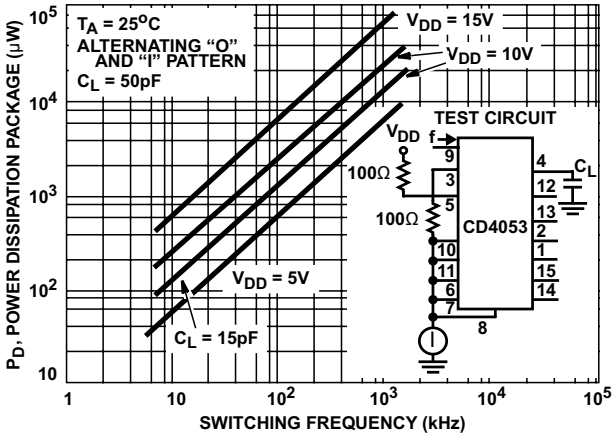

図 6-3. Dynamic Power Dissipation vs Switching Frequency (CD4053B)

7 Parameter Measurement Information

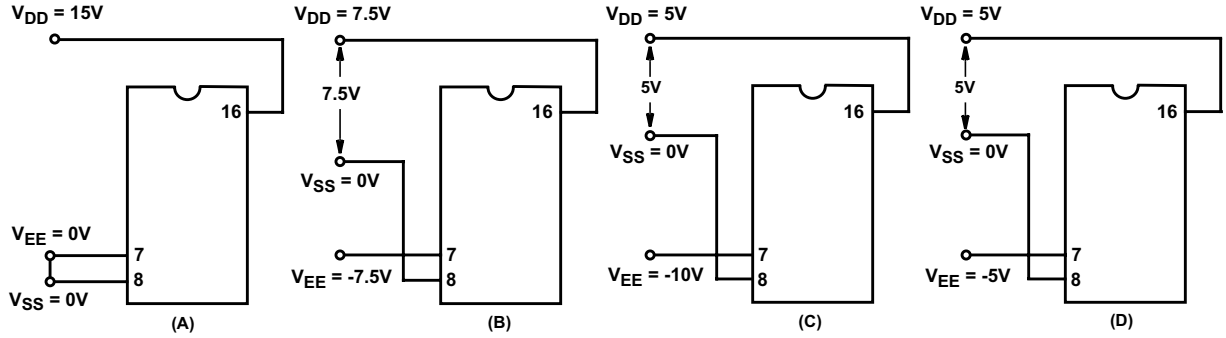

図 7-1. Typical Bias Voltages

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注

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V_{SS} and 1 = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

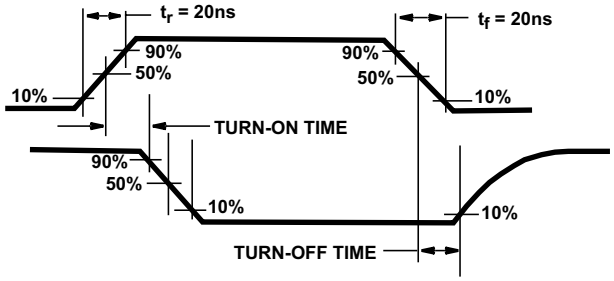

図 7-2. Waveforms, Channel Being Turned ON (R_L = 1 kΩ)

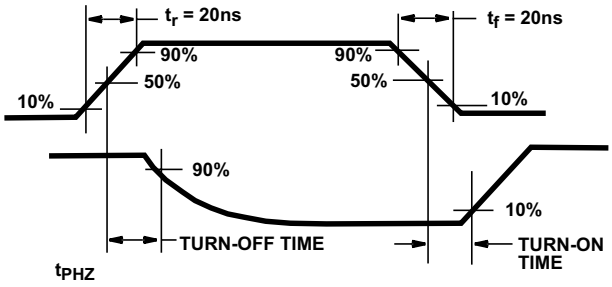

図 7-3. Waveforms, Channel Being Turned OFF (R_L = 1 kΩ)

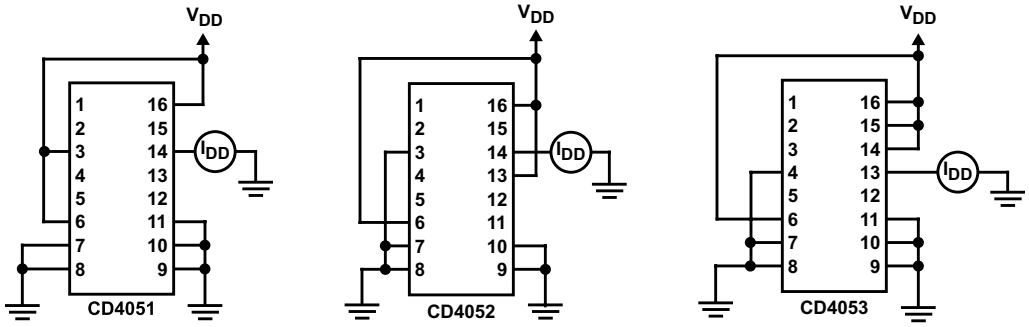

図 7-4. OFF Channel Leakage Current – Any Channel OFF

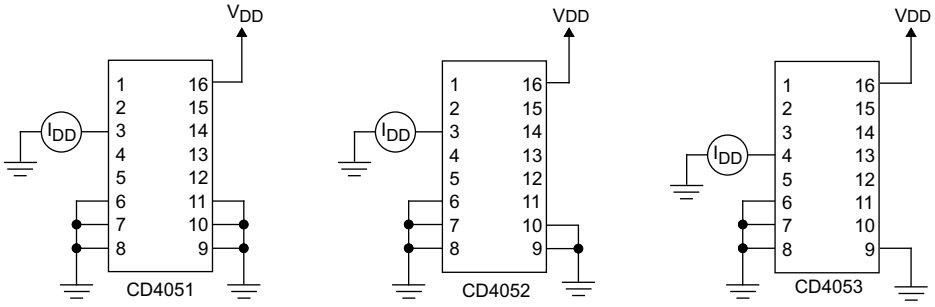

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図 7-5. On Channel Leakage Current – Any Channel On

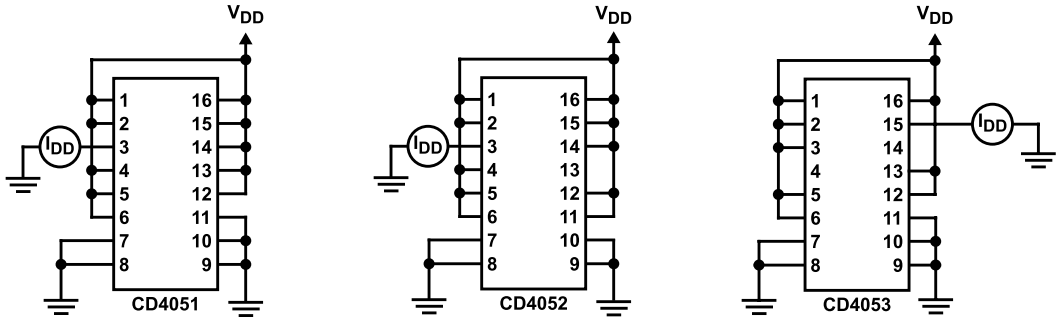

図 7-6. OFF Channel Leakage Current – All Channels OFF

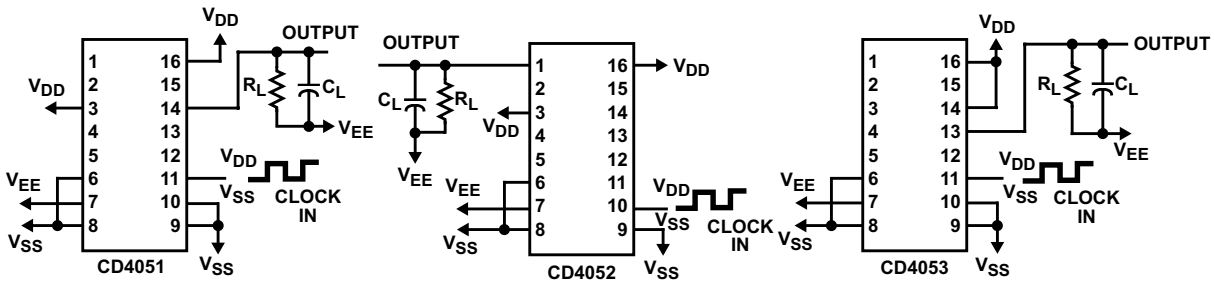

図 7-7. Propagation Delay – Address Input to Signal Output

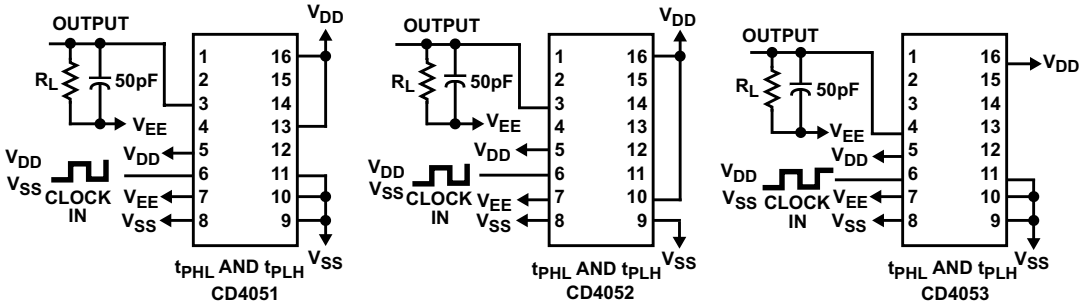

図 7-8. Propagation Delay – Inhibit Input to Signal Output

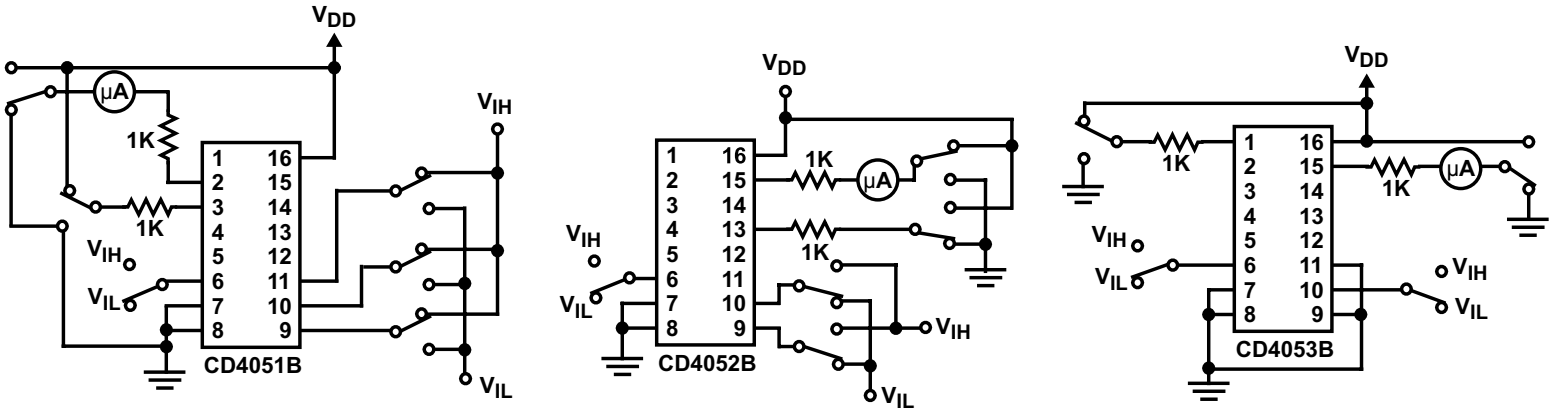

図 7-9. Input Voltage Test Circuits (Noise Immunity)

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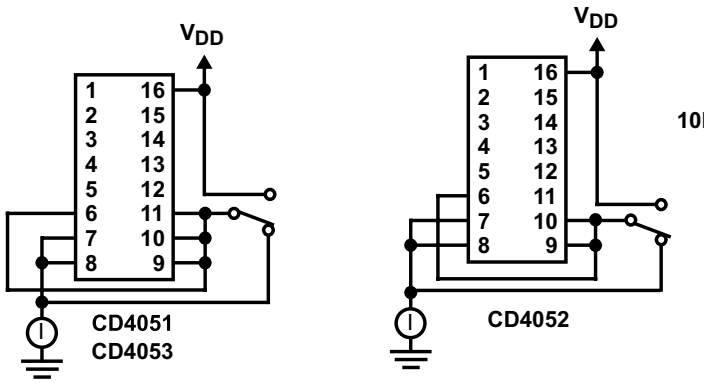


図 7-10. Quiescent Device Current

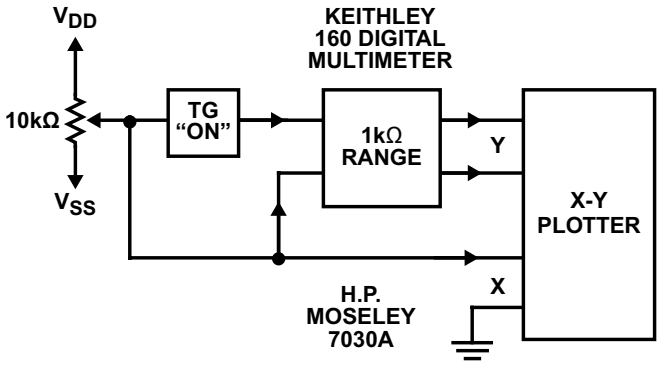
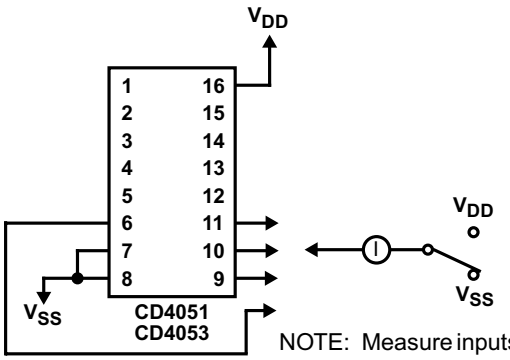
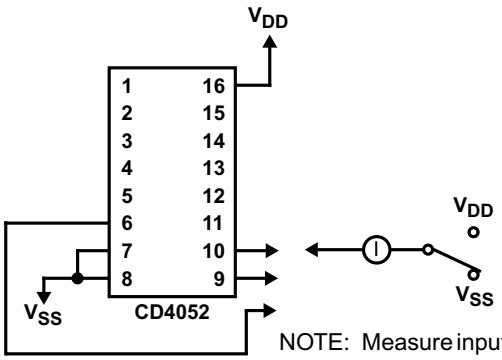


図 7-11. Channel ON Resistance Measurement Circuit



NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.



NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.

図 7-12. Input Current

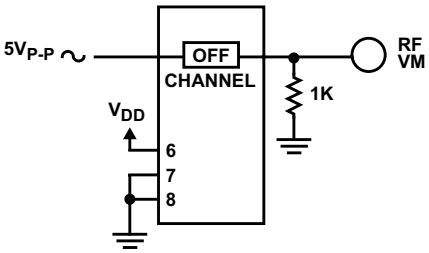


図 7-13. Feed-Through (All Types)

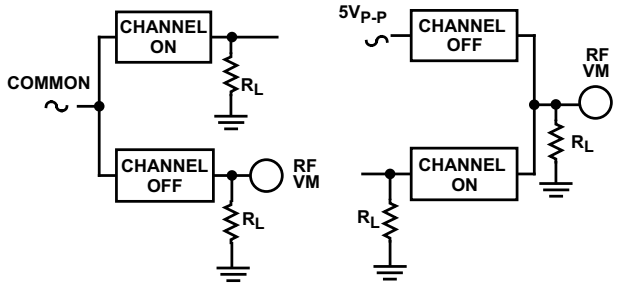
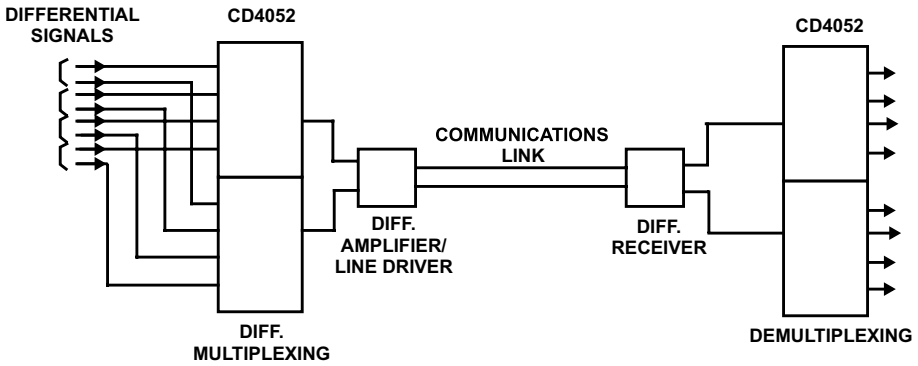


図 7-14. Crosstalk Between Any Two Channels (All Types)

図 7-15. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)



Special Considerations: In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

図 7-16. Typical Time-Division Application of the CD4052B

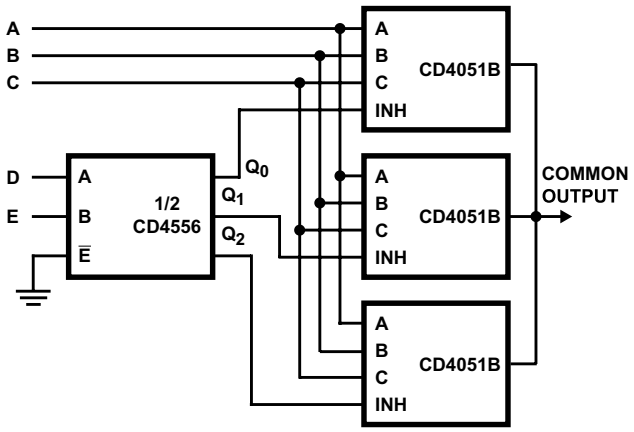


図 7-17. 24-to-1 MUX Addressing

8 Detailed Description

8.1 Overview

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V_{P-P} can be achieved by digital signal amplitudes of 4.5 V to 20 V (if $V_{DD} – V_{SS}$ = 3 V, a $V_{DD} – V_{EE}$ of up to 13 V can be controlled; for $V_{DD} – V_{EE}$ level differences above 13 V, a $V_{DD} – V_{SS}$ of at least 4.5 V is required). For example, if V_{DD} = +4.5 V, V_{SS} = 0 V, and V_{EE} = –13.5 V, analog signals from –13.5 V to +4.5 V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} – V_{SS}$ and $V_{DD} – V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic 1 is present at the inhibit input terminal, all channels are off.

The CD4051B device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B device is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

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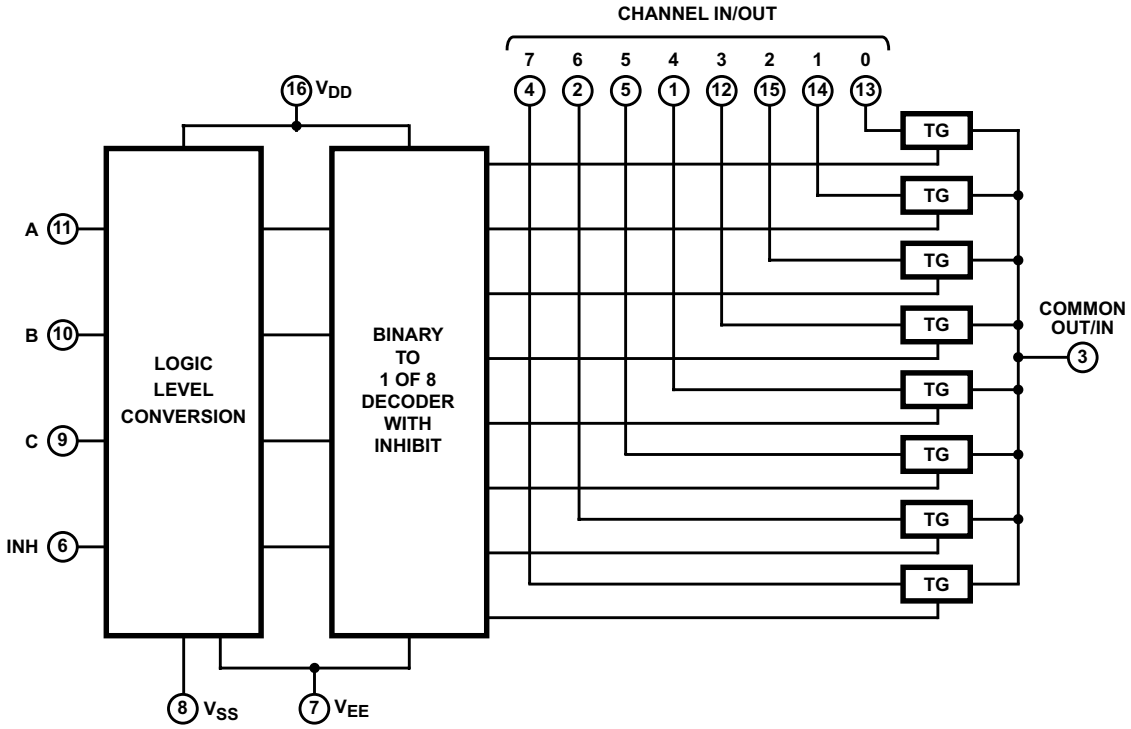
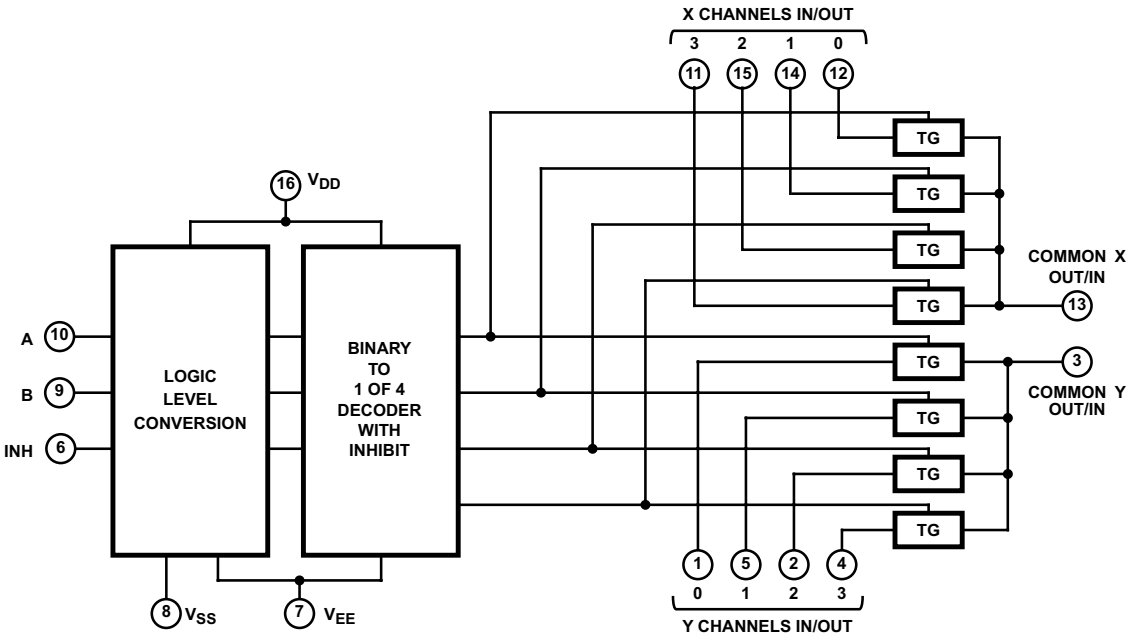
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

8.2 Functional Block Diagrams



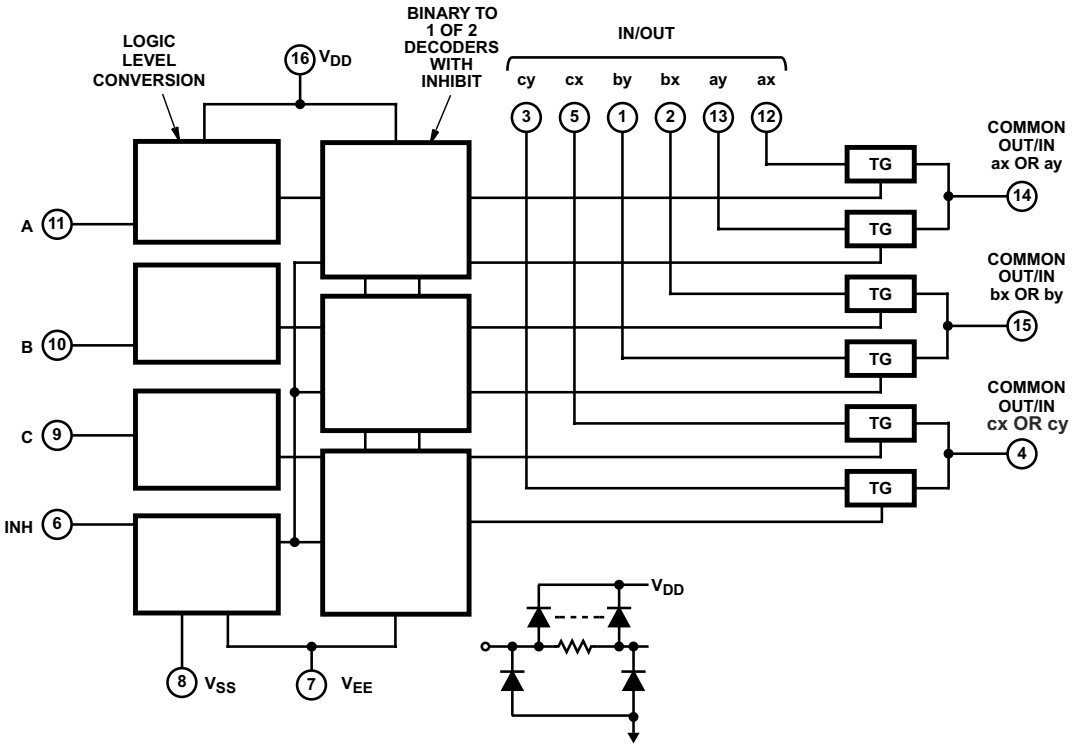
All inputs are protected by standard CMOS protection network.

図 8-1. Functional Block Diagram, CD4051B



All inputs are protected by standard CMOS protection network.

図 8-2. Functional Block Diagram, CD4052B



All inputs are protected by standard CMOS protection network.

図 8-3. Functional Block Diagram, CD4053B

8.3 Feature Description

The CD405xB line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3 V to 20 V, and analog signals are accepted at levels ≤ 20 V. The devices have low ON resistance, typically 125 Ω over 15 V_{P-P} signal input range for V_{DD} – V_{EE} = 18 V. This feature allows for very little signal loss through the switch. Matched switch characteristics are typically r_{ON} = 5 Ω for V_{DD} – V_{EE} = 15 V.

The CD405xB devices also have high OFF resistance, which keeps from wasting power when the switch is in the OFF position, with typical channel leakage of ±100 pA at V_{DD} – V_{EE} = 18 V. Very low quiescent power dissipation under all digital-control input and supply conditions, typically 0.2 µW at V_{DD} – V_{SS} = V_{DD} – V_{EE} = 10 V keeps power consumption total very low. All devices have been 100% tested for quiescent current at 20 V with maximum input current of 1 µA at 18 V over the full package temperature range, and only 100 nA at 18 V and 25°C.

Logic-level conversion for digital addressing signals of 3 V to 20 V (V_{DD} – V_{SS} = 3 V to 20 V) to switch analog signals to 20 V_{P-P} (V_{DD} – V_{EE} = 20 V). Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

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8.4 Device Functional Modes

表 8-1. Truth Table(1)

INPUT STATES				ON CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
CD4053B				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1) X = Do not care

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9 Application and Implementation

注

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9.1 Application Information

The CD405xB multiplexers and demultiplexers can be used for a wide variety of applications.

9.2 Typical Application

One application of the CD4051B is to use it in conjunction with a microcontroller to poll a keypad. 図 9-1 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

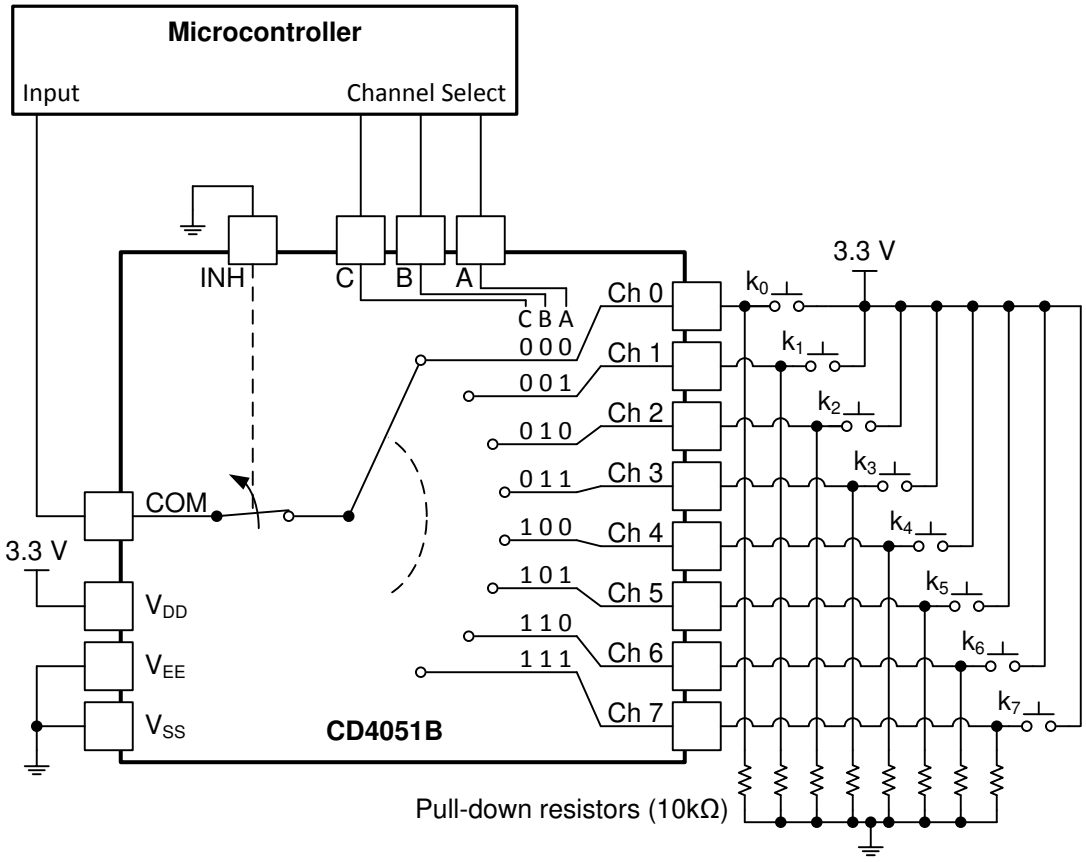

図 9-1. The CD4051B Being Used to Help Read Button Presses on a Keypad

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

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9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For switch time specifications, see propagation delay times in *Electrical Characteristics*.
   - Inputs should not be pushed more than 0.5 V above V_{DD} or below V_{EE}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in *Electrical Characteristics*.
2. Recommended Output Conditions:
   - Outputs should not be pulled above V_{DD} or below V_{EE}.
3. Input or output current consideration:
   - The CD405xB series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

9.2.3 Application Curve

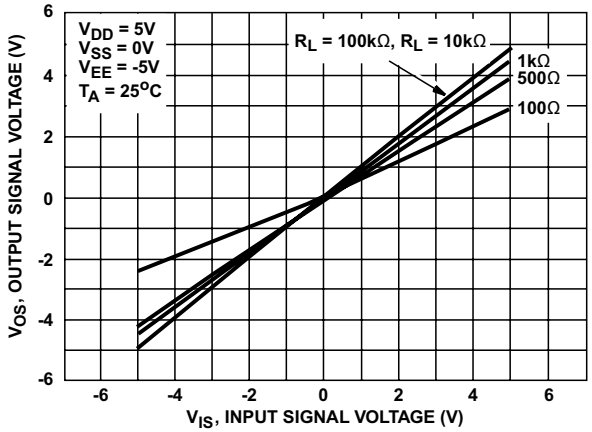

図 9-2. ON Characteristics for 1 of 8 Channels (CD4051B)

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Electrical Characteristics*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 図 9-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

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9.4.2 Layout Example

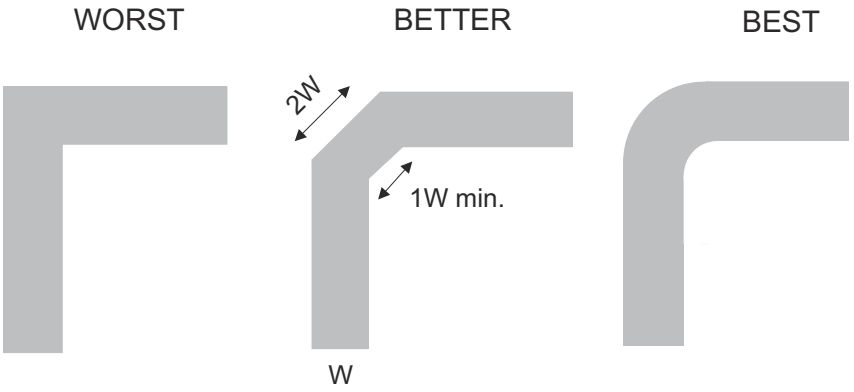

図 9-3. Trace Example

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7901502EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	Samples
8101801EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	Samples
CD4051BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4051BE	Samples
CD4051BEE4	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4051BE	
CD4051BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF	Samples
CD4051BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF3A	Samples
CD4051BM	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	
CD4051BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	Samples
CD4051BM96G3	LIFEBUY	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	
CD4051BM96G4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	
CD4051BMG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	
CD4051BMT	LIFEBUY	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	
CD4051BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	Samples
CD4051BPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	
CD4051BPWE4	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	
CD4051BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	Samples
CD4051BPWRG4	NRND	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	
CD4051BQPWRG4KN	LIFEBUY	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		CM051BQ	
CD4052BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	Samples
CD4052BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	Samples
CD4052BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4052BF	Samples
CD4052BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4052BM	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	
CD4052BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	Samples
CD4052BM96G3	LIFEBUY	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4052BM	
CD4052BM96G4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	
CD4052BMG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	
CD4052BMT	LIFEBUY	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	
CD4052BNS	LIFEBUY	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		CD4052B	
CD4052BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B	Samples
CD4052BPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	
CD4052BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4052BPWRG3	NRND	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CM052B	
CD4052BPWRG4	NRND	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	
CD4053BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4053BF	Samples
CD4053BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	Samples
CD4053BM	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BM96E4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BM96G3	LIFEBUY	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BM96G4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BMG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BMT	LIFEBUY	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	
CD4053BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B	Samples
CD4053BPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	
CD4053BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4053BPWRG3	NRND	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	CM053B	
CD4053BPWRG4	NRND	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4051B, CD4051B-MIL, CD4052B, CD4052B-MIL, CD4053B, CD4053B-MIL :

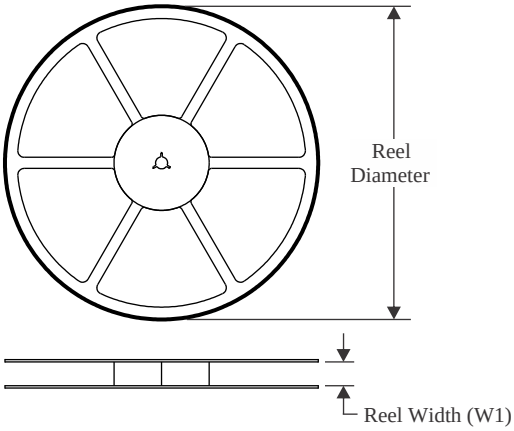
- Catalog : CD4051B, CD4052B, CD4053B
- Automotive : CD4051B-Q1, CD4051B-Q1, CD4053B-Q1, CD4053B-Q1
- Military : CD4051B-MIL, CD4052B-MIL, CD4053B-MIL

NOTE: Qualified Version Definitions:

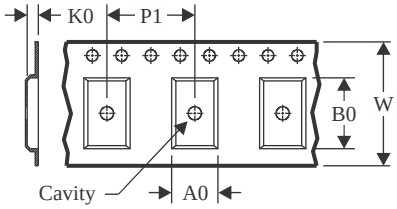
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

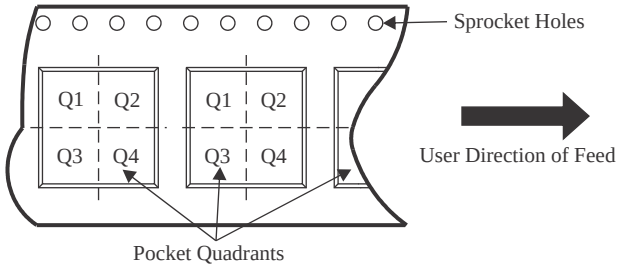


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

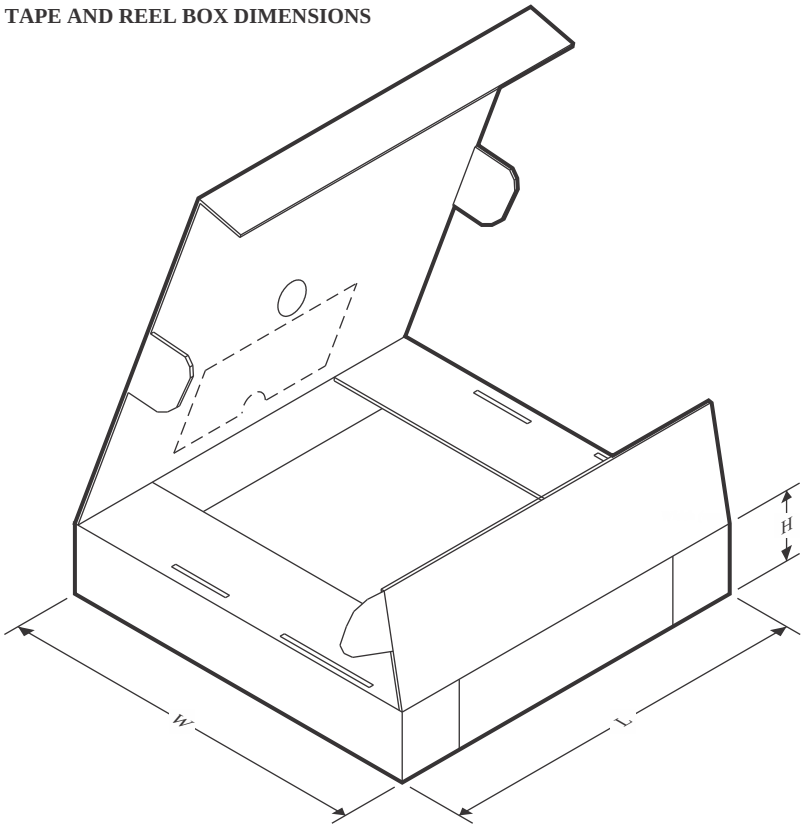


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4051BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BQPWRG4KN	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4052BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4053BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

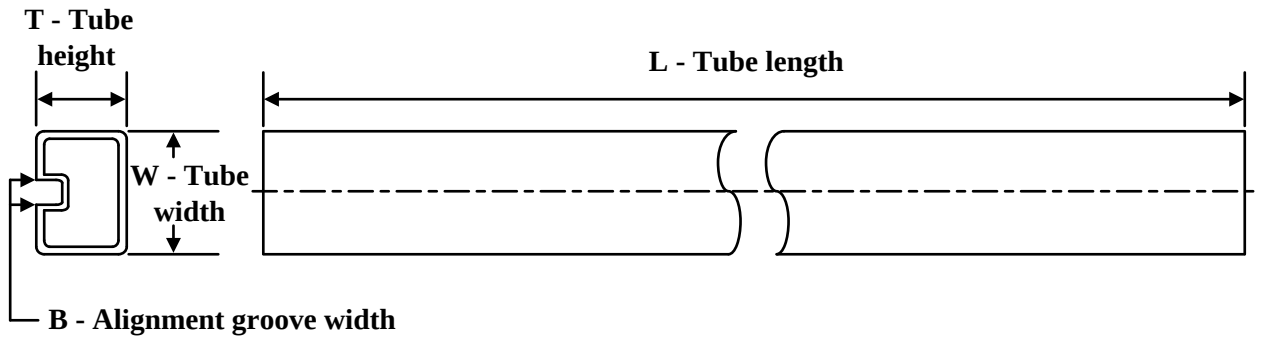


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BM96	SOIC	D	16	2500	356.0	356.0	35.0
CD4051BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4051BM96G4	SOIC	D	16	2500	340.5	336.1	32.0
CD4051BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD4051BNSR	SO	NS	16	2000	353.0	353.0	32.0
CD4051BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4051BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4051BQPWRG4KN	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BM96	SOIC	D	16	2500	356.0	356.0	35.0
CD4052BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4052BM96G4	SOIC	D	16	2500	340.5	336.1	32.0
CD4052BNSR	SO	NS	16	2000	353.0	353.0	32.0
CD4052BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD4052BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4052BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4053BM96G3	SOIC	D	16	2500	364.0	364.0	27.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4053BM96G4	SOIC	D	16	2500	340.5	336.1	32.0
CD4053BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD4053BNSR	SO	NS	16	2000	353.0	353.0	32.0
CD4053BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4053BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

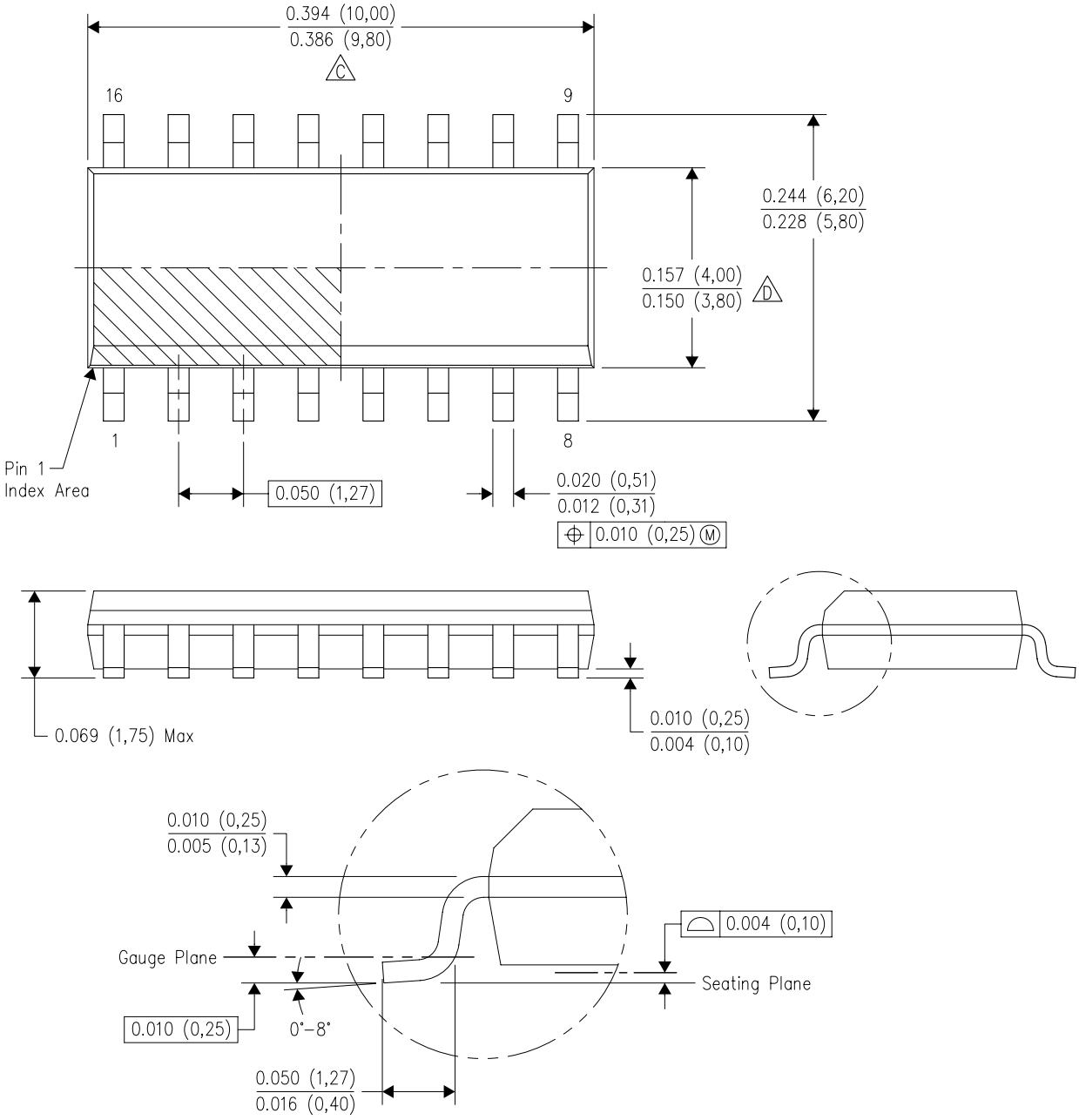
TUBE



*All dimensions are nominal

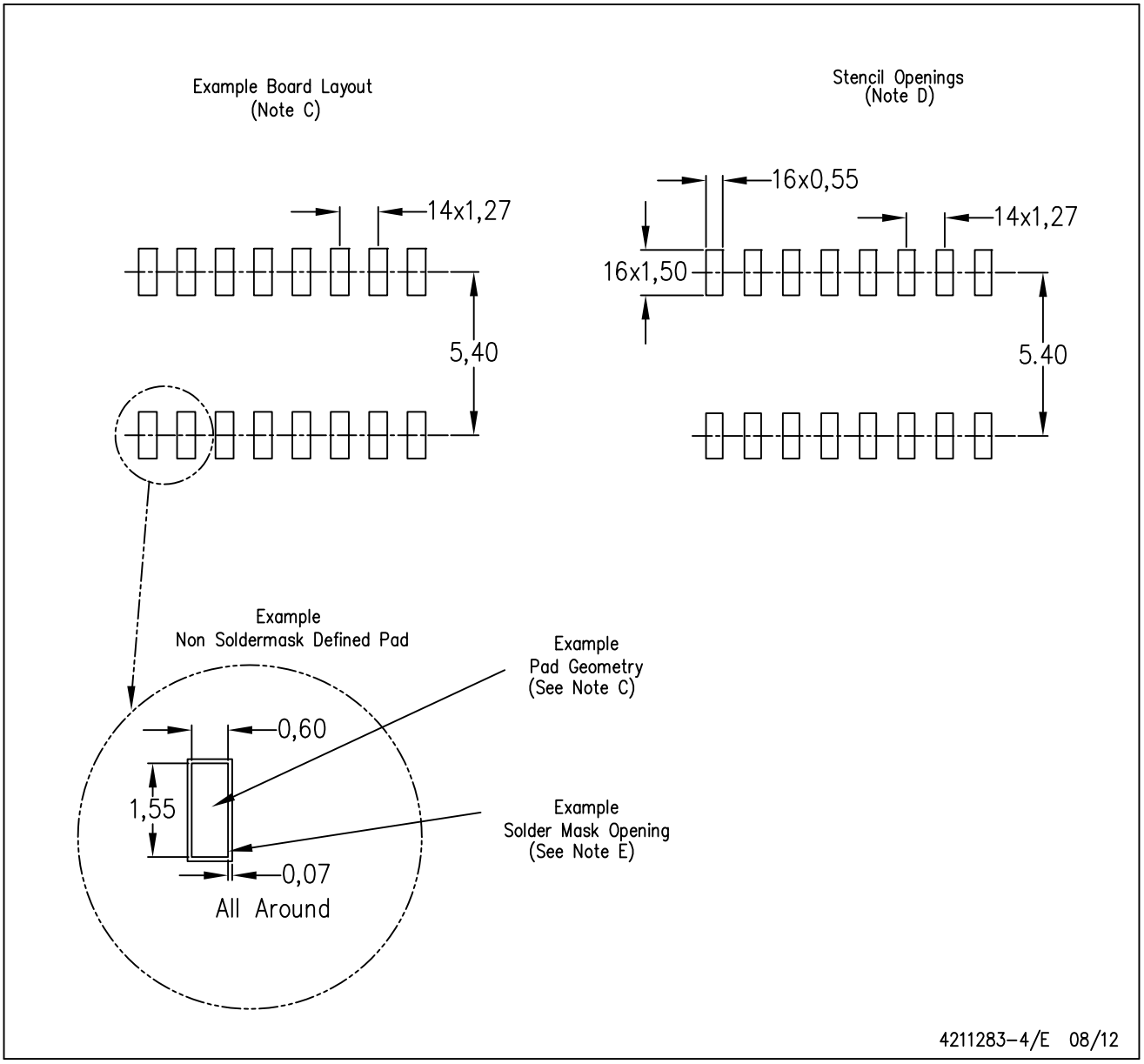
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4051BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4051BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4051BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4051BM	D	SOIC	16	40	506.6	8	3940	4.32
CD4051BM	D	SOIC	16	40	507	8	3940	4.32
CD4051BMG4	D	SOIC	16	40	507	8	3940	4.32
CD4051BMG4	D	SOIC	16	40	506.6	8	3940	4.32
CD4051BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4051BPWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4052BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BM	D	SOIC	16	40	507	8	3940	4.32
CD4052BMG4	D	SOIC	16	40	507	8	3940	4.32
CD4052BNS	NS	SOP	16	50	530	10.5	4000	4.1
CD4052BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4053BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BM	D	SOIC	16	40	507	8	3940	4.32
CD4053BMG4	D	SOIC	16	40	507	8	3940	4.32
CD4053BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



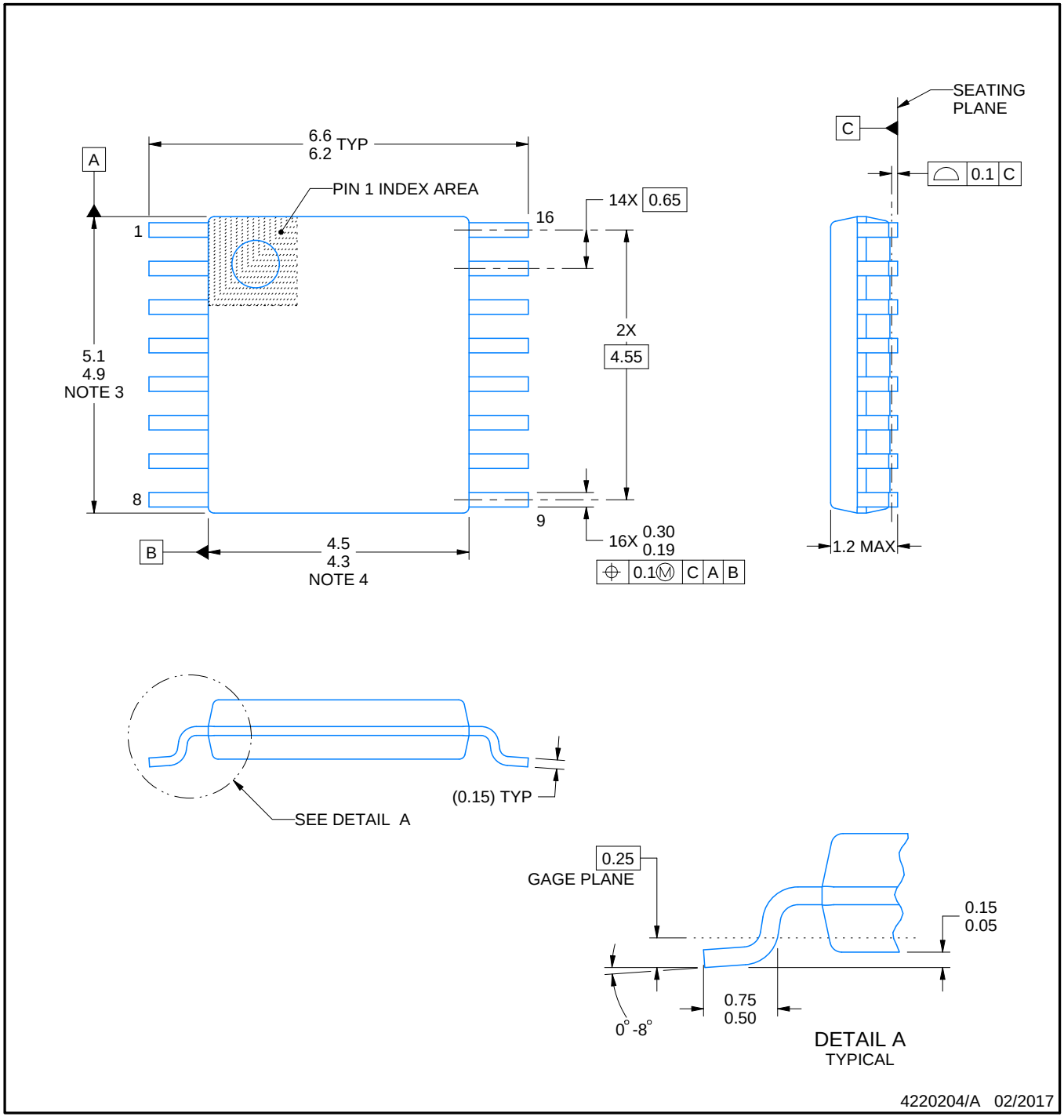
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

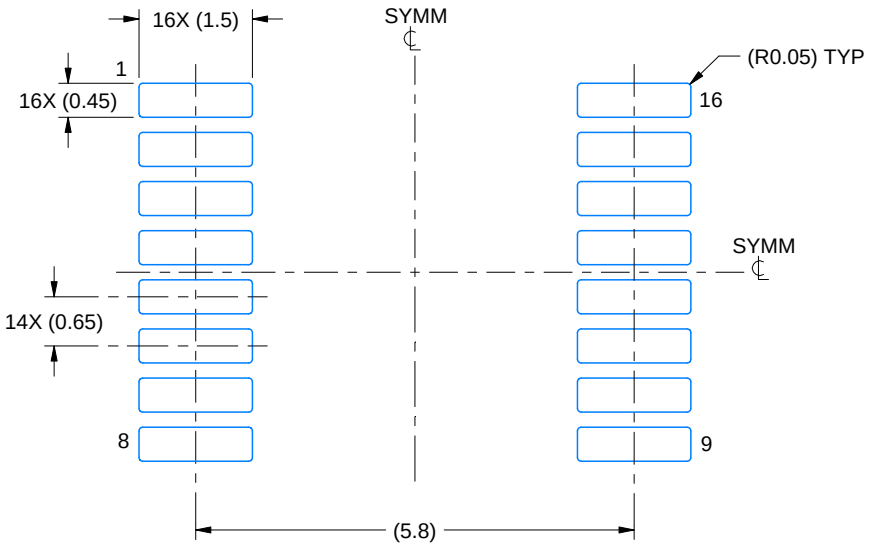
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



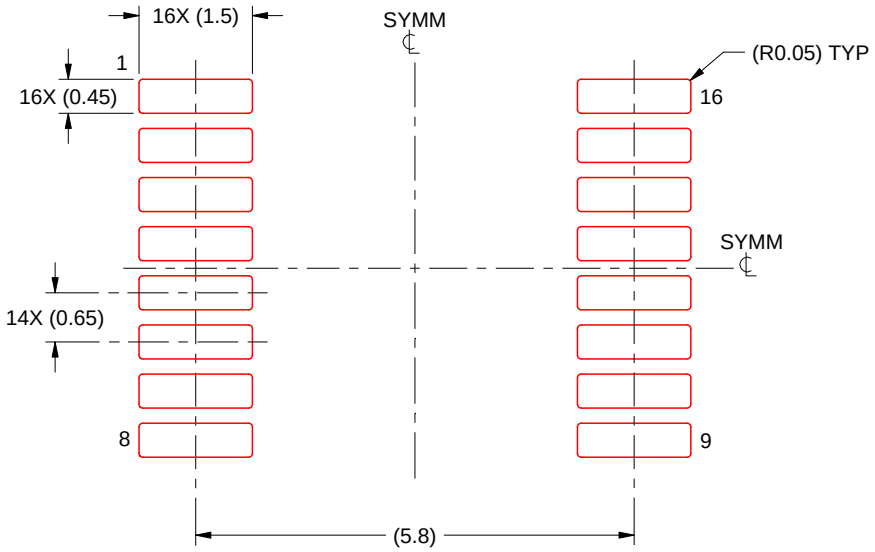
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

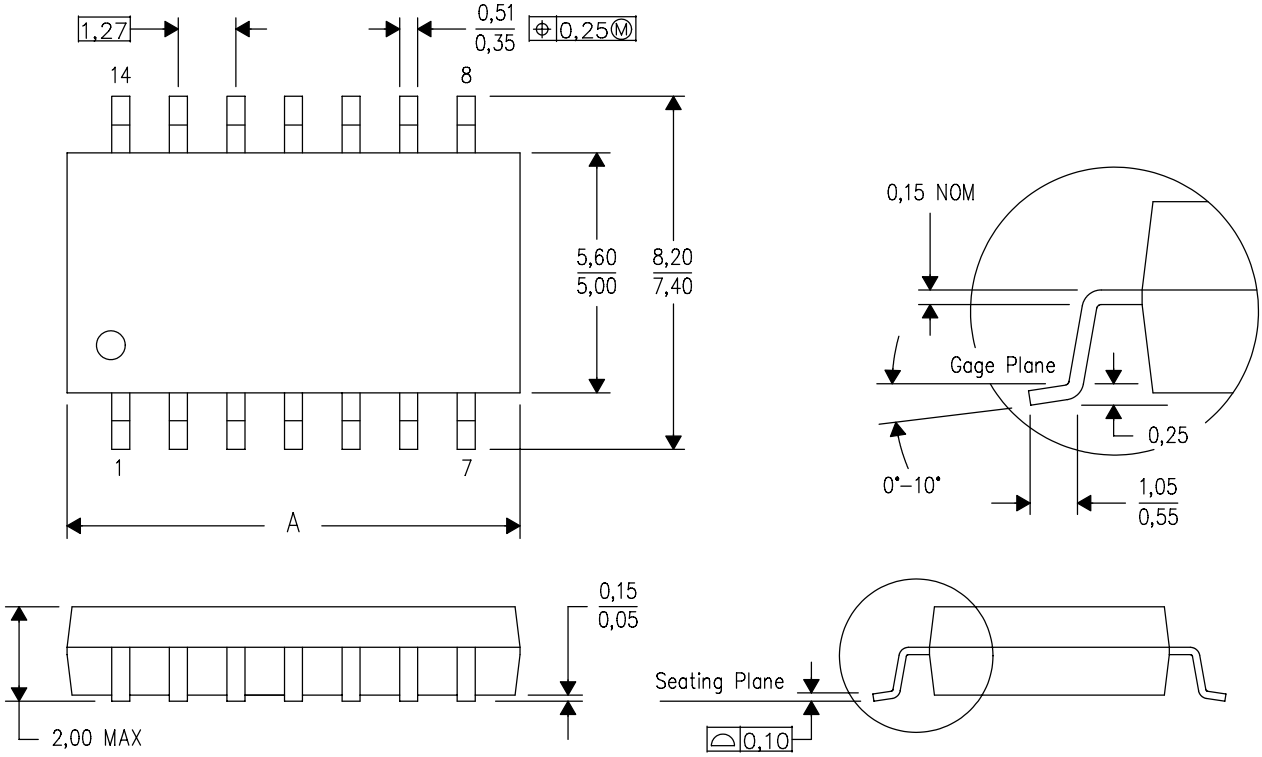
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

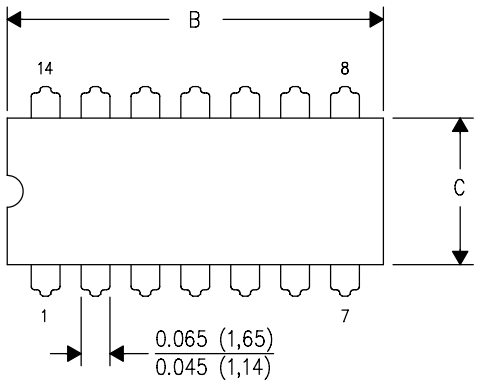
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

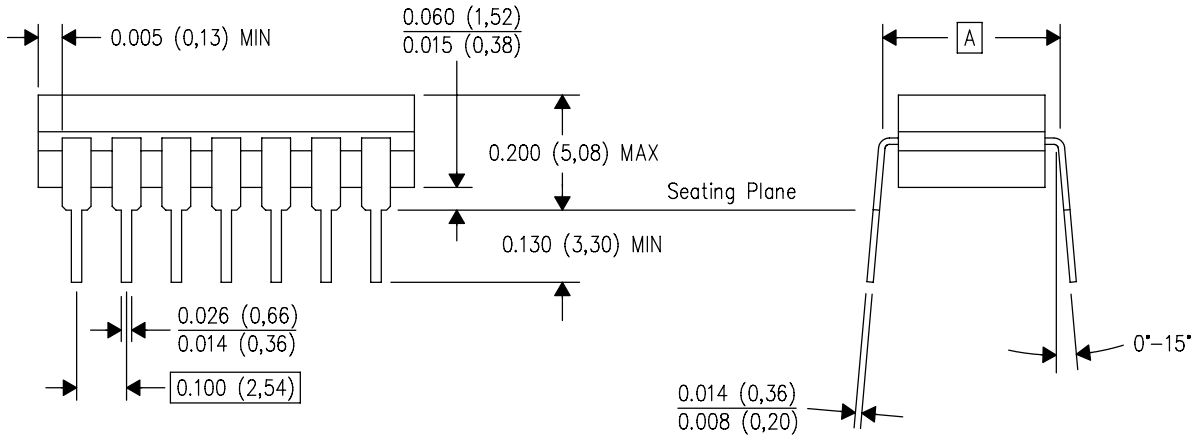
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



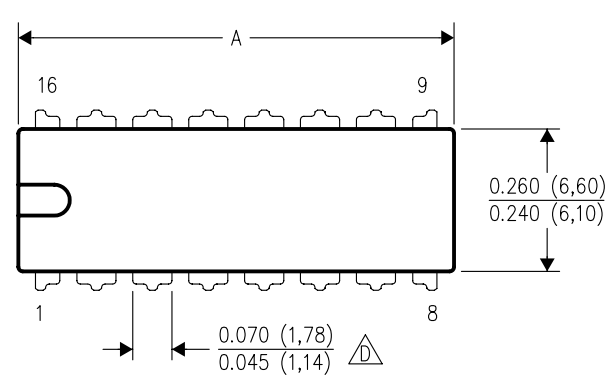
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

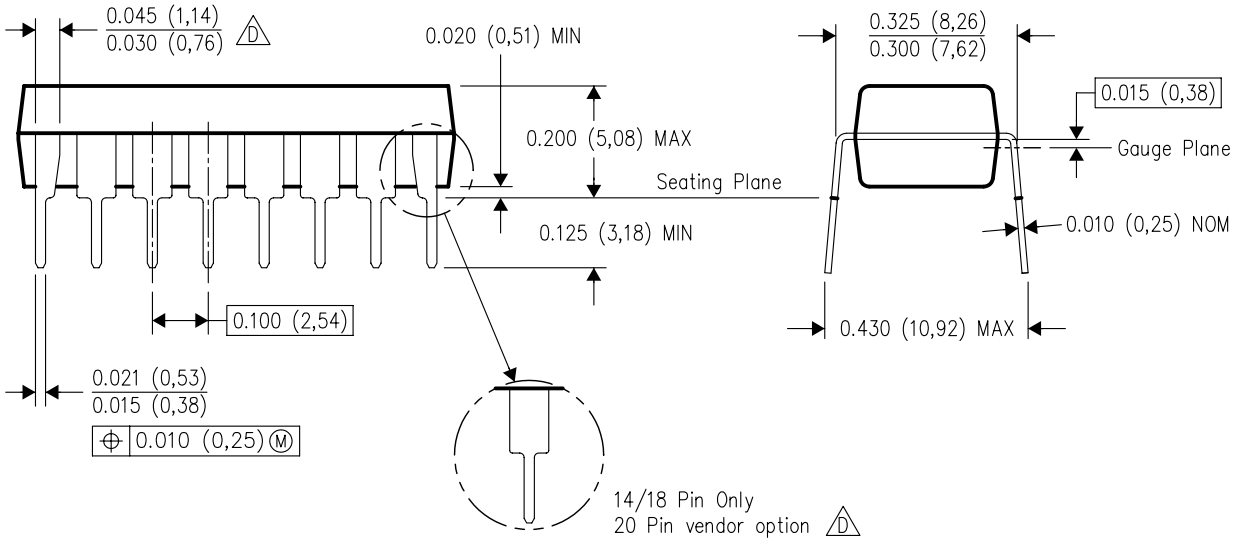
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

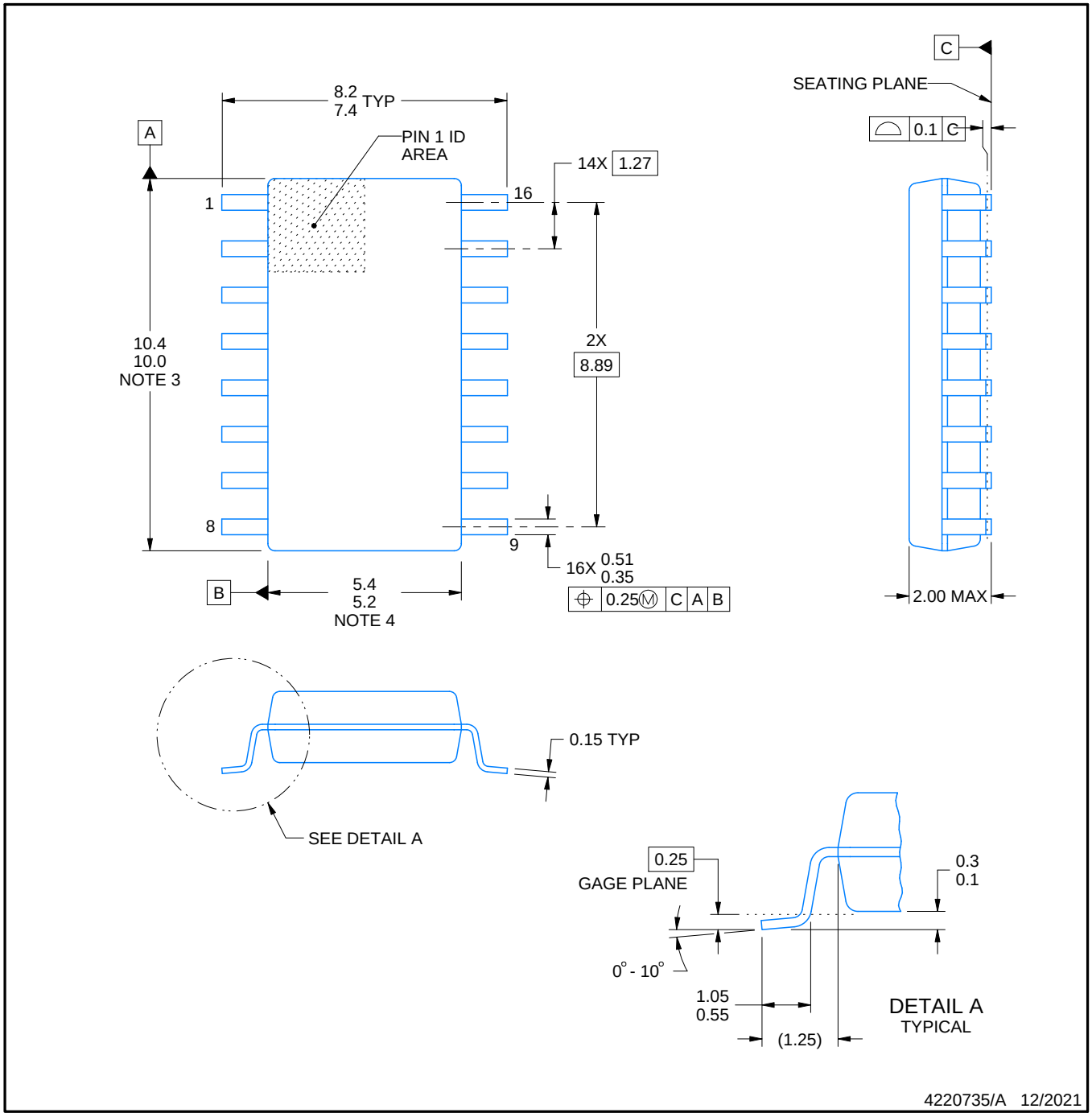


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



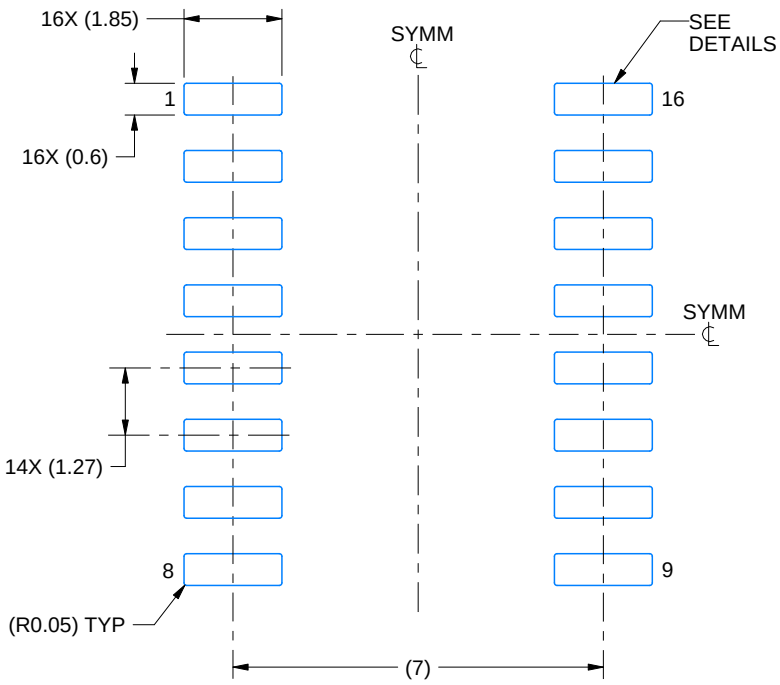
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

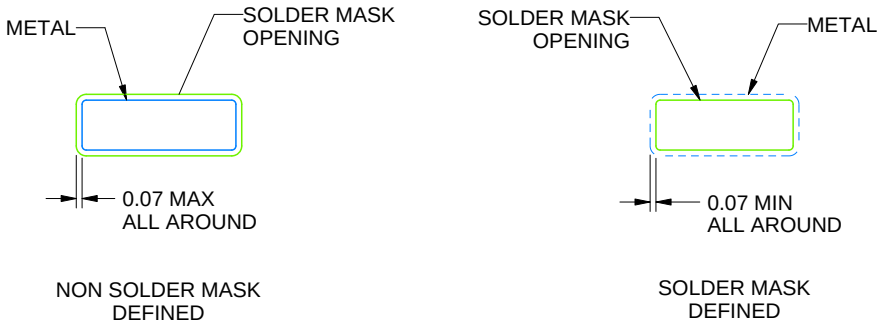


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

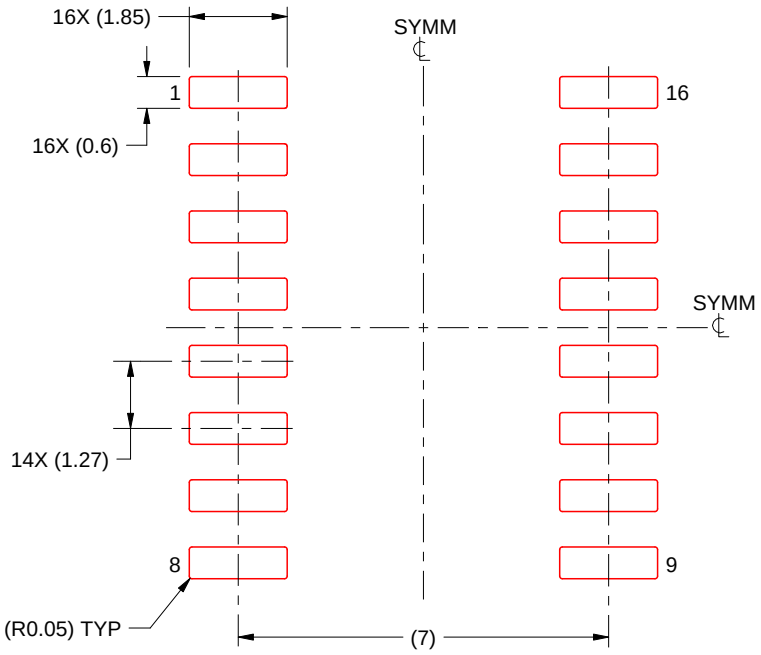


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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