TEXAS INSTRUMENTS
CSD13385F5
JAJSCK8B – OCTOBER 2016 – REVISED FEBRUARY 2022

CSD13385F5 12V N チャネル FemtoFET™ MOSFET

1 特長

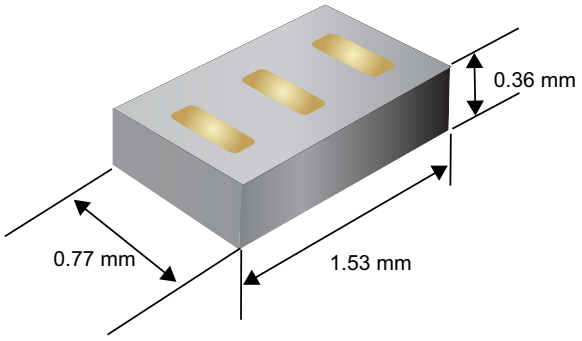
- 低いオン抵抗
- 低い Q_g および Q_{gd}
- 極めて小さいフットプリント
  - 1.53mm × 0.77mm
- 薄型
  - 高さ 0.36mm
- ESD 保護ダイオード搭載
  - HBM 定格 4kV 超
  - CDM 定格 2kV 超
- 鉛およびハロゲン不使用
- RoHS 準拠

2 アプリケーション

- 産業用ロード・スイッチ・アプリケーションに最適
- 汎用スイッチング・アプリケーションに最適

3 概要

この 12V、15mΩ、N チャネル FemtoFET™ MOSFET テクノロジは、さまざまなハンドヘルドおよびモバイル・アプリケーション向けに、フットプリントを最小化するよう設計され、最適化されています。標準の小信号 MOSFET をこのテクノロジに置き換えることで、フットプリント・サイズを大幅に低減できます。



標準的な部品寸法

製品概要

T_A = 25℃		標準値		単位
V_{DS}	ドレイン - ソース間電圧	12		V
Q_g	ゲートの合計電荷 (4.5V)	3.9		nC
Q_{gd}	ゲート電荷、ゲート - ドレイン間	0.39		nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	V_{GS} = 1.8V	26	mΩ
		V_{GS} = 2.5V	18	
		V_{GS} = 4.5V	15	
$V_{GS(th)}$	スレッショルド電圧	0.8		V

製品情報(1)

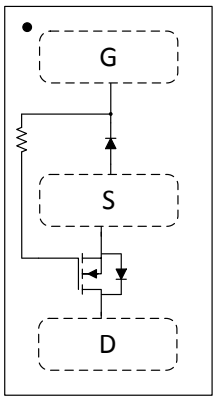
デバイス	数量	メディア	パッケージ	出荷形態
CSD13385F5	3000	7 インチ・リール	Femto 1.53mm × 0.77mm SMD リードレス	テープ・アンド・リール
CSD13385F5T	250			

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

絶対最大定格

T_A = 25℃		値	単位
V_{DS}	ドレイン - ソース間電圧	12	V
V_{GS}	ゲート - ソース間電圧	8	V
I_D	連続ドレイン電流(1)	4.3	A
	連続ドレイン電流(2)	7.1	
I_{DM}	パルス・ドレイン電流(1) (3)	41	A
P_D	消費電力(1)	0.5	W
	消費電力(2)	1.4	
$V_{(ESD)}$	人体モデル (HBM)	4	kV
	デバイス帯電モデル (CDM)	2	
T_J、T_{stg}	動作時の接合部温度、保存温度	–55～150	℃

(1) 最小 Cu、$R_{\theta JA}$ = 245℃/W (標準値)
(2) 最大 Cu、$R_{\theta JA}$ = 90℃/W (標準値)
(3) パルス幅 ≤ 100µs、デューティ・サイクル ≤ 1%



上面図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2017) to Revision B (February 2022) **Page**

- 超薄型の箇条書き項目を、高さ 0.35mm から 0.36mm に変更。.....1
- 超薄型の画像の高さを 0.35mm から 0.36mm に更新。.....1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....8
- Added FemtoFET Surface Mount Guide note.....9

Changes from Revision * (October 2016) to Revision A (May 2017) **Page**

- Changed I_{DSS} and $_{IGSS}$ unit value from µA to nA in the *Electrical Characteristics* table. 3

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.5	0.8	1.2	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 1.8 V, I_{DS} = 0.1 A		26	50	mΩ
		V_{GS} = 2.5 V, I_{DS} = 0.9 A		18	23	
		V_{GS} = 4.5 V, I_{DS} = 0.9 A		15	19	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_{DS} = 0.9 A		11.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		519	674	pF
C_{oss}	Output capacitance			305	396	pF
C_{rss}	Reverse transfer capacitance			29	38	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.9 A		3.9	5.0	nC
Q_{gd}	Gate charge gate-to-drain			0.39		nC
Q_{gs}	Gate charge gate-to-source			0.74		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.46		nC
Q_{oss}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		2.5		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.9 A, R_G = 2 Ω		7		ns
t_r	Rise time			10		ns
$t_{d(off)}$	Turnoff delay time			33		ns
t_f	Fall time			10		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.9 A, V_{GS} = 0 V		0.67	1.0	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		245		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

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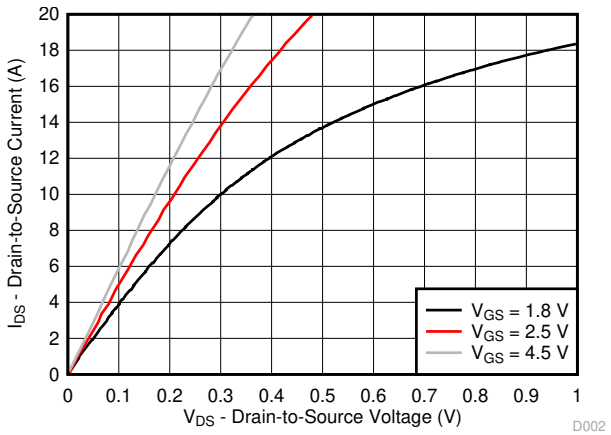
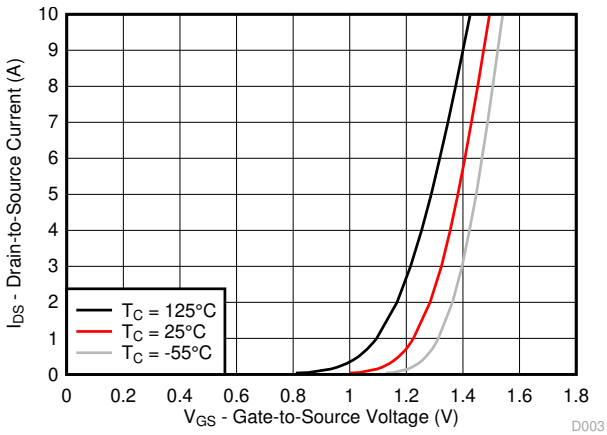


図 5-1. Saturation Characteristics



V_{DS} = 5 V

図 5-2. Transfer Characteristics

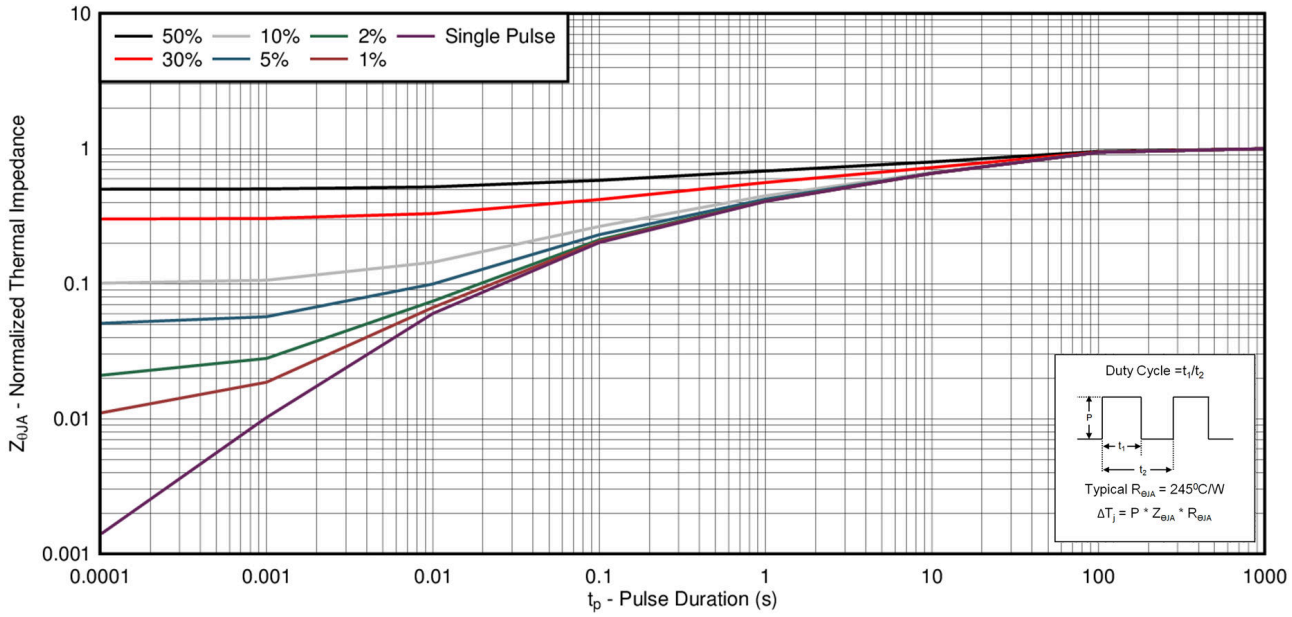
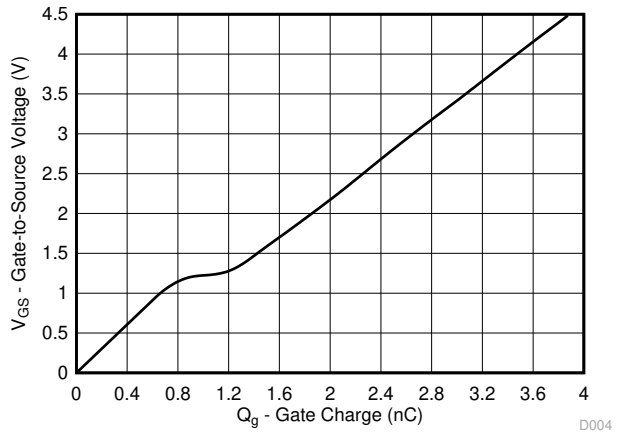


図 5-3. Transient Thermal Impedance

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I_D = 0.9 A V_{DS} = 6 V

図 5-4. Gate Charge

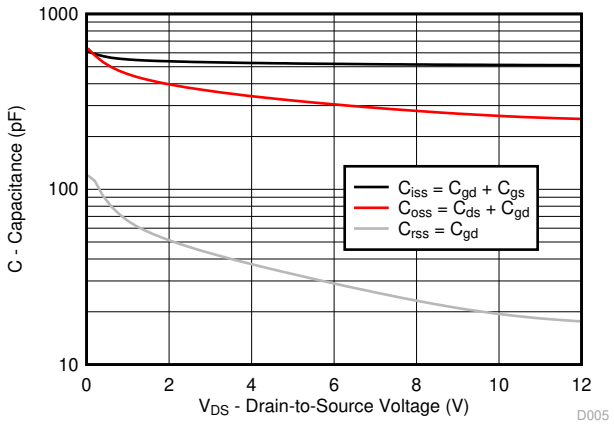
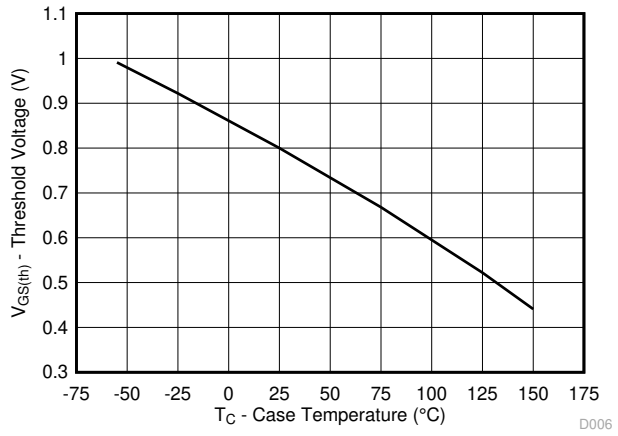


図 5-5. Capacitance



I_D = 250 µA

図 5-6. Threshold Voltage vs Temperature

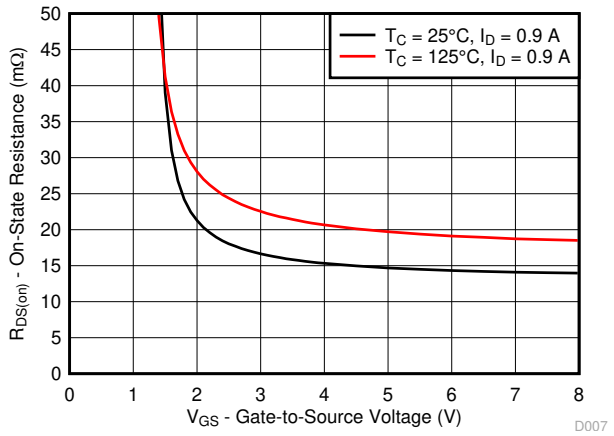
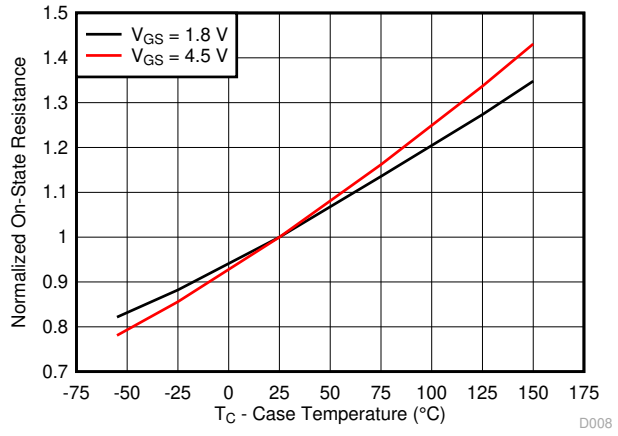


図 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 0.9 A

図 5-8. Normalized On-State Resistance vs Temperature

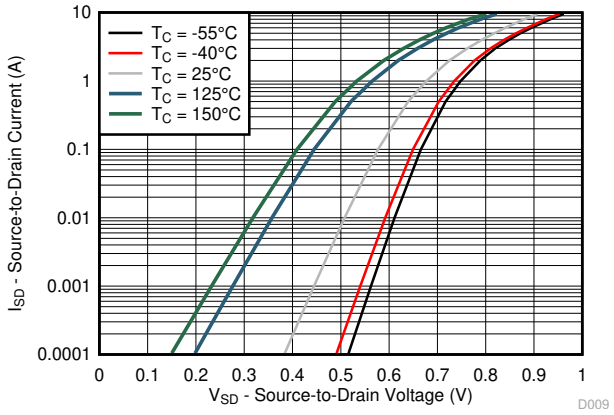
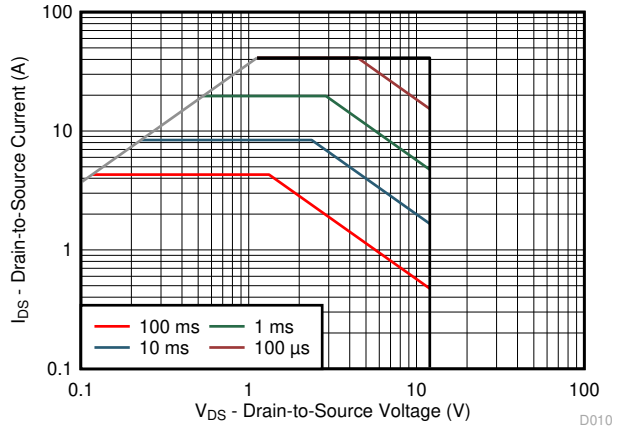


図 5-9. Typical Diode Forward Voltage

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Single pulse, typical $R_{\theta JA}$ = 290°C/W

図 5-10. Maximum Safe Operating Area (SOA)

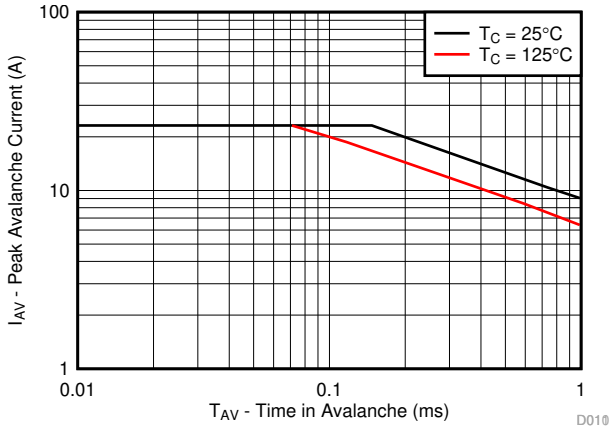
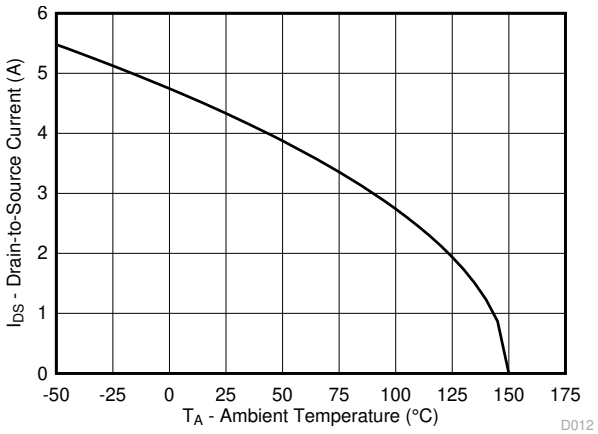


図 5-11. Single Pulse Unclamped Inductive Switching



Typical $R_{\theta JA}$ = 245°C/W

図 5-12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

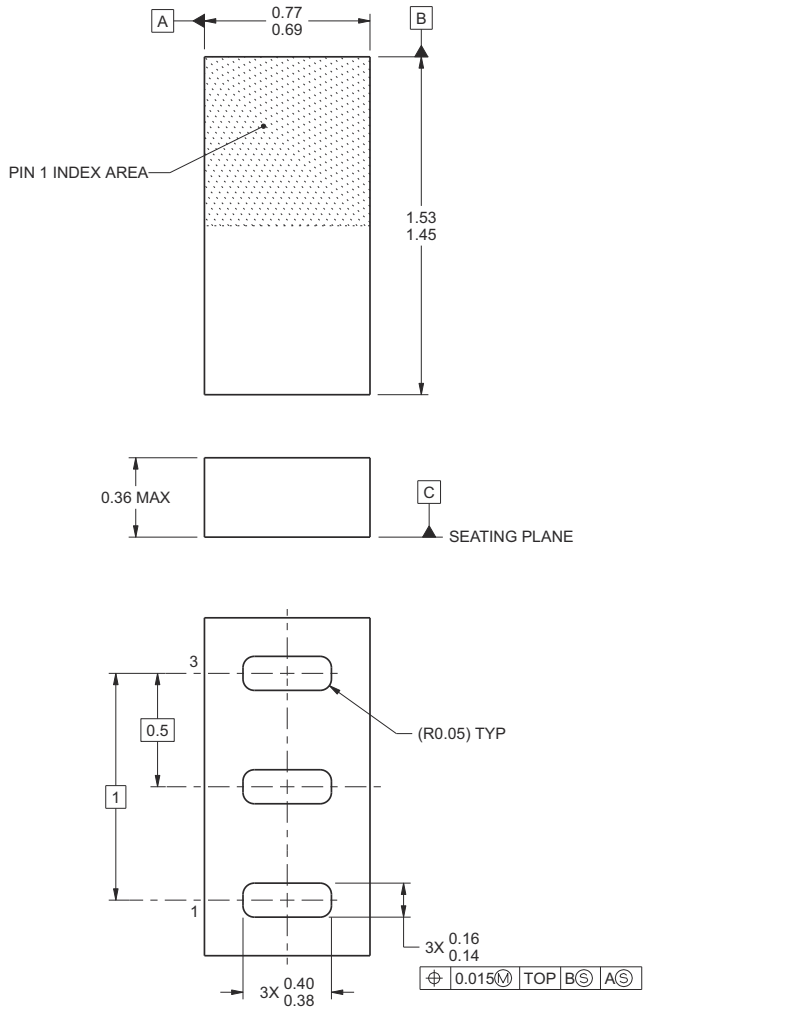
6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



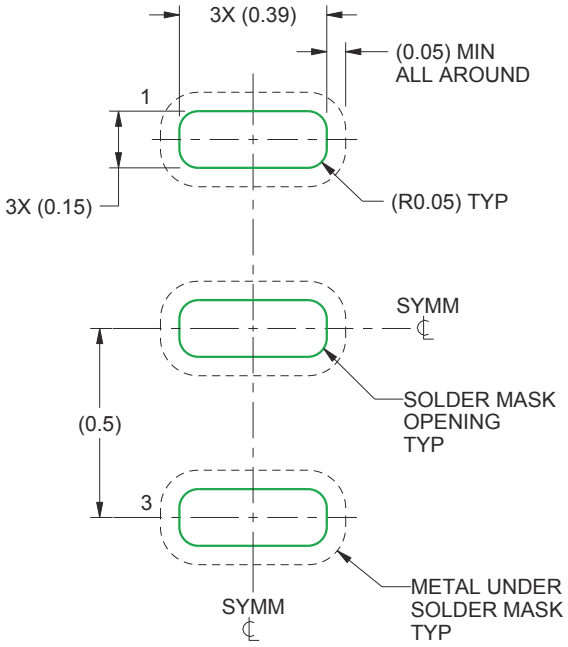
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

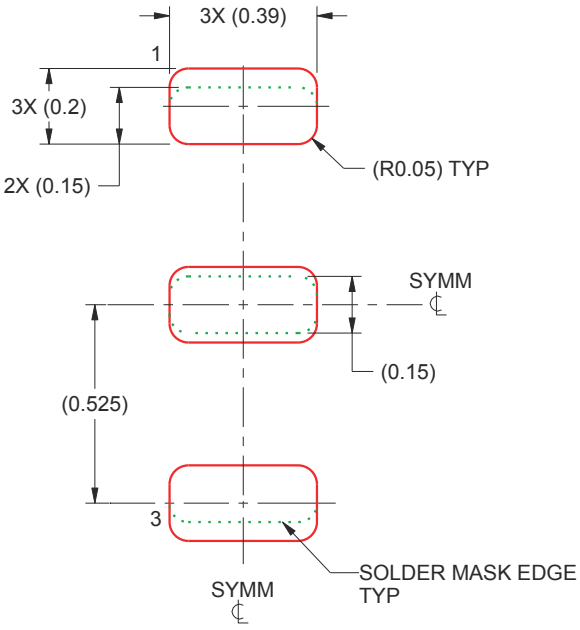
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7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13385F5	ACTIVE	PICOSTAR	YJK	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4V	Samples
CSD13385F5T	ACTIVE	PICOSTAR	YJK	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

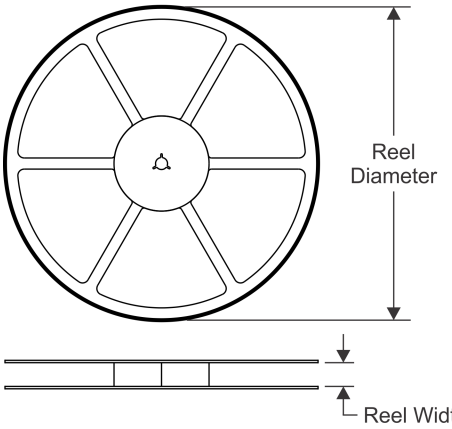
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

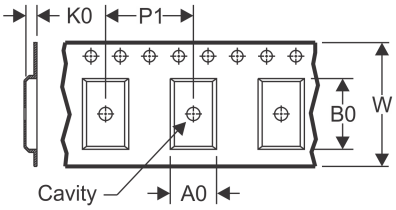
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

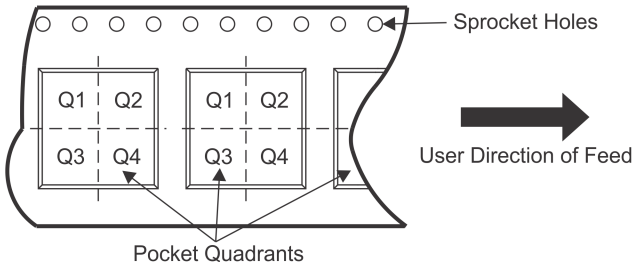


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

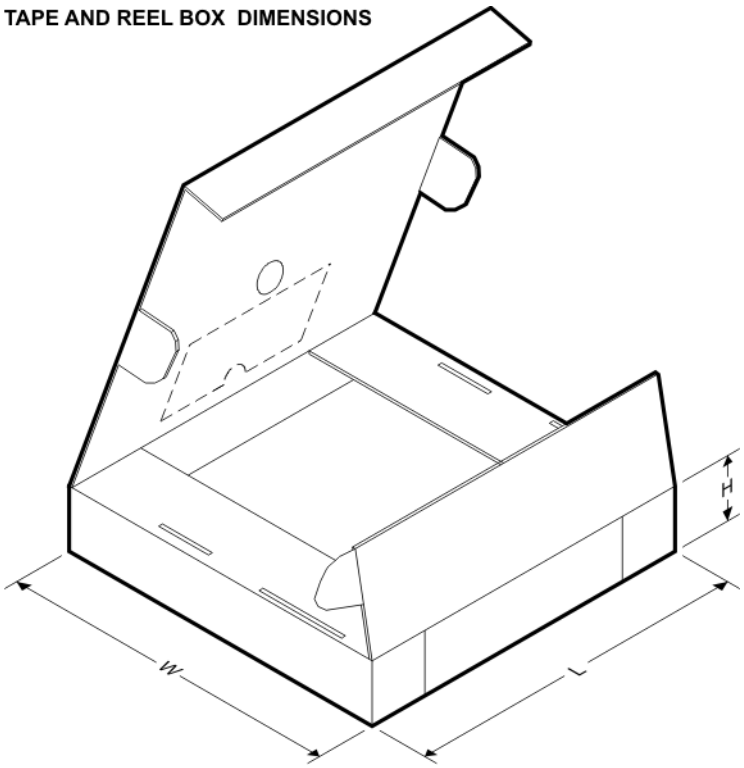
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

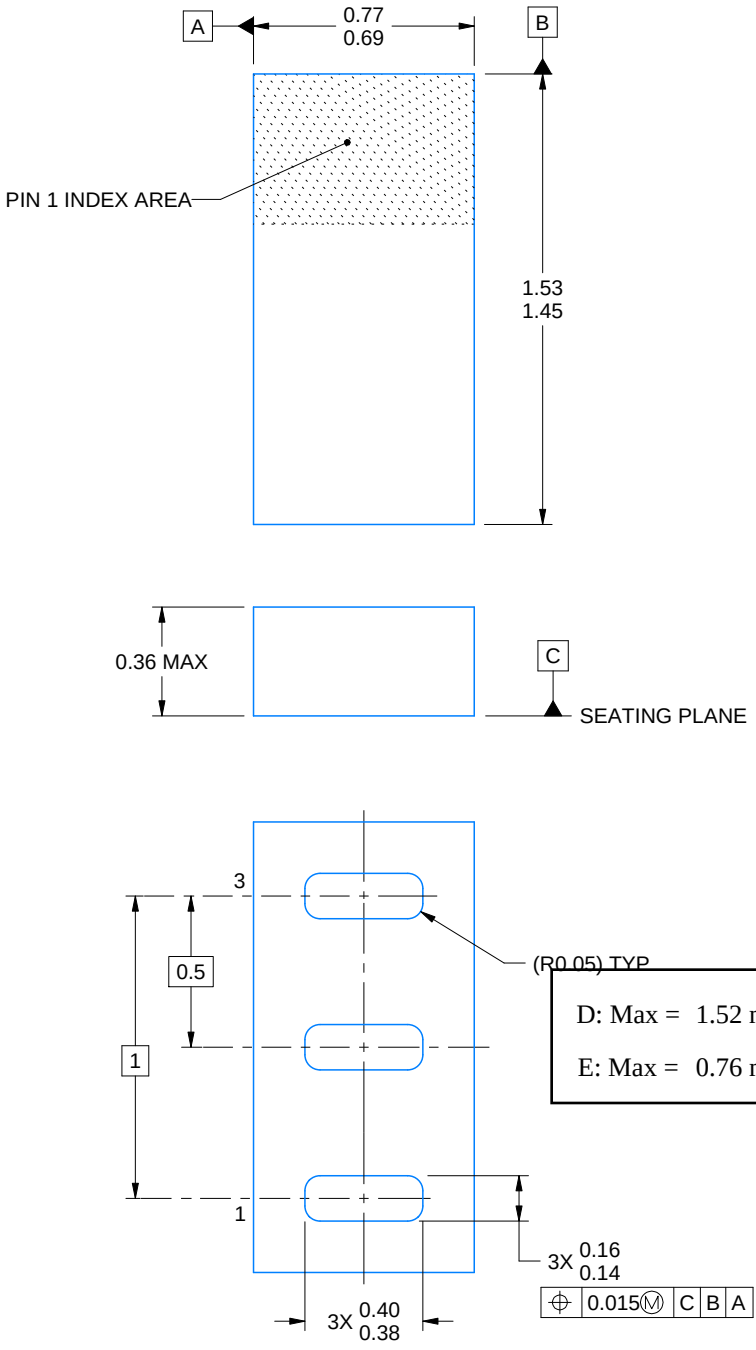
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13385F5	PICOSTAR	YJK	3	3000	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5T	PICOSTAR	YJK	3	250	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13385F5	PICOSTAR	YJK	3	3000	220.0	220.0	35.0
CSD13385F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD13385F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0
CSD13385F5T	PICOSTAR	YJK	3	250	220.0	220.0	35.0

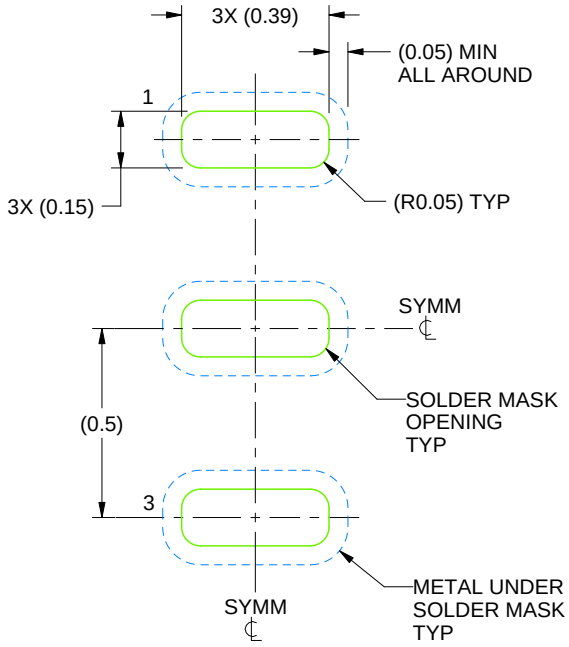


4222132/C 03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

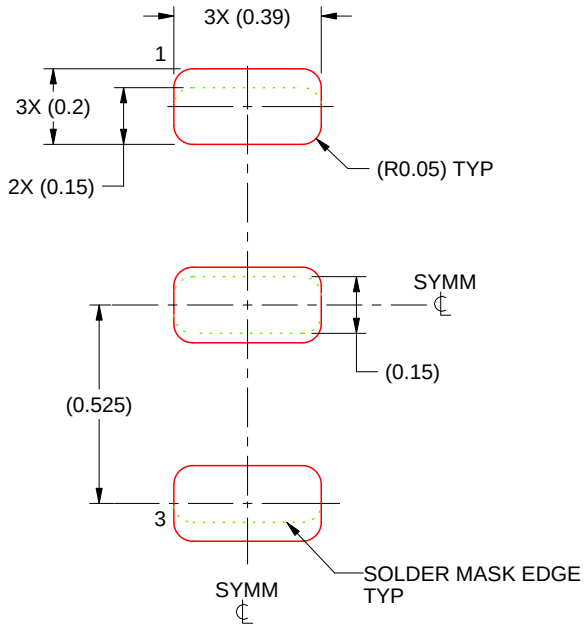


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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