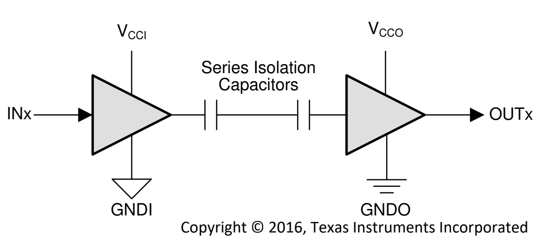
ISO652x 汎用、デュアルチャネル、機能的アイソレータ

1 特長

- デュアルチャネル、CMOS 出力機能的アイソレータ
- 50Mbps のデータ レート
- CMTI が ±150kV/μs (標準値) の堅牢な SiO_2 絶縁バリア
- 機能絶縁 (8-REU):
  - $200V_{RMS}$、$280V_{DC}$ の動作電圧
  - $570V_{RMS}$、$800V_{DC}$ の過渡電圧 (60s)
- 機能絶縁 (8-D):
  - $450V_{RMS}$、$637V_{DC}$ の動作電圧
  - $707V_{RMS}$、$1000V_{DC}$ の過渡電圧 (60s)
- 沿面距離 >2.2mm のコンパクトな 8-REU パッケージで供給
- 幅広い電源電圧範囲:1.71V～1.89V、2.25V～5.5V
- 1.71V から 5.5V への電圧変換
- デフォルト出力 HIGH (ISO652x) および LOW (ISO652xF) のオプション
- 幅広い温度範囲:-40℃～125℃
- チャネルごとに 1.8mA (標準値、3.3V、1Mbps 時)
- 小さい伝搬遅延:11ns (標準値、3.3V 時)
- 堅牢な電磁両立性 (EMC)
  - システム レベルでの ESD、EFT、サージ耐性
  - きわめて低い電磁放射
- Leadless-DFN (8-REU) パッケージおよび Narrow-SOIC (D-8) パッケージのオプション

2 アプリケーション

- 電源
- 電力網、電力量計
- モーター ドライブ
- ファクトリ オートメーション
- ビル オートメーション
- 照明器具
- 電化製品



V_{CCI}=入力電源、V_{CCO}=出力電源
GNDI=入力グランド、GNDO=出力グランド

概略回路図

3 概要

ISO652x デバイスは、安全ではないアプリケーション用の絶縁を必要とするが、コスト重視でスペースに制約があるようなアプリケーション向けに設計された、高性能なデュアル チャネルの機能的アイソレータです。この絶縁バリアは、$200V_{RMS}$ / $280V_{DC}$ の動作電圧と、$570V_{RMS}$ / $800V_{DC}$ の過渡電圧に対応しています。

デバイスは、CMOS または LVCMOS デジタル I/O を絶縁しながら、低消費電力で高い電磁気耐性と低い放射を実現します。各絶縁チャネルは、テキサス・インスツルメンツの二重容量性二酸化ケイ素 (SiO_2) 絶縁バリアで分離されたロジック入力および出力バッファを備えています。ISO6520 は 2 つの絶縁チャネルを備えており、どちらのチャネルも同一方向です。ISO6521 は 2 つの絶縁チャネルを備えており、各チャネルは別方向です。入力電力または入力信号が失われた場合のデフォルト出力は、接尾辞 F のないデバイスでは High、接尾辞 F のあるデバイスでは Low です。詳細は「デバイスの機能モード」のセクションを参照してください。

これらのデバイスにより、UART、SPI、RS-485、RS-232、CAN などのデータ バスのノイズ電流によって敏感な回路が損傷を受けることを防止できます。チップ設計およびレイアウト技法により、は電磁両立性が大幅に強化されているため、システム レベルの ESD および放射のコンプライアンスを容易に達成できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ISO6520、ISO6520F	DFN (8-REU)	3.0mm × 2.0mm
ISO6521、ISO6521F	DFN (8-REU)	3.0mm × 2.0mm
ISO6520、ISO6520F	D (8)	4.9mm × 6.0mm
ISO6521、ISO6521F	D (8)	4.9mm × 6.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

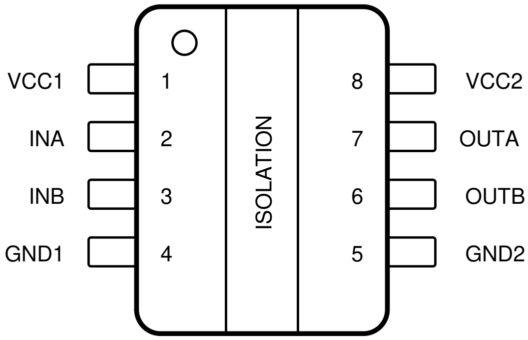

図 4-1. ISO6520 D Package 8-Pin SOIC Top View

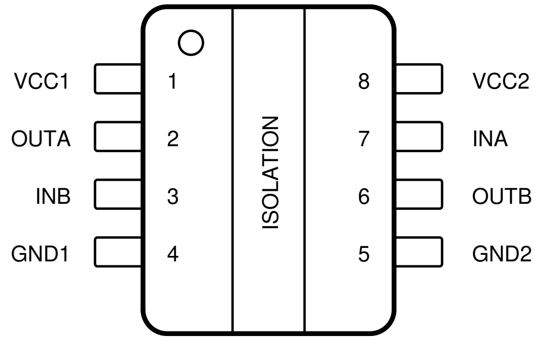

図 4-2. ISO6521 D Package 8-Pin SOIC Top View

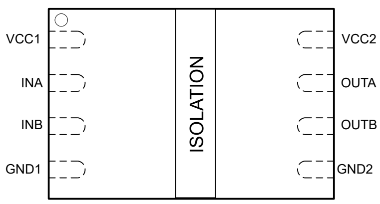

図 4-3. ISO6520 DFN Package 8-Pin REU Top View

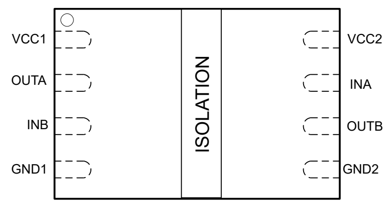

図 4-4. ISO6521 DFN Package 8-Pin REU Top View

表 4-1. Pin Functions

NAME	PIN		TYPE[(1)]	Description
	ISO6520	ISO6521		
GND1	4	4	-	Ground connection for V_{CC1}
GND2	5	5	-	Ground connection for V_{CC2}
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	P	Power supply, V_{CC1}
V_{CC2}	8	8	P	Power supply, V_{CC2}

(1) I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

See[(1)]

		MIN	MAX	UNIT
Supply Voltage [(2)]	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5 [(3)]	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5 [(3)]	
Output Current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C
Transient Isolation Voltage (REU-8)	AC Voltage, t=60s		570	V_{RMS}
	DC Voltage, t=60s		800	V_{DC}
Transient Isolation Voltage (SOIC-8)	AC Voltage, t=60s		707	V_{RMS}
	DC Voltage, t=60s		1000	V_{DC}

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC1} [(1)]	Supply Voltage Side 1	V_{CC} = 1.8 V [(3)]	1.71		1.89	V
V_{CC1} [(1)]	Supply Voltage Side 1	V_{CC} = 2.5 V to 5 V [(3)]	2.25		5.5	V
V_{CC2} [(1)]	Supply Voltage Side 2	V_{CC} = 1.8 V [(3)]	1.71		1.89	V
V_{CC2} [(1)]	Supply Voltage Side 2	V_{CC} = 2.5 V to 5 V [(3)]	2.25		5.5	V
V_{CC} (UVLO+)	UVLO threshold when supply voltage is rising			1.53	1.71	V
V_{CC} (UVLO-)	UVLO threshold when supply voltage is falling		1.1	1.41		V
Vhys (UVLO)	Supply voltage UVLO hysteresis		0.08	0.13		V
V_{IH}	High level Input voltage		0.7 x V_{CCI} [(2)]		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V

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		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{OH}	High level output current	V_{CCO} [(2)] = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
		V_{CCO} = 1.8 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
		V_{CCO} = 1.8 V			1	mA
DR	Data Rate		0		50	Mbps
T_A	Ambient temperature		-40	25	125	°C
V_{IOWM}	Functional Isolation Working Voltage (REU-8)	AC Voltage (sine wave)			200	V_{RMS}
		DC Voltage			280	V_{DC}
V_{IOWM}	Functional Isolation Working Voltage (SOIC-8)	AC Voltage (sine wave)			450	V_{RMS}
		DC Voltage			637	V_{DC}

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when 1.89 V < V_{CC1}, V_{CC2} < 2.25 V and 1.05 V < V_{CC1}, V_{CC2} < 1.71 V

5.4 Thermal Information

THERMAL METRIC [(1)]		ISO652x		UNIT
		DFN (REU-8)	D (SOIC-8)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.4	104.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.0	48.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.3	52.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.2	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.7	52.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Package Characteristics

PARAMETER		TEST CONDITIONS	VALUE	VALUE	UNIT
			8-REU	8-D	
CLR	External clearance[(1)]	Shortest pin to pin distance through air	>2.2	>4	mm
CPG	External creepage[(1)]	Shortest pin to pin distance across the package surface	>2.2	>4	mm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	>400	V
	Material Group	According to IEC 60664-1	II	II	
C_{IO}	Capacitance, input to output[(2)]	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	≅0.5	≅0.5	pF
R_{IO}	Resistance, input to output[(2)]	T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω

(1) Creepage and clearance requirements must be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to verify that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) All pins on each side of the barrier tied together creating a two-pin device.

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5.6 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See 図 6-1	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 6-1			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, V_{CM} = 700V ; See 図 6-3	100	150		kV/μs
C_i	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4\times\sin(2\pi ft)$, f = 2 MHz, V_{CC} = 5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to same side ground.

5.7 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6520							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1) (ISO6520), V_I = 0 V (ISO6520 with F suffix)		I_{CC1}		1.1	1.7	mA
			I_{CC2}		1.3	2.2	
	V_I = 0V (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)		I_{CC1}		3.2	4.6	
			I_{CC2}		1.4	2.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.1	3.1	
			I_{CC2}		1.5	2.4	
		10 Mbps	I_{CC1}		2.2	3.2	
			I_{CC2}		2.7	3.6	
		50 Mbps	I_{CC1}		2.5	3.6	
			I_{CC2}		7.9	9.5	
ISO6521							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1) (ISO6521); V_I = 0 V (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		1.2	2.2	mA
	V_I = 0 V (ISO6521); $V_I = V_{CCI}$ (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		2.3	3.5	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.9	2.9	
		10 Mbps	I_{CC1}, I_{CC2}		2.5	3.6	
		50 Mbps	I_{CC1}, I_{CC2}		5.2	6.7	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.8 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA; See 図 6-1	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; See 図 6-1			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, V_{CM} = 700V ; See 図 6-3	100	150		kV/μs
C_i	Input Capacitance(2)	$V_I = V_{CC}$/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 3.3 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to same side ground.

5.9 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6520							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1) (ISO6520), V_I = 0 V (ISO6520 with F suffix)		I_{CC1}		1.1	1.6	mA
			I_{CC2}		1.3	2.2	mA
	V_I = 0V (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)		I_{CC1}		3.2	4.5	mA
			I_{CC2}		1.4	2.3	mA
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.1	3.1	mA
			I_{CC2}		1.4	2.3	mA
		10 Mbps	I_{CC1}		2.2	3.1	mA
			I_{CC2}		2.3	3.2	mA
		50 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		6	7.3	mA
ISO6521							
Supply current - DC signal (2)	$V_I = V_{CCI}$ (1) (ISO6521); V_I = 0 V (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		1.2	2.2	mA
	V_I = 0 V (ISO6521); $V_I = V_{CCI}$ (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		2.3	3.5	mA
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.8	2.9	mA
		10 Mbps	I_{CC1}, I_{CC2}		2.3	3.4	mA
		50 Mbps	I_{CC1}, I_{CC2}		4.2	5.5	mA

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.10 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; See 図 6-1	V_{CCO} - 0.1			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; See 図 6-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			μA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 700V ; See 図 6-3	100	150		kV/μs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 2.5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to same side ground.

5.11 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6520							
Supply current - DC signal (2)	V_I = V_{CCI} (1) (ISO6520), V_I = 0 V (ISO6520 with F suffix)		I_{CC1}		1.1	1.6	mA
			I_{CC2}		1.3	2.1	
	V_I = 0V (ISO6520), V_I = V_{CC1} (ISO6520 with F suffix)		I_{CC1}		3.1	4.5	
			I_{CC2}		1.4	2.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.1	3.1	
			I_{CC2}		1.4	2.3	
		10 Mbps	I_{CC1}		2.1	3.1	
			I_{CC2}		2	2.9	
		50 Mbps	I_{CC1}		2.3	3.3	
			I_{CC2}		4.8	6	
ISO6521							
Supply current - DC signal (2)	V_I = V_{CCI} (1) (ISO6521); V_I = 0 V (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		1.2	2.2	mA
	V_I = 0 V (ISO6521); V_I = V_{CCI} (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		2.3	3.5	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.8	2.9	
		10 Mbps	I_{CC1}, I_{CC2}		2.1	3.2	
		50 Mbps	I_{CC1}, I_{CC2}		3.6	4.9	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.12 Electrical Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA; See 図 6-1	V_{CCO} - 0.1			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; See 図 6-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			μA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 700V ; See 図 6-3	100	150		kV/μs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 1.8 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to same side ground.

5.13 Supply Current Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6520							
Supply current - DC signal (2)	V_I = V_{CCI} (1) (ISO6520), V_I = 0 V (ISO6520 with F suffix)		I_{CC1}		0.8	1.5	mA
			I_{CC2}		1.2	2.1	
	V_I = 0V (ISO6520), V_I = V_{CC1} (ISO6520 with F suffix)		I_{CC1}		2.8	4.3	
			I_{CC2}		1.3	2.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.8	2.9	
			I_{CC2}		1.3	2.3	
		10 Mbps	I_{CC1}		1.8	2.9	
			I_{CC2}		1.8	2.7	
		50 Mbps	I_{CC1}		2	3.1	
			I_{CC2}		3.8	4.9	
ISO6521							
Supply current - DC signal (2)	V_I = V_{CCI} (1) (ISO6521); V_I = 0 V (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		1.1	2.1	mA
	V_I = 0 V (ISO6521); V_I = V_{CCI} (ISO6521 with F suffix)		I_{CC1}, I_{CC2}		2.1	3.4	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.7	
		10 Mbps	I_{CC1}, I_{CC2}		1.9	3	
		50 Mbps	I_{CC1}, I_{CC2}		3	4.2	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

5.14 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1		11	18	ns
$t_{P(dft)}$	Propagation delay drift			8		ps/℃
t_{UI}	Minimum pulse width	See 図 6-1	20			ns
PWD	Pulse width distortion[(1)] $\lvert t_{PHL} - t_{PLH}\rvert$	See 図 6-1		0.2	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time [(2)]	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time [(3)]				6	ns
t_r	Output signal rise time	See 図 6-1		2.6	4.5	ns
t_f	Output signal fall time			2.6	4.5	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.2V. See 図 6-2		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.15 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1		11	18	ns
$t_{P(dft)}$	Propagation delay drift			9.2		ps/℃
t_{UI}	Minimum pulse width	See 図 6-1	20			ns
PWD	Pulse width distortion[(1)] $\lvert t_{PHL} - t_{PLH}\rvert$	See 図 6-1		0.5	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time [(2)]	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time [(3)]				6	ns
t_r	Output signal rise time	See 図 6-1		1.6	3.2	ns
t_f	Output signal fall time			1.6	3.2	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.2V. See 図 6-2		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.16 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1		12	20.5	ns
$t_{P(dft)}$	Propagation delay drift			14.3		ps/°C
t_{UI}	Minimum pulse width	See 図 6-1	20			ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See 図 6-1		0.6	7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time(3)				6.1	ns
t_r	Output signal rise time	See 図 6-1		2	4	ns
t_f	Output signal fall time			2	4	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.2V. See 図 6-2		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

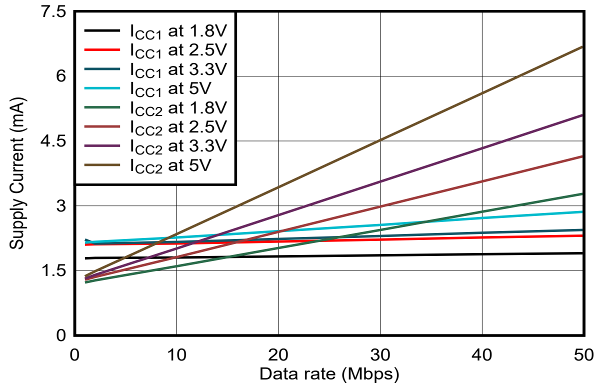
5.17 Switching Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2}$ = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1		15	25.1	ns
$t_{P(dft)}$	Propagation delay drift			15.2		ps/°C
t_{UI}	Minimum pulse width	See Figure 7-1	20			ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 7-1		0.7	8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time(3)				8.8	ns
t_r	Output signal rise time	See Figure 7-1		2.7	5.3	ns
t_f	Output signal fall time			2.7	5.3	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.2V. See 図 6-2		0.1	0.3	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

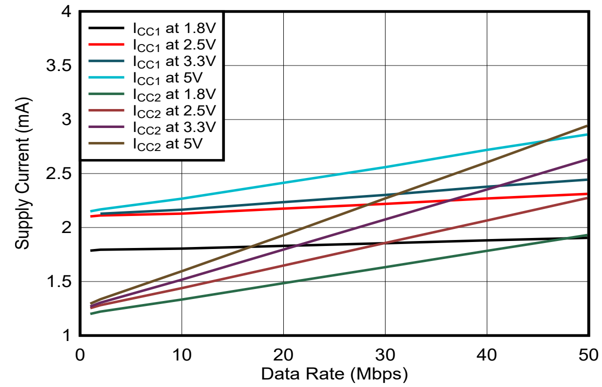
(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Typical Characteristics



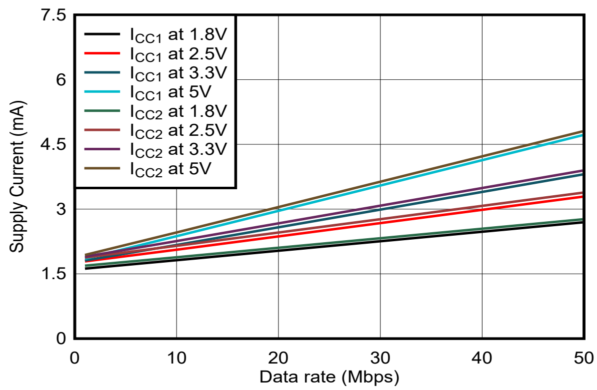
T_A = 25°C C_L = 15 pF

図 5-1. ISO6520 Supply Current vs Data Rate (With 15-pF Load)



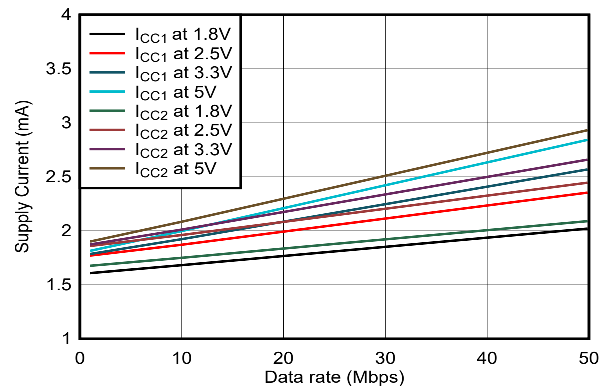
T_A = 25°C C_L = 15 pF

図 5-2. ISO6520 Supply Current vs Data Rate (With No Load)



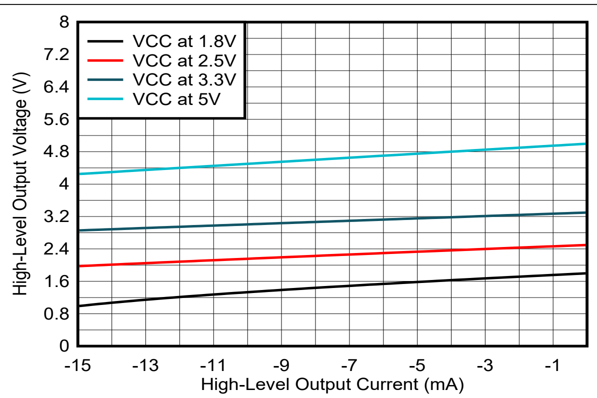
T_A = 25°C C_L = 15 pF

図 5-3. ISO6521 Supply Current vs Data Rate (With 15-pF Load)



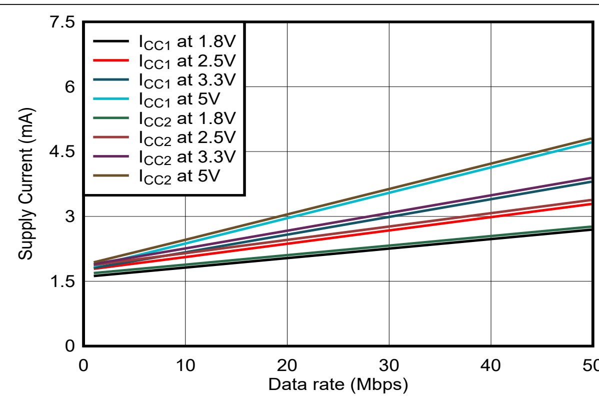
T_A = 25°C C_L = No Load

図 5-4. ISO6521 Supply Current vs Data Rate (With No Load)



T_A = 25°C

図 5-5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

図 5-6. Low-Level Output Voltage vs Low-Level Output Current

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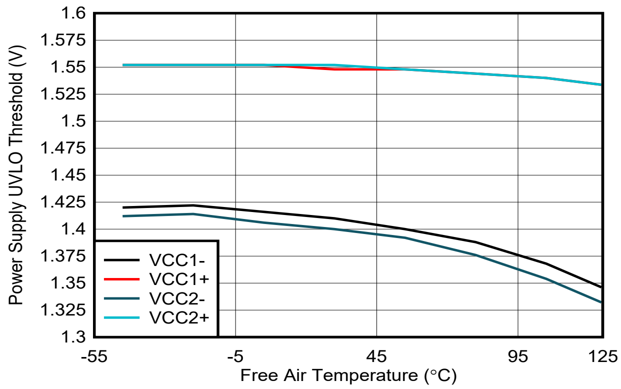


図 5-7. Power Supply Undervoltage Threshold vs Free-Air Temperature

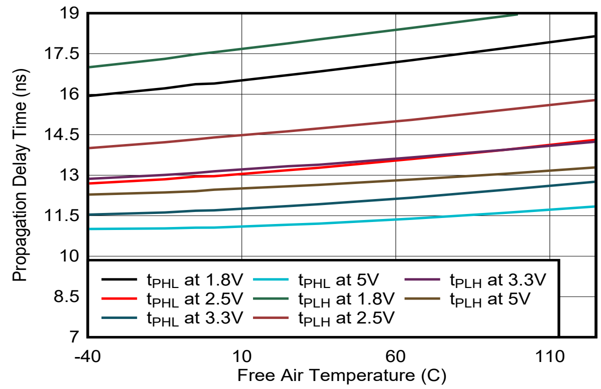
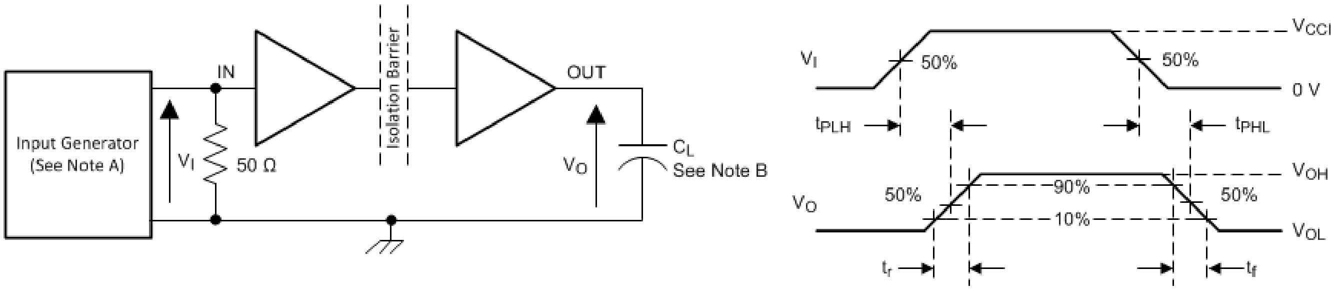


図 5-8. Propagation Delay Time vs Free-Air Temperature

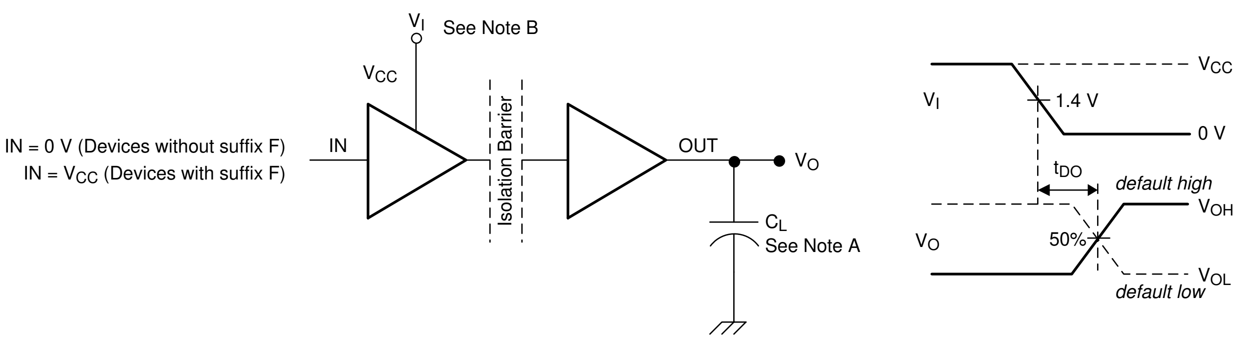
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω resistor is not needed in the actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

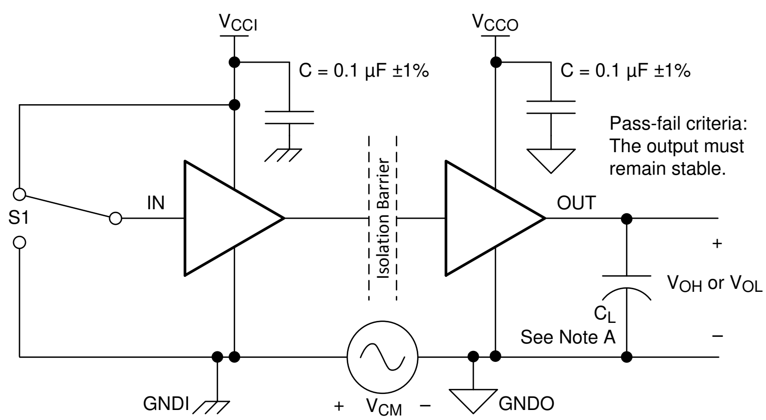
図 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

図 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-3. Common-Mode Transient Immunity Test Circuit

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7 Detailed Description

7.1 Overview

The ISO652x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

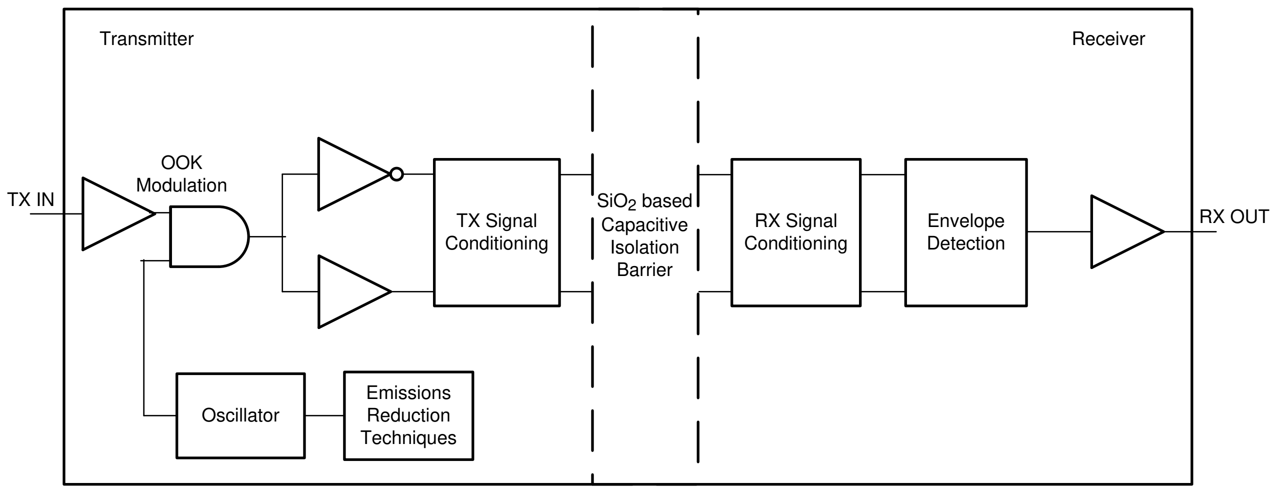

図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 7-2 shows a conceptual detail of how the OOK scheme works.

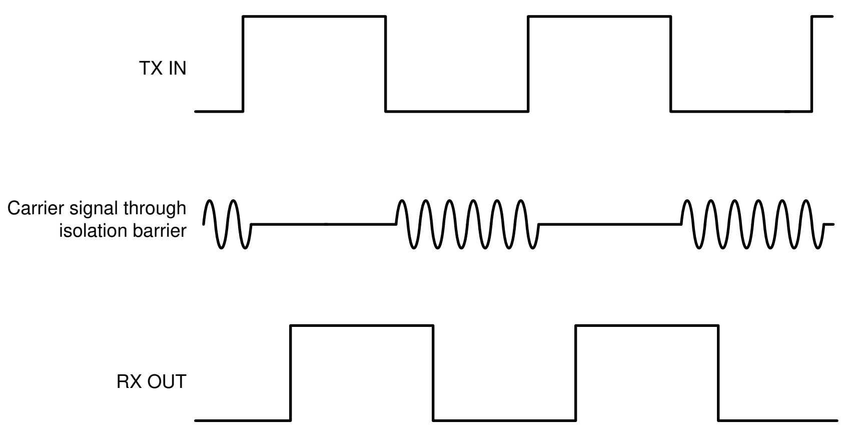

図 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

family of devices is available in two channel configurations and default output state options to enable a variety of application uses. lists the device features of the devices.

表 7-1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE
ISO6520	50 Mbps	2 Forward, 0 Reverse	High	REU-8
ISO6520F	50 Mbps	2 Forward, 0 Reverse	Low	REU-8
ISO6521	50 Mbps	1 Forward, 1 Reverse	High	REU-8
ISO6521F	50 Mbps	1 Forward, 1 Reverse	Low	REU-8

7.4 Device Functional Modes

表 7-2 lists the functional modes for the devices.

表 7-2. Function Table

<table>
<tr><th>V_{CCI} (1)</th><th>V_{CCO}</th><th>INPUT (INx)(2)</th><th>OUTPUT (OUTx)</th><th>COMMENTS</th></tr>
<tr><td rowspan="3">PU</td><td rowspan="3">PU</td><td>H</td><td>H</td><td rowspan="2">Normal Operation: A channel output assumes the logic state of the input.</td></tr>
<tr><td>L</td><td>L</td></tr>
<tr><td>Open</td><td>Default</td><td>Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is High for and Low for with F suffix.</td></tr>
<tr><td>PD</td><td>PU</td><td>X</td><td>Default</td><td>Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is High for and Low for with F suffix.
When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.
When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.</td></tr>
<tr><td>X</td><td>PD</td><td>X</td><td>Undetermined</td><td>When V_{CCO} is unpowered, a channel output is undetermined(3).
When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input</td></tr>
</table>

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq 1.71V$); PD = Powered down ($V_{CC} \leq 1.05$ V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.89 V < V_{CCI}, V_{CCO} < 2.25 V and 1.05 V < V_{CCI}, V_{CCO} < 1.71 V

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7.4.1 Device I/O Schematics

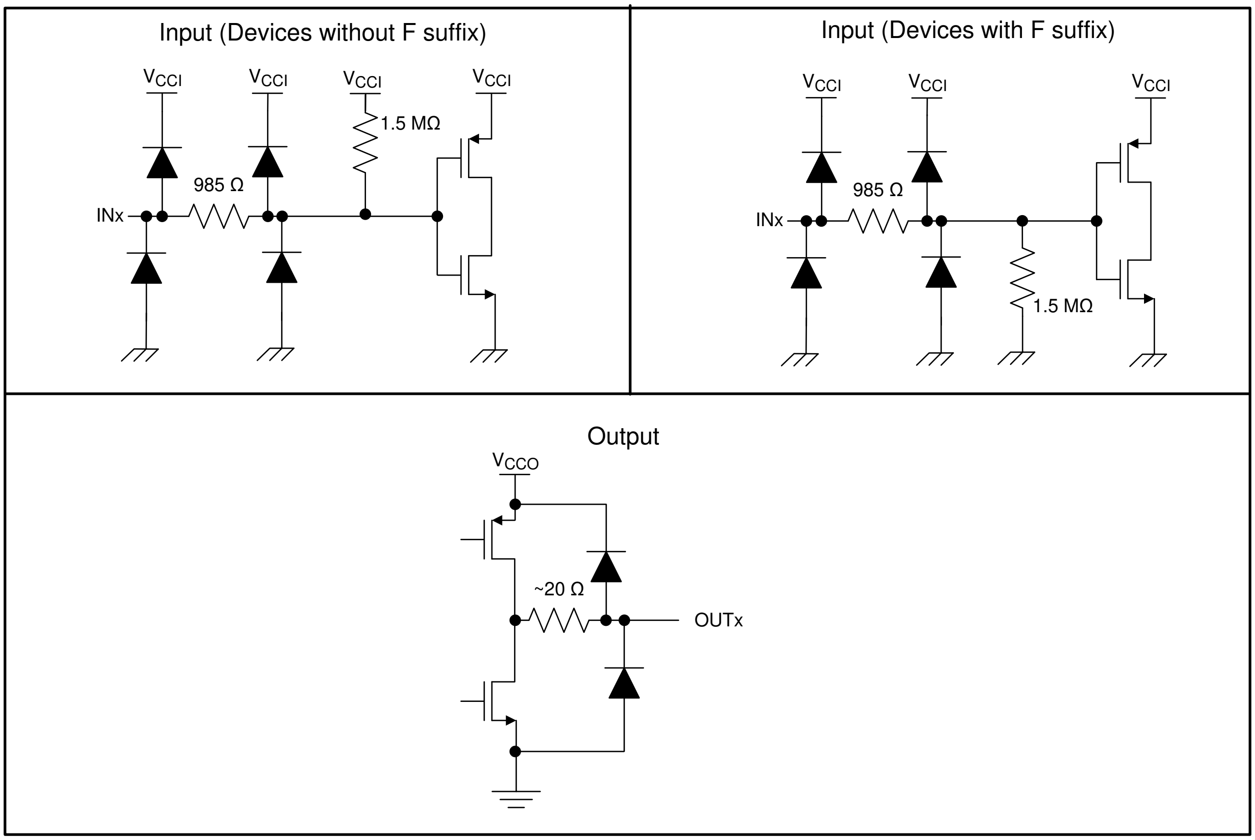

図 7-3. Device I/O Schematics

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO652x devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within the recommended operating conditions. As an example, supplying V_{CC1} with 3.3 V (which is within 1.71 V to 1.89 V and 2.25 V to 5 V) and V_{CC2} with 5 V (which is also within 1.71 V to 1.89 V and 2.25 V to 5 V) is possible. The digital isolator can be used as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

注

ISO652x is a functional isolator, and is not certified for isolation by standard bodies. For applications that require certified isolation by standard bodies, customers must choose ISO672x, ISO772x or ISO782x families of digital isolators.

8.2 Typical Application

ISO652x can be used with Texas Instruments' mixed signal microcontroller, voltage regulator and GaN with integrated drivers in several power supply designs. ISO652x helps isolate high voltage power MOSFETs from sensitive logic control circuitry.

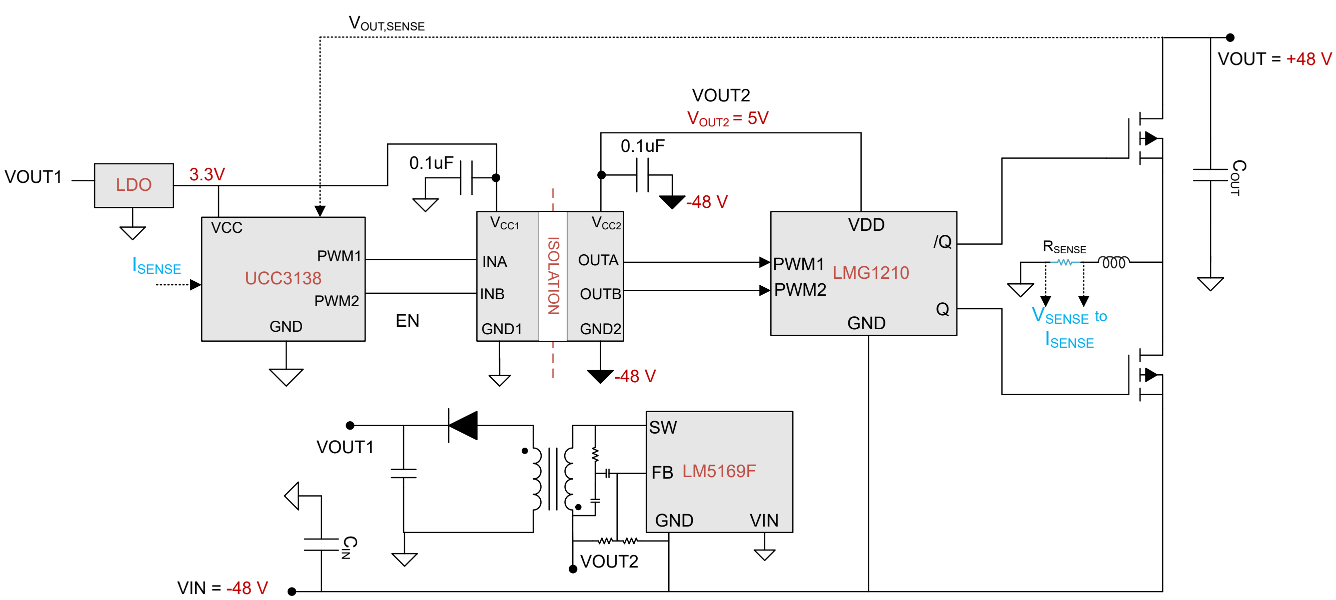

図 8-1. ISO6520 for Level shifting PWM signals from controller referenced to Ground to the FET driver in an Inverted Buck Boost Topology

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8.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μF
Decoupling capacitor from V_{CC2} and GND2	0.1 μF

9 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Drivers for Isolated Power Supplies* or *SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies*.

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used. Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Bypass the VCC pin to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 μF when using a ceramic capacitor with an X5R- or X7R-rated dielectric. The capacitor must be placed as close to the VCC pin as possible in the PCB layout and on the same layer. The capacitor must have a voltage rating greater than the VCC voltage level.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

10.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

10.2 Layout Example

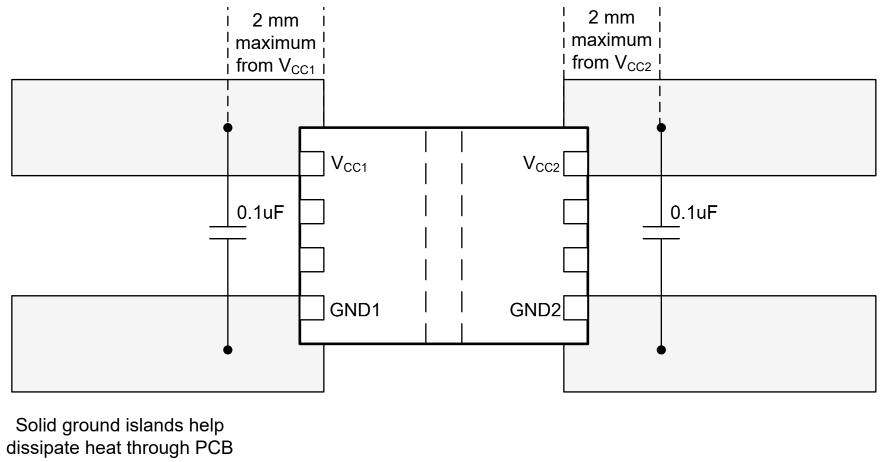

図 10-1. Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *SN6505x Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*, data sheet
- Texas Instruments, *SN6507 Low-Emissions, 36-V Push-Pull Transformer Driver with Duty Cyle Control for Isolated Power Supplies*, data sheet
- Texas Instruments, *LMG341xR070 600-V 70-mΩ GaN with Integrated Driver and Protection*, data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Trademarks

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11.5 静電気放電に関する注意事項

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2023) to Revision B (April 2024) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新。 ... 1
- ドキュメント全体を通して ISO6521F バリアントの情報を追加 ... 1

Changes from Revision * (August 2023) to Revision A (December 2023) — **Page**

- デバイスのステータスを「量産データ」に更新 ... 1
- Updated Typical Application Diagram ... 18

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO6520DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520	Samples
ISO6520FDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F	Samples
ISO6520FREUR	ACTIVE	VSON	REU	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F	Samples
ISO6520REUR	ACTIVE	VSON	REU	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520	Samples
ISO6521DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521	Samples
ISO6521FDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F	Samples
ISO6521FREUR	ACTIVE	VSON	REU	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F	Samples
ISO6521REUR	ACTIVE	VSON	REU	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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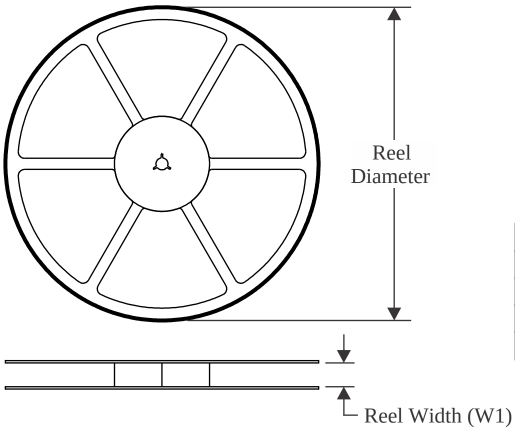
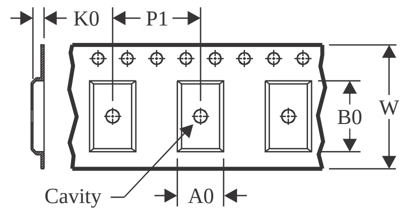
TAPE AND REEL INFORMATION

REEL DIMENSIONS

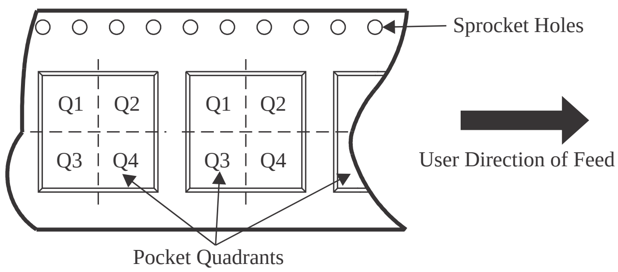


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

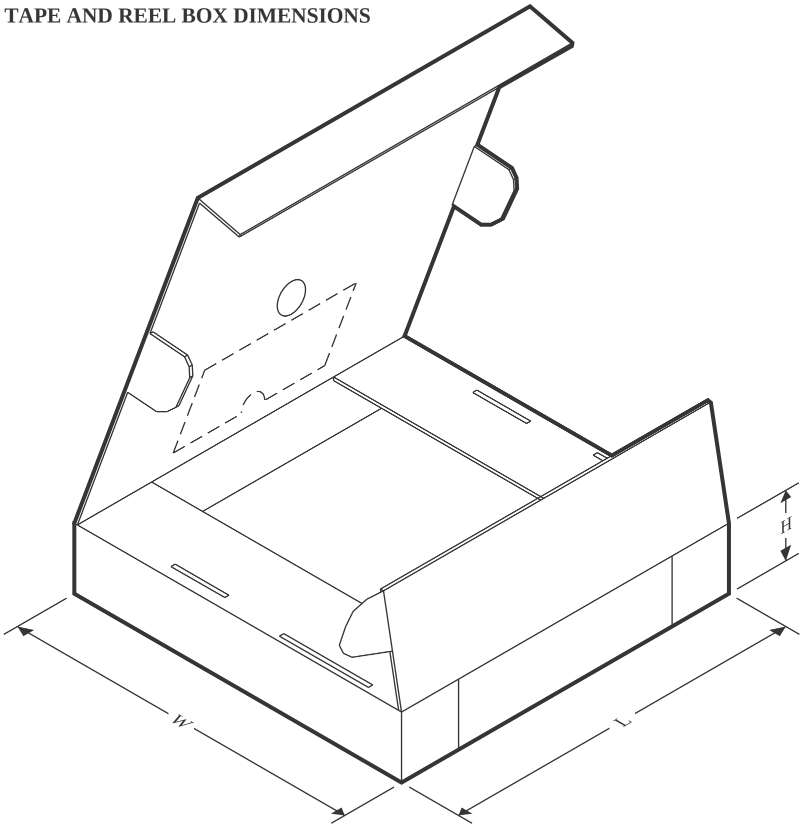
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

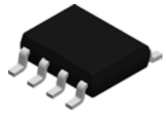
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6520DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6520FDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6520FREUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2
ISO6520REUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2
ISO6521DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6521FDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6521REUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

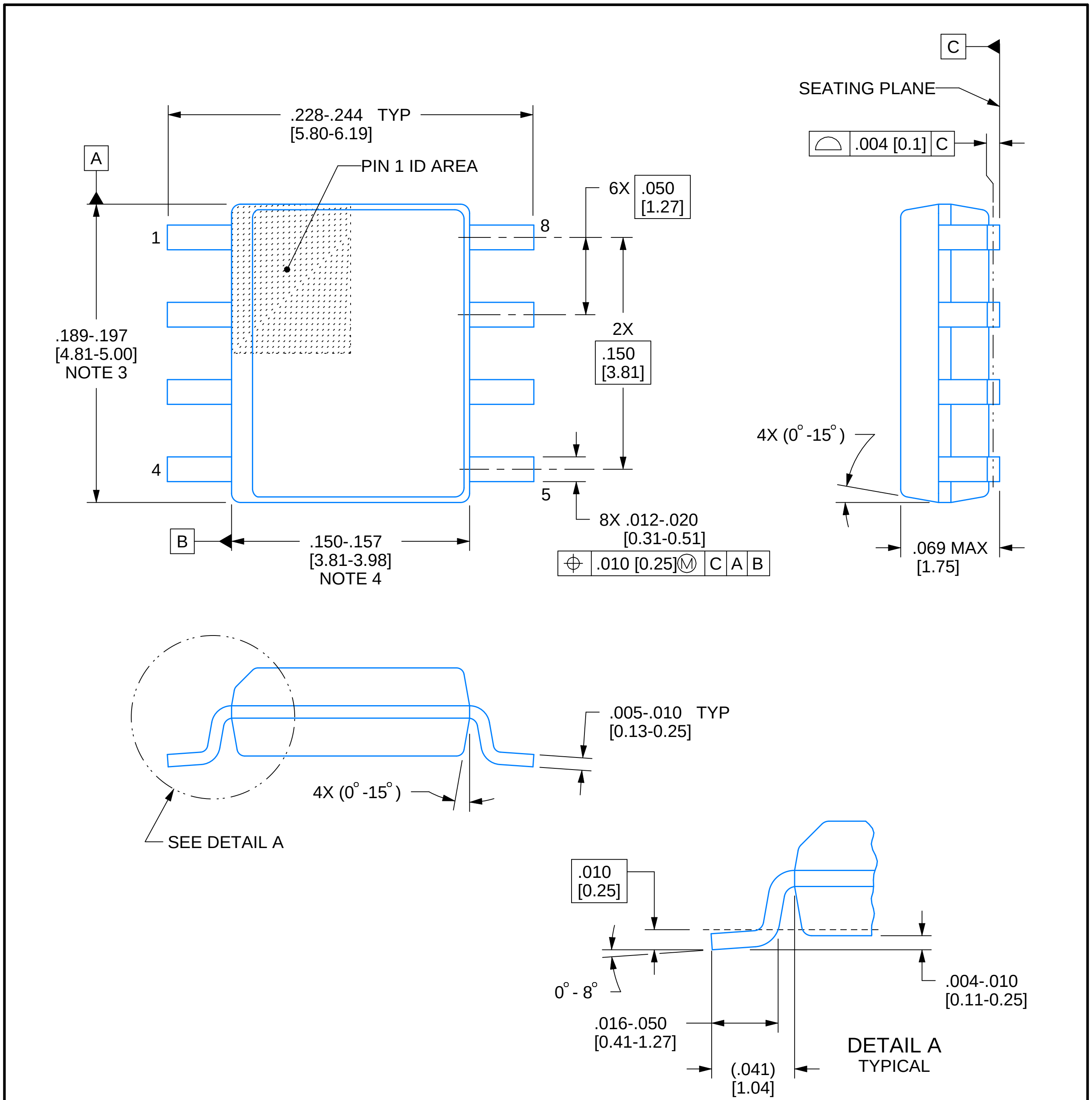
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6520DR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6520FDR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6520FREUR	VSON	REU	8	3000	210.0	185.0	35.0
ISO6520REUR	VSON	REU	8	3000	210.0	185.0	35.0
ISO6521DR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6521FDR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6521REUR	VSON	REU	8	3000	210.0	185.0	35.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

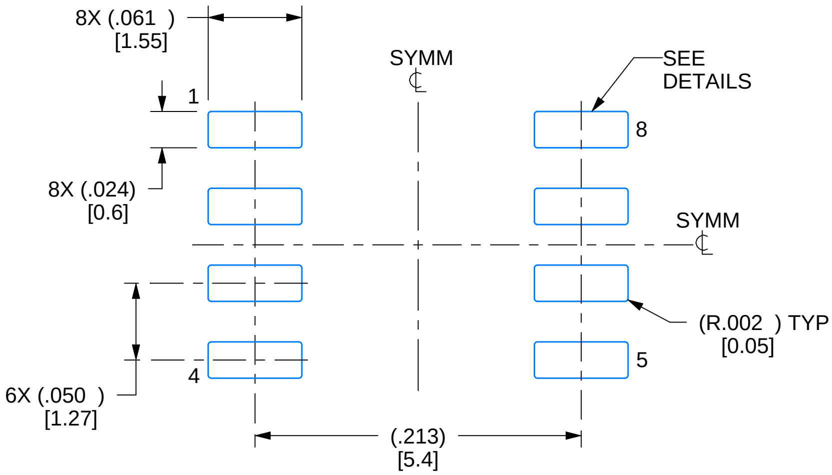
SMALL OUTLINE INTEGRATED CIRCUIT



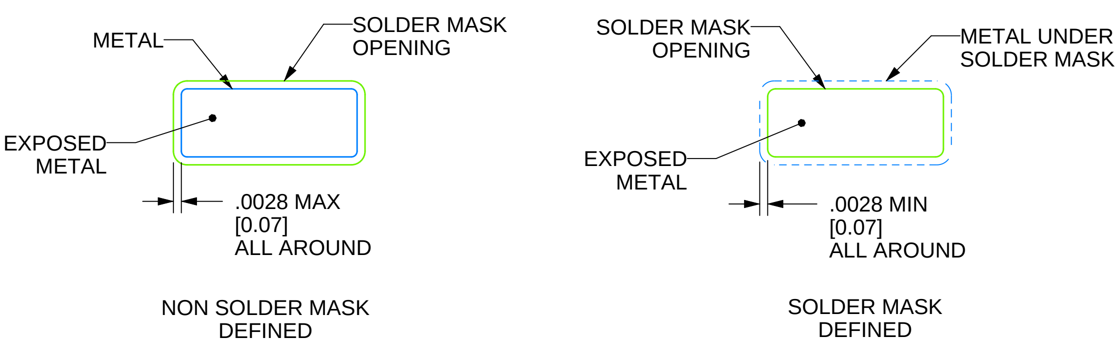
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

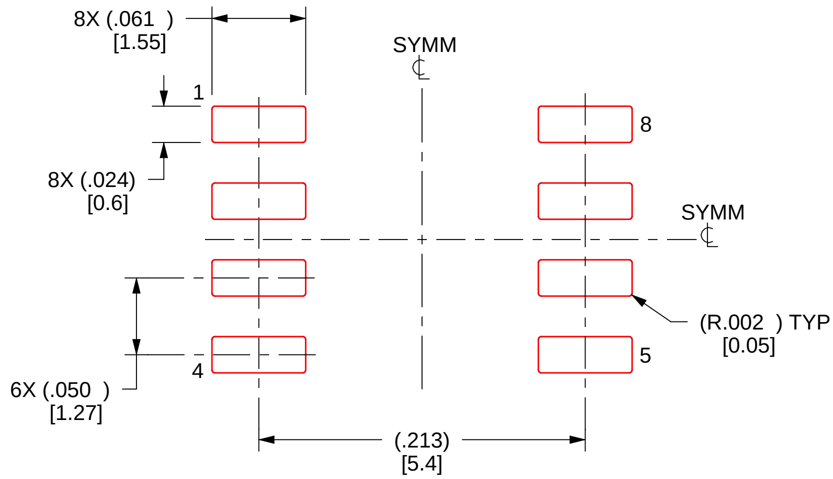


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

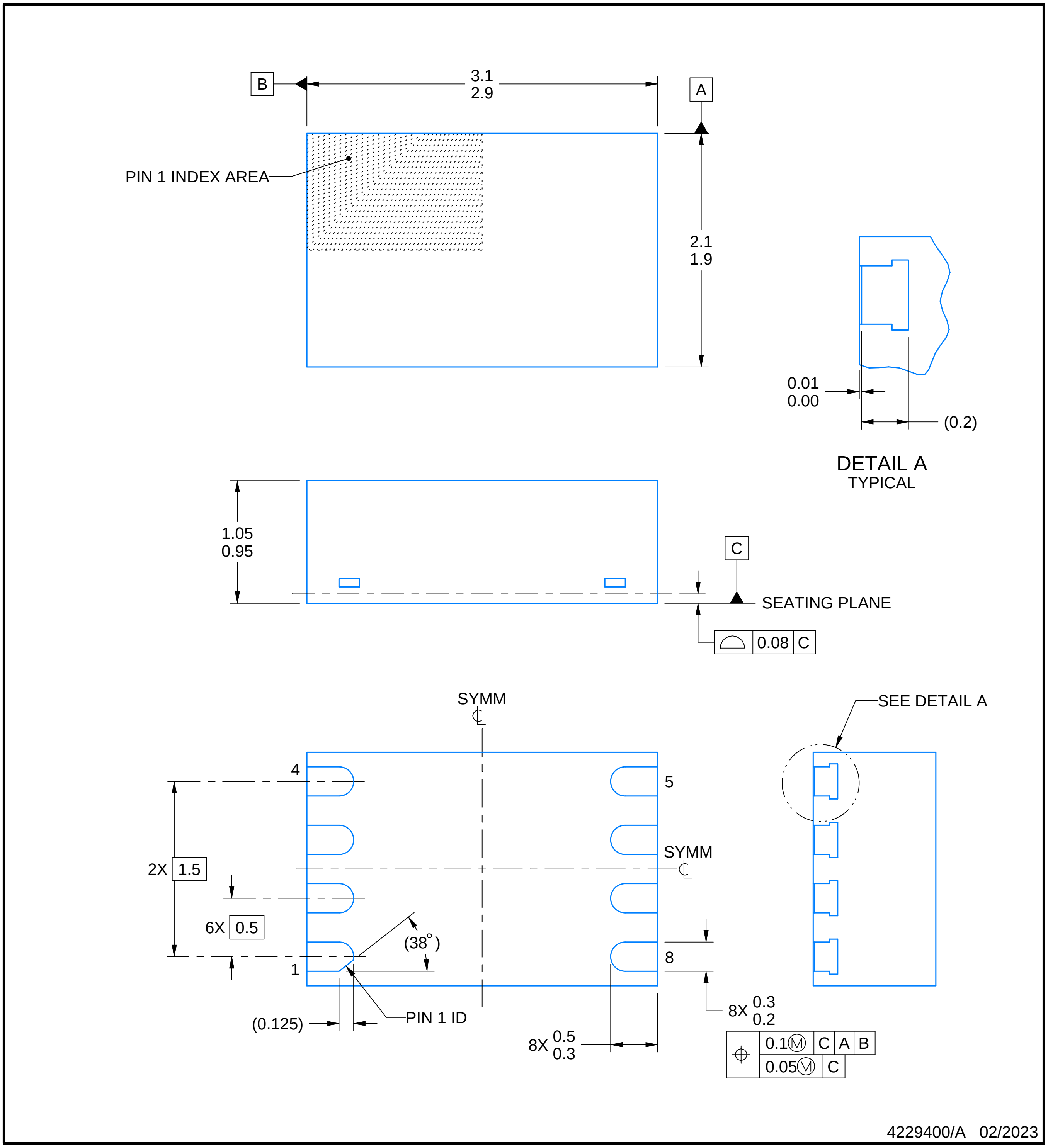


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

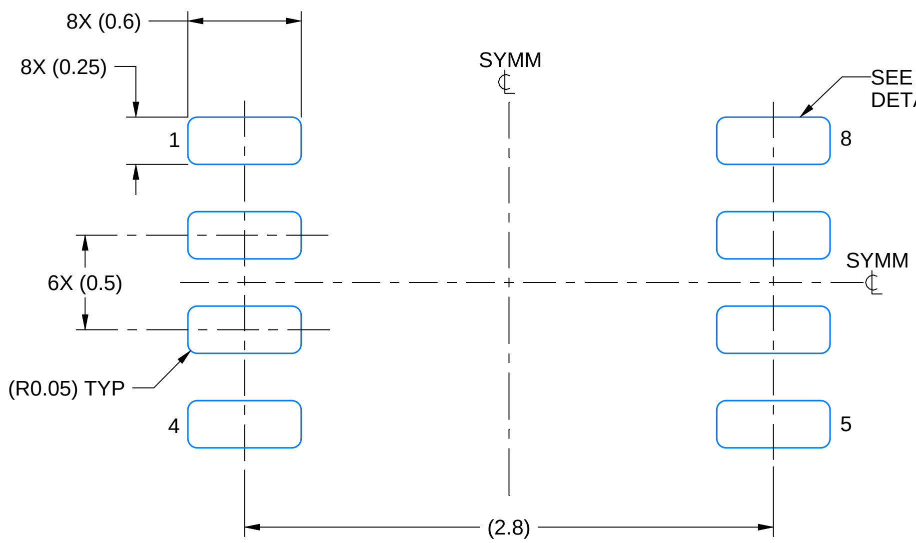
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

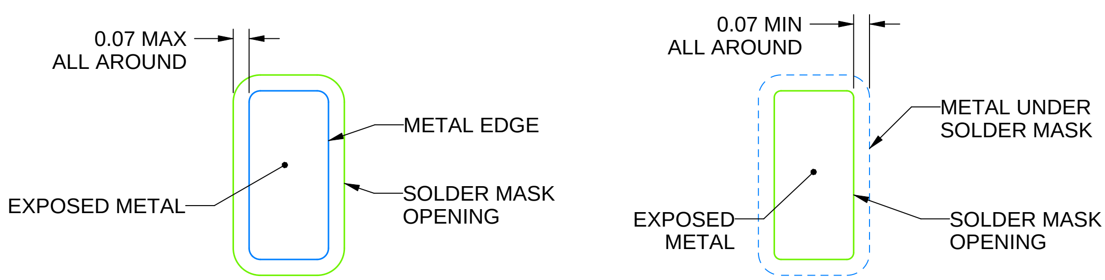


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON SOLDER MASK DEFINED
(PREFERRED)

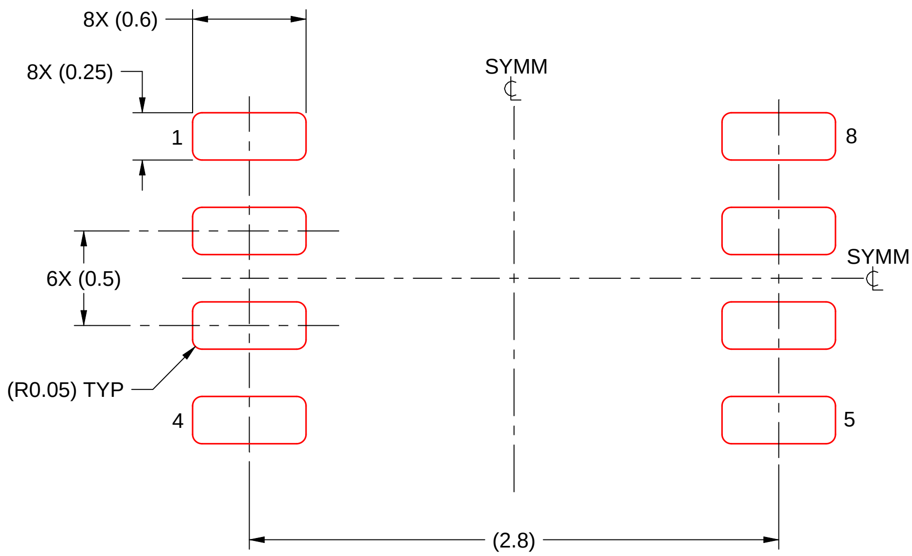
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4229400/A 02/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4229400/A 02/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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