ISOTMP35-Q1 車載対応 ±1.5℃、3kV$_{RMS}$ の絶縁型温度センサ、アナログ出力付き、応答時間 2 秒未満、動作電圧 500V$_{RMS}$

1 特長

- 次の測定結果により AEC-Q100 認定済み:
  - 温度グレード 0:-40℃～150℃の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
- 堅牢な内蔵絶縁バリア:
  - 絶縁耐圧:3000V$_{RMS}$
  - 絶縁動作電圧:500 V$_{RMS}$
- 絶縁バリアの寿命:> 50 years
- 温度センサの精度
  - ±0.5℃ (標準 25℃)
  - 0℃～70℃で ±1.5℃以下
  - -40℃～+150℃で ±2.0℃以下
- 動作電源電圧範囲:2.3V～5.5V
- 正のスロープ・センサ・ゲイン:10mV/℃、0℃で 500mV のオフセット
- 高速な熱応答:2 秒未満
- 短絡保護された出力
- 低消費電力:9µA (標準値)
- DFQ (SOIC-7) パッケージ
- 安全関連認証 (予定):
  - UL 1577 に準拠した絶縁耐圧:3kV$_{RMS}$ (1 分間)

2 アプリケーション

- 炭化ケイ素 (SiC) PowerFET 温度監視
- 絶縁型ゲート・バイポーラ・トランジスタ (IGBT) PowerFET 温度監視
- HEV/EV のバッテリ管理システム (BMS)
- HEV/EV のオンボード・チャージャ (OBC) およびワイヤレス・チャージャ
- HEV/EV の DC/DC コンバータ
- HEV/EV のインバータおよびモーター制御
- パワートレイン温度センサ

3 概要

ISOTMP35-Q1 は、業界初の絶縁型温度センサ IC であり、最大 3000V$_{RMS}$ の耐電圧の内蔵絶縁バリアと、-40℃～+150℃で 10mV/℃の勾配を特長とするアナログ温度センサを組み合わせています。この統合により、高価な絶縁回路を必要とせずに、センサを高電圧熱源 (たとえば HV FET、IGBT、HV コンタクタ) と同じ場所に設置することができます。また、高電圧熱源に直接接触することで、絶縁要件を満たすためにセンサを遠くに配置するアプローチに比べ、より高い精度と高速な熱応答が得られます。

ISOTMP35-Q1 は非絶縁型の 2.3V～5.5V 電源で動作するため、高電圧プレーンでサブレギュレートされた電源を利用できないアプリケーションに簡単に統合できます。

内蔵絶縁バリアは UL 1577 の要件を満たしています。表面実装パッケージ (7 ピン SOIC) は、熱源から組み込み熱センサへの優れた熱流を提供し、熱質量を最小限に抑え、より正確な熱源測定を実現します。これにより、時間のかかる熱モデリングの必要性が減り、製造や組み立てによる機械的なばらつきが減少するため、システム設計のマージンが向上します。

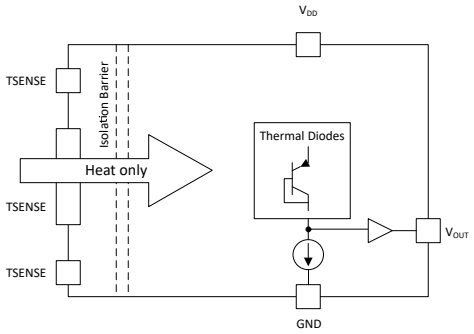
ISOTMP35-Q1 の Class-AB 出力ドライバは、最大出力が 500µA と強力で、最大 1000pF の容量性負荷を駆動でき、A/D コンバータ (ADC) のサンプル・ホールド入力と直接インターフェイスするように設計されています。

パッケージ情報

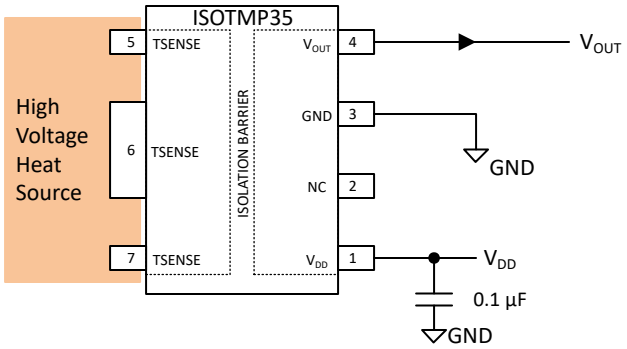
部品番号	パッケージ (1)	パッケージ・サイズ (2)
ISOTMP35-Q1	DFQ (SOIC、7)	4.9mm × 6mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

ADVANCE INFORMATION



機能ブロック図



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

ADVANCE INFORMATION

5 Pin Configuration and Functions

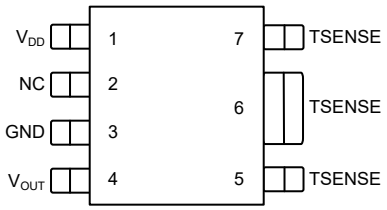

図 5-1. DFQ Package 7-Pin SOIC Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DFQ		
GND	3	G	Ground
NC	2	–	No connect
TSENSE	5	–	Temperature pin connected to high-voltage heat source
	6		
	7		
V_{DD}	1	P	Supply voltage
V_{OUT}	4	O	Output voltage proportional to temperature

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	6	V
Output voltage	V_{OUT}	–0.3	V_{DD} + 0.3	V
Output current	V_{OUT}	–30	30	mA
Operating junction temperature, T_J		–60	155	°C
Storage temperature, T_{stg}		–65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2500	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.3		5.5	V
T_A	Operating ambient temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		ISOTMP35-Q1 DFQ (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	38.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	°C/W
M_T	Thermal Mass	51.0	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Insulation Specification

Over free-air temperature range and V_{DD} = 2.3 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External Clearance(1)	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112; IEC 60112	>400	V
	Material Group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	707	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	500	V_{RMS}
		At DC voltage	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	TBD	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	7800	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤ 5	
		Method b2, at routine test (100% production)(6), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$; $t_{ini} = t_m$ = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	TBD	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	TBD	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	TBD	
		V_{IO} = 500 V at T_A = 150°C	TBD	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of the board design to make sure that the mounting pads of the isolator on the printedcircuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the isolation barrier.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.
(6) Either method b1 or b2 is used in production

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6.6 Electrical Characteristics

Over free-air temperature range and V_{DD} = 2.3 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy	0°C to 70°C		–1.5	±0.5	1.5	°C
T_{ERR}	Temperature accuracy	-40°C to 150°C		–2.5	±0.5	2.5	°C
PSR	DC power supply rejection			–0.05		0.05	°C/V
T_{SENS}	Temperature sensitivity	T_A = –40°C to 150°C			10.00		mV/°C
T_{LTD}	Long-term drift(1)	1000 hours at 150°C, 3.3 V			TBD		°C
V_{OUT}	Output voltage	T_A = 0°C			500		mV
		T_A = 25°C			750		mV
NL	Nonlinearity	T_A = –40°C to 150°C			0.5		°C
t_{RESP_D}	Directional Response time	2-layer 62-mil Rigid PCB 2 oz. Copper	τ = 63 % TSENSE = 25°C to 75°C Pins 4 to 7 = 25°C		TBD		ms
t_{RESP_L}	Response time (Stirred Liquid)	Unmounted (Single layer Flex PCB)	τ = 63 % 25°C to 125°C		TBD		ms
		Mounted (2-layer 62-mil PCB)			TBD		ms
ANALOG OUTPUT							
Z_{OUT}	Output impedance	I_{LOAD} = 100 µA, f = 100 Hz			20		Ω
		I_{LOAD} = 100 µA, f = 500 Hz			50		Ω
I_{OUT}	Output current					500	µA
L_R	Load regulation	I_{LOAD} = –600 µA to 600 µA			6		mV
C_L	Maximum capacitive load					1	nF
POWER SUPPLY							
I_{DD}	Operating current	V_{DD} = 3.3 V T_A = 25°C			10	12	µA
		T_A = –40°C to 150°C				17	µA

(1) Long term stability is determined using accelerated operational life testing at a junction temperature of 150°C.

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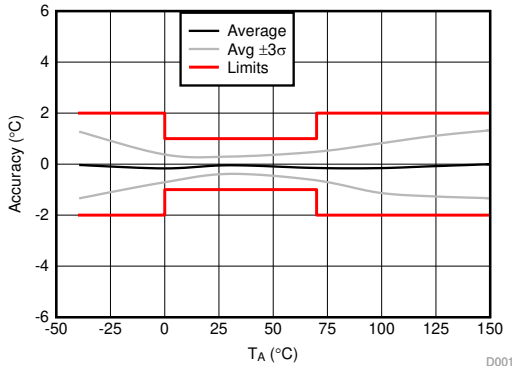
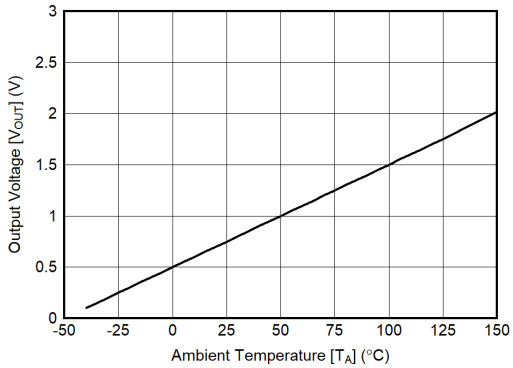
6.7 Typical Characteristics

at T_A = 25°C, (unless otherwise noted)



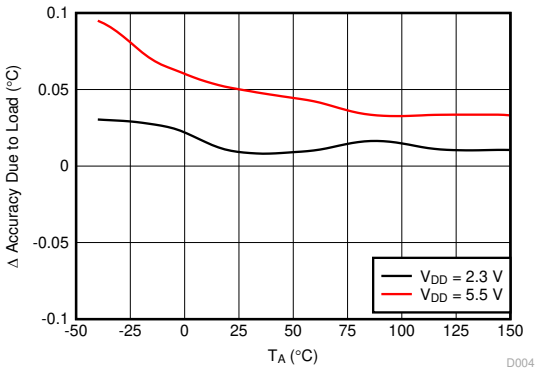
V_{DD} = 2.3 to 5.5 V, I_{OUT} = 0 µA, C_{LOAD} = 1000 pF

図 6-1. Accuracy vs T_A Temperature



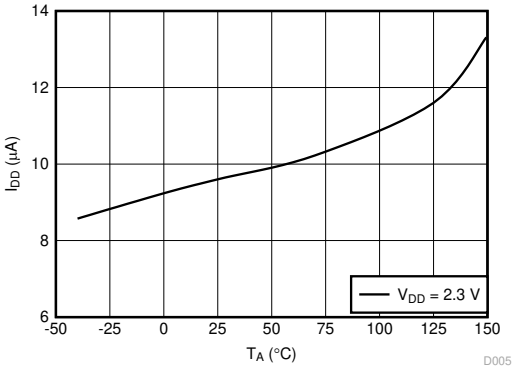
I_{OUT} = 0 µA, C_{LOAD} = 1000 pF

図 6-2. Output Voltage vs Ambient Temperature



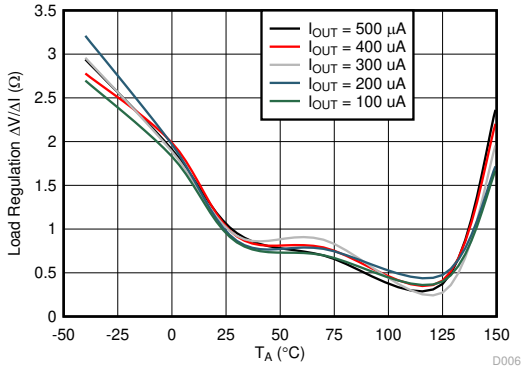
I_{OUT} = from 0 µA to 100 µA, C_{LOAD} = 1000 pF

図 6-3. Changes in Accuracy vs Ambient Temperature (Due to Load)



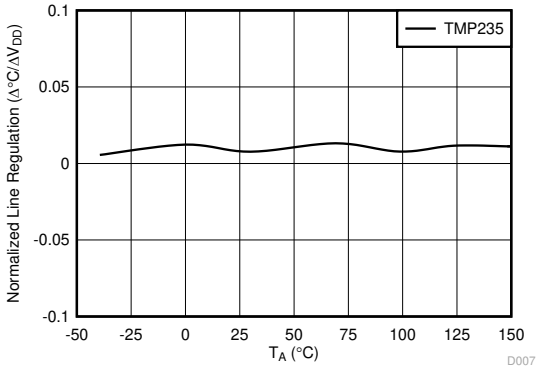
I_{OUT} = 0 µA, C_{LOAD} = 1000 pF

図 6-4. Supply Current vs Temperature



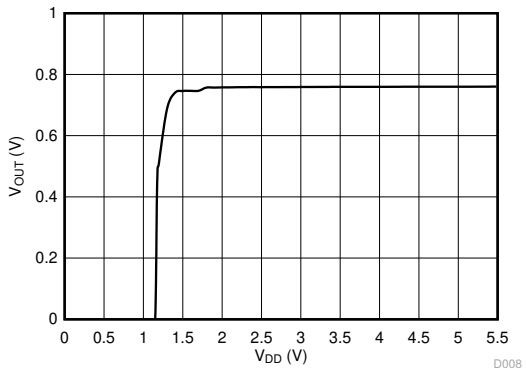
V_{DD} = 2.3 V, C_{LOAD} = 1000 pF

図 6-5. Load Regulation vs Ambient Temperature



V_{DD} = 2.3 to 5.5 V, I_{OUT} = 0 µA, C_{LOAD} = 1000 pF

図 6-6. Line Regulation (Δ°C / ΔV_{DD}) vs Ambient Temperature



T_A = 25°C

図 6-7. Output Voltage vs Power Supply

Graph Placeholder

T_A = 25°C

図 6-8. Output vs. Settling Time to Step V_{DD}

Graph Placeholder

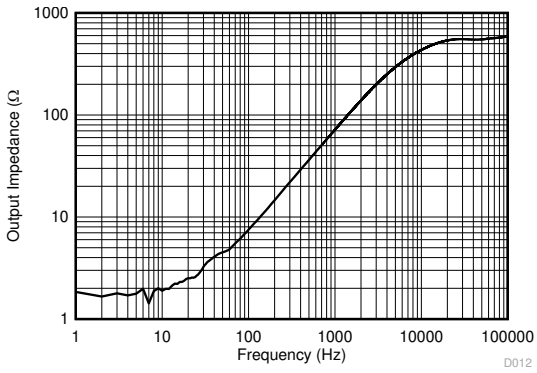
T_A = 25°C, V_{DD} Ramp Rate = 5 V/ms

図 6-9. Output vs. Settling Time to Ramp V_{DD}

Graph Placeholder

1 × 1 (inches) PCB, Air 26°C to Fluid Bath 123°C

図 6-10. Thermal Response (Air-to-Fluid Bath)



T_A = 25°C, V_{DD} = 5 V, I_{OUT} = 100 µA

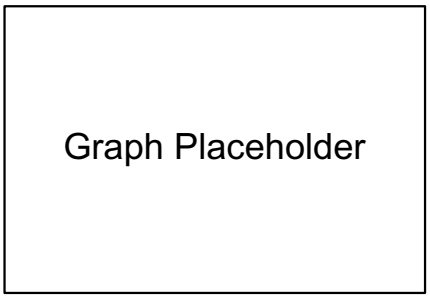
図 6-11. Output Impedance vs Frequency

Graph Placeholder

T_A = 25°C

図 6-12. PSRR vs Frequency

ADVANCE INFORMATION



T_A = 25°C

図 6-13. Output Noise Density

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7 Detailed Description

7.1 Overview

The ISOTMP35-Q1 is a linear analog output temperature sensor with an output voltage proportional to temperature. The temperature sensor has an accuracy from 0°C to +125°C of ±1°C. The ISOTMP35-Q1 provides a positive slope output of 10 mV/°C over the full –40°C to +150°C and a supply range from 2.3 V to 5.5 V. A class-AB output driver provides a maximum output of 500 µA to drive capacitive loads up to 1000 pF.

7.2 Functional Block Diagram

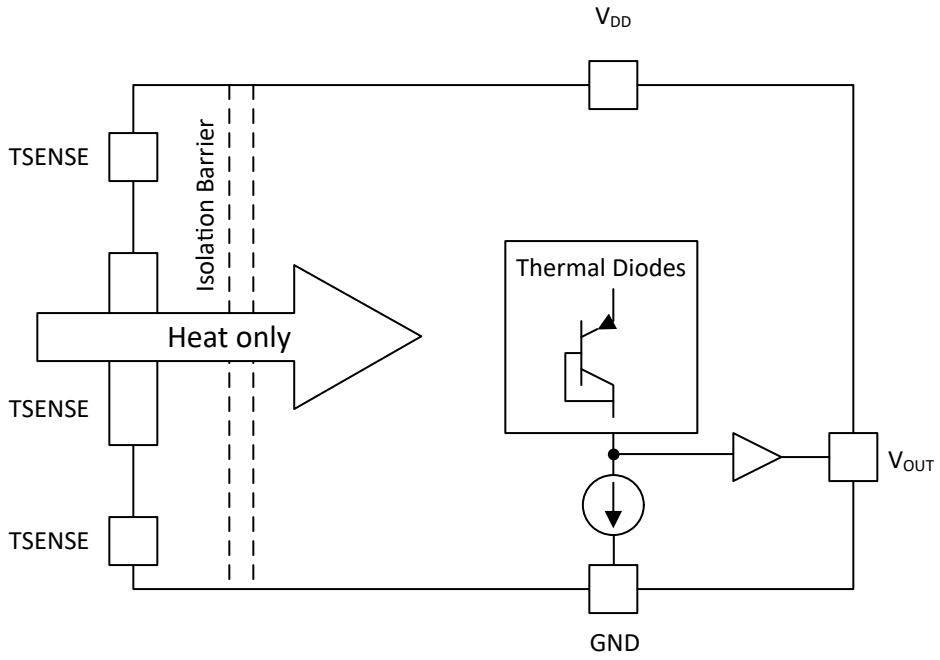

図 7-1. Functional Block Diagram

7.3 Features Description

The ISOTMP35-Q1 device combines a robust integrated isolation barrier with a tight accuracy analog output temperature sensor. All the features related to the analog output, accuracy, output characteristics of the sensor, and drive characteristic of the output will be treated under the analog output section.

7.3.1 Integrated Isolation Barrier and Thermal Response

The ISOTMP35-Q1 is designed to integrate a robust isolation barrier while maximizing the heat flow. This is made possible by a SO-7 package designed to provide the 3-kVRMS isolating rating (UL1577) and isolation mechanism that minimizes the thermal response from the TSENSE pins to the temperature sensor.

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7.3.2 Analog Output

The analog output of the ISOTMP35-Q1 has several characteristics, such as the output accuracy, linearity and drive capability, that must be understood to design the interface to the rest of the signal chain.

7.3.3 Thermal Response

The SOIC-7 package is designed to maximize the heat flow, and minimize the thermal response time, from the TSENSE pins to the temperature sensor while also providing the 3 kV_{RMS} isolation rating (UL1577).

7.4 Device Functional Modes

The singular functional mode of the ISOTMP35-Q1 is an analog output directly proportional to temperature.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The features of the ISOTMP35-Q1 make the device versatile for various high voltage temperature-sensing applications. The ISOTMP35-Q1 can operated down to a 2.3-V supply with 9-µA current consumption. As a result, the device is also well designed for battery applications where a number of these batteries may be stacked for high voltage output.

8.1.1 Output Voltage Linearity

As illustrated in 図 6-2, the ISOTMP35-Q1 device exhibit a linear output of 10 mV/°C. For temperature above 100°C, a small gain shift (T_C) is present on the output (V_{OUT}). When small shifts are expected, a piecewise linear function provides the best accuracy and is used for the device accuracy specifications. 表 8-2 lists the typical output voltages of the ISOTMP35-Q1 device across the full operating temperature range. The calculated linear column represents the ideal linear V_{OUT} output response with respect to temperature, while the piecewise linear columns indicate the small voltage shift at elevated temperatures.

The piecewise linear function uses three temperature ranges listed in 表 8-1. Use 式 1 to calculate the voltage output V_{OUT} of the ISOTMP35-Q1:

$$V_{OUT} = (T_A - T_{INFL}) \times T_C + V_{OFFS} \quad (1)$$

where

- V_{OUT} is the voltage output for a given temperature
- T_A is the ambient temperature in°C
- T_{INFL} is the temperature inflection point for a piecewise segment in°C
- T_C is the temperature coefficient or gain
- V_{OFFS} is the voltage offset

Use 表 8-2 to calculate the ambient temperature (T_A) for a given V_{OUT} voltage output within a piecewise voltage range (V_{RANGE}). For applications where the accuracy enhancement above 100°C is not required, use the first row of 表 8-1 for all voltages.

$$T_A = (V_{OUT} - V_{OFFS}) \div T_C + T_{INFL} \quad (2)$$

表 8-1. Piecewise Linear Function Summary

T_A RANGE (°C)	V_{RANGE} (mV)	T_{INFL} (°C)	T_C (mV/°C)	V_{OFFS} (mV)
–40 to +100	< 1500	0	10	500
+100 to +125	1500 to 1752.5	100	10.1	1500
+125 to +150	> 1752.5	125	10.6	1752.5

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表 8-2. Transfer Table

TEMPERATURE (°C)	V_{OUT} (mV) CALCULATED LINEAR VALUES	V_{OUT} (mV) PIECEWISE LINEAR VALUES
–40	100	100
–35	150	150
–30	200	200
–25	250	250
–20	300	300
–15	350	350
–10	400	400
–5	450	450
0	500	500
5	550	550
10	600	600
15	650	650
20	700	700
25	750	750
30	800	800
35	850	850
40	900	900
45	950	950
50	1000	1000
55	1050	1050
60	1100	1100
65	1150	1150
70	1200	1200
75	1250	1250
80	1300	1300
85	1350	1350
90	1400	1400
95	1450	1450
100	1500	1500
105	1550	1550.5
110	1600	1601
115	1650	1651.5
120	1700	1702
125	1750	1752.5
130	1800	1805/5
135	1850	1858/5
140	1900	1911.5
145	1950	1964.5
150	2000	2017.5

8.1.2 Load Regulation

Load regulation is how the analog output voltage of the ISOTMP35-Q1 will change as the output load current changes, and is measured across temperature. Load regulation is important because when implementing the ISOTMP35-Q1 with an ADC, the user can use an RC filter on the analog output. Knowing how the output voltage will change based on the current pulled with different resistive and capacitive loads will help the user make accurate temperature measurements with the ISOTMP35-Q1. See 図 6-5 for more details on Load Regulation and セクション 8.1.6 for more details on how to use the ISOTMP35-Q1 with an ADC.

8.1.3 Start-Up Settling Time

The ISOTMP35-Q1 can support either a step input power supply or a ramp power supply. When powering the device, consider the analog output settling time upon start-up. For a step V_{DD} input, start-up time is approximately 1 ms.

The ISOTMP35-Q1 can support either a step input power supply or a ramp power supply. When powering the ISOTMP35-Q1, the user must keep in mind that the ISOTMP35-Q1 requires time to settle the analog output upon start-up:

- For a step V_{DD} input, start-up time is approximately 1 ms.
- For a ramp V_{DD} input with a ramp rate of 5 V/ms, start-up time is approximately 1.25 ms.

See 図 6-8 and 図 6-9 for more information.

8.1.4 Thermal Response

The 7-pin SOIC package is designed to maximize the heat flow, and minimize the thermal response time, from the TSENSE pins to the temperature sensor while also providing the 3 kV_{RMS} isolation rating (UL1577).

8.1.5 External Buffer

In case of higher capacitance on the output or a long trace between the sensor and the ADC, a external buffer can be added. This implementation is shown in 図 8-1 for the signal to be temperature voltage to be sent through a differential pair.

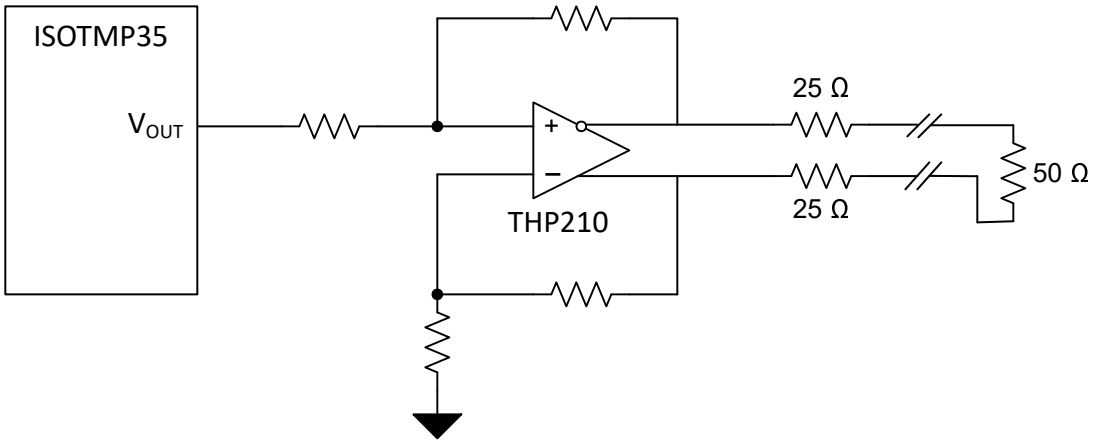

図 8-1. Buffering Prior to Sending Data Through a Differential Pair

8.1.6 ADC Selection and Impact on Accuracy

When connecting the ISOTMP35-Q1 analog output to an ADC, it is important to use an RC filter on the output. Most ADCs have a sampled comparator input structure. When the sampling is active, a switch internal to the ADC will charge an internal capacitor (C_{SAMPLE}). The capacitor requires instantaneous charge from the analog output source (ISOTMP35-Q1), so this will lead to voltage drops on the ISOTMP35-Q1 analog output, which will appear as incorrect temperature reads. By placing a filter capacitor (C_{FILTER}) load on the ISOTMP35 analog output, the voltage drops are mitigated. This works because C_{FILTER} will store charge from the analog output that

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the ADC can pull from when sampling, so there will not be a voltage drop on the ISOTMP35-Q1 output. Users can also add R_{FILTER} to filter out noise on the analog output.

Consider the maximum load capacitance. The ISOTMP35-Q1 has a maximum load capacitance of 1000 pF, therefore the total capacitance on the analog output, including those in the ADC input, must not exceed 1000 pF.

When choosing the R and C filter values, the RC time constant will change the settling time of the ISOTMP35-Q1. ADCs often have customizable sampling rates, so the settling time of the ISOTMP35-Q1 must be less than the chosen sampling time of the ADC. For example, an ADC with a data rate (DR) of 1 KSPS will have a conversion time of 1 ms, therefore any chosen R and C filter values must be completely settled within 1 ms ($5 \times R \times C < 1/DR$).

ADCs often have customizable full scale ranges (FSR), either digitally or through reference voltages. The ISOTMP35-Q1 at 150°C will output a maximum voltage of 2017.5 mV. When choosing an ADC, there should be a full scale range option with at least that much range. TI recommends a FSR option of at least +3 V to avoid headroom concerns in this example. To determine the desired ADC resolution, the ADC LSB size must be known. For the ISOTMP35-Q1, the device does not have an LSB but rather the LSB of the ADC will determine the measurement resolution.

- For example, a 12-bit ADC with an FSR of 3.3 V, has an LSB size of 806 µV. This translates to 80 m°C of temperature resolution. A 16-bit ADC with an FSR of 3.3 V, has an LSB size of 50 µV, which gives 5 m°C of temperature resolution. A 12-bit ADC will be sufficient for most applications.
- It is important to be mindful that the analog output voltage from the ISOTMP35-Q1 cannot exceed the V_{DD} being supplied to the ADC. So, it is necessary to choose a V_{DD} for the ADC that exceeds the chosen FSR required to fully capture the ISOTMP35-Q1 analog output range.

表 8-3. ADC Settling Times and Cutoff Frequencies

SETTLING TIME (µs) & CUTOFF FREQUENCY (KHz)	SETTLING TIME (5*RC TIME CONSTANT)			CUTOFF FREQUENCY (fC = 1/(2πRC))		
	100 pF	680 pF	1000 pF	100 pF	680 pF	1000 pF
1 KΩ	0.5 µs	3.4 µs	5 µs	1592 KHz	234.2 KHz	159.2 KHz
4.7 KΩ	2.35 µs	15.98 µs	23.5 µs	338.8 KHz	49.8 KHz	33.88 KHz
10 KΩ	5 µs	34 µs	50 µs	159.2 KHz	23.42 KHz	15.92 KHz
100 KΩ	50 µs	340 µs	500 µs	15.92 KHz	2.34 KHz	1.592 KHz

8.1.7 Implementation Guidelines

Voltage clearance on the line must be respected.

A minimum of two layers is required for the ISOTMP35-Q1. Standard layer stacking can be used for a 4-layer PCB where the signal traces can run either on the top or bottom layer. Solid ground and power plane must form the inner layer. See PCB Cross-Section for a depiction of plane and trace clearance under the device.

図 8-2. PCB Cross-Section

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8.1.8 PSRR

Depending on the application, there may be a significant amount of high frequency noise on the power supply line. If high frequency noise (>100 KHz) is present, the user can switch to a 1-µF bypass capacitor to provide additional filtering on the power supply line. Increasing the bypass capacitance or choosing a capacitor with a lower ESR across frequency will improve PSRR performance.

An additional power supply consideration is line regulation. For the ISOTMP35-Q1, line regulation refers to the change in output temperature with changing power supply. 図 6-6 shows that, across the entire environment temperature range, ISOTMP35-Q1 maintains a steady amount change in temperature across V_{DD}.

8.2 Typical Application

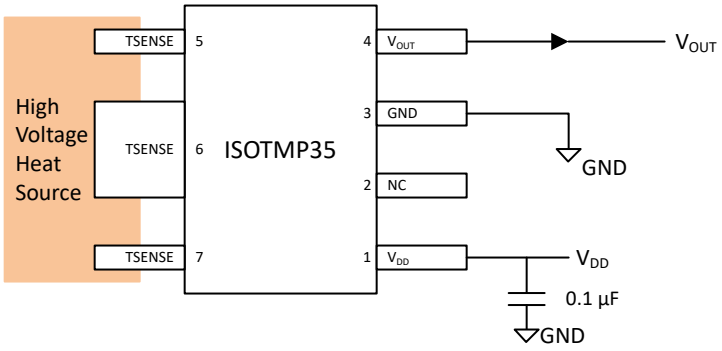

図 8-3. Typical ISOTMP35-Q1 Circuit

8.2.1 Design Requirements

To design with ISOTMP35-Q1, use the parameters listed in 表 8-4. Most CMOS-based ADCs have a sampled data comparator input structure. When the ADC charges the sampling capacitor, the capacitor requires instantaneous charge from the output of the analog temperature sensor, such as the ISOTMP35-Q1. Therefore, the output impedance of the temperature sensor can affect ADC performance. In most cases, adding an external capacitor mitigates design challenges. The ISOTMP35-Q1 is specified and characterized with a 1000-pF maximum capacitive load (C_{LOAD}). The C_{LOAD} is a sum of the C_{FILTER}, C_{MUX} and C_{SAMPLE}. TI recommends maximizing the C_{FILTER} value while allowing for the maximum specified ADC input capacitance (C_{MUX} + C_{SAMPLE}) to limit the total C_{LOAD} at 1000 pF. In most cases, a 680-pF C_{FILTER} provides a reasonable allowance for ADC input capacitance to minimize ADC sampling error and reduce noise coupling. An optional series resistor (R_{FILTER}) and C_{FILTER} provides additional low-pass filtering to reject system level noise. TI recommends placing R_{FILTER} and C_{FILTER} as close to the ADC input as possible for optimal performance.

表 8-4. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{DD}	2.3 V to 5.5 V
Decoupling capacitor between V_{DD} and GND	0.1 µF

8.2.2 Detailed Design Procedure

Depending on the input characteristics of the ADC, an external C_{FILTER} can be required. The value of C_{FILTER} depends on the size of the sampling capacitor (C_{SAMPLE}) and the sampling frequency while observing a maximum C_{LOAD} of 1000 pF. The capacitor requirements can vary because the input stages of all ADCs are not identical.

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8.2.2.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 8-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature.

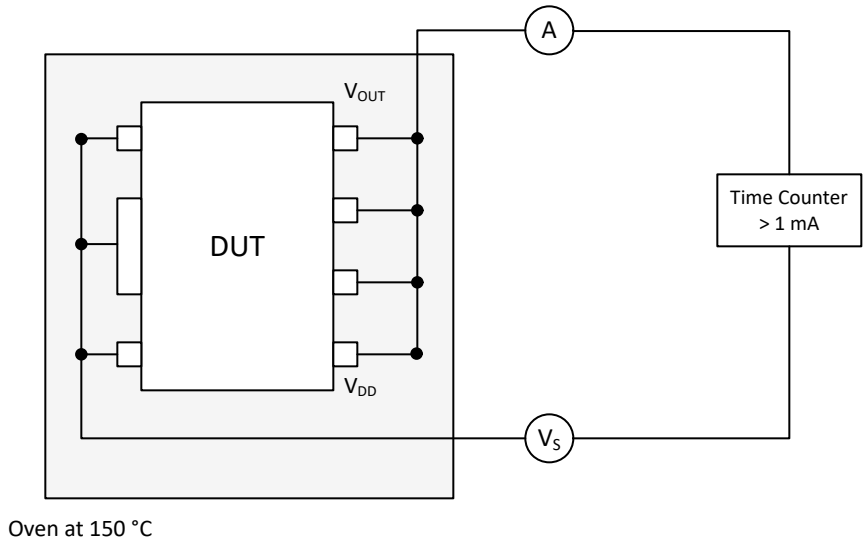

図 8-4. Test Setup for Insulation Lifetime Measurement

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8.3 Power Supply Recommendations

To help ensure reliable operation at supply voltages, a 0.1-µF bypass capacitor is recommended at the V_{DD} supply pin. Place the capacitor as close to the supply pin as possible. As there is on a single side power supply for the ISOTMP35-Q1, there is no need to generate isolated power.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of two layers is required for the ISOTMP35-Q1. For a 4-layer PCB, TI recommends a standard layer stacking method where the signal traces run either on the top of bottom layer. Solid ground and power plane must form the inner layer.

8.4.2 Layout Example

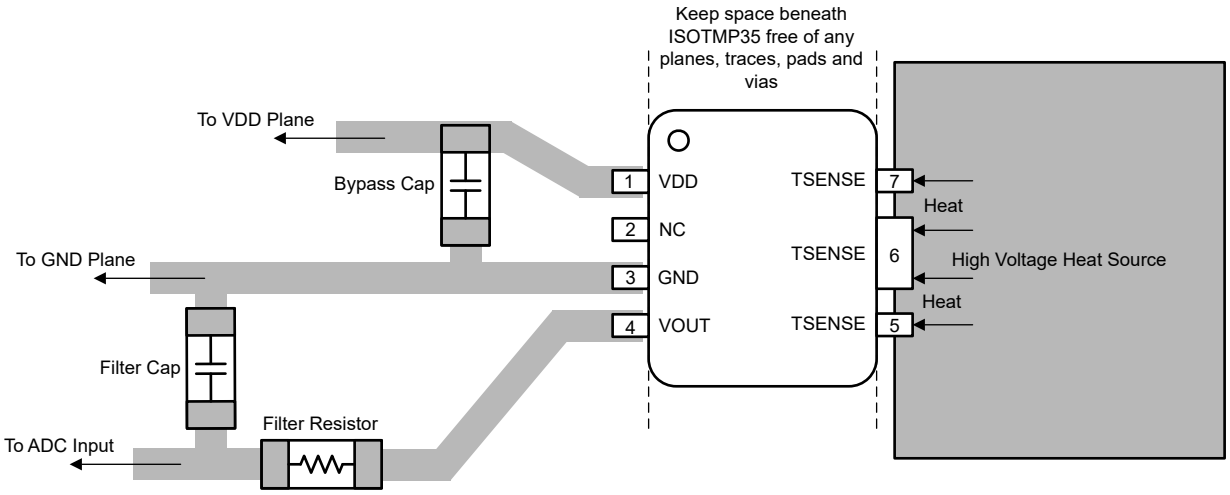

図 8-5. Layout Example

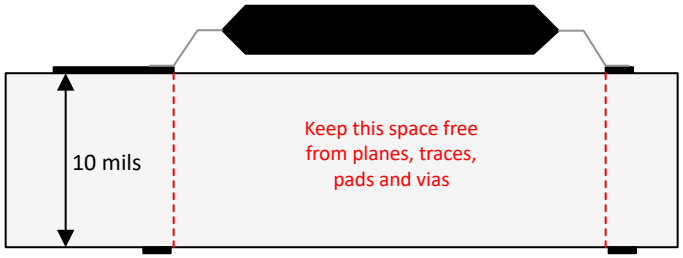

図 8-6. Layout Example - PCB Cross-Section

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ISOTMP35 Evaluation Module User's Guide*
- Texas Instruments, *Circuit for driving an ADC with an instrumentation amplifier in high gain*
- Texas Instruments, *Driving a SAR ADC directly without a front-end buffer circuit (low-power, low-sampling-speed DAQ)*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

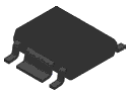
9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

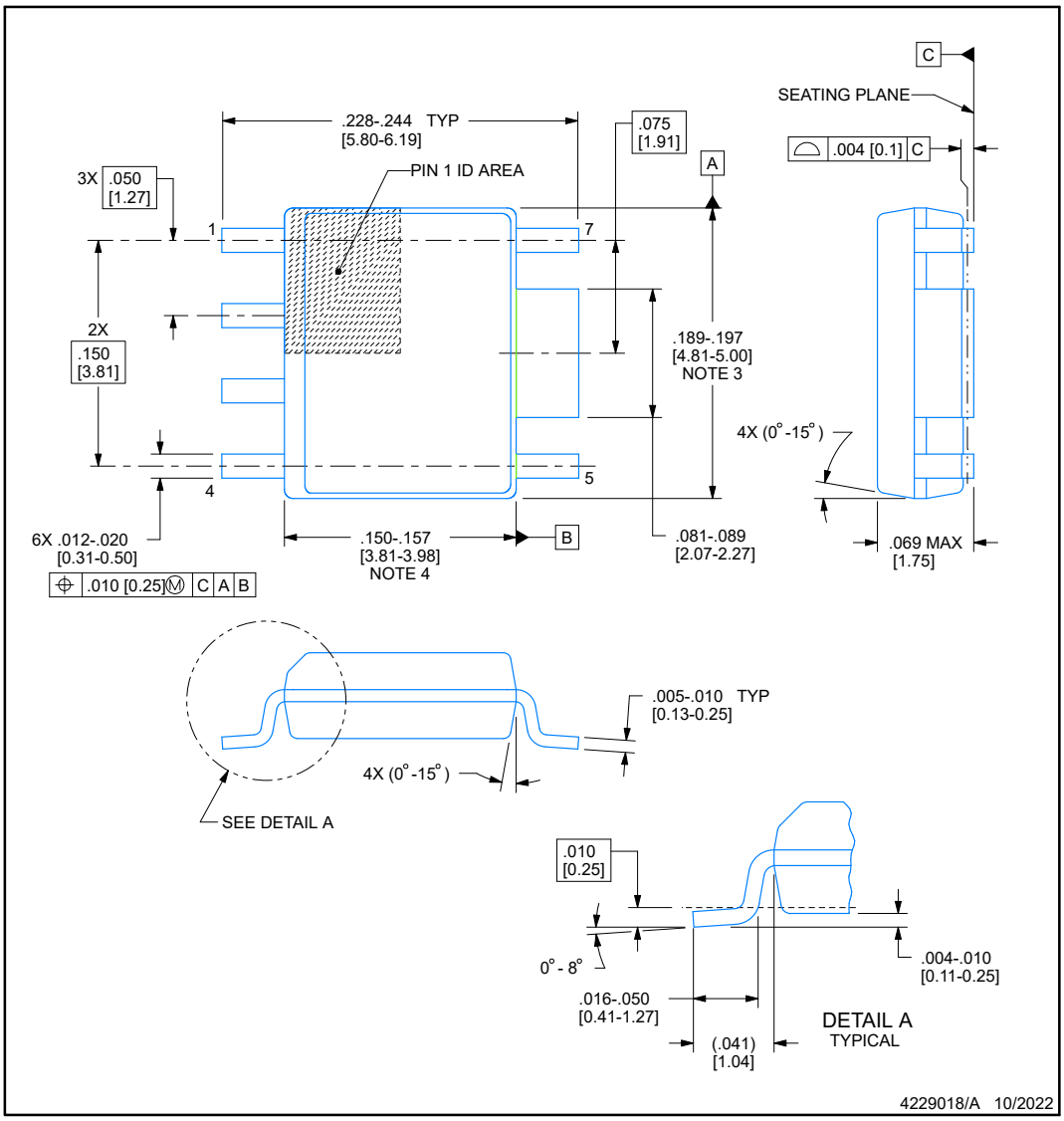


PACKAGE OUTLINE

DFQ0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. No JEDEC Registration as of September 2022

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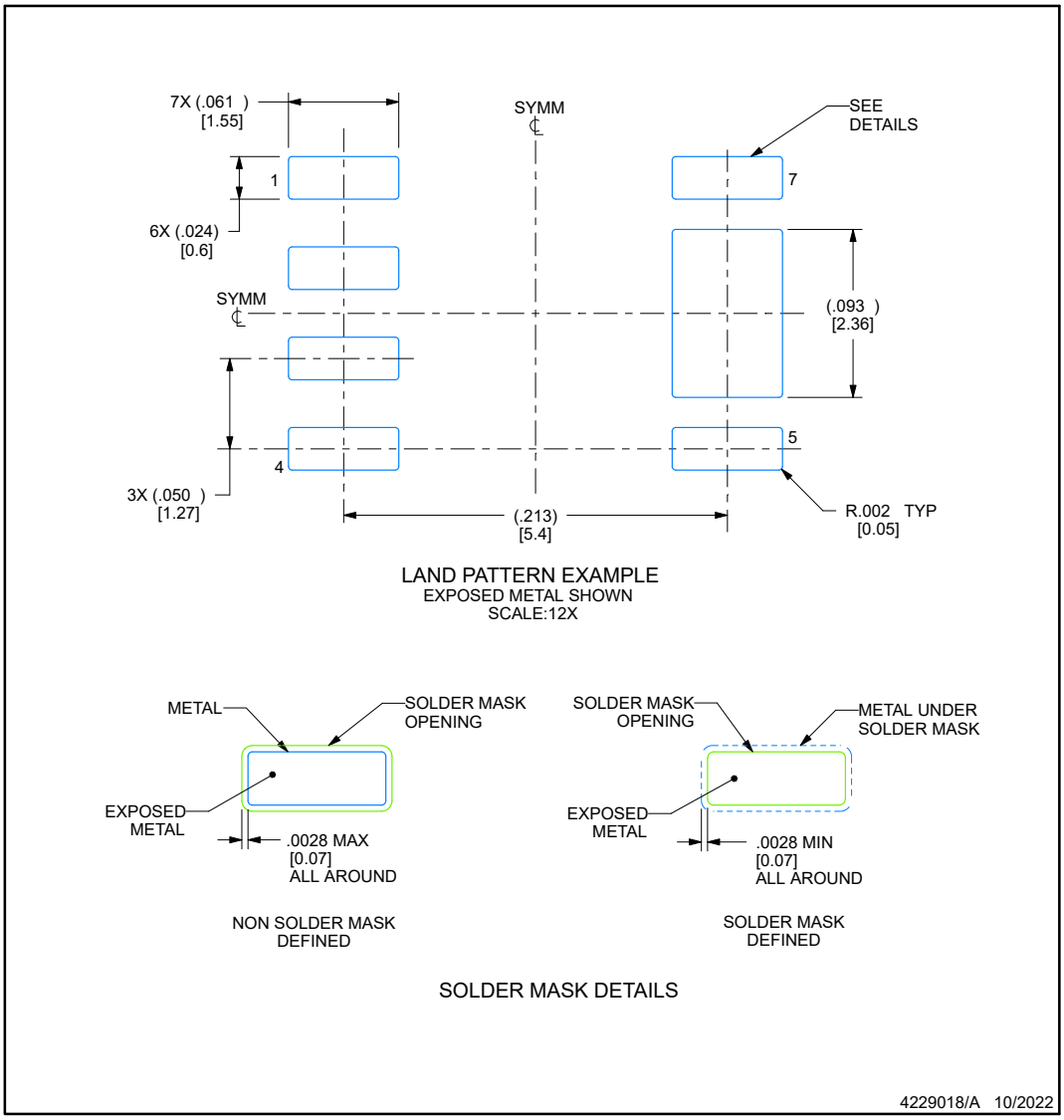
EXAMPLE BOARD LAYOUT

DFQ0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PISOTMP35BDFQRQ1	ACTIVE	SOIC	DFQ	7	3000	Call TI	Call TI	Call TI	-40 to 150	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

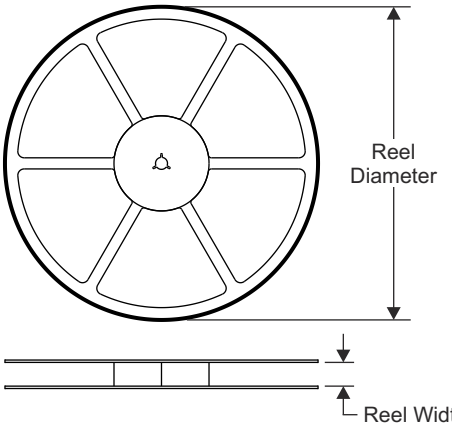
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

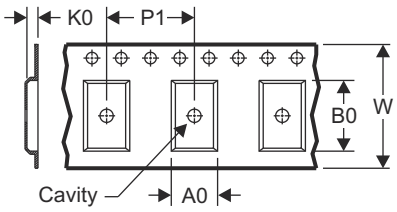
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Tape and Reel Information

REEL DIMENSIONS

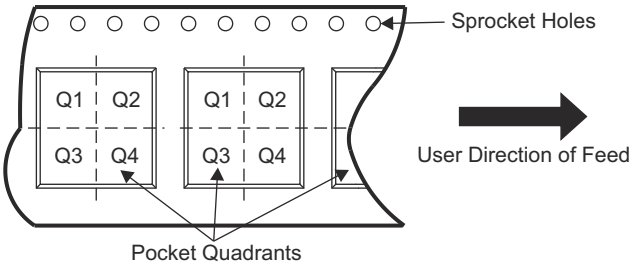


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PISOTMP35BDFQRQ1	SOIC	DFQ	7	3000	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI

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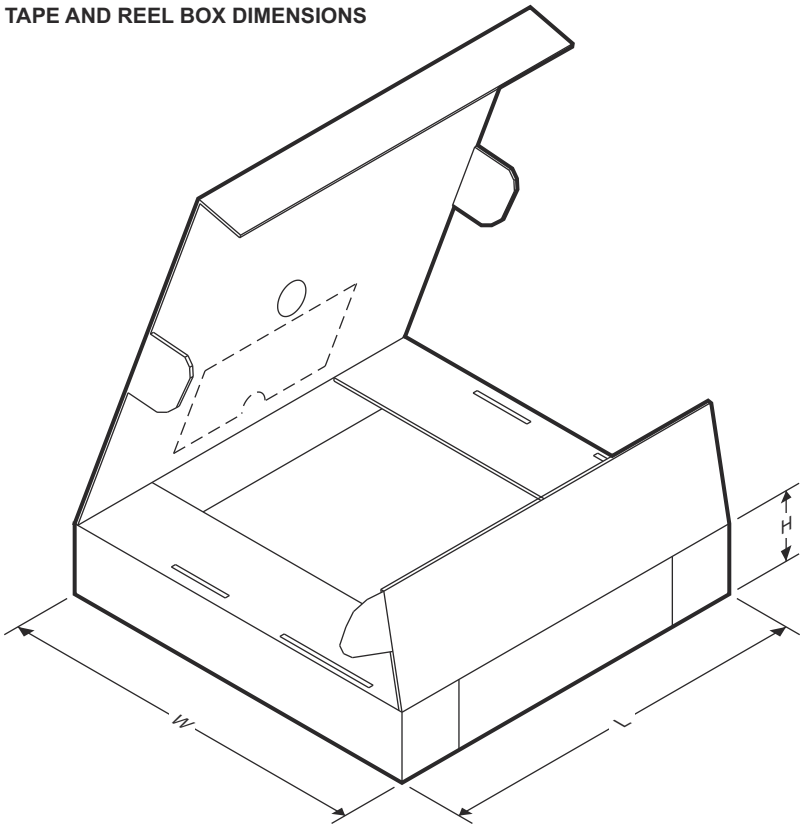
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PISOTMP35BDFQRQ1	SOIC	DFQ	7	3000	Call TI	Call TI	Call TI

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PISOTMP35BEDFQRQ1	ACTIVE	SOIC	DFQ	7	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISOTMP35-Q1 :

- Catalog : ISOTMP35

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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