TEXAS INSTRUMENTS
LM25575-Q1
JAJSEF9 – DECEMBER 2017

LM25575-Q1 42V、1.5A降圧型スイッチング・レギュレータ

1 特長

- 車載アプリケーションに対応
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
- 42V、330mΩのNチャネルMOSFETを内蔵
- 非常に広い入力電圧範囲: 6V～42V
- 出力電圧を最低1.225Vまで調整可能
- 1.5%のフィードバック・リファレンス精度
- 単一の抵抗により、動作周波数を50kHz～1MHzの範囲で設定可能
- マスタまたはスレーブの周波数同期
- 調整可能なソフト・スタート
- 電流モード制御アーキテクチャのエミュレーション
- 広帯域幅のエラー・アンプ
- 内蔵の保護機能
- HTSSOP-16EP (露出パッド)
- WEBENCH® Power Designerにより、LM25575-Q1を使用するカスタム設計を作成

2 アプリケーション

- 産業用

3 概要

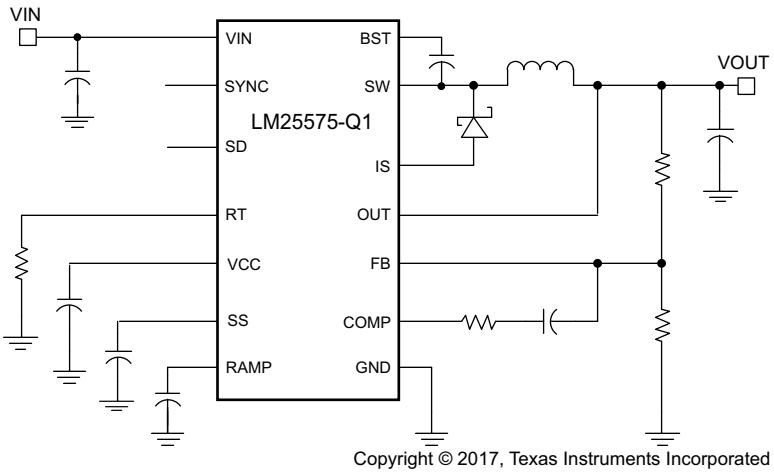
LM25575-Q1は、使いやすい降圧型レギュレータで、設計エンジニアは最小点数の部品を使用して、堅牢な電源を設計し、最適化できます。LM25575-Q1は6V～42Vの範囲の入力電圧で動作し、内蔵の330mΩ NチャネルMOSFETにより、1.5Aの連続出力電流を供給します。このレギュレータはエミュレーション電流モード・アーキテクチャを活用しているため、ライン・レギュレーション、厳格な負荷過渡応答、容易なループ補償という固有の特性があり、電流モード・レギュレータで一般的な、低いデューティ・サイクルの制限はありません。動作周波数は50kHz～1MHzの範囲に設定でき、サイズと効率を最適化できます。EMIを低減するための周波数同期ピンがあり、LM(2)557xファミリに属する複数のICで、自己同期または外部クロックへの同期を選択できます。LM25575-Q1のサイクルごとの電流制限、短絡保護、サーマル・シャットダウン、およびリモート・シャットダウン機能により、堅牢性が保証されます。このデバイスは、放熱を助けるために露出したパッドがダイに取り付けられ、消費可能電力が増大した、HTSSOP-16パッケージで供給されます。LM25575-Q1は、WEBENCH®オンライン設計ツールの完全なスイートでサポートされています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM25575-Q1	HTSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

簡略化されたアプリケーション回路図



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4 改訂履歴

日付	改訂内容	注
2017年12月	*	初版

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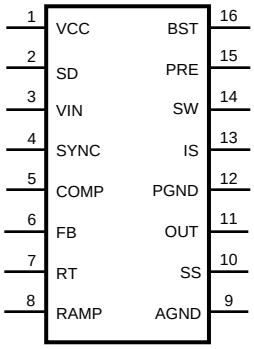
5 Pin Configuration and Functions

PWP
16-Pin HTSSOP
Top View



Pin Functions

NO.	Name	Description
1	VCC	Output of the bias regulator V_{CC} tracks V_{IN} up to 9 V. Beyond 9 V, V_{CC} is regulated to 7 Volts. A 0.1 uF to 1 uF ceramic decoupling capacitor is required. An external voltage (7.5 V – 14 V) can be applied to this pin to reduce internal power dissipation.
2	SD	Shutdown or UVLO input If the SD pin voltage is below 0.7 V the regulator will be in a low power state. If the SD pin voltage is between 0.7 V and 1.225 V the regulator will be in standby mode. If the SD pin voltage is above 1.225 V the regulator will be operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5 µA pull-up current source configures the regulator fully operational.
3	VIN	Input supply voltage Nominal operating range: 6 V to 42 V
4	SYNC	Oscillator synchronization input or output The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM25575-Q1 devices can be synchronized together by connection of their SYNC pins.
5	COMP	Output of the internal error amplifier The loop compensation network should be connected between this pin and the FB pin.
6	FB	Feedback signal from the regulated output This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225 V.
7	RT	Internal oscillator frequency set input The internal oscillator is set with a single resistor, connected between this pin and the AGND pin.
8	RAMP	Ramp control signal An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50 pF to 2000 pF.
9	AGND	Analog ground Internal reference for the regulator control functions
10	SS	Soft-start An external capacitor and an internal 10 µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, V_{CC} UVLO and thermal shutdown.
11	OUT	Output voltage connection Connect directly to the regulated output voltage.
12	PGND	Power ground Low side reference for the PRE switch and the IS sense resistor.
13	IS	Current sense Current measurement connection for the re-circulating diode. An internal sense resistor and a sample/hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
14	SW	Switching node The source terminal of the internal buck switch. The SW pin should be connected to the external Schottky diode and to the buck inductor.

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Pin Functions (continued)

NO.	Name	Description
15	PRE	Pre-charge assist for the bootstrap capacitor This open drain output can be connected to SW pin to aid charging the bootstrap capacitor during very light load conditions or in applications where the output may be pre-charged before the LM25575-Q1 is enabled. An internal pre-charge MOSFET is turned on for 250 ns each cycle just prior to the on-time interval of the buck switch.
16	BST	Boost input for bootstrap capacitor An external capacitor is required between the BST and the SW pins. A 0.022 µF ceramic capacitor is recommended. The capacitor is charged from V_{CC} via an internal diode during the off-time of the buck switch.
NA	EP	Exposed Pad Exposed metal pad on the underside of the device. It is recommended to connect this pad to the PWB ground plane, in order to aid in heat dissipation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} to GND		45	V
BST to GND		60	V
PRE to GND		45	V
SW to GND (Steady State)		–1.5	V
BST to V_{CC}		45	V
SD, V_{CC} to GND		14	V
BST to SW		14	V
OUT to GND	Limited	V_{IN}	V
SYNC, SS, FB, RAMP to GND		7	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

	MIN	MAX	UNIT
V_{IN}	6	42	V
T_J Operation junction temperature	–40	125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC(1)		LM25575-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	14	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_J = 25°C, and V_{IN} = 24 V, R_T = 32.4 kΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STARTUP REGULATOR							
V_{CC}Reg	V_{CC} Regulator Output	T_J = –40°C to +125°C		6.85	7.15	7.45	V
	V_{CC} LDO Mode turn-off				9		V
	V_{CC} Current Limit	V_{CC} = 0 V			25		mA
VCC SUPPLY							
	V_{CC} UVLO Threshold	(V_{CC} increasing)	T_J = –40°C to +125°C	5.03	5.35	5.67	V
	V_{CC} Undervoltage Hysteresis				0.35		V
	Bias Current (Iin)	FB = 1.3 V	T_J = –40°C to +125°C		3.7	4.5	mA
	Shutdown Current (Iin)	SD = 0 V	T_J = –40°C to +125°C		48	70	µA
SHUTDOWN THRESHOLDS							
	Shutdown Threshold	(SD Increasing)	T_J = –40°C to +125°C	0.47	0.7	0.9	V
	Shutdown Hysteresis				0.1		V
	Standby Threshold	(Standby Increasing)	T_J = –40°C to +125°C	1.17	1.225	1.28	V
	Standby Hysteresis				0.1		V
	SD Pull-up Current Source				5		µA
CURRENT LIMIT							
	Cycle by Cycle Current Limit	RAMP = 0 V	T_J = –40°C to +125°C	1.8	2.1	2.5	A
	Cycle by Cycle Current Limit Delay	RAMP = 2.5 V			85		ns
SOFT-START							
	SS Current Source	T_J = –40°C to +125°C		7	10	14	µA
OSCILLATOR							
	Frequency 1	T_J = –40°C to +125°C		180	200	220	kHz
	Frequency 2	R_T = 11 kΩ	T_J = –40°C to +125°C	425	485	545	kHz
	SYNC Source Impedance				11		kΩ
	SYNC Sink Impedance				110		Ω
	SYNC Threshold (falling)				1.3		V
	SYNC Frequency	R_T = 11 kΩ	T_J = –40°C to +125°C	550			kHz
	SYNC Pulse Width Minimum	T_J = –40°C to +125°C		15			ns
RAMP GENERATOR							
	Ramp Current 1	V_{IN} = 36 V, V_{OUT} = 10 V	T_J = –40°C to +125°C	272	310	368	µA
	Ramp Current 2	V_{IN} = 10 V, V_{OUT} = 10 V	T_J = –40°C to +125°C	36	50	64	µA
PWM COMPARATOR							
	Forced Off-time	T_J = –40°C to +125°C		416	500	575	ns
	Min On-time				80		ns
	COMP to PWM Comparator Offset				0.7		V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are assured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

at T_J = 25°C, and V_{IN} = 24 V, R_T = 32.4 kΩ (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ERROR AMPLIFIER							
Feedback Voltage		Vfb = COMP	T_J = –40°C to +125°C	1.207	1.225	1.243	V
FB Bias Current					17		nA
DC Gain					70		dB
COMP Sink / Source Current		T_J = –40°C to +125°C		3			mA
Unity Gain Bandwidth					3		MHz
DIODE SENSE RESISTANCE							
D_{SENSE}					83		mΩ
THERMAL SHUTDOWN							
Tsd	Thermal Shutdown Threshold				165		°C
	Thermal Shutdown Hysteresis				25		°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buck Switch Rds(on)	T_J = –40°C to +125°C		330	660	mΩ
BOOST UVLO			4		V
BOOST UVLO Hysteresis			0.56		V
Pre-charge Switch Rds(on)			70		Ω
Pre-charge Switch on-time			250		ns

6.7 Typical Characteristics

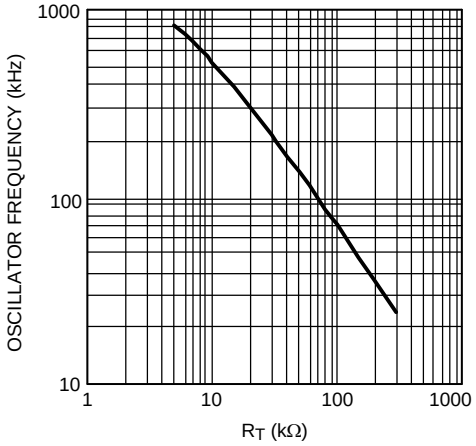

Figure 1. Oscillator Frequency vs R_T

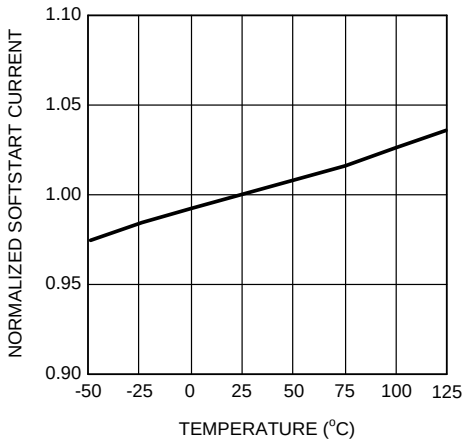

Figure 2. Soft Start Current vs Temperature

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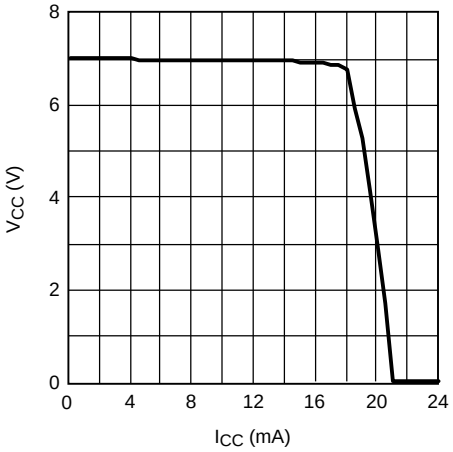
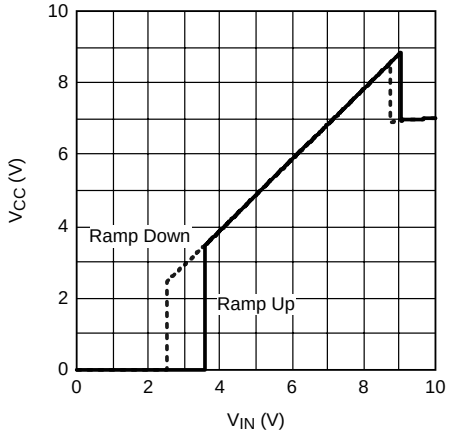
Typical Characteristics (continued)



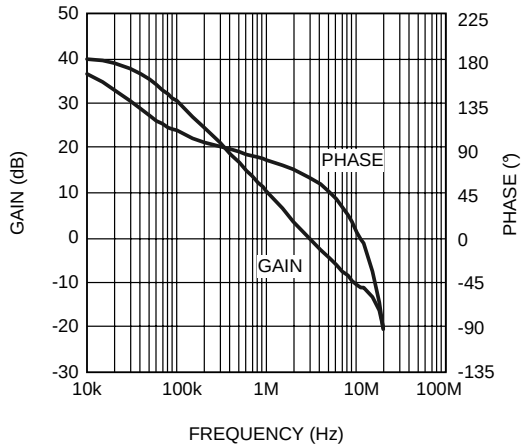
V_{IN} = 12 V

Figure 3. V_{CC} vs I_{CC}



R_L = 7 kΩ

Figure 4. V_{CC} vs V_{IN}



A_{VCL} = 101

Figure 5. Error Amplifier Gain and Phase

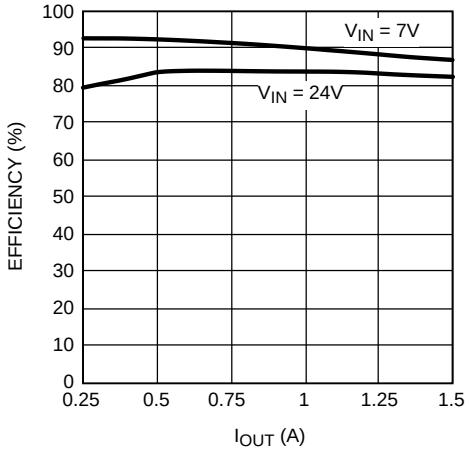


Figure 6. Demoboard Efficiency vs I_{OUT} and V_{IN}

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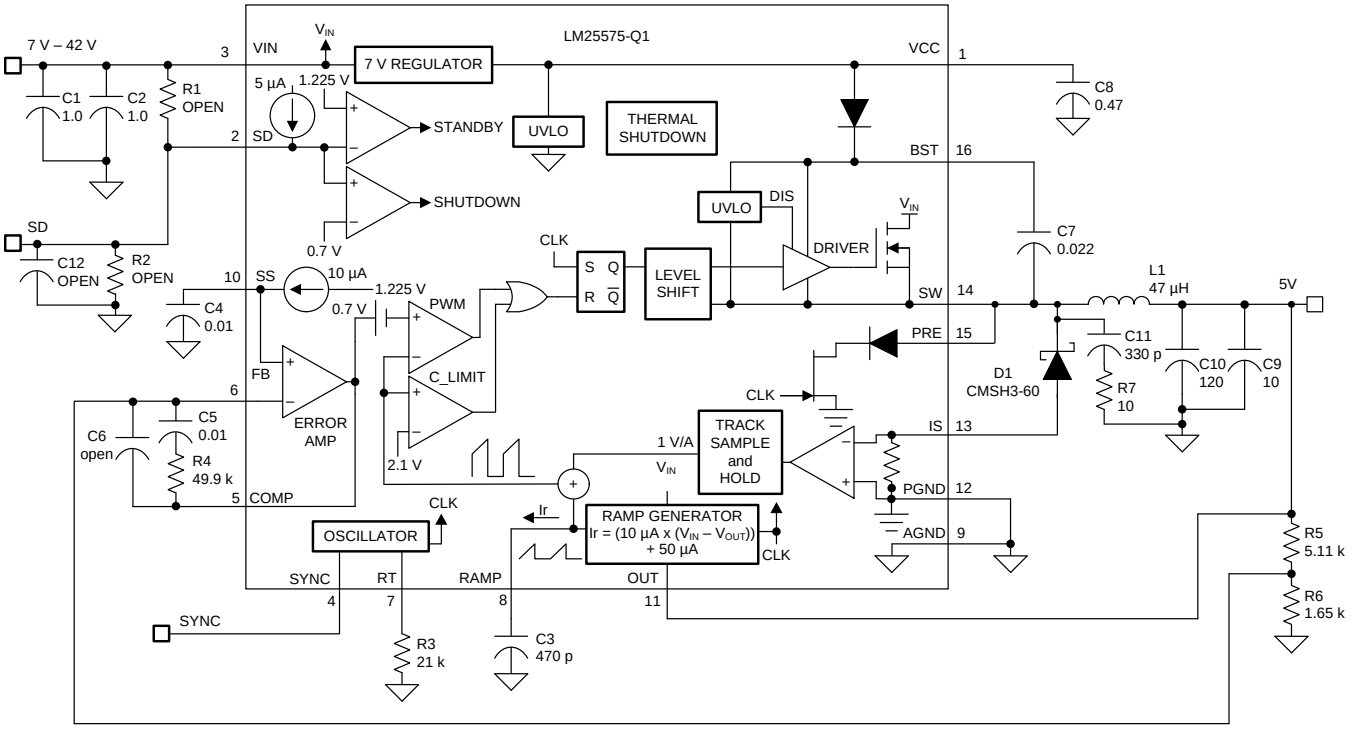
7 Detailed Description

7.1 Overview

The LM25575-Q1 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 42-V N-Channel buck switch with an output current capability of 1.5 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 1 MHz. An oscillator synchronization pin allows multiple LM25575-Q1 regulators to self synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225 V. Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the HTSSOP-16 package featuring an exposed pad to aid thermal dissipation.

The functional block diagram and typical application of the LM25575-Q1 are shown in *Functional Block Diagram*. The LM25575-Q1 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator

The LM25575-Q1 contains a dual-mode internal high voltage startup regulator that provides the V_{CC} bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (VIN) can be connected directly to the input voltage, as high as 42 Volts. For input voltages below 9 V, a low dropout switch connects V_{CC} directly to V_{IN}. In this supply range, V_{CC} is approximately equal to V_{IN}. For V_{IN} voltage greater than 9 V, the low dropout switch is disabled and the V_{CC} regulator is enabled to maintain V_{CC} at approximately 7 V. The wide operating range of 6 V to 42 V is achieved through the use of this dual mode regulator.

Feature Description (continued)

The output of the V_{CC} regulator is current limited to 25 mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the V_{CC} UVLO threshold of 5.35 V and the SD pin is greater than 1.225 V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until V_{CC} falls below 5 V or the SD pin falls below 1.125 V.

An auxiliary supply voltage can be applied to the V_{CC} pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3 V, the internal regulator will essentially shut off, reducing the IC power dissipation. The V_{CC} regulator series pass transistor includes a diode between V_{CC} and V_{IN} that should not be forward biased in normal operation. Therefore the auxiliary V_{CC} voltage should never exceed the V_{IN} voltage.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 45 V. During line or load transients, voltage ringing on the V_{IN} line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

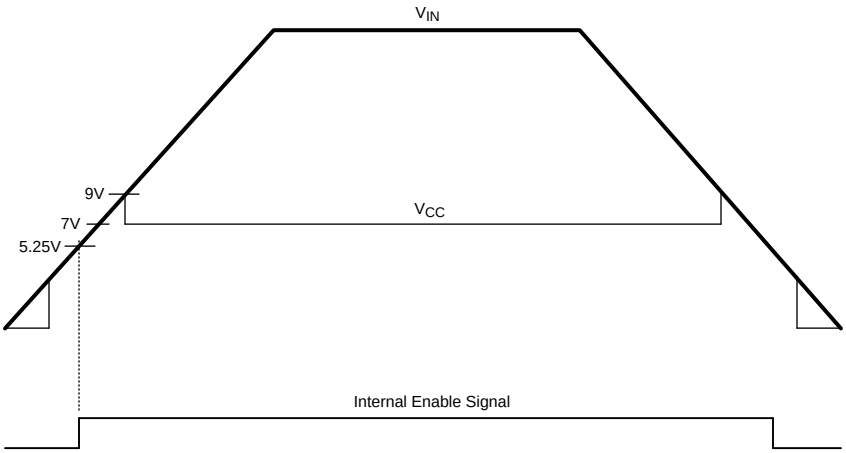

Figure 7. V_{IN} and V_{CC} Sequencing

7.4 Device Functional Modes

7.4.1 Shutdown and Stand-by Mode

The LM25575-Q1 contains a dual level Shutdown (SD) circuit. When the SD pin voltage is below 0.7 V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7 V but less than 1.225 V, the regulator is in standby mode. In standby mode the V_{CC} regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225 V, the output switch is enabled and normal operation begins. An internal 5 µA pull-up current source configures the regulator to be fully operational if the SD pin is left open.

An external set-point voltage divider from VIN to GND can be used to set the operational input range of the regulator. The divider must be designed such that the voltage at the SD pin will be greater than 1.225 V when V_{IN} is in the desired operating range. The internal 5 µA pull-up current source must be included in calculations of the external set-point divider. Hysteresis of 0.1 V is included for both the shutdown and standby thresholds. The SD pin is internally clamped with a 1 kΩ resistor and an 8 V zener clamp. The voltage at the SD pin should never exceed 14 V. If the voltage at the SD pin exceeds 8 V, the bias current will increase at a rate of 1 mA/V.

The SD pin can also be used to implement various remote enable and disable functions. Pulling the SD pin below the 0.7 V threshold totally disables the controller. If the SD pin voltage is above 1.225 V the regulator will be operational.

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Device Functional Modes (continued)

7.4.2 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225 V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network, as illustrated in *Functional Block Diagram*. This network creates a pole at DC, a zero and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

7.4.3 Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulsewidth. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulsewidths and duty cycles is necessary for regulation. The LM25575-Q1 utilizes a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample and hold DC level and an emulated current ramp.

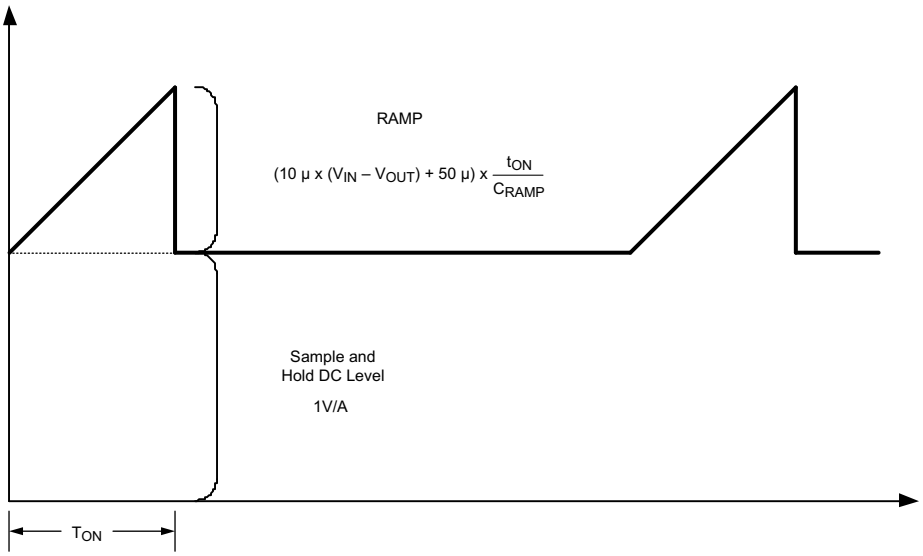

Figure 8. Composition of Current Sense Signal

The sample and hold DC level illustrated in Figure 8 is derived from a measurement of the re-circulating Schottky diode anode current. The re-circulating diode anode should be connected to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample & hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the V_{IN} and V_{OUT} voltages per Equation 1:

$$I_{RAMP} = (10\ \mu \times (V_{IN} - V_{OUT})) + 50\ \mu A \quad (1)$$

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Device Functional Modes (continued)

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. The value of C_{RAMP} can be selected from: $C_{RAMP} = L \times 10^{-5}$, where L is the value of the output inductor in Henrys. With this value, the scale factor of the emulated current ramp will be approximately equal to the scale factor of the DC level sample and hold (1.0 V / A). The C_{RAMP} capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 50 µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, additional slope may be required. In these applications, a pull-up resistor may be added between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5 V:

Calculate optimal slope current, $I_{OS} = V_{OUT} \times 10$ µA/V.

For example, at V_{OUT} = 10 V, I_{OS} = 100 µA.

Install a resistor from the RAMP pin to V_{CC}:

$R_{RAMP} = V_{CC} / (I_{OS} - 50\ \mu A)$

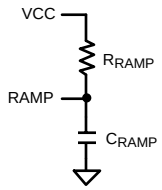

Figure 9. R_{RAMP} to V_{CC} for V_{OUT} > 7.5 V

7.4.4 Maximum Duty Cycle and Input Drop-out Voltage

There is a forced off-time of 500 ns implemented each cycle to ensure sufficient time for the diode current to be sampled. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle will vary with the operating frequency.

$$D_{MAX} = 1 - Fs \times 500\ ns \quad (2)$$

Where Fs is the oscillator frequency. Limiting the maximum duty cycle will raise the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. An approximation of the input dropout voltage is:

$$Vin_{MIN} = \frac{Vout + V_D}{1 - Fs \times 500\ ns} \quad (3)$$

Where V_D is the voltage drop across the re-circulatory diode. Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

7.4.5 Current Limit

The LM25575-Q1 contains a unique current monitoring scheme for control and over-current protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 1.0 V / A. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 2.1 V (2.1 A) the present current cycle is terminated (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the diode current

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Device Functional Modes (continued)

sampling circuit will detect the excess inductor current during the off-time of the buck switch. If the sample & hold DC level exceeds the 2.1 V current limit threshold, the buck switch will be disabled and skip pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

7.4.6 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10 µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage is connected to the reference input of the error amplifier. Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (over-temperature, V_{CC} UVLO, SD) the soft-start capacitor will be discharged. When the fault condition is no longer present a new soft-start sequence will commence.

7.4.7 Boost Pin

The LM25575-Q1 integrates an N-Channel buck switch and associated floating high voltage level shift / gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022 µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately –0.5 V and the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 500 ns to ensure that the bootstrap capacitor is recharged.

Under very light load conditions or when the output voltage is pre-charged, the SW voltage will not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor will not receive sufficient voltage to operate the buck switch gate driver. For these applications, the PRE pin can be connected to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 250 ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current will flow through the pre-charge MOSFET/diode.

7.4.8 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 External Components

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 1. The circuit shown in *Functional Block Diagram* is configured for the following specifications:

- V_{OUT} = 5 V
- V_{IN} = 7 V to 42 V
- Fs = 300 kHz
- Minimum load current (for CCM) = 200 mA
- Maximum load current = 1.5 A

8.1.2 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 300 kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300 kHz switching frequency can be calculated Equation 4:

$$R_T = \frac{[(1 / 300 \times 10^3) - 580 \times 10^{-9}]}{135 \times 10^{-12}} \quad (4)$$

The nearest standard value of 21 kΩ was chosen for R_T.

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Application Information (continued)

8.1.3 L1

The inductor value is determined based on the operating frequency, load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$).

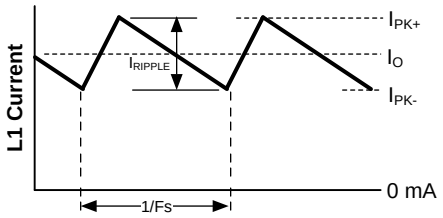

Figure 10. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} should be less than twice the minimum load current, or 0.4 Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \text{ x } (V_{IN(max)} - V_{OUT})}{I_{RIPPLE} \text{ x } F_S \text{ x } V_{IN(max)}} \quad (5)$$

$$L1 = \frac{5V \text{ x } (42V - 5V)}{0.4A \text{ x } 300 \text{ kHz x } 42V} = 37 \text{ µH} \quad (6)$$

This procedure provides a guide to select the value of L1. The nearest standard value (47µH) will be used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 2.1 A nominal (2.5 A maximum). The selected inductor (see Table 1) has a conservative 3.25 Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

8.1.4 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is:

$$C_{RAMP} = L \times 10^{-5} \quad (7)$$

Where L is in Henrys

With L1 selected for 47 µH the recommended value for C3 is 470 pF.

8.1.5 C9, C10

The output capacitors, C9 and C10, smooth the inductor ripple current and provide a source of charge for transient loading conditions. For this design a 10 µF ceramic capacitor and a 120 µF AL organic capacitor were selected. The ceramic capacitor provides ultra low ESR to reduce the output ripple voltage and noise spikes, while the AL capacitor provides a large bulk capacitance in a small volume for transient loading conditions. An approximation for the output ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times F_S \times C_{OUT}} \right) \quad (8)$$

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Application Information (continued)

8.1.6 D1

A Schottky type re-circulating diode is required for all LM25575-Q1 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM25575-Q1. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. The reverse breakdown rating should be selected for the maximum V_{IN}, plus some safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. “Rated” current for diodes vary widely from various manufacturers. The worst case is to assume a short circuit load condition. In this case the diode will carry the output current almost continuously. For the LM25575-Q1 this current can be as high as 2.1 A. Assuming a worst case 1 V drop across the diode, the maximum diode power dissipation can be as high as 2.1 W. For the reference design a 60 V Schottky in a SMC package was selected.

8.1.7 C1, C2

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage effects, two 1.0 µF, 100 V ceramic capacitors will be used. If step input voltage transients are expected near the maximum rating of the LM25575-Q1, a careful evaluation of ringing and possible spikes at the device VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

8.1.8 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. A value of 0.47 µF was selected for this design.

8.1.9 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022 µF, and should be a good quality, low ESR, ceramic capacitor.

8.1.10 C4

The capacitor at the SS pin determines the soft-start time, that is the time for the reference voltage and the output voltage, to reach the final regulated value. The time is determined from Equation 9:

$$t_{ss} = \frac{C4 \times 1.225V}{10\ \mu A} \quad (9)$$

For this application, a C4 value of 0.01 µF was chosen which corresponds to a soft-start time of 1 ms.

8.1.11 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated from Equation 10:

$$R5/R6 = (V_{OUT} / 1.225\ V) - 1 \quad (10)$$

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Application Information (continued)

For a 5 V output, the R5 and R6 ratio calculates to 3.082. The resistors should be chosen from standard value resistors, a good starting point is selection in the range of 1.0 kΩ - 10 kΩ. Values of 5.11 kΩ for R5, and 1.65 kΩ for R6 were selected.

8.1.12 R1, R2, C12

A voltage divider can be connected to the SD pin to set a minimum operating voltage $V_{IN(min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (between 10 kΩ and 100 kΩ recommended) then calculate R2 from Equation 11:

$$R2 = 1.225 \times \left(\frac{R1}{V_{IN(min)} + (5 \times 10^{-6} \times R1) - 1.225} \right) \quad (11)$$

Capacitor C12 provides filtering for the divider. The voltage at the SD pin should never exceed 8 V, when using an external set-point divider it may be necessary to clamp the SD pin at high input voltage conditions. The reference design utilizes the full range of the LM25575-Q1 (6 V to 42 V); therefore these components can be omitted. With the SD pin open circuit the LM25575-Q1 responds once the V_{CC} UVLO threshold is satisfied.

8.1.13 R7, C11

A snubber network across the power diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM25575-Q1 or the re-circulating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. For the current levels typical for the LM25575-Q1 a resistor value between 5 Ω and 20 Ω is adequate. Increasing the value of the snubber capacitor results in more damping but higher losses. Select a minimum value of C11 that provides adequate damping of the SW pin waveform at high load.

8.1.14 R4, C5, C6

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM25575-Q1 is as follows:

$$DC\ Gain_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 1 \times R_{LOAD} \quad (12)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD},) and output capacitance (C_{OUT}). The corner frequency of this pole is as follows:

$$f_{p(MOD)} = 1 / (2\pi\ R_{LOAD}\ C_{OUT}) \quad (13)$$

For R_{LOAD} = 5 Ω and C_{OUT} = 130 µF then $f_{p(MOD)}$ = 245 Hz

$DC\ Gain_{(MOD)}$ = 1 × 5 = 14 dB

For the design example of *Functional Block Diagram* the following modulator gain vs. frequency characteristic was measured as shown in Figure 11.

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Application Information (continued)

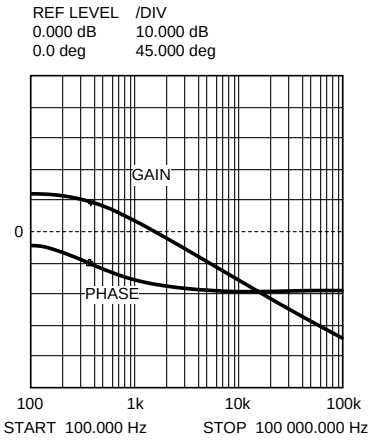

Figure 11. Gain and Phase of Modulator R_{LOAD} = 5 Ohms and C_{OUT} = 130 µF

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 / (2πR4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 15 kHz was selected. The compensation network zero (f_Z) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 / (2π R4 C5) to be less than 2 kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example C5 was selected for 0.01 µF and R4 was selected for 49.9 kΩ. These values configure the compensation network zero at 320 Hz. The error amp gain at frequencies greater than f_Z is: R4 and R5, which is approximately 10 (20 dB).

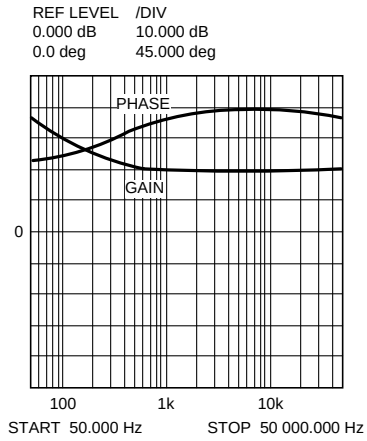

Figure 12. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

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Application Information (continued)

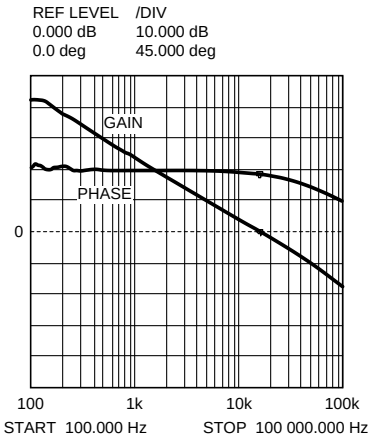

Figure 13. Overall Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C6 can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C6 must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is: f_{p2} = fz × C5 / C6.

8.1.15 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step-down the input voltage V_{IN} to a nominal V_{CC} level of 7 V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the V_{CC} regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 14 and Figure 15 depict two methods to bias the IC from the output voltage. In each case the internal V_{CC} regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7 V regulation level, which effectively disables the internal V_{CC} regulator. The voltage applied to the VCC pin should never exceed 14 V. The V_{CC} voltage should never be larger than the V_{IN} voltage.

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Application Information (continued)

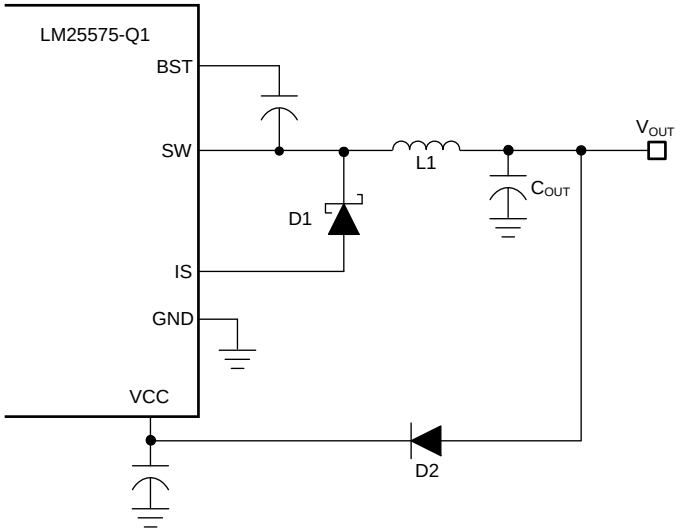

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Figure 14. VCC Bias From VOUT For 8 V < VOUT < 14 V

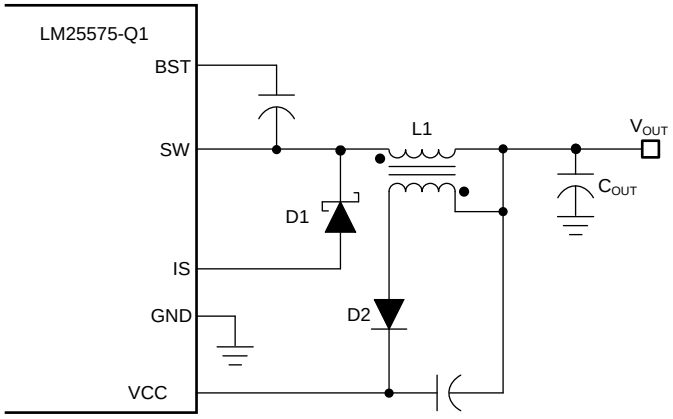

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Figure 15. VCC Bias With Additional Winding on the Output Inductor

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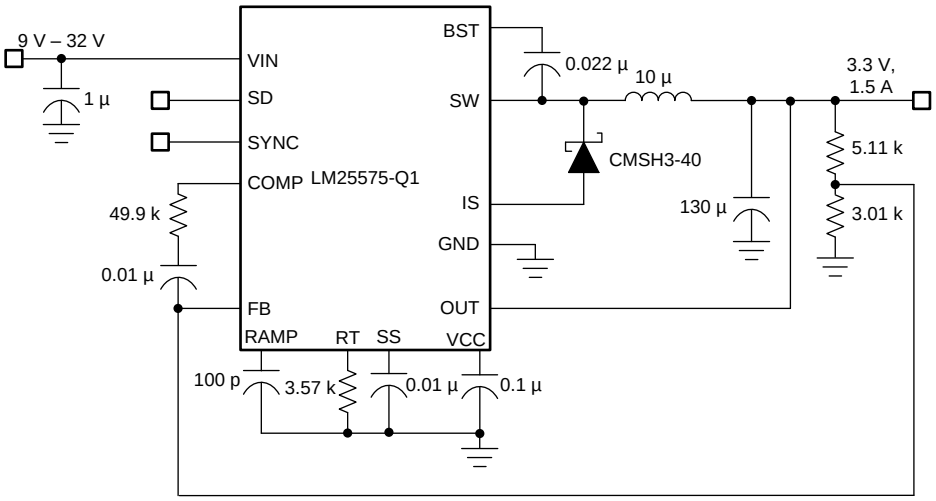
8.2 Typical Application

8.2.1 Typical Schematic for High Frequency (1 MHz) Application



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9 Layout

9.1 Layout Guidelines

9.1.1 PCB Layout and Thermal Considerations

The circuit in *Functional Block Diagram* serves as both a block diagram of the LM25575-Q1 and a typical application board schematic for the LM25575-Q1. In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM25575-Q1 regulator IC. The easiest method to determine the power dissipated within the LM25575-Q1 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. An approximation for the Schottky diode loss is P = (1-D) × Iout × Vfwd. An approximation for the output inductor power is P = I_{OUT}^2 × R × 1.1, where R is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses. If a snubber is used, an approximation for the damping resistor power dissipation is P = V_{IN}^2 × Fsw × Csnub, where Fsw is the switching frequency and Csnub is the snubber capacitor. The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will aid the power dissipation of the diode.

The most significant variables that affect the power dissipated by the LM25575-Q1 are the output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The operating frequency of the LM25575-Q1 evaluation board has been designed for 300 kHz. When operating at 1.5 A output current with a 42 V input the power dissipation of the LM25575-Q1 regulator is approximately 0.9 W.

The junction-to-ambient thermal resistance of the LM25575-Q1 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. Referring to the evaluation board artwork, the area under the LM25575-Q1 (component side) is covered with copper and there are 5 connection vias to the solder side ground plane. Additional vias under the IC will have diminishing value as more vias are added. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM25575-Q1 mounted in the evaluation board varies from 50°C/W with no airflow to 28°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM25575-Q1 will be 25 + (50 × 0.9) = 70°C. If the evaluation board is operated at 1.5 A output current, 70 V input voltage and high ambient temperature for a prolonged period of time the thermal shutdown protection within the IC may activate. The IC will turn off allowing the junction to cool, followed by restart with the soft-start capacitor reset to zero.

Table 1. 5 V, 1.5 A Demo Board Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C3225X7R2A105M	CAPACITOR, CER, TDK	1 µ, 100 V
C	2	C3225X7R2A105M	CAPACITOR, CER, TDK	1 µ, 100 V
C	3	C0805A471K1GAC	CAPACITOR, CER, KEMET	470 p, 100 V
C	4	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01 µ, 100 V
C	5	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01 µ, 100 V
C	6	OPEN	NOT USED	
C	7	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022 µ, 100 V
C	8	C2012X7R1C474M	CAPACITOR, CER, TDK	0.47 µ, 16 V

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Layout Guidelines (continued)

Table 1. 5 V, 1.5 A Demo Board Bill of Materials (continued)

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	9	C3225X7R1C106M	CAPACITOR, CER, TDK	10 µ, 16 V
C	10	APXE6R3ARA121ME61G	CAPACITOR, AL, NIPPON	120 µ, 6.3 V
C	11	C0805C331G1GAC	CAPACITOR, CER, KEMET	330 p, 100 V
C	12	OPEN	NOT USED	
D	1	CMSH3-60	DIODE, 60V, CENTRAL	
L	1	DR125-470	INDUCTOR, COOPER	47 µH
R	1	OPEN	NOT USED	
R	2	OPEN	NOT USED	
R	3	CRCW08052102F	RESISTOR	21 kΩ
R	4	CRCW08054992F	RESISTOR	49.9 kΩ
R	5	CRCW08055111F	RESISTOR	5.11 kΩ
R	6	CRCW08051651F	RESISTOR	1.65 kΩ
R	7	CRCW2512100J	RESISTOR	10, 1 W
U	1	LM25575-Q1	REGULATOR, TEXAS INSTRUMENTS	

9.2 Layout Example

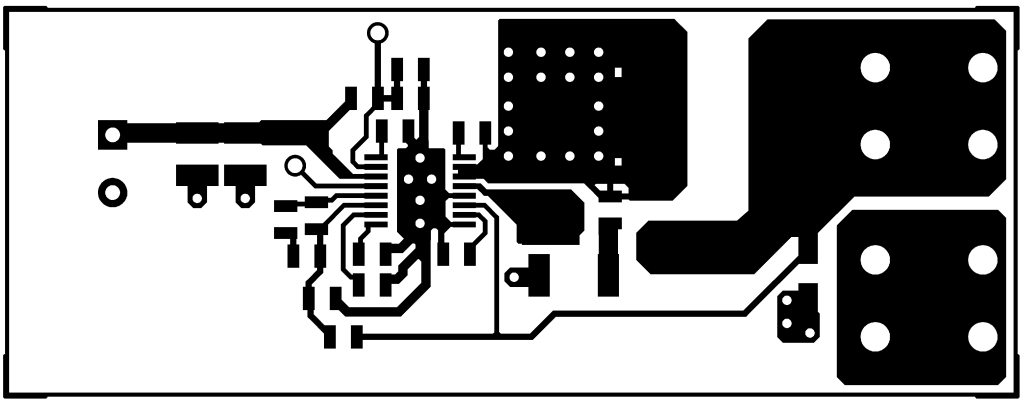

Figure 16. Component Side

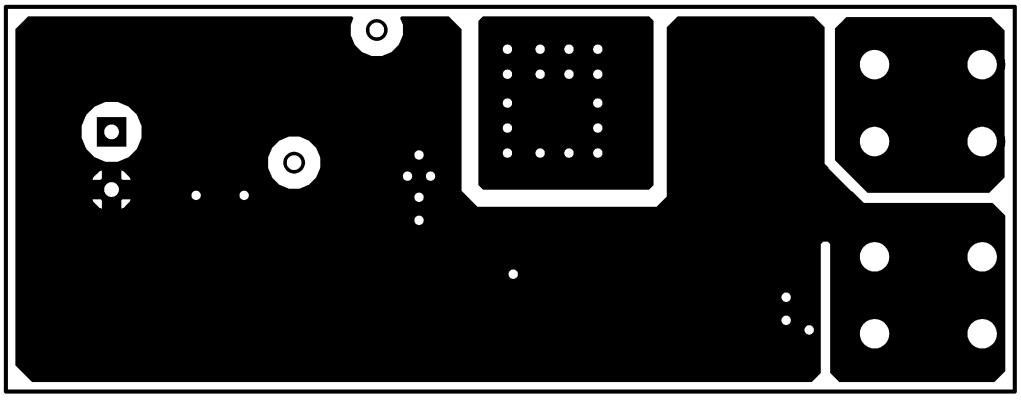

Figure 17. Solder Side

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Layout Example (continued)

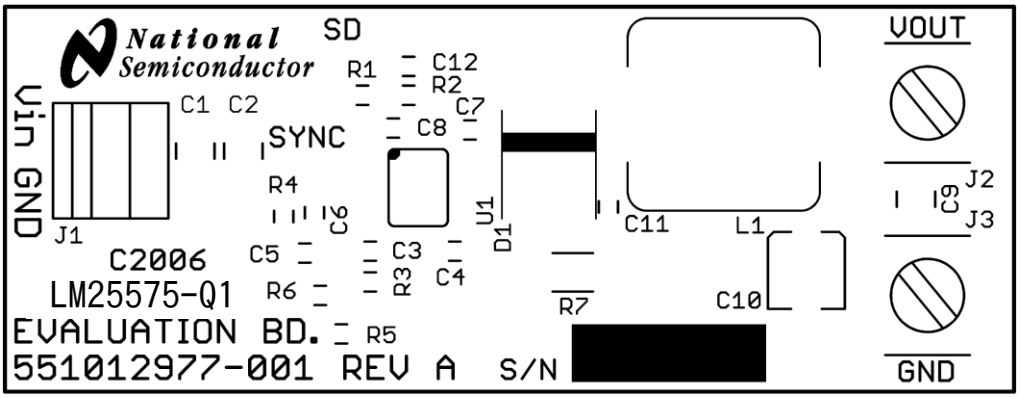

Figure 18. Silkscreen

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10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 開発サポート

10.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LM25575-Q1デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

10.4 商標

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WEBENCH is a registered trademark of Texas Instruments.
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10.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25575QMH/NOPB	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25575 QMH	Samples
LM25575QMHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25575 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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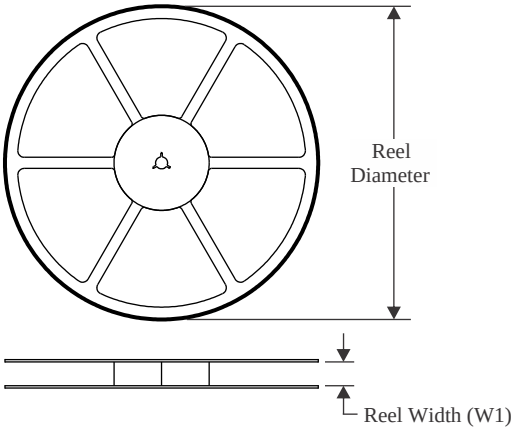
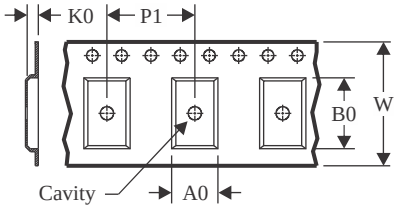
TAPE AND REEL INFORMATION

REEL DIMENSIONS

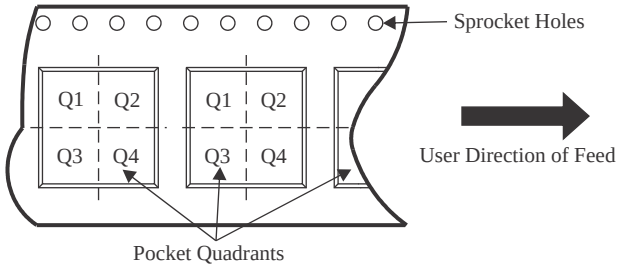


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

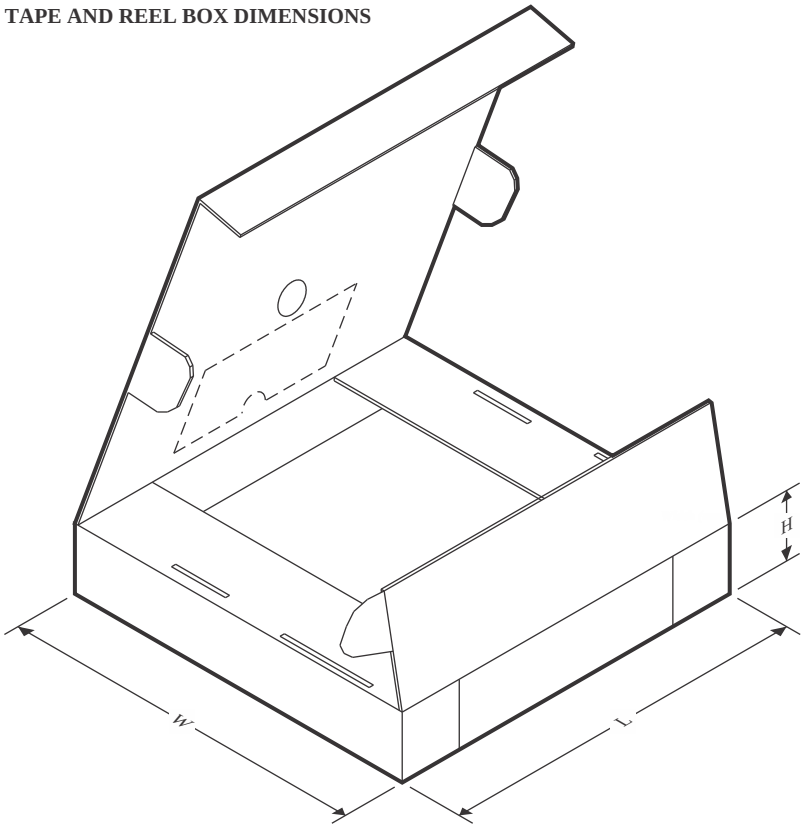
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25575QMHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

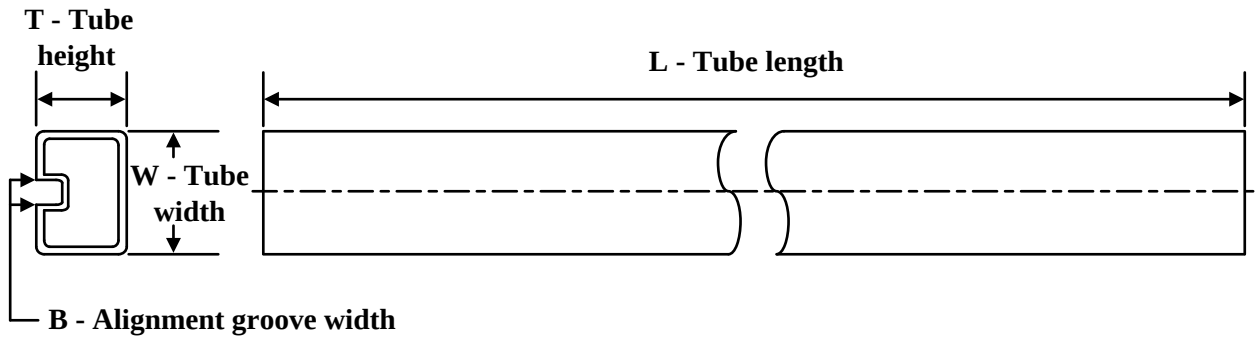
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

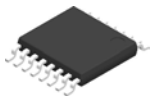
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25575QMHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25575QMH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM25575QMH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06

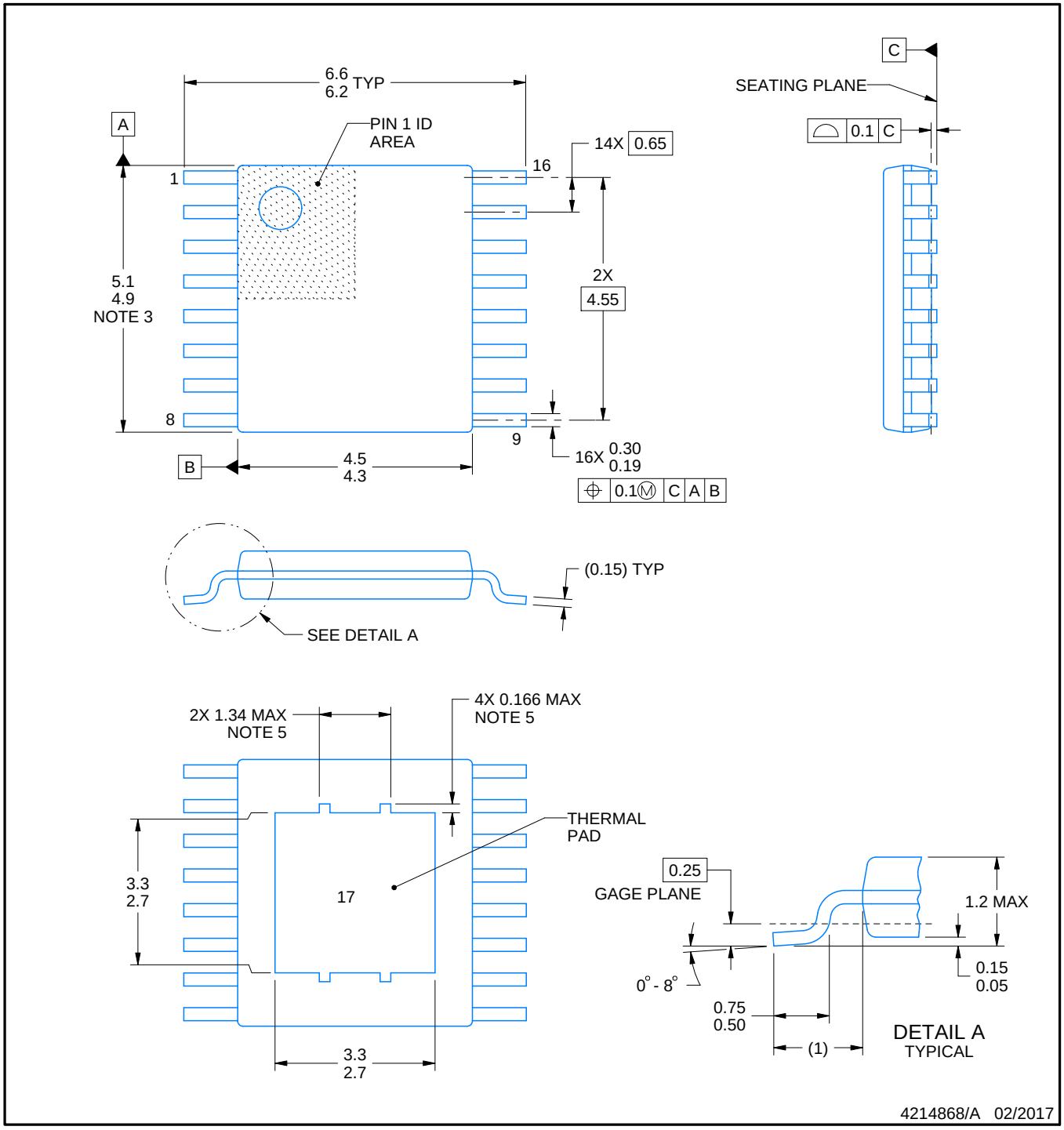


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

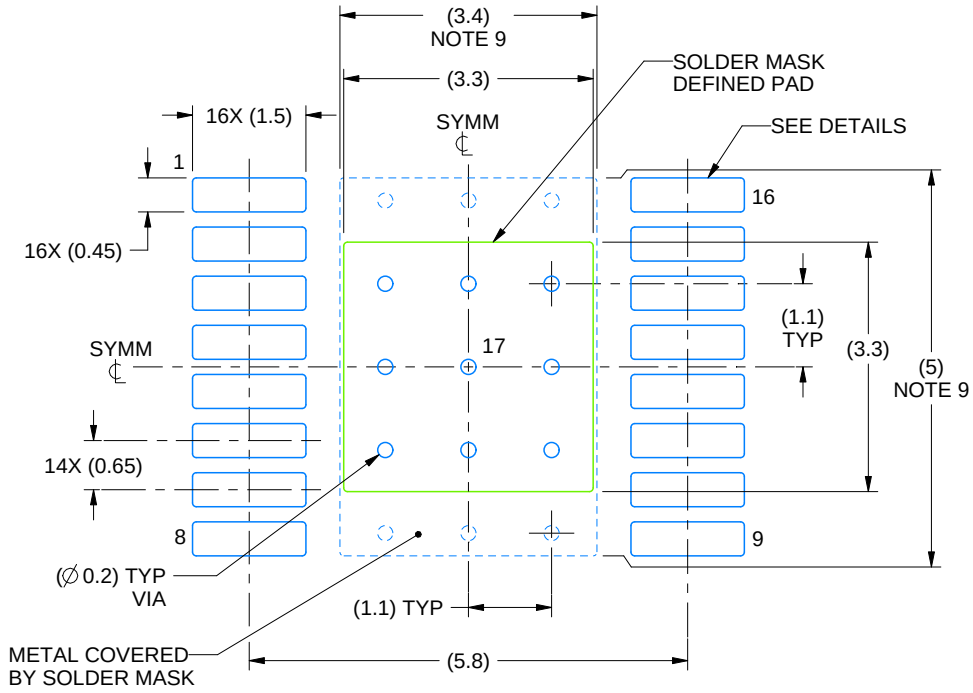
PLASTIC SMALL OUTLINE



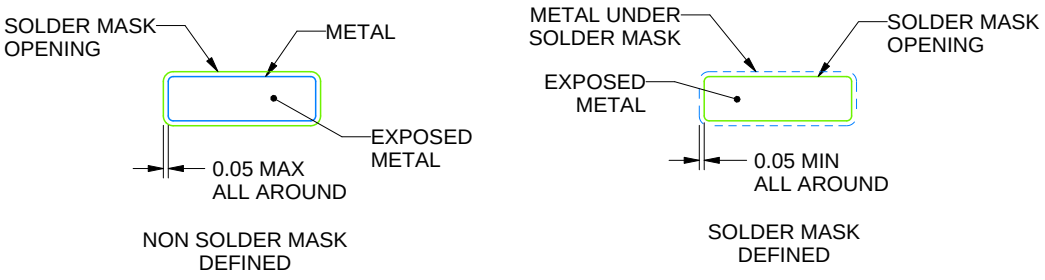
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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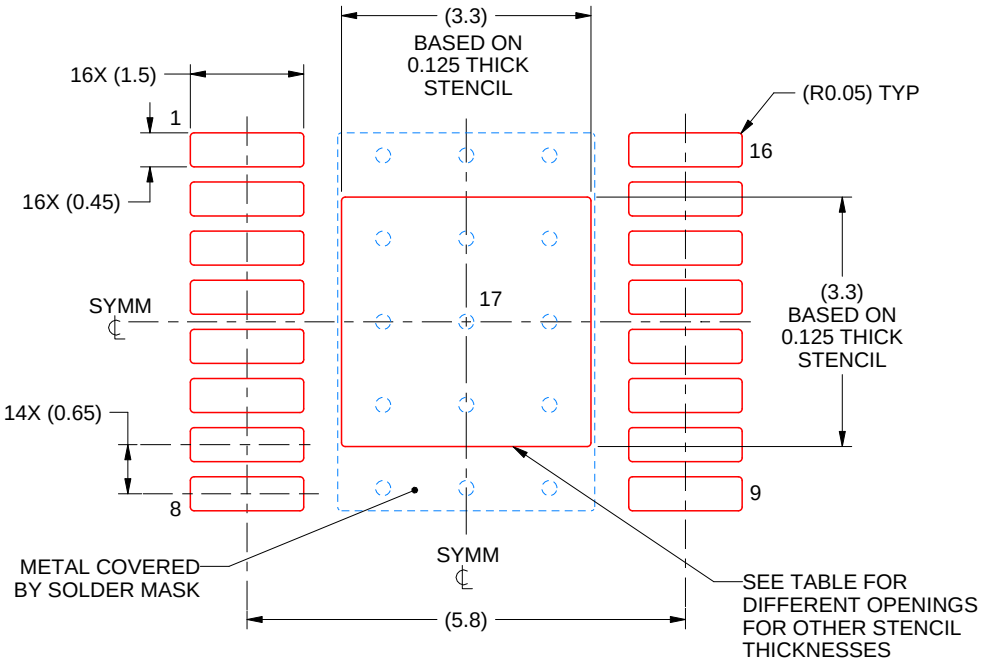
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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