LMC608x 高精度 CMOS デュアル オペアンプ

1 特長

- (特に記述のない限り標準値)
- 低いオフセット電圧:150μV
- 単一電源動作:4.5V～15.5V
- 超低入力バイアス電流:10fA
- 出力スイングは、電源レールから 20mV 以内、2kΩ 負荷
- 入力同相範囲に V- を含む
- 高い電圧ゲイン:123dB、2kΩ 負荷
- ラッチアップ耐性の向上

2 アプリケーション

- 計装アンプ
- フォトダイオードおよび赤外線検出器のプリアンプ
- トランスデューサ アンプ
- 医療用計測装置
- DA コンバータ(DAC)
- 圧電トランスデューサ用チャージ アンプ

3 概要

LMC6081、LMC6082、LMC6084 (LMC608x) は、単一電源動作が可能な高精度、低オフセット電圧のオペアンプです。性能特性としては、きわめて小さい入力バイアス電流、高い電圧ゲイン、レール ツール レールの出力段を備えており、入力同相電圧範囲にグランドが含まれます。これらの特長に加え、オフセット電圧が低いことから、LMC608x は高精度回路アプリケーションに最適です。

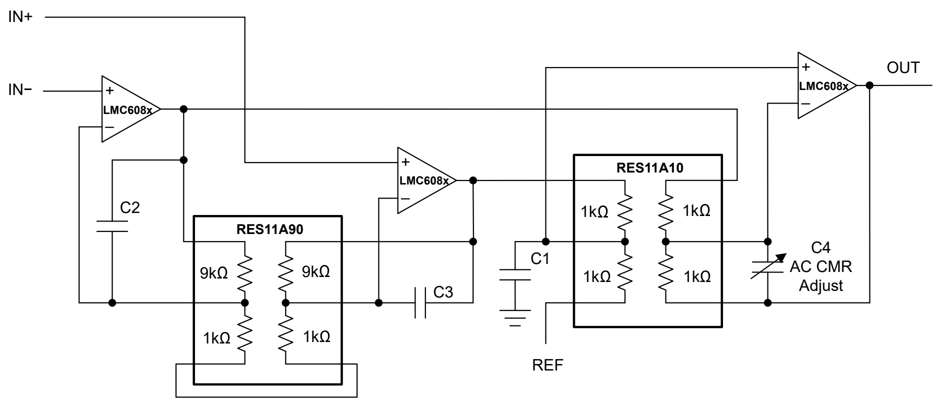
LMC608x を使用する他のアプリケーションには、高精度の全波整流器、積分器、リファレンス、サンプル / ホールド回路があります。

電力要件がより重要な設計については、高精度、デュアル、マイクロパワー オペアンプ LMC6062 をご覧ください。

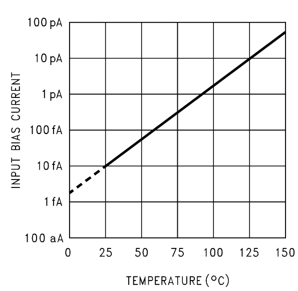
製品情報

部品番号	チャネル数	パッケージ (1)
LMC6081	シングル	D (SOIC、8)
LMC6082	デュアル	D (SOIC、8)
LMC6084	クワッド	D (SOIC、14)

(1) 詳細については、セクション 9 を参照してください。



RES11A を使った計装アンプ



入力バイアス電流と温度との関係

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4 Pin Configuration and Functions

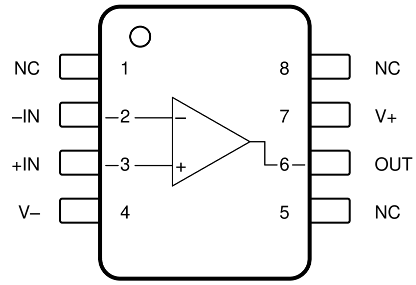


図 4-1. LMC6081 D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP

表 4-1. Pin Functions: LMC6081

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	2	Input	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

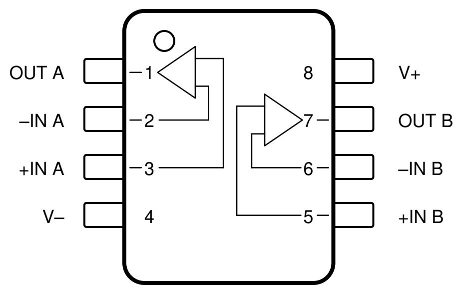


図 4-2. LMC6082 D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP

表 4-2. Pin Functions: LMC6081

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
–IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

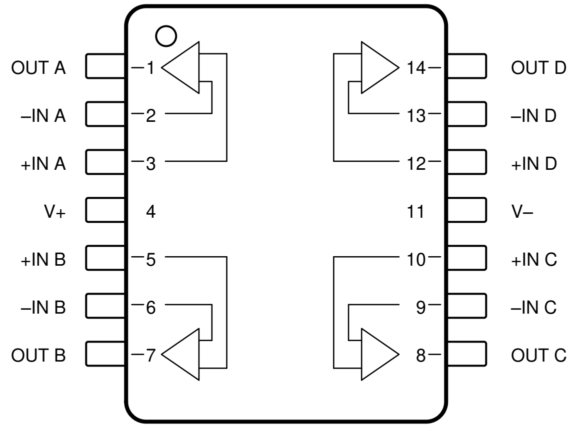


図 4-3. LMC6084 D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP

表 4-3. Pin Functions: LMC6084

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Differential input voltage range			±Supply voltage	V
Supply voltage, V_S = (V+) – (V–)	Single supply	0	16	V
	Dual supply		±8	
Output short circuit	To V+		See[(3)]	mA
	To V–		See[(4)]	
Signal input pins	Voltage	(V–) – 0.3	(V+) + 0.3	V
	Current		±10	mA
Output pin current			±30	mA
Power supply pin current			40	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	
Power dissipation			See[(5)]	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Do not connect output to V+, when V+ is greater than 13V or reliability is adversely affected.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} − T_A) /θ_{JA}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single supply	4.5		15.5	V
	Dual supply	±2.25		±7.75	
Temperature range, T_J		–40		85	°C
Power dissipation				See[(1)]	

(1) For operating at elevated temperatures, the device must be derated based on the thermal resistance $θ_{JA}$ with $P_D = (T_J − T_A) / θ_{JA}$. All numbers apply for packages soldered directly into a printed circuit board.

5.4 Thermal Information LMC6081

THERMAL METRIC[(1)]		LMC6081		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	115	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information LMC6082

THERMAL METRIC[(1)]		LMC6082		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	115	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information LMC6084

THERMAL METRIC[(1)]		LMC6084		UNIT
		D (SOIC)	P(PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126	81	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics

at T_A = 25°C, V_S = 5V (V– = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LMC608xAI			±150	±350	µV
			T_A = –40°C to +85°C			±800	
		LMC608xI			±150	±800	
			T_A = –40°C to +85°C			±1300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			1		µV/°C
PSRR	Power-supply rejection ratio	Positive 5V ≤ V_{CM} ≤ 15V	LMC608xAI	75	85		dB
			LMC608xAI T_A = –40°C to +85°C	72			
			LMC608xI	66	85		
			LMC608xI T_A = –40°C to +85°C	63			
		Negative –10V ≤ V_{CM} ≤ 0V	LMC608xAI	84	94		
			LMC608xAI T_A = –40°C to +85°C	81			
			LMC608xI	74	94		
			LMC608xI T_A = –40°C to +85°C	71			
INPUT BIAS CURRENT							
I_B	Input bias current				±10		fA
		T_A = –40°C to +85°C				±4	pA
I_{OS}	Input offset current				±5		fA
		T_A = –40°C to +85°C				±2	pA
NOISE							
e_n	Input voltage noise density	f = 1kHz			22		nV/√Hz
i_n	Input current noise density	f = 1kHz			4		fA/√Hz
THD	Total harmonic distortion	f= 10kHz, G = – 10V/V, R_L = 2kΩ, V_{OUT} = $8V_{pp}$, V_S = ±5V			0.2		%
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	To positive rail 5V ≤ V_S ≤ 15V, CMRR > 60dB			(V+) – 1.9	(V+) – 2.3	V
			T_A = –40°C to +85°C			(V+) – 2.5	
		To negative rail 5V ≤ V_S ≤ 15V, CMRR > 60dB		(V–) – 0.1	(V–) – 0.4		
			T_A = –40°C to +85°C	(V–)			
CMRR	Common-mode rejection ratio	V_S = 15V, 0V < V_{CM} < 12V	LMC608xAI	75	85		dB
			LMC608xAI, T_A = –40°C to +85°C	72			
			LMC608xI	66	85		
			LMC608xI, T_A = –40°C to +85°C	63			
INPUT IMPEDANCE							
R_{IN}	Input resistance				10		TΩ

5.7 Electrical Characteristics (続き)

at T_A = 25°C, V_S = 5V (V– = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing, V_S = 15V, V_{CM} = 7.5V, 7.5V < V_O < 11.5V, R_L = 2kΩ	LMC608xAI	400	1400		V/mV
			LMC608xAI, T_A = –40°C to +85°C	300			
			LMC608xI	300	1400		
			LMC608xI, T_A = –40°C to +85°C	200			
		Sinking, V_S = 15V, V_{CM} = 7.5V, 2.5V < V_O < 7.5V, R_L = 2kΩ	LMC608xAI	180	350		
			LMC608xAI, T_A = –40°C to +85°C	100			
			LMC608xI	90	350		
			LMC608xI, T_A = –40°C to +85°C	60			
		Sourcing, V_S = 15V, V_{CM} = 7.5V, 7.5V < V_O < 11.5V, R_L = 600Ω	LMC608xAI	400	1200		
			LMC608xAI, T_A = –40°C to +85°C	150			
			LMC608xI	200	1200		
			LMC608xI, T_A = –40°C to +85°C	80			
		Sinking, V_S = 15V, V_{CM} = 7.5V, 2.5V < V_O < 7.5V, R_L = 600Ω	LMC608xAI	100	150		
			LMC608xAI, T_A = –40°C to +85°C	50			
			LMC608xI	70	150		
			LMC608xI, T_A = –40°C to +85°C	35			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.3		MHz
SR	Slew rate[(2)]	V_S = 15V, 10V step		0.8	1.5		V/µs
			T_A = –40°C to +85°C	0.6			
θ_m	Phase margin				50		°
	Crosstalk	Dual and quad channel, V_S = 15V, R_L = 100kΩ to 7.5V, f = 1kHz, V_{OUT} = 12V_{pp}			140		dB

5.7 Electrical Characteristics (続き)

at T_A = 25°C, V_S = 5V (V– = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing	Positive rail V_S = 5V, R_L = 2kΩ	LMC608xAI	4.80	4.87		V
			LMC608xAI, T_A = –40°C to +85°C	4.73			
			LMC608xI	4.75	4.87		
			LMC608xI, T_A = –40°C to +85°C	4.67			
		Negative rail V_S = 5V, R_L = 2kΩ	LMC608xAI		0.10	0.13	
			LMC608xAI, T_A = –40°C to +85°C			0.17	
			LMC608xI		0.10	0.20	
			LMC608xI, T_A = –40°C to +85°C			0.24	
		Positive rail V_S = 5V, R_L = 600Ω	LMC608xAI	4.50	4.61		
			LMC608xAI, T_A = –40°C to +85°C	4.31			
			LMC608xI	4.50	4.61		
			LMC608xI, T_A = –40°C to +85°C	4.21			
		Negative rail V_S = 5V, R_L = 600Ω	LMC608xAI		0.30	0.40	
			LMC608xAI, T_A = –40°C to +85°C			0.50	
			LMC608xI		0.30	0.50	
			LMC608xI, T_A = –40°C to +85°C			0.63	
		Positive rail V_S = 15V, R_L = 2kΩ	LMC608xAI	14.50	14.63		
			LMC608xAI, T_A = –40°C to +85°C	14.34			
			LMC608xI	14.37	14.63		
			LMC608xI, T_A = –40°C to +85°C	14.25			
		Negative rail V_S = 15V, R_L = 2kΩ	LMC608xAI		0.26	0.35	
			LMC608xAI, T_A = –40°C to +85°C			0.45	
			LMC608xI		0.26	0.44	
			LMC608xI, T_A = –40°C to +85°C			0.56	
		Positive rail V_S = 15V, R_L = 600Ω	LMC608xAI	13.35	13.90		
			LMC608xAI, T_A = –40°C to +85°C	12.86			
			LMC608xI	14.37	13.90		
			LMC608xI, T_A = –40°C to +85°C	14.25			
		Negative rail V_S = 15V, R_L = 600Ω	LMC608xAI		0.79	1.16	
			LMC608xAI, T_A = –40°C to +85°C			1.32	
			LMC608xI		0.79	1.33	
			LMC608xI, T_A = –40°C to +85°C			1.58	

5.7 Electrical Characteristics (続き)

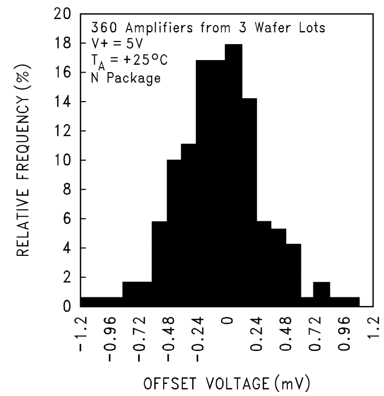
at T_A = 25°C, V_S = 5V (V– = 0V), V_{CM} = 1.5V, V_{OUT} = V_S / 2, and R_L = 1MΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	Sourcing V_S = 5V, V_{OUT} = 0V	LMC608xAI	16	22		mA
			LMC608xAI, T_A = –40°C to +85°C	10			
			LMC608xI	13	22		
			LMC608xI, T_A = –40°C to +85°C	8			
		Sinking V_S = 5V, V_{OUT} = 5V	LMC608xAI	16	21		
			LMC608xAI, T_A = –40°C to +85°C	13			
			LMC608xI	13	21		
			LMC608xI, T_A = –40°C to +85°C	10			
		Sourcing V_S = 15V, V_{OUT} = 0V	LMC608xAI	28	30		
			LMC608xAI, T_A = –40°C to +85°C	22			
			LMC608xI	23	30		
			LMC608xI, T_A = –40°C to +85°C	18			
		Sinking V_S = 15V, V_{OUT} = 13V(1)	LMC608xAI	28	34		
			LMC608xAI, T_A = –40°C to +85°C	22			
			LMC608xI	23	34		
			LMC608xI, T_A = –40°C to +85°C	18			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{OUT} = 1.5V, V_S = 5V			0.45	0.75	mA
			T_A = –40°C to +85°C			0.9	
		V_{OUT} = 7.5V, V_S = 15V LMC6082, LMC6084			0.55	0.85	
			T_A = –40°C to +85°C			1	
		V_{OUT} = 7.5V, V_S = 15V LMC6081			0.55	0.85	
			T_A = –40°C to +85°C			0.95	

(1) Do not connect output to V+, when V+ is greater than 13V or reliability is adversely affected.
(2) Specification limit established from device population bench system measurements across multiple lots. Number specified is the slower of the positive and negative slew rates.

5.8 Typical Characteristics

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L≥ 1MΩ (unless otherwise specified)



T_A = 25°C

図 5-1. Distribution of LMC6082 Input Offset Voltage

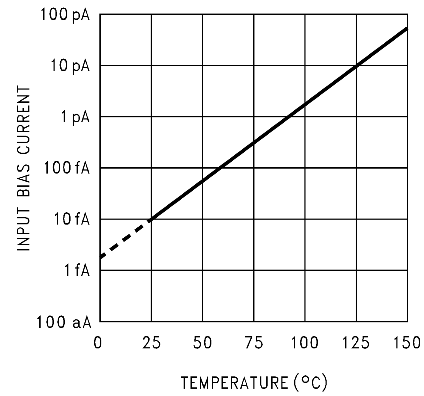


図 5-2. Input Bias Current vs Temperature

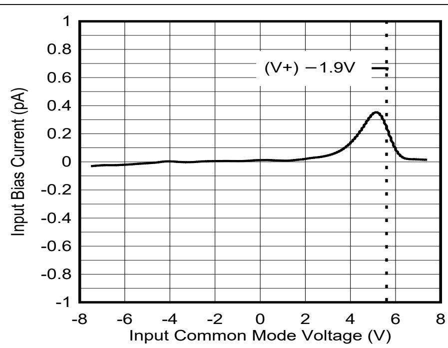


図 5-3. Input Bias Current vs Common-Mode Voltage

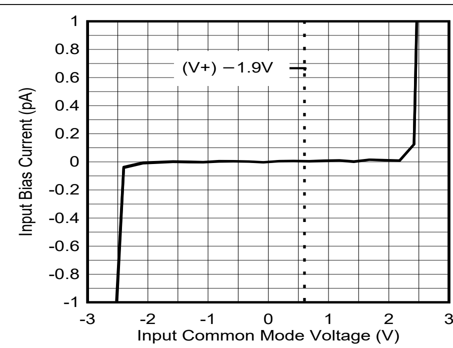


図 5-4. Input Bias Current vs Common-Mode Voltage

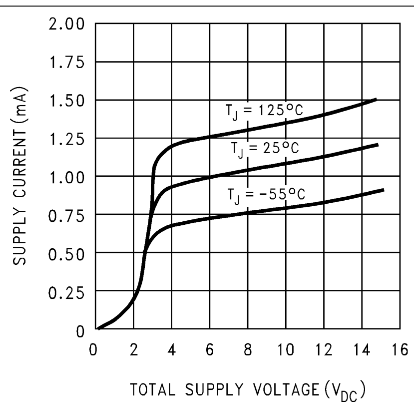


図 5-5. Supply Current vs Supply Voltage

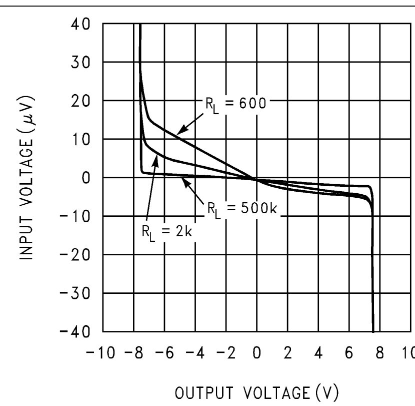


図 5-6. Input Voltage vs Output Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L≥ 1MΩ (unless otherwise specified)

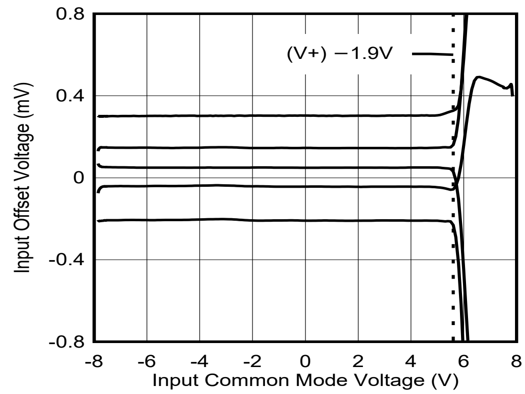


図 5-7. Input Offset Voltage vs Common Mode Voltage

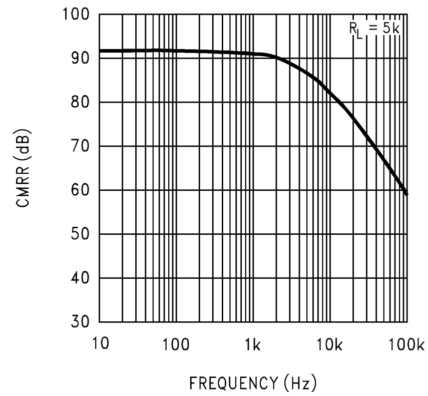


図 5-8. Common Mode Rejection Ratio vs Frequency

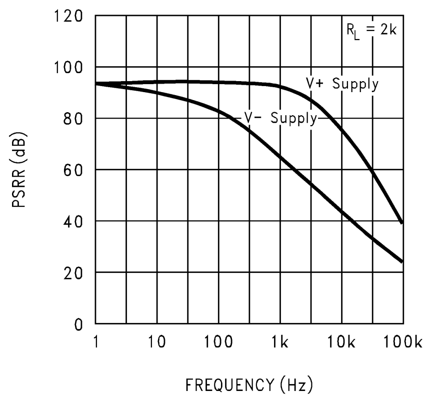


図 5-9. Power Supply Rejection Ratio vs Frequency

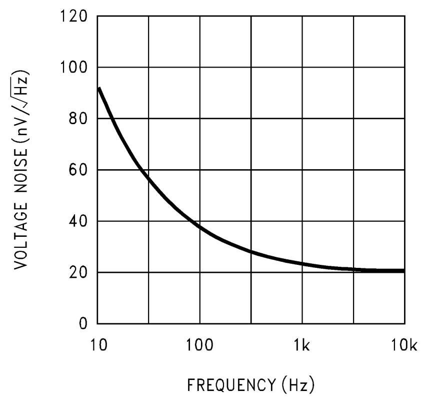


図 5-10. Input Voltage Noise vs Frequency

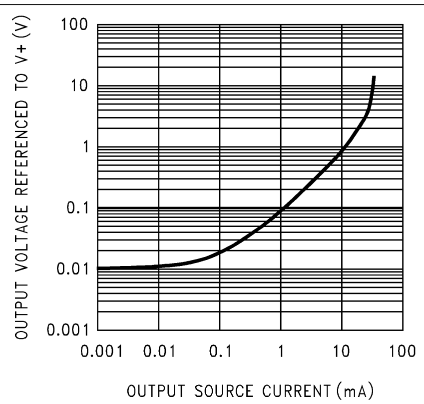


図 5-11. Output Characteristics Sourcing Current

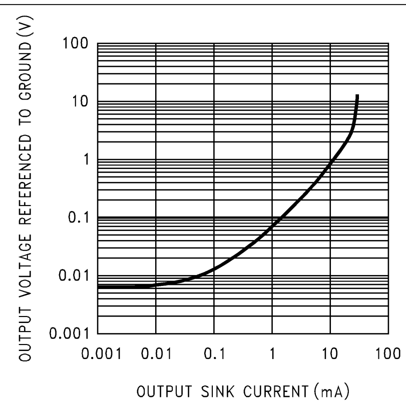


図 5-12. Output Characteristics Sinking Current

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L≥ 1MΩ (unless otherwise specified)

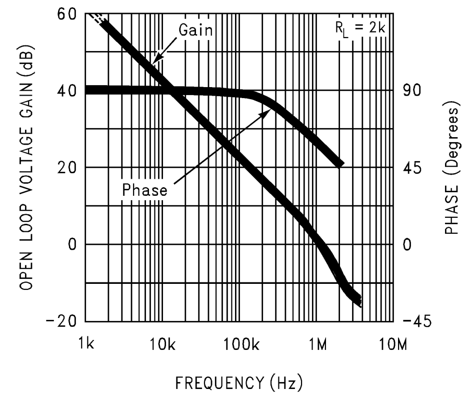
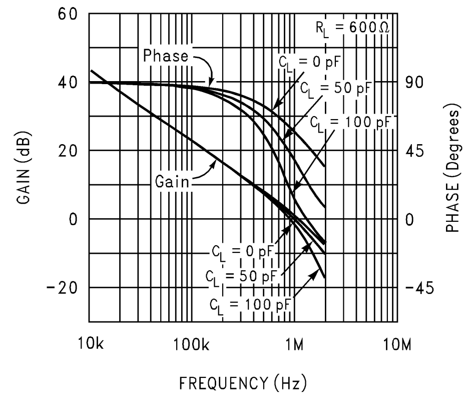
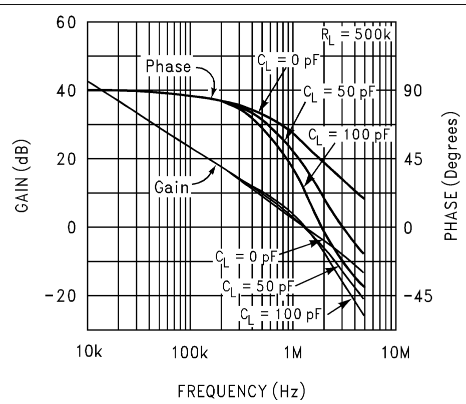


図 5-13. Gain and Phase Response vs Temperature



R_L = 600Ω

図 5-14. Gain and Phase Response vs Capacitive Load



R_L = 500kΩ

図 5-15. Gain and Phase Response vs Capacitive Load

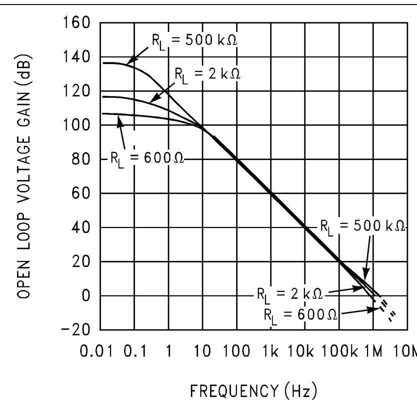


図 5-16. Open-Loop Frequency Response

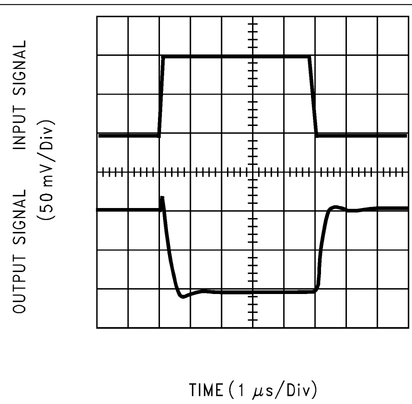


図 5-17. Inverting Small-Signal Pulse Response

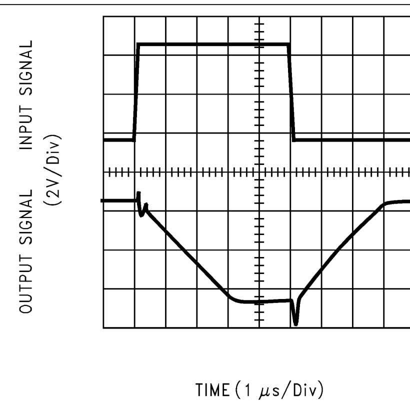


図 5-18. Inverting Large-Signal Pulse Response

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±7.5V, V_{OUT} = mid-supply, and R_L≥ 1MΩ (unless otherwise specified)

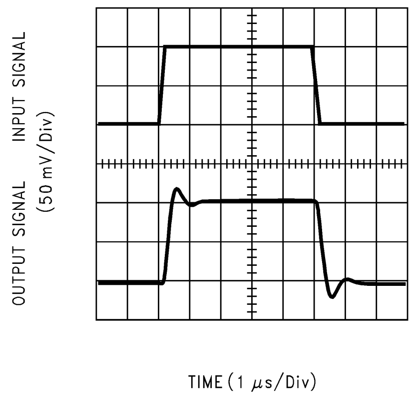


図 5-19. Noninverting Small-Signal Pulse Response

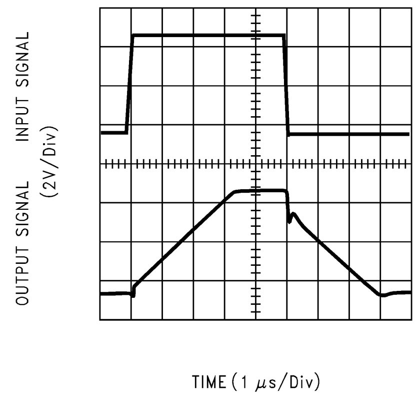


図 5-20. Noninverting Large-Signal Pulse Response

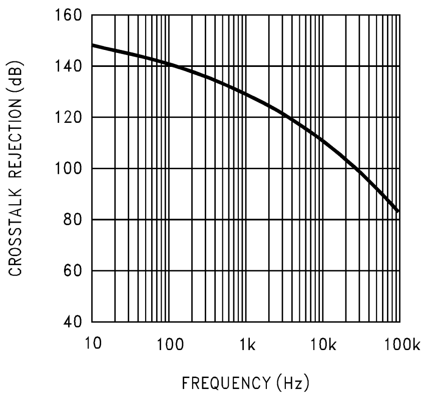
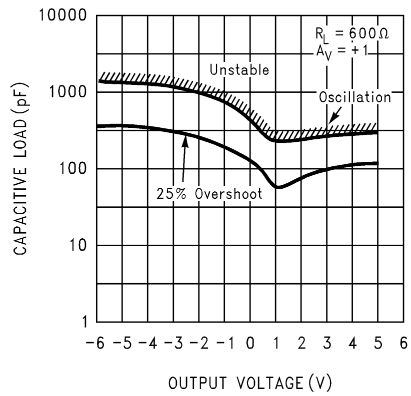
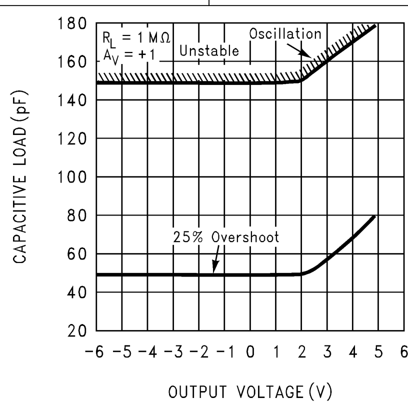


図 5-21. Crosstalk Rejection vs Frequency



R_L = 600Ω

図 5-22. Stability vs Capacitive Load



R_L = 1MΩ

図 5-23. Stability vs Capacitive Load

6 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

6.1 Application Information

6.1.1 Amplifier Topology

The LMC608x incorporate a novel op amp design topology that enables rail to rail output swing even when driving a large load. The topology provides both low output impedance and large gain. Special compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op amps. These features make the LMC608x both easier to design with, and provide higher speed than products typically found in this ultra-low power class. The LMC608x provide a wide input common-mode voltage range extending to the negative supply. In the presence of large input common-mode voltages, input bias current performance can be degraded. Large common-mode voltages are uncommon in very low leakage designs.

6.1.2 Compensating for Input Capacitance

The use of large value feedback resistors is quite common for amplifiers with ultra-low input current, like the LMC608x.

Although the LMC608x are highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When a high input impedance is demanded, guarding of the LMC608x is suggested. Guarding input lines not only reduces leakage, but lowers stray input capacitance as well. (See Printed-Circuit-Board Layout for High Impedance Work)

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in 図 6-1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

The exact value of C_{IN} can be difficult to find, so C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC66x for a more detailed discussion on compensating for input capacitance.

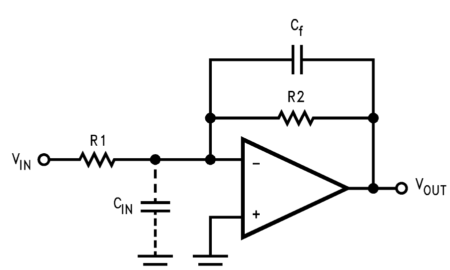


図 6-1. Canceling the Effect of Input Capacitance

6.1.3 Capacitive Load Tolerance

All rail-to-rail output swing op amps have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see セクション 5.8).

Direct capacitive loading reduces the phase margin of many op amps. A pole in the feedback loop is created by the combination of the op amp output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in 図 6-2.

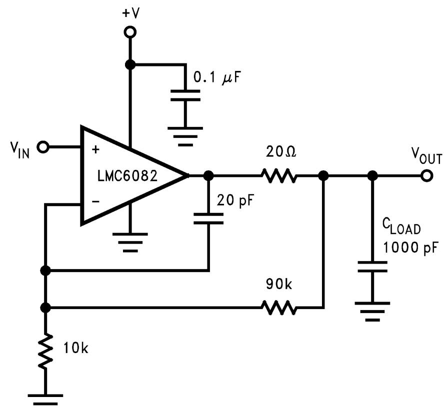


図 6-2. LMC6082 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of 図 6-2, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ 図 6-3. Typically a pull up resistor conducting 500µA or more significantly improves capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pullup resistor (see セクション 5.7).

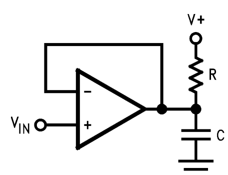


図 6-3. Compensating for Large Capacitive Loads With a Pullup Resistor

6.1.4 Latch-Up

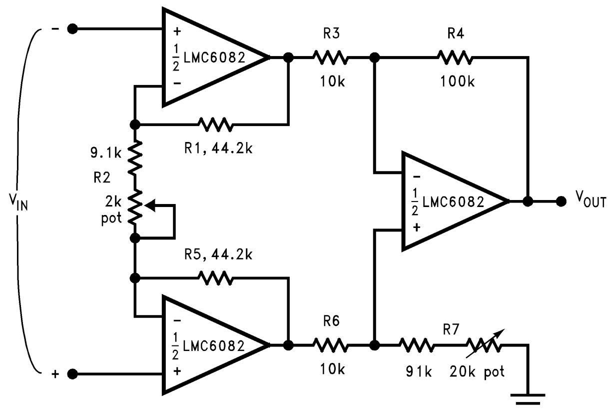
CMOS devices tend to be susceptible to latch-up as a result of the internal, parasitic, silicon-controlled rectifier (SCR) effects. The input and output (I/O) pins look similar to the gate of the SCR. A minimum current is required to trigger the SCR gate lead. Use some resistive method to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latch-up mode. Limiting current to the supply pins also inhibits latch-up susceptibility.

6.2 Typical Applications

6.2.1 Typical Single-Supply Applications

The extremely high input impedance, and low power consumption, make the LMC608x an excellent choice for applications that require battery-powered operation. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

図 6-4 shows an instrumentation amplifier that features high differential and common mode input resistance (> $10^{14}\Omega$), 0.01% gain accuracy at A_V = 1000, excellent CMRR with 1kΩ imbalance in bridge source resistance. Input current is less than 100fA and offset drift is less than 2.5μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, use low drift resistors like the RES11A. An example of an instrumentation amplifier with the LMC608x is provided in the next section.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3} \quad (3)$$

$A_V \approx 100$ for circuit shown (R_2 = 9.822kΩ).

図 6-4. Instrumentation Amplifier

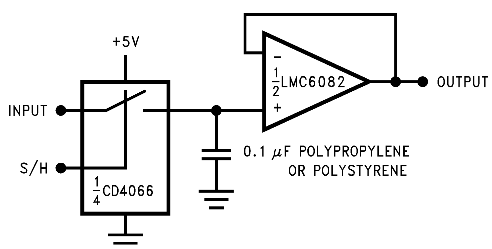


図 6-5. Low Leakage Sample and Hold

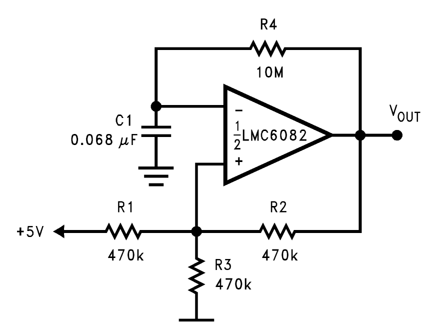


図 6-6. 1Hz Square-Wave Oscillator

6.2.2 Instrumentation Amplifier

The measurement of differential signals is quite common across many applications and are especially prevalent in biopotential sensors, for example electrocardiograms. Biopotential sensors can often be high impedance and require low input bias and current noise. Instrumentation amplifiers, introduced in the previous section, are commonly used to condition differential signals from biopotential sensors The LMC608x are a great choice in particular due to the extremely low input bias current and current noise, high common-mode rejection ratio (CMRR) and low power. A high performance instrumentation amplifier can be achieved by using the LMC608x and a pair of RES11A matched resistors.

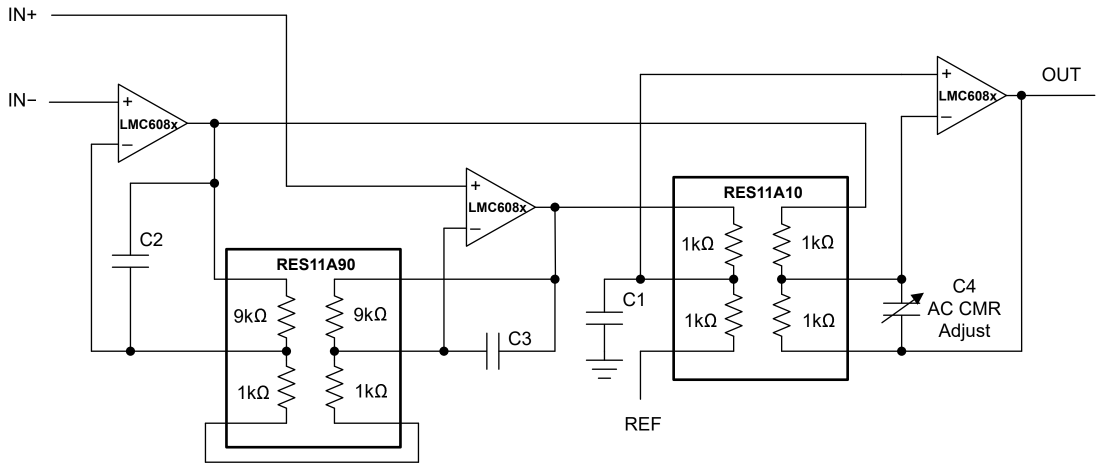


図 6-7. Instrumentation Amplifier With the RES11A

図 6-7 shows an instrumentation amplifier design with a gain of 10V/V. The first RES11A is used to set the gain of the amplifier. In this case, a ratio of 1:9 is used to create a gain of 10V/V, but many different gain configurations are possible. The second RES11A is used to build a high CMRR, low drift, unity gain difference amplifier. This design provides a precision, differential-to-single ended amplifier with very high input impedance. A smaller, lower power design, a two op amp instrumentation amplifier, is possible using the dual channel LMC6082 and only one RES11A matched pair at the expense of higher CMRR.

6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 Printed Circuit Board Layout for High-Impedance Work

Generally, any circuit that operates with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC608x, typically less than 10fA, an excellent layout is crucial. Fortunately, the techniques of obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though the leakage can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC608x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op amp inputs, as in 図 6-8. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PCB foil must then be connected to a voltage that is at the same voltage as the amplifier inputs because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of the input. This leakage causes a 100 times degradation from the LMC608x actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 0.05pA of leakage current. See 図 6-9 to 図 6-11 for typical connections of guard rings for standard op amp configurations.

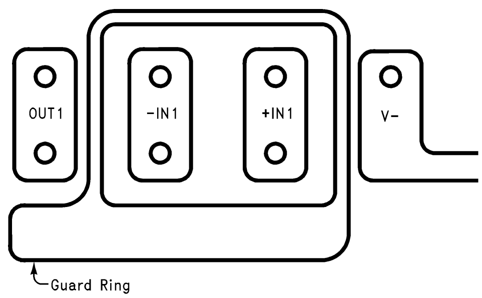


図 6-8. Example of Guard Ring in Printed Circuit Board Layout

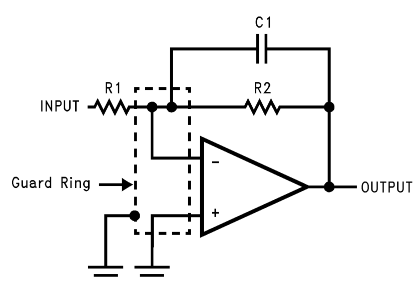


図 6-9. Typical Connections of Guard Rings: Inverting Amplifier

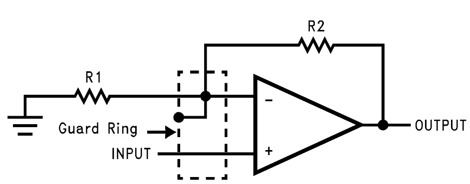


図 6-10. Typical Connections of Guard Rings: Noninverting Amplifier

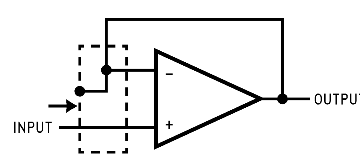
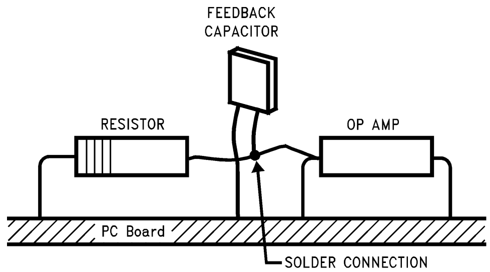


図 6-11. Typical Connections of Guard Rings: Follower

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, there is another technique that is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all; instead, bend the pin up in the air and use only air as an insulator because air is an excellent insulator. In this case, some of the advantages of PCB construction are lost, but the advantages of air are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See 図 6-12.



注

Input pins are lifted out of PCB and soldered directly to components. All other pins are connected to PCB.

図 6-12. Air wiring

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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7.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (March 2013) to Revision E (February 2024) **Page**

- LMC6081 および LMC6084 デバイスと関連コンテンツを追加....................1
- 電気的特性に合わせて、「特長」の出力スイング負荷条件を 100kΩ から 2kΩ に変更、単一電源動作を 15V から 15.5V に変更、高電圧ゲインを 130dB から 123dB に変更 1
- 「概要」のデバイスの説明を更新....................1
- Added *Pin Configurations and Functions* 3
- Added *Thermal Information* 6
- Changed separate DC and AC *Electrical Characteristics* into single *Electrical Characteristics* 7
- Changed parameter names to conform to latest data sheet standards in *Electrical Characteristics* 7
- Changed input current noise density specification from 0.2fA/√Hz to 4fA/√Hz in *Electrical Characteristics* 7
- Changed total harmonic distortion specification from 0.01% to 0.2% in *Electrical Characteristics* 7
- Added footnote detailing how slew rate minimum specification is specified in *Electrical Characteristics* 7
- Added offset voltage vs input common mode voltage and input bias vs common mode voltage curves in *Typical Characteristics* 11
- Added R_L, V_{CM}, and V_{OUT} conditions to the *Typical Characteristics* header....................11
- Deleted Figure 4 and Figure 5 from *Typical Characteristics* 11
- Updated description in *Amplifier Topology* 15

- Added reference to RES11A instrumentation amplifier circuit in *Typical Single-Supply Applications* 17
- Added *Instrumentation Amplifier* section... 18

Changes from Revision C (March 2013) to Revision D (March 2013) — Page

- 「ピン構成および機能」、「仕様」、「絶対最大定格」、「 ESD 定格」、「推奨動作条件」、「熱に関する情報」、「電気的特性」、「代表的特性」、「詳細説明」、「概要」、「機能ブロック図」、「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「代表的なアプリケーション」、「電源に関する推奨事項」、「レイアウト」、「レイアウトのガイドライン」、「レイアウト例」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報 」の各セクションを追加 1
- Changed layout of National Data Sheet to TI format...17

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6081-MDA	ACTIVE	DIESALE	Y	0	270	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LMC6081AIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81AIM	
LMC6081AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81AIM	Samples
LMC6081IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81IM	Samples
LMC6081IN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6081 IN	Samples
LMC6082AIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 82AIM	
LMC6082AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 82AIM	Samples
LMC6082AIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6082 AIN	Samples
LMC6082IM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 82IM	
LMC6082IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 82IM	Samples
LMC6082IN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6082 IN	Samples
LMC6084AIM/NOPB	LIFEBUY	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6084 AIM	
LMC6084AIMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6084 AIM	Samples
LMC6084IM/NOPB	LIFEBUY	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6084IM	
LMC6084IMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6084IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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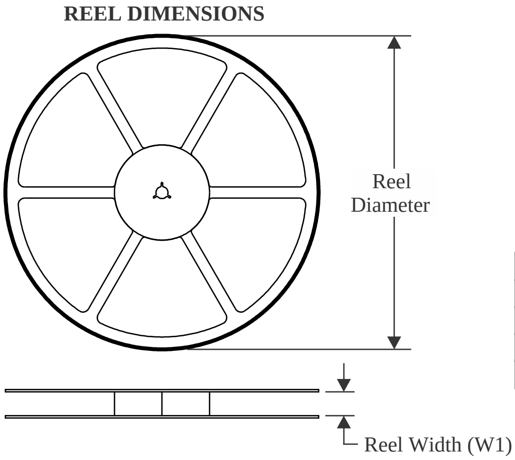
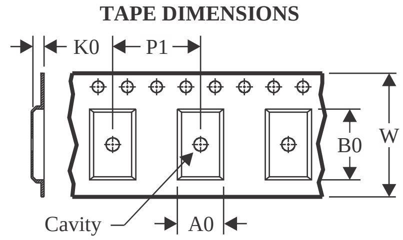
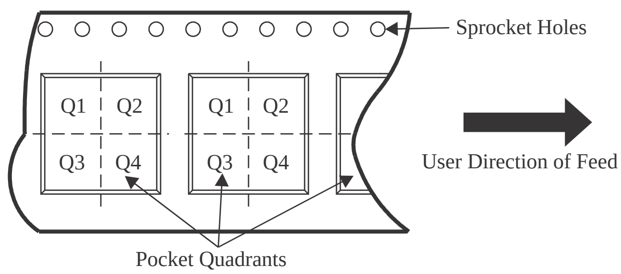
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

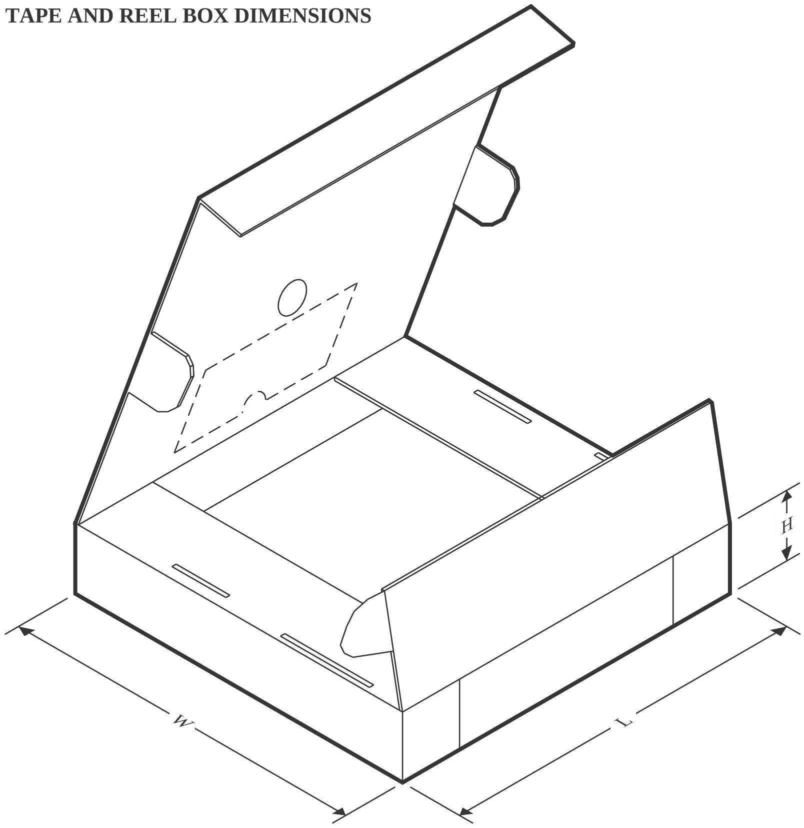
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6081AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6081IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6082AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6082IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6084AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6084IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

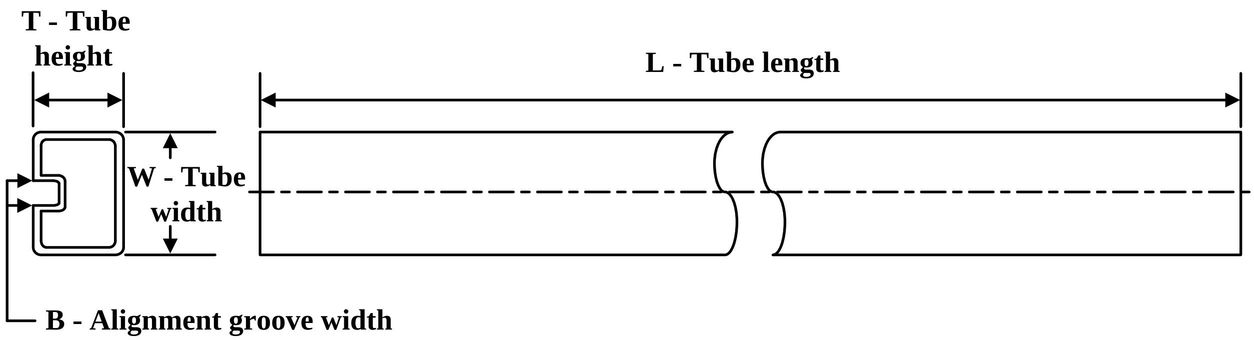
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6081AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6081IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6082AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6082IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6084AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6084IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

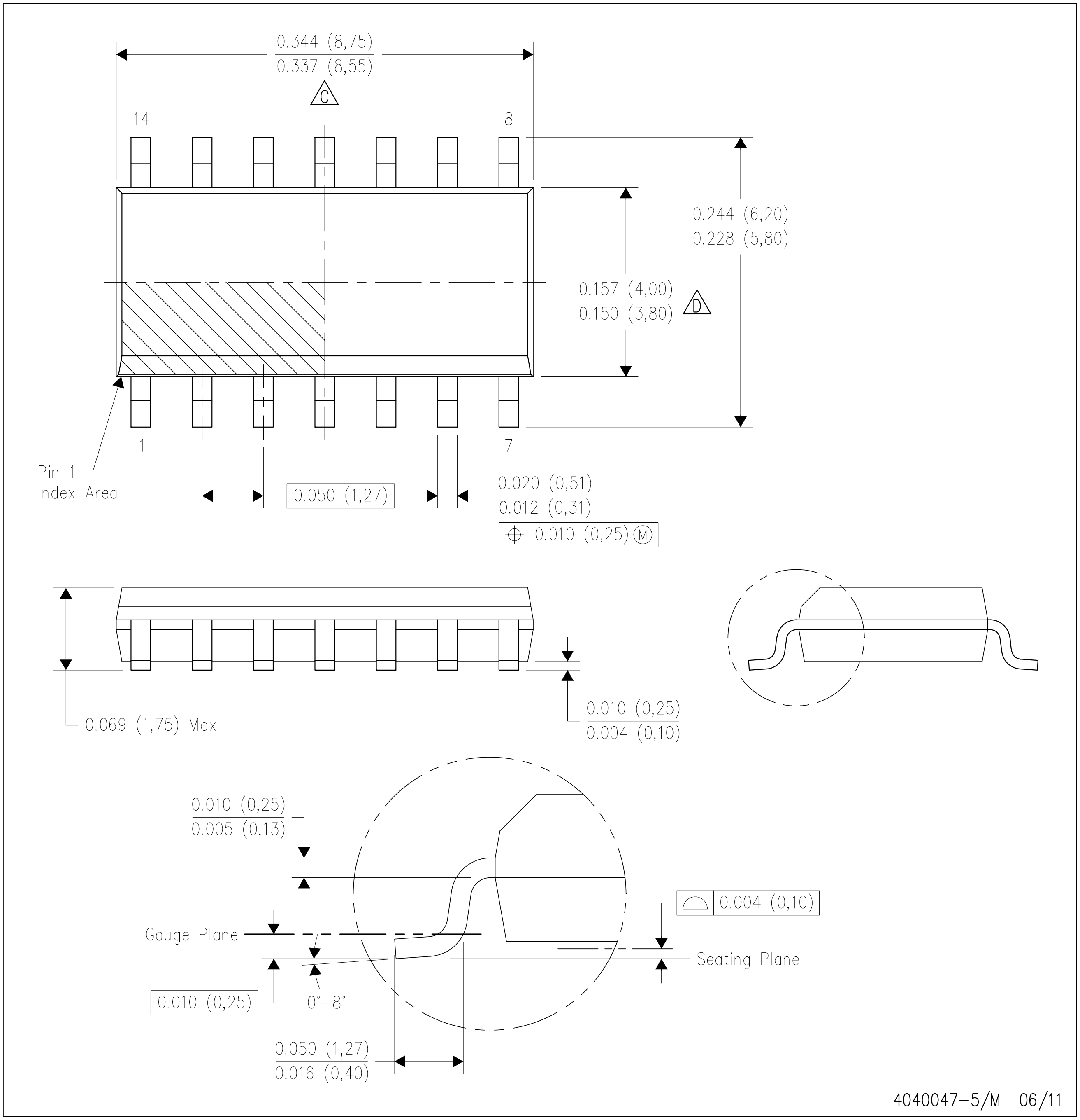
TUBE



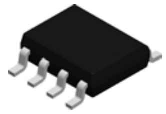
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6081AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6081IN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6082AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6082AIN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6082IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6082IN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6084AIM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMC6084IM/NOPB	D	SOIC	14	55	495	8	4064	3.05

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

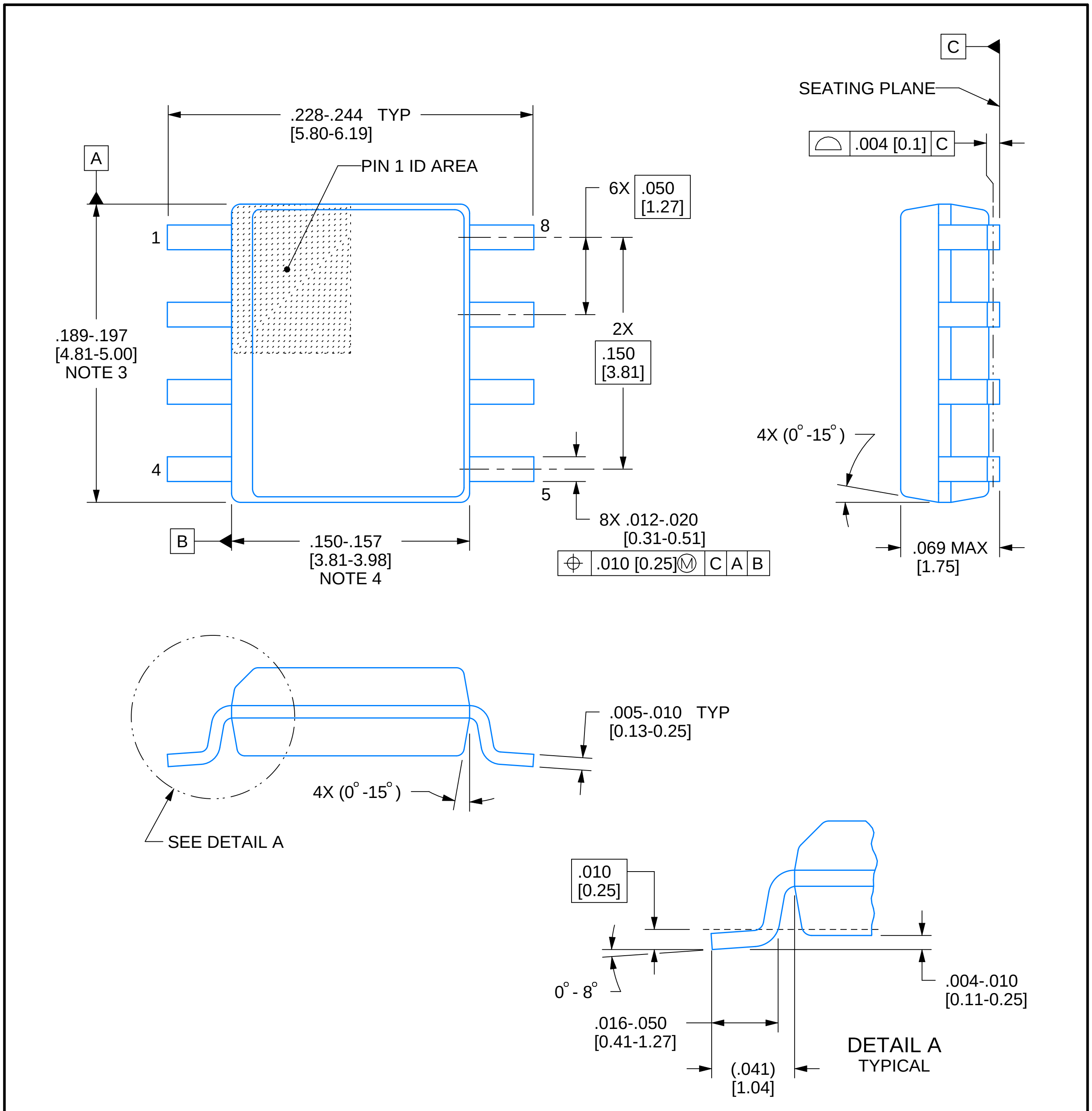


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

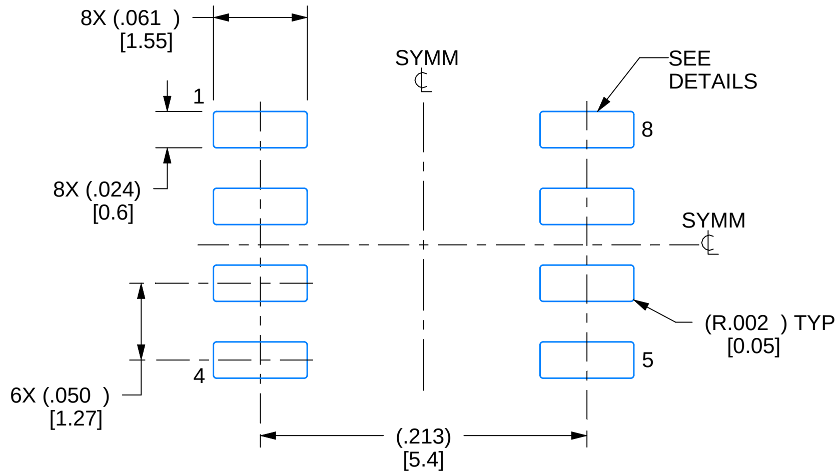
SMALL OUTLINE INTEGRATED CIRCUIT



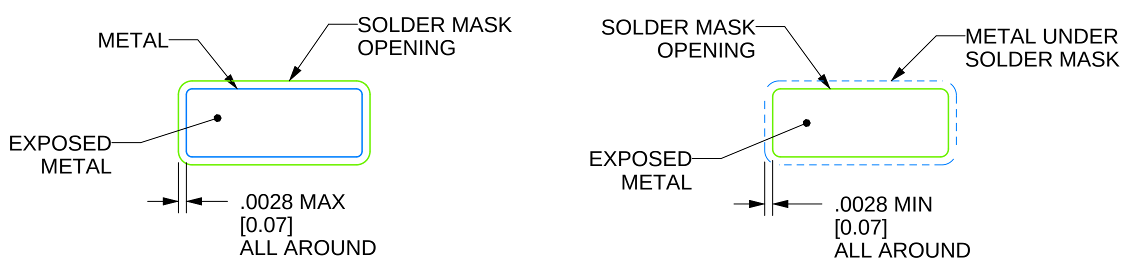
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

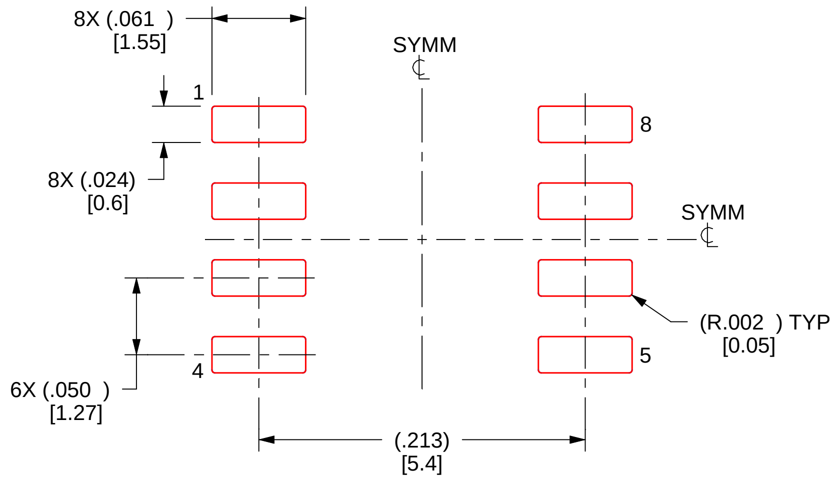
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



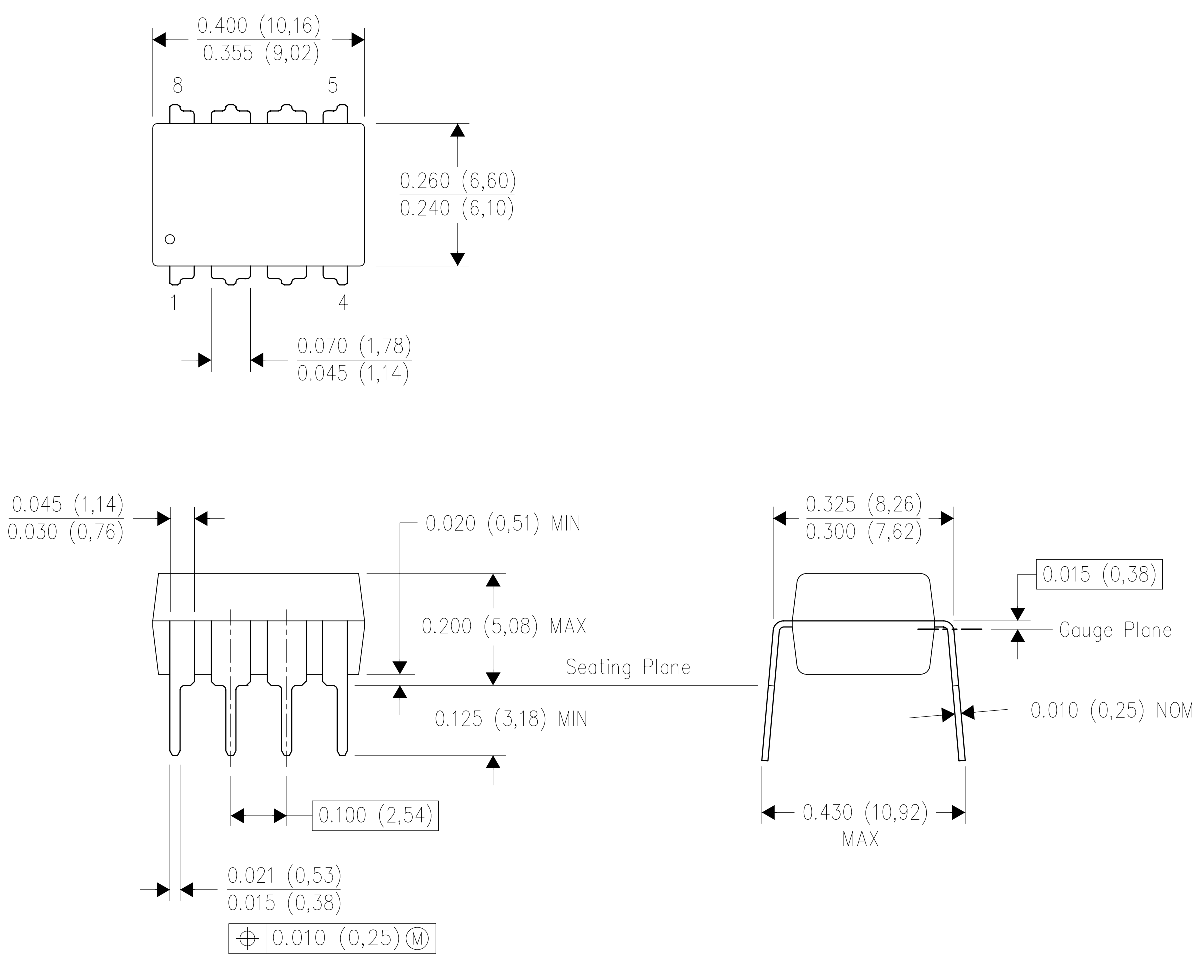
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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