



LMH6703 1.2GHz、シャットダウン機能付きの低歪みオペアンプ

1 特長

- -3dBの帯域幅($V_{OUT} = 0.5V_{PP}$, $A_V = 2$) 1.2GHz
- 2次および3次高調波(20MHz、SOT-23) -69/-90dBc
- 低ノイズ: $2.3nV/\sqrt{Hz}$
- 速いスルーレート: $4500V/\mu s$
- 消費電流: 11mA
- 出力電流: 90mA
- 低差動ゲインおよび位相0.01%/0.02°

2 アプリケーション

- RGBビデオ・ドライバ
- 高解像度プロジェクタ
- フラッシュA/Dドライバ
- D/Aトランスインピーダンス・バッファ
- 広帯域幅のIFアンプ
- レーダー/通信レシーバ
- DDSポストアンプ
- ライン・ドライバ

3 概要

LMH™6703は非常に帯域幅が広い、DCカップリングのモノリシック・オペアンプで、非常に優れた信号の忠実性を必要とする、超高解像度のビデオ・システムや、広ダイナミック・レンジのシステム用に設計されています。

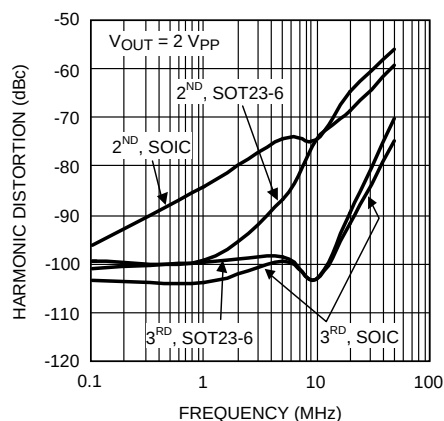
LMH6703は、電流帰還型アーキテクチャを活用して $\pm 1 \sim \pm 10$ の実用的ゲイン範囲を提供するとともに、ユニティ・ゲイン時でも外部補償の必要なしに安定して動作します。ゲイン2で、LMH6703は750MHz、 $2V_{PP}$ 、-3dBの帯域幅で、超高解像度のビデオ・システムをサポートします。10MHzまで12ビットの歪みレベル($R_L = 100\Omega$)、および $2.3nV/\sqrt{Hz}$ の入力換算ノイズにより、LMH6703は高速フラッシュA/DおよびD/Aコンバータ用に理想的なドライバまたはバッファとなります。レーダーや通信レシーバなど、ダイナミック・レンジの広いシステムで、非常に優れた信号の純粋性を提供する広帯域幅のアンプを必要とする場合、LMH6703は入力換算ノイズと高調波歪みが低いことから、魅力的なソリューションになります。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
LMH6703	SOIC (8)	4.90mm×3.91mm
	SOT-23 (6)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

高調波歪みと周波数との関係



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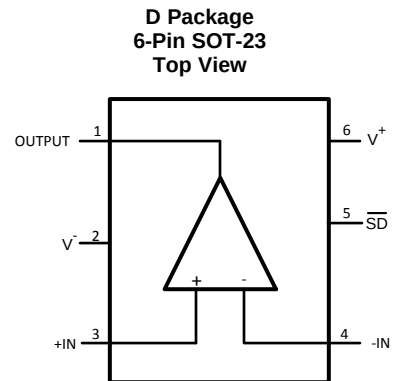
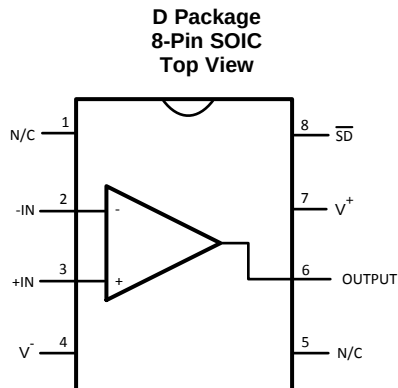
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (March 2013) から Revision E に変更	Page
「ピン機能」の表、「ESD定格」の表、「熱情報」の表、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 - Updated maximum value of Input Bias Current (non-inverting) from ± 20 to -20 in <i>Electrical Characteristics</i> - Updated boldface maximum value (temperature extreme) of Input Bias Current (non-inverting) from ± 23 to -23 in <i>Electrical Characteristics</i>	1 5 5

Revision C (March 2013) から Revision D に変更	Page
Changed layout of National Data Sheet to TI format	14

5 Pin Configuration and Functions



Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	D	DBV		
- IN	2	4	I	Inverting input voltage
+ IN	3	3	I	Non-inverting input voltage
N/C	1, 5	—	—	No connection
OUT	6	1	O	Output
V -	4	2	I	Negative supply
V +	7	6	I	Positive supply
$\overline{\text{SD}}$	8	5	I	Shutdown (active low)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V _S		±6.75	V
I _{OUT}	See ⁽²⁾		
Common mode input voltage	V ⁻	V ⁺	V
Maximum junction temperature		150	°C
Storage temperature	-65	150	°C
Soldering Information	Infrared or convection (20 sec.)	235	°C
	Wave soldering (10 sec.)	260	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
	Machine model (MM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±200

- (1) Human body model: 1.5 kΩ in series with 100 pF. JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) Machine model: 0 Ω in series with 200 pF. JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 200-V MM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	NOM	MAX	UNIT
Operating temperature	-40		85	°C
Supply voltage	±4		±6	V

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMH6703		UNIT
		DBV (SOT-23)	D (SOIC)	
		6 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	182	133	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	139	79	°C/W
R _{θJB}	Junction-to-board thermal resistance	40	73	°C/W
ψ _{JT}	Junction-to-top characterization parameter	28	28	°C/W
ψ _{JB}	Junction-to-board characterization parameter	40	73	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

at $T_J = 25^\circ\text{C}$, $A_V = 2$, $V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $R_F = 560\ \Omega$, $\overline{SD} = \text{Floating}$ (unless otherwise noted)⁽¹⁾

Boldface limits apply at the temperature extremes.

PARAMETER		CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	–3-dB bandwidth	V _{OUT} = 0.5 V _{PP} , A _V = +1	1800		MHz	
		V _{OUT} = 0.5 V _{PP} , A _V = +2	1200			
LSBW		V _{OUT} = 2 V _{PP}	750			
		V _{OUT} = 4 V _{PP}	500			
GF	0.1-dB gain flatness	V _{OUT} = 0.5 V _{PP}	150		MHz	
		V _{OUT} = 2 V _{PP}	150			
DG	Differential gain	R _L = 150 Ω, 4.43 MHz	0.01%			
DP	Differential phase	R _L = 150 Ω, 4.43 MHz	0.02		deg	
TIME DOMAIN RESPONSE						
t _r	Rise time	2-V step, 10% to 90%	0.5		ns	
		6-V step, 10% to 90%	1.05		ns	
t _f	Fall time	2-V step, 10% to 90%	0.5		ns	
		6-V step, 10% to 90%	1.05		ns	
SR	Slew rate	4-V step, 10% to 90% ⁽⁴⁾	4200		V/μs	
		6-V step, 10% to 90% ⁽⁴⁾	4500			
t _s	Settling time	2-V step, V _{OUT} within 0.1%	10		ns	
DISTORTION AND NOISE RESPONSE						
HD2	2 nd harmonic distortion	2 V _{PP} , 5 MHz, SOT-23-6	–87		dBc	
		2 V _{PP} , 20 MHz, SOT-23-6	–69			
		2 V _{PP} , 50 MHz, SOT-23-6	–60			
HD3	3 rd harmonic distortion	2 V _{PP} , 5 MHz, SOT-23-6	–100		dBc	
		2 V _{PP} , 20 MHz, SOT-23-6	–90			
		2 V _{PP} , 50 MHz, SOT-23-6	–70			
IMD	3 rd order intermodulation products	50 MHz, P _O = 5 dBm/ tone	–80		dBc	
e _n	Input referred voltage noise	>1 MHz	2.3		nV/√Hz	
i _n	Input referred noise current	Inverting Pin >1 MHz	18.5		pA/√Hz	
	Input referred noise current	Non-Inverting Pin >1 MHz	3		pA/√Hz	
u						
V _{OS}	Input offset voltage		±1.5		±7 ±9	mV
TCV _{OS}	Input offset voltage average drift	⁽⁵⁾	22			μV/°C
I _B	Input bias current	Non-Inverting ⁽⁶⁾	–7		–20 –23	μA
		Inverting ⁽⁶⁾	–2		±35 ±44	
TCI _B	Input bias current average drift	Non-Inverting ⁽⁵⁾	+30		nA/°C	
		Inverting ⁽⁵⁾	–70			

- (1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
- (2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (3) Typical numbers are the most likely parametric norm.
- (4) Slew rate is the average of the rising and falling edges.
- (5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
- (6) Negative input current implies current flowing out of the device.

LMH6703

JAJSA84E – FEBRUARY 2005 – REVISED MAY 2016

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Electrical Characteristics (continued)

 at $T_J = 25^\circ\text{C}$, $A_V = 2$, $V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $R_F = 560\ \Omega$, $\overline{\text{SD}}$ = Floating (unless otherwise noted)⁽¹⁾
Boldface limits apply at the temperature extremes.

PARAMETER		CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_O	Output voltage range	$R_L = \infty$	± 3.3	± 3.45		V
		$R_L = 100\ \Omega$	± 3.2 ± 3.14	± 3.4		
PSRR	Power supply rejection ratio	$V_S = \pm 4.0\text{ V to } \pm 6.0\text{ V}$	48 46	52		dB
CMRR	Common mode rejection ratio	$V_{CM} = -1.0\text{ V to } +1.0\text{ V}$	45 44	47		dB
I_S	Supply current (enabled)	$\overline{\text{SD}} = 2\text{ V}$, $R_L = \infty$		11	12.5 15.0	mA
	Supply current (disabled)	$\overline{\text{SD}} = 0.8\text{ V}$, $R_L = \infty$		0.2	0.900 0.935	mA
MISCELLANEOUS PERFORMANCE						
R_{IN+}	Non-inverting input resistance			1		M Ω
R_{IN-}	Inverting input resistance	Output Impedance of Input Buffer		30		Ω
C_{IN}	Non-inverting input capacitance			0.8		pF
R_O	Output resistance	Closed Loop		0.05		Ω
CMVR	Input common mode voltage range	CMRR $\geq 40\text{ dB}$	± 1.9			V
I_O	Linear output current	$V_{IN} = 0\text{ V}$, $V_{OUT} \leq \pm 80\text{ mV}$	± 55	± 90		mA
ENABLE/DISABLE PERFORMANCE (DISABLED LOW)						
T_{ON}	Enable time			10		ns
T_{OFF}	Disable time			10		ns
	Output glitch			50		mV _{PP}
V_{IH}	Enable voltage	$\overline{\text{SD}} \geq V_{IH}$	2.0			V
V_{IL}	Disable voltage	$\overline{\text{SD}} \leq V_{IL}$			0.8	V
I_{IH}	Disable pin bias current, high	$\overline{\text{SD}} = V^{+(6)}$		-7	± 70	μA
I_{IL}	Disable pin bias current, low	$\overline{\text{SD}} = 0\text{ V}^{(6)}$	-50	-240	-400	μA
I_{OZ}	Disabled output leakage current	$V_{OUT} = \pm 1.8\text{ V}$		0.07	± 25 ± 40	μA

7 Typical Characteristics

at $A_V = 2$, $R_L = 100\ \Omega$, $V_S = \pm 5\ \text{V}$, $R_F = 560\ \Omega$, $T_A = 25^\circ\text{C}$, SOT-23-6 (unless otherwise noted)

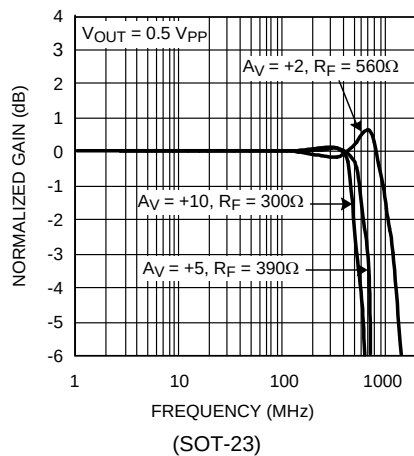


Figure 1. Small Signal Non-Inverting Frequency Response

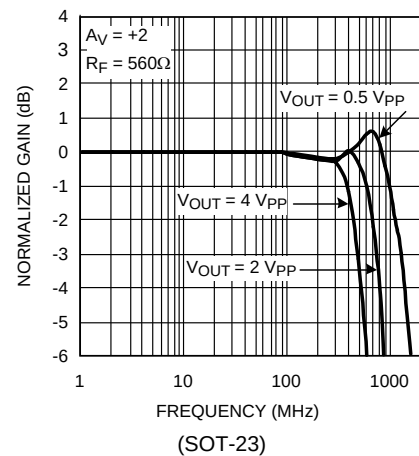


Figure 2. Large Signal Frequency Response

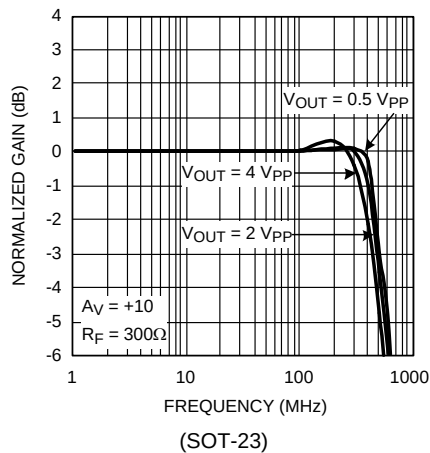


Figure 3. Large Signal Frequency Response

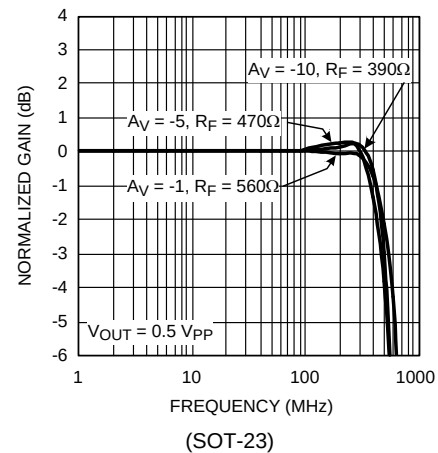


Figure 4. Small Signal Inverting Frequency Response

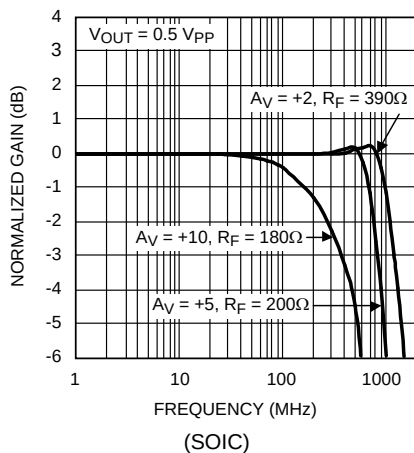


Figure 5. Small Signal Non-Inverting Frequency Response

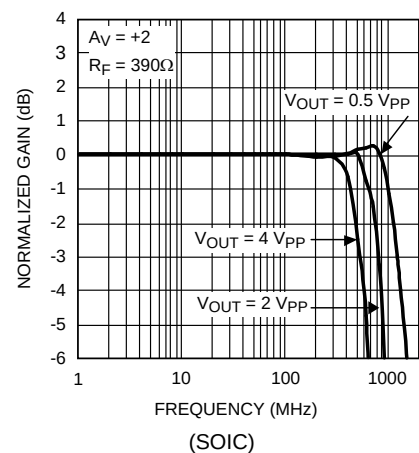


Figure 6. Large Signal Frequency Response

Typical Characteristics (continued)

at $A_V = 2$, $R_L = 100\ \Omega$, $V_S = \pm 5\text{ V}$, $R_F = 560\ \Omega$, $T_A = 25^\circ\text{C}$, SOT-23-6 (unless otherwise noted)

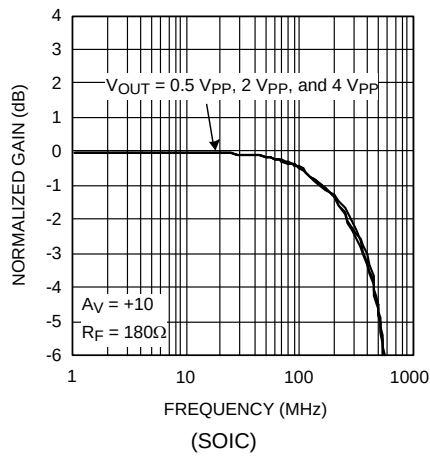


Figure 7. Large Signal Frequency Response

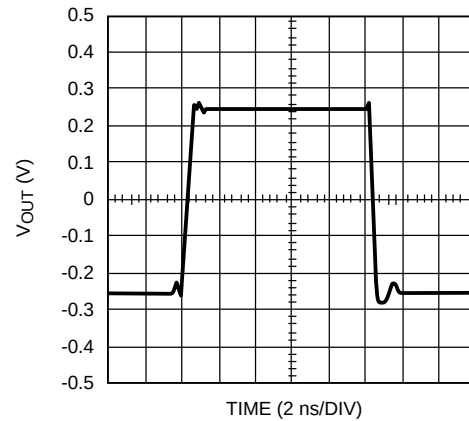


Figure 8. Small Signal Pulse Response

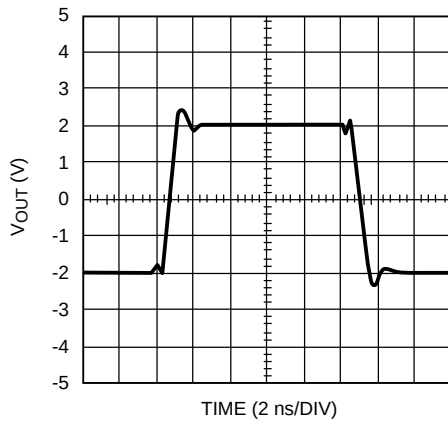


Figure 9. Large Signal Pulse Response

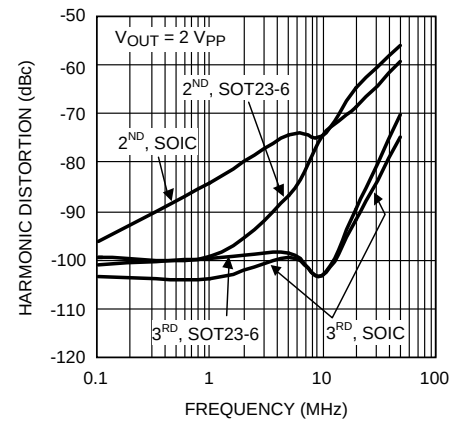


Figure 10. Harmonic Distortion vs Frequency

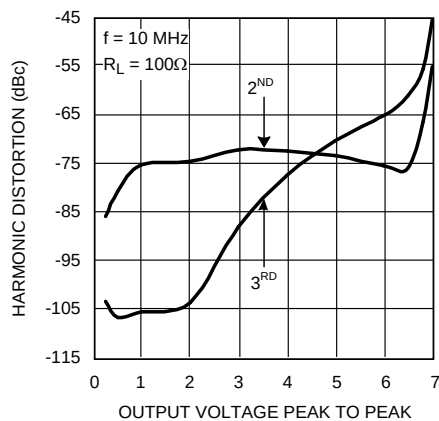


Figure 11. Harmonic Distortion vs Output Voltage

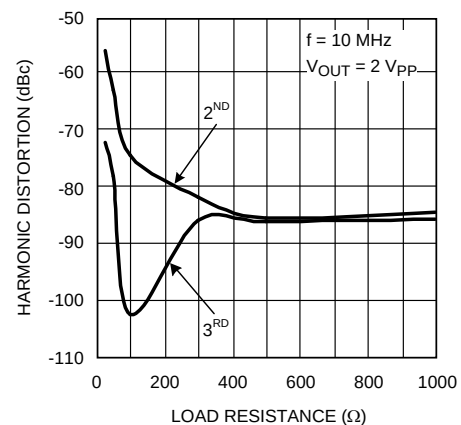


Figure 12. Harmonic Distortion vs. Load

Typical Characteristics (continued)

at $A_V = 2$, $R_L = 100\ \Omega$, $V_S = \pm 5\ \text{V}$, $R_F = 560\ \Omega$, $T_A = 25^\circ\text{C}$, SOT-23-6 (unless otherwise noted)

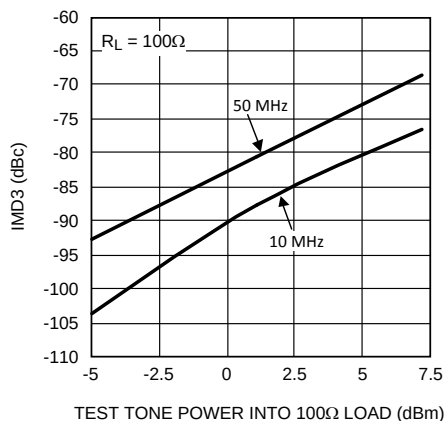


Figure 13. 2-Tone 3rd Order Intermodulation

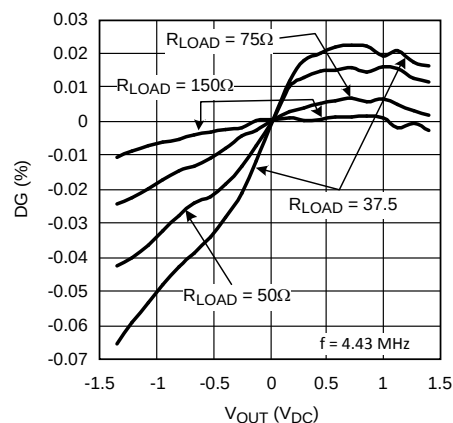


Figure 14. Differential Gain

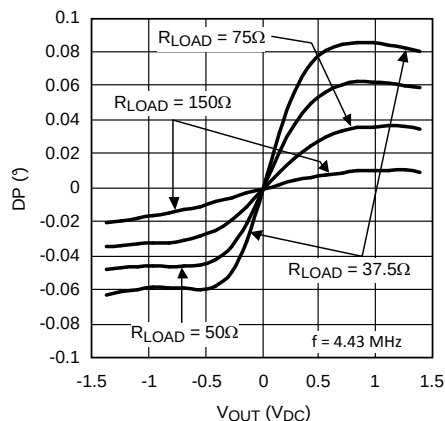


Figure 15. Differential Phase

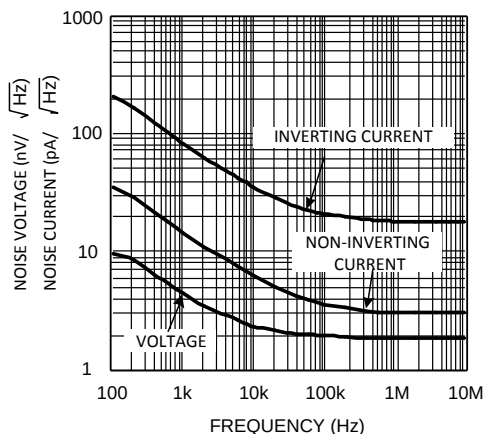


Figure 16. Noise

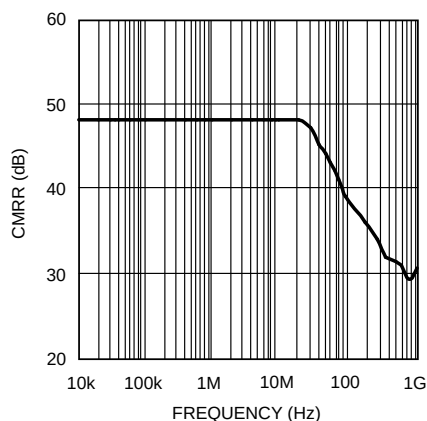


Figure 17. CMRR vs Frequency

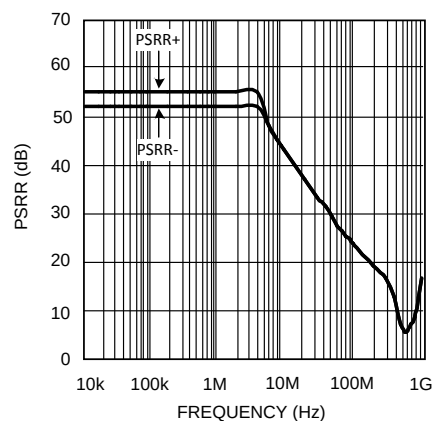


Figure 18. PSRR vs Frequency

Typical Characteristics (continued)

at $A_V = 2$, $R_L = 100\ \Omega$, $V_S = \pm 5\text{ V}$, $R_F = 560\ \Omega$, $T_A = 25^\circ\text{C}$, SOT-23-6 (unless otherwise noted)

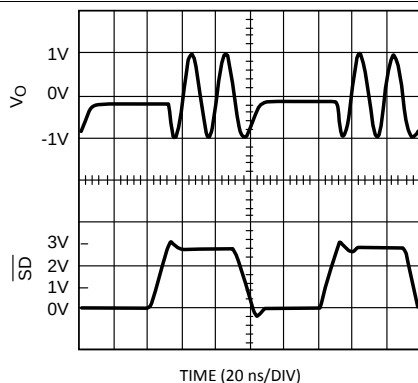


Figure 19. Disable Timing

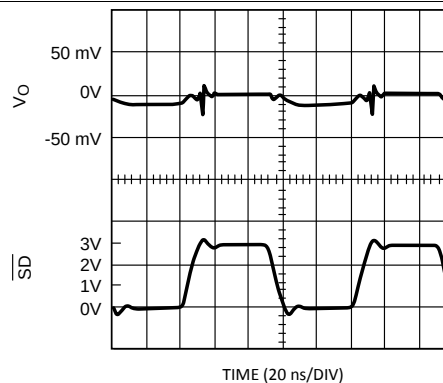
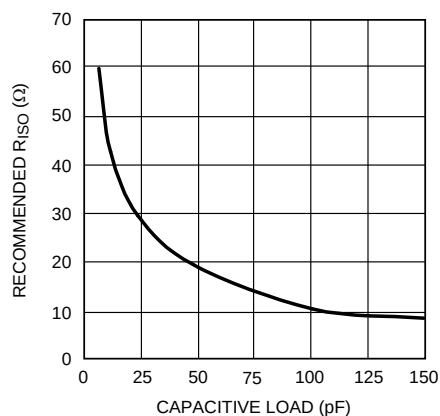


Figure 20. Disable Output Glitch



(See [Application and Implementation](#))

Figure 21. R_{ISO} VS C_{LOAD}

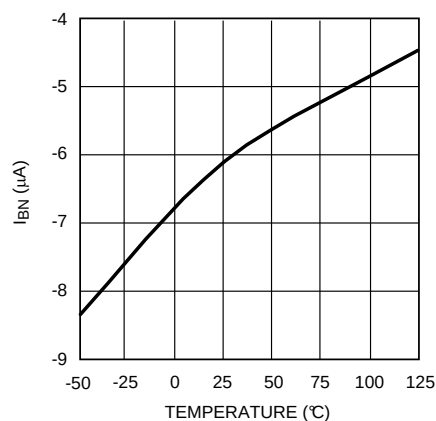


Figure 22. Non-Inverting Input Bias vs Temperature

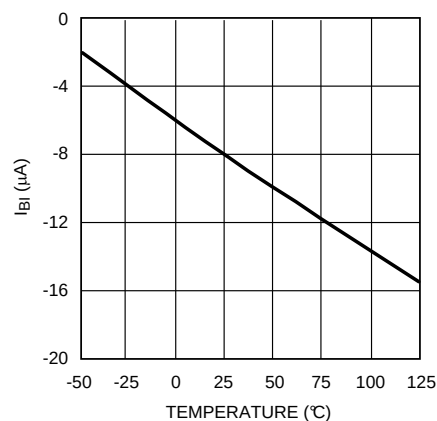


Figure 23. Inverting Input Bias vs Temperature

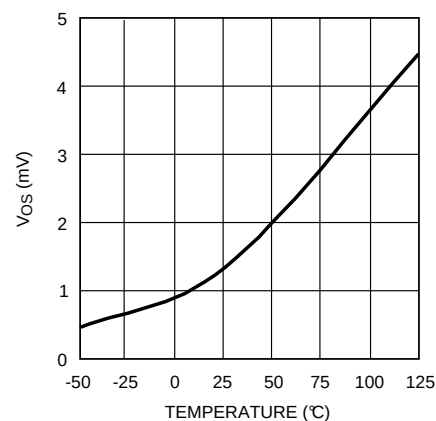


Figure 24. Input Offset vs Temperature

Typical Characteristics (continued)

at $A_V = 2$, $R_L = 100\ \Omega$, $V_S = \pm 5\text{ V}$, $R_F = 560\ \Omega$, $T_A = 25^\circ\text{C}$, SOT-23-6 (unless otherwise noted)

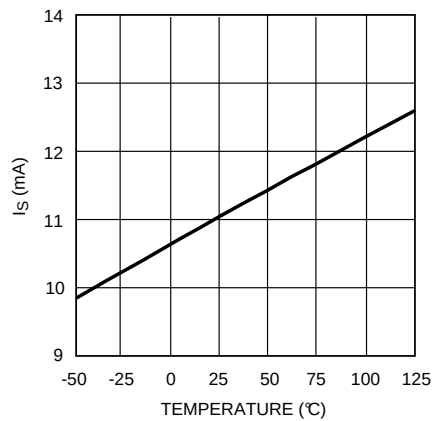


Figure 25. Supply Current vs Temperature

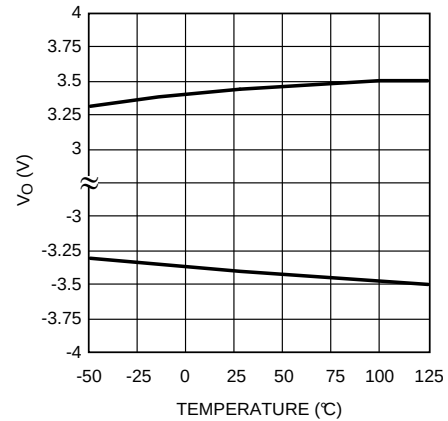


Figure 26. Voltage Swing vs Temperature

8 Detailed Description

8.1 Overview

The LMH6703 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6703 distortions shown in [Typical Characteristics](#).

8.2 Feature Description

The LMH6703 is a high speed current feedback amplifier, optimized for excellent bandwidth, gain flatness, and low distortion. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6703 in the SOT-23-6 package is optimized for use with a 560- Ω feedback resistor. The LMH6703 in the SOIC package is optimized for use with a 390- Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 ([SNOA366](#)) discusses this in detail along with the occasions where a different R_F might be advantageous.

8.3 Device Functional Modes

8.3.1 Feedback Resistor Selection

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Characteristics plots specify an R_F of 560 Ω (390 Ω for the SOIC package), a gain of 2 V/V, and ± 5 -V power supplies (unless otherwise specified). Generally, lowering R_F from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below its recommended value will cause overshoot, ringing and, eventually, oscillation.

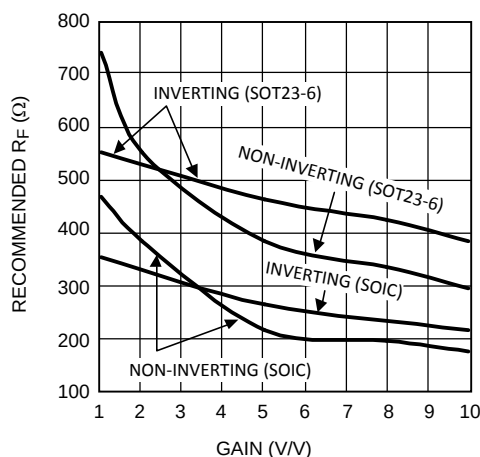


Figure 27. Recommended R_F vs. Gain

Since a current feedback amplifier is dependant on the value of R_F to provide frequency compensation and since the value of R_F can be used to optimize the frequency response, different packages use different R_F values. As shown in [Figure 27](#), the SOT-23-6 and the SOIC package use different values for the feedback resistor, R_F . Since each application is slightly different, it is worth some experimentation to find the optimal R_F for a given circuit. In general, a value of R_F that produces ≈ 0.1 dB of peaking is the best compromise between stability and maximum bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6703 requires a 560 Ω (390 Ω for SOIC package) feedback resistor for stable operation.

Device Functional Modes (continued)

The LMH6703 was optimized for high speed operation. As shown in [Figure 27](#), the suggested value for R_F decreases for higher gains. Due to the output impedance of the input buffer, there is a practical limit for how small R_F can go, based on the lowest practical value of R_G . This limitation applies to both inverting and non inverting configurations. For the LMH6703 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R_G . The LMH6703 begins to operate in a gain bandwidth limited fashion in the region when R_G is nearly equal to the input buffer impedance. Note that the amplifier will operate with R_G values well below 20 Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the Inverting and Non-Inverting inputs cannot be expected to remain small.

Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is $R_G \parallel R_T$ (R_T is optional). The value of R_G is R_F / Gain . Thus for a SOT-23 in a gain of $-5V/V$, an R_F of 460 Ω is optimum and R_G is 92 Ω. Without a termination resistor, R_T , the input impedance would equal R_G , 92 Ω. Using an R_T of 109Ω will set the input resistance to match a 50-Ω source. Note that source impedances greater than R_G cannot be matched in the inverting configuration.

For more information see Application Note OA-13 ([SNOA366](#)) which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6703 is approximately 30 Ω. The LMH6703 is designed for optimum performance at gains of 1 to 10 V/V and -1 to -9 V/V. Higher gain configurations are still useful, however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

The LMH6703 data sheet shows both SOT-23-6 and SOIC data in the Electrical Characteristic section to aid in selecting the right package. The Typical Characteristics section shows SOT-23-6 package plots only.

8.3.2 DC Accuracy and Noise

Example below shows the output offset computation equation for the non-inverting configuration (see [Figure 29](#)) using the typical bias current and offset specifications for $A_V = 2$:

$$\text{Output Offset : } V_O = (I_{BN} \times R_{IN} \pm V_{OS}) (1 + R_F/R_G) \pm I_{BI} \times R_F$$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for $A_V = 2$, $R_F = 560$ Ω, $R_{IN} = 25$ Ω:

$$V_O = (7 \mu A \times 25 \Omega \pm 1.5 \text{ mV}) (1 + 560/560) \pm 2 \mu A \times 560 \approx -3.7 \text{ mV to } 4.5 \text{ mV}$$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-07 ([SNOA365](#)). The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 ([SNOA375](#)) for a full discussion of noise calculations for current feedback amplifiers.

Device Functional Modes (continued)

8.3.3 Enable/Disable

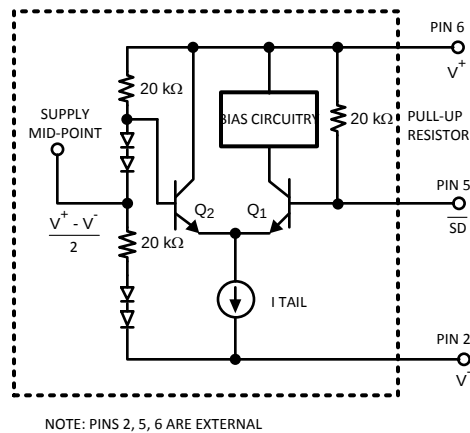


Figure 28. $\overline{\text{SD}}$ Pin Simplified Schematic (SOT-23 Pinout Shown)

For 5-V supplies only, the LMH6703 has a TTL logic compatible disable function. Apply a logic low ($< 0.8 \text{ V}$) to the $\overline{\text{SD}}$ pin and the LMH6703 is disabled. Apply a logic high ($> 2.0 \text{ V}$), or let the pin float and the LMH6703 is enabled. Voltage, not current, at the Shutdown pin (SD) determines the enable/disable state. Care must be exercised to prevent the shutdown pin voltage from going more than 0.8 V below the midpoint of the supply voltages (0V with split supplies, $V^+/2$ with single supply biasing). Doing so could cause transistor Q1 to Zener resulting in damage to the disable circuit (See [Figure 28](#)). The core amplifier is unaffected by this, but the shutdown operation could become permanently slower as a result.

Disabled, the LMH6703 inputs and output become high impedances. While disabled the LMH6703 quiescent current is approximately $200 \mu\text{A}$. Because of the pull up resistor on the shutdown circuit, the I_{CC} and I_{EE} currents (positive and negative supply currents respectively) are not balanced in the disabled state. The positive supply current (I_{CC}) is approximately $300 \mu\text{A}$ while the negative supply current (I_{EE}) is only $200 \mu\text{A}$. The remaining I_{EE} current of $100 \mu\text{A}$ flows through the shutdown pin.

The disable function can be used to create analog switches or multiplexers. Implement a single analog switch with one LMH6703 positioned between an input and output. Create an analog multiplexer with several LMH6703s and tie the outputs together.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

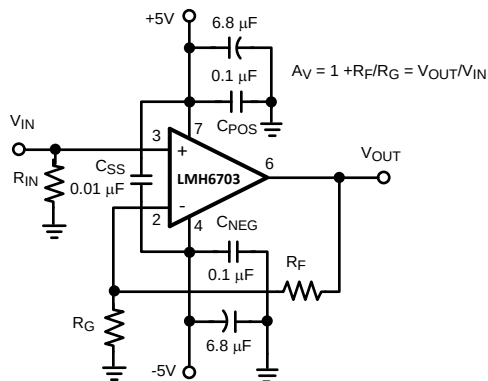


Figure 29. Recommended Non-Inverting Gain Circuit (SOIC Pinout Shown)

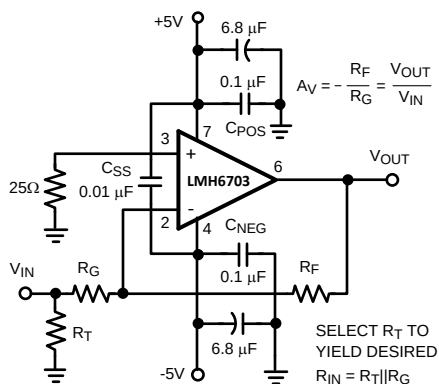


Figure 30. Recommended Inverting Gain Circuit (SOIC Pinout Shown)

9.1.1 Capacitive Load Drive

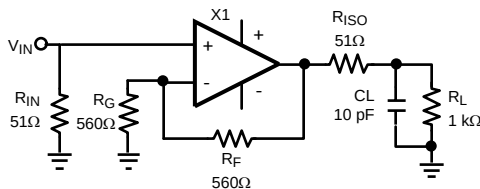


Figure 31. Decoupling Capacitive Loads

Typical Application (continued)

Capacitive output loading applications will benefit from the use of a series output resistor R_{ISO} . Figure 31 shows the use of a series output resistor, R_{ISO} , to stabilize the amplifier output under capacitive loading. Capacitive loads from 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 21 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This produces a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{ISO} can be reduced slightly from the recommended values.

9.1.2 Video Performance

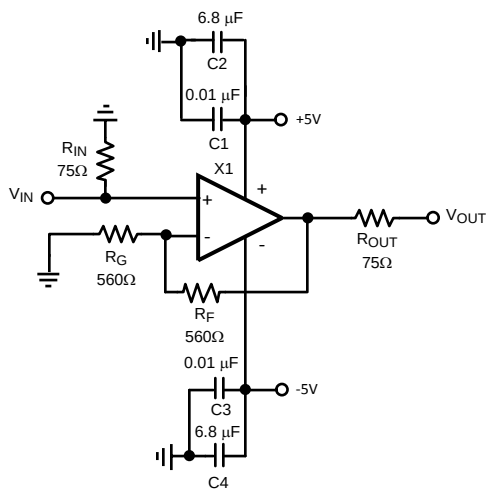


Figure 32. Typical Video Application

The LMH6703 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless with DG of 0.01% and DP of 0.02°. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitance from the amplifier output stage. Figure 32 shows a typical configuration for driving 75Ω cable. The amplifier is configured for a gain of two compensating for the 6 dB loss due to R_{OUT} .

10 Power Supply Recommendations

The LMH6703 can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

11 Layout

11.1 Layout Guidelines

Whenever questions about layout arise, use the evaluation board (see [Table 1](#)) as a guide. The LMH730216 is the evaluation board for SOT-23-6 samples and the LMH730227 is the evaluation board for SOIC samples.

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. Components in the feedback path should be placed as close to the device as possible to minimize parasitic capacitance. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each voltage rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located further from the device, the smaller ceramic bypass capacitors should be placed as close to the device as possible. In [Figure 29](#) and [Figure 30](#), C_{SS} is optional, but is recommended for best second order harmonic distortion.

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. See *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 ([SNOA367](#)). The evaluation board(s) is a good example of high frequency layout techniques as a reference.

General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing, as shown in [Figure 33](#) and [Figure 34](#), with matched impedance traces for longer runs. However, open up both ground and power planes around the capacitive sensitive input and output device pins.
- Use good, high-frequency decoupling capacitors (0.1 μF) on the ground plane at the device power pins as shown in [Figure 33](#). Higher value capacitors (2.2 μF) are required, but may be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junction is very sensitive to parasitic capacitance. Connect any R_f and R_g elements into the summing junction with minimal trace length to the device pin side of the resistor, as shown in [Figure 34](#). The other side of these elements can have more trace length if needed to the source or to ground.

Table 1. Evaluation Boards

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6703MF	SOT-23-6	LMH730216
LMH6703MA	SOIC	LMH730227

11.2 Layout Example

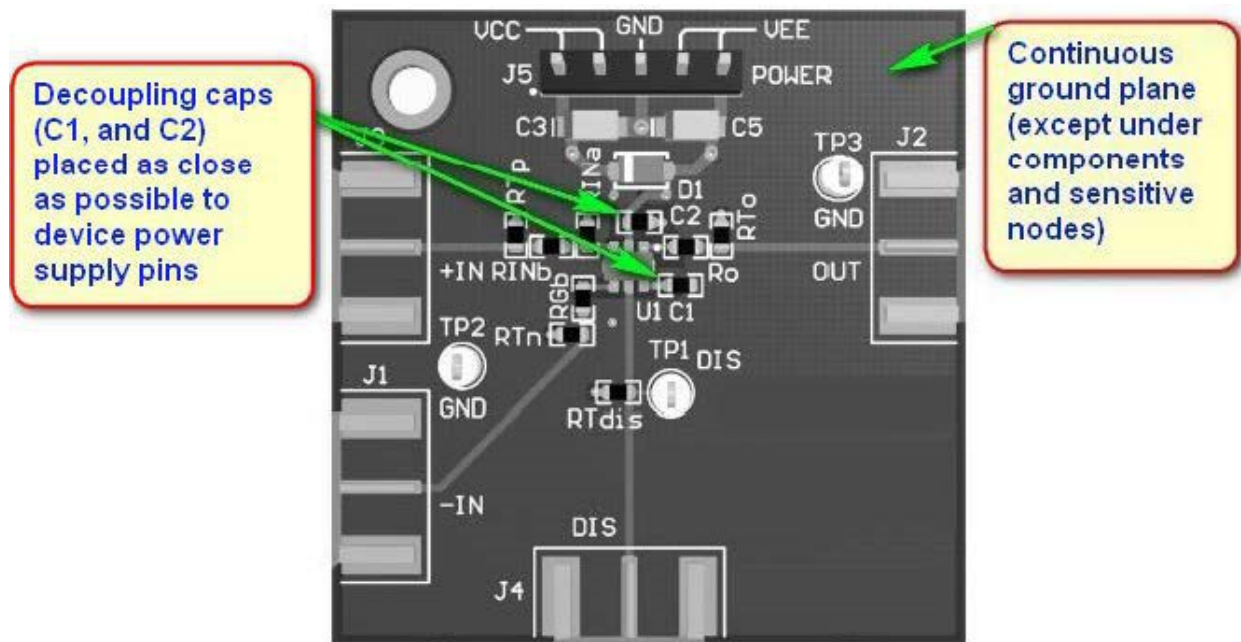


Figure 33. Evaluation Board Layer 1

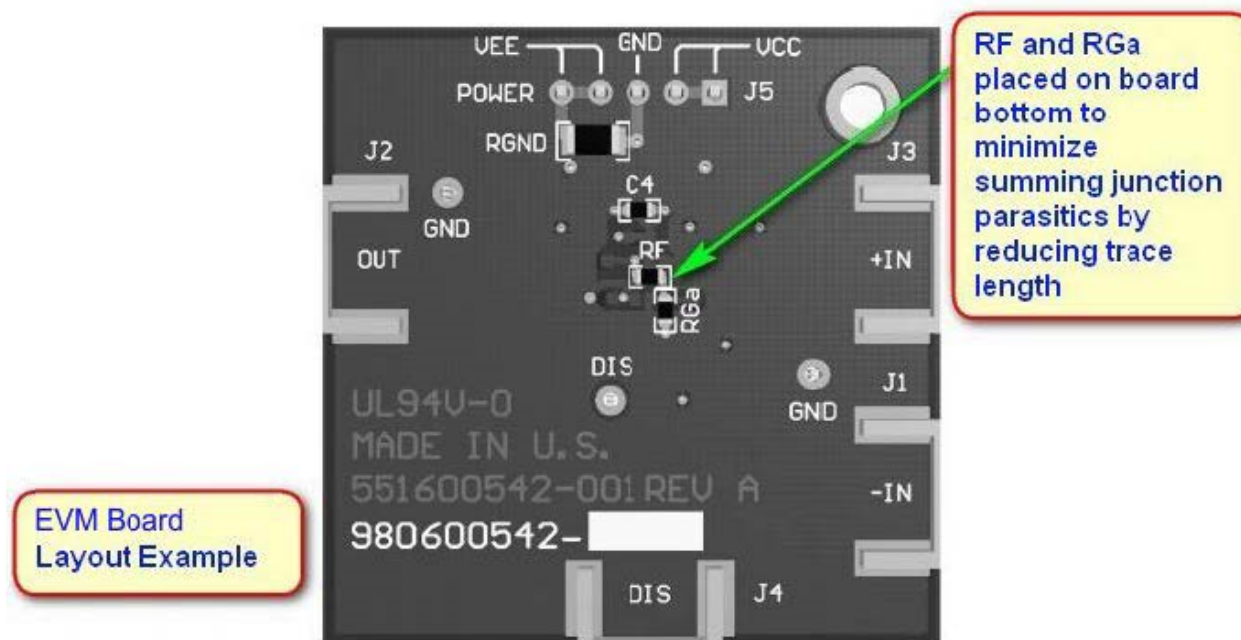


Figure 34. Evaluation Board Layer 2

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- 『ハンダ付けの絶対最大定格』(SNOA549)
- 『電流帰還型オペアンプ・アプリケーション回路ガイド』、アプリケーション・ノートOA-07 (SNOA365)
- 『広帯域電流帰還型アンプ適用時に多見される失敗』、アプリケーション・ノートOA-15 (SNOA367)
- 『Comlinearアンプのノイズ解析』、アプリケーション・ノートOA-12 (SNOA375)
- 『半導体およびICパッケージの熱指標』(SPRA953)

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6703MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 03MA	Samples
LMH6703MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 03MA	Samples
LMH6703MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AR1A	Samples
LMH6703MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AR1A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

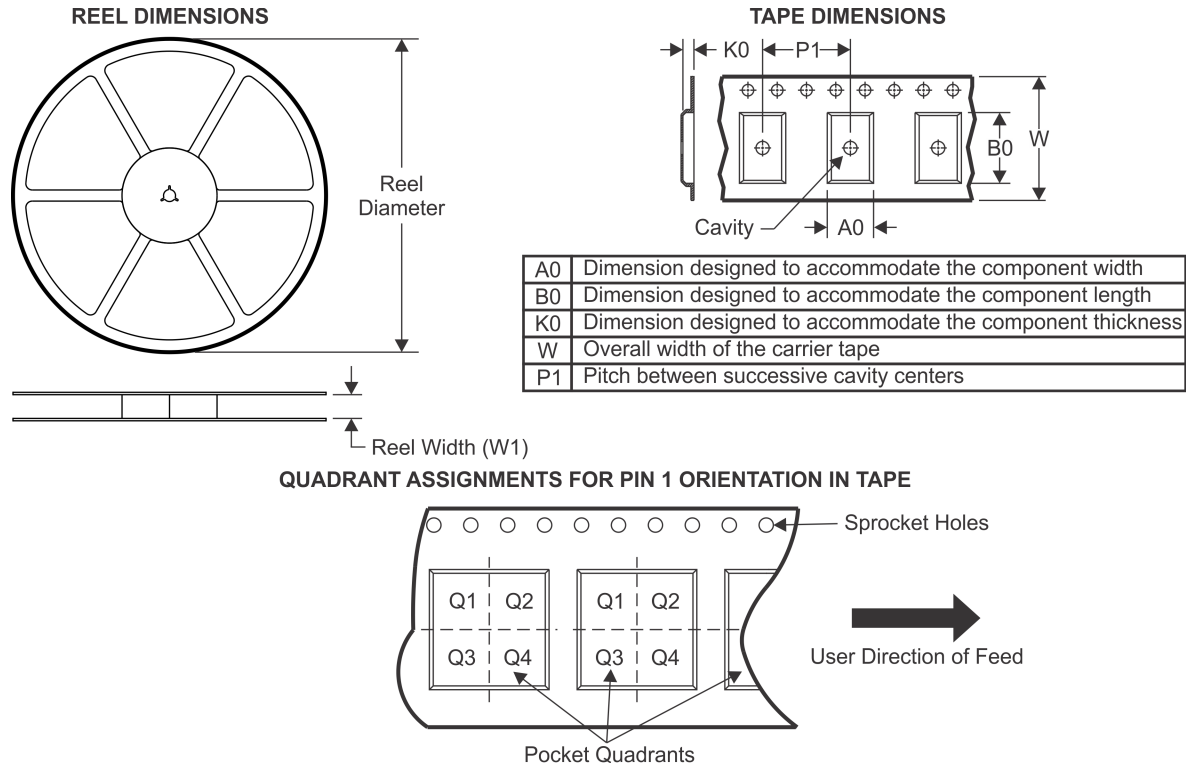
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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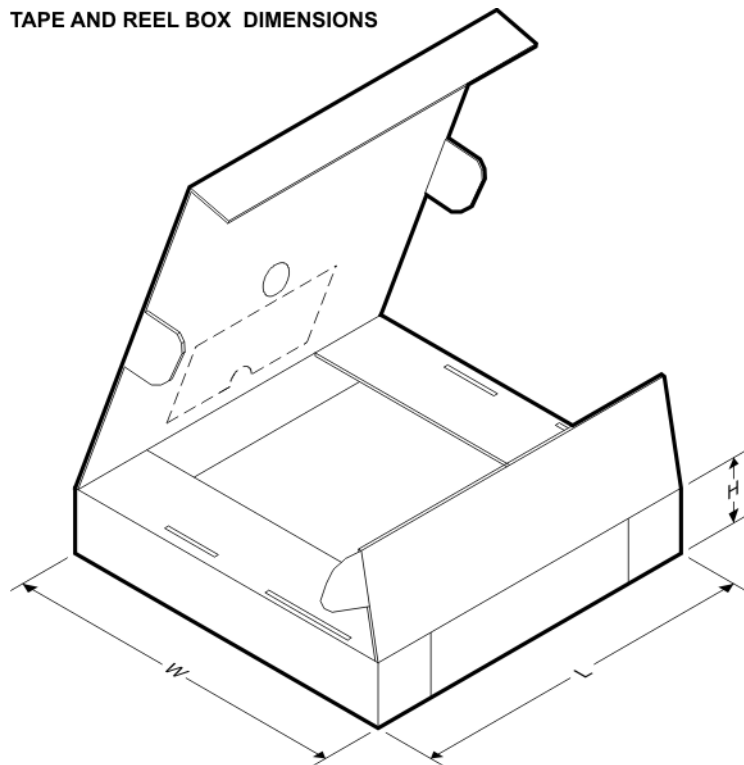
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6703MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6703MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6703MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

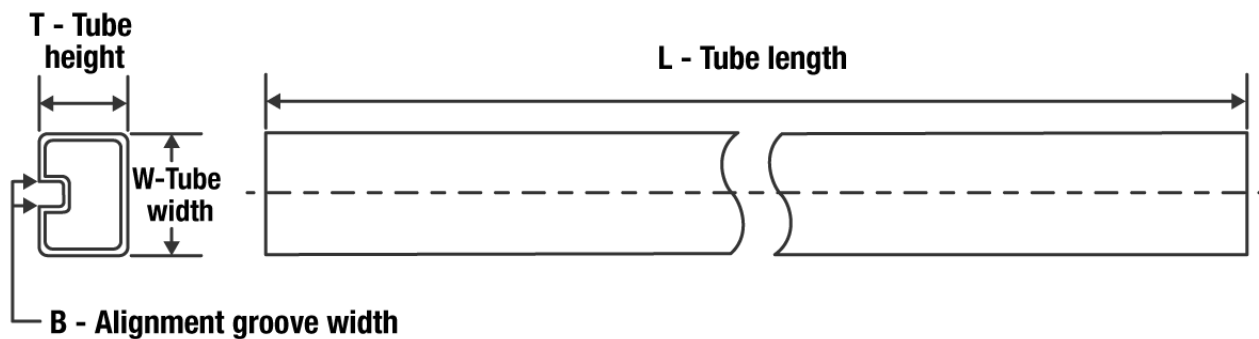
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6703MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6703MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMH6703MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0

TUBE



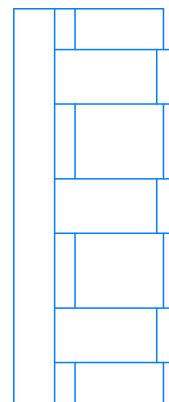
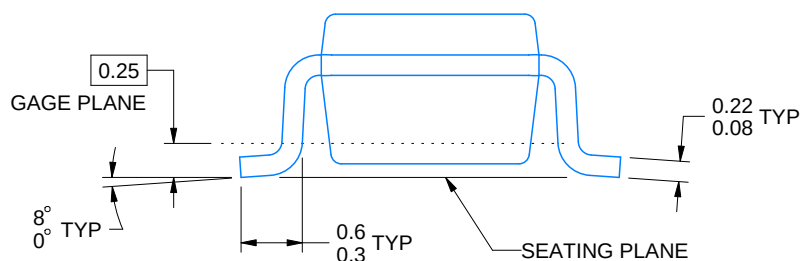
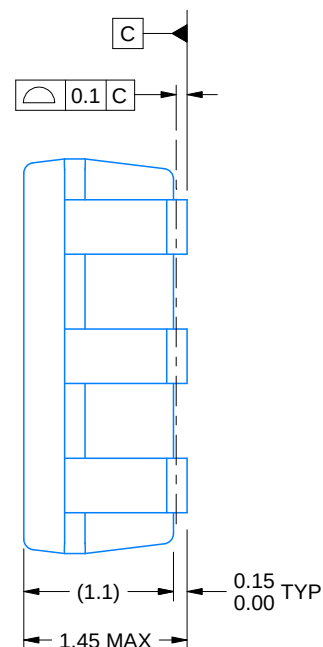
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMH6703MA/NOPB	D	SOIC	8	95	495	8	4064	3.05



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/E 02/2024

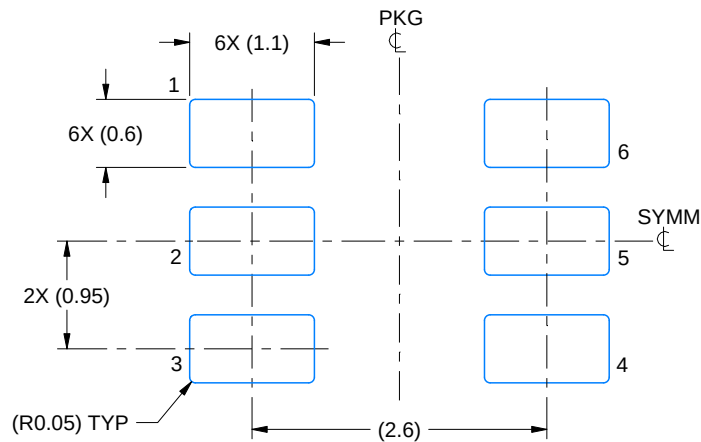
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

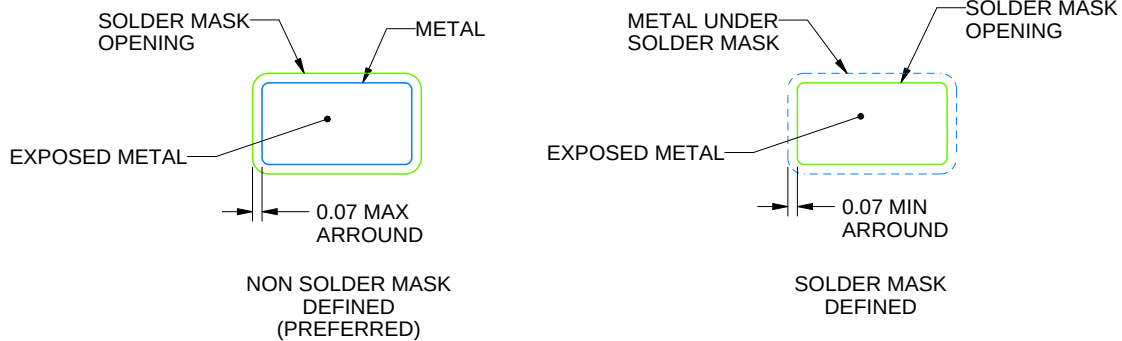
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

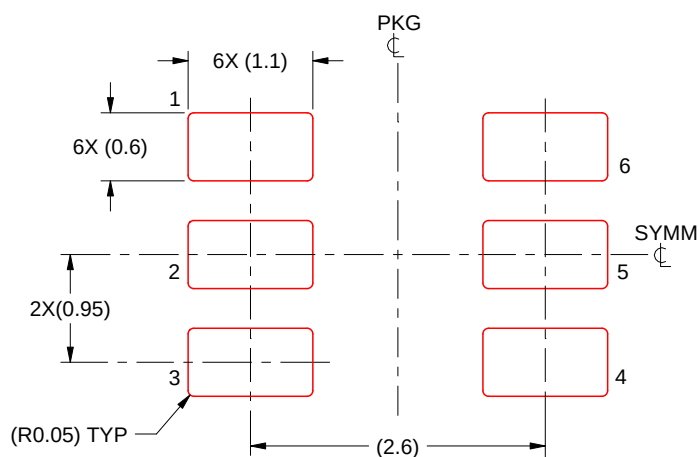
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

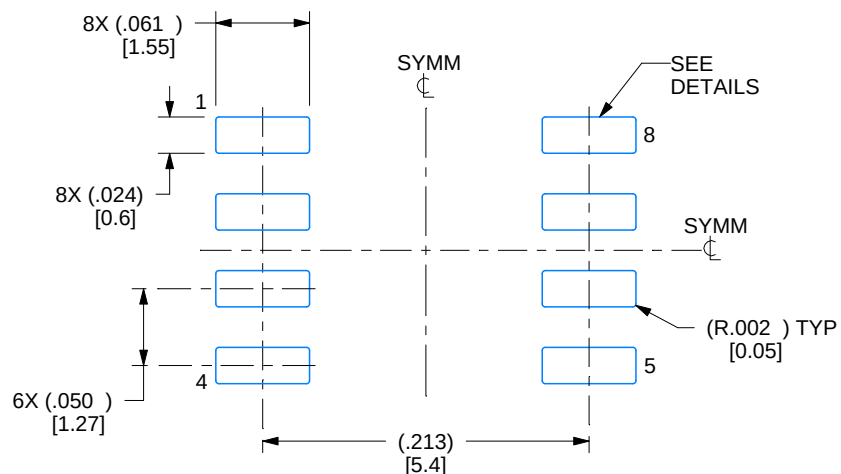


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

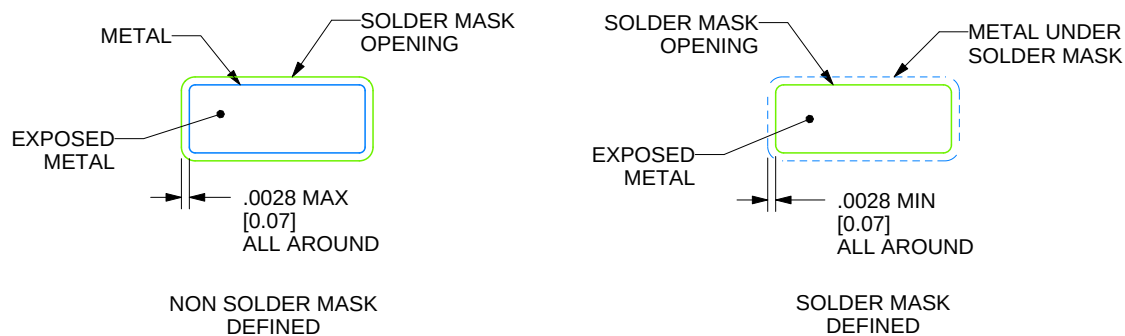
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

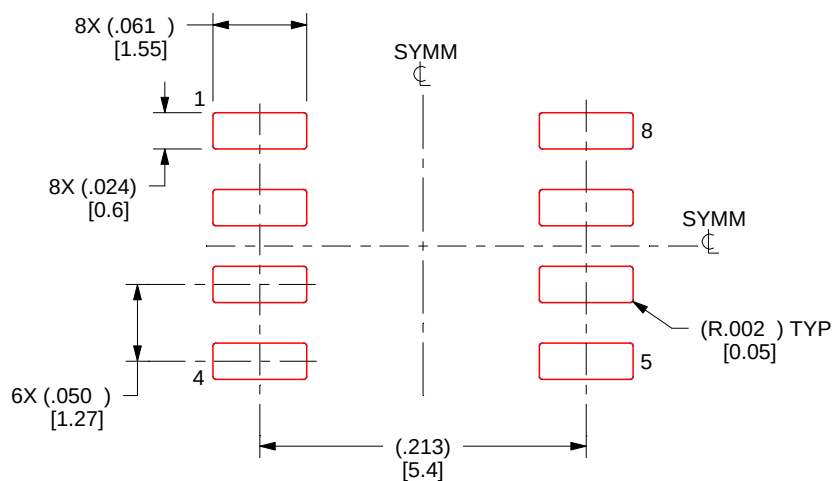
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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