LMK6x 低ジッタ、高性能 BAW 発振器

1 特長

- 以下の範囲内の固定周波数をサポートする高性能差動およびシングルエンド出力発振器
  - LMK6D：1MHz～400MHz、LVDS 出力
  - LMK6H：1MHz～400MHz、HCSL 出力
  - LMK6P：1MHz～400MHz、LVPECL 出力
  - LMK6C：1MHz～200MHz、LVCMOS 出力
- 超低ジッタ：
  - LMK6D/LMK6H/LMK6P：156.25MHz での RMS ジッタ 100fs (標準値) / 125fs (最大値) (12kHz～20MHz)
  - LMK6C：100MHz での RMS ジッタ 350fs (標準値) / 500fs (最大値) (12kHz～20MHz)
  - LMK6H：PCIe Gen 1～Gen 6 準拠
- 10 年の経年劣化やその他のすべての要因を含め、合計周波数安定性 ±25ppm
- 業界標準の最小 DLE および DLF パッケージ
- 産業用拡張温度範囲をサポート：
  - LMK6P/LMK6D/LMK6H：–40℃～85℃
  - LMK6C：–40℃～105℃
- 内蔵 LDO により、堅牢な電源ノイズ耐性を実現：
  - 500kHz リップル時に -72dBc PSRR
- スタートアップ時間：5ms 未満
- 標準周波数：
  - LVCMOS (MHz)：1、2.04、4、8.192、10、12、12.288、16、19.2、20、23.5、24、24.57、25、25.6、26、26.21、27、28.12、32.768、33.333、40、48、49.15、50、54、60、65.53、66、74.25、76.8、80、100、108、125、133.330、156.25
  - 差動 (MHz)：25、26、32.5、50、51.84、54、65、76.8、80、100、108、122.88、125、133.330、148.35、148.5、150、155.52、156.25、161.1328125、200、312.5、400
- デバイスは、1MHz～400MHz の任意の周波数をサポート可能。周波数とサンプルが必要な場合は、テキサス・インスツルメンツの担当者にお問い合わせください

2 アプリケーション

- 56G/112G PAM4 のクロック供給
- 100G/200G/400G/800G 光伝送ネットワークおよびコヒーレント光ファイバ
- ネットワーク機器、スイッチ、ルータ、ライン・カード、SAN、データ・センター、ベースバンド・ユニット (BBU)
- PCIe Gen 1～Gen 6 準拠のリファレンス・クロック
- 産業用アプリケーション
- 試験および測定機器
- ASIC、FPGA、MCU のリファレンス・クロック供給
- 高性能水晶発振器の代替品

3 概要

テキサス・インスツルメンツのバルク弾性波 (BAW) は、超低ジッタ クロック回路を使用して高精度 BAW 共振器をパッケージに直接統合できるマイクロ共振器テクノロジーです。BAW は、シリコン ベースのその他の製造プロセスと同様に TI の工場で全面的に設計および製造されています。

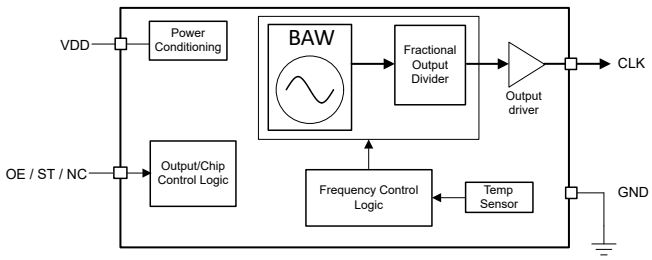
LMK6x デバイスは、共振器源として BAW を採用した超低ジッタ固定周波数発振器です。本デバイスは、特定の動作モードごとに、周波数、電圧、出力タイプ、機能ピンを含めて工場出荷時にプログラムされています。高性能フラクショナル分周器を備えた LMK6x は、規定された範囲内の任意の周波数を生成することが可能です。1 つのデバイス ファミリで、あらゆる周波数のニーズに対応することが可能となります。

このデバイスの高性能クロック供給、機械的安定性、フレキシビリティ、小型パッケージの選択肢は、通信、データおよびエンタープライズ ネットワーク、産業用アプリケーションで使用される高速 SERDES のリファレンスおよびコアクロック向けに設計されています。

パッケージ情報

部品番号	出力タイプ	パッケージ (1)	パッケージ サイズ(2)
LMK6C	LVCMOS	VSON (DLE-4)	3.2mm × 2.5mm
LMK6C		VSON (DLF-4)	2.5mm × 2mm
LMK6D LMK6H LMK6P	LVDS、HCSL、LVPECL	VSON (DLE-6)	3.2mm × 2.5mm
LMK6D LMK6H LMK6P		VSON (DLF-6)	2.5mm × 2mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



LMK6C の概略ブロック図

Table of Contents

4 Device Ordering Information

Use 図 4-1 and 図 4-2 to understand the device nomenclature of the LMK6x orderable options.

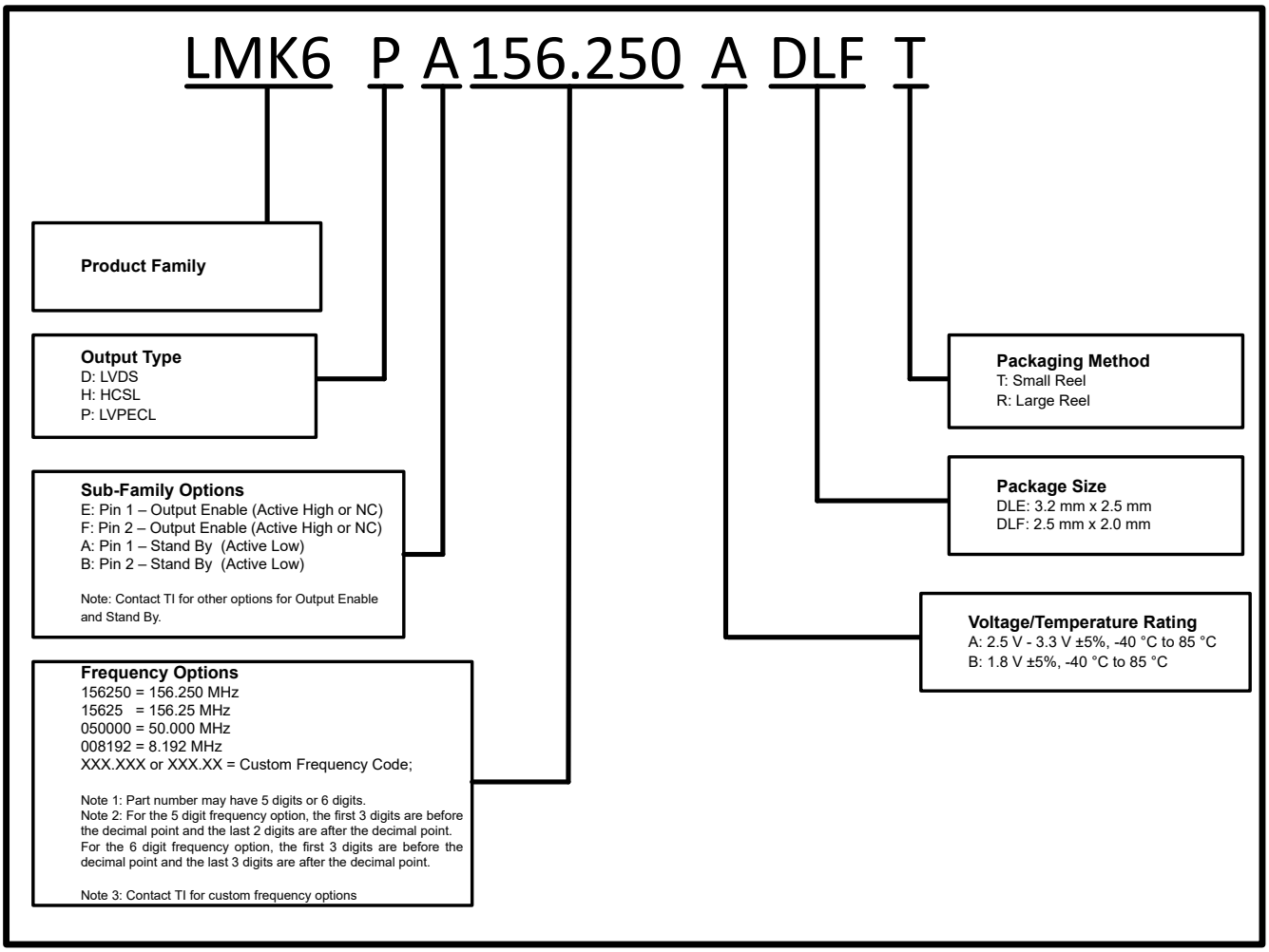


図 4-1. Part Number Guide: LMK6D, LMK6H, and LMK6P

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

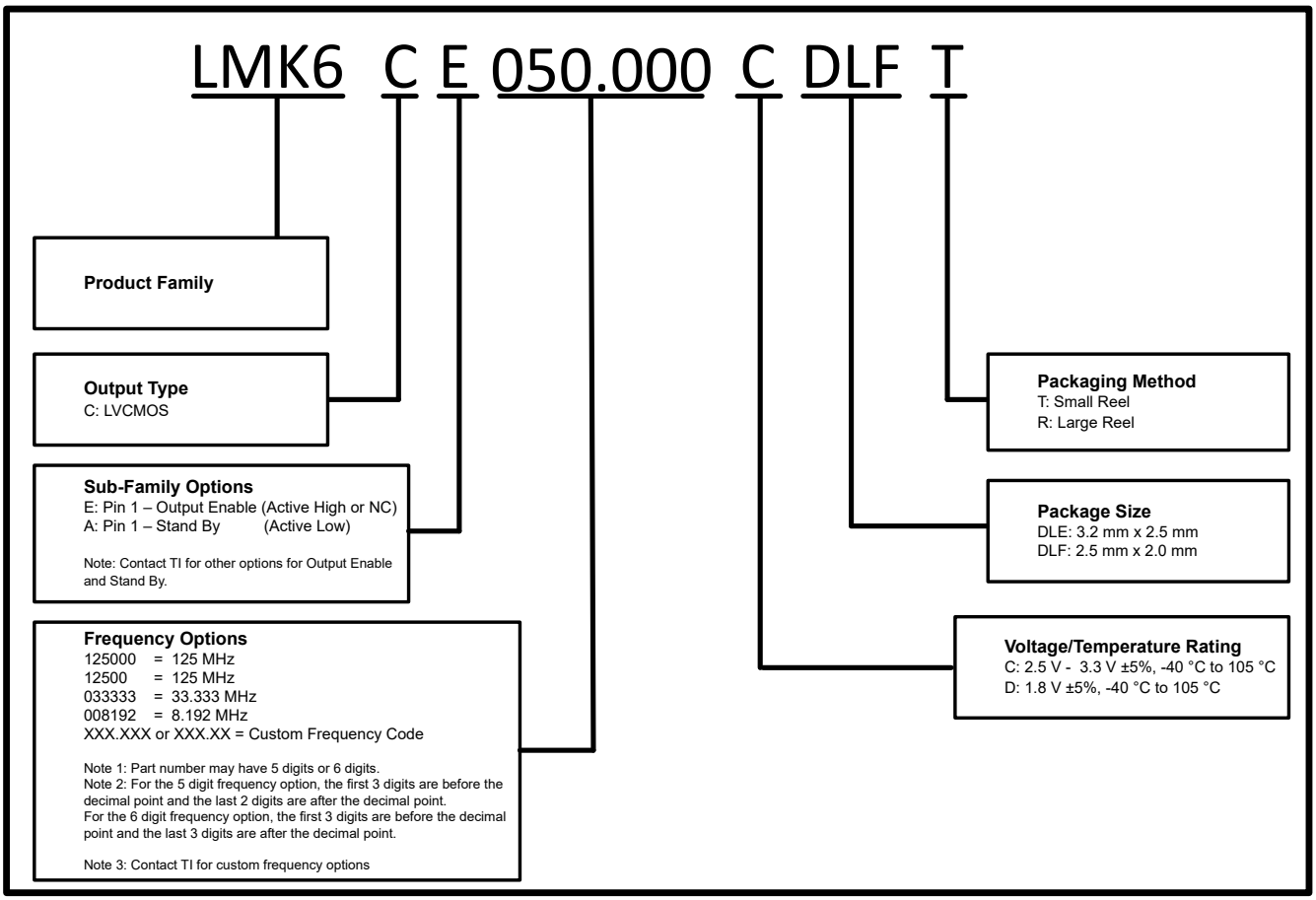


図 4-2. Part Number Guide: LMK6C

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

5 Pin Configuration and Functions

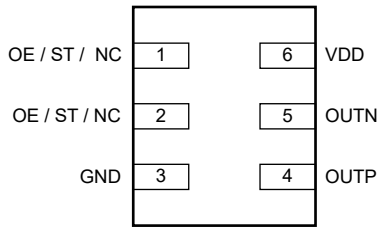


図 5-1. LMK6P, LMK6D, or LMK6H 6-Pin VSON (Top View)

表 5-1. LMK6P, LMK6D, or LMK6H Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	DLE/DLF		
OE / ST / NC	1	I / NC	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See 表 8-1 for more details.
OE / ST / NC	2	NC / I	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See 表 8-1 for more details.
GND	3	G	Device ground
OUTP	4	O	Positive differential output clock
OUTN	5	O	Negative differential output clock
VDD	6	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).

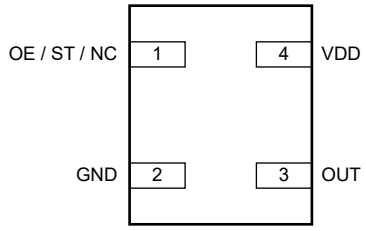


図 5-2. LMK6C 4-Pin VSON (Top View)

表 5-2. LMK6C Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	DLE/DLF		
OE / ST / NC	1	I / NC	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See 表 8-2 for more details.
GND	2	G	Device ground
OUT	3	O	LVCMOS output clock
VDD	4	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage(2)	–0.3	3.63	V
	Device Supply Voltage(3)	–0.3	1.98	V
EN	Logic Input Voltage	–0.3	VDD + 0.3	V
OUTP, OUTN	Clock Output Voltage(4)	–0.3	VDD + 0.3	V
OUT	Clock Output Voltage(5)	–0.3	VDD + 0.3	V
T_J	Junction Temperature		125	℃
T_{STG}	Storage Temperature		150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For all devices with Recommended Operating Voltage of 2.5 V +/- 5% and 3.3 V +/- 5%
(3) For all devices with Recommended Operating Voltage of 1.8 V +/- 5%
(4) For all differential outputs - LMK6D, LMK6H, and LMK6P.
(5) For single ended outputs - LMK6C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Environmental Compliance

		VALUE	UNIT
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
	MIL-STD-883F, Method 2007, Condition A	20	g
Moisture Sensitivity Level (MSL)		MSL1	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage(1)	1.7	1.8	1.9	V
	Device Supply Voltage(2)	2.37	2.5, 3.3	3.5	V
T_A	Ambient temperature(3)	–40		85	°C
	Ambient temperature(4)	–40		105	°C
T_J	Junction temperature			125	°C
t_{RAMP}	VDD power-up ramp time(1) (2)	0.1		100	ms

(1) For all devices with Recommended Operating Voltage of 1.8V +/- 5%
(2) For all devices with Recommended Operating Voltage of 2.5V +/- 5% and 3.3V +/- 5%
(3) For all differential outputs - LMK6D, LMK6H and LMK6P.

(4) For single-ended output - LMK6C.

6.5 Thermal Information

THERMAL METRIC(1)		LMK6D/H/P		UNIT
		DLE (VSON)	DLF (VSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.2	107.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	70.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.3	39.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.1	39.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information

THERMAL METRIC(1)		LMK6C		UNIT
		DLE (VSON)	DLF (VSON)	
		4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.8	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	73.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.5	39.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.8	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.3	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)[7]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD}	Device Power Consumption (LVPECL,VDD = 2.5 V/3.3 V, Excluding load current)	100 MHz		65	82	mA
		156.25 MHz		69	87	mA
		200 MHz		67	85	mA
		312.5 MHz		76	95	mA
		400 MHz		88	108	mA
	Device Power Consumption (LVPECL,VDD = 1.8 V, Excluding load current)	100 MHz		61	79	mA
		156.25 MHz		66	83	mA
		200 MHz		64	82	mA
		312.5 MHz		73	91	mA
		400 MHz		84	104	mA
	Device Power Consumption (HCSL,VDD = 2.5 V/3.3 V, Excluding load current)	100 MHz		65	82	mA
		156.25 MHz		69	87	mA
		200 MHz		67	86	mA
		312.5 MHz		76	96	mA
		400 MHz		88	108	mA
	Device Power Consumption (HCSL,VDD = 1.8 V, Excluding load current)	100 MHz		58	75	mA
		156.25 MHz		62	80	mA
		200 MHz		60	78	mA
		312.5 MHz		69	88	mA
		400 MHz		77	97	mA
	Device Power Consumption (LVDS,VDD = 2.5 V/3.3 V, Excluding load current)	100 MHz		54	71	mA
		156.25 MHz		58	75	mA
		200 MHz		56	74	mA
		312.5 MHz		65	84	mA
		400 MHz		76	96	mA
	Device Power Consumption (LVDS,VDD = 1.8 V, Excluding load current)	100 MHz		52	68	mA
		156.25 MHz		56	72	mA
		200 MHz		54	71	mA
		312.5 MHz		63	80	mA
		400 MHz		74	92	mA
	Device Power Consumption (LVCMOS,VDD = 2.5 V / 3.3 V, with load)	100 MHz		45	62	mA
		156.25 MHz		55	71	mA
		200 MHz		61	77	mA
	Device Power Consumption (LVCMOS,VDD = 1.8 V, with load)	100 MHz		44	59	mA
		156.25 MHz		50	65	mA
		200 MHz		56	72	mA
$I_{DD-STBY}$	Device Stand By current	ST (Stand By) = GND		6	13	mA
I_{DD-PD}	Device current with output disabled (100 MHz)	OE = GND, LVPECL mode, VDD = 3.3 V		48	67	mA
		OE = GND, HCSL mode, VDD = 3.3 V		49	67	mA
		OE = GND, LVDS mode, VDD = 3.3 V		49	66	mA
		OE = GND, LVCMOS mode, VDD = 3.3 V		40	56	mA
LVPECL Output Characteristics						

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{out}	Output Frequency		1		400	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC coupled, VDD = 3.3V	525	645	765	mV
		AC coupled, VDD = 2.5V	450	555	660	mV
		AC coupled, VDD = 1.8 V	280	375	470	mV
		DC coupled, VDD = 2.5 V/ 3.3 V(1)	650	800	950	mV
		DC coupled, VDD = 1.8 V(1)	450	600	750	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing			2×|V_{OD}|		V_{pp}
V_{OS}	Output Common-Mode Voltage	VDD = 3.3 V(1)	1.5	1.6	1.7	V
		VDD = 2.5 V(1)	0.825	0.9	0.975	V
		VDD = 1.8 V(1)	0.45	0.5	0.55	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5 V/ 3.3 V		120	200	ps
		20% to 80% of $V_{OD,DIFF}$, VDD = 1.8 V		120	200	ps
ODC	Output Duty Cycle	VDD = 2.5 V/ 3.3V, measured between 50% points on the waveform	45	50	55	%
		VDD = 1.8 V, measured between 50% points on the waveform	45	50	55	%
LVDS Output Characteristics						
F_{out}	Output Frequency		1		400	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	Under LVDS Load condition	250	350	450	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing			2×|V_{OD}|		V_{pp}
V_{OS}	Output Common Mode Voltage	VDD = 2.5V/3.3 V	1.025	1.2	1.375	V
		VDD = 1.8 V	0.80	0.9	1.0	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$, VDD = 2.5V/3.3 V		150	250	ps
		20% to 80% of $V_{OD,DIFF}$, VDD = 1.8V		150	250	ps
ODC	Output Duty Cycle	VDD = 2.5 V/3.3 V, measured between 50% points on the waveform	45	50	55	%
		VDD = 1.8V, measured between 50% points on the waveform	45	50	55	%
HCSL Output characteristics						
F_{out}	Output Frequency		1		400	MHz
V_{OH}	Output High Voltage	DC coupled, 50 ohms to ground, VDD = 2.5 V/ 3.3 V	650	750	850	mV
		DC coupled, 50 ohms to ground, VDD = 1.8 V	460	560	660	mV
V_{OL}	Output Low Voltage	DC coupled, 50 ohms to ground, VDD = 2.5 V/ 3.3 V	–150	0	150	mV
		DC coupled, 50 ohms to ground, VDD = 1.8 V	–150	0	150	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing			2×|V_{OH} - V_{OL}|		V
V_{cross}	Absolute Crossing Point Voltage	VDD = 3.3 V / 2.5 V, f_{out} = 100 MHz	0.2	0.35	0.50	V_{pp}
		VDD = 1.8 V, f_{out} = 100 MHz	0.15	0.275	0.40	V_{pp}
$V_{cross-delta}$	Absolute Crossing Point Voltage variation	VDD = 3.3 V / 2.5 V / 1.8 V, f_{out} = 100 MHz		0.14		V

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dV/dt	Output Slew Rate	50 ohms to ground; DC coupled load; measured slew rate in +/-150mV from Center.	2		12	V/ns
ΔdV/dt	Output Slew Rate variation				20	%
ODC	Output Duty Cycle		45	50	55	%
LVCMOS Output Characteristics						
F_{out}	Output Frequency		1		200	MHz
V_{OL}	Output Low Voltage	I_{OL} = 3.6 mA, VDD = 1.8 V			0.36	V
		I_{OL} = 5.0 mA, VDD = 2.5 V			0.5	V
		I_{OL} = 6.6 mA, VDD = 3.3 V			0.66	V
V_{OH}	Output High Voltage	I_{OH} = 3.6 mA, VDD = 1.8 V	1.44			V
		I_{OH} = 5.0 mA, VDD = 2.5 V	2			V
		I_{OH} = 6.6 mA, VDD = 3.3 V	2.64			V
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH} -V_{OL}, C_L = 2 pF		0.5	1	ns
ODC	Output Duty Cycle		45	50	55	%
R_{out}	Output Impedance	OE = HIGH	40	50	60	Ω
C_L	Maximum capacitive load	Fout > 50 MHz(3)			15	pF
		Fout < 50 MHz(3)			30	pF
Function Pin Input Characteristics (OE/ST pin)						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.3			V
I_{IL}	Input Low Current	OE = GND	-40			µA
I_{IH}	Input High Current	OE = VDD			40	µA
C_{IN}	Input Capacitance			2		pF
LVDS, HCSL and LVPECL Frequency Tolerance						
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 85℃, variation over rated supply voltage range, and 10 year aging at 25℃.	–25		25	ppm
		Inclusive of: solder shift, initial tolerance, variation over -40℃ to 85℃, variation over supply voltage range.	–20		20	ppm
LVCMOS Frequency Tolerance						
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 105℃, variation over rated supply voltage range, and 10 year aging at 25℃.	-25		25	ppm
		Inclusive of: solder shift, initial tolerance, variation over -40℃ to 105℃, variation over rated supply voltage range.	-20		20	ppm
Differential output PSRR Characteristics						
PSRR	Spur induced by 50 mV power supply ripple at 156.25 MHz output, VDD = 2.5 V/3.3 V, No power supply decoupling capacitor	Sine wave at 50 kHz		–71		dBc
		Sine wave at 100 kHz		–71		dBc
		Sine wave at 500 kHz		–72		dBc
		Sine wave at 1 MHz		–70		dBc

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spur induced by 50 mV power supply ripple at 156.25 MHz output, VDD = 1.8 V, No power supply decoupling capacitor	Sine wave at 50 kHz		–64		dBc
		Sine wave at 100 kHz		–64		dBc
		Sine wave at 500 kHz		–67		dBc
		Sine wave at 1 MHz		–68		dBc
PSRR	Jitter sensitivity to Power supply ripple;	100 kHz sine wave ripple, 3.3 V Supply(2)		4		fs/mV
LVCMOS PSRR Characteristics						
PSRR	Spur induced by 50 mV power supply ripple at 50MHz output, VDD = 2.5V/3.3 V, No power supply decoupling capacitor	Sine wave at 50 kHz		–72		dBc
		Sine wave at 100 kHz		–71		dBc
		Sine wave at 500 kHz		–70		dBc
		Sine wave at 1 MHz		–69		dBc
PSRR	Spur induced by 50 mV power supply ripple at 50MHz output, VDD = 1.8V, No power supply decoupling capacitor	Sine wave at 50 kHz		–50		dBc
		Sine wave at 100 kHz		–50		dBc
		Sine wave at 500 kHz		–52		dBc
		Sine wave at 1 MHz		–55		dBc
PSRR	Jitter sensitivity to Power supply ripple;	100 kHz sine wave ripple, 3.3 V Supply(2)		10		fs/mV
Power-On Characteristics						
t_{START_UP}	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification; Tested with a VDD supply ramp time of around 200 µs			5	ms
t_{OE-EN}	Output Enable Time	Time elapsed from OE = V_{IH} until output is enabled and output is within specification, F_{out} > 10 MHz			25	µs
t_{OE-DIS}	Output Disable Time	Time elapsed from OE = V_{IL} until output is disabled, F_{out} > 10 MHz			1	µs
LVPECL - Clock Output Jitter						
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 156.25 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 156.25 MHz.		–95		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–127		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–146		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–156		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–158		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 312.5 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 312.5 MHz.		–89		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–121		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–140		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–150		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–154		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 100 MHz		125	170	fs
		F_{out} = 125 MHz		100	125	fs
		F_{out} = 155.52 MHz		100	125	fs
		F_{out} = 161.1328125 MHz		110	150	fs
		F_{out} = 200 MHz		120	150	fs
		F_{out} = 400 MHz		100	135	fs

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$RPeriodJITT,RMS$	RMS Period Jitter	F_{out} ≥ 25 MHz		1.7		ps
$RJITT,PK-PK$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		13		ps
LVDS - Clock Output Jitter						
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 156.25 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 156.25 MHz		–95		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–128		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–146		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–156		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–156.5		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 312.5 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 312.5 MHz.		–89		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–122		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–139		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–150		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–153.5		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 100 MHz		140	170	fs
		F_{out} = 125 MHz		110	125	fs
		F_{out} = 155.52 MHz		105	140	fs
		F_{out} = 161.1328125 MHz		125	160	fs
		F_{out} = 200 MHz		125	150	fs
		F_{out} = 400 MHz		100	135	fs
$RPeriodJITT,RMS$	RMS Period Jitter	F_{out} ≥ 25 MHz		1.6		ps
$RJITT,PK-PK$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		13		ps
HCSL - Clock output jitter						

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-cc}$	PCIe Gen 1 Common Clock jitter (jitter limit = 86 ps)	F_{out} = 100 MHz	0.146		6.4	ps
$J_{PCIe1-SRNS}$	PCIe Gen 1 SRNS jitter		0.447		6.99	ps
$J_{PCIe2-cc}$	PCIe Gen 2 Common Clock jitter (jitter limit = 3 ps)		0.103		0.554	ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter		0.135		0.56	ps
$J_{PCIe3-cc}$	PCIe Gen 3 Common Clock jitter (jitter limit = 1 ps)		0.029		0.164	ps
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter		0.033		0.180	ps
$J_{PCIe4-cc}$	PCIe Gen 4 Common Clock jitter (jitter limit = 500 fs)		0.029		0.164	ps
$J_{PCIe4-SRNS}$	PCIe Gen 4 SRNS jitter		0.033		0.180	ps
$J_{PCIe5-cc}$	PCIe Gen 5 Common Clock jitter (jitter limit = 150 fs)		0.007		0.070	ps
$J_{PCIe5-SRNS}$	PCIe Gen 5 SRNS jitter		0.007		0.074	ps
$J_{PCIe6-cc}$	PCIe Gen 6 Common Clock jitter (jitter limit = 100 fs)		0.007		0.042	ps
$J_{PCIe6-SRNS}$	PCIe Gen 6 SRNS jitter		0.009		0.052	ps
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 156.25 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 156.25 MHz.		–95		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–127		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–146		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–156		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–158		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 312.5 MHz		100	125	fs
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 312.5 MHz.		–89		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–121		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–140		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–150		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–154		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 100 MHz		125	170	fs
		F_{out} = 125 MHz		100	125	fs
		F_{out} = 155.52 MHz		100	125	fs
		F_{out} = 161.1328125 MHz		110	150	fs
		F_{out} = 200 MHz		120	150	fs
		F_{out} = 400 MHz		100	135	fs
$R_{PeriodJITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz		1.7		ps
$R_{JITT,PK-PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		13		ps
LVCMOS - Clock Output Jitter						

over Recommended Operating Conditions, Typical Temp = 25°C, Frequency output = 156.25 MHz, VDD = 3.3 V, LVCMOS Output Capacitor load = 2.2 pF (unless otherwise specified)(7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_J	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 156.25 MHz		0.25	0.5	ps
PN_{1k}	Phase Noise at 1 kHz Offset	F_{out} = 156.25 MHz		–100		dBc/Hz
PN_{10k}	Phase Noise at 10 kHz Offset			–128		dBc/Hz
PN_{100k}	Phase Noise at 100 kHz Offset			–143		dBc/Hz
PN_{1M}	Phase Noise at 1 MHz Offset			–150		dBc/Hz
PN_{10M}	Phase Noise at 10 MHz Offset			–152		dBc/Hz
R_J	RMS Jitter (Integration BW: 12 kHz to 5 MHz)	F_{out} = 24 MHz		0.25	0.5	ps
		F_{out} = 25 MHz		0.25	0.5	ps
		F_{out} = 33.33 MHz		0.25	1	ps
	RMS Jitter (Integration BW: 12 kHz to 20 MHz)	F_{out} = 40 MHz		0.5	1	ps
		F_{out} = 50 MHz		0.4	1	ps
		F_{out} = 66.66 MHz		0.5	1	ps
		F_{out} = 74.25 MHz		0.3	0.5	ps
		F_{out} = 78 MHz		0.35	0.5	ps
		F_{out} = 100 MHz		0.35	0.5	ps
		F_{out} = 125 MHz		0.35	0.5	ps
$R_{PeriodJITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz		1.5		ps
$R_{JITT,PK-PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		13		ps

(1) DC Load condition
(2) Measured using TI LMK6x Evaluation Module;
(3) Refer to *Application Curves section* for Rise time and fall time details for different capacitor load values.
(4) The Jitter specifications are based on design and characterization

6.8 Timing Diagrams

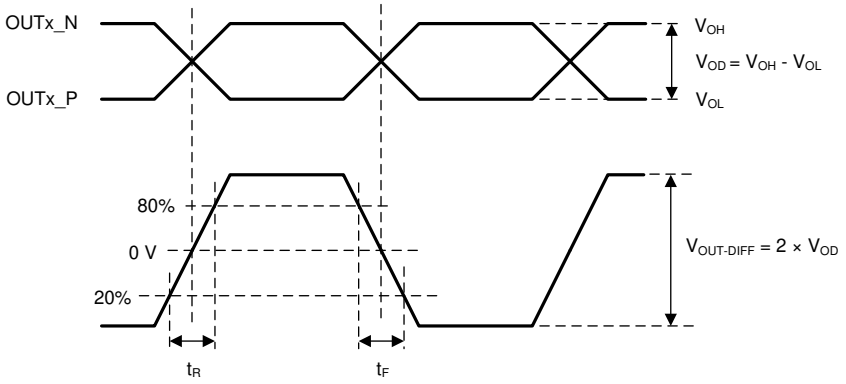


図 6-1. Differential Output Voltage and Rise/Fall Time

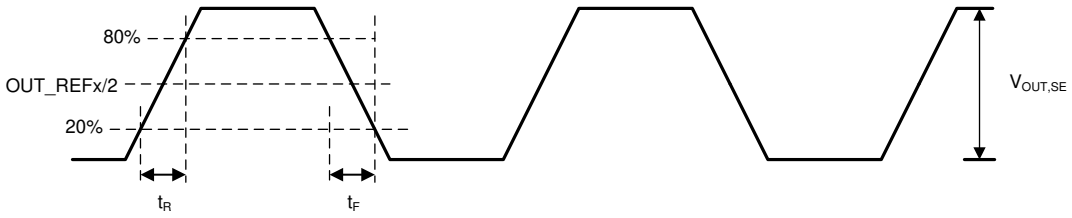


図 6-2. Single-Ended Output Voltage and Rise/Fall Time

6.9 Typical Characteristics

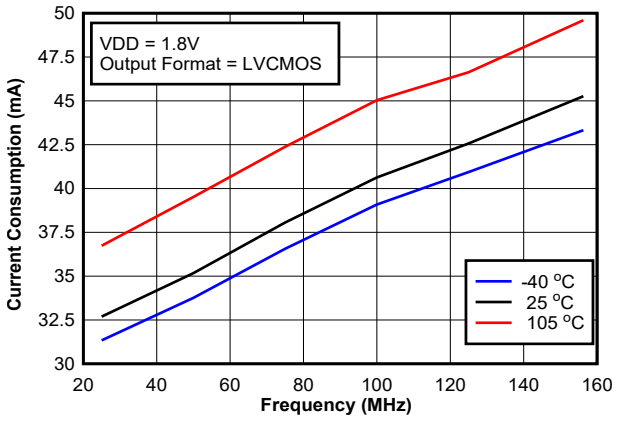


図 6-3. Current Consumption vs Frequency (LVCMOS, 1.8 V)

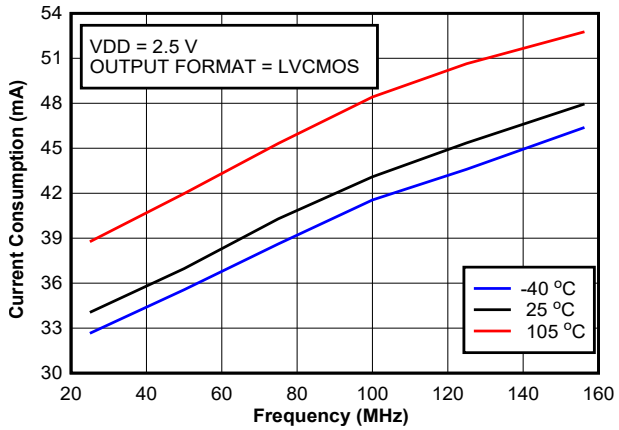


図 6-4. Current Consumption vs Frequency (LVCMOS, 2.5 V)

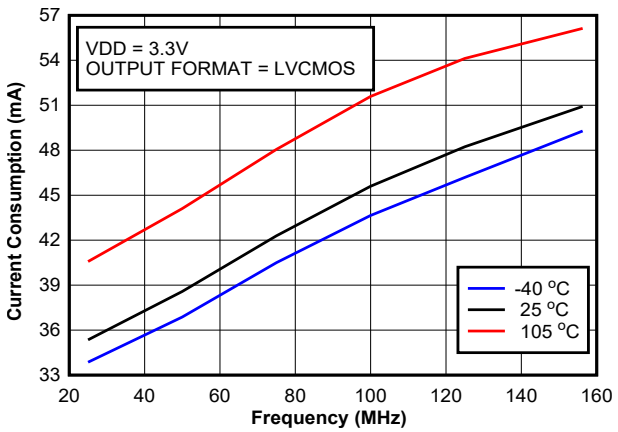


図 6-5. Current Consumption vs Frequency (LVCMOS, 3.3 V)

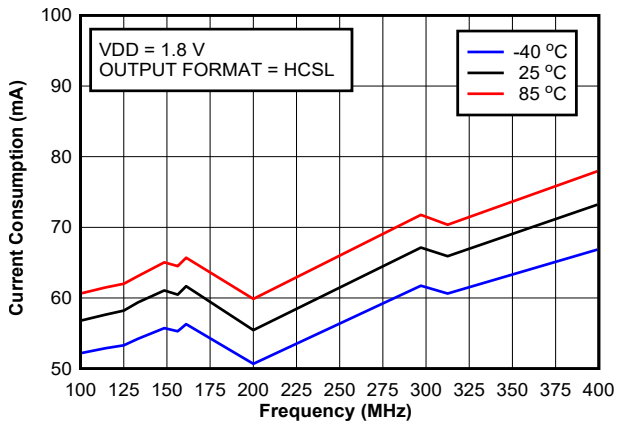


図 6-6. Current Consumption vs Frequency (HCSL, 1.8 V)

6.9 Typical Characteristics (continued)

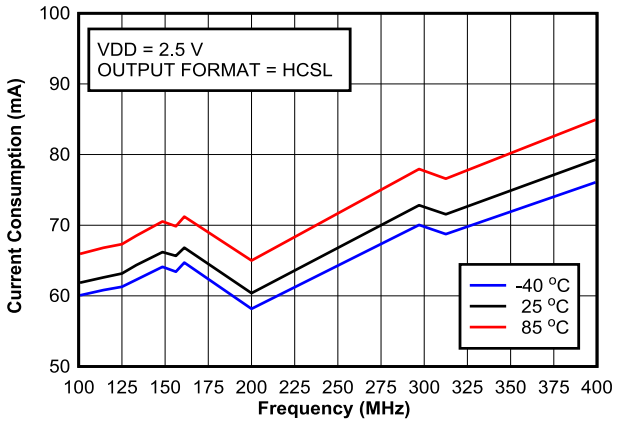


図 6-7. Current Consumption vs Frequency (HCSL, 2.5 V)

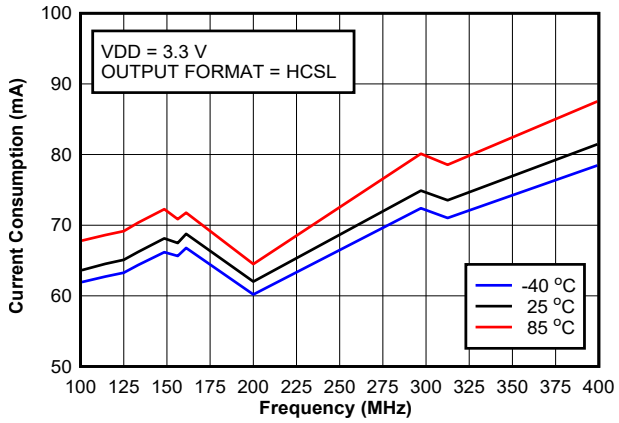


図 6-8. Current Consumption vs Frequency (HCSL, 3.3 V)

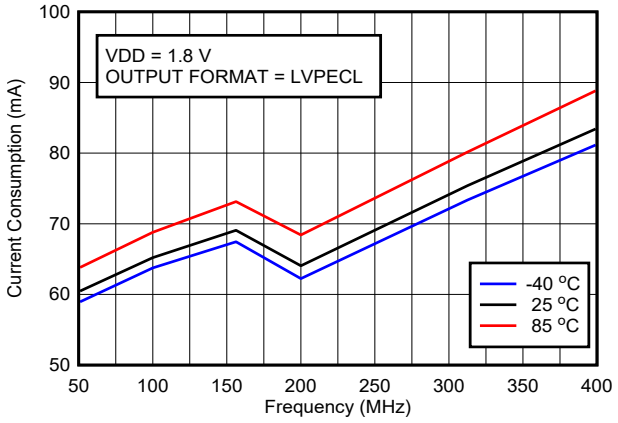


図 6-9. Current Consumption vs Frequency (LVPECL, 1.8 V)

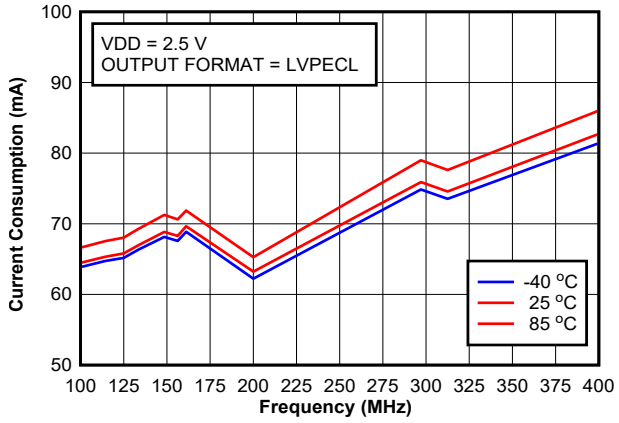


図 6-10. Current Consumption vs Frequency (LVPECL, 2.5 V)

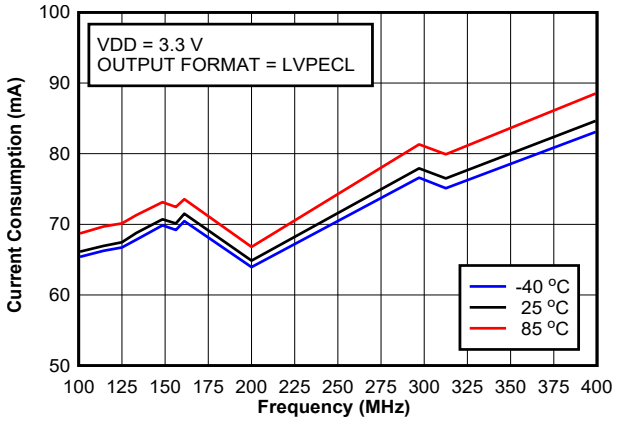


図 6-11. Current Consumption vs Frequency (LVPECL, 3.3 V)

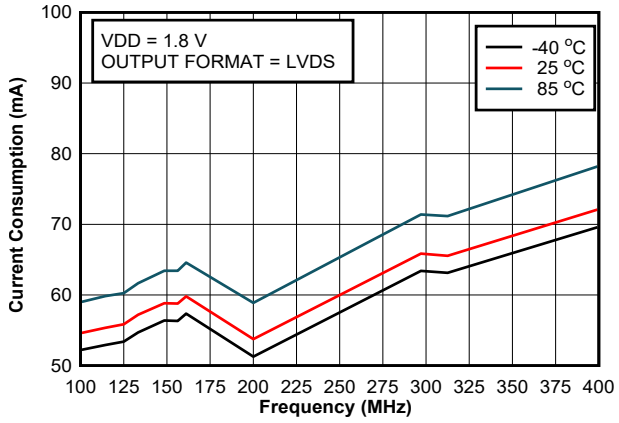


図 6-12. Current Consumption vs Frequency (LVDS, 1.8 V)

6.9 Typical Characteristics (continued)

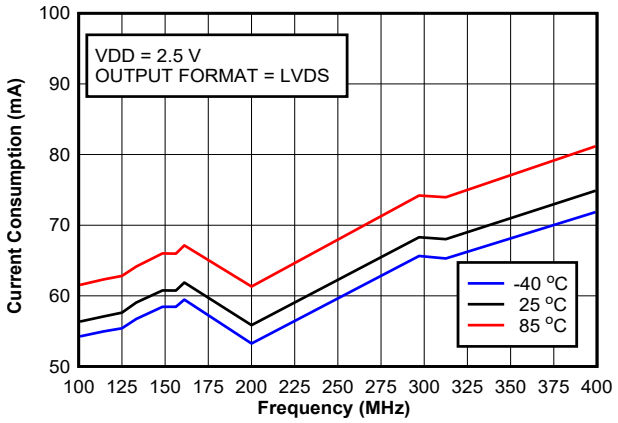


図 6-13. Current Consumption vs Frequency (LVDS, 2.5 V)

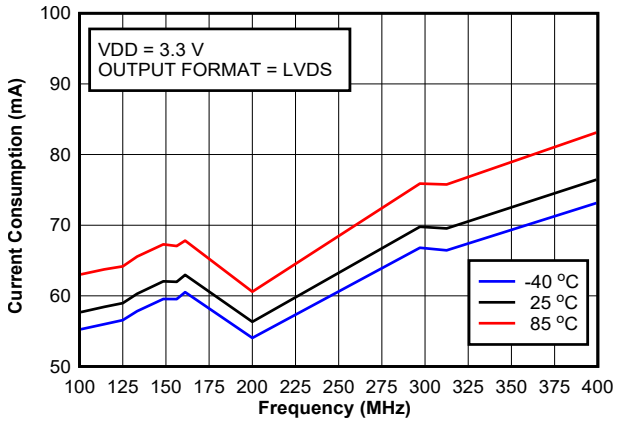


図 6-14. Current Consumption vs Frequency (LVDS, 3.3 V)

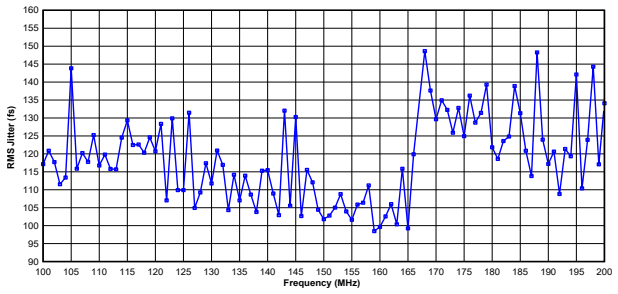


図 6-15. RMS Jitter vs Frequency (100 MHz to 200 MHz) for LVPECL, HCSL; TYPICAL 3.3 V, 25°C

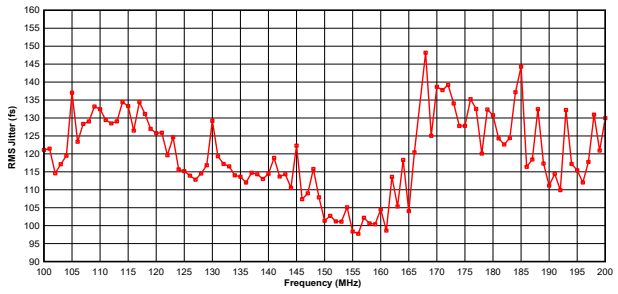


図 6-16. RMS Jitter vs Frequency (100 MHz to 200 MHz) for LVDS; TYPICAL 3.3 V, 25°C

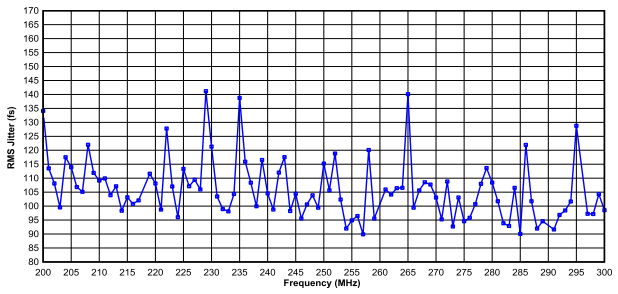


図 6-17. RMS Jitter vs Frequency (200 MHz to 300 MHz) for LVPECL, HCSL; TYPICAL 3.3 V, 25°C

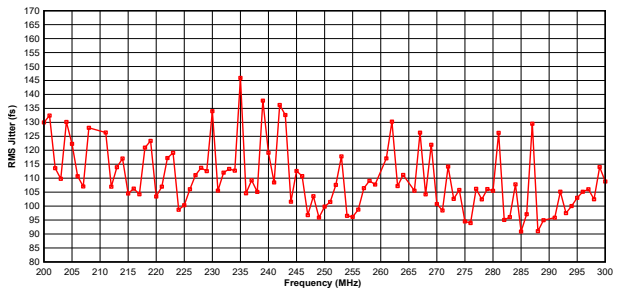


図 6-18. RMS Jitter vs Frequency (200 MHz to 300 MHz) for LVDS; TYPICAL 3.3 V, 25°C

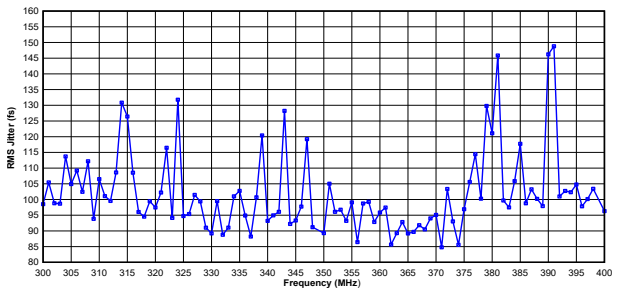


図 6-19. RMS Jitter vs Frequency (300 MHz to 400 MHz) for LVPECL, HCSL; TYPICAL 3.3 V, 25°C

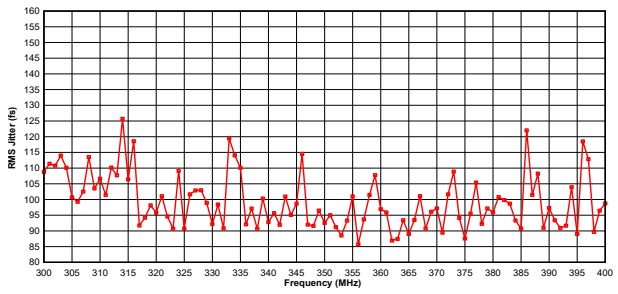


図 6-20. RMS Jitter vs Frequency (300 MHz to 400 MHz) for LVDS; TYPICAL 3.3 V, 25°C

6.9 Typical Characteristics (continued)

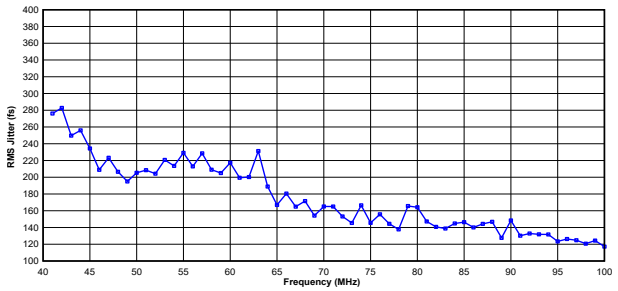


図 6-21. RMS Jitter vs Frequency (Below 100 MHz) for LVPECL, HCSL; TYPICAL 3.3 V, 25°C

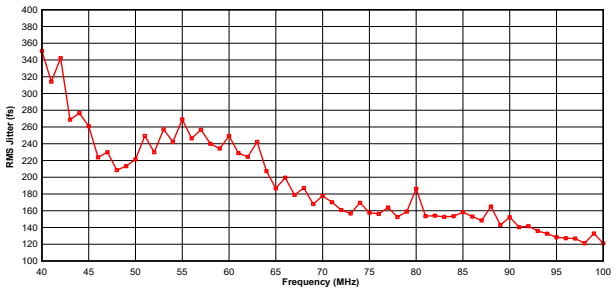


図 6-22. RMS Jitter vs Frequency (Below 100 MHz) for LVDS; TYPICAL 3.3 V, 25°C

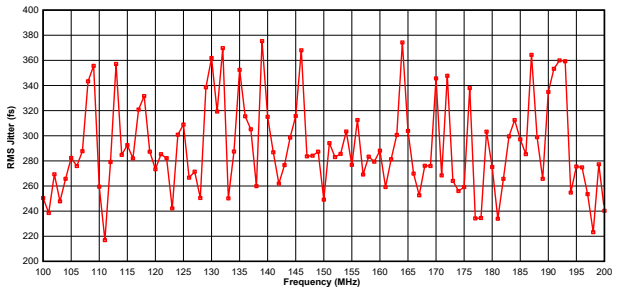


図 6-23. RMS Jitter vs Frequency (100 MHz - 200 MHz) for LVCMOS; TYPICAL 3.3 V, 25°C

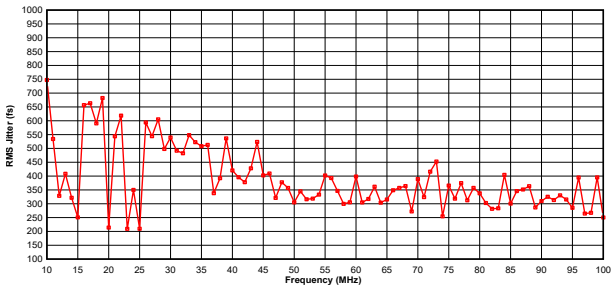


図 6-24. RMS Jitter vs Frequency (10 MHz - 100 MHz) for LVCMOS; TYPICAL 3.3 V, 25°C

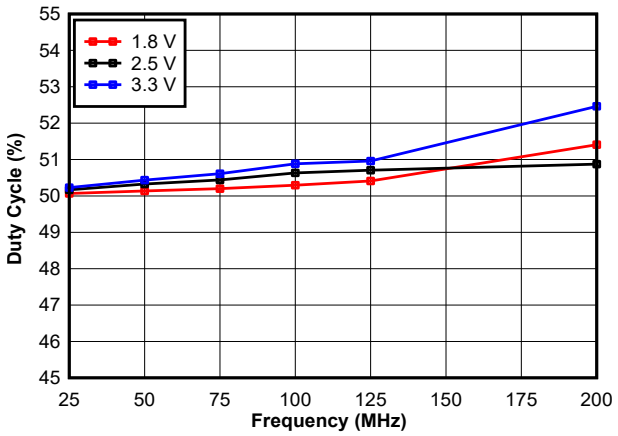


図 6-25. Duty Cycle (%) vs Frequency vs Power Supply; 25°C

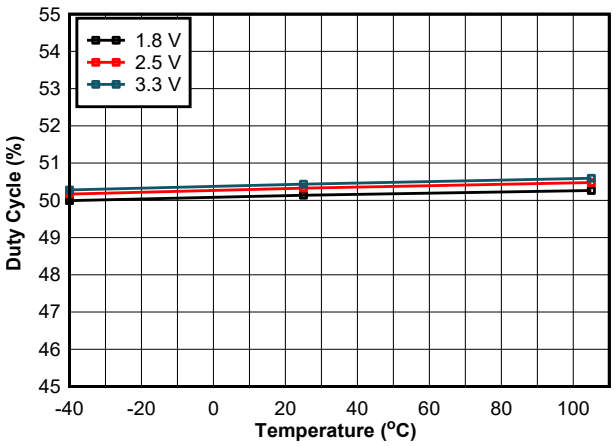


図 6-26. Duty Cycle (%) vs Temperature vs Power Supply; 50-MHz Frequency

6.9 Typical Characteristics (continued)

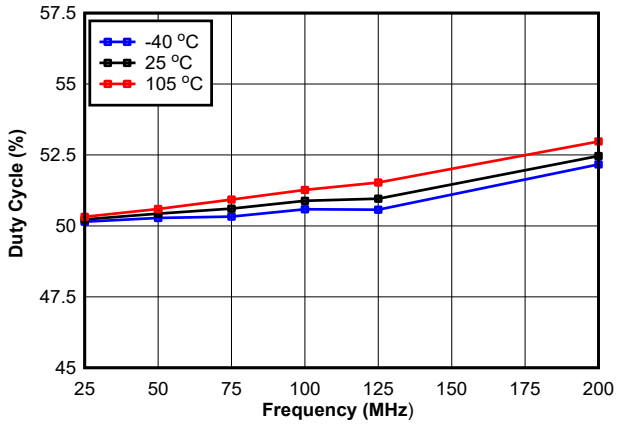


図 6-27. Duty Cycle (%) vs Frequency Over Temperature Range for LVCMOS; 3.3 V

7 Parameter Measurement Information

7.1 Device Output Configurations

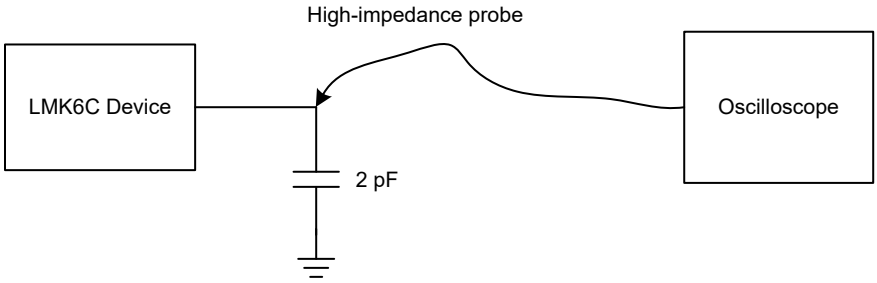


図 7-1. LMK6C Output Test Configuration

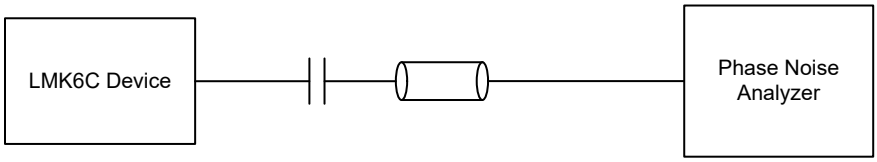


図 7-2. LMK6C Output Phase Noise Test Configuration

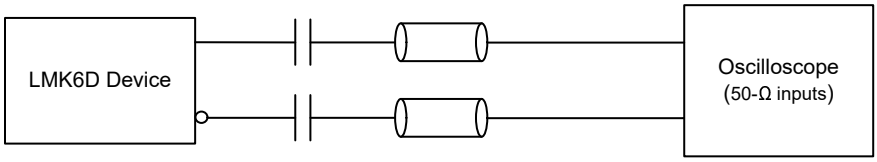


図 7-3. LMK6D Output Test Configuration

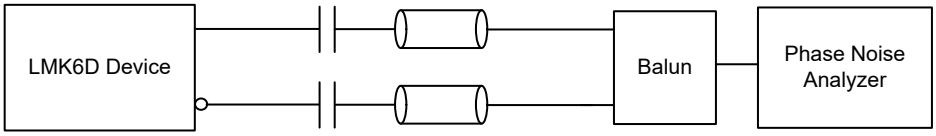


図 7-4. LMK6D Output Phase Noise Configuration

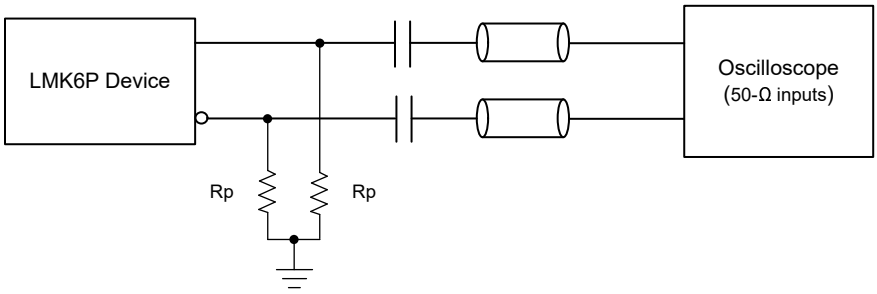


図 7-5. LMK6P Output Test Configuration

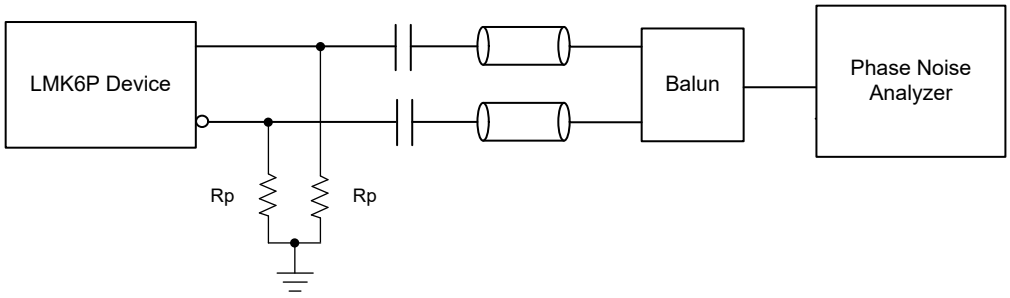


図 7-6. LMK6P Output Phase Noise Configuration

表 7-1. LMK6P Output Test configuration and Phase Noise Configuration Rp Values

SUPPLY (V)	Rp (Ω)
3.3 V	207.5
2.5 V	112.5
1.8 V	83.3

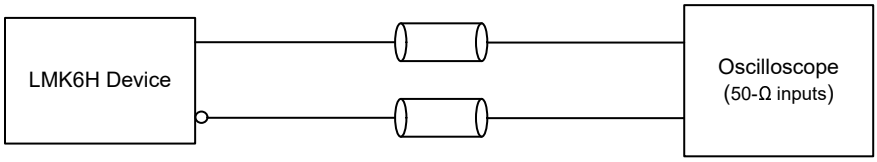


図 7-7. LMK6H Output Test Configuration

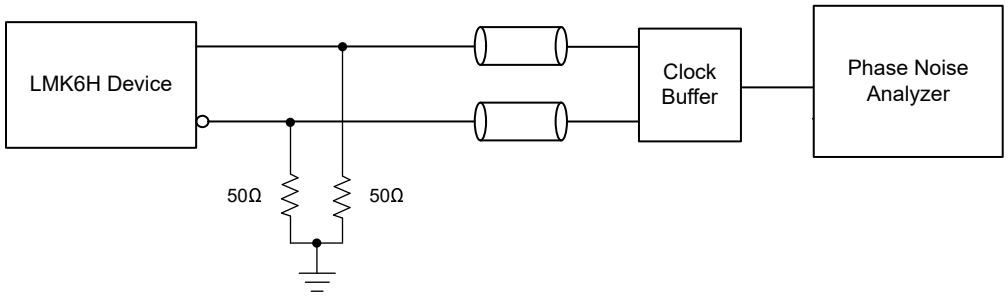


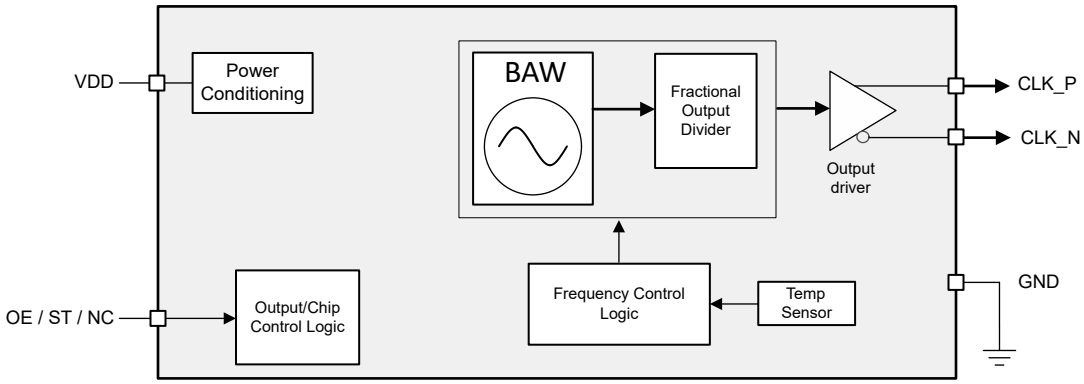
図 7-8. LMK6H Output Phase Noise Configuration

8 Detailed Description

8.1 Overview

The LMK6x is a fixed-frequency BAW based oscillator that can provide ultra-low jitter for both differential and single-ended output types.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5 GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by adsorption of surface contaminants and can be directly placed in a non-hermetic plastic package with the oscillator IC in small standard oscillator footprints. Refer to BAW for more details on BAW technology.

8.3.2 Device Block-Level Description

The device contains a BAW oscillator, a Fractional Output Divider (FOD), and output driver, which together generates a pre-programmed output frequency. Temperature variations of oscillation frequency are continuously monitored by internal precision temperature sensor and provided as input to the frequency control logic block. Using this frequency control logic block, frequency corrections are performed internally for maintaining the output frequency within ±25 ppm across temperature range and aging. The output driver is capable of providing both single-ended LVCMOS and differential LVPECL, LVDS, and HCSL output formats. The device contains an internal LDO which reduces the power supply noise, resulting in low noise clock output.

8.3.3 Function Pin(s)

Pin 1 on the LMK6C and pin 1 or pin 2 on the LMK6P, LMK6D, and LMK6H are the function pins which have multiple functions based on the orderable part number. The function can be used as Output Enable (OE), Stand By (ST) or No Connect (NC). Options for both Active High and Active Low are available for OE and ST. Contact TI for Active Low options. 表 8-1 lists the functions of pin 1 and pin 2 for differential output 6-pin packages and 表 8-2 lists the functions of pin 1 for single-ended outputs.

表 8-1. Function Pin Descriptions for 6-Pin Packages (LMK6D, LMK6H, LMK6P)

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION	OTHER FUNCTIONAL PIN CONFIGURATION
E (Pin 1)	Output Enable (Active High / NC)	**HIGH or No Connect** : Output active at Specified Frequency **LOW** : Output disabled, high impedance; current consumption is given by I_{DD-PD}	Pin 2 can be left floating or grounded
F (Pin 2)	Output Enable (Active High / NC)	**HIGH or No Connect** : Output active at Specified Frequency **LOW** : Output disabled, high impedance; current consumption is given by I_{DD-PD}	Pin 1 can be left floating or grounded
A (Pin 1)	Standby (Active Low)	**LOW** : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ **HIGH or No Connect** : Output active at Specified Frequency	Pin 2 can be left open or grounded
B (Pin 2)	Standby (Active Low)	**LOW** : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ **HIGH or No Connect** : Output active at Specified Frequency	Pin 1 can be left open or grounded

表 8-2. Function Pin Descriptions for 4-Pin Packages (LMK6C)

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
E (Pin 1)	Output Enable (Active High / NC)	**HIGH or No Connect** : Output active at Specified Frequency **LOW** : Output disabled, high impedance; current consumption is given by I_{DD-PD}
A (Pin 1)	Standby (Active Low)	**LOW** : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ **HIGH or No Connect** : Output active at Specified Frequency

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of the *Electrical Characteristics* table. The return to the output clock active time corresponds to same as the initial start-up time.

The Function Pin is driven internally with resistance >100 kΩ.

8.3.4 Clock Output Interfacing and Termination

These figures show the recommended output interfacing and termination circuits.

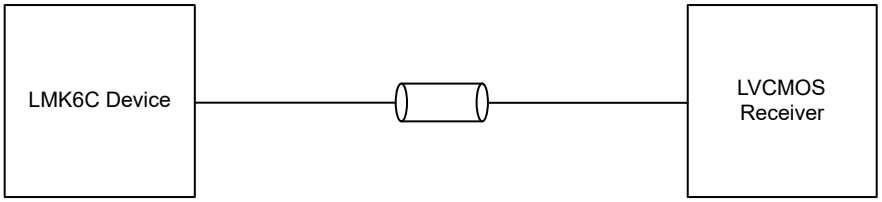


図 8-1. LMK6C Output to LVCMOS Receiver

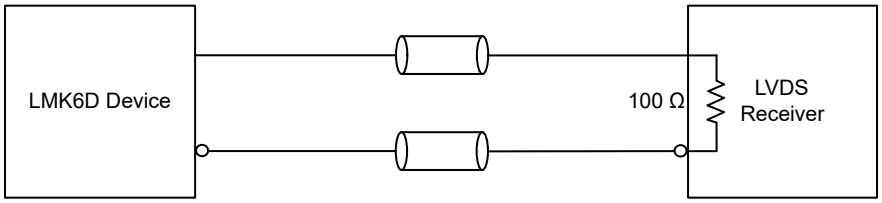


図 8-2. LMK6D Output DC-Coupled to LVDS Receiver With Internal Termination/Biasing

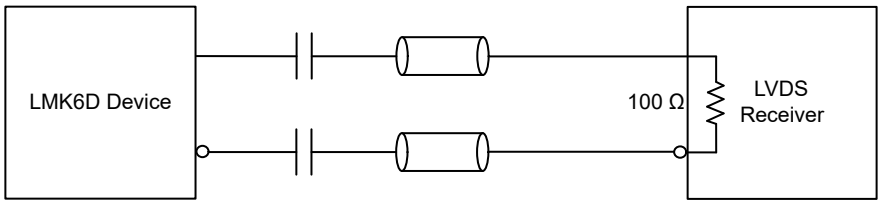


図 8-3. LMK6D Output AC Coupled to LVDS Receiver With Internal Termination/Biasing

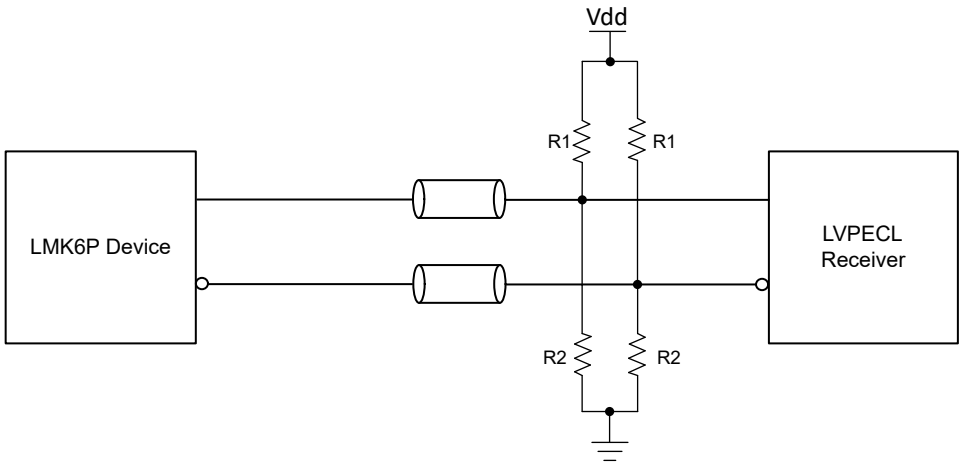


図 8-4. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)

表 8-3. LMK6P T-Network DC-Coupled Resistor Values

SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	133	82
2.5	250	62.5
1.8	450	56.5

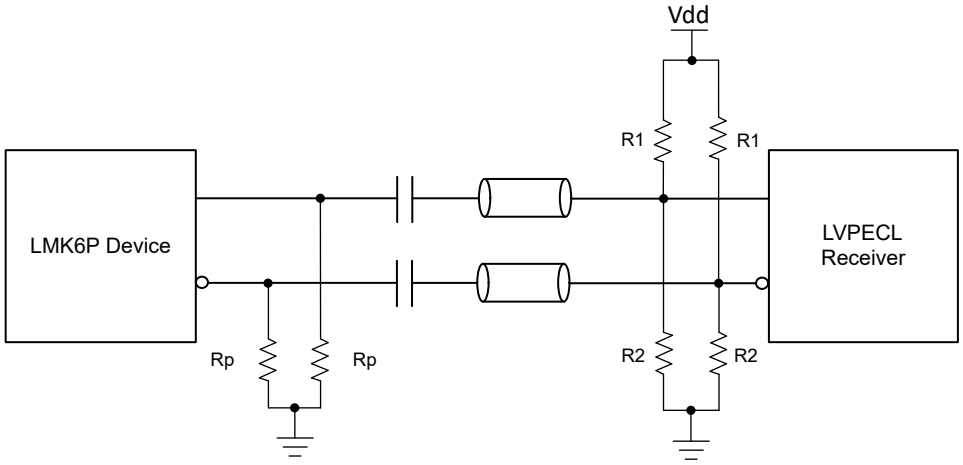


図 8-5. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)

表 8-4. LMK6P T-Network AC-Coupled Resistor Values

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	133	82
2.5	112.5	250	62.5
1.8	83.3	450	56.6

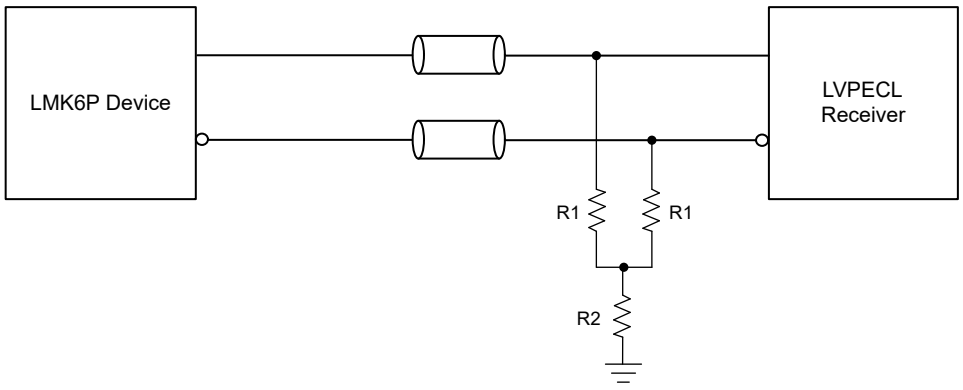


図 8-6. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)

表 8-5. LMK6P Y-Network DC-Coupled Resistor Values

SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	50	78.8
2.5	50	31.3
1.8	50	16.7

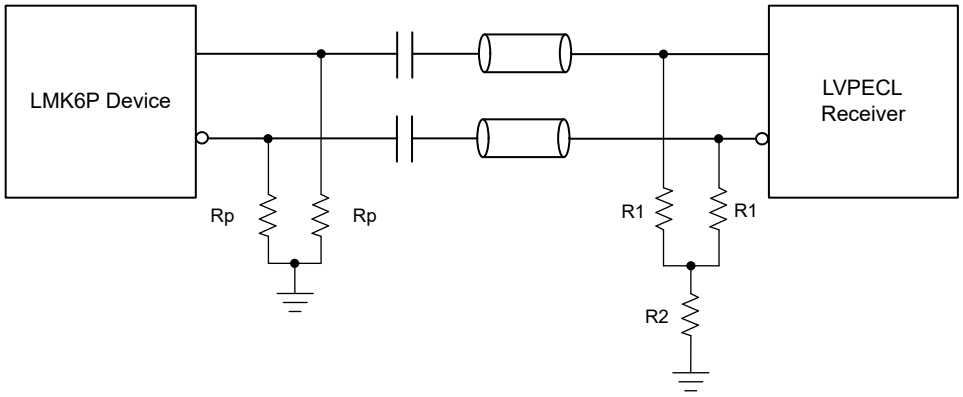


図 8-7. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)

表 8-6. LMK6P Y-Network AC-Coupled Resistor Values

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	50	78.8
2.5	112.5	50	31.3
1.8	83.3	50	16.7

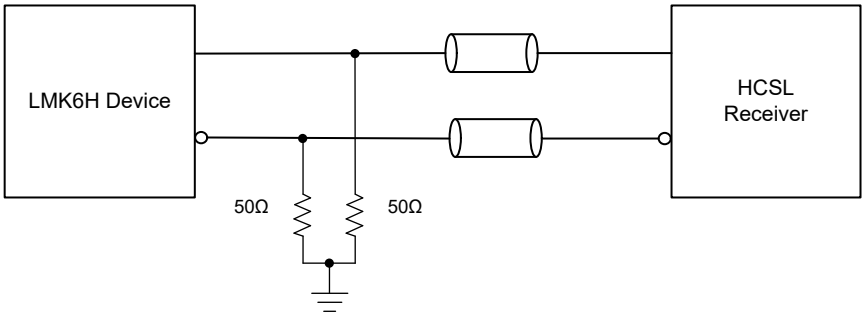


図 8-8. LMK6H Output to HCSL Receiver With External Termination

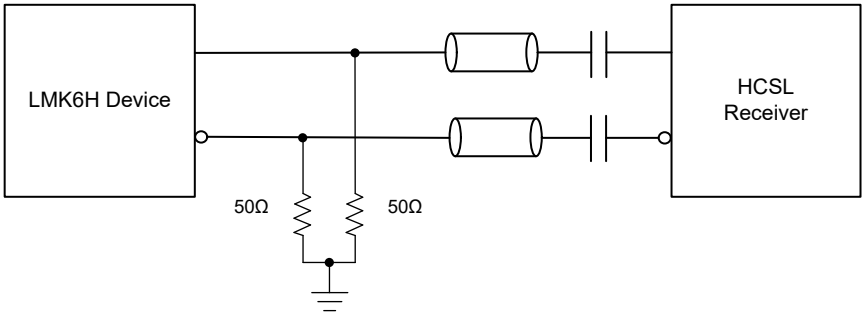


図 8-9. LMK6H Output AC-Coupled to HCSL Receiver With External Termination

8.3.5 Temperature Stability

図 8-10 shows the frequency variation of the LMK6x differential output oscillator over the temperature range of –40°C to 85°C for total of 60 units. 図 8-11 shows the frequency variation of the LMK6C single-ended output oscillator over the operating temperature range of –40°C to 105°C. These plots represent the typical temperature

stability of the device, remaining below ±10 ppm. The devices are soldered onto the evaluation board as per the standard soldering profile and frequency variation measurements are carried out. The output frequency is 156.25 MHz for these tests.

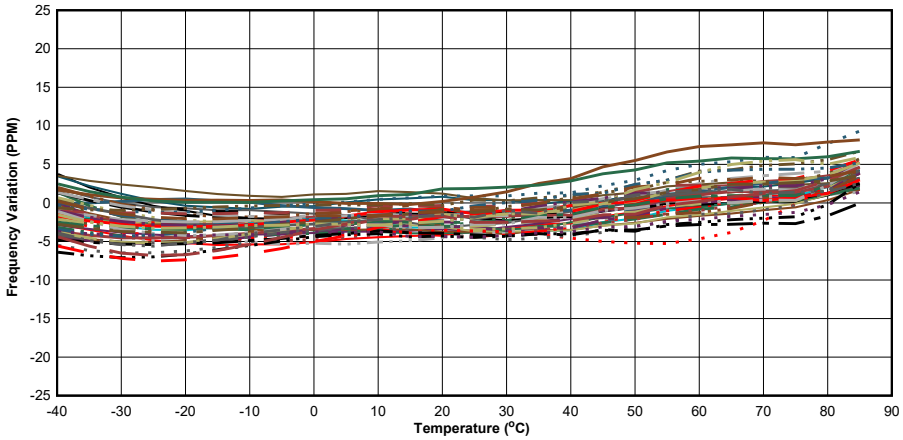


図 8-10. Frequency Change Over Temperature (LMK6x Differential Output Device)

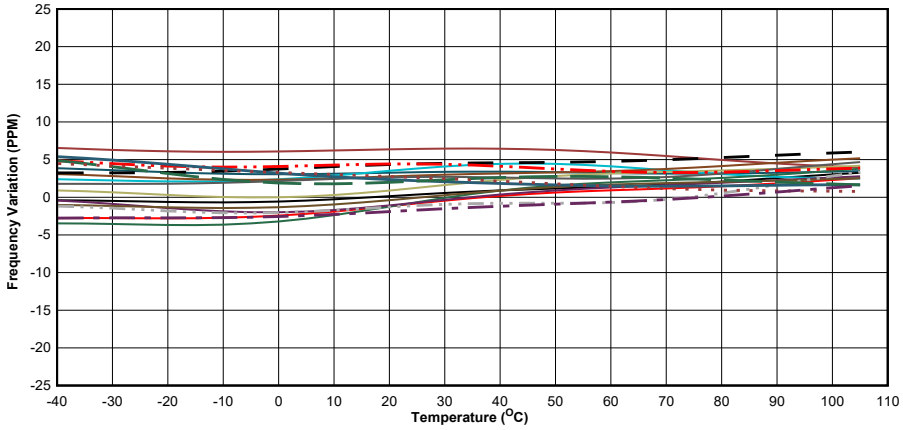


図 8-11. Frequency Change Over Temperature (LMK6C Single-Ended Output Device)

8.3.6 Mechanical Robustness

For reference oscillators, vibration and shock are common causes for increased phase noise and jitter, frequency shift and spikes, or even physical damages to the resonator and the package. Compared to quartz crystals, the BAW resonator is more immune to vibration and shock due to its orders of magnitude, smaller mass, and higher frequency, which means force applied to the device from acceleration is much smaller due to smaller mass.

図 8-12 shows the LMK6x BAW oscillator vibration performance. In this test, the LMK6x oscillator mounted on an EVM is subject to 10g acceleration force, ranging from 50 Hz to 2 kHz in x, y, and z-axis. Phase noise trace with spur due to vibration is captured using Keysight E5052B and frequency deviation is calculated from the spur power. Then the frequency deviation is converted to ppb by noting the carrier frequency and normalized to ppb/g. Finally, the RMS sum of ppb/g along all three axes is reported as the Vibration sensitivity in ppb/g. LMK6x performance under vibration is approximately 2 ppb/g while most quartz oscillators best case is 3 ppb/g and worse can be above 10 ppb/g.

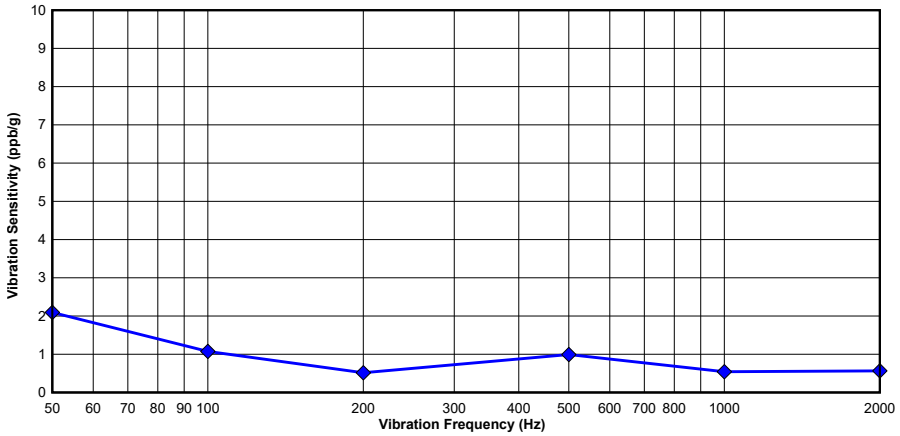


図 8-12. LMK6X BAW Oscillator Vibration Performance

8.4 Device Functional Modes

The LMK6x BAW Oscillator is a fixed output frequency device and does not require any programming. The device pin 1 (and pin 2 for a 6-pin device) has different functions. See the *Function Pin(s)* section for more information on the function pins.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK6x is high-performance, fixed-frequency oscillator that can be used as a reference clock. The product family supports any output frequency between 1 MHz to 400 MHz for differential LMK6D, LMK6H, LMK6P or 1 MHz to 200 MHz for singled-ended LVCMOS clock output types, and 1.8-V or 2.5-V through 3.3-V supply rails.

9.2 Typical Application

For reference schematic implementation for LMK6x family of oscillators, refer to the *LMK6EVM User's Guide* for bypass capacitor and AC-coupling capacitor value recommendations. Refer to the *Clock Output Interfacing and Termination* section for output clock required termination and biasing.

図 9-1 shows a typical application example. The LMK6D differential oscillator is used as an input to the LVDS buffer input in this example.

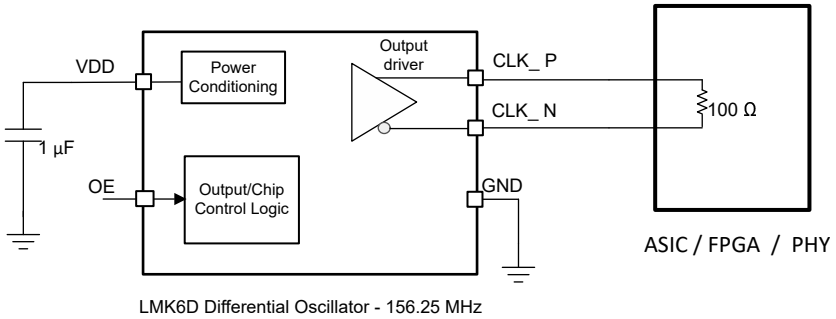


図 9-1. Application Example

9.2.1 Design Requirements

The LMK6x is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in the *Clock Output Interfacing and Termination* section closely. Refer to the *Function Pin(s)* section to understand the pin 1 and pin 2 functions, and order the part number as per your requirements for Output Enable (OE), Standby (ST) options.

9.2.2 Detailed Design Procedure

The LMK6x has three different options for differential output which are LVDS, LVPECL, HCSL type and one LVCMOS single-ended output type. For designing with the any of the oscillator output type in actual system, use the proper AC or DC termination based on the application requirement. Refer to the *Clock Output Interfacing and Termination* section for the details of all the AC and DC termination schemes and use the appropriate option. The figures in this section have all the AC and DC coupling options with the termination resistor values. The LMK6x has an integrated LDO and has excellent PSRR performance as shown in the *Electrical Characteristics* table. Refer to the LMK6EVM for the reference layout recommendation while designing the LMK6x BAW oscillator.

For the Function Pin 1 of LMK6C, connect typical 10-kΩ or less resistor to VDD for driving the OE pin High. Note this pin can be left open if you do not want to use pullup resistor as the device has > 100-kΩ internal pullup resistor. For driving the OE pin to Low, use the typical 10 kΩ or less resistor as a pulldown resistor. For the

Function Pin 1 or Functional Pin 2 for LMK6D, LMK6H, LMK6P, you can use the similar approach described for LMK6C.

9.2.3 Application Curves

The LMK6C LVCMOS output connects to different load capacitances based on the actual application use case in a system. With the different load capacitance, the rise time / fall time varies for the specific output frequency. The following graphs shows the Rise / Fall time for load capacitance of 2.2 pF, 4.7 pF, 10 pF, 15 pF and 22 pF for temperature range from –40°C to 105°C.

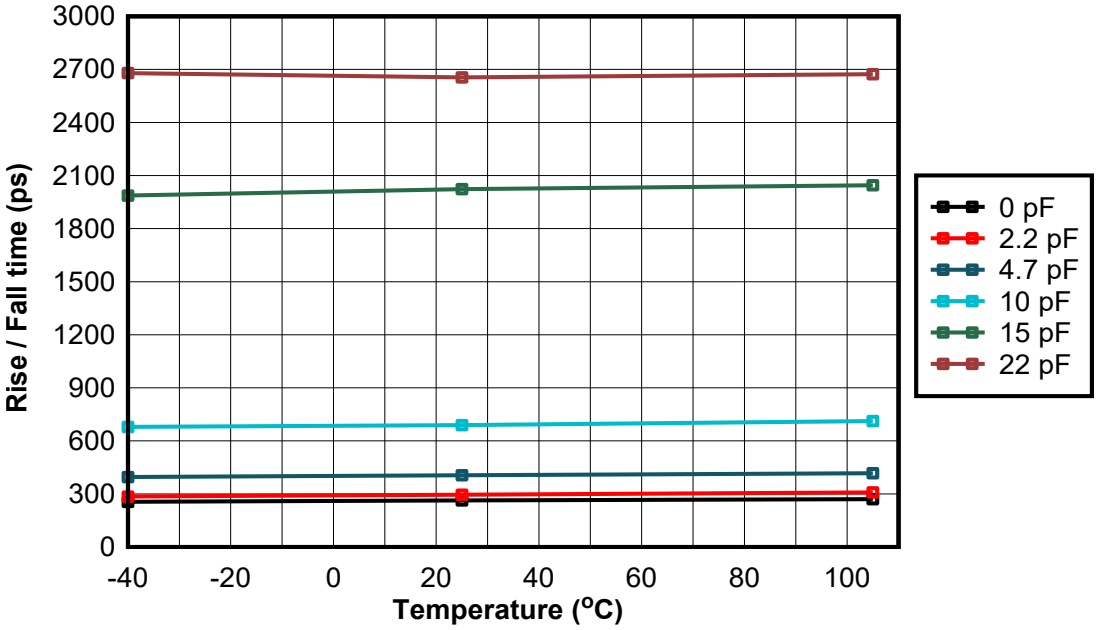


図 9-2. Rise / Fall time (ps) vs Temperature for 25-MHz Output Frequency, 3.3-V Supply

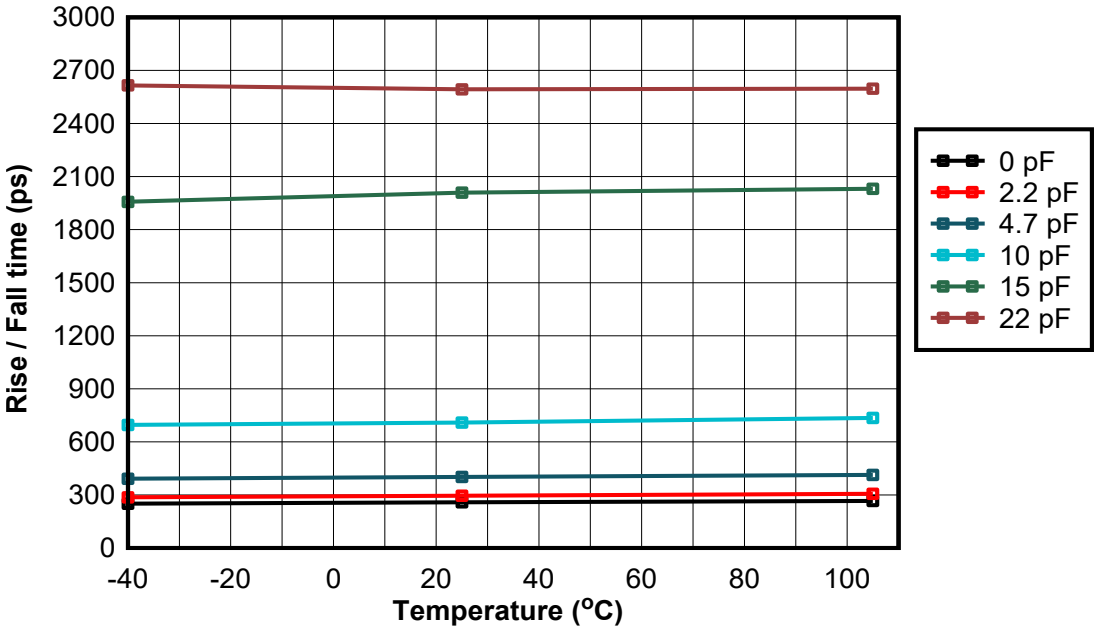


図 9-3. Rise / Fall time (ps) vs Temperature for 50-MHz Output Frequency, 3.3-V Supply

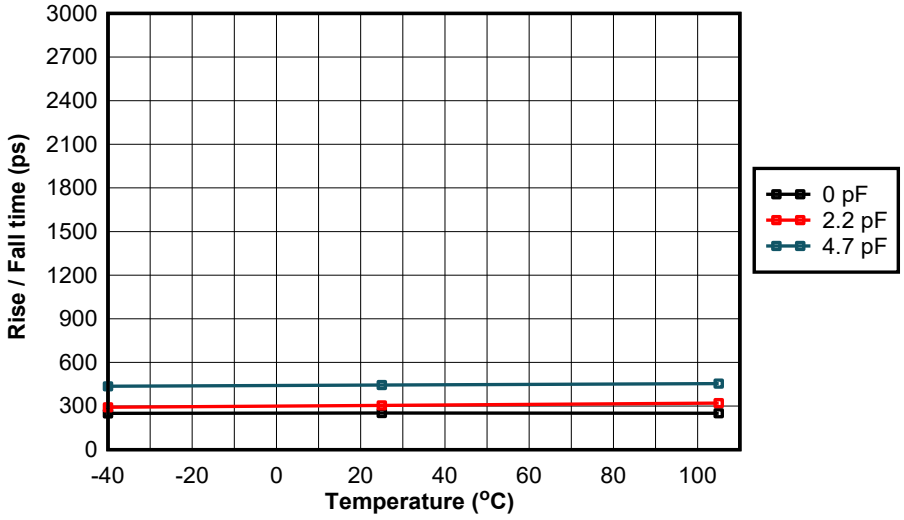


図 9-4. Rise / Fall time (ps) vs Temperature for 100-MHz Output Frequency, 3.3-V Supply

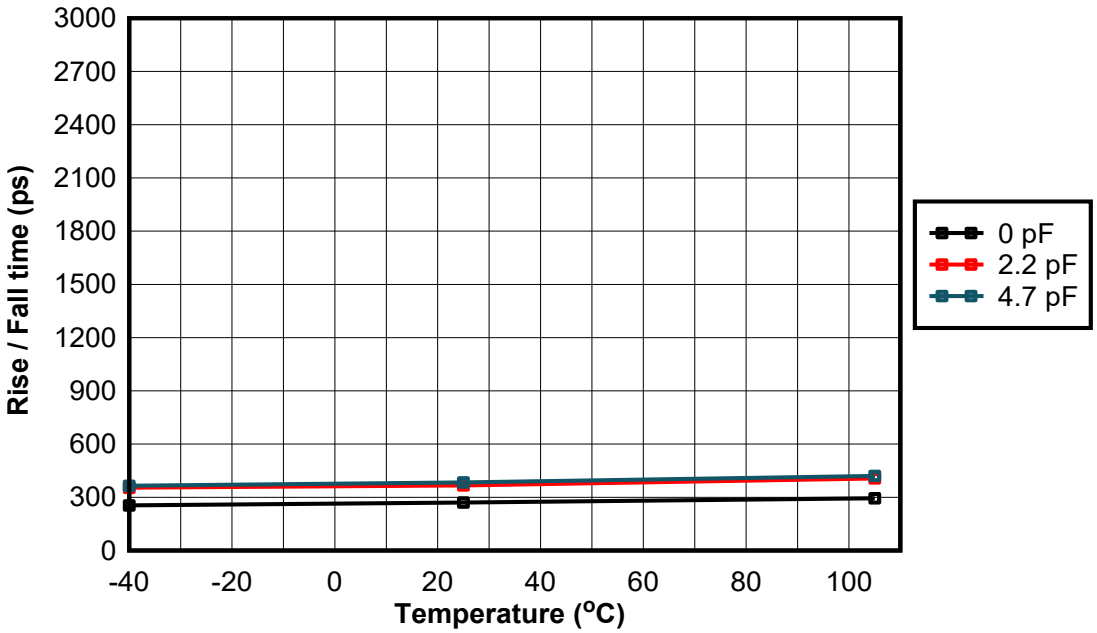


図 9-5. Rise / Fall time (ps) vs Temperature for 200-MHz Output Frequency, 3.3-V Supply

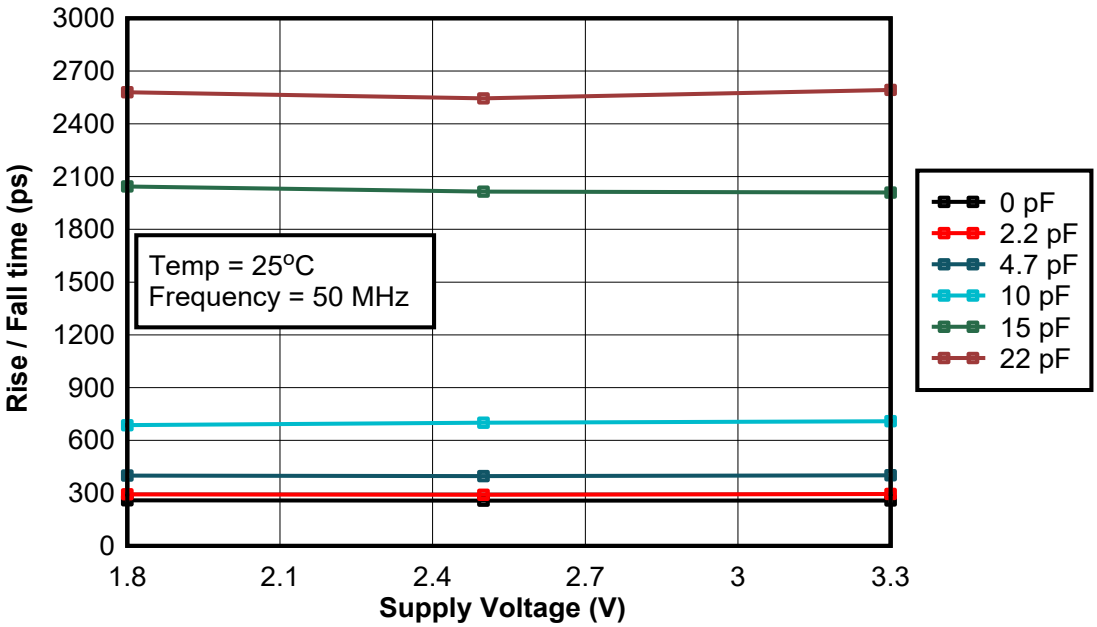


図 9-6. Rise / Fall time (ps) vs Supply Voltage vs Load Capacitance

9.3 Power Supply Recommendations

For the best electrical performance of the LMK6x, TI recommends use 1 µF capacitor on the device power supply bypass network. TI also recommends using component side mounting of the power-supply bypass capacitors, and best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

9.4 Layout

9.4.1 Layout Guidelines

The following sections provide recommendations for board layout, solder reflow profile and power-supply bypassing when using the LMK6x to ensure good thermal and electrical performance and signal integrity of the entire system.

9.4.1.1 Ensuring Thermal Reliability

The LMK6x is a high-performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

The equation below describes the relationship between the PCB temperature around the LMK6x and its junction temperature.

$$T_B = T_J – \Psi_{JB} \times P \quad (1)$$

where

- T_B: PCB temperature around the LMK6x
- T_J: Junction temperature of LMK6x
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK6x (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- P: On-chip power dissipation of LMK6x

9.4.1.2 Recommended Solder Reflow Profile

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK6x to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

9.4.2 Layout

Refer to the *LMK6EVM User's Guide* for printed circuit board layout examples for LMK6D, LMK6H, LMK6P and LMK6C devices. The figured below show the PCB layout example as done on the evaluation module for the LMK6x EVM.

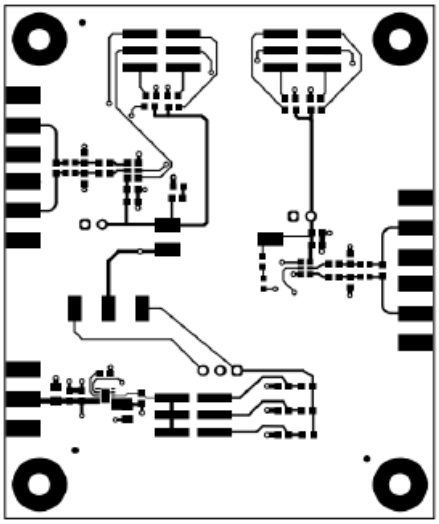


図 9-7. PCB Layout Example From LMK6 EVM - Top Layer

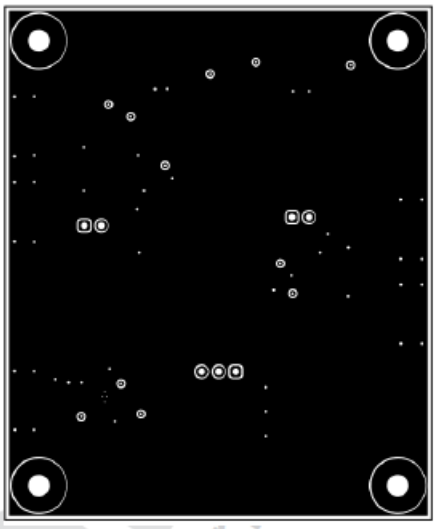


図 9-8. PCB Layout Example From LMK6 EVM - GND Layer 1

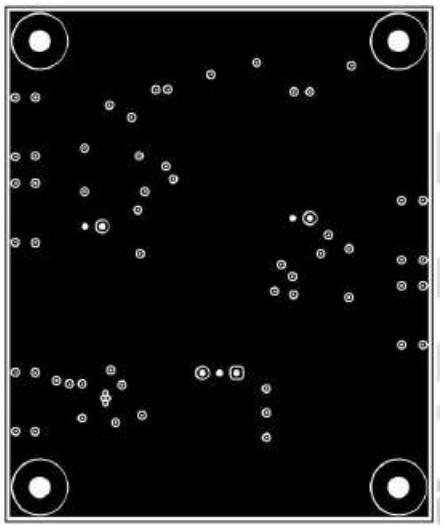


図 9-9. PCB Layout Example From LMK6 EVM - GND Layer 2

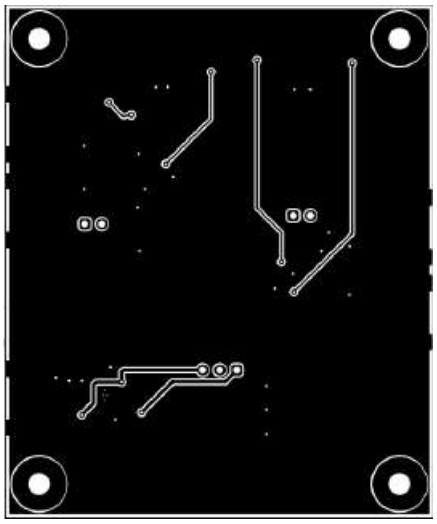


図 9-10. PCB Layout Example From LMK6 EVM - Bottom Layer

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMK6EVM User's Guide*
- Texas Instruments, *Standalone BAW Oscillators Advantages Over Quartz Oscillators application note*
- Texas Instruments, *BAW oscillator solutions for Building Automation application note*
- Texas Instruments, *BAW oscillator solutions for Factory Automation application note*
- Texas Instruments, *BAW oscillator solutions for Grid Infrastructure application note*
- Texas Instruments, *BAW oscillator solutions for Optical Modules application note*

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

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10.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (February 2023) to Revision E (January 2024)	Page
• 標準周波数のリストに値を追加	1
• Changed the part number guides in the *Device Ordering Information* section	3

Changes from Revision C (December 2022) to Revision D (February 2023)	Page
• Changed the NO. column to DLE/DLF in the *Pin Functions* table for the DLF package release	5

Changes from Revision B (November 2022) to Revision C (December 2022) **Page**

- データシートのステータスを「事前情報」から「量産データ」に変更 1
- LMK6D、LMK6H、LMK6P デバイスからプレビューの注を削除 1

12 Mechanical, Packaging, and Orderable Information

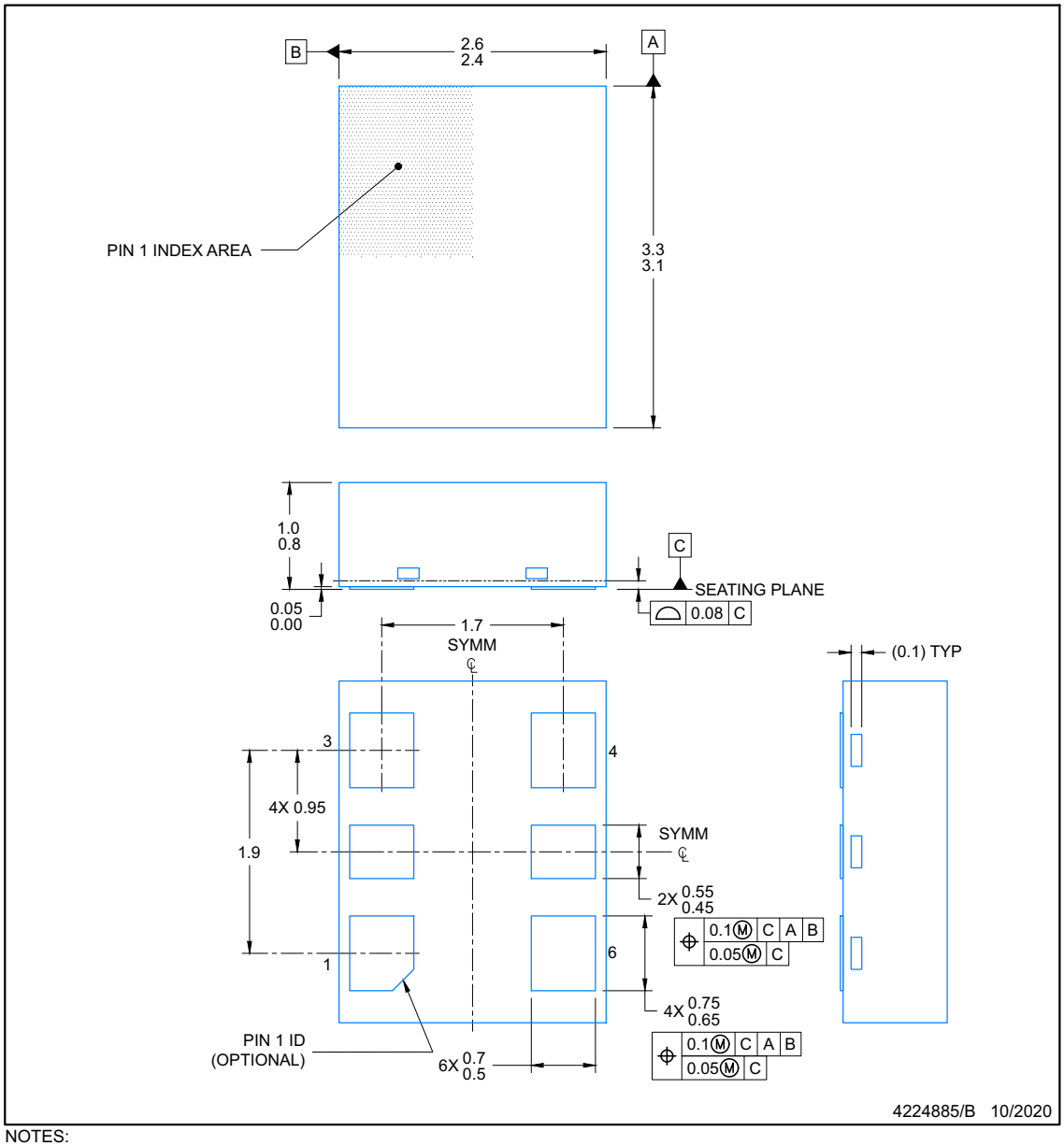
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DLE0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

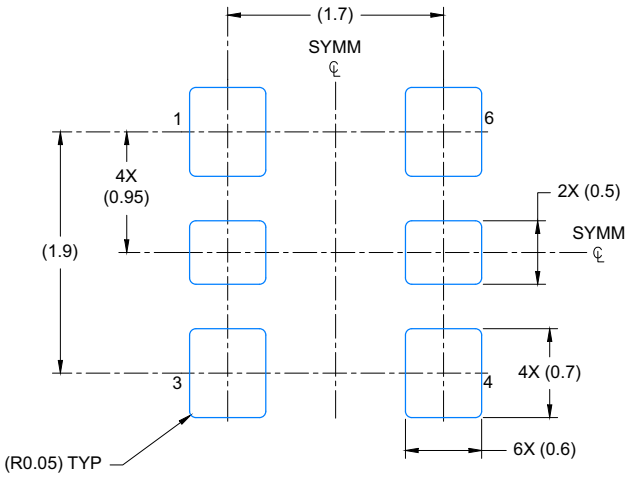
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

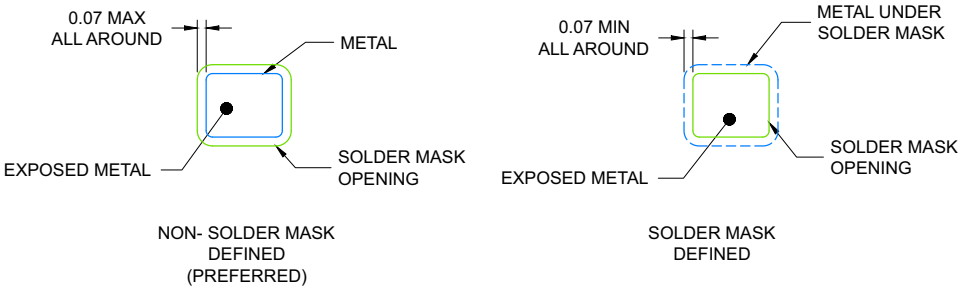
DLE0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224885/B 10/2020

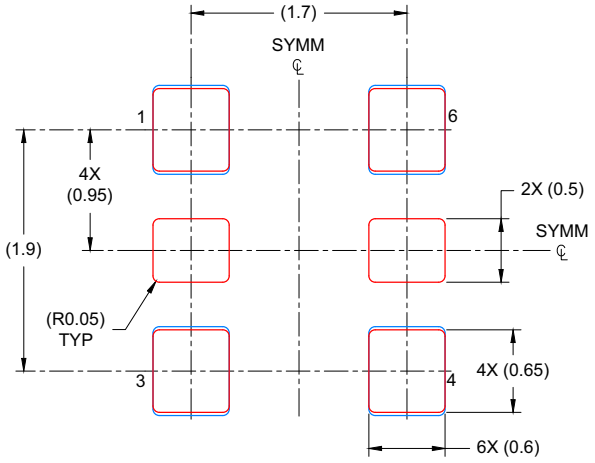
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLE0006A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 93%
SCALE: 20X

4224885/B 10/2020

NOTES: (continued)

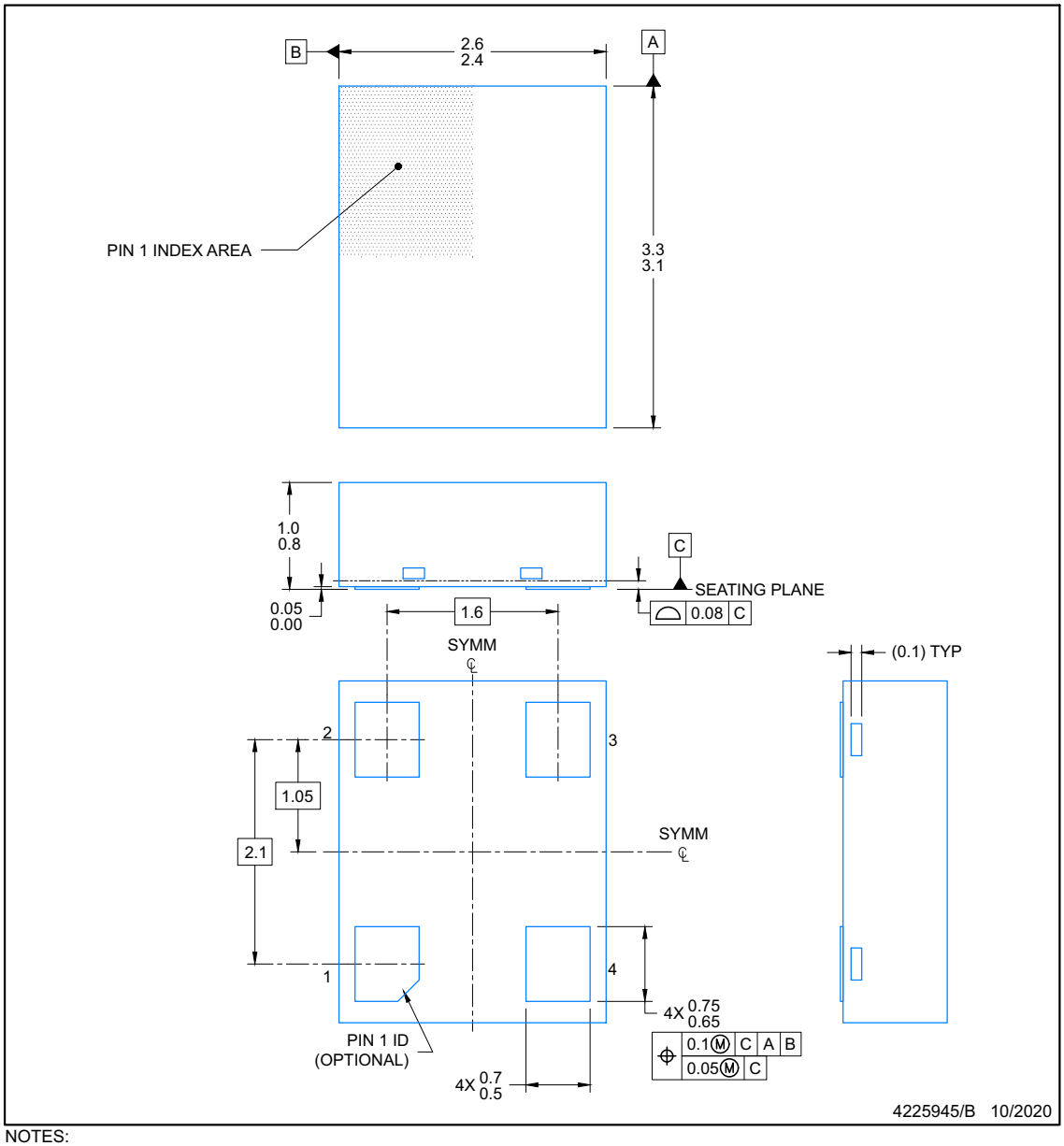
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLE0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



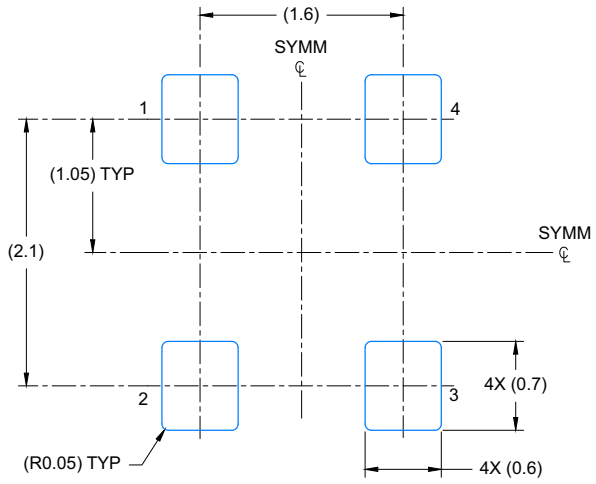
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

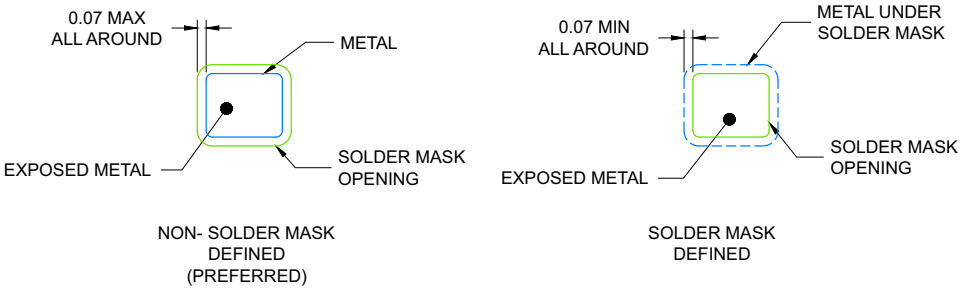
EXAMPLE BOARD LAYOUT

DLE0004A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225945/B 10/2020

NOTES: (continued)

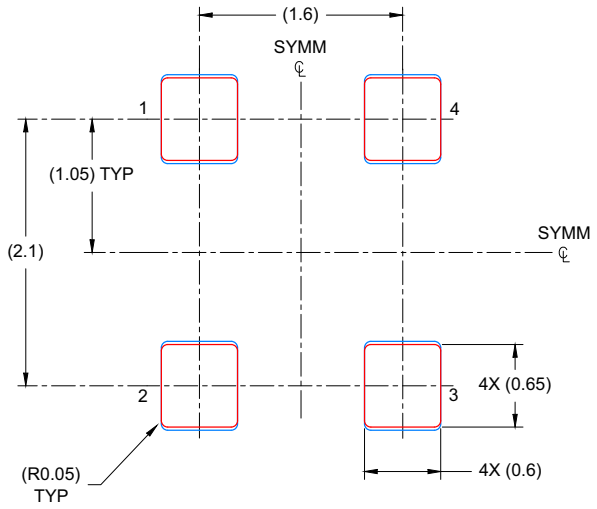
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLE0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 93%
SCALE: 20X

4225945/B 10/2020

NOTES: (continued)

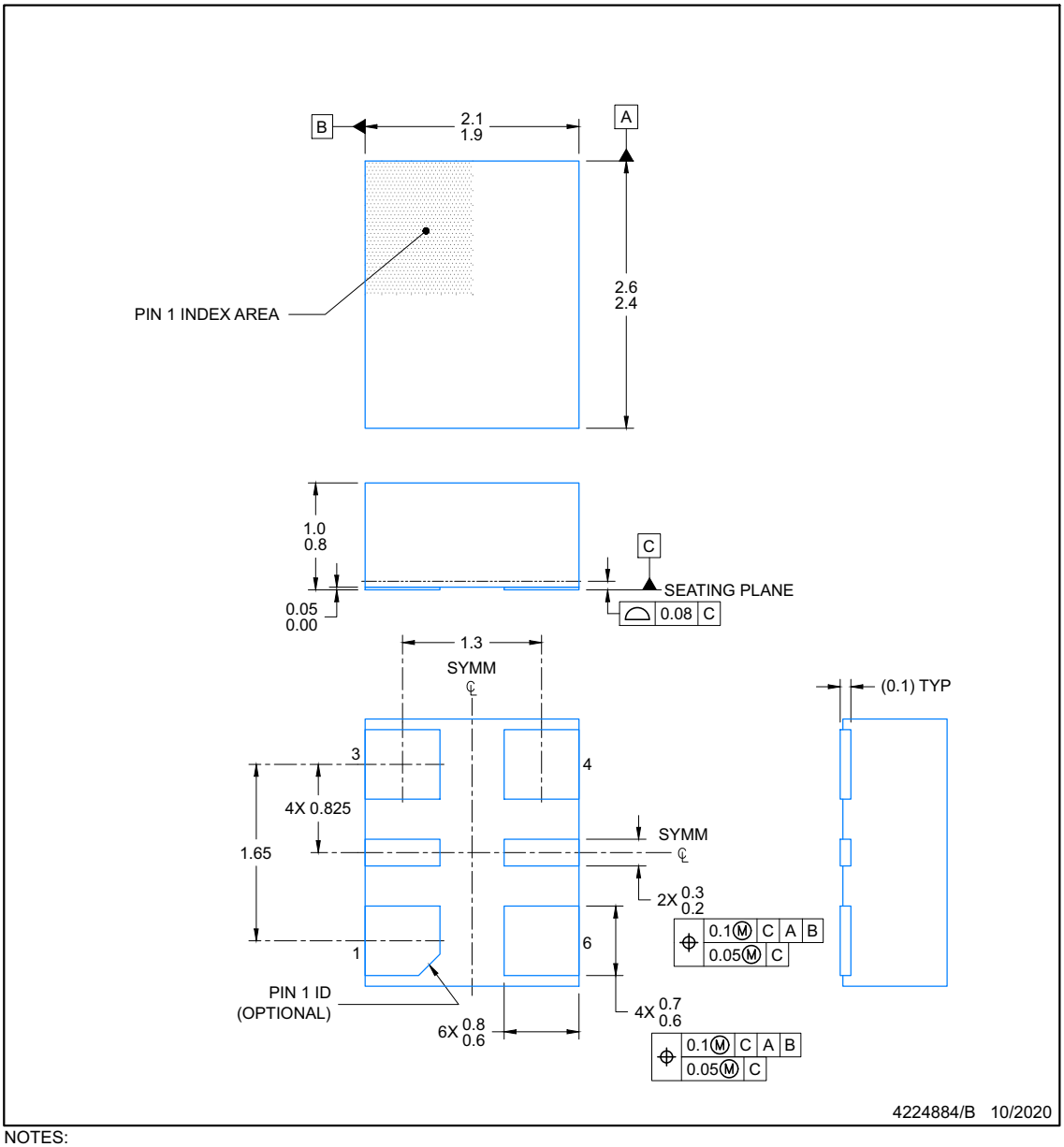
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

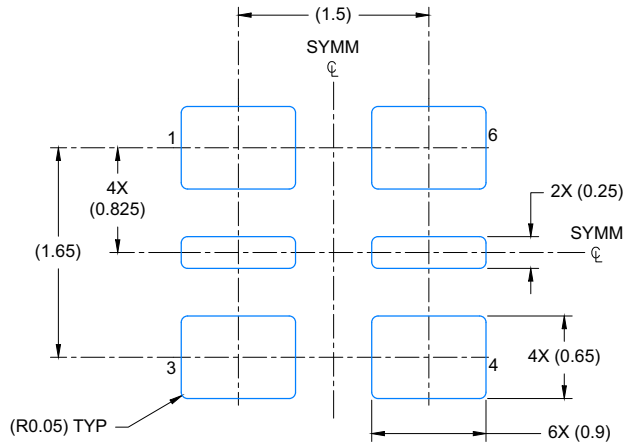
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

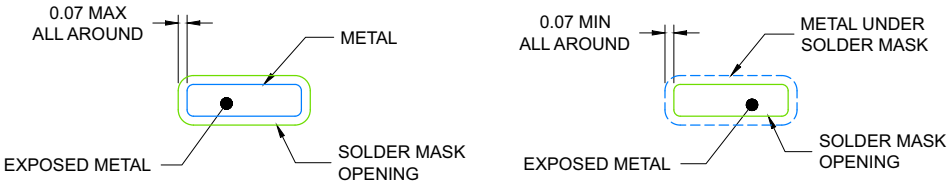
DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224884/B 10/2020

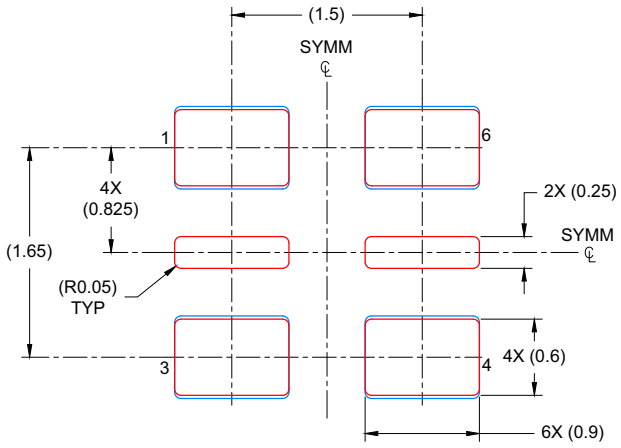
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLF0006A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4224884/B 10/2020

NOTES: (continued)

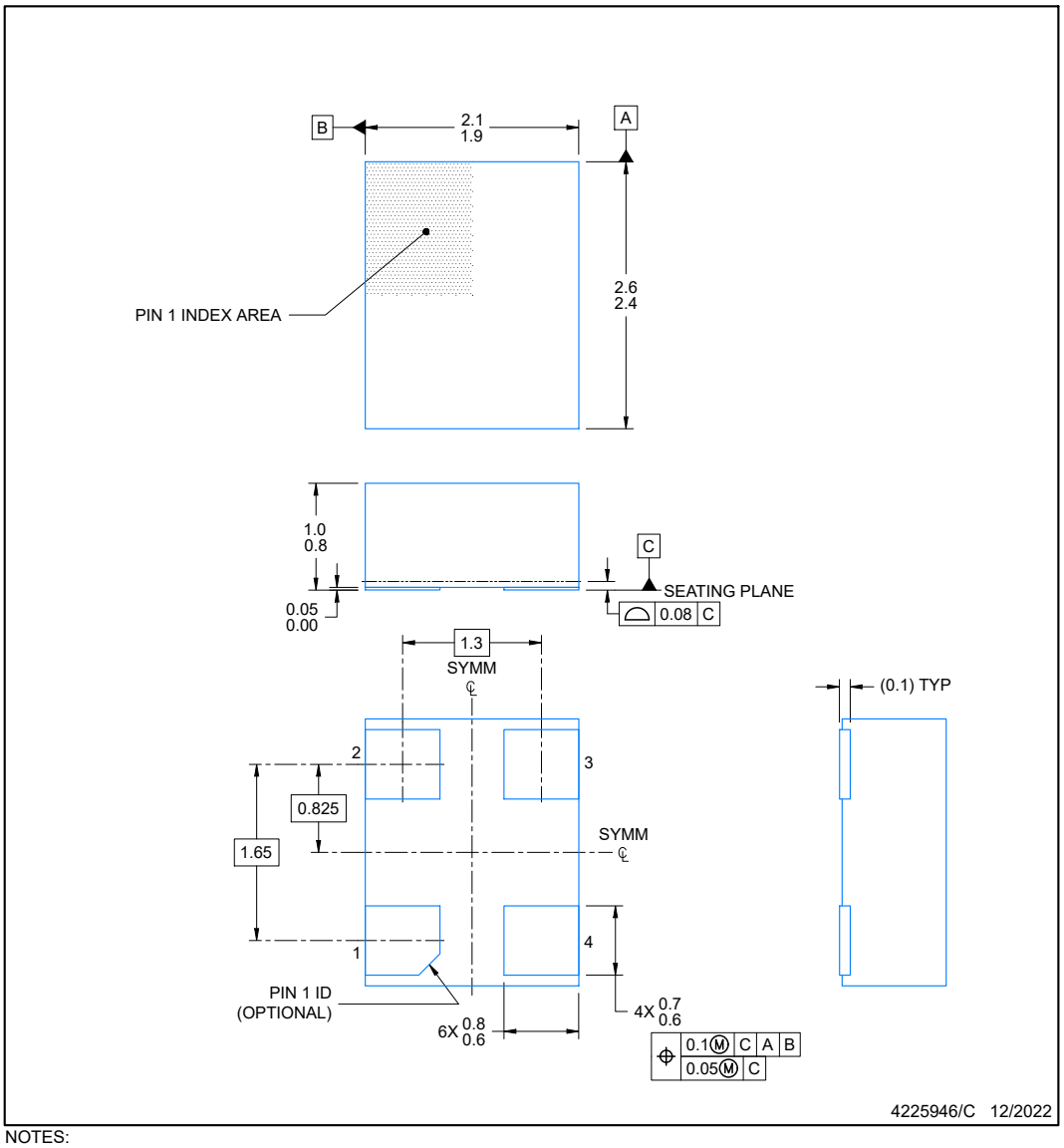
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLF0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



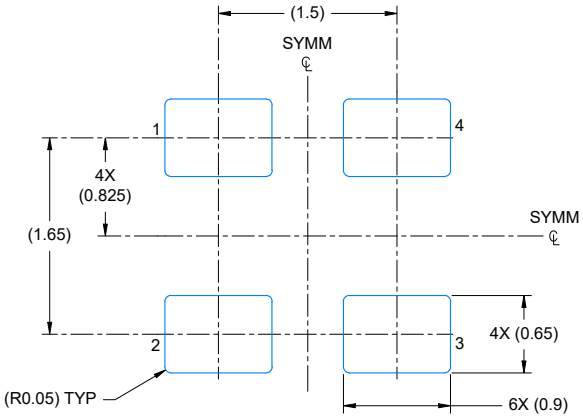
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

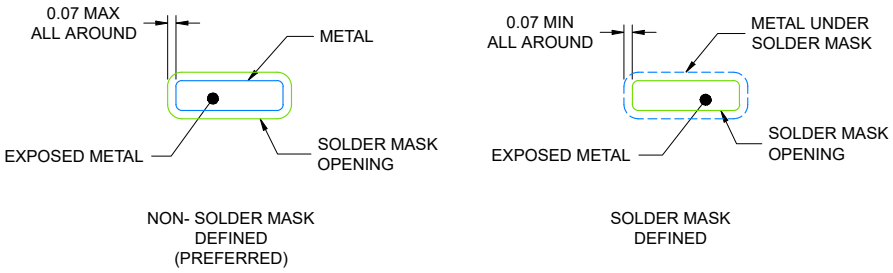
EXAMPLE BOARD LAYOUT

DLF0004A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225946/C 12/2022

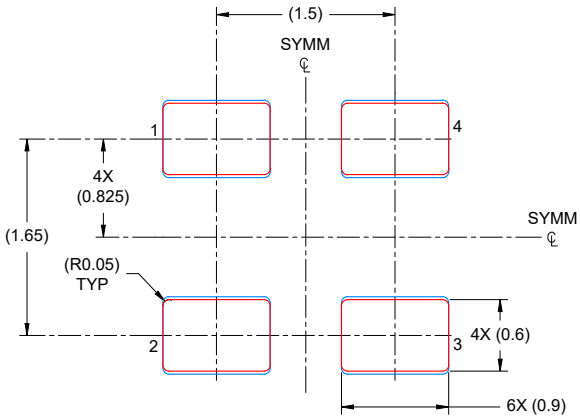
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLF0004A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4225946/C 12/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6CE012288CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBJ	Samples
LMK6CE012288CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBJ	Samples
LMK6CE02500CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBG	Samples
LMK6CE02500CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBG	Samples
LMK6CE02500DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1G	Samples
LMK6CE02500DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1G	Samples
LMK6CE03333CDLER	ACTIVE	VSON	DLE	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB8	Samples
LMK6CE03333CDLET	ACTIVE	VSON	DLE	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB8	Samples
LMK6CE04000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB6	Samples
LMK6CE04000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB6	Samples
LMK6CE04800DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1C	Samples
LMK6CE04800DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1C	Samples
LMK6CE05000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCCB	Samples
LMK6CE05000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCCB	Samples
LMK6CE07425DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC19	Samples
LMK6CE07425DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC19	Samples
LMK6CE10000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB8	Samples
LMK6CE10000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB8	Samples
LMK6CE10000DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC18	Samples
LMK6CE10000DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC18	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6CE12500CDLER	ACTIVE	VSON	DLE	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB6	Samples
LMK6CE12500CDLET	ACTIVE	VSON	DLE	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB6	Samples
LMK6CE15625DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC12	Samples
LMK6CE15625DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC12	Samples
LMK6DA05184ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDAH	Samples
LMK6DA05184ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDAH	Samples
LMK6DA10000ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA8	Samples
LMK6DA10000ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA8	Samples
LMK6DA12288ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA4	Samples
LMK6DA12288ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA4	Samples
LMK6DA12500ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA6	Samples
LMK6DA12500ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA6	Samples
LMK6DA15552ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA3	Samples
LMK6DA15552ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA3	Samples
LMK6DA15625ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA2	Samples
LMK6DA15625ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA2	Samples
LMK6DA20000ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA1	Samples
LMK6DA20000ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA1	Samples
LMK6DA31250ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA0	Samples
LMK6DA31250ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDA0	Samples
LMK6DA40000ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDAM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6DA40000ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LDAM	Samples
LMK6HA10000ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000BDLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH18	Samples
LMK6HA10000BDLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH18	Samples
LMK6HA15625ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA2	Samples
LMK6HA15625ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA2	Samples
LMK6HE40000ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LHGM	Samples
LMK6HE40000ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LHGM	Samples
LMK6PA15625ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
PLMK6DA15625ADLET	ACTIVE	VSON	DLE	6	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

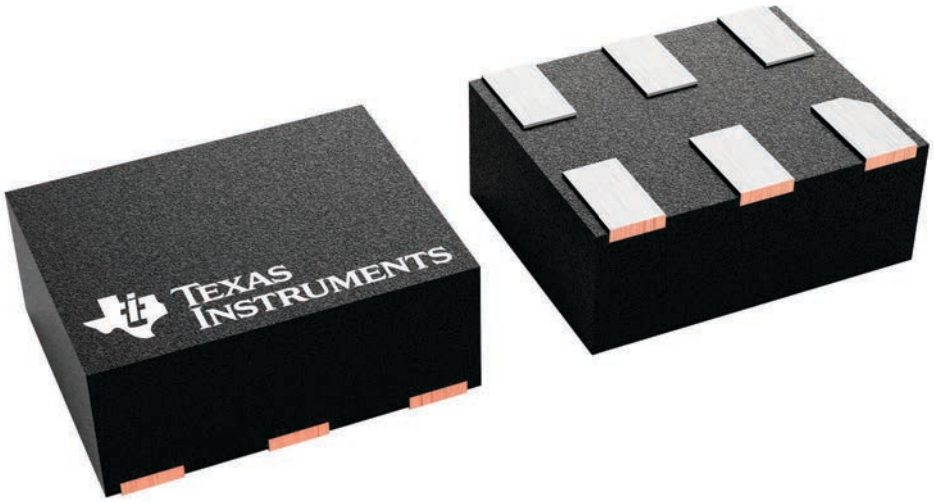
DLF 6

VSON - 1 mm max height

2 x 2.5, multiple pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



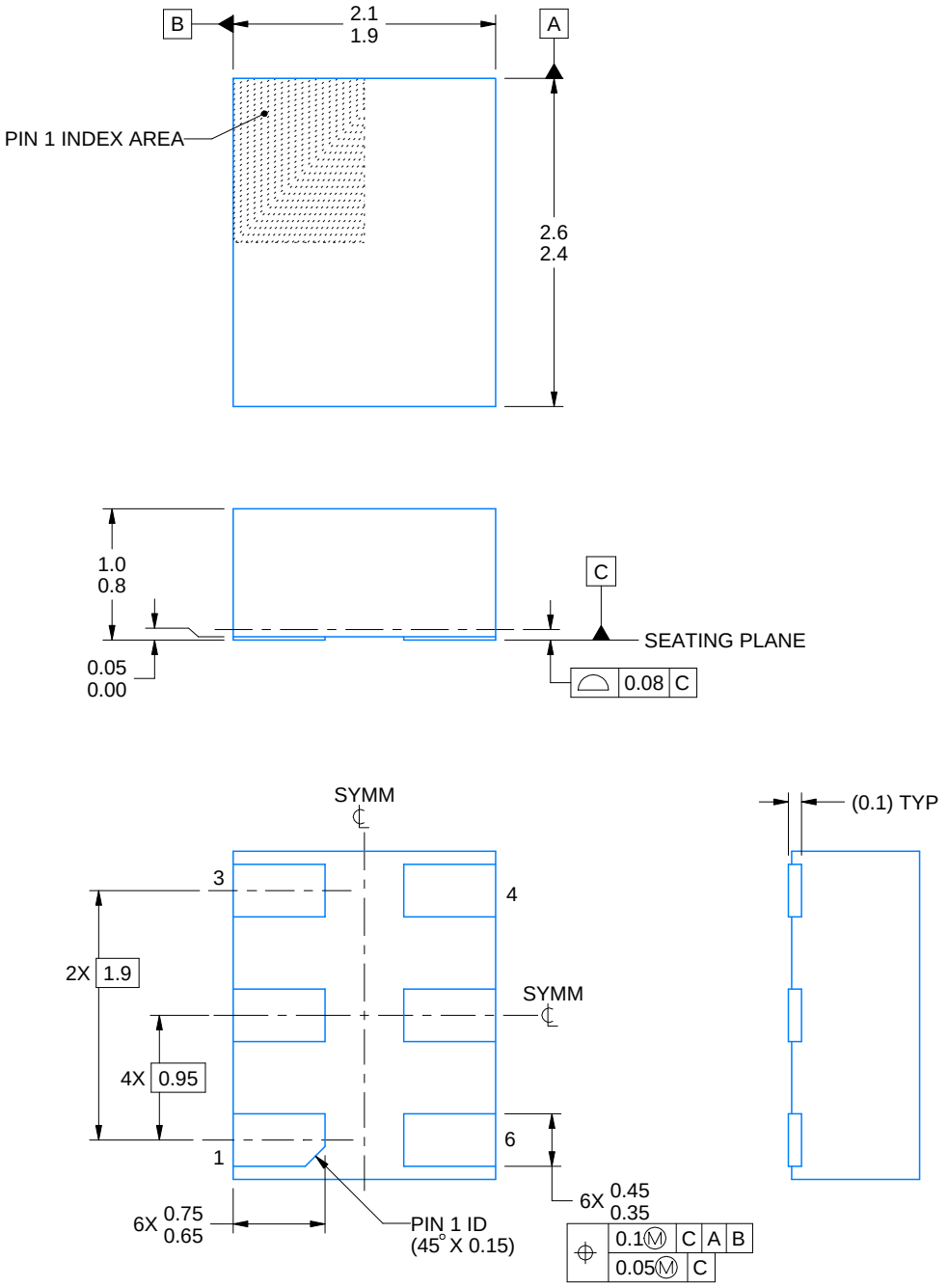
4229715/A

DLF0006B

PACKAGE OUTLINE

VSON - 1 mm max height

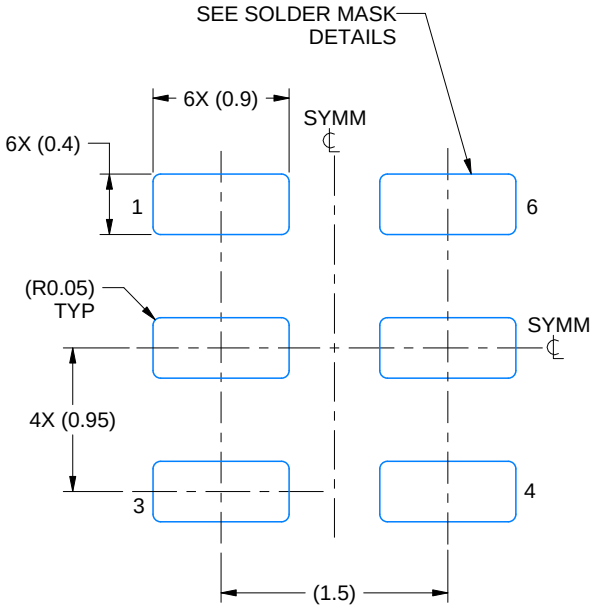
PLASTIC SMALL OUTLINE - NO LEAD



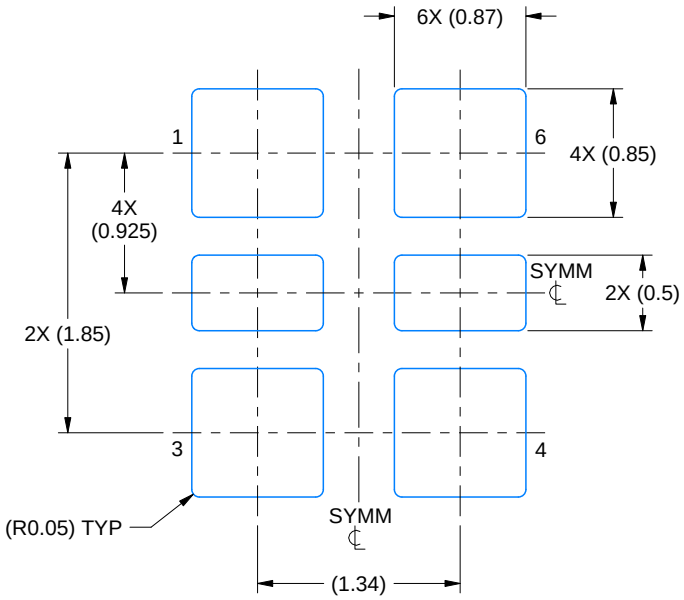
4229693/B 12/2023

NOTES:

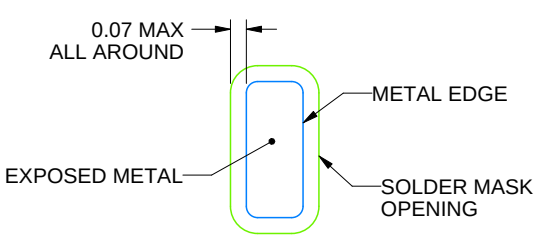
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



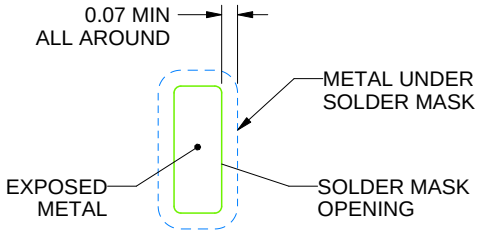
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4229693/B 12/2023

NOTES: (continued)

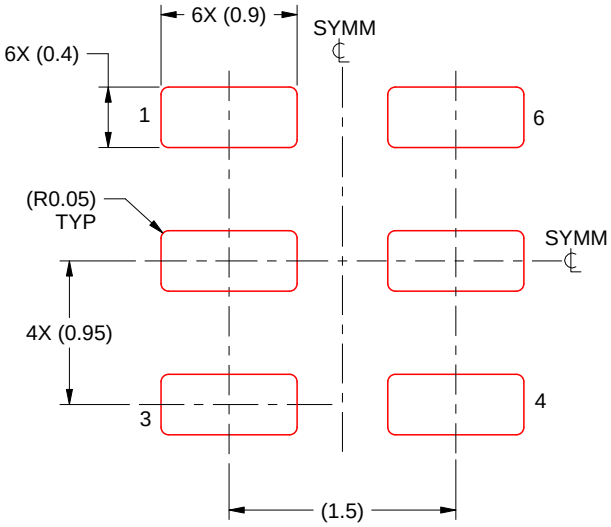
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

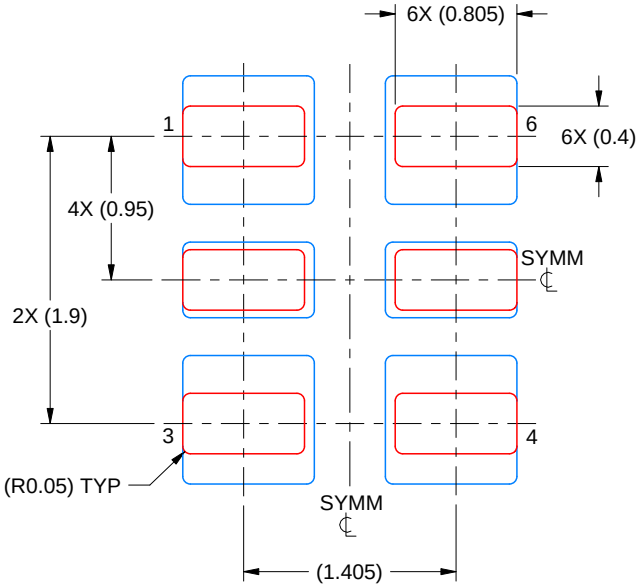
DLF0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK
STENCILSCALE 20.000

4229693/B 12/2023

NOTES: (continued)

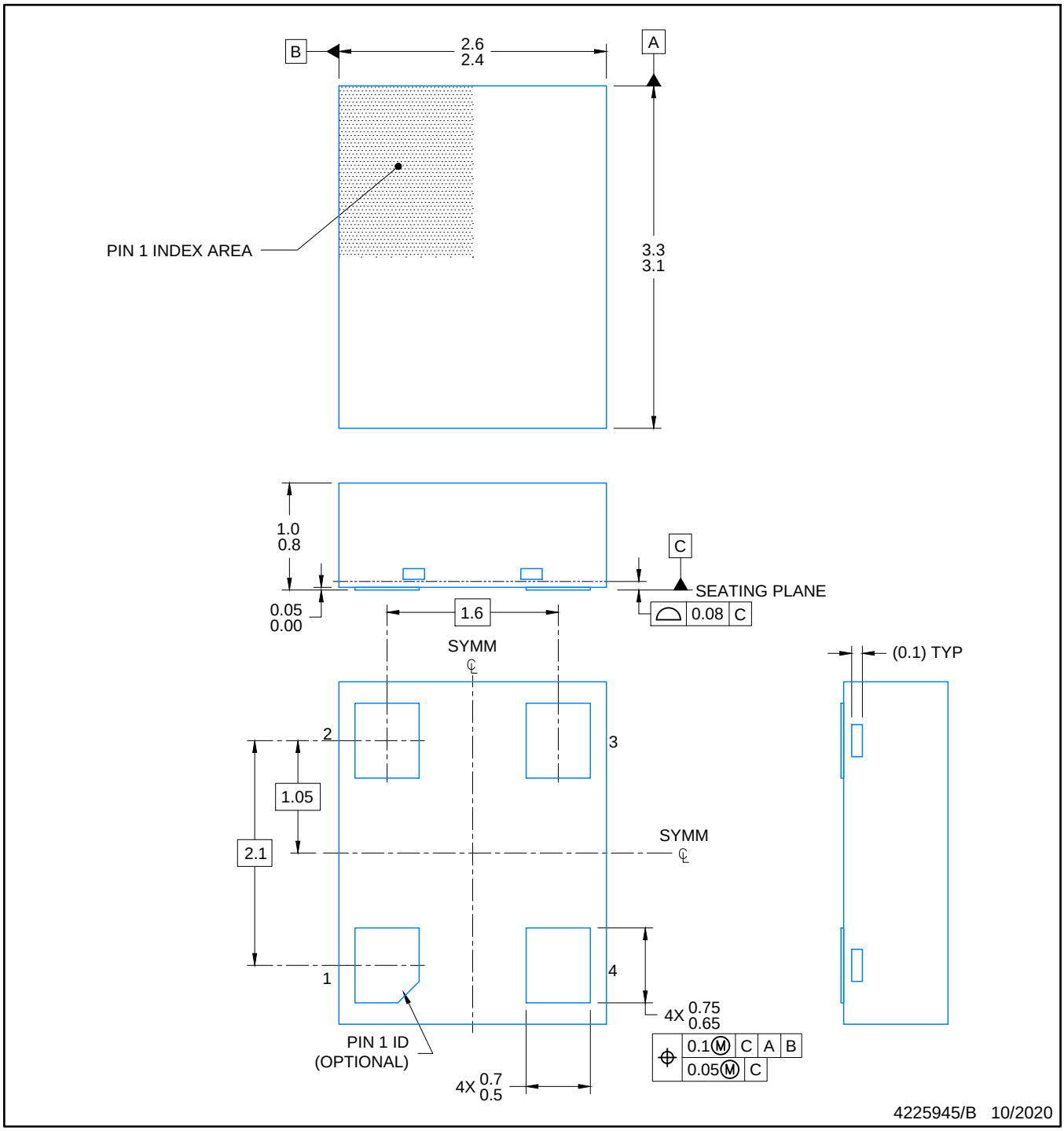
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLE0004A

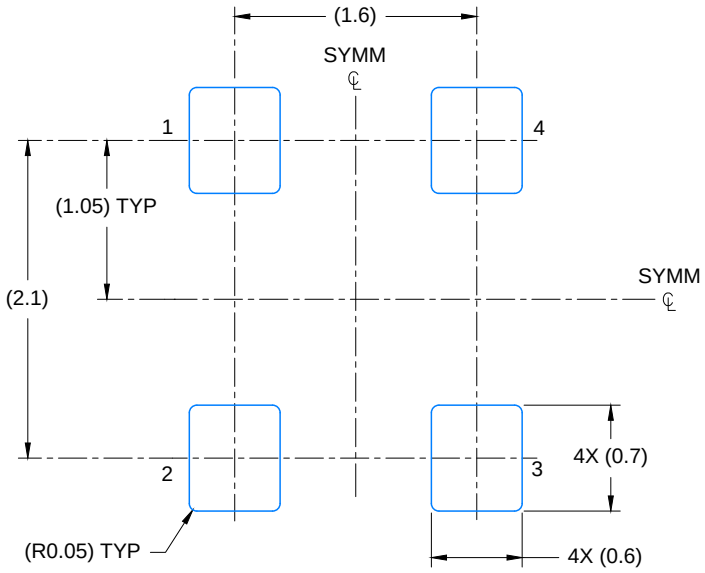
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

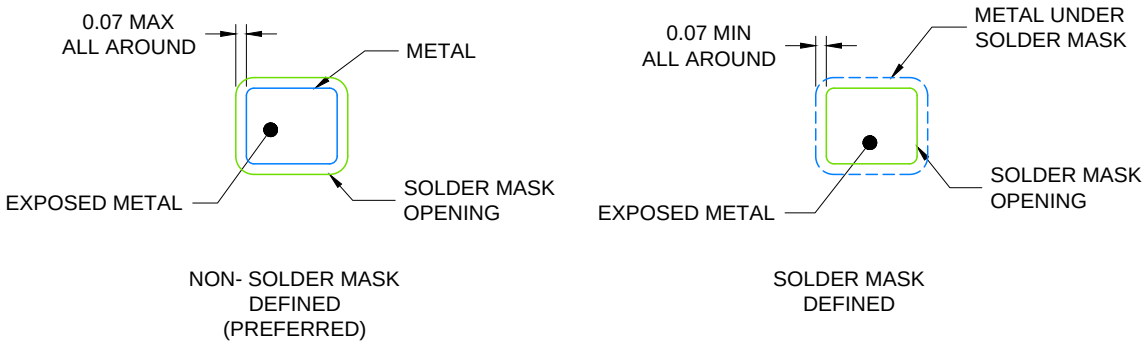


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

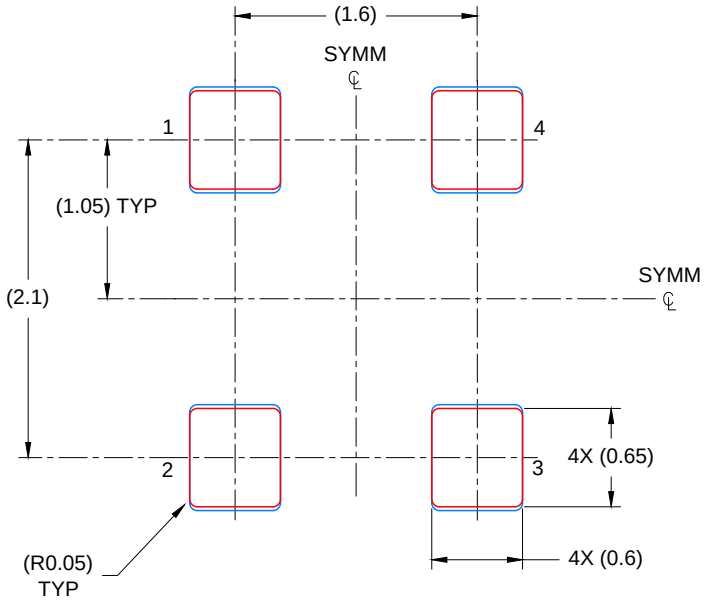


SOLDER MASK DETAILS

4225945/B 10/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 93%
SCALE: 20X

4225945/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

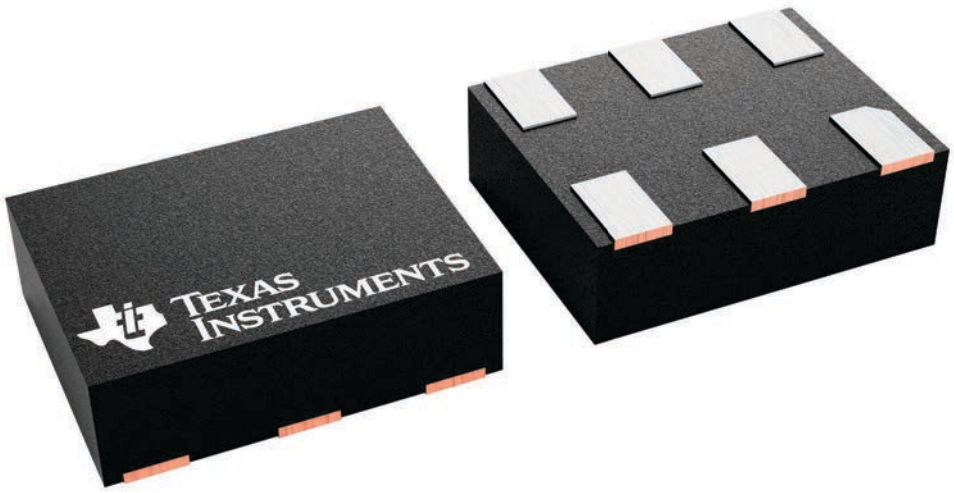
DLE 6

VSON - 1 mm max height

2.5 x 3.2, multiple pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



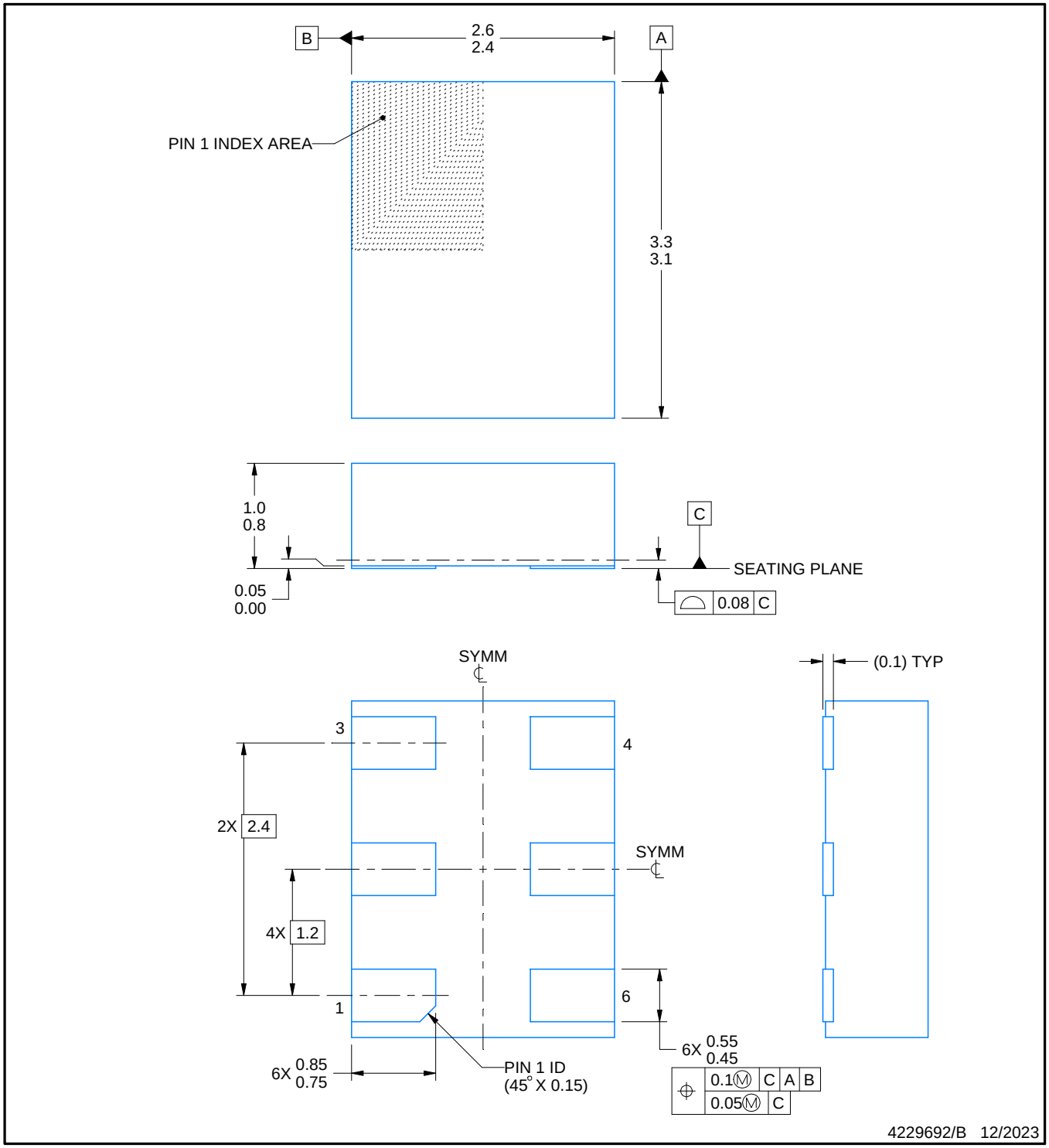
4229714/A

DLE0006B

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

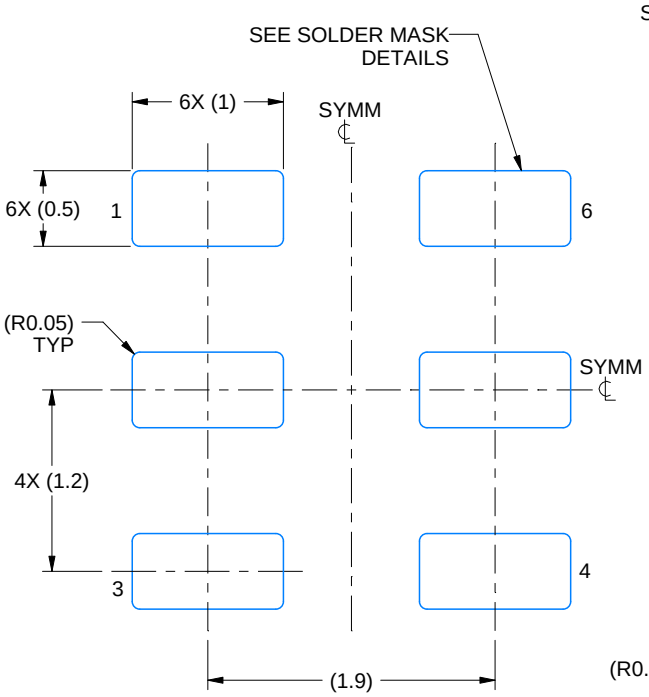
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

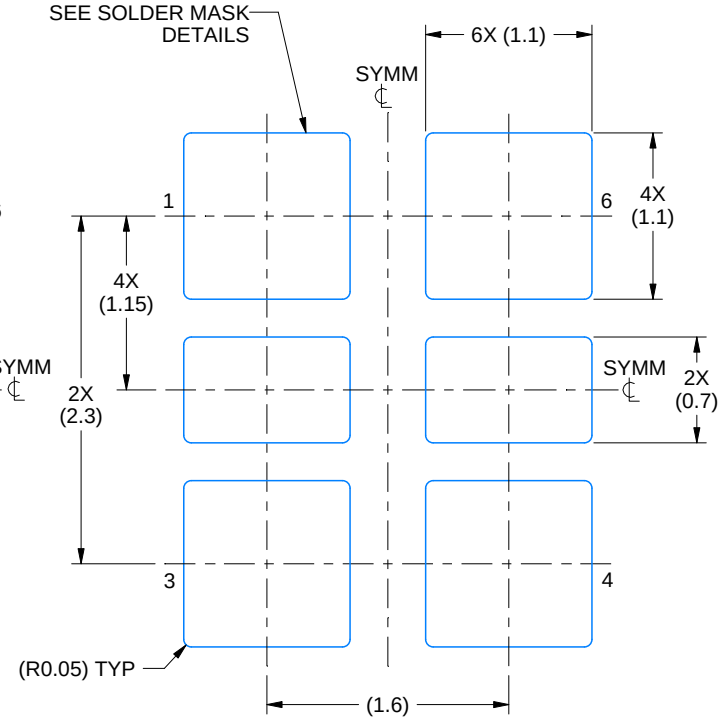
DLE0006B

VSON - 1 mm max height

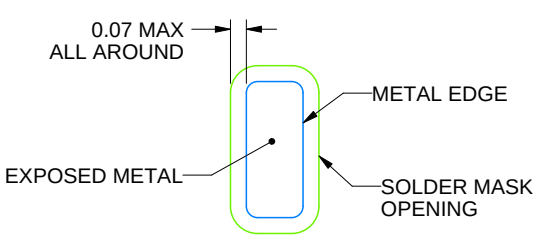
PLASTIC SMALL OUTLINE - NO LEAD



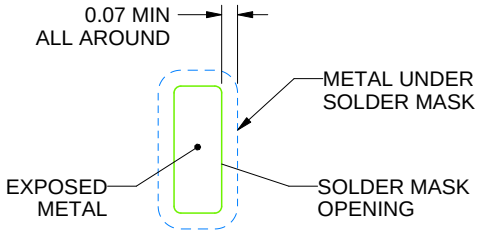
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



UNIVERSAL LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED
(PREFERRED)



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4229692/B 12/2023

NOTES: (continued)

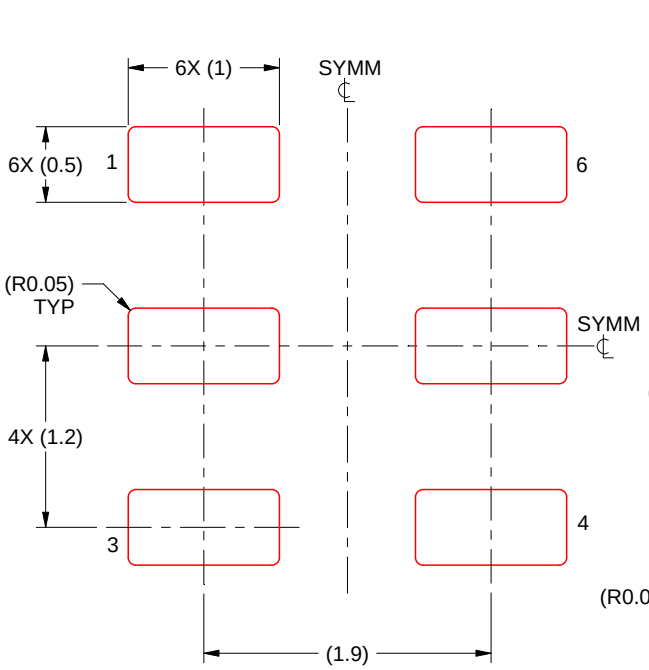
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

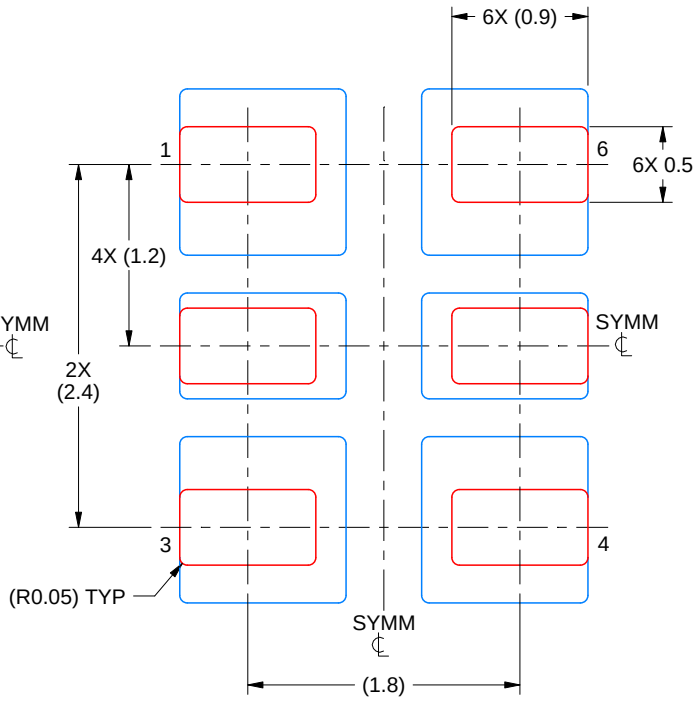
DLE0006B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X



UNIVERSAL SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229692/B 12/2023

NOTES: (continued)

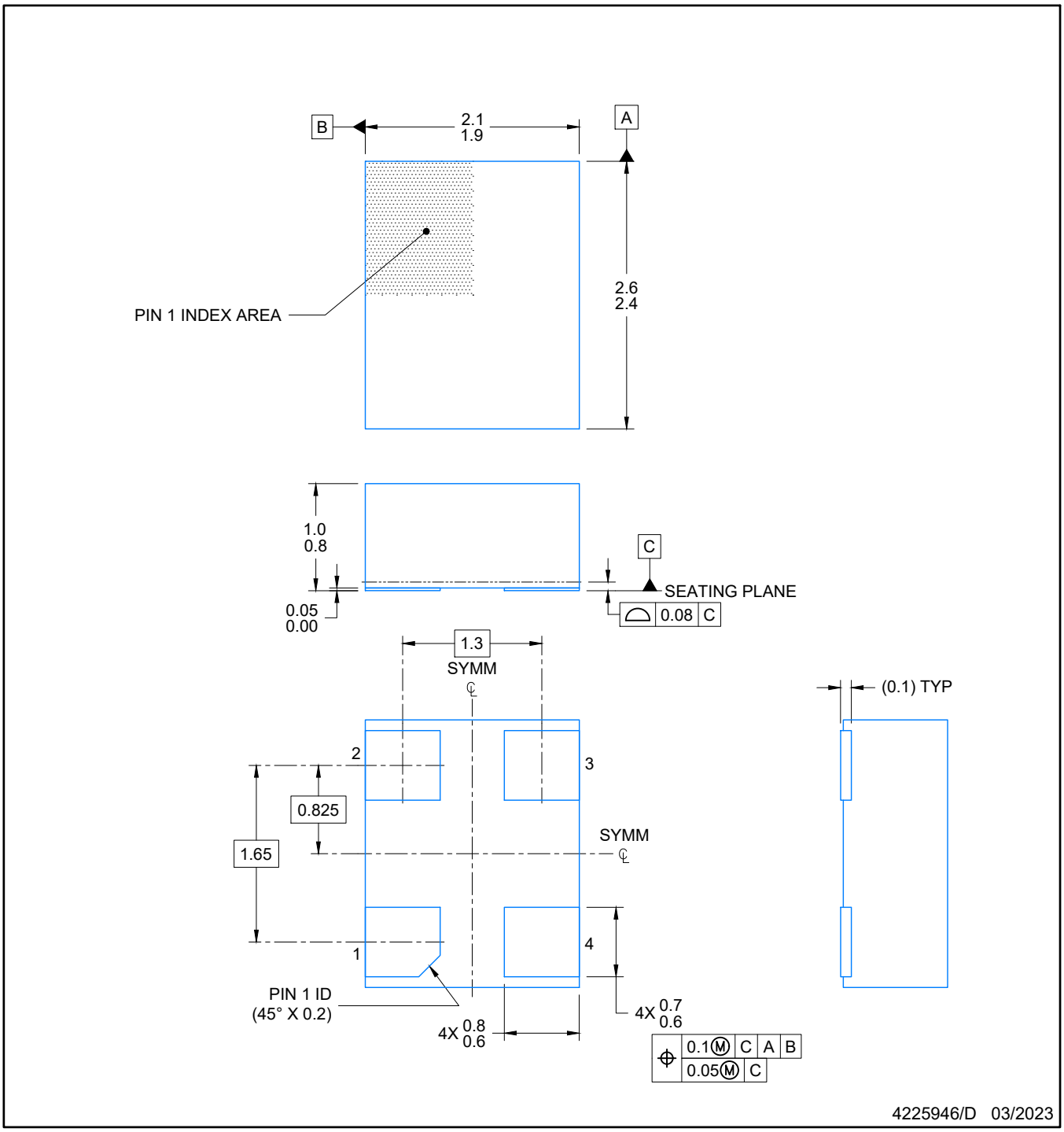
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLF0004A

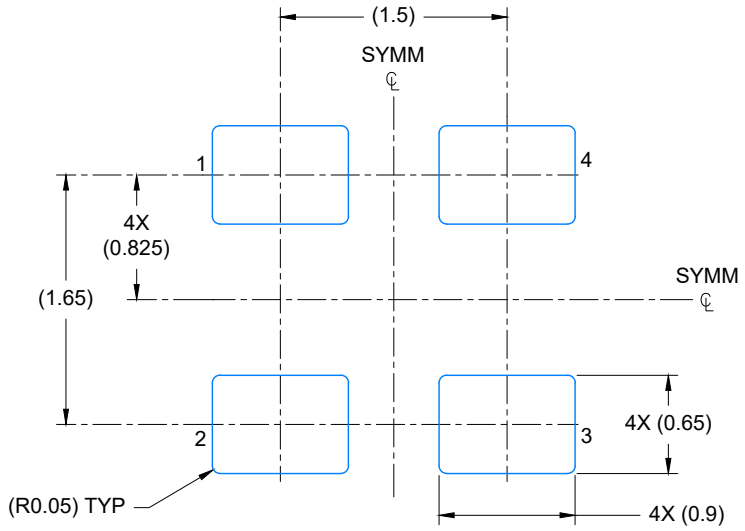
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

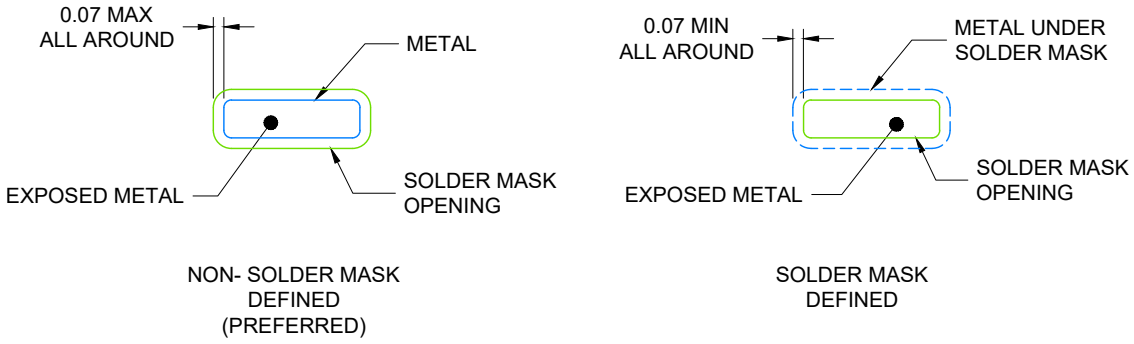


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

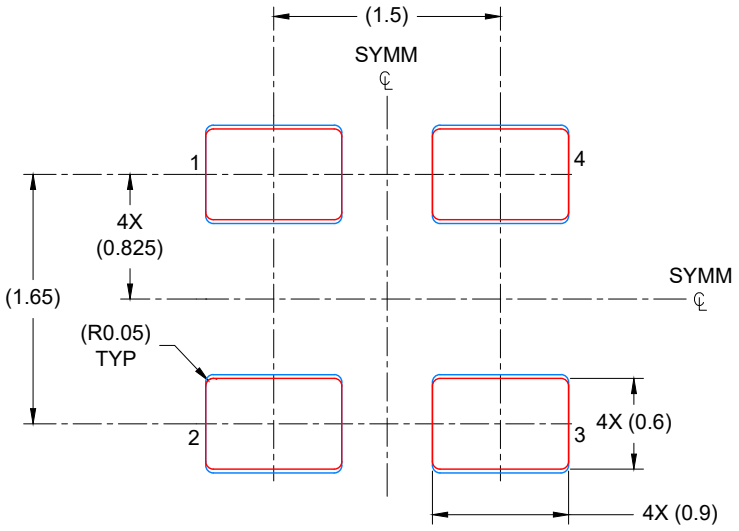


SOLDER MASK DETAILS

4225946/D 03/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4225946/D 03/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265